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Dual Isolated Half-Duplex RS-485 Repeater

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Circuit Description

This reference design demonstrates a dual isolated, half-duplex repeater with data rate independent flow-control for long-haul RS-485 networks. The design provides transient protection protecting the signal path against ESD, EFT, and surge transients specified in the IEC 61000 family of transient immunity standards.

Isolated DC-DC converters provide power supply across the isolation barriers utilizing the push-pull converter principle.

Design Resources

Design Archive	All Design Files
ISO3082	Product Folder
SN6501	Product Folder
TPS76350	Product Folder
SN74LVC2G14	Product Folder

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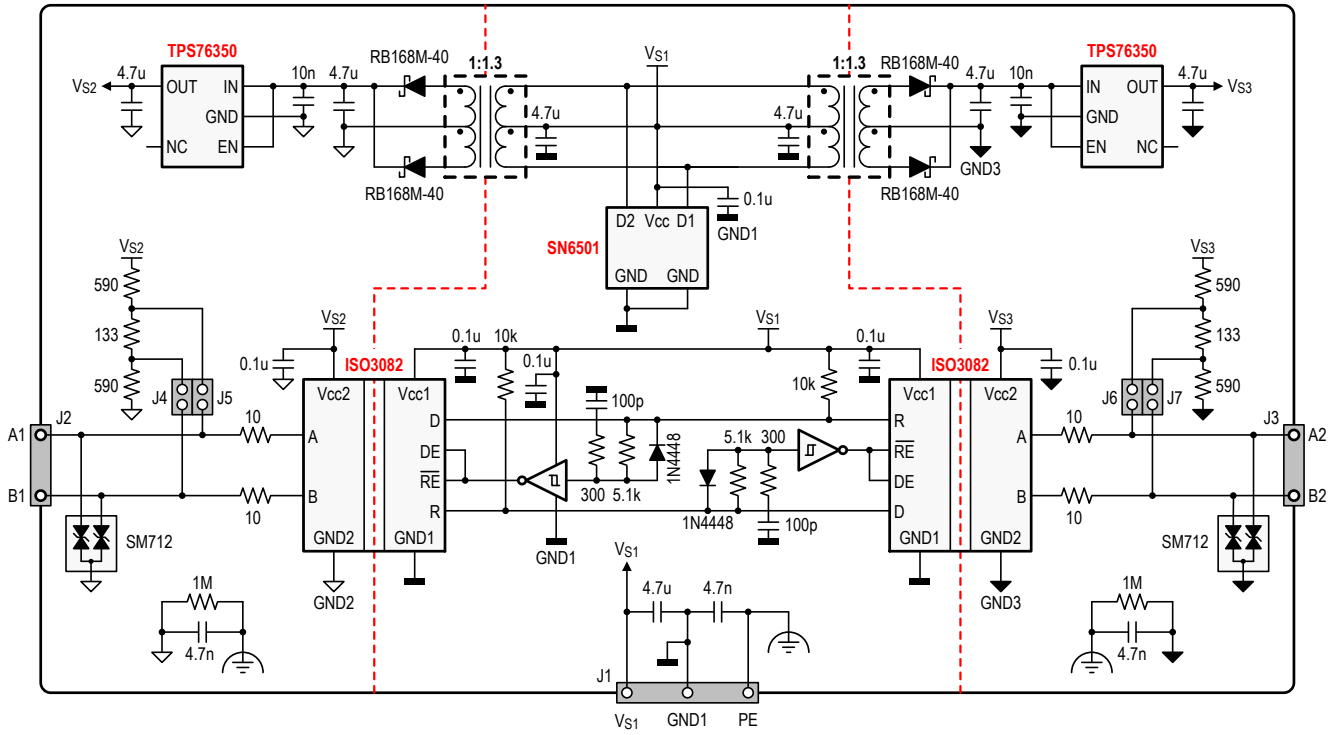

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1 Design Summary

1.1 Overview

Industrial long-haul networks comprise two or more long distance bus segments. Data transmission occurs in half-duplex mode to support two-wire twisted pair installations assuring low cable and wiring cost. Data rates are in the lower tens of kilo-bits-per-second (kbps). Due to signal degradation across long transmission distance, recovery and regeneration of the bus signal is required. In addition large ground potential differences (GPDs) between remote bus nodes make galvanic isolation of supply and signal path a necessity for each node. The dual isolated half-duplex repeater in Figure 1 satisfies all of the above requirements.

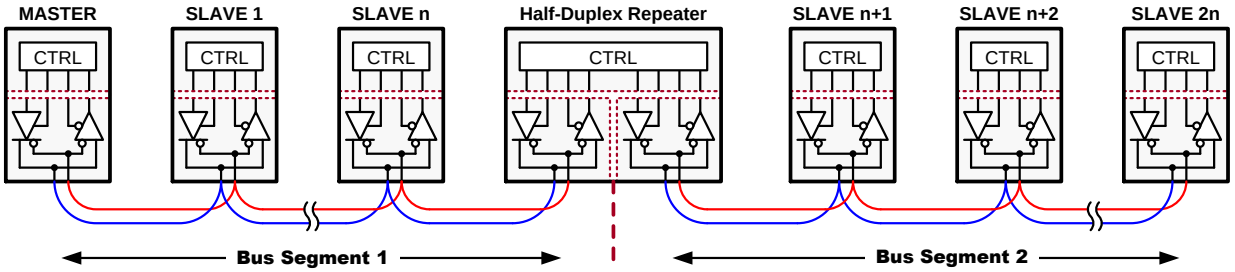

Figure 1. Simplified diagram of a two-segment long-haul network

1.2 Features

The half-duplex repeater in this reference design provides the following features:

- Data rate up to 100kbps
- Data rate independent flow control
- 4kV peak isolation
- IEC 61000-4-2 up to 16kV
- IEC 61000-4-4 up to 4kV
- IEC 61000-4-5 up to 1kV

2 Design Considerations

To support bidirectional data traffic the half-duplex repeater utilizes two isolated transceivers. Additional logic circuitry provides data rate independent flow control.

2.1 Isolated Transceiver

The ISO3082 is an isolated, half-duplex differential line transceiver for TIA/EIA 485/422 applications. The device is ideal for long transmission lines since the ground loop is broken to allow for a much larger common-mode voltage range. The symmetrical isolation barrier of the device is tested to provide 4kVpk of isolation for 60s between the bus-line transceiver and the logic-level interface.

Any cabled I/O can be subjected to electrical noise transients from various sources. These noise transients can damage the transceiver and near-by sensitive circuitry. Isolated transceivers however can significantly increase protection and reduce the risk of potential damage to expensive control circuits. The ISO3082 is qualified for use from –40°C to 85°C.

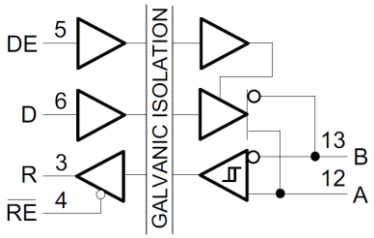

Figure 2: ISO3082 functional block diagram

2.2 Data Flow Control

The SM712 transient voltage suppressor (TVS) provides ESD, EFT, and Surge protection for data ports A commonly applied timing-control method is the inverting buffer with time-delay in Figure 3.

To ensure correct switching behavior this method requires defined start conditions after powering-up and bus idling. This is accomplished through failsafe biasing resistors, R_{FS}, which create a failsafe voltage, V_{FS}, above the receiver input sensitivity of V_{FS} > +200 mV, when no transceiver is actively driving the bus.

This robust and data rate independent timing control utilizes an inverting Schmitt-trigger buffer with different charge and discharge times. The underlying principle is to actively drive a bus during logic low states and disabling the driver during logic high states. The enabling and disabling sequence occurs on a per-bit basis making the repeater function independent of data rate and packet length.

Stepping through the functional sequence of the inverter-controlled repeater using Figure 3 clarifies its operation.

During bus-idling the receiver outputs of both repeater ports are high due to the failsafe voltage, V_{FS}. The delay capacitor, C_D, is fully charged, driving the inverter output low to maintain the transceiver in receive mode.

1) Then a low-bit on bus 1 driving the output of R_1 low, rapidly discharges C_D and enables driver D_2.
2) When the bus voltage turns positive (V_{Bus} > 200 mV) the output of R_1 turns high, thus driving D_2's output high while slowly charging C_D via R_D. The minimum time constant (R_D x C_D) must be so calculated that at the maximum supply voltage, $V_{CC\text{-}max}$, and the minimum positive inverter input threshold, $V_{TH+\ min}$, the delay time, t_D, exceeds the maximum low-to-high propagation delay, $t_{PLH\text{-}max}$, of the driver by say 30 %. For a given capacitance of, i.e. C_D = 100 pF, the required resistor value for R_D thus calculates to:

$$R_D = \left| \frac{1.3 \cdot t_{PLH-max}}{C_D \cdot \ln\left(1 - V_{IT+min} / V_{CC-max}\right)} \right|$$

3) The driver enable time is extended by the delay time, t_D, versus the actual data bit interval to establish a valid high signal on the bus prior to switching from transmit to receive mode in order to keep the receiver output continuously high. Because receiver propagation delays are shorter than those of drivers it is impossible for the receiver to turn low, not even for a short instant. Once the driver is disabled, the external failsafe resistors bias bus 2 to above 200 mV, which is seen by the active receiver as a defined high.
4) The differential output voltages on bus 2 are $V_{OD} = V_{FS}$ > + 200 mV during and idle bus, V_{OD} < -1.5V for a low bit, and V_{OD} > 1.5 V for the time delay, t_D, at the beginning of a high bit, and afterwards $V_{OD} = V_{FS}$ > + 200 mV for the reminder of a high bit.

R) **R** represents the receiver output state of a remote transceiver.

While legacy repeater designs are limited to data rates of 20 kbps, modern transceivers with shorter propagation delays allow for higher data rates of up to 200 kbps.

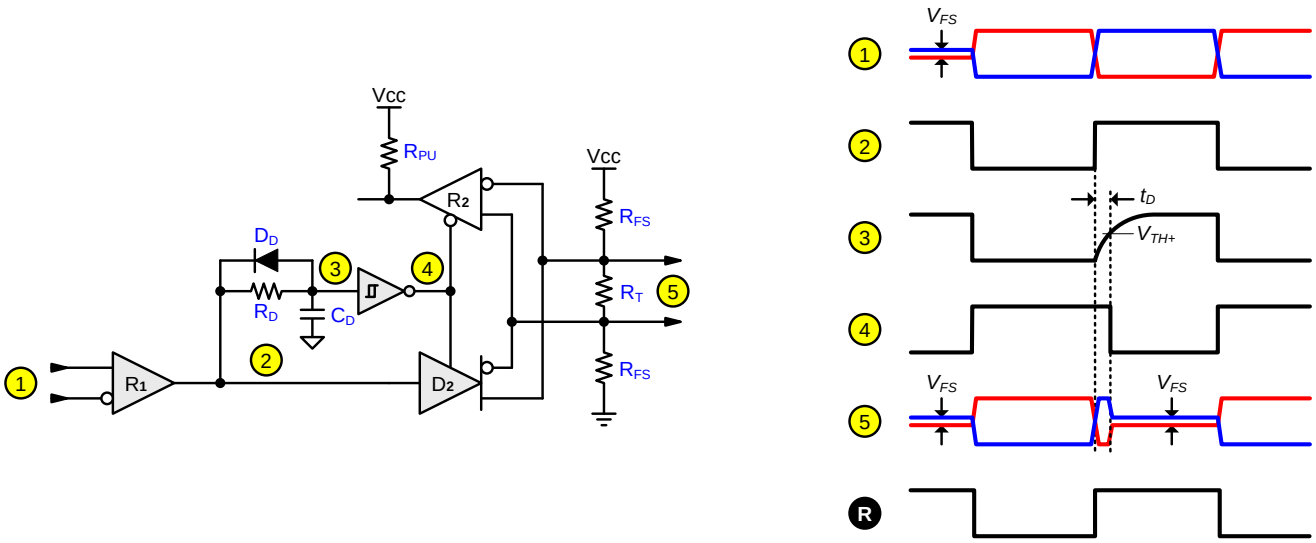

Figure 3. Data flow-control principle (left) with timing diagram (right)

(For clarity the isolation barriers have been omitted)

2.3 Transient Protection

The SM712 transient voltage suppressor (TVS) provides ESD, EFT, and Surge protection for data ports meeting IEC 61000-4-2 (ESD), IEC 61000-4-4 (EFT), and IEC 61000-4-5 (Surge) requirements. The device comprises two bidirectional TVS diodes rated for 400W peak power at an 8/20 µs peak pulse current of 17A.

Its high clamping voltage of 26V, however, can trigger the internal ESD diode structure of the transceiver. When this happens, the internal ESD structure shunts the external TVS and absorbs the entire transient energy. This can lead to latch-up and transceiver damage. To prevent this from happening, 10Ω, pulse-proof, thick-film resistors are inserted between the TVS diodes and the transceiver A and B bus terminals. These resistors provide sufficient voltage drop during a transient event to maintain the external TVS turned on.

A high-voltage capacitor (4700pF/2kV) provides an AC connection between ISO-ground and Protective-Earth (PE). Implemented here as a header pin, this allows for the connection of a low-inductance cable between the surge generator and ground.

The high-impedance resistor (1M) parallel to the high-voltage capacitor functions as a bleeder resistor to prevent the build-up of electrostatic charges on the bus lines

2.4 Power Supply

The isolated DC-DC power supply converter utilizes the push-pull converter principle. Two isolation transformers are used to power each transceiver separately. For this reason the SN6501 transformer driver drives two center-tapped transformers whose outputs are rectified by Schottky diodes (D1 to D4). The rectified outputs are smoothened by bulk capacitors (C6 and C9). The subsequent low dropout regulators, TPS76350, provide regulated 5V outputs for output currents of up to 250mA. For best stability and lowest ripple, low-ESR, 4.7µF ceramic capacitors are recommended.

3 Measurement

3.1 Data Transmission

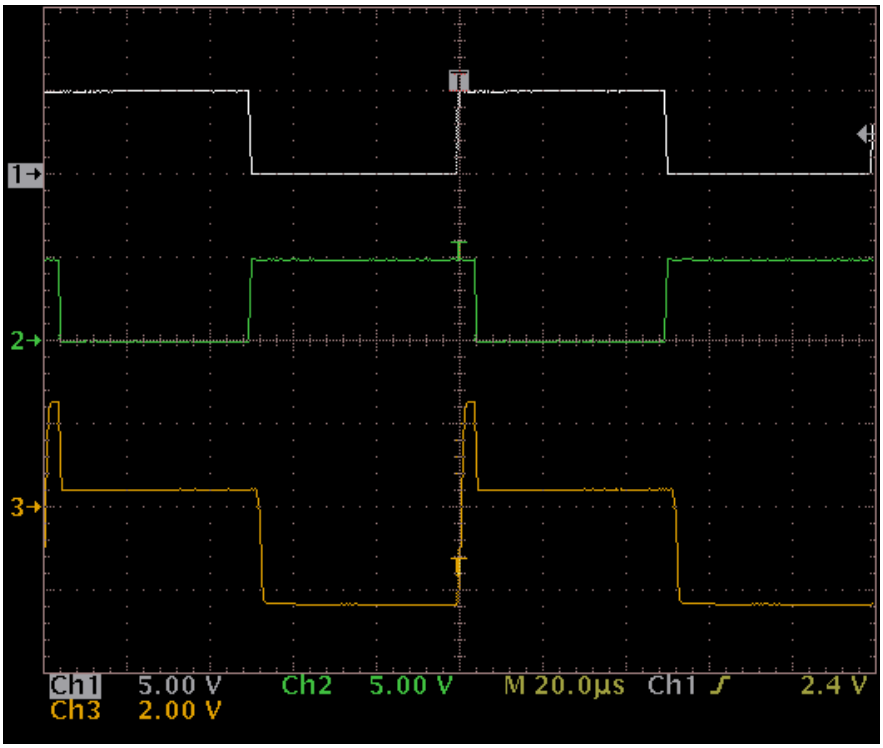

Figure 4. Data flow-control: Ch1 = D, Ch2 = DE, /RE, Ch3 = V_{BUS}

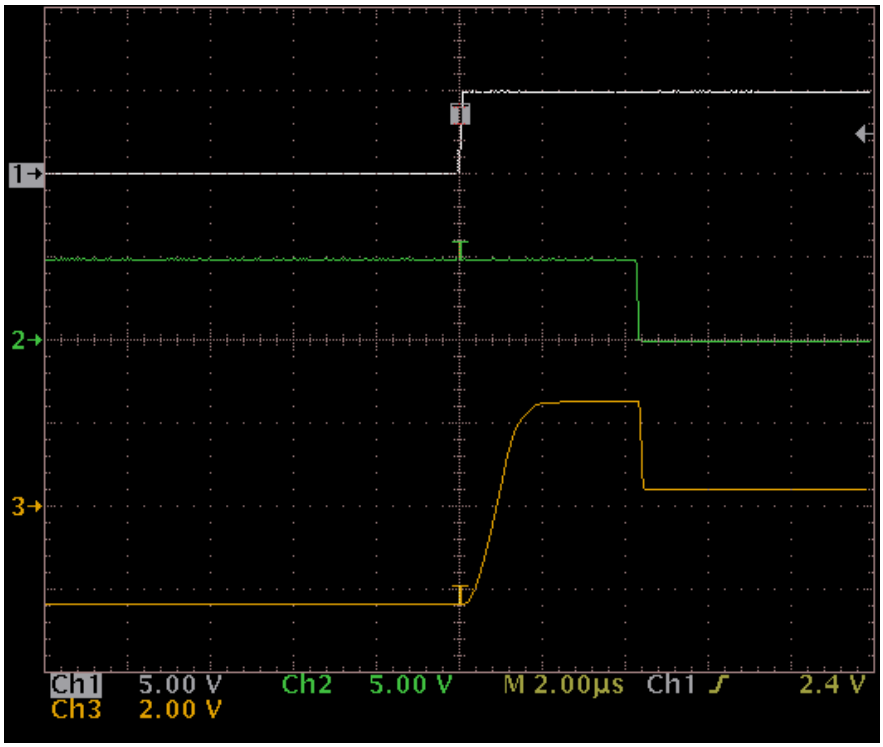

Figure 5. Data flow-control zoomed-in: Ch1 = D, Ch2 = DE, /RE, Ch3 = V_{BUS}

4 PCB Design

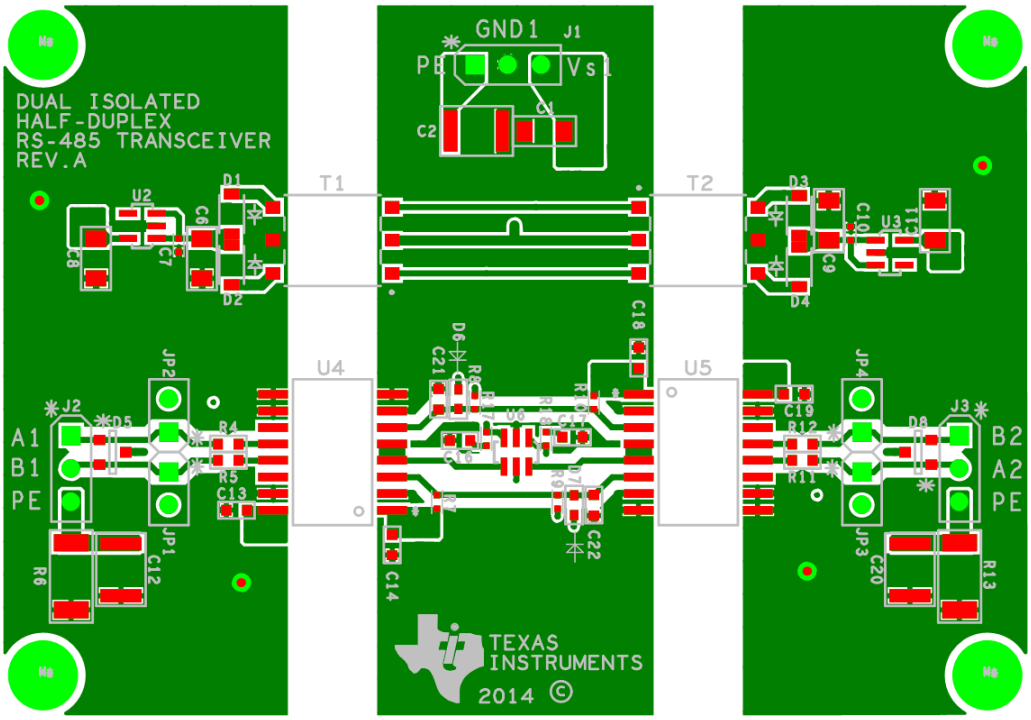

Figure 6: PCB layout top

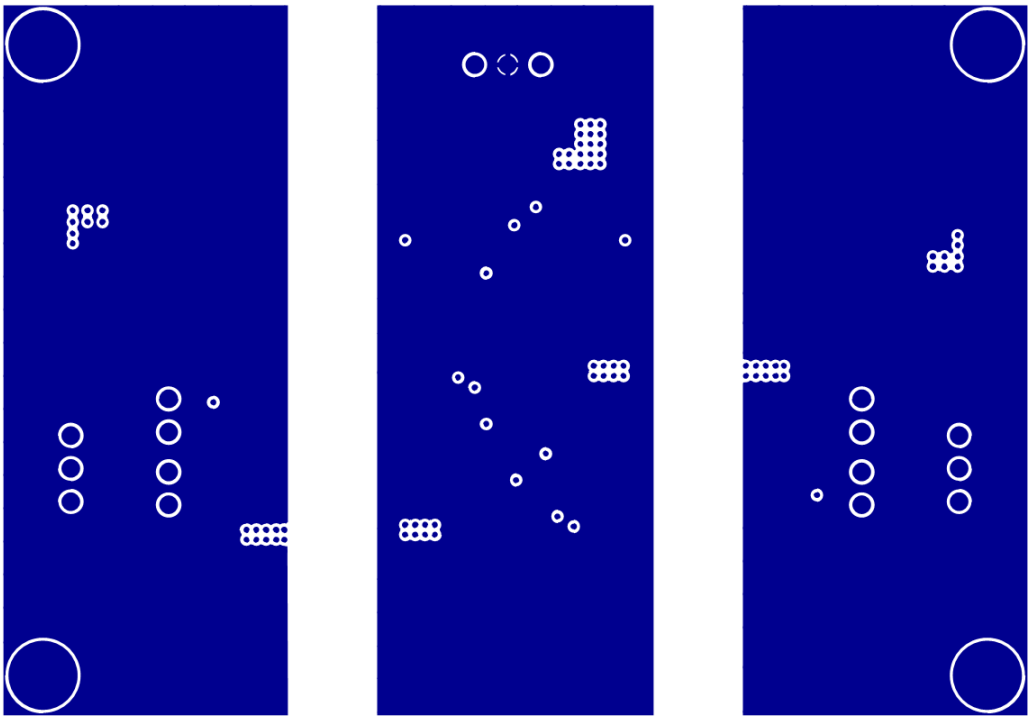

Figure 7: PCB layout ground

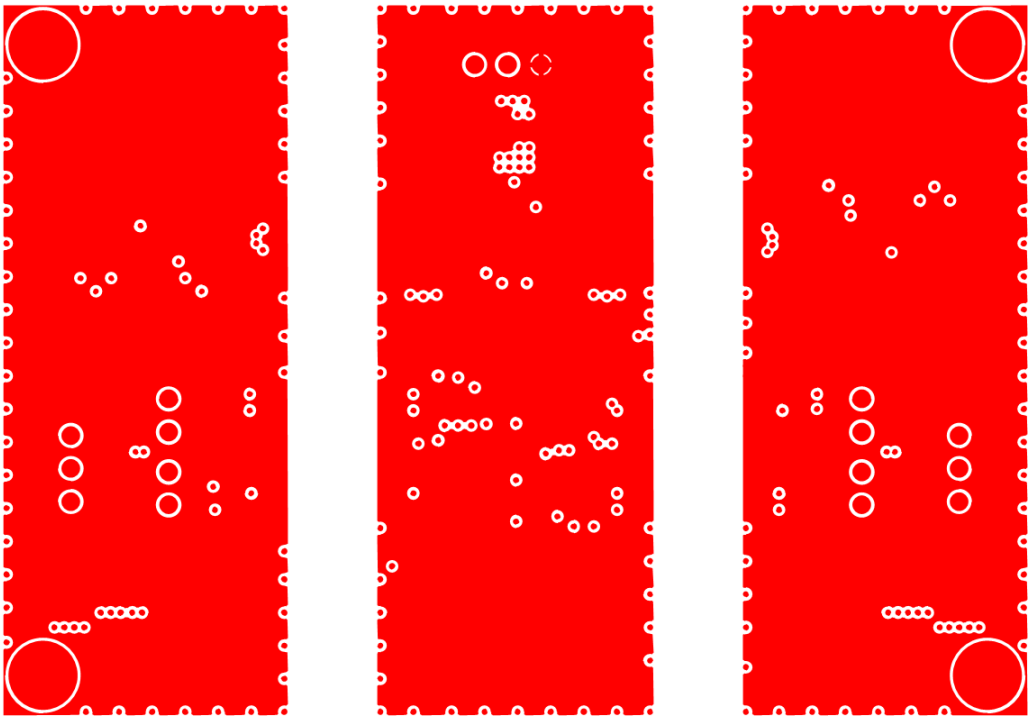

Figure 8: PCB layout power

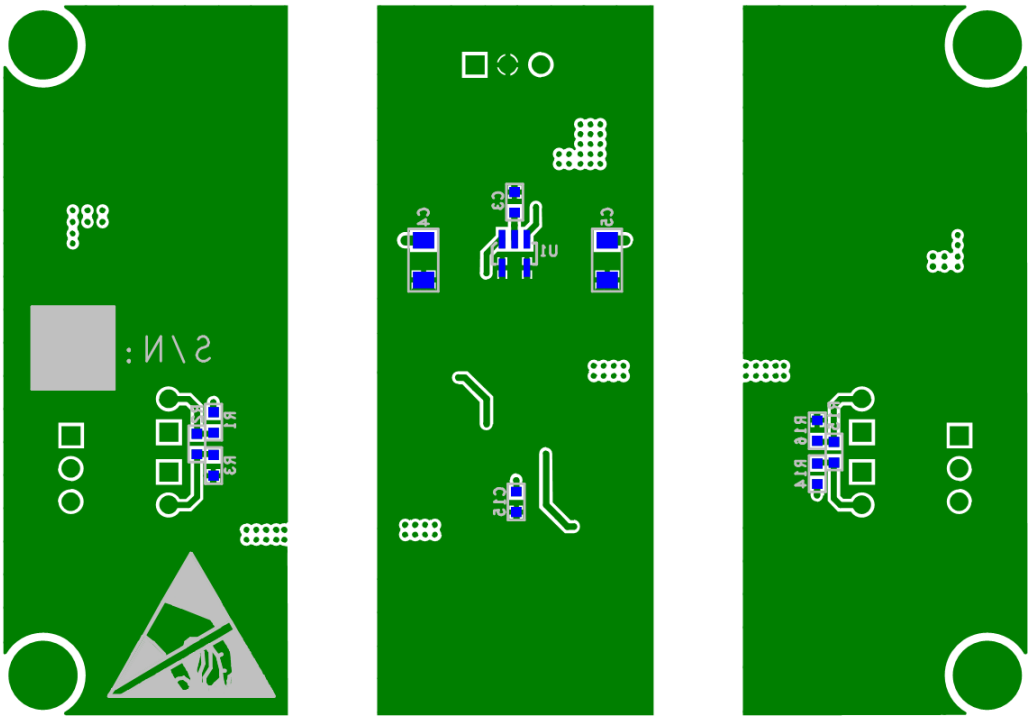

Figure 9: PCB layout bottom

5 References

1. *Data Rate Independent Half-Duplex Repeater Design for RS-485*, SLYT480
2. *RS-485 Design Guide, Kugelstadt 2008, SLLA272B*

6 Appendix

6.1 Schematic

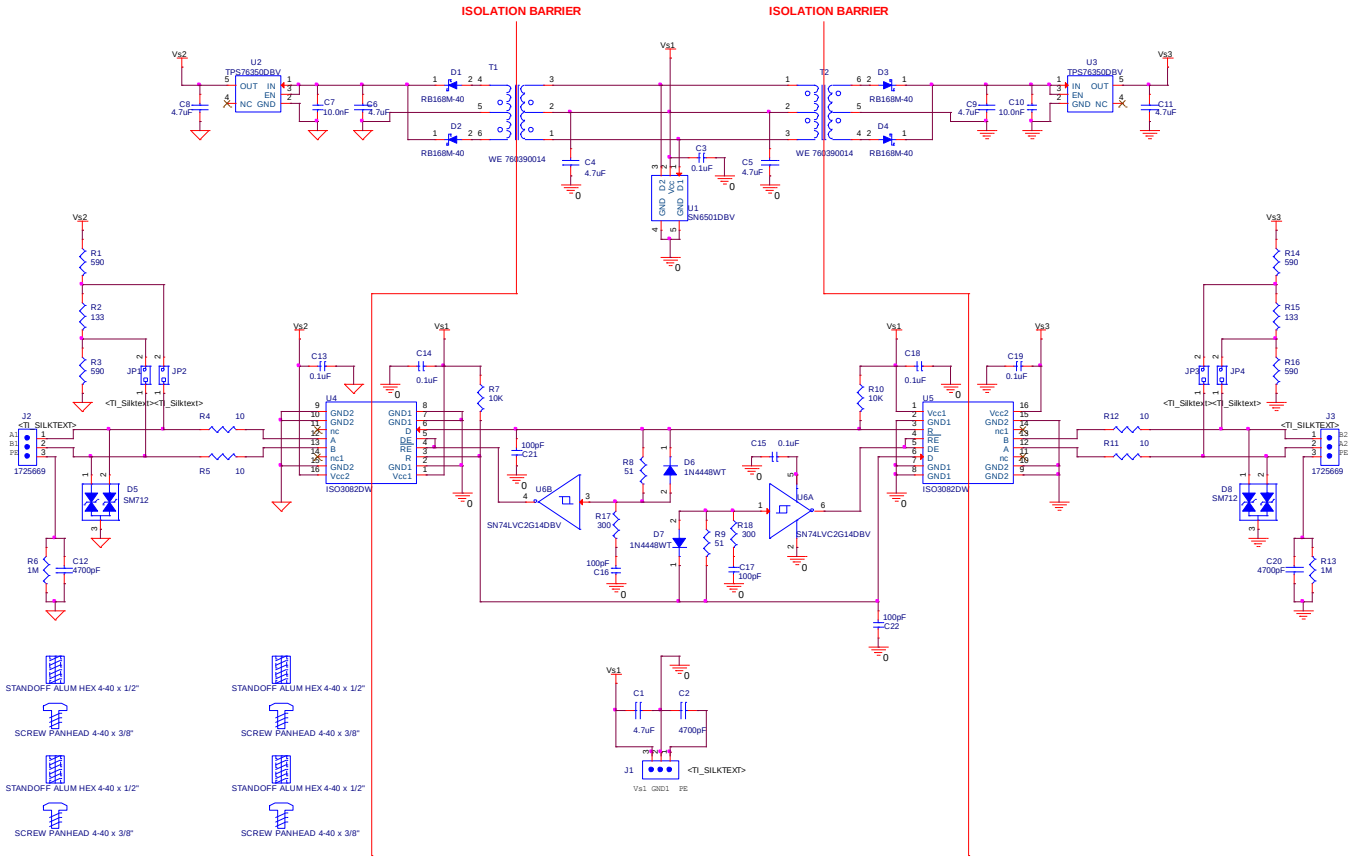

Figure 10: Dual isolated half-duplex RS-485 repeater

6.2 Bill of Materials

Table 1: Isolated auto-polarity RS-485 transceiver Bill of Materials

Item	Quantity	Reference	Part	Footprint	Manufacturer	Manufacturer Part Number
1	7	C1, C4, C5, C6, C8, C9, C11	4.7uF	1206	TDK	C3216X7R1H475K160AC
2	3	C2, C12, C20	4700pF	1812	NOVACAP	1812 B 472 K 202 N T
3	6	C3, C13, C14, C15, C18, C19	0.1uF	603	Murata	GRM188R71H104KA93D
4	2	C7, C10	10nF	402	Yageo	CC0402KRX7R9BB103
5	2	C16, C17	100pF	603	Kemet	C0603C101J5RACTU
6	2	C21, C22	DNI	603		
7	4	D1, D2, D3, D4	Schottky diode		Rohm	RB168M-40
8	2	D5, D8	TVS	SOT-23	Micro Commercial	SM712-TP
9	2	D6, D7	Diode	SOD523F	Fairchild	1N4448WT
10	3	J1, J2, J3				
11	4	JP1, JP2, JP3, JP4				
12	4	R1, R3, R14, R16	590 Ω	603	Yageo	RC0603FR-07590RL
13	2	R2, R15	133 Ω	603	Yageo	RC0603FR-07133RL
14	4	R4, R5, R11, R12	10 Ω	603	Vishay	CRCW060310R0JNEAHP
15	2	R6, R13	1 MΩ	2010	HVC 2010 1M0 G T3	TT Electronics
16	2	R7, R10,	10 kΩ	402	Yageo	RC0402JR-0710KL
17	2	R8, R9	51 kΩ	402	Yageo	RC0402JR-0751KL
18	2	R17, R18	300 Ω	402	Yageo	RC0402FR-07300RL
19	2	T1, T2	1:1.3	SMT	Wurth Electronics	760390014
20	1	U1	SN6501	SOT23-5	Texas Instruments	SN6501DBVT
21	2	U2, U3	TPS76350	SOT23-5	Texas Instruments	TPS76350DBVR
22	2	U4, U5	ISO3082	16DW	Texas Instruments	ISO3082DW
23	1	U6	SN74LVC2G14	SOT23-6	Texas Instruments	SN74LVC2G14DBVR

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