TI Designs

Analog Input, Output, and Relay Drive Output Module for Smart Grid IEDs

TI Designs

TI Designs provide the foundation that you need including methodology, testing and design files to quickly evaluate and customize the system. TI Designs help *you* accelerate your time to market.

Design Resources

TIDA-00310	Tool Folder Containing Design Files
ADS8684	Product Folder
DAC8760	Product Folder
OPA188	Product Folder
TCA6408A	Product Folder
TPL7407L	Product Folder
TPS7A1650	Product Folder
TPS7A1633	Product Folder

TI E2E™ Community

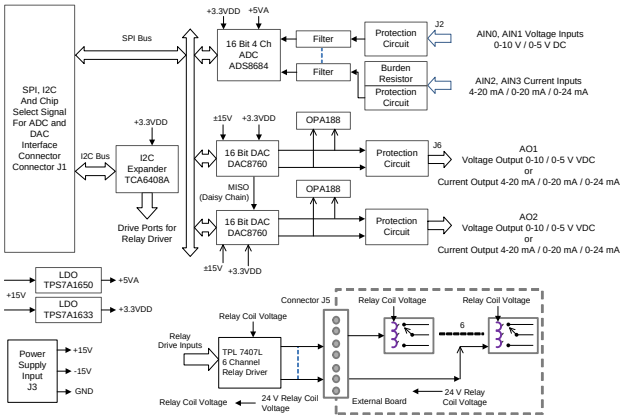
ASK Our E2E Experts
WEBENCH® Calculator Tools

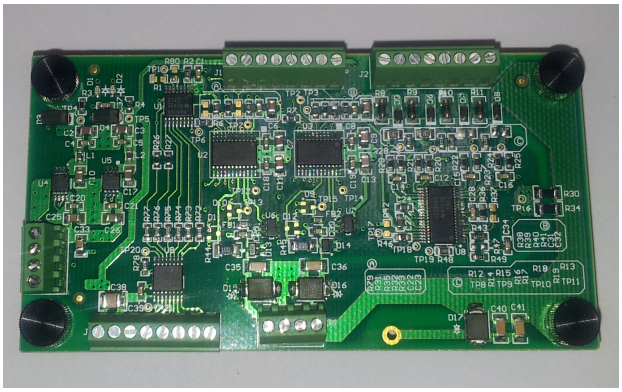
Design Features

- DC Analog Input Design Based on ADS8684 4-Channel 16-Bit ADC
- Provision to Measure Two Current Inputs and Two Voltage Inputs
- Accuracy of < ±0.2% of Full Scale at 25°C
- DC Analog Output Design Based on DAC8760 Single-Channel 16-Bit Digital Analog Converter (DAC)
- Provision for Two Output Channels (Each Channel Configurable as Either Voltage or Current Output)
- Uses SPI With Daisy Chain With Two DAC8760s
- Accuracy < ±0.2% Full Scale Value At 25°C
- TPL7407L Low-Side Driver Configured to Drive Six Relay Outputs
- Relay-Drive Output Supports Coil Voltage Rating of 12-, 15-, and 24-V DC
- TCA6408A I/O Expander With I2C Interface to Provide Inputs to TPL7407L for Relay Control

Featured Applications

- Multifunction Protection Relay
- Power Quality Meters
- Substation Automation Products and Remote Terminal Units (RTUs)
- I/O Expansion Modules





1 System Description

Protection relays are commonly found along the entire grid infrastructure pathway from generation to transmission and distribution. Protection relays allow operators to monitor and control the grid at different points. The two main functionalities of a protection relay are measurement and protection. In modern protection relays, communication is also an integral part of the solution, enabling operators to remotely monitor and operate the grid infrastructure. The protection relay typically functions as the local intelligence that signals to a circuit breaker to open or close. The basic purpose of a protection relay is to protect the grid (further downstream) in the event of a malfunction. The protection relay protects the grid by monitoring the current and voltage on specific lines on the grid. The circuit breaker sits on the line. The inputs into a protection relay are typically the current and voltage from a sensor on the line, plus any communication from other related auxiliary equipment or sensor on the grid communication network, for example, health information of the transformer from temperature and pressure sensors. The output consists of signals to a circuit breaker (to turn open or close) and communication to the grid network. In situations where the protection relay detects a fault, the relay commands a breaker to open the line, thus protecting everything down the line from the protection relay.

Remote terminal units are also used in entire smart grid infrastructures to record parameter information related to the health of equipment like generators, motors, or transformers.

The accurate measurement of the voltage, current, or other parameters like temperature pressure or the vibration of power system equipment are prerequisites to any form of control, ranging from automatic closed-loop control to the recording of data for statistical purposes. There are a variety of ways to measure these parameters, including the use of direct-reading instruments and electrical measuring transducers.

1.1 Instrumentation in Smart Grid

1.1.1 Analog Inputs

Transducers produce an accurate DC analogue output (usually a current) that corresponds to the parameter being measured (the measured). Outputs from transducers may be used in many ways, from the simple presentation of measured values for an operator, to utilization by a network automation scheme to determine the control strategy. There are two types of transducers:

1. Analog transducers where output is a function of time
2. Digital transducers which use analog transducers along with digital processing

Analog transducers are used for the following measurements in power systems:

- Voltage and current measurement
- Vibration measurement
- Temperature and pressure measurement of oil in the transformer
- Status signal for breaker health
- Tap changer status signal

CT and VT are normally preferred to measure voltage and current. For other parameters, transducers with the following outputs are used:

(a) Voltage outputs ranging from

(a) ±10-V DC

(b) 0- to 10-V DC

(c) 0- to 5-V DC

2. Current outputs ranging from
   (a) ±20 mA
   (b) 0 to 20 mA
   (c) 0 to 24 mA
   (d) 4 to 20 mA

Protection relays and RTUs use the analog input module for interfacing with such transducers. This interfacing uses analog front end (AFE), which comprises ADC, programmable gain array, the signal-conditioning chain, and other filter circuits.

The TI portfolio includes devices which contain the AFE for the measurement of 4-8 channels in a single chip.

1.1.2 Analog Outputs

Multifunction protection relays and RTUs also include analog outputs that can transfer any parameters such as energy to an RTU or protection relay. These analog outputs also provide the required input supply for an analog instrumentation system.

The analog output can either be a voltage output or a current output.

Voltage output can be

- 0- to 10-V DC
- 0- to 5-V DC
- ±10-V DC

whereas current output can be

- ±20 mA
- 0 to 20 mA
- 0 to 24 mA
- 4 to 20 mA

Analog outputs use DAC which can be 12- to 16-bit. The TI portfolio includes several DAC devices that can be configured to provide either voltage or current outputs.

1.1.3 Relay Drive Outputs

Multifunction protection relays and RTUs also include relay outputs. This relay output uses electromechanical relay switching to convey the status of particular incidents, especially for the interlocking of protection relays and the circuit breaker system.

Relay outputs can also provide power to the auxiliary equipment. The electromechanical relay used to provide power to auxiliary equipment are power relays with ratings from 8 A to 12 A at 240-V AC. Such relay outputs are also known as wet contacts.

The basic solution to drive electromechanical relays utilizes a discrete bipolar junction transistor (BJT) or metal-oxide semiconductor field-effect transistor (MOSFET). This solution requires more PCB space and is also unreliable because of stress occurrences due to the switching of inductive loads. This solution is also prone to malfunction due to the effect of electromagnetic interference (EMI). The number of ports required for driving the relays rises with an increase in the number of relays.

The TI portfolio includes a single-chip solution, which can be used to drive seven electromechanical relays with high current ratings simultaneously. The TI portfolio also includes an I2C to parallel-bus expander, which can be used to drive the relay driver, reducing the number of interfaces or driving ports from the MCU.

1.2 TI Design

The TI Designs Reference Design Library is a robust reference design library spanning across analog, embedded processor, and connectivity products. All TI designs include schematics, block diagrams, BOMs, and design files.

This reference TI design provides details for the design and development of an analog input module, analog output module, and relay output-driver module, which can be directly used in a protection relay and RTU system.

This TI design also includes an external protection circuit that has been tested and verified to be compliant with the IEC61000-4 standard for electrostatic discharge (ESD).

This user sheet provides all of the relevant design files for users to evaluate this reference design in Section 8 such as schematics, BOM, PCB layouts, and Gerber files.

2 Design Features

This TI design has the following specifications.

Table 1. Design Features

ANALOG INPUTS		
ADC Details	ADC resolution	16 Bit
	ADC type and speed	Successive approximation (SAR)
	Maximum sampling rate	500 kSPS
Voltage Input	DC voltage Inputs	0- to 10-V DC
		0- to 5-V DC
	Number of voltage input channels	2
	Input impedance for voltage channel	> 1 MΩ
Current Input	DC current inputs	4 to 20 mA
		0 to 20 mA
		0 to 24 mA
	Input impedance	< 300 Ω
	Number of current input channels	2
Accuracy	% of full scale value at 25ºC	< ±0.2 %
Interface	Interface with host controller	SPI
EMC	ESD immunity IEC61000-4-2	± 4 kV Contact discharge
Connector	8-Pin 2.54-mm pitch screw type	
ANALOG OUTPUTS		
DAC Details	DAC resolution	16 Bit
	DAC type	Resistor string monotonic
Output Configuration	Number of analog output channels	2
	Voltage and current output[(1)]	0- to 5-V DC
		0- to 10-V DC
		4- to 20-mA DC
		0- to 20-mA DC
		0- to 24-mA DC
Accuracy	% of full scale value at 25ºC	< ±0.2 %
Load	Output load	For V_{OUT}: R_L = 1 kΩ, C_L= 200 pF; for I_{OUT}: R_L = 300 Ω
Interface	Interface with host controller	SPI
EMC	ESD immunity IEC61000-4-2	±4 kV Contact discharge
Connector	4-Pin 2.54-mm pitch screw type	

(1) Either voltage or current output is available.

RELAY DRIVE OUTPUTS		
Number of Outputs		6
Type of Outputs		Open drain
Voltage Rating	Rated coil voltage	12-, 15-, and 24-V DC
Interface to Host Controller	I2C	
	Using I2C to parallel port expander	8-Bit parallel port
Connector	8-Pin 2.54-mm pitch screw type	
POWER SUPPLY		
On-Board Power Supply	Analog supply for DAC	+15-V DC
		–15-V DC
		Ground
	Digital power supply for ADC, DAC, and I2C expander	3.3 V
	Analog power supply for ADC	5-V DC
Relay Drive Power Supply	External power supply	12- , 15-, and 24-V DC
	Connector	Common with relay drive output connector

3 Block Diagram

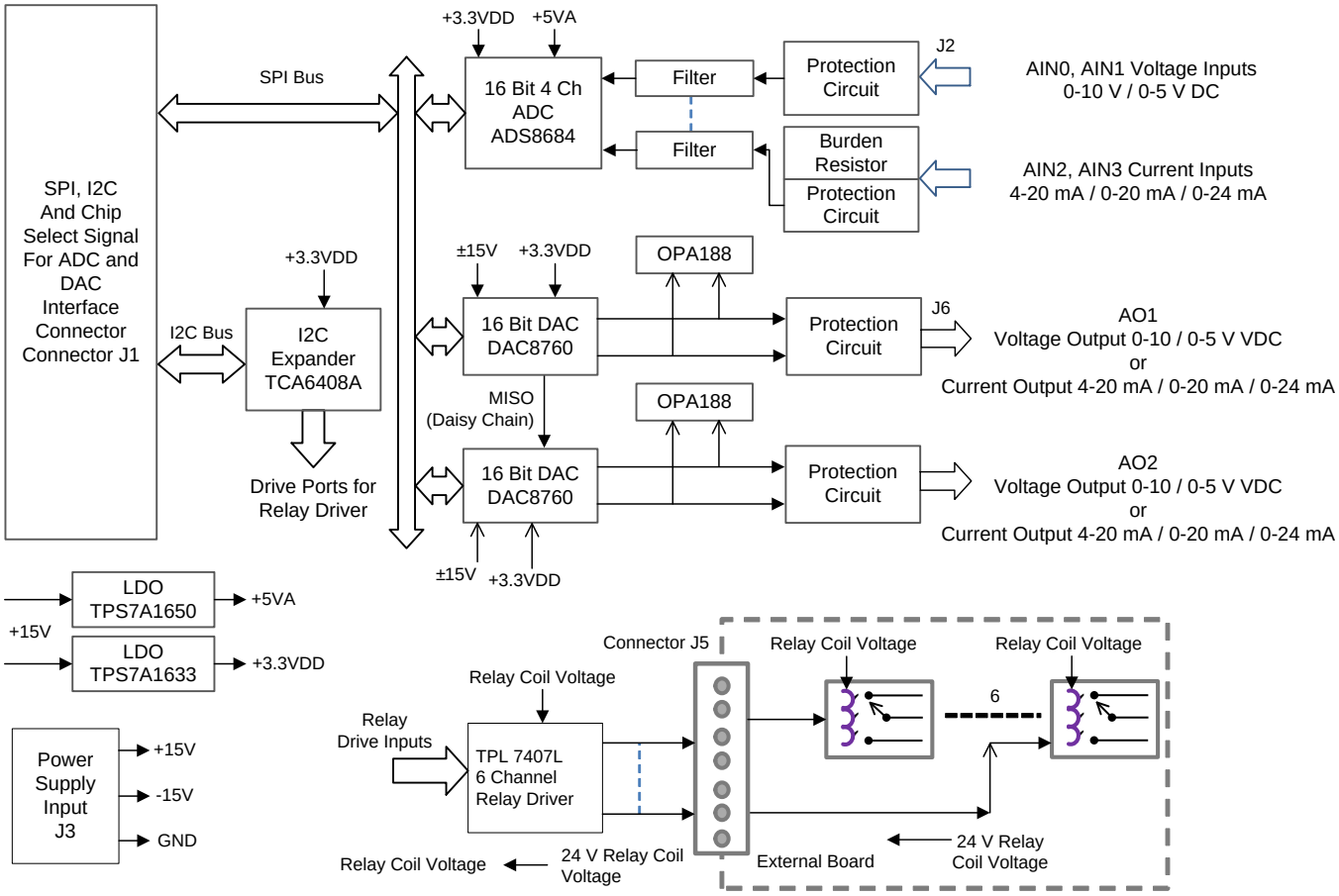


Figure 1. Block Diagram of TIDA-00310

3.1 Analog Input Section

3.1.1 ADC

The analog input section has a provision for four inputs. This design uses the ADS8684 device (16-bit, 4-channel, SAR ADC) with an on-chip programmable gain amplifier (PGA) and reference. The ADC provides a high-input impedance (typically 1 MΩ). The ADC interfaces with the host controller through the use of SPI. The on-chip 4.096-V ultra-low drift voltage reference is used as the reference for the ADC.

3.1.2 Input Type and Range Supported

Analog inputs AIN0 and AIN1 are configured as voltage inputs; AIN2 and AIN3 are configured as current inputs.

This design supports the following input ranges:

- 0- to 5-V DC and 0- to 10-V DC for voltage channels.
- 0- to 20-mA DC, 0- to 24-mA DC, and 4- to 20-mA DC for current channel.

3.1.3 Power Supply

This analog input module requires a 3.3-V digital power supply and a 5-V analog power supply.

3.1.4 Connector Details

An 8-pin screw-type connector J2 is used for analog inputs with two pins for each analog channel. The input applied is single-ended.

3.2 Analog Ouput

3.2.1 DAC

This design uses a 16-bit resolution DAC8760 device. Each DAC provides one output for either voltage or current . This design uses two DACs to meet the two AO requirements.

The DAC8760 is a low-cost, precision, fully-integrated, 16-bit DAC.

Users can program the DAC8760 device as a:

- current output with a range of 4- to 20- mA, 0- to 20- mA, or 0- to 24- mA.
- voltage output with a range of 0- to 5- V, 0- to 10- V, ±5 V, or ±10 V, with a 10% over-range. (0- to 5.5- V, 0- to 11- V, ±5.5 V, or ±11 V).

The DAC interfaces with the host controller through the use of SPI communication. This DAC has a feature that allows a daisy-chain SPI.

3.2.2 Output Type and Range Supported

The DAC outputs can be configured as either voltage output or current output. Both AO support the following ranges:

- 0- to 5-V DC and 0- to 10-V DC
- 0- to 20-mA DC, 0- to 24-mA DC, and 4- to 20-mA DC
- For V_{OUT}: R_L = 1 kΩ, C_L= 200 pF; for I_{OUT}: R_L = 300 Ω

3.2.3 Output Voltage Sense Buffering

$+V_{SENSE}$ and $–V_{SENSE}$ enable the sensing of a load. Ideally the load is connected to V_{OUT} at the terminals. As V_{OUT} and I_{OUT} are tied together, and when used as a current output, there is a gain error due to the current leakage of the $+V_{SENSE}$ pin. This current leakage introduces a gain error of –0.36%. This error can be minimized by using a high input impedance, low-input bias current op-amp. In the current design the $+V_{SENSE}$ connects to V_{OUT} through the buffer implemented using TI's op-amp OPA188, which has a typical input bias current of 160 pA.

3.2.4 Power Supply

This DAC requires 3.3 V and ±15.0 V.

3.2.5 Connector

The 4-pin screw type connector J6 is used for analog outputs with two pins for each analog output.

3.3 Relay Drive Output

3.3.1 Relay Driver

The relay drive output module provides six low-side drive outputs for driving electromagnetic relays. This design uses the TPL7407L device, which is a high-voltage, high-current n-channel MOS (NMOS) transistor array. This device consists of seven NMOS transistors that feature high-voltage outputs with common-cathode clamp diodes for the purpose of switching inductive loads. The maximum drain-current rating for a single NMOS channel is 600 mA.

3.3.2 I2C I/0 Expander

The digital input required for the relay driver is provided by the I2C I/O expander. The TCA6408A device provides a drive signal to the TPL7407L device. This 8-bit I/O expander interfaces with the host controller through the I2C interface (serial clock (SCL) and serial data (SDA)). The major benefit of the I2C I/O expander is a wide VCC range. The device can operate from 1.65 V to 5.5 V on the P-port side as well as the SDA and SCL sides. Pull-up resistors are provided in the design.

3.3.3 Power Supply

This module requires a 3.3-V digital power supply. This module requires an external power supply of 12- to 24-V DC that can be applied to two pins of connector J5. Refer to the schematics in Section 4.1.4 and the test setup details in Section 6 for connection purposes.

3.3.4 Connector

The relay drive outputs use an 8-pin screw type connector, J5.

3.4 Power Supply

3.4.1 Input Supply

This TI design requires a ±15-V DC input voltage to be connected to connector J3.

3.4.2 On-Board Supply

The ADS8684 ADC requires 5 V for the analog supply, which is derived from 15 V using the low-dropout (LDO) TPS7A1650 device that can provide a 100-mA output current.

The ADS8684 and DAC8760 devices require a 3.3-V supply for digital power supply VDD, which is derived from the 15 V using an LDO TPS7A1633.

The TPS7A16 family of ultra-low power, LDO voltage regulators offers benefits such as an ultra-low, quiescent current around 5 µA; a 60-V high input voltage; and miniaturized, high thermal-performance packaging that can source a 100-mA load.

3.5 Interface to Host Controller

This TI design can interface to a host controller through the connector J1.

J1 is an 8-pin, 2.54-mm pitch connector and has chip select signals (CS0 and CS1) for ADC and DAC, SPI standard signal, ground, and I2C standard signals.

For testing purposes the TM4C1294XL device TIVA™ C-series LaunchPad™ is used as a host controller. Use the following signals on the LaunchPad to interface:

- SPI Clock ---- PA2
- SPI MOSI ---- PA4
- SPI MISO ---- PA5
- SPI Chip Select for ADC ---- PA3
- SPI Chip Select for DAC ---- PK3
- I2C Clock(SCLK) ---- PB2
- I2C Data(SDATA) ---- PB3
- Ground

4 Circuit Design and Component Selection

4.1 Analog Input

4.1.1 ADC Description

The 4-channel analog input design is based on the ADS8684 16-bit SAR ADC device. The ADS8684 is a 4-channel integrated data acquisition systems based on a 16-bit SAR ADC. The device features integrated AFE circuitry for each input channel with over-voltage protection up to ±20 V, a 4-channel multiplexer with automatic and manual scanning modes, and an on-chip 4.096-V reference with extremely low drift. Operating on a single analog supply of 5 V, each input channel on the devices can support true bipolar input ranges of ±10.24 V, ±5.12 V, and ±2.56 V; as well as unipolar input ranges of 0 to 10.24 V and 0 to 5.12 V. The input range selection is done by software programming of the device internal registers and is independent for each channel. The ADS8684 offers a 1-MΩ constant, resistive-input impedance regardless of the selected input range.

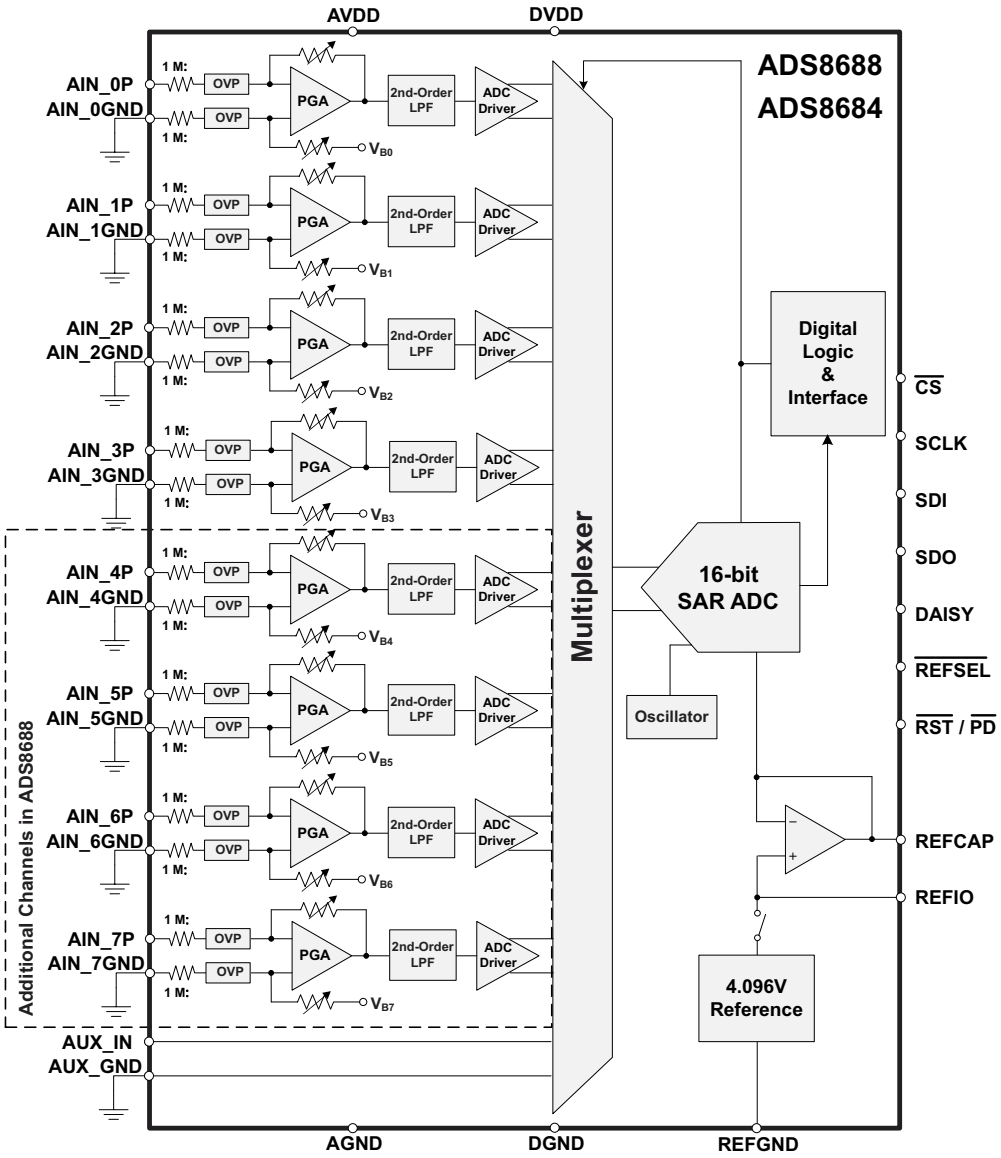


Figure 2. Internal Block Diagram of ADS8684

The ADS8684 ADC has the following features:

- A 16-bit ADC with an integrated AFE
- A 4-channel multiplexor (MUX) with auto and manual scan
- Software programmable inputs per channel
  - Bipolar ranges: ±10.24 V, ±5.12 V, and ±2.56 V
  - Unipolar ranges: 0 to 10.24 V and 0 to 5.12 V
- A 5-V analog supply; 1.65- to 5-V I/O supply
- Excellent performance:
  - 500-kSPS Aggregate throughput
  - INL: ±2.5 LSB
  - SNR: 91 dB
  - Low power: 70 mW
- An SPI™-compatible interface

The ADS8684 device offers a simple SPI-compatible serial interface to the host. The digital supply operates from 1.65 V to 5.25 V, enabling direct interface to a wide range of host controllers.

The device also offers integrated front end signal processing including a multiplexer, second-order anti-aliasing filter, ADC driver amplifier, and an extended industrial temperature range, which all make the ADS8684 ideal for any standard industrial analog input measurement.

In the design, analog input channels AIN0 and AIN1 are used for voltage input. The voltage input has the following possible input ranges:

- 0- to 10-V DC
- 0- to 5-V DC
- Accuracy < ±0.2% full scale at 25°C
- Input impendence > 1 MΩ

Analog Input channels AIN2 and AIN3 are used for current input. The current input has the following possible input ranges:

- 0- to 20-mA, 0- to 24-mA, and 4- to 20-mA DC input current ranges
- Accuracy < ±0.2% full scale at 25°C
- Input impendence < 300 Ω

4.1.1.1 Analog Input AIN0-AIN3

The ADS8684 device has four analog input channels; the positive inputs, AIN_nP (n = 0 to 3), are the single-ended analog inputs and the negative inputs, AIN_nGND, are tied to GND.

Figure 3 shows the simplified circuit schematic for each analog input channel, including the input overvoltage protection circuit, PGA, low-pass filter (LPF), high-speed ADC driver, and analog multiplexer.

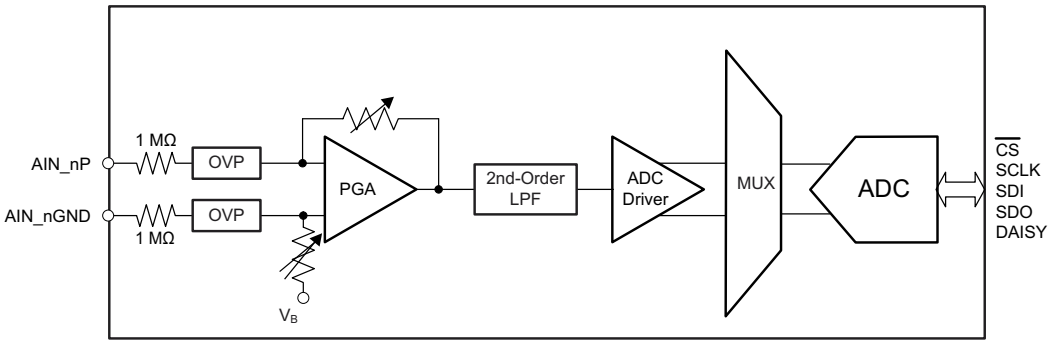


Figure 3. Front-End Circuit Schematic for Each Analog Input Channel

4.1.1.2 Input Section

The devices support multiple unipolar or bipolar, single-ended input voltage ranges based on the configuration of the program registers. The input voltage range for each analog channel can be configured to bipolar ±2.5 × V_{REF}, ±1.25 × V_{REF}, and ±0.625 × V_{REF}; or unipolar 0 to 2.5 × V_{REF} and 0 to 1.25 × V_{REF}. With the internal or external reference voltage set to 4.096 V, the input ranges of the device can be configured to bipolar ranges of ±10.24 V, ±5.12 V, and ±2.56 V or unipolar ranges of 0.0 V to 10.24 V and 0.0 V to 5.12 V.

Any of these input ranges can be assigned to any analog input channel of the device. The device samples the voltage difference (AIN_nP – AIN_nGND) between the selected analog input channel and the AIN_nGND pin. TI recommends running separate wires from the AIN_nGND pin of the device to the sensor or signal conditioning ground.

Each analog input channel in the device presents a constant resistive impedance of 1 MΩ. The input impedance is independent of either the ADC sampling frequency, the input signal frequency, or range. The primary advantage of such high-impedance inputs is the ease of driving the ADC inputs without requiring driving amplifiers with low output impedance.

To maintain the DC accuracy of the system, matching the external source impedance on the AIN_nP input pin with an equivalent resistance on the AIN_nGND pin is recommended. This matching helps to cancel any additional offset error contributed by the external resistance.

4.1.1.3 PGA

The AD8684 ADC offers a PGA at each individual analog input channel, which convert the original single-ended input signal into a fully-differential signal to drive the internal 16-bit ADC. The PGA also adjusts the common-mode level of the input signal before being fed into the ADC to ensure maximum usage of the ADC input dynamic range. Depending on the range of the input signal, the PGA gain can adjust accordingly by setting the Range_CHn[2:0] (n = 0 to 3) bits in the program register. The default or power-on state for the Range_CHn[2:0] bits is 000, which corresponds to an input signal range of ±2.5 × V_{REF} as Table 2 shows.

Table 2. Input Range Selection Bits Configuration

ANALOG INPUT RANGE	Range_CH*n*[2:0]		
	BIT 2	BIT 1	BIT 0
±2.5 × V_{REF}	0	0	0
±1.25 × V_{REF}	0	0	1
±0.625 × V_{REF}	0	1	0
0 to 2.5 × V_{REF}	1	0	1
0 to 1.25 × V_{REF}	1	1	0

4.1.1.4 Multiplexer (MUX)

The ADS8684 device features an integrated 4-channel analog multiplexer. For each analog input channel, the voltage difference between the positive analog input AIN_nP and the negative ground input AIN_nGND is conditioned by the AFE circuitry before being fed into the multiplexer. The ADC directly samples the output of the multiplexer. The multiplexer in the device can scan analog inputs in either manual or auto-scan mode. In manual mode (MAN_Ch_n), the channel is selected for every sample through a register write; in auto-scan mode (AUTO_RST), the channel number is incremented automatically on every $\overline{CS}$ falling edge after the present channel is sampled. The analog inputs can be selected for an auto scan with register settings.

The devices automatically scan only the selected analog inputs and in ascending order. The maximum overall throughput for ADS8684 is specified at 500 kSPS across all of the channels. The per-channel throughput value depends on the number of channels selected in the multiplexer scanning sequence. For example, the throughput per channel is equal to 250 kSPS only if two channels are selected; but, the throughput per channel is equal to 125 kSPS per channel if four channels are selected.

4.1.1.5 Reference

The ADS8684 device can operate with either an internal voltage reference or an external voltage reference using the internal buffer. The internal or external reference selection is defined by an external REFSEL pin biasing. The device has a built-in buffer amplifier to drive the actual reference input of the internal ADC core to maximize performance. The ADS8684 has an internal 4.096-V (nominal value) reference. In order to select the internal reference, the REFSEL pin must be tied low or connected to AGND. When using the internal reference option, the REFIO (pin 5) becomes an output pin with the internal reference value. TI recommends placing a 10-µF (minimum) decoupling capacitor between the REFIO pin and the REFGND (pin 6), as shown in Figure 4. Place the capacitor as close to the REFIO pin as possible.

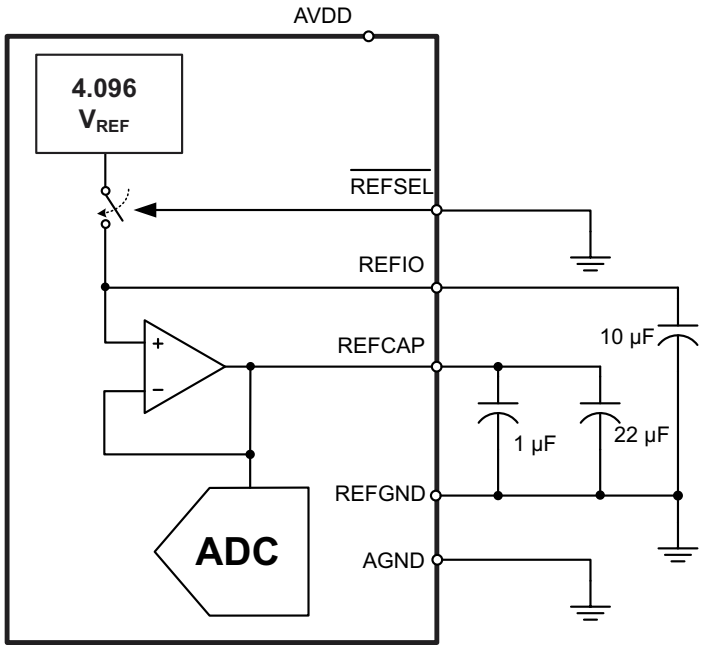


Figure 4. Device Connections for Using an Internal 4.096-V Reference

The internal reference is also temperature compensated to provide excellent temperature drift over an extended industrial temperature range of –40°C to 125°C.

4.1.1.6 Power Supply Recommendations

The device uses two separate power supplies: AVDD and DVDD. The internal circuits of the device operate on AVDD, while DVDD is used for the digital interface. AVDD and DVDD can be independently set to any value within the permissible range.

The AVDD supply pins must be decoupled with AGND by using a minimum 10-µF and 1-µF capacitor on each supply. Place the 1-µF capacitor as close to the supply pins as possible. Place a minimum 10-µF decoupling capacitor very close to the DVDD supply to provide the high-frequency digital switching current. The effect of using the decoupling capacitor is illustrated in the difference between the power-supply rejection ratio (PSRR) performance of the device.

4.1.1.7 Digital Interface

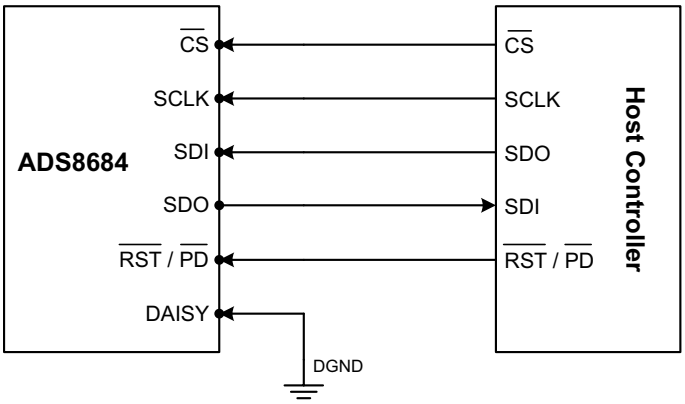


Figure 5. ADS8684 Digital Interface

$\overline{CS}$ (Input)

$\overline{CS}$ is an active-low, chip-select signal. CS is also used as a control signal to trigger a conversion on the falling edge. Each data frame begins with the falling edge of the $\overline{CS}$ signal. The analog input channel to be converted during a particular frame is selected in the previous frame. On the $\overline{CS}$ falling edge, the devices sample the input signal from the selected channel and a conversion is initiated using the internal clock. The device settings for the next data frame can be input during this conversion process. When the $\overline{CS}$ signal is high, the ADC is considered to be in an idle state.

SCLK (Input)

This pin is the clock input for the data interface. All synchronous accesses to the device are timed with respect to the falling edges of the SCLK signal.

SDI (Input)

SDI is the data input line. SDI is used by the host processor to program the internal device registers for device configuration. At the beginning of each data frame, the CS signal goes low and the data on the SDI line are read by the device at every falling edge of the SCLK signal for the next 16 SCLK cycles. Any changes made to the device configuration in a particular data frame are applied to the device on the subsequent falling edge of the $\overline{CS}$ signal.

SDO (Input)

SDO is the data output line. SDO is used by the device to output conversion data. The size of the data output frame varies depending on the register setting for the SDO format. A low level on $\overline{CS}$ releases the SDO pin from the Hi-Z state. SDO is kept low for the first 15 SCLK falling edges. The MSB of the output data stream is clocked out on SDO on the 16th SCLK falling edge, followed by the subsequent data bits on every falling edge thereafter. The SDO line goes low after the entire data frame is output and goes to a Hi-Z state when $\overline{CS}$ goes high.

4.1.2 Input Range Supported

This TI design supports the following input ranges.

VOLTAGE INPUT	
DC Voltage	0- to 10-V DC 0- to 5-V DC
Number of Voltage Input Channels	2
Input Impedance for Voltage Channels	> 1 MΩ
Connector Details	AIN0 -> J2.1 - J2.2 AIN1 -> J2.3 - J2.4
CURRENT INPUT	
DC Current	0- to 20-mA DC 0- to 24-mA DC 4- to 20-mA DC
Input Impedance for Current Input Channel	< 300 Ω
Number of Current Inputs	2
Connector Details	AIN3 -> J2.5 - J2.6 AIN4 -> J2.7- J2.8
ACCURACY	
For Both Current and Voltage Inputs	< 0.2% Full scale

On the AINx line 100-Ω resistors are used to protect the input Zener (CSDO323) from high current due to EMI. A 1-K resistor is also used for overvoltage protection. To create balance, a 1.11-K resistor is used in the return line AIN_xGND. After these balancing resistors, AIN_xGND is connected to signal ground through the 0-Ω resistor.

4.1.3 Power Supply Requirement

VOLTAGE	VOLTAGE – V	I – mA
Analog supply	5	11.5 mA
Digital supply	3.3	1

The analog power supply of 5.0 V derives from a 15-V supply using an LDO TPS7A1650.

The digital power supply of 3.3 V derives from a 15-V supply using an LDO TPS7A1633. View further details about the power supply of this design in Section 4.2.3.

4.1.4 Schematics

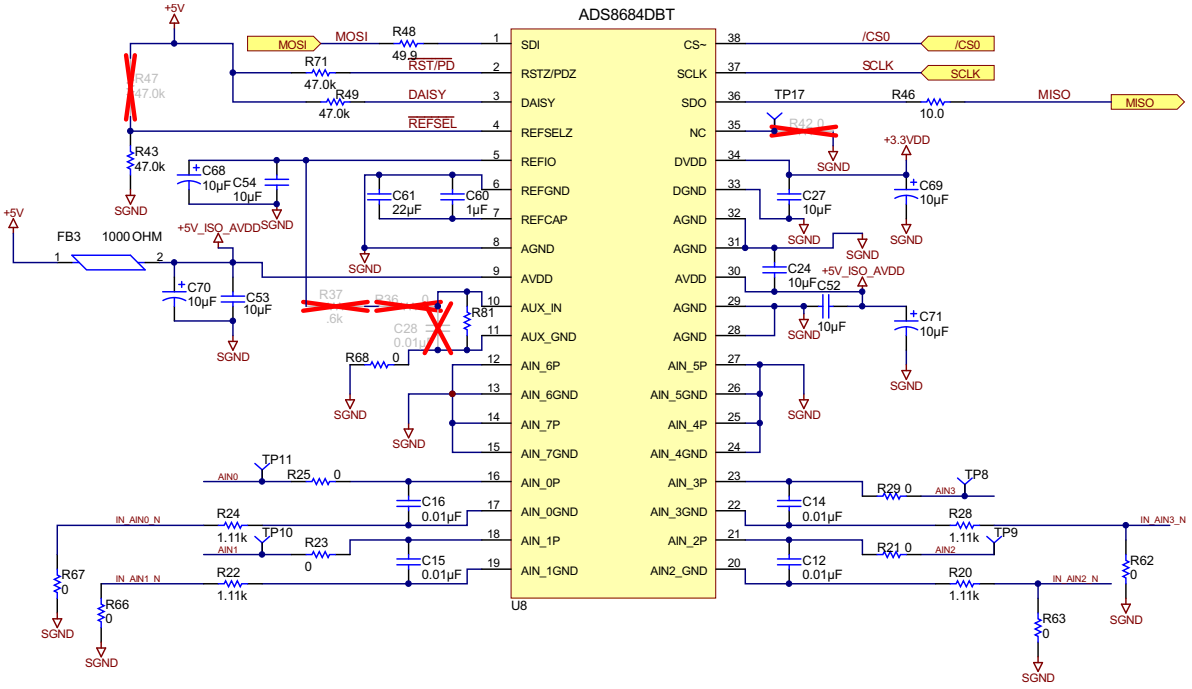


Figure 6. Analog I/P ADSC8684 Interface

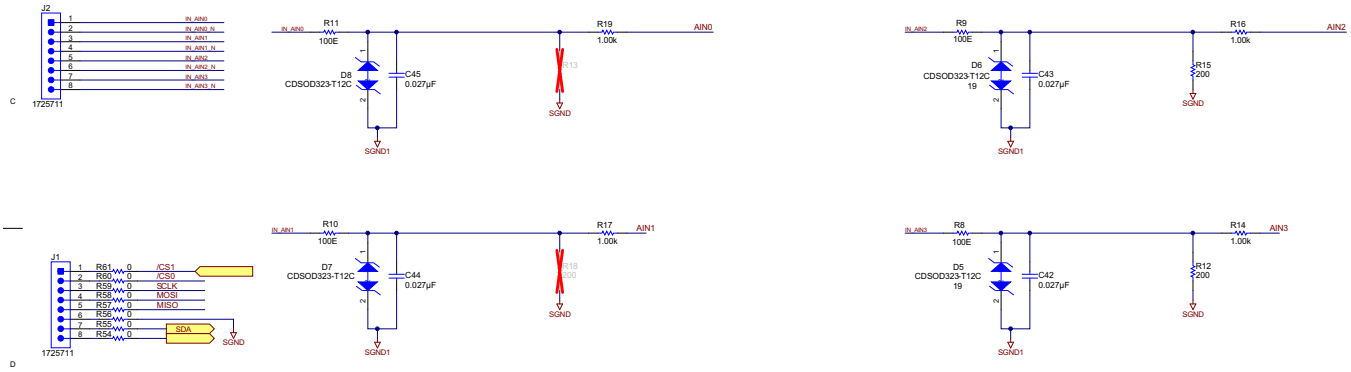


Figure 7. Analog I/P Front End

4.2 Analog Output

4.2.1 DAC Description

This design uses the DAC8760 device. DAC8760s are low-cost, precision, fully-integrated, 16-bit DACs designed to meet the requirements of smart grid process-control applications. The DAC8760 device has the following features:

- DC current output: 4 to 20 mA, 0 to 20 mA, and 0 to 24 mA
- DC voltage output: 0 to 5 V, 0 to 10 V, ±5 V, ±10 V, 0 to 5.5 V, 0 to 11 V, ±5.5 V, and ±11 V
- ±0.1% Full-scale reading (FSR) total unadjusted error (TUE) max
- DNL: ±1 LSB max
- Simultaneous voltage and current output
- Internal 5-V reference (10 ppm/°C, max)
- Internal 4.6-V power supply output
- Reliability features:
  - CRC check and watchdog timer
  - Thermal alarm
  - Open alarm, short current limit
- Wide temperature range: –40°C to +125°C
- Devices can superimpose an external HART® signal on the current output and can operate with either a single 10- to 36-V supply, or dual supplies of up to ±18 V

AO1 and AO2 can be configured for either voltage output or for current output. Both AO1 and AO2 support the following ranges:

1. 0- to 5-V DC, 0- to 10-V DC
2. 0- to 20-mA DC, 0- to 24-mA DC, and 4- to 20-mA DC
3. For V_{OUT}: R_L = 1 kΩ, C_L= 200 pF; for I_{OUT}: R_L = 300 Ω

4.2.1.1 DAC Architecture

The DAC8760 consists of a resistor-string DAC followed by a buffer amplifier. The output of the buffer drives the current output and the voltage output. The resistor-string section is simply a string of resistors, each of value R, from REF to GND. This type of architecture ensures the DAC is monotonic.

The current-output stage converts the voltage output from the string to current. The voltage output provides a buffered output of the programmed range to the external load. When the current output or the voltage output is disabled, the analog output is in a high impedance (Hi-Z) state. After power-on, both output stages are disabled.

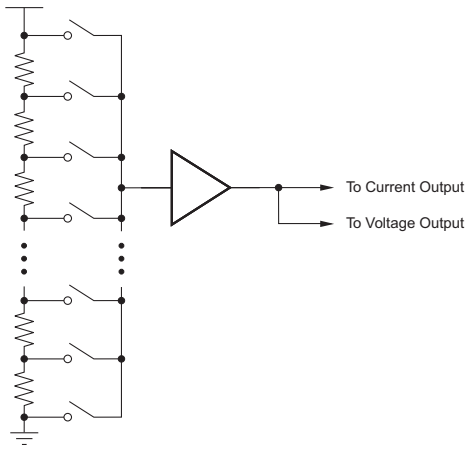


Figure 8. DAC Structure: Resistor String of DAC8760

4.2.1.2 Voltage Output Stage

The voltage output stage as shown in Figure 9 provides the voltage output according to the DAC code and output range setting. The output range can be programmed as 0 V to 5 V or 0 V to 10 V for unipolar output mode and ±5 V or ±10 V for bipolar output mode. In addition, an option is available to increase the output voltage range by 10%. The output current drive can be up to 10 mA. The output stage has short-circuit current protection that limits the output current to 30 mA. The voltage output is able to drive a capacitive load up to 1 µF. For loads greater than 20 nF, an external compensation capacitor can be connected between CMP and VOUT to keep the output voltage stable at the expense of reduced bandwidth and increased settling time.

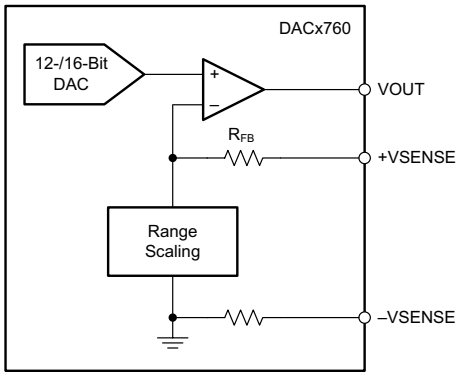


Figure 9. Voltage Output

The +VSENSE pin is provided to enable sensing of the load by connecting to points electrically closer to the load. This configuration allows the internal output amplifier to make sure that the correct voltage is applied across the load, as long as headroom is available on the power supply. Ideally, this pin is used to correct for resistive drops on the system board and is connected to VOUT at the terminals. In some cases, both VOUT and +VSENSE are brought out as terminals and, through separate lines, connected remotely together at the load. In such cases, if the +VSENSE line is cut, the amplifier loop is broken; use an optional 5-kΩ resistor between VOUT and +VSENSE to prevent this from occurring. The –VSENSE pin, on the other hand, is provided as a GND sense reference output from the internal VOUT amplifier. The output swing of the VOUT amplifier is relative to the voltage seen at this pin. The actual voltage difference between the –VSENSE pin and the device GND pins is not expected to be more than a few 100 µV. The internal resistor shown in Figure 9 between the device internal GND and the –VSENSE pin is typically 2 kΩ.

After power on, the power-on-reset circuit confirms that all registers are at default values. The voltage output buffer is in a Hi-Z state; however, the +VSENSE pin connects to the amplifier inputs through an internal 60-kΩ feedback resistor (R_{FB} in Figure 9). If the VOUT and +VSENSE pins are connected together, the VOUT pin is also connected to the same node through the feedback resistor. This node is protected by internal circuitry and settles to a value between GND and the reference input.

The output voltage (VOUT) can be expressed as Equation 1 and Equation 2.

For unipolar output mode:

$$VOUT = VREF \times GAIN \times \frac{CODE}{2^N} \quad (1)$$

For bipolar output mode:

$$VOUT = VREF \times GAIN \times \frac{CODE}{2^N} - GAIN \times \frac{VREF}{2} \quad (2)$$

where

- *CODE* is the decimal equivalent of the code loaded to the DAC.
- *N* is the bits of resolution; 16 for DAC8760 and 12 for DAC7760.
- *VREF* is the reference voltage; for internal reference, VREF = +5.0 V.
- *GAIN* is automatically selected for a desired voltage output range as shown in Table 3.

Table 3. Voltage Output Range vs Gain Setting

VOLTAGE OUTPUT RANGE	GAIN
0- to 5-V	1
0- to 10-V	2
±5 V	2
±10 V	4

4.2.1.3 Current Output Stage

The current output stage consists of a pre-conditioner and a current source as shown in Figure 10. This stage provides a current output according to the DAC code. The output range can be programmed as 0 to 20 mA, 0 to 24 mA, or 4 to 20 mA. An external boost transistor can be used to reduce the power dissipation of the device. The maximum compliance voltage on pin IOUT equals (AVDD – 2 V). In single power supply mode, the maximum AVDD is 36 V and the maximum compliance voltage is 34 V. After power-on, the IOUT pin is in a Hi-Z state.

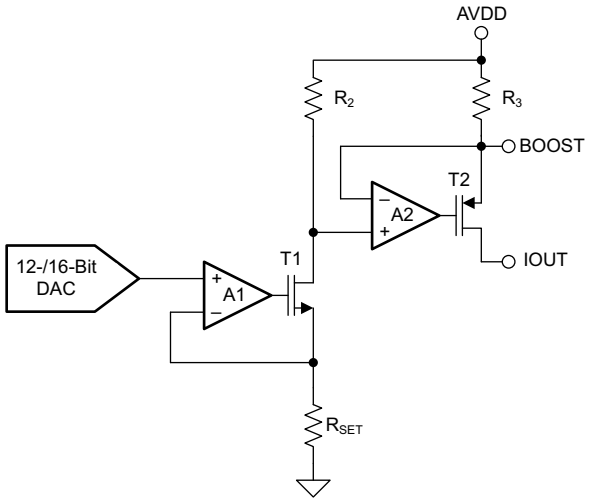


Figure 10. Current Output

Resistor R_{SET} (used to convert the DAC voltage to current) determines the stability of the output current over temperature. If desired, an external, low-drift, precision 15-kΩ resistor can be connected to the ISET-R pin and used instead of the internal R_{SET} resistor.

For a 5-V reference, the output can be expressed as Equation 3, Equation 4, and Equation 5.

For a 0- to 20-mA output range:

$$IOUT = 20\ mA \times \frac{CODE}{2^N} \quad (3)$$

For a 0- to 20-mA output range:

$$IOUT = 24\ mA \times \frac{CODE}{2^N} \quad (4)$$

For a 4- to 20-mA output range:

$$IOUT = 16\ mA \times \frac{CODE}{2^N} + 4\ mA \quad (5)$$

where

- *CODE* is the decimal equivalent of the code loaded to the DAC.
- *N* is the bits of resolution; 16 for DAC8760.

4.2.1.4 DAC Clear

The DAC has an asynchronous clear function through the CLR pin which is active high and allows the voltage output to be cleared to either zero-scale code or midscale code. This action is user selectable through the CLR-SEL pin or the CLRSEL bit. The CLR-SEL pin and CLRSET register are ORed together. The current output clears to the bottom of its preprogrammed range. When the CLR signal returns to low, the output remains at the cleared value. The pre-clear value can be restored by pulsing the LATCH signal without clocking any data. A new value cannot be programmed until the CLR pin returns to low.

In addition to defining the output value for a clear operation, the CLRSEL bit and CLR-SEL pin also define the default output value. During the selection of a new voltage range, the output value corresponds to the definitions given in Table 4.

Table 4. CLR-SEL Options

CLR-SEL	OUTPUT VALUE	
	UNIPOLAR OUTPUT RANGE	BIPOLAR OUTPUT RANGE
0	0 V	0 V
1	Midscale	Negative full-scale

The CLR-SEL pin is shorted to ground for both DACs.

4.2.2 Range Supported

Table 5. Analog Output Range

NUMBER OF OUTPUTS	2 Channels
VOLTAGE OUTPUT(1)(2)	0- to 5-V DC
	0- to 10-V DC
CURRENT OUTPUT(1)(2)	4- to 20-mA DC
	0- to 20-mA DC
	0- to 24-mA DC

(1) Either current or voltage output mode is configurable.
(2) For V_{OUT}: R_L = 1 kΩ, C_L= 200 pF; for I_{OUT}: R_L = 300 Ω.

4.2.3 Power Supply

This design uses +15 V as AVDD and –15 V for AVSS. These inputs are directly applied from an external DC digital power supply, 3.3 V is derived from a 15-V supply using an LDO TPS7A1633. Further details concerning power supply are given in Section 4.2.3.2 and Section 4.2.3.3.

4.2.3.1 Internal Reference

The DAC8760 includes an integrated 5-V reference with a buffered output (REFOUT) capable of driving up to 5 mA (source or sink) with an initial accuracy of ±5 mV maximum and a temperature drift coefficient of 10 ppm/°C maximum.

4.2.3.2 Digital Power Supply

An internally generated 4.6-V supply capable of driving up to 10 mA can be output on DVDD by leaving the DVD-EN pin unconnected. The supply eases the system supply design especially when isolation barriers must be crossed to generate the digital supply. If an external supply is preferred, the DVDD pin can be made into an input by tying DVDD-EN to GND.

4.2.3.3 Power Supply Sequence

The DAC8760 has internal power-on reset (POR) circuitry for both the digital DVDD and analog AVDD supplies. This circuitry ensures that the internal logic and power-on state of the DAC power up to the proper state independent of the supply sequence. While there is no required supply power-on sequence, the recommendation is to first have the digital DVDD supply come up, followed by the analog supplies, AVDD and AVSS. AVSS is powered assuming a negative supply is being used; otherwise, AVSS is tied to GND.

4.2.4 SPI

The device is controlled over a versatile four-wire serial interface (SDI, SDO, SCLK, and LATCH) that operates at clock rates of up to 30 MHz and is compatible with SPI, QSPI™, Microwire, and digital signal processing (DSP) standards.

4.2.4.1 Daisy Chain Operation

For systems that contain multiple DAC8760s, the SDO pin is used to daisy-chain in the SPI. This mode is useful in reducing the number of serial interface lines in applications that use multiple SPI devices. Daisy-chain mode is enabled by setting the DCEN bit of the control register to '1'. By connecting the SDO of the first device to the SDI input of the next device in the chain, a multiple-device interface is constructed, as Figure 11 shows.

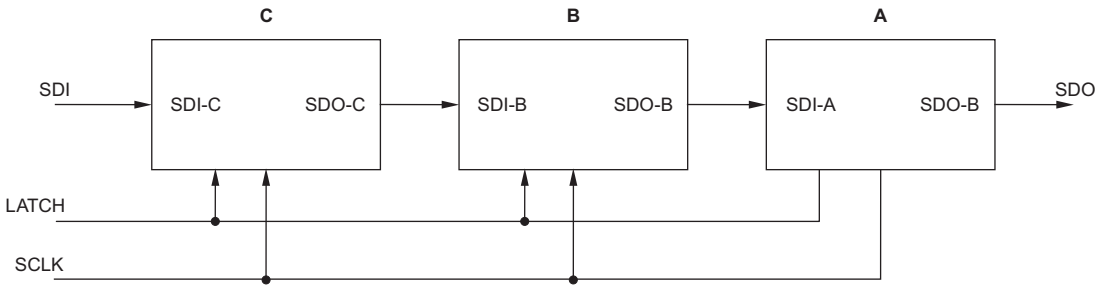


Figure 11. DAC8760 in Daisy-Chain Mode

Like stand-alone operation, the SPI daisy-chain write operation requires one frame, and the read requires two frames. The rising edge of SCLK that clocks in the most significant bit (MSB) of the input frame marks the beginning of the write cycle. When the serial transfer to all devices is complete, LATCH is taken high. This action transfers the data from the SPI shift registers to the device internal register of each DAC8760 in the daisy-chain. However, the number of clocks in each frame in this case depends on the number of devices in the daisy chain. For two devices, each frame is 48 clocks; the first 24 clocks are for the second

DAC and the next 24 bits are for the first DAC. For a readback, the data are read from the two DACs in the following 48-bit frame; the first 24 clocks are for the second DAC and the next 24 clocks are for the first DAC. The input data to the DACs during the second frame can be another command or NOP. Similar to the two-device case described, for N devices, each frame is N × 24 clocks, where *N* is the total number of the DAC8760s in the chain.

The serial clock can be a continuous or gated clock. A continuous SCLK source can only be used if LATCH is taken high after the correct number of clock cycles. In gated clock mode, a burst clock containing the exact number of clock cycles must be used and LATCH must be taken high after the final clock to latch the data.

4.2.5 Buffering

In this design, VOUT and IOUT are tied together and never simultaneously enabled.

Special consideration must be paid to the +VSENSE pin in this case. When VOUT is disabled, the +VSENSE pin is connected to the internal amplifier input through an internal 60-kΩ resistor. This internal node has diode clamps to REFIN and GND. Setting bit 6 of the configuration resistor forces this internal node to be tied to GND via a 10-kΩ resistor—in effect, the +VSENSE pin is tied to GND through a 70-kΩ power-down resistor.

Whether the APD bit is set or not set, the current output in this case incurs a gain error because the internal resistor acts as a parallel load in addition to the external load. If this gain error is undesirable, it can be corrected through use of the application circuit as shown in Figure 12.

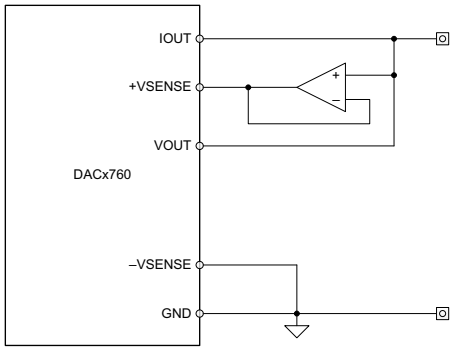


Figure 12. VOUT and IOUT Tied Together to One Terminal

The buffer amplifier prevents leakage through the internal 60-kΩ resistor in current output mode and does not allow it to be seen as a parallel load. The VOUT pin is in high impedance mode in this case and will allow minimal leakage current. Note that the offset of the external amplifier will add to the overall VOUT offset error and any potential phase shift from the external amplifier can cause VOUT stability issues.

4.2.6 Schematics

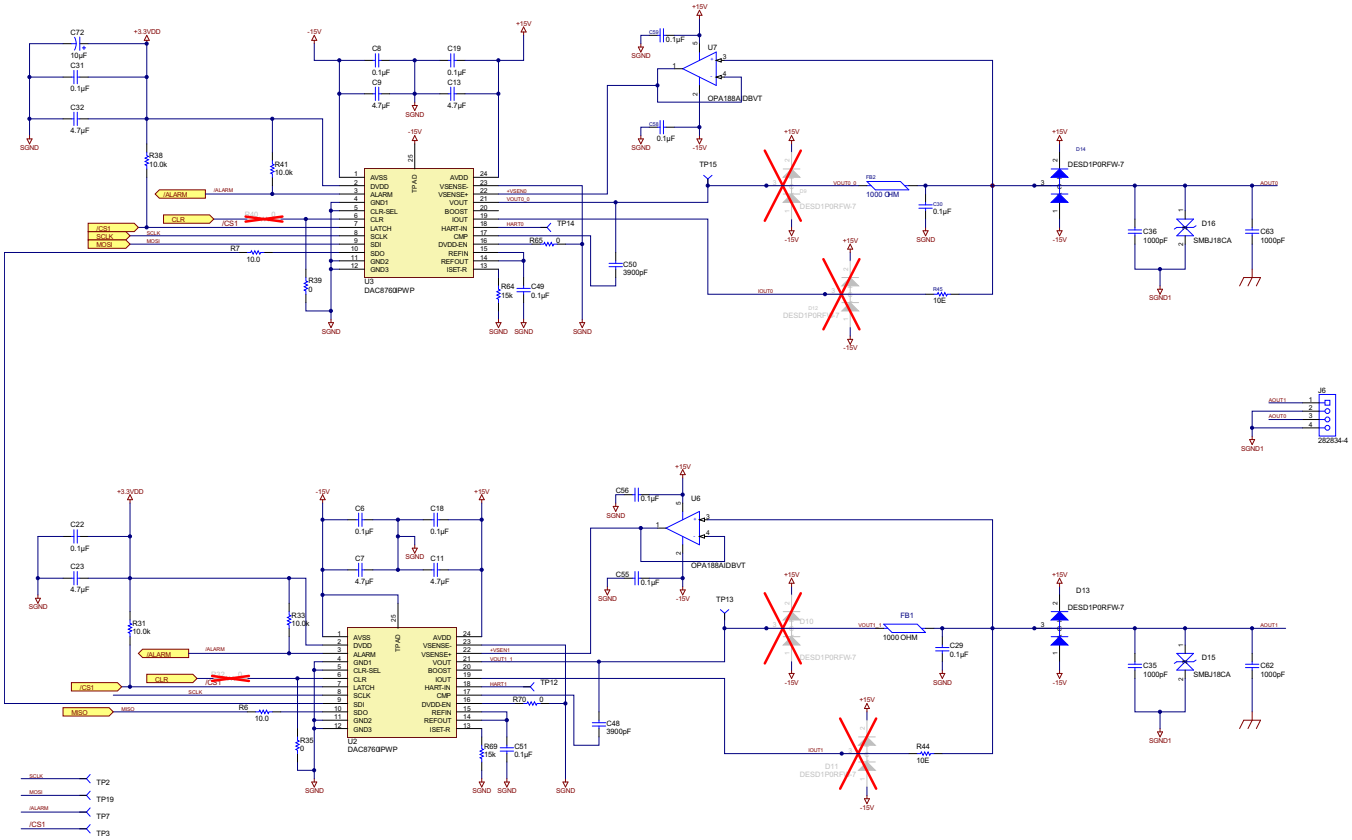


Figure 13. Analog Output

4.3 Relay Drive Outputs

This TI design provides six high-current relay driver outputs.

4.3.1 Low Side Relay Driver

The TPL7407L is a high-voltage, high-current NMOS transistor array. This device consists of seven NMOS transistors that feature high-voltage outputs with common-cathode clamp diodes for switching inductive loads. The maximum drain-current rating of a single NMOS channel is 600 mA.

The key benefit of the TPL7407L is its improved power efficiency and lower leakage than a Bipolar Darlington Implementation. The TPL7407L device features the following:

- 600-mA rated drain current (per channel)
- Power efficient (very low V_{OL})
  - Less than 4 times lower V_{OL} at 100 mA than Darlington array
- Very low output leakage < 10 nA per channel
- Compatible with 1.8-V to 5.0-V microcontrollers and logic interface
- Internal free-wheeling diodes for inductive kick-back protection
- Input RC-snubber to eliminate spurious operation in noisy environments

4.3.1.1 TPL7407L Functional Block Diagram

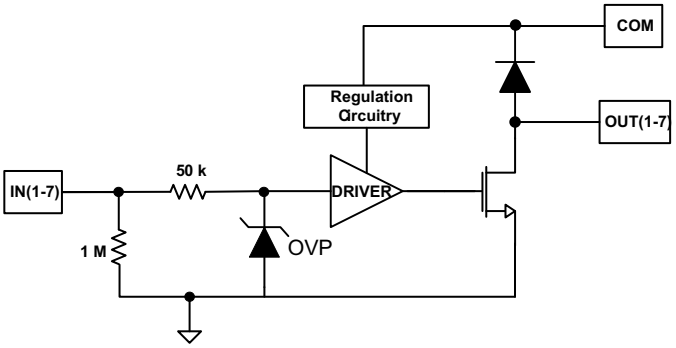


Figure 14. TPL7407L Functional Block Diagram

The TPL7407L comprises seven high voltage, high current NMOS transistors tied to a common ground driven by internal level shifting and gate drive circuitry. The TPL7407L offers solutions to many interface needs, including solenoids, relays, lamps, small motors, and LEDs. Applications requiring sink currents beyond the capability of a single output may be accommodated by paralleling the outputs.

Each channel of TPL7407L consists of high power, low-side NMOS transistors driven by level shifting and gate driving circuitry. The gate drivers allow for high output current drive with a very low input voltage, essentially equating to operability with low general purpose input and output (GPIO) voltages.

In order to enable floating inputs, a 1-MΩ pull-down resistor exists on each channel. Another 50-kΩ resistor exists between the input and gate-driving circuitry. This resistor exists to limit the input current whenever there is an overvoltage and the internal Zener clamps. The resistor also interacts with the inherent capacitance of the gate driving circuitry to behave as an RC snubber to help prevent spurious switching in a noisy environment.

In order to power the gate driving circuitry an LDO exists. The diodes connected between the output and COM pin are used to suppress kick-back voltage from an inductive load that is excited when the NMOS drivers are turned off (stop sinking) and the stored energy in the coils causes a reverse current to flow into the coil supply.

4.3.1.2 TTL and Other Logic Inputs

TPL7407L input interface is specified for the standard 1.8-V through 5-V complementary metal oxide semiconductor (CMOS) logic interface and can tolerate up to 30 V. At any input voltage, the output drivers are driven at the maximum when V_{COM} is greater than or equal to 8.5 V.

4.3.1.3 Input RC Snubber

TPL7407L features an input RC snubber that helps prevent spurious switching in noisy environments. Connect an external 1-kΩ to 5-kΩ resistor in series with the input to further enhance the TPL7407Ls noise tolerance.

4.3.1.4 High-Impedance Input Driver

TPL7407L features a 1-MΩ input pull-down resistor. The presence of this resistor allows the input drivers to be tri-stated. When a high-impedance driver is connected to a channel input, the TPL7407L device detects the channel input as a low-level input and remains in the OFF position. The input RC snubber helps improve noise tolerance when input drivers are in the high-impedance state.

4.3.1.5 Drive Current

The coil current is determined by the coil voltage (V_{SUP}), coil resistance, and output low voltage (V_{OL}).

$I_{COIL} = (V_{SUP} – V_{OL}) / R_{COIL}$

The output low voltage (VOL) is the drain to source (VDS) voltage of the output NMOS transistors when the input is driven high and the transistor is sinking current.

4.3.1.6 Thermal Considerations

The number of coils driven is dependent on the coil current and on-chip power dissipation.

For a more accurate determination of number of coils possible, use Equation 6 to calculate TPL7407Ls on-chip power dissipation P_D:

$$P_D = \sum_{i=1}^{N} V_{OLi} \times I_{Li} \quad (6)$$

where

- N is the number of channels active together.
- V_{OLi} is the OUT_i pin voltage for the load current I_{Li}. This is the same as $V_{CE(SAT)}$.

In order to guarantee reliability of TPL7407L and the system, the on-chip power dissipation must be lower than or equal to the maximum allowable power dissipation ($P_{D(MAX)}$) dictated by Equation 7.

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA} \quad (7)$$

where

- $T_{J(MAX)}$ is the target maximum junction temperature.
- T_A is the operating ambient temperature.
- θ_{JA} is the package junction to ambient thermal resistance.

TI recommends to limit TPL7407L ICs die junction temperature to less than 125°C. The IC junction temperature is directly proportional to the on-chip power dissipation.

4.3.1.7 Power Supply Recommendation

The COM pin is the power supply pin of this device to power the gate drive circuitry. This design ensures full drive potential with any GPIO above 1.5 V. The gate drive circuitry is based on low voltage CMOS transistors that can only handle a max gate voltage of 7 V. An integrated LDO reduces the COM voltage of 8.5 V to 40 V to a regulated voltage of 7 V. Though 8.5 V minimum is recommended for V_{COM}, the part still functions with a reduced COM voltage, with a reduced gate drive voltage, and a resulting higher Rds(on).

To prevent overvoltage on the internal LDO output due to a line transient on the COM pin, the COM pin must be limited to below 3.5 V/µs. Faster slew-rate (or hot-plug) may cause damage to the internal gate driving circuitry due to the LDOs inability to clamp a fast-input transient fast enough. Because most modern power supplies are loaded by capacitors > 10 µF, this inability to clamp should not be of any concern. TI recommends to use a bypass capacitor that limits the slew rate to below 0.5 V/µs.

In summary, whenever the COM pin experiences a slew rate greater than 0.5 V/µs, a capacitor must be added to limit the slew to < 0.5 V/µs.

4.3.1.8 Layout Recommendation

Thin traces can be used on the input due to the low current logic that is typically used to drive the TPL7407L device. Care must be taken to separate the input channels as much as possible, as to eliminate cross-talk. Thick traces are recommended for the output to drive whatever high currents that may be needed. Determine the wire thickness by the current density and desired drive current of the trace material.

Because all of the channels currents return to a common ground, the best method is to size that trace width to be very wide—some applications require up to 2 A.

Because the COM pin only draws up to 25 µA, thick traces are not necessary.

4.3.2 I2C I/O Expander

This TI design uses an I2C I/O expander to provide digital inputs for driving the relay driver inputs. The TCA6408A is a low voltage 8-bit I2C I/O expander. The device is compliant to a 400-KHz fast I2C bus.

The bidirectional voltage-level translation in the TCA6408A is provided through V_{CCI}. The V_{CCI} is to be connected to the V_{CC} of the external SCL/SDA lines. This connection indicates the V_{CC} level of the I2C bus to the TCA6408A device. The voltage level on the P-port of the TCA6408A is determined by V_{CCP}.

The TCA6408A consists of one 8-bit configuration (input or output selection), input, output, and polarity inversion (active high) register. At power on, the I/Os are configured as inputs. However, the system master can enable the I/Os as either inputs or outputs by writing to the I/O configuration bits. The data for each input or output is kept in the corresponding input or output register. The polarity of the input port register can be inverted with the polarity inversion register. The system master can read all registers.

The system master can reset the TCA6408A in the event of a timeout or other improper operation by asserting a low in the $\overline{\text{RESET}}$ input. The power-on reset puts the registers in their default state and initializes the I2C state machine. The $\overline{\text{RESET}}$ pin causes the same reset and initialization to occur without depowering the part.

The TCA6408A open-drain interrupt ($\overline{\text{INT}}$) output activates when any input state differs from its corresponding input port register state and is used to indicate to the system master that an input state has changed.

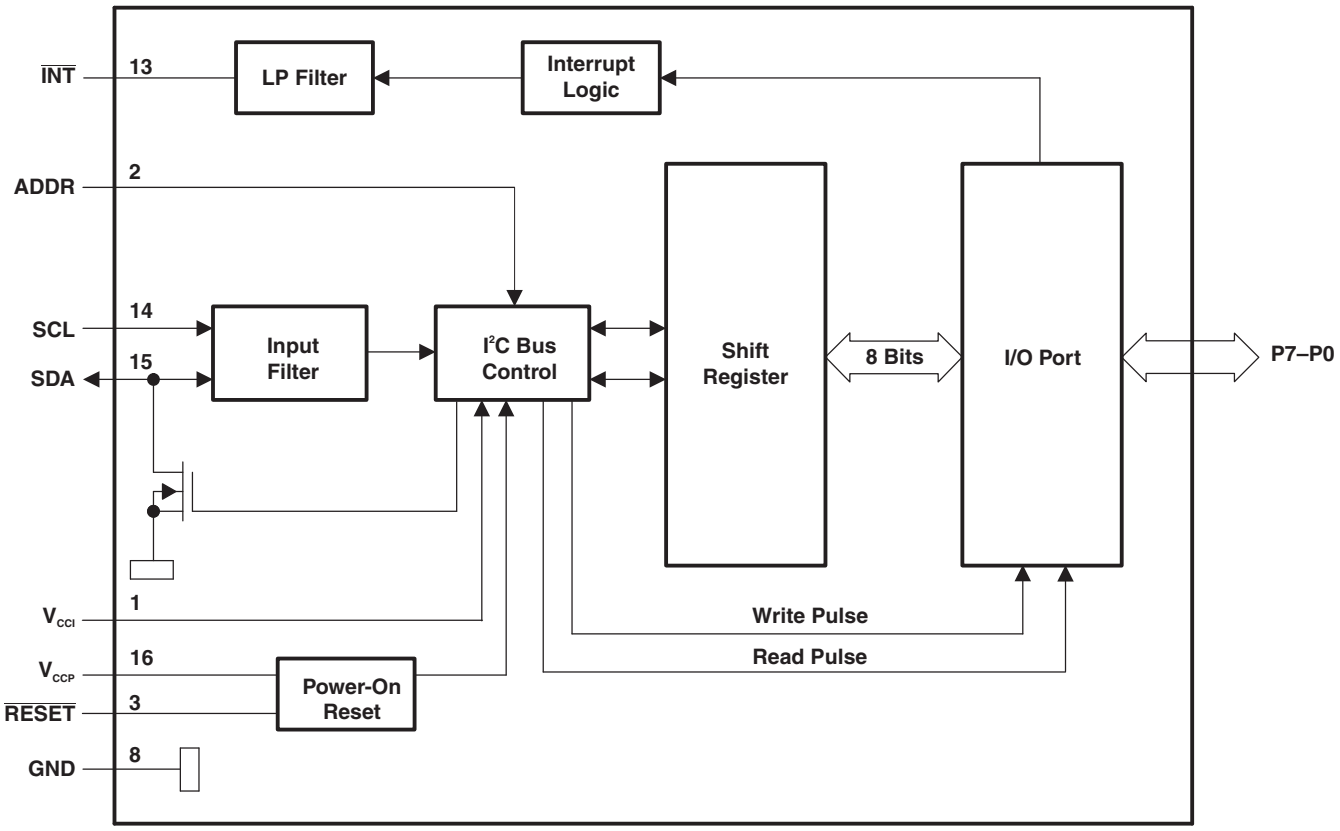
$\overline{\text{INT}}$ can be connected to the interrupt input of a microcontroller. By sending an interrupt signal on this line, the remote I/O can inform the microcontroller if there is incoming data on its ports without having to communicate through the I2C bus. Thus, the TCA6408A can remain a simple slave device.

The device P-port outputs have high-current sink capabilities for directly driving LEDs while consuming low device current.

As shown in Table 6, one hardware pin (ADDR) can be used to program the I2C address to allow two devices to share the same I2C bus.

Table 6. Address Reference

ADDRESS	I2C BUS SLAVE ADDRESS
L	32 (decimal), 20 (hexadecimal)
H	33 (decimal), 21 (hexadecimal)



A All pin numbers shown are for the PW package. B. All I/Os are set to inputs at reset.

Figure 15. TCA6408 I2C to Parallel Bus Expander Block

Table 7. Terminal Functions

TERMINAL			NAME	DESCRIPTION
NUMBER				
TSSOP (PW)	µQFN (RSV)	QFN (RGT)		
1	15	15	V_{CCI}	Supply voltage of I^2C bus. Connect directly to the V_{CC} of the external I^2C master. Provides voltage level translation.
2	16	16	ADDR	Address input. Connect directly to V_{CCP} or ground.
3	1	1	$\overline{RESET}$	Active-low reset input. Connect to V_{CCI} through a pull-up resistor, if no active connection is used.
4	2	2	P0	P-port input/output (push-pull design structure). At power on, P0 is configured as an input.
5	3	3	P1	P-port input/output (push-pull design structure). At power on, P1 is configured as an input.
6	4	4	P2	P-port input/output (push-pull design structure). At power on, P2 is configured as an input.
7	5	5	P3	P-port input/output (push-pull design structure). At power on, P3 is configured as an input.
8	6	6	GND	Ground.
9	7	7	P4	P-port input/output (push-pull design structure). At power on, P4 is configured as an input.
10	8	8	P5	P-port input/output (push-pull design structure). At power on, P5 is configured as an input.
11	9	9	P6	P-port input/output (push-pull design structure). At power on, P6 is configured as an input.

Table 7. Terminal Functions (continued)

12	10	10	P7	P-port input/output (push-pull design structure). At power on, P7 is configured as an input.
13	11	11	$\overline{INT}$	Interrupt output. Connect to V_{CCI} through a pull-up resistor.
14	12	12	SCL	Serial clock bus. Connect to VCCI through a pull-up resistor.
15	13	13	SDA	Serial data bus. Connect to VCCI through a pull-up resistor.
16	14	14	V_{CCP}	Supply voltage of TCA6408A for P-port.

4.3.3 Schematics

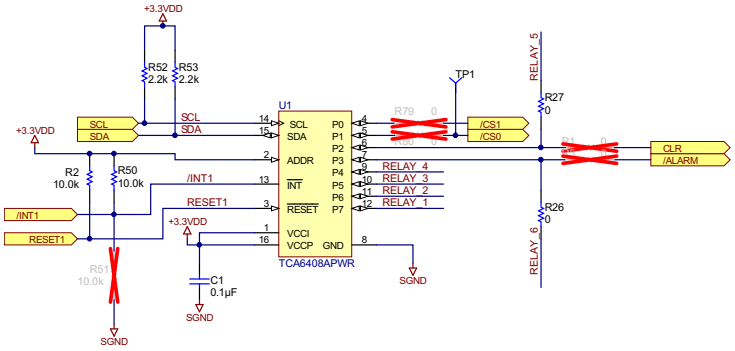


Figure 16. I2C I/O Expander

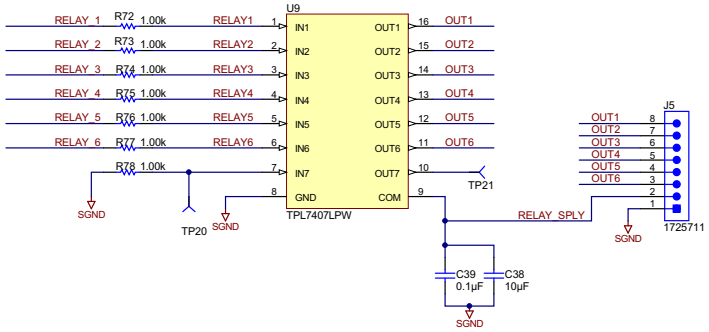


Figure 17. Digital Output Relay Driver

4.4 Power Supply

This TI design requires the following power supplies.

1. 15-V DAC analog supply
2. –15-V DAC analog supply
3. 3.3-V Digital power supply
4. 5.0-V Analog power supply

4.4.1 Supply Input

This design has the following power supply inputs.

- 15 V
- –15 V
- Ground

4.4.2 Analog Power Supply for DAC

A ±15-V supply is directly used for DAC analog supply in the analog output module. Both ±15 V are properly decoupled at the input connector and at the analog power supply of DAC8760. A +15-V supply is also used for generating 3.3-V and 5.0-V supplies.

4.4.3 Digital Power Supply +3.3 V and Analog Power Supply +5.0 V (For ADC)

For generating a 3.3-V digital power supply, this TI design uses a TPS7A1633 LDO. For generating a 5.0-V analog power supply for ADC, this TI design uses a TPS7A16450 LDO. The TPS7A16 family of ultra-low power, LDO voltage regulators offers the benefits of an ultra -low quiescent current, high input voltage, and miniaturized, high thermal-performance packaging. The TPS7A16 family is designed for continuous or sporadic (power backup) battery-powered applications where ultra-low quiescent current is critical to extending system battery life. The following are features of the TPS7A series LDO.

- Wide input voltage range: 3 V to 60 V
- Ultra-low quiescent current: 5 µA
- Quiescent current at shutdown: 1 µA
- Output current: 100 mA
- Low dropout voltage: 60 mV at 20 mA
- Accuracy: 2% power good with programmable delay
- Current-limit and thermal shutdown
- Stable with ceramic output capacitors: ≥ 2.2 µF

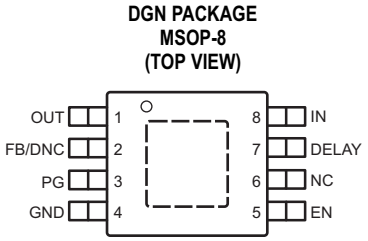


Figure 18. Pin Configuration TPS7A1633

4.4.4 Schematics

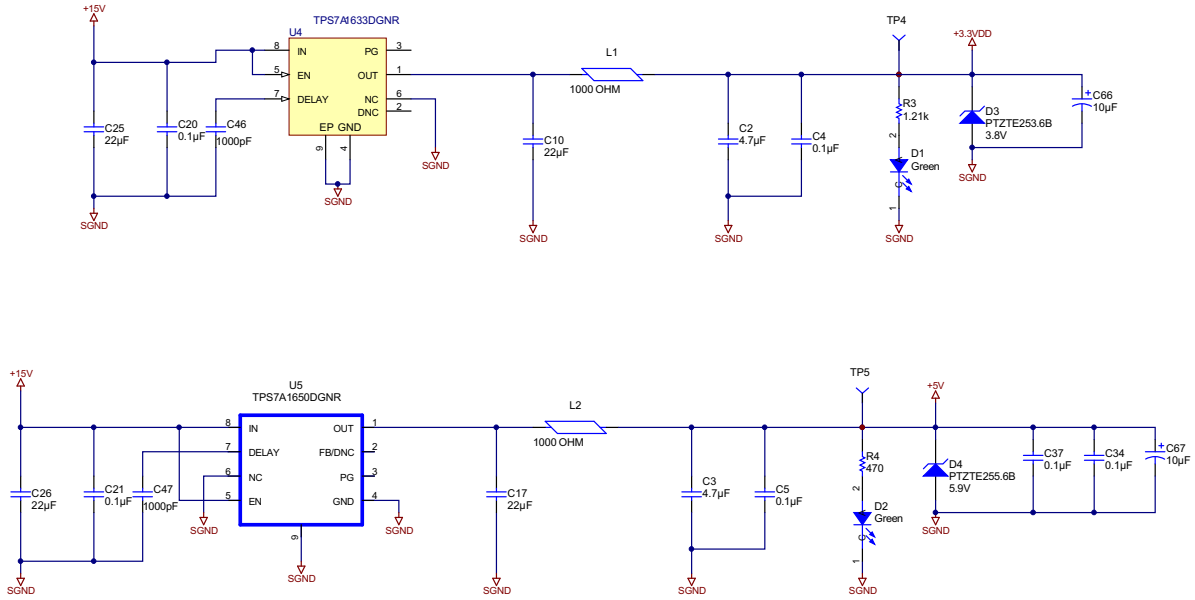


Figure 19. Digital Power Supply 3.3 V and Analog Power Supply 5.0-V Regulators

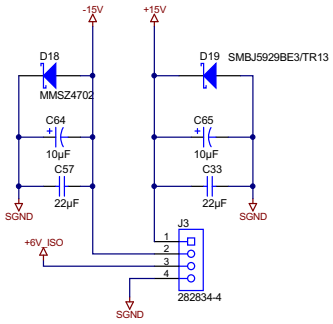


Figure 20. Front End Power Supply Connector and Filter

4.5 Host Controller Interface

4.5.1 Host Controller Details

The testing for this TI design uses the TM4C1294 LaunchPad Evaluation Board. The Tiva™ C-Series TM4C1294 Connected LaunchPad Evaluation Board (EK-TM4C1294XL) is a low-cost evaluation platform for ARM® Cortex™-M4F-based microcontrollers. The Connected LaunchPad design highlights the TM4C1294NCPDT microcontroller with its on-chip 10/100 Ethernet MAC and PHY, USB 2.0, hibernation module, motion control pulse-width modulation, and a multitude of simultaneous serial connectivity.

4.5.2 Host Controller

The following lines are used for the interfacing with the TI design board from the LaunchPad.

- SPI Clock ---- PA2
- SPI MOSI ---- PA4
- SPI MISO ---- PA5
- SPI Chip Select for ADC -- PA3
- I2C Clock(SCLK) -- PB2
- I2C Data(SDATA) -- PB3
- SPI Chip select for DAC: PK3
- Ground

4.5.3 SPI and I2C Communication

The TIVA controller used in the LaunchPad kit has an SPI peripheral module with an SPI clock that can reach up to 30 MHz. To get the 500-kSPS sampling rate of the ADS8684 device, set the SPI clock rate to 17 MHz; and for the DAC8760 device, set the SPI clock rate to 4 MHz.

TIVA has an I2C peripheral module to support standard, fast, and high-speed modes of I2C communication. This module can be used to communicate with the I/O expander at the standard mode (100 KHz).

4.5.4 Connector

J1 is an 8-pin, 2.54-mm pitch connector that has chip select signals (CS0 and CS1) for ADC and DAC, the SPI standard signal, ground, and the I2C standard signal.

4.5.5 Schematic

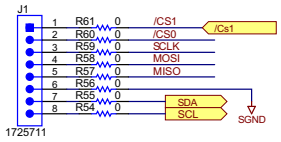


Figure 21. J1 Connector

4.6 Protection

4.6.1 Analog Input

The goal of electromagnetic compatibility (EMC)-protected circuitry is to shunt any sort of external transient to earth ground with low impedance and protect the analog input module from damage. The 100R pulse withstanding resistors protect each analog input line against overcurrent occurrences due to high voltage EMI phenomenon. The RC filter, comprised by a 100-Ω resistor and a 0.027-µF capacitor, filters out all high-frequency disturbances. The bidirectional transient voltage suppressor (CDSOD323-T12C) protects each analog input line from ESD.

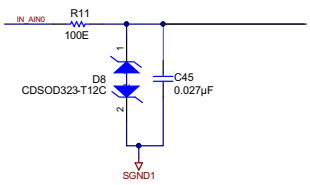


Figure 22. Analog Input EMC Protection

4.6.2 Analog Output

The output stage is designed to withstand ±4-kV of contact discharge. The TVS SMBJ18CA protects every channel. This circuit clamps overvoltage inputs to approximately 25 V. The ESD protection diodes also protect against overvoltage inputs. Layout guidelines must be followed to ensure compliance to EMC standards. The selected protection devices are chosen to dissipate the required energy. There are also Y-capacitors connected across the analog output and earth for filtering out all high frequency disturbances. There are overvoltage clamping diodes connected on each output line.

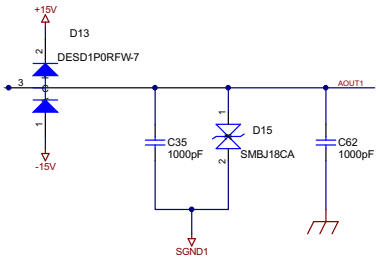


Figure 23. Analog Output EMC Protection

5 Software Description

For software description and code examples for TIDA-00310, please see TIDU577: Software Code Examples for TIDA-00310.

5.1 Analog Inputs

5.1.1 Range Select Register

The 4-analog input channels of ADS8684 can be configured to a given voltage range by configuring the range select register.

- Channel 0 range selector register address is 05h
- Channel 1 range selector register address is 06h
- Channel 2 range selector register address is 07hW
- Channel 3 range selector register address is 08h

Table 8. Channel *n* Input Range Registers

7	6	5	4	3	2	1	0
0	0	0	0	0	Range_CH*n*[2:0]		
R	R	R	R	R	R/W	R/W	R/W

Table 9. Channel *n* Input Range Registers Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7:3	0	R	0h	Must always be set to 0
2:0	Range_CH*n*[2:0]	R/W	0h	Input range selection bits for channel n (n = 0 to 3 for ADS8684) 000 = Input range is set to ±2.5 x V_{REF} 001 = Input range is set to ±1.25 x V_{REF} 010 = Input range is set to ±0.625 x V_{REF} 101 = Input range is set to 0 to 2.5 x V_{REF} 110 = Input range is set to 0 to 1.25 x V_{REF}

5.1.2 ADC Gain Control — Programmable Gain Amplifier

The devices offer a PGA at each individual analog input channel, which converts the original single-ended input signal into a fully-differential signal to drive the internal 16-bit ADC. The PGA also adjusts the common-mode level of the input signal before being fed into the ADC to ensure maximum usage of the ADC input dynamic range. Depending on the range of the input signal, the PGA gain can be accordingly adjusted by setting the Range_CHn[2:0] (n = 0 to 3) bits in the program register. The default or power-on state for the Range_CHn[2:0] bits is 000, which corresponds to an input signal range of ±2.5 × VREF. Table 10 lists the various configurations of the Range_CHn[2:0] bits for the different analog input voltage ranges. The PGA uses a very highly-matched network of resistors for multiple gain configurations. Matching between these resistors and the amplifiers across all channels is accurately trimmed to keep the overall gain error low across all channels and input ranges.

Table 10. PGA of ADS8684

ANALOG INPUT RANGE	Range_CH*n*[2:0]		
	BIT 2	BIT 1	BIT 0
±2.5 × V_{REF}	0	0	0
±1.25 × V_{REF}	0	0	1
±0.625 × V_{REF}	0	1	0
0 to 2.5 × V_{REF}	1	0	1
0 to 1.25 × V_{REF}	1	1	0

5.1.3 ADC Sampling —Auto Scan Sequencing Control Register

In AUTO_RST mode, the device automatically scans the preselected channels in ascending order with a new channel selected for every conversion. Each individual channel can be selectively included in the auto channel sequencing. For the channels that are not selected for auto sequencing, the AFE circuitry can be individually powered down.

Command Register Description

The command register is a 16-bit, write-only register that is used to set the operating modes of ADS8684. The settings in this register are used to select the channel sequencing mode (AUTO_RST or MAN_Ch_n), configure the device in standby (STDBY) or power-down (PWR_DN) mode, and reset (RST) the program registers to their default values. All command settings for this register are listed in Table 11. During power-up or reset, the default content of the command register is all 0s and the device waits for a command to be written before being placed into any mode of operation The device executes the command at the end of this particular data frame when the $\overline{CS}$ signal goes high.

Table 11. Command Register Description of ADS8684

REGISTER	MSB BYTE								LSB BYTE	COMMAND (Hex)	OPERATION IN NEXT FRAME
	B15	B14	B13	B12	B11	B10	B9	B8	B[7:0]		
Continued Operation (NO_OP)	0	0	0	0	0	0	0	0	0000 0000	0000h	Continue operation in previous mode
Standby (STDBY)	1	0	0	0	0	0	1	0	0000 0000	8200h	Device is placed into standby mode
Power Down (PWR_DN)	1	0	0	0	0	0	1	1	0000 0000	8300h	Device is powered down
Reset Program Registers (RST)	1	0	0	0	0	1	0	1	0000 0000	8500h	Program register is reset to default
Auto Ch. Sequence with Reset (AUTO_RST)	1	0	1	0	0	0	0	0	0000 0000	A000h	Auto mode enabled following a reset
Manual Ch 0 Selection (MAN_Ch_0)	1	1	0	0	0	0	0	0	0000 0000	C000h	Channel 0 input is selected
Manual Ch 1 Selection (MAN_Ch_1)	1	1	0	0	0	1	0	0	0000 0000	C400h	Channel 1 input is selected
Manual Ch 2 Selection (MAN_Ch_2)	1	1	0	0	1	0	0	0	0000 0000	C800h	Channel 2 input is selected
Manual Ch 3 Selection (MAN_Ch_3)	1	1	0	0	1	1	0	0	0000 0000	CC00h	Channel 3 input is selected
Manual AUX Selection (MAN_AUX)	1	1	1	0	0	0	0	0	0000 0000	E000h	AUX channel input is selected

5.1.4 Auto-Scan Sequence Enable Register (Address = 01h)

This register selects individual channels for sequencing in AUTO_RST mode. The default value for this register is FFh, which implies that in default condition all channels are included in the auto-scan sequence.

Table 12. Auto_SEQ_EN Register

7	6	5	4	3	2	1	0
CH7_EN	CH6_EN	CH5_EN	CH4_EN	CH3_EN	CH2_EN	CH1_EN	CH0_EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 13. Auto_SEQ_EN Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
3	CH3_EN	R/W	1h	Channel 3 enable. 0 = Channel 3 is not selected for sequencing in AUTO_RST mode 1 = Channel 3 is selected for sequencing in AUTO_RST mode
2	CH2_EN	R/W	1h	Channel 2 enable. 0 = Channel 2 is not selected for sequencing in AUTO_RST mode 1 = Channel 2 is selected for sequencing in AUTO_RST mode
1	CH1_EN	R/W	1h	Channel 1 enable. 0 = Channel 1 is not selected for sequencing in AUTO_RST mode 1 = Channel 1 is selected for sequencing in AUTO_RST mode
0	CH0_EN	R/W	1h	Channel 0 enable. 0 = Channel 0 is not selected for sequencing in AUTO_RST mode 1 = Channel 0 is selected for sequencing in AUTO_RST mode

5.1.5 ADC Transfer Function

The ADS8684 is a family of multichannel devices that supports single-ended, bipolar, and unipolar input ranges on all input channels. The output of the device is in a straight binary format for both bipolar and unipolar input ranges. The format for the output codes is the same across all analog channels.

The ideal transfer characteristic for each ADC channel for all input ranges is shown in Figure 24. The FSR for each input signal is equal to the difference between the positive full-scale (PFS) input voltage and the negative full-scale (NFS) input voltage. The LSB size is equal to
FSR / 2^{16} = FSR / 65536 because the resolution of the ADC is 16 bits. For a reference voltage of V_{REF} = 4.096 V, the LSB values corresponding to the different input ranges are listed in Table 14.

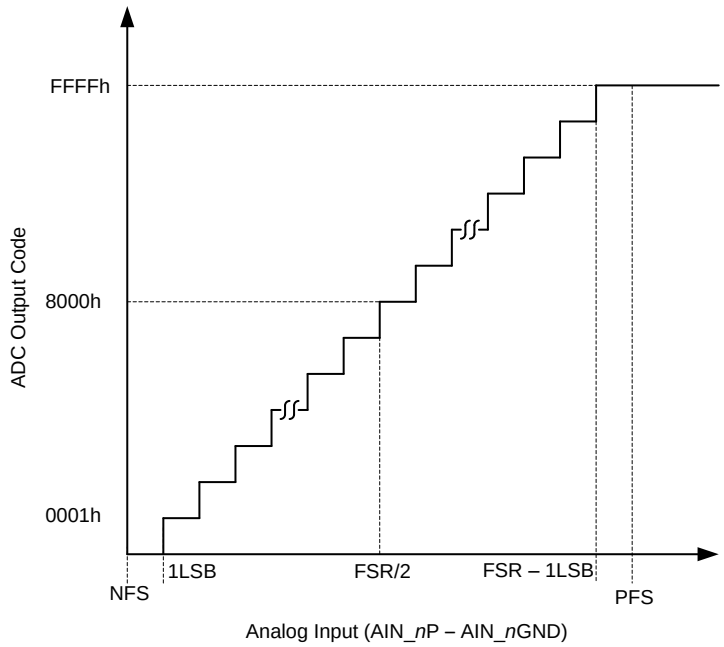


Figure 24. ADC Transfer Function

Table 14. ADC LSB Values for Different Input Ranges (V_{REF} = 4.096 V)

INPUT RANGE	POSITIVE FULL SCALE	NEGATIVE FULL SCALE	FULL-SCALE RANGE	LSB (µV)
±2.5 × V_{REF}	10.24 V	–10.24 V	20.48 V	312.50
±1.25 × V_{REF}	5.12 V	–5.12 V	10.24 V	156.25
±0.625 × V_{REF}	2.56 V	–2.56 V	5.12 V	78.125
0 to 2.5 × V_{REF}	10.24 V	0 V	10.24 V	156.25
0 to 1.25 × V_{REF}	5.12 V	0 V	5.12 V	78.125

5.1.6 SPI—ADC Data Acquisition

Data Acquisition Example

This section provides an example of how a host processor can use the device interface to configure the device internal register, as well as convert and acquire data for sampling a particular input channel. The timing diagram shown in Figure 25 provides further details.

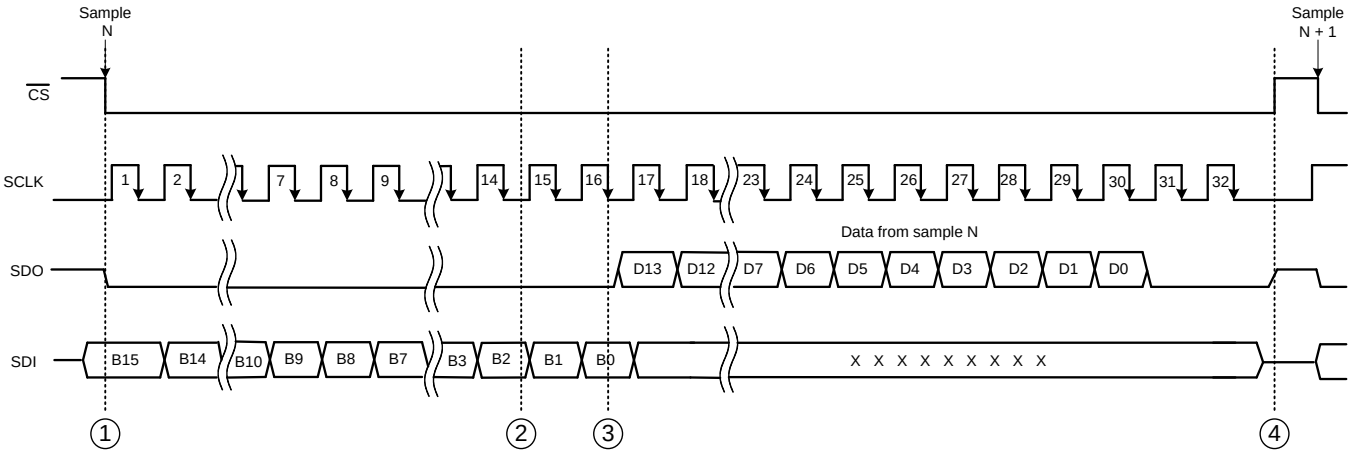


Figure 25. Device Operation Using the Serial Interface Timing Diagram of ADS8684

There are four events shown in Figure 25:

- **Event 1**: The host initiates a data conversion frame through a falling edge of the $\overline{CS}$ signal. The analog input signal at the instant of the $\overline{CS}$ falling edge is sampled by the ADC and conversion is performed using an internal oscillator clock. The analog input channel converted during this frame is selected in the previous data frame. The internal register settings of the device for the next conversion can be input during this data frame using the SDI and SCLK inputs. Initiate SCLK at this instant and latch data on the SDI line into the device on every SCLK falling edge for the next 16 SCLK cycles. At this instant, SDO goes low because the device does not output internal conversion data on the SDO line during the first 16 SCLK cycles.
- **Event 2**: During the first 16 SCLK cycles, the device completes the internal conversion process and data are now ready within the converter. However, the device does not output data bits on SDO until the 16th falling edge appears on the SCLK input. Because the ADC conversion time is fixed (the maximum value is given in the *Electrical Characteristics* table in Section 7.5 of the SBAS582 datasheet), the 16th SCLK falling edge must appear after the internal conversion is over, otherwise the data output from the device is incorrect. Therefore, the SCLK frequency cannot exceed a maximum value, as provided in the *Timing Requirements: Serial Interface* table in Section 7.6 of the SBAS582 datasheet.
- **Event 3**: At the 16th falling edge of the SCLK signal, the device reads the LSB of the input word on the SDI line. The device does not read anything from the SDO line for the remaining data frame. On the same edge, the MSB of the conversion data is output on the SDO line and can be read by the host processor on the subsequent falling edge of the SCLK signal. For 16 bits of output data, the LSB can be read on the 32nd SCLK falling edge. The SDO outputs 0 on subsequent SCLK falling edges until the next conversion is initiated.
- **Event 4**: When the internal data from the device is received, the host terminates the data frame by deactivating the $\overline{CS}$ signal to high. The SDO output goes into a Hi-Z state until the next data frame is initiated, as explained in Event 1.

5.2 Analog Output

The DAC8760 device has a number of 16-bit registers. These need to be configured, read, and written to achieve the desired functionality. A brief overview is described in Table 15. For details refer to the DAC8760 datasheet.

Table 15. Command and Register Map of DAC8760

REGISTER / COMMAND	READ/WRITE ACCESS	DATA BITS (DB15:DB0)														
		15	14	13	12	11	10:9	8	7	6	5	4	3	2	1	0
Control	R/W	CLRSEL	OVR	REXT	OUTEN	SRCLK			SRSTEP			SREN	DCEN	RANGE		
Configuration	R/W	X(1)					IOUT RANGE	DUAL OUTEN	APD	Reserved	CALEN	HARTEN	CRCEN	WDEN	WDPD	
DAC Data(2)	R/W	D15:D0														
No operation(3)	—	X														
Read Operation	—	X									READ ADDRESS					
Reset	W															RESET
Status	R	Reserved										CRC-FLT	WD-FLT	I-FLT	SR-ON	T-FLT
DAC Gain Calibration(2)	RW	G15:G0, unsigned														
DAC Zero Calibration(2)	RW	Z15:Z0, signed														
WATCHDOG TIMER(3)	—	X														

(1) X denotes *don't care* bits.
(2) DAC8760 (16-bit version) shown. DAC7760 (12-bit version) contents are located in DB15:DB4. For DAC7760, DB3:DB0 are *don't care* bits when writing and zeros when reading.
(3) *No operation*, *read operation*, and *watchdog timer* are commands and not registers.

1. Control and Configuration registers provide users with the option to select Output Type, Range (over range), and Slew rate. These registers also allow the user to set the following : Output, Watchdog, HART, Dual Output.
2. DAC Data register allows users to write the digital equivalent of the desired Analog Output.
3. Read, Status, and Watchdog Timer commands allow the user to monitor the DAC function.
4. Calibration registers allow the user to write the calibration values for Zero Error and Gain Error Correction.
5. Control and Configuration registers must be used to initialize each of the DACs at power up.
6. DAC Data register must be loaded with relevant values to generate the desired Analog Output.

5.2.1 Control Register

The DAC8760 control register is written to at address 0x55.

Table 16. Control Register of DAC8760

DATA BIT(S)	NAME	DEFAULT	DESCRIPTION
DB15	CLRSEL	0	VOUT clear value select bit. When bit = '0', VOUT is 0 V in *Section 4.2.1.4* mode or after reset. When bit = '1', VOUT is midscale in unipolar output and negative-full-scale in bipolar output in *Section 4.2.1.4* mode or after reset.
DB14	OVR	0	Setting the bit increases the voltage output range by 10%.
DB13	REXT	0	External current setting resistor enable.
DB12	OUTEN	0	Output enable. Bit = '1': Output is determined by RANGE bits. Bit = '0': Output is disabled. IOUT and VOUT are *Hi-Z*.
DB11:DB8	SRCLK[3:0]	0000	Slew rate clock control. Ignored when bit SREN = '0'
DB7:DB5	SRSTEP[2:0]	000	Slew rate step size control. Ignored when bit SREN = '0'

Table 16. Control Register of DAC8760 (continued)

DATA BIT(S)	NAME	DEFAULT	DESCRIPTION
DB4	SREN	0	Slew Rate Enable. Bit = '1': Slew rate control is enabled, and the ramp speed of the output change is determined by SRCLK and SRSTEP. Bit = '0': Slew rate control is disabled. Bits SRCLK and SRSTEP are ignored. The output changes to the new level immediately.
DB3	DCEN	0	Daisy-chain enable.
DB2:DB0	RANGE[2:0]	000	Output range bits.

5.2.2 Configuration Register

The DAC8760 configuration register is written to at address 0x57.

Table 17. : Configuration Register of DAC8760

DATA BIT(S)	NAME	DEFAULT	DESCRIPTION
DB15:DB11		0h	Reserved. User must not write any value other than zero to these bits.
DB10:DB9	IOUT RANGE	00	IOUT range. These bits are only used if both voltage and current outputs are simultaneously enabled via bit 8 (DUAL OUTEN). The voltage output range is still controlled by bits 2:0 of the Section 5.2.1 (RANGE bits). The current range is controlled by these bits and has similar behavior to RANGE[1:0] when RANGE[2] = '1'. However, unlike the RANGE bits, a change to this field does not make the DAC data register go to its default value.
DB8	DUAL OUTEN	0	DAC dual output enable. This bit controls if the voltage and current outputs are enabled simultaneously. Both are enabled when this bit is high. However, both outputs are controlled by the same DAC data register.
DB7	APD	0	Alternate power down. On power-up, +VSENSE is connected to the internal VOUT amplifier inverting terminal. Diodes exist at this node to REFIN and GND. Setting this bit connects this node to ground through a resistor. When set, the equivalent resistance seen from +VSENSE to GND is 70 kΩ. This is useful in applications where the VOUT and IOUT terminals are tied together.
DB6		0	Reserved. Do not write any value other than zero to these bits.
DB5	CALEN	0	User calibration enable. When user calibration is enabled, the DAC data are adjusted according to the contents of the gain and zero calibration registers.
DB4	HARTEN	0	Enable interface through HART-IN pin (only valid for IOUT set to 4-mA to 20-mA range via RANGE bits). Bit = '1': HART signal is connected through internal resistor and modulates output current. Bit = '0': HART interface is disabled.
DB3	CRCEN	0	Enable frame error checking.
DB2	WDEN	0	Watchdog timer enable.
DB1:DB0	WDPD[1:0]	00	Watchdog timeout period.

5.2.3 DAC Registers

The DAC registers consist of a DAC data register (Table 18), a DAC gain calibration register (Table 19), and a DAC zero calibration register (Table 20).

Table 18. DAC Data Register

DATA BITS	NAME	DEFAULT	DESCRIPTION
DB15:DB0	D15:D0	0000h	DAC data register. Format is unsigned straight binary.

Table 19. DAC Gain Calibration Register

DATA BITS	NAME	DEFAULT	DESCRIPTION
DB15:DB0	G15:G0	0000h	Voltage and current gain calibration register for user calibration. Format is unsigned straight binary.

Table 20. DAC Zero Calibration Register

DATA BITS	NAME	DEFAULT	DESCRIPTION
DB15:DB0	Z15:Z0	0000h	Voltage and current zero calibration register for user calibration. Format is twos complement.

5.2.4 Setting Voltage and Current Output Ranges

For voltage and current outputs in normal mode (VOUT and IOUT are not simultaneously enabled), the output range is set according to Table 21.

Table 21. Setting Voltage And Current Output Ranges of DAC8760

RANGE	OUTPUT RANGE
000	0 V to 5 V
001	0 V to 10 V
010	±5 V
011	±10 V
100	Not allowed(1)
101	4 mA to 20 mA
110	0 mA to 20 mA
111	0 mA to 24 mA

(1) RANGE bits cannot be programmed to 0x100. Previous value is held when this command is written.

Note that changing the RANGE bits at any time causes the DAC data register to be cleared based on the value of CLR-SEL (pin or register bit) and the new value of the RANGE bits.

In addition to the RANGE bits, the OVR bit extends the voltage output range by 10%. If the OVR bit is set, the voltage output range follows as shown in Table 22, as long as there is headroom with the supply.

Table 22. Voltage Output Overrange of DAC8760

VOLTAGE OUTPUT RANGE	VOLTAGE OUTPUT OVERRANGE
0 V to 5 V	0 V to 5.5 V
0 V to 10 V	0 V to 11 V
±5 V	±5.5 V
±10 V	±11 V

5.2.5 DAC Configuration Examples

To set the voltage output range of 0 to 10 V and SSI as daisy-chained, perform the following steps:

1. Set the slew rate and enable output.
2. Provide no overrange.
3. Set the control register as shown in Table 23.
4. Write the configuration registers for:
   - No dual output
   - No HART
   - 10 ms for the watchdog timer
   - No APD
   - No calibration

Table 23. Example 1: DAC Configured as Voltage Output of 0 to 10 V

REGISTER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CONTROL	0	0	1	1	0	0	0	0	0	0	0	0	1	0	0	1
CONFIGURATION	X	X	X	X	X	0	0	0	0	0	0	0	0	0	0	0

To set the current output range of 0 to 24 mA and SSI as daisy-chained, perform the following steps:

1. Set the slew rate and enable output.
2. Provide no overrange.
3. Set the control register as shown in Table 24.
4. Write the configuration registers for
   - No dual output
   - No HART
   - 51 ms for the watchdog timer
   - No APD
   - No calibration

Table 24. Example 2: DAC Configured as Voltage Output of 0 to 24 mA

REGISTER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CONTROL	0	0	1	1	0	0	0	0	0	0	0	0	1	1	1	1
CONFIGURATION	X	X	X	X	X	0	0	0	0	0	0	0	0	0	0	1

5.3 Relay Drive Outputs

5.3.1 I2C Interface

The bidirectional I2C bus consists of the serial clock (SCL) and serial data (SDA) lines. Both lines must be connected to a positive supply through a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

I2C communication with this device is initiated by a master sending a Start condition, a high-to-low transition on the SDA input and output, while the SCL input is high. After the Start condition, the device address byte is sent, most significant bit (MSB) first, including the data direction bit (R/W).

After receiving the valid address byte, this device responds with an acknowledge (ACK), a low on the SDA input and output during the high of the ACK-related clock pulse. The address (ADDR) input of the slave device must not be changed between the Start and the Stop conditions.

On the I2C bus, only one data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high pulse of the clock period, as changes in the data line at this time are interpreted as control commands (Start or Stop).

A Stop condition, a low-to-high transition on the SDA input/\ and output while the SCL input is high, is sent by the master.

Any number of data bytes can be transferred from the transmitter to receiver between the Start and the Stop conditions. Each byte of eight bits is followed by one ACK bit. The transmitter must release the SDA line before the receiver can send an ACK bit. The device that acknowledges must pull down the SDA line during the AC clock pulse, so that the SDA line is stable low during the high pulse of the ACK-related clock period. When a slave receiver is addressed, it must generate an ACK after each byte is received. Similarly, the master must generate an ACK after each byte that it receives from the slave transmitter. Setup and hold times must be met to ensure proper operation.

A master receiver signals an end of data to the slave transmitter by not generating an acknowledge (NACK) after the last byte has been clocked out of the slave. This is done by the master receiver by holding the SDA line high. In this event, the transmitter must release the data line to enable the master to generate a Stop condition.

Table 25. Interface Definition

BYTE	BIT							
	7 (MSB)	6	5	4	3	2	1	0 (LSB)
I2C slave address	L	H	L	L	L	L	ADDR	R/$\overline{W}$
I/O data bus	P7	P6	P5	P4	P3	P2	P1	P0

5.3.2 Device Address

The address of the TCA6408A is shown in Figure 26

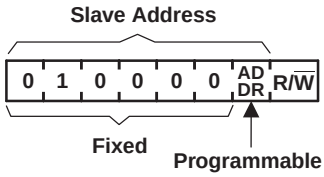


Figure 26. TCA6408A Address

Table 26. Address Reference

ADDRESS	I2C BUS SLAVE ADDRESS
L	32 (decimal), 20 (hexadecimal)
H	33 (decimal), 21 (hexadecimal)

The last bit of the slave address defines the operation (read or write) to be performed. A high (1) selects a read operation, while a low (0) selects a write operation.

5.3.3 Control Register and Command Byte

Following the successful acknowledgment of the address byte, the bus master sends a command byte, which is stored in the Control Register in the TCA6408A. Two bits of this data byte state the operation (read or write) and the internal registers (Input, Output, Polarity Inversion, or Configuration) that will be affected. This register can be written or read through the I2C bus. The command byte is sent only during a write transmission.

B7	B6	B5	B4	B3	B2	B1	B0

Table 27. Control Register Bits and Command Byte

CONTROL REGISTER BITS								COMMAND BYTE (HEX)	REGISTER	PROTOCOL	POWER-UP DEFAULT
B7	B6	B5	B4	B3	B2	B1	B0				
0	0	0	0	0	0	0	0	00	Input port	Read byte	xxxx xxxx
0	0	0	0	0	0	0	1	01	Output port	Read/write byte	1111 1111
0	0	0	0	0	0	1	0	02	Polarity inversion	Read/write byte	0000 0000
0	0	0	0	0	0	1	1	03	Configuration	Read/write byte	1111 1111

5.3.4 Register Description

The Input Port Register (register 0) reflects the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by the Configuration Register. The registers act only on read operation. Writes to this register have no effect. The default value (X) is determined by the externally applied logic level. Before a read operation, a write transmission is sent with the command byte to indicate to the I2C device that the Input Port Register is to be accessed next.

Table 28. Register 0 (Input Port Register)

BIT	I-7	I-6	I-5	I-4	I-3	I-2	I-1	I-0
DEFAULT	X	X	X	X	X	X	X	X

The Output Port Register (Table 29) shows the outgoing logic levels of the pins defined as outputs by the Configuration Register. Bit values in this register have no effect on pins defined as inputs. In turn, reads from this register reflect the value that is in the flip-flop controlling the output selection, not the actual pin value.

Table 29. Register 1 (Output Port Register)

BIT	O-7	O-6	O-5	O-4	O-3	O-2	O-1	O-0
DEFAULT	1	1	1	1	1	1	1	1

The Polarity Inversion Register (Table 30) allows polarity inversion of pins defined as inputs by the Configuration Register. If a bit in this register is set (written with 1), the polarity of the corresponding port pin is inverted. If a bit in this register is cleared (written with a 0), the polarity of the corresponding port pin is retained.

Table 30. Register 2 (Polarity Inversion Register)

BIT	N-7	N-6	N-5	N-4	N-3	N-2	N-1	N-0
DEFAULT	0	0	0	0	0	0	0	0

The Configuration Register (Table 31) configures the direction of the I/O pins. If a bit in this register is set to 1, the corresponding port pin is enabled as an input with a high-impedance output driver. If a bit in this register is cleared to 0, the corresponding port pin is enabled as an output.

Table 31. Register 3 (Configuration Register)

BIT	C-7	C-6	C-5	C-4	C-3	C-2	C-1	C-0
DEFAULT	1	1	1	1	1	1	1	1

5.3.5 Bus Transactions

Data is exchanged between the master and TCA6408A through write and read commands.

5.3.5.1 Write Operation

Data is transmitted to the TCA6408A by sending the device address and setting the least significant bit (LSB) to a logic 0 .The command byte is sent after the address and determines which register receives the data that follows the command byte. There is no limitation on the number of data bytes sent in one write transmission.

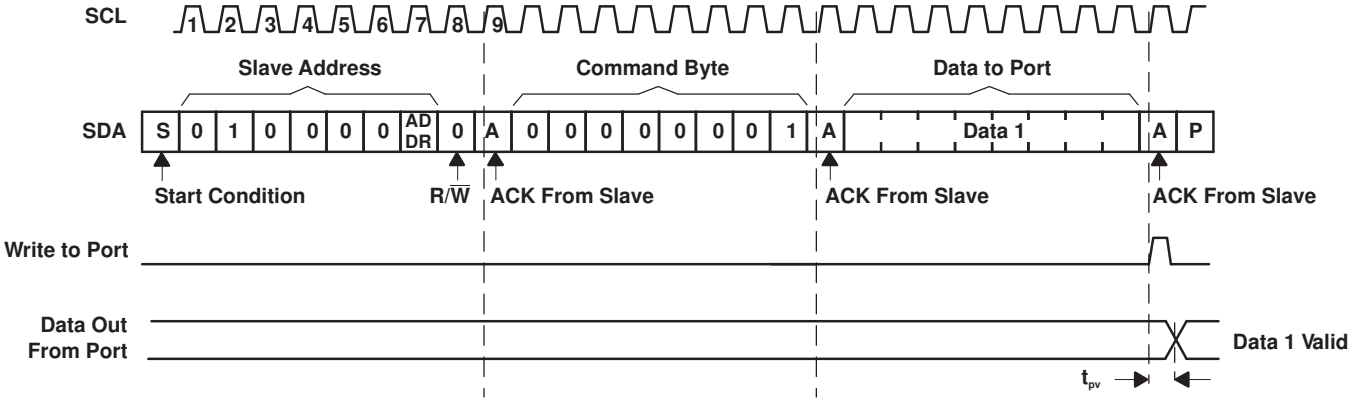


Figure 27. Write to Output Port Register

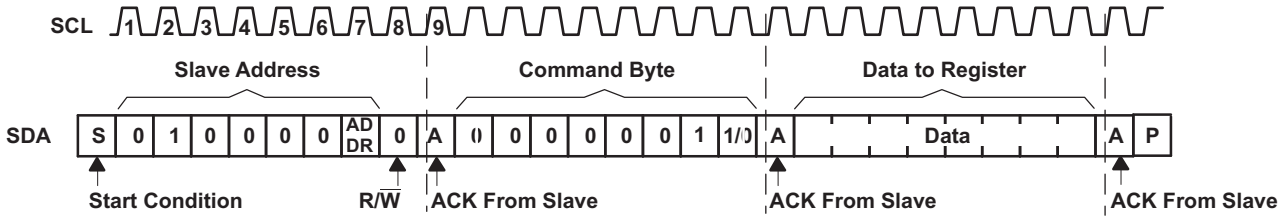


Figure 28. Write to Configuration or Polarity Inversion Registers

5.3.5.2 Read Operation

The bus master must first send the TCA6408A address with the LSB set to a logic 0. The command byte is sent after the address and determines which register is accessed.

After a restart, the device address is sent again, but now with the LSB set to a logic 1. Data from the register defined by the command byte is then sent by the TCA6408A.

Data is clocked into the register on the rising edge of the ACK clock pulse.

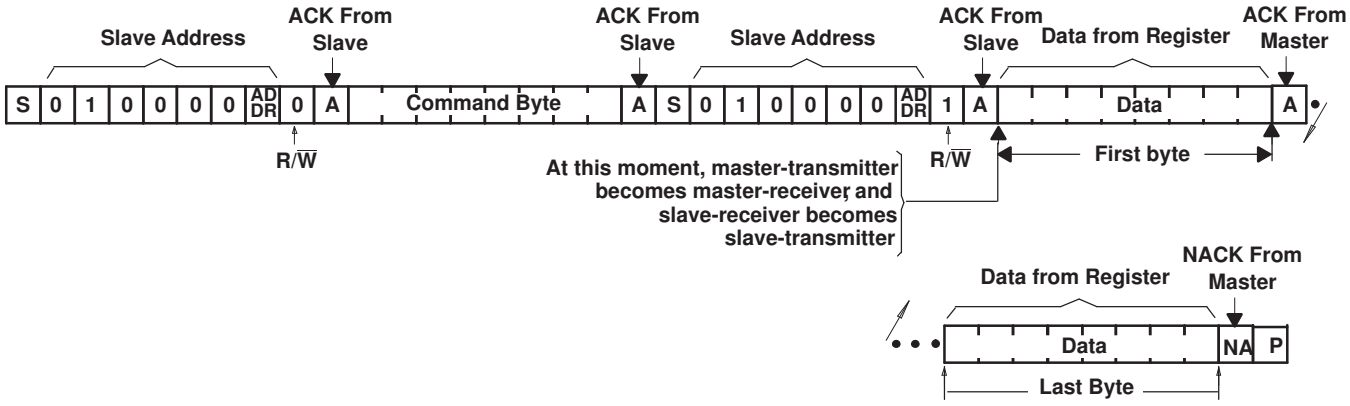


Figure 29. Read From Register

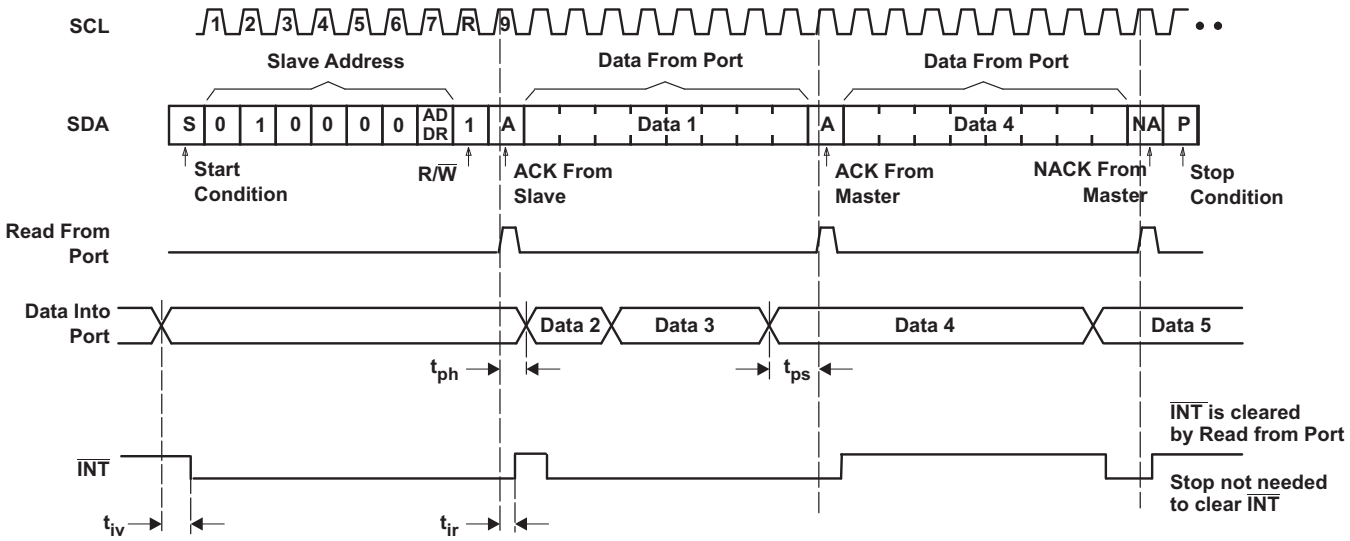


Figure 30. Read From Input Port Register

5.4 Front Panel

The test module uses a USB interface to communicate between the PC and the analog I/O board. The test module uses a command and response based interface to set and receive data from the ADC and DAC. Figure 31 shows a screen capture of the graphic user interface (GUI).

There are individual panes for each channel of the ADC and DAC as shown in the image.

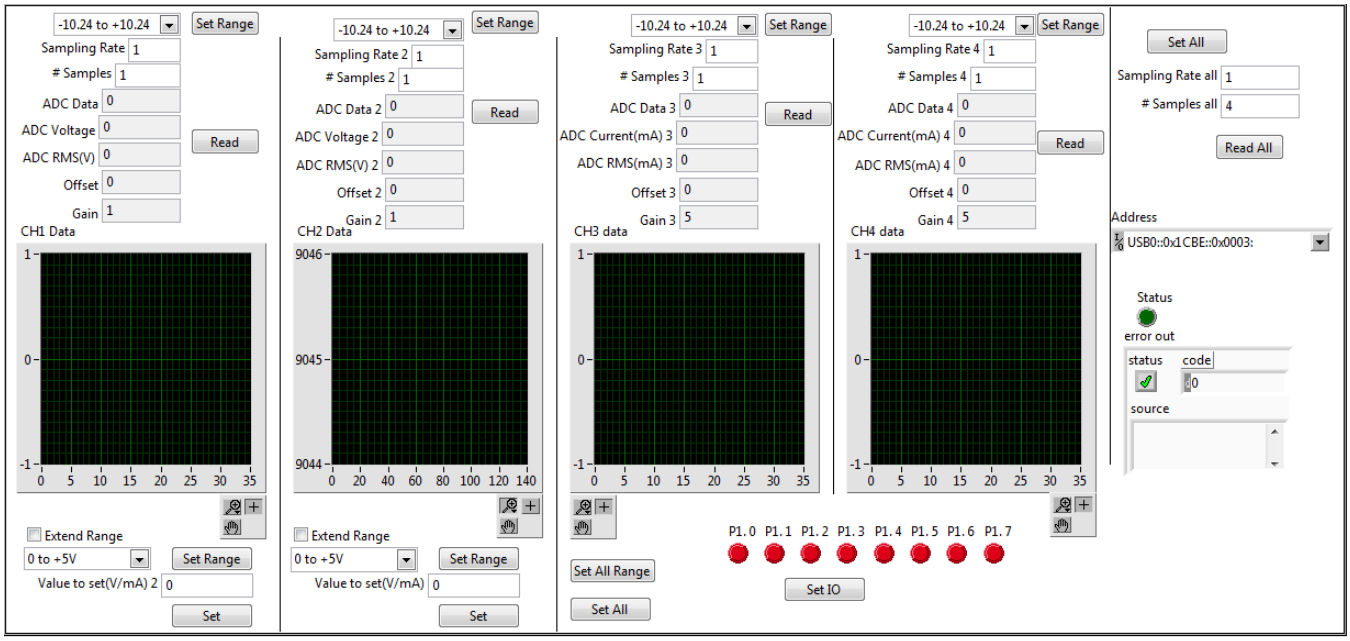


Figure 31. Graphical User Interface

5.4.1 ADC Configuration

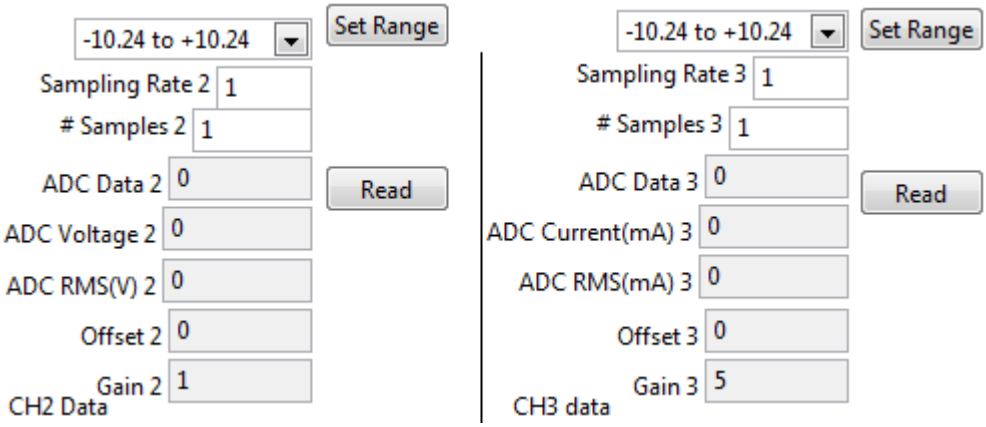


Figure 32. ADC Configuration

Steps to capture the data:

1. Select the range of input and press “Set Range.”
2. Set the sampling rate and number of samples.
3. Click on the read button.

5.4.2 DAC Configuration

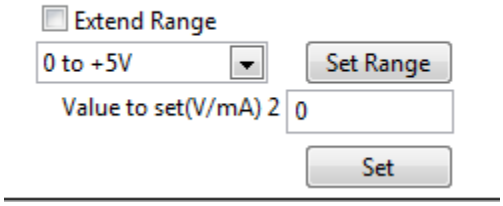


Figure 33. DAC Configuration

Steps to set the DAC values:

1. Select the range and click “Set Range.”
2. Select the value to be set in DAC and press “Set Button.”

5.4.3 Relay Drive Output

Steps to set the I/O port:

1. Select the input state by clicking the icons.
2. Click on “Set IO” to set the current value of the I/O port.

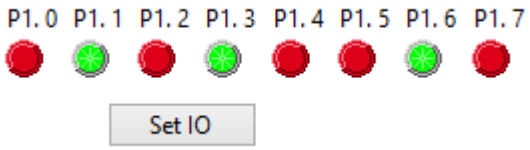


Figure 34. Relay Drive Output Control

6 Test Setup

6.1 Connection Setup Between TIVA Launch Pad and TI Design Board

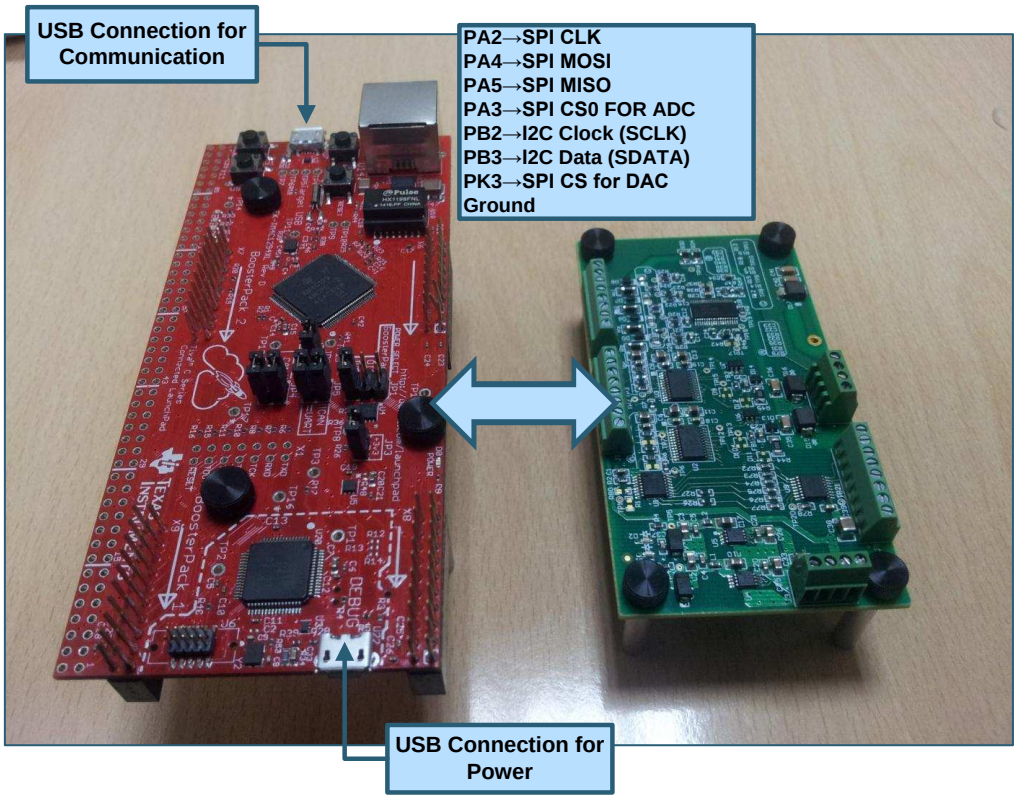


Figure 35. Connection With Host Controller

6.2 Connector Details

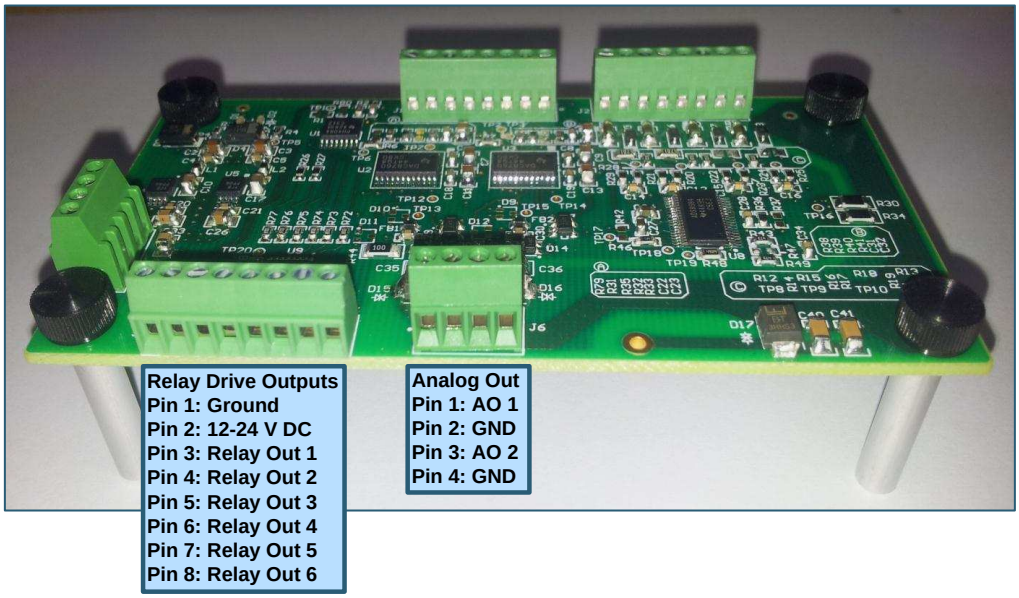


Figure 36. Connector Details Relay Drive Outputs and Analog Outputs

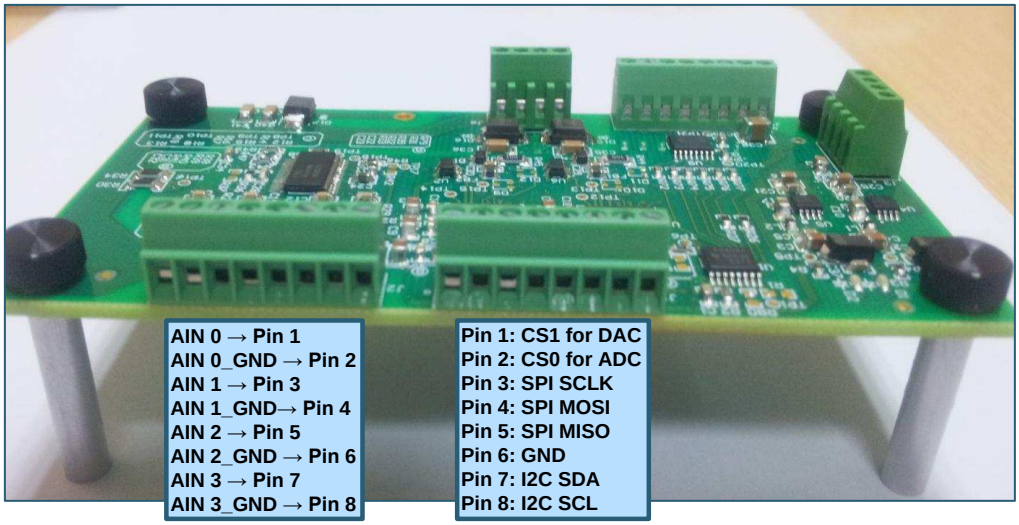


Figure 37. Connector Details Analog Input and Interface Connector

6.3 Instrumentation Used

- HP Digital Multimeter 34401A
- KEITHLEY™ model 2450 SourceMeter®
- HP E3631A DC Power Supply

7 Test Results

7.1 Test Results: Analog Input

Table 32. Analog Input: Voltage Input[1]

ANALOG INPUT CHANNEL			AIN0	AIN1	AIN2	AIN3	ADC RANGE	AIN0	AIN1	AIN2	AIN3
SET INPUT	UNIT	ACTUAL INPUT	VOLTAGE ON GUI, V					% FS ERROR	% FS ERROR	% FS ERROR	% FS ERROR
5	mV	5.00794	0.00510	0.00553	0.00553	0.00582	0-5.12 V	0.00	–0.01	–0.01	–0.02
10		10.01148	0.01012	0.01052	0.01050	0.01082		0.00	–0.01	–0.01	–0.02
15		15.00876	0.01511	0.01550	0.01549	0.01581		0.00	–0.01	–0.01	–0.02
20		20.03415	0.02013	0.02053	0.02050	0.02083		0.00	–0.01	–0.01	–0.02
25		25.02971	0.02510	0.02554	0.02549	0.02583		0.00	–0.01	–0.01	–0.02
50		50.03321	0.05008	0.05049	0.05048	0.05083		0.00	–0.01	–0.01	–0.02
75		75.02685	0.07506	0.07544	0.07549	0.07579		0.00	–0.01	–0.01	–0.01
100		100.0212	0.10001	0.10041	0.10045	0.10078		0.00	–0.01	–0.01	–0.01
150		150.0229	0.14998	0.15032	0.15045	0.15068		0.00	–0.01	–0.01	–0.01
200		200.0315	0.19991	0.20030	0.20042	0.20065		0.00	–0.01	–0.01	–0.01
225		225.0209	0.22492	0.22525	0.22539	0.22559		0.00	0.00	–0.01	–0.01
250		250.0413	0.24989	0.25026	0.25037	0.25060		0.00	0.00	–0.01	–0.01
275		275.0297	0.27486	0.27524	0.27534	0.27555		0.00	0.00	–0.01	–0.01
300		300.0136	0.29984	0.30018	0.30029	0.30053		0.00	0.00	–0.01	–0.01
325		325.0436	0.32481	0.32521	0.32533	0.32551		0.00	0.00	–0.01	–0.01
350		350.0302	0.34975	0.35018	0.35029	0.35049		0.01	0.00	–0.01	–0.01
375		375.0214	0.37476	0.37513	0.37524	0.37548		0.01	0.00	0.00	–0.01
400		400.034	0.39974	0.40010	0.40025	0.40046		0.01	0.00	0.00	–0.01
425		425.0294	0.42467	0.42509	0.42519	0.42545		0.01	0.00	0.00	–0.01
450		450.0156	0.44964	0.45004	0.45015	0.45039		0.01	0.00	0.00	–0.01
475		475.046	0.47462	0.47506	0.47516	0.47542		0.01	0.00	0.00	–0.01
500		500.034	0.49961	0.50000	0.50014	0.50038		0.01	0.00	0.00	–0.01
600		600.022	0.59942	0.59991	0.60009	0.60023		0.01	0.00	0.00	0.00
700		700.0459	0.69931	0.69982	0.70005	0.70020		0.01	0.00	0.00	0.00
800		800.0333	0.79920	0.79974	0.79994	0.80006		0.02	0.01	0.00	0.00
900		900.0242	0.89909	0.89963	0.89983	0.89996		0.02	0.01	0.00	0.00
1	V	1.000007	0.99900	0.99947	0.99977	0.99983		0.02	0.01	0.00	0.00
1.5		1.5	1.49838	1.49896	1.49939	1.49932		0.03	0.02	0.01	0.01
2		1.999971	1.99771	1.99839	1.99898	1.99882		0.04	0.03	0.02	0.02
2.5		2.499757	2.49694	2.49772	2.49841	2.49812		0.06	0.04	0.03	0.03
3		3.000016	2.99658	2.99744	2.99831	2.99784		0.07	0.05	0.03	0.04
3.5		3.499905	3.49590	3.49682	3.49779	3.49726		0.08	0.06	0.04	0.05
4		3.999725	3.99512	3.99609	3.99721	3.99661		0.09	0.07	0.05	0.06
4.5		4.499575	4.49434	4.49549	4.49673	4.49597		0.10	0.08	0.06	0.07
5		4.999488	4.99558	4.99484	4.99616	4.99555	0-10.24 V	0.04	0.05	0.03	0.04
5.5		5.500035	5.49582	5.49479	5.49610	5.49566		0.04	0.05	0.04	0.04
6		5.999979	5.99524	5.99424	5.99595	5.99513		0.05	0.06	0.04	0.05
6.5		6.499888	6.49505	6.49358	6.49531	6.49451		0.05	0.06	0.04	0.05
7		6.999719	6.99434	6.99311	6.99467	6.99401		0.05	0.06	0.05	0.06
7.5		7.499618	7.49398	7.49219	7.49447	7.49447		0.06	0.07	0.05	0.05

[1] All channels are configured as voltage inputs (200-R burden at AIN2 and AIN3 removed).

Table 32. Analog Input: Voltage Input[1] (continued)

8	V	7.999891	7.99380	7.99210	7.99421	7.99318	0-10.24 V	0.06	0.08	0.06	0.07
8.5		8.499819	8.49334	8.49134	8.49375	8.49283		0.06	0.08	0.06	0.07
9		8.999725	8.99292	8.99098	8.99320	8.99222		0.07	0.09	0.06	0.07
9.5		9.499628	9.49242	9.49024	9.49280	9.49169		0.07	0.09	0.07	0.08
10		9.999924	9.99235	9.99003	9.99269	9.99155		0.07	0.10	0.07	0.08
10.23		10.22976	10.22210	10.21950	10.22250	10.22110		0.07	0.10	0.07	0.08

Table 33. Analog Input: Current Input[1]

SOURCE CURRENT	MEASURED CURRENT		BURDEN. OHMS	VOLTAGE INPUT AT ADC, V	AIN2, V	AIN3, V	AIN RANGE	FSV, V	% FS ERROR AIN2	% FS ERROR AIN3
100	99.62326		200	0.02000	0.02029	0.02085		5.12	–0.006	–0.017
200	199.6684		200	0.04000	0.04025	0.04081		5.12	–0.005	–0.016
300	299.6829		200	0.06000	0.06023	0.06079		5.12	–0.005	–0.015
400	399.7036		200	0.08000	0.08022	0.08075		5.12	–0.004	–0.015
500	499.7151		200	0.10000	0.10021	0.10075		5.12	–0.004	–0.015
600	599.7146	µA	200	0.12000	0.12014	0.12074		5.12	–0.003	–0.014
700	699.7421		200	0.14000	0.14008	0.14072		5.12	–0.002	–0.014
800	799.7833		200	0.16000	0.16007	0.16072		5.12	–0.001	–0.014
900	899.7575		200	0.18000	0.18008	0.18071		5.12	–0.002	–0.014
1000	999.7475		200	0.20000	0.20003	0.20063		5.12	0.000	–0.012
1.25	1.24985		200	0.25000	0.24999	0.25063		5.12	0.000	–0.012
1.5	1.499985		200	0.30000	0.30004	0.30055		5.12	–0.001	–0.011
1.75	1.7499		200	0.35000	0.34999	0.35052		5.12	0.000	–0.010
2.0	2.000002		200	0.40000	0.40000	0.40050		5.12	0.000	–0.010
2.25	2.25001		200	0.45000	0.44989	0.45056		5.12	0.002	–0.011
2.5	2.500001		200	0.50000	0.49985	0.50051	0-5.12 V	5.12	0.003	–0.010
2.75	2.75011		200	0.55000	0.54977	0.55051		5.12	0.004	–0.010
3.0	3.00016		200	0.60000	0.59973	0.60053		5.12	0.005	–0.010
3.25	3.2503		200	0.65000	0.64969	0.65045		5.12	0.006	–0.009
3.5	3.50023	mA	200	0.70000	0.69966	0.70043		5.12	0.007	–0.008
3.75	3.75024		200	0.75000	0.74963	0.75041		5.12	0.007	–0.008
4.0	4.00033		200	0.80000	0.79956	0.80039		5.12	0.009	–0.008
4.25	4.25035		200	0.85000	0.84946	0.85029		5.12	0.011	–0.006
4.5	4.50052		200	0.90000	0.89949	0.90029		5.12	0.010	–0.006
4.75	4.75047		200	0.95000	0.94941	0.95021		5.12	0.012	–0.004
5.0	5.00047		200	1.00000	0.99942	1.00015		5.12	0.011	–0.003
5.25	5.25054		200	1.05000	1.04939	1.05010		5.12	0.012	–0.002
5.5	5.50006		200	1.10000	1.09935	1.10002		5.12	0.013	0.000
5.75	5.75043		200	1.15000	1.14929	1.14999		5.12	0.014	0.000
6.0	6.00065		200	1.20000	1.19921	1.19995		5.12	0.015	0.001
6.25	6.2507		200	1.25000	1.24916	1.24997		5.12	0.016	0.001
6.5	6.50078		200	1.30000	1.29916	1.29986		5.12	0.016	0.003
6.75	6.75082		200	1.35000	1.34908	1.34991		5.12	0.018	0.002
7.00	7.00076		200	1.40000	1.39901	1.39988		5.12	0.019	0.002
7.25	7.25091		200	1.45000	1.44900	1.44989		5.12	0.020	0.002
7.5	7.50106		200	1.50000	1.49901	1.49992		5.12	0.019	0.002

[1] AIN 3 and AIN 4 are configured as current input.

Table 33. Analog Input: Current Input[1] (continued)

7.75	7.75107		200	1.55000	1.54894	1.54985		5.12	0.021	0.003
8.0	8.00115		200	1.60000	1.59894	1.59989		5.12	0.021	0.002
8.25	8.25102		200	1.65000	1.64880	1.64980		5.12	0.023	0.004
8.5	8.50108		200	1.70000	1.69874	1.69976		5.12	0.025	0.005
8.75	8.75127		200	1.75000	1.74878	1.74969		5.12	0.024	0.006
9.0	9.00127		200	1.80000	1.79873	1.79964		5.12	0.025	0.007
9.25	9.25123		200	1.85000	1.84871	1.84960	0-5.12 V	5.12	0.025	0.008
9.5	9.50129		200	1.90000	1.89868	1.89950		5.12	0.026	0.010
9.75	9.75144		200	1.95000	1.94863	1.94952		5.12	0.027	0.009
10.0	10.00152		200	2.00000	1.99864	1.99951		5.12	0.027	0.010
10.50	10.50105		200	2.10000	2.09837	2.09937		5.12	0.032	0.012
11.0	11.00111		200	2.20000	2.19833	2.19929		5.12	0.033	0.014
11.5	11.50116		200	2.30000	2.29818	2.29932		5.12	0.036	0.013
12.0	12.0005		200	2.40000	2.39816	2.39928		5.12	0.036	0.014
12.5	12.5007		200	2.50000	2.49812	2.49921		5.12	0.037	0.015
13.0	12.999		200	2.60000	2.59774	2.59864		5.12	0.044	0.027
13.5	13.4994		200	2.70000	2.69771	2.69863		5.12	0.045	0.027
14.0	13.9995		200	2.80000	2.79762	2.79856		5.12	0.046	0.028
14.5	14.4995		200	2.90000	2.89754	2.89855		5.12	0.048	0.028
15.0	14.9994		200	3.00000	2.99756	2.99856		5.12	0.048	0.028
15.5	15.4998	mA	200	3.10000	3.09762	3.09858		5.12	0.046	0.028
16	16.0001		200	3.20000	3.19885	3.19894		10.24	0.011	0.010
16.5	16.5004		200	3.30000	3.29892	3.29886		10.24	0.011	0.011
17	17.0008		200	3.40000	3.39886	3.39879		10.24	0.011	0.012
17.5	17.5005		200	3.50000	3.49894	3.49861		10.24	0.010	0.014
18.0	18.0007		200	3.60000	3.59882	3.59864		10.24	0.012	0.013
18.5	18.5008		200	3.70000	3.69880	3.69857		10.24	0.012	0.014
19.0	19.01		200	3.80000	3.79869	3.79868		10.24	0.013	0.013
19.5	19.5014		200	3.90000	3.89859	3.89843		10.24	0.014	0.015
20.0	19.9995		200	4.00000	3.99803	3.99844		10.24	0.019	0.015
20.25	20.2502		200	4.05000	4.04808	4.04839		10.24	0.019	0.016
20.5	20.4994		200	4.10000	4.09801	4.09812		10.24	0.019	0.018
20.75	20.7506		200	4.15000	4.14806	4.14849		10.24	0.019	0.015
21.0	20.9995		200	4.20000	4.19788	4.19811	0-10.24 V	10.24	0.021	0.018
21.25	21.2508		200	4.25000	4.24796	4.24842		10.24	0.020	0.015
21.50	21.4999		200	4.30000	4.29789	4.29798		10.24	0.021	0.020
21.75	21.7508		200	4.35000	4.34791	4.34826		10.24	0.020	0.017
22	21.999		200	4.40000	4.39786	4.39796		10.24	0.021	0.020
22.50	22.2509		200	4.45000	4.44794	4.44803		10.24	0.020	0.019
22.5	22.5002		200	4.50000	4.49762	4.49786		10.24	0.023	0.021
22.75	22.7508		200	4.55000	4.54791	4.54796		10.24	0.020	0.020
23.0	23.0005		200	4.60000	4.59764	4.59769		10.24	0.023	0.023
23.25	23.2495		200	4.65000	4.64747	4.64738		10.24	0.025	0.026
23.5	23.5		200	4.70000	4.69766	4.69767		10.24	0.023	0.023
23.75	23.7501		200	4.75000	4.74764	4.74741		10.24	0.023	0.025
24.00	24.0004		200	4.80000	4.79766	4.79766		10.24	0.023	0.023

7.2 Test Results: Analog Output

7.2.1 Analog Output, AO1, and AO2 Configured as Current Output 0-20 mA

SET OUTPUT CURRENT, mA	FSV, mA	CURRENT MEASUREMENT VALUE			AO1 DAC1 % FULL SCALE ERROR	AO2 DAC2 % FULL SCALE ERROR
		AO1 DAC1 MEASURED	AO2 DAC2 MEASURED	UNIT		
0.1	20	101.1546	100.1286		–0.01	0.00
0.125	20	126.6541	125.4644		–0.01	0.00
0.15	20	151.4425	150.2087		–0.01	0.00
0.175	20	175.9686	174.7462		0.00	0.00
0.2	20	201.2354	200.1133		–0.01	0.00
0.225	20	226.1972	224.9388		–0.01	0.00
0.25	20	251.0675	249.7024		–0.01	0.00
0.275	20	276.1555	275.0766		–0.01	0.00
0.3	20	301.3071	299.9955		–0.01	0.00
0.325	20	326.1047	324.6818		–0.01	0.00
0.35	20	351.2101	349.9976		–0.01	0.00
0.375	20	376.4913	375.1062		–0.01	0.00
0.4	20	401.1415	399.7092		–0.01	0.00
0.425	20	426.1755	424.9613	µA	–0.01	0.00
0.45	20	451.7797	450.1715		–0.01	0.00
0.475	20	475.9122	474.3765		0.00	0.00
0.5	20	500.8371	499.6487		0.00	0.00
0.55	20	551.0857	549.4429		–0.01	0.00
0.6	20	601.6115	599.9602		–0.01	0.00
0.65	20	650.9167	649.5129		0.00	0.00
0.7	20	701.3452	699.5341		–0.01	0.00
0.75	20	751.6795	749.8812		–0.01	0.00
0.8	20	801.0213	799.1851		–0.01	0.00
0.85	20	851.3024	849.4277		–0.01	0.00
0.9	20	901.3037	899.5898		–0.01	0.00
0.95	20	951.231	949.2567		–0.01	0.00
1	20	1.001701	0.9996745		–0.01	0.00
1.25	20	1.251726	1.249214		–0.01	0.00
1.5	20	1.501522	1.499354		–0.01	0.00
1.75	20	1.751159	1.749765		–0.01	0.00
2	20	2.001716	2.00569		–0.01	–0.03
2.25	20	2.251422	2.250719		–0.01	0.00
2.5	20	2.501041	2.500703	mA	–0.01	0.00
2.75	20	2.75072	2.750807		0.00	0.00
3	20	3.00355	3.001236		–0.02	–0.01
3.25	20	3.250846	3.251739		0.00	–0.01
3.5	20	3.501161	3.502262		–0.01	–0.01
3.75	20	3.751183	3.752343		–0.01	–0.01
4	20	4.00975	4.002047		–0.05	–0.01
4.25	20	4.25064	4.25196		0.00	–0.01
4.5	20	4.501012	4.501899		–0.01	–0.01
4.75	20	4.751028	4.751925		–0.01	–0.01
5	20	5.00075	5.00138		0.00	–0.01

5.5	20	5.50022	5.50085		0.00	0.00
6	20	6.00058	6.00051		0.00	0.00
6.5	20	6.50075	6.50053		0.00	0.00
7	20	7.00073	7.00163		0.00	–0.01
7.5	20	7.50052	7.50225		0.00	–0.01
8	20	7.99983	8.003		0.00	–0.02
8.5	20	8.50021	8.50402		0.00	–0.02
9	20	9.00045	9.00421		0.00	–0.02
9.5	20	9.50058	9.50392		0.00	–0.02
10	20	10.00045	10.00227		0.00	–0.01
10.5	20	10.49991	10.50287	mA	0.00	–0.01
11	20	11.00019	11.00258		0.00	–0.01
11.5	20	11.5002	11.50258		0.00	–0.01
12	20	11.9996	12.0026		0.00	–0.01
12.5	20	12.499	12.5027		0.00	–0.01
13	20	12.9984	13.0036		0.01	–0.02
13.5	20	13.4985	13.5045		0.01	–0.02
14	20	13.9984	14.0041		0.01	–0.02
14.5	20	14.4988	14.5044		0.01	–0.02
15	20	14.9984	15.0036		0.01	–0.02
15.5	20	15.498	15.5034		0.01	–0.02
16	20	15.9982	16.003		0.01	–0.02
16.25	20	16.2483	16.2526		0.01	–0.01
16.5	20	16.4982	16.5029		0.01	–0.01
16.75	20	16.7482	16.7537		0.01	–0.02
17	20	16.9987	17.009		0.01	–0.05
17.25	20	17.2485	17.2546		0.01	–0.02
17.5	20	17.4985	17.5048		0.01	–0.02
17.75	20	17.7479	17.755		0.01	–0.02
18	20	17.998	18.0058		0.01	–0.03
18.25	20	18.2482	18.2561		0.01	–0.03
18.5	20	18.498	18.5065		0.01	–0.03
18.75	20	18.7478	18.7568		0.01	–0.03
19	20	18.9979	19.0063		0.01	–0.03
19.25	20	19.2476	19.2564		0.01	–0.03
19.5	20	19.4985	19.5068		0.01	–0.03
19.75	20	19.7484	19.7565		0.01	–0.03
20	20	19.9981	20.006		0.01	–0.03

7.2.2 Analog Output, AO1, and AO2 Configured as Current Output 4-20 mA

SET OUTPUT CURRENT, mA	FSV VALUE, mA	MEASUREMENT VALUE			AO1 DAC1 % FULL SCALE ERROR	AO2 DAC2 % FULL SCALE ERROR
		AO1 DAC1 MEASURED	AO2 DAC2 MEASURED	UNIT		
4	20	3.9997	4.0017		0.00	–0.01
4.25	20	4.24962	4.25145		0.00	–0.01
4.5	20	4.49968	4.50128		0.00	–0.01
4.75	20	4.7492	4.75127		0.00	–0.01
5	20	5.0002	5.00116		0.00	–0.01
5.25	20	5.25028	5.25145		0.00	–0.01
5.5	20	5.50005	5.50171		0.00	–0.01
5.75	20	5.74983	5.75211		0.00	–0.01
6	20	5.9976	6.00256		0.01	–0.01
6.25	20	6.24961	6.25285		0.00	–0.01
6.5	20	6.49969	6.50322		0.00	–0.02
6.75	20	6.74972	6.75335		0.00	–0.02
7	20	7.00008	7.0004		0.00	0.00
7.25	20	7.25002	7.2539		0.00	–0.02
7.5	20	7.49996	7.50364		0.00	–0.02
7.75	20	7.74985	7.75345		0.00	–0.02
8	20	7.99976	8.00338		0.00	–0.02
8.25	20	8.24968	8.25305		0.00	–0.02
8.5	20	8.49975	8.50294		0.00	–0.01
8.75	20	8.74981	8.75275		0.00	–0.01
9	20	9.00003	9.00262		0.00	–0.01
9.25	20	9.25009	9.25309		0.00	–0.02
9.5	20	9.50009	9.50337		0.00	–0.02
9.75	20	9.74985	9.75383		0.00	–0.02
10	20	9.99981	10.00425		0.00	–0.02
10.5	20	10.49956	10.50509		0.00	–0.03
11	20	10.99992	11.00612		0.00	–0.03
11.5	20	11.50001	11.50573		0.00	–0.03
12	20	11.9994	12.0043		0.00	–0.02
12.5	20	12.4989	12.5038	mA	0.01	–0.02
13	20	12.9991	13.0034		0.00	–0.02
13.5	20	13.4991	13.504		0.00	–0.02
14	20	13.9989	14.0047		0.01	–0.02
14.25	20	14.2486	14.2549		0.01	–0.02
14.5	20	14.4984	14.5053		0.01	–0.03
14.75	20	14.7484	14.7556		0.01	–0.03
15	20	14.9985	15.006		0.01	–0.03
15.25	20	15.2486	15.256		0.01	–0.03
15.5	20	15.4986	15.5058		0.01	–0.03
15.75	20	15.7486	15.7556		0.01	–0.03
16	20	15.9986	16.0055		0.01	–0.03
16.25	20	16.2485	16.2553		0.01	–0.03
16.5	20	16.4983	16.505		0.01	–0.02
16.75	20	16.7484	16.7548		0.01	–0.02
17	20	16.9985	17.0047		0.01	–0.02

17.25	20	17.2486	17.2551		0.01	–0.03
17.5	20	17.4987	17.5056		0.01	–0.03
17.75	20	17.7486	17.756		0.01	–0.03
18	20	17.9987	18.0065		0.01	–0.03
18.25	20	18.2484	18.2568		0.01	–0.03
18.5	20	18.4982	18.5072		0.01	–0.04
18.75	20	18.748	18.7575		0.01	–0.04
19	20	18.9981	19.0081	mA	0.01	–0.04
19.25	20	19.2485	19.258		0.01	–0.04
19.5	20	19.4985	19.5078		0.01	–0.04
19.75	20	19.7485	19.7576		0.01	–0.04
20	20	19.9986	20.0075		0.01	–0.04

7.2.3 Analog Output, AO1, and AO2 Configured as Current Output 0-24 mA

SET INPUT CURRENT, mA	FULL SCALE VALUE, mA	CURRENT MEASUREMENT VALUE			AO1 DAC1 % FULL SCALE ERROR	AO2 DAC2 % FULL SCALE ERROR
		AO1 DAC1 MEASURED	AO2 DAC2 MEASURED	UNIT		
0.1	24	99.87032	98.07372		0.00	0.01
0.125	24	124.5209	122.852		0.00	0.01
0.15	24	150.4937	148.694		0.00	0.01
0.175	24	175.3049	173.5619		0.00	0.01
0.2	24	199.9909	198.0814		0.00	0.01
0.225	24	224.7248	223.0289		0.00	0.01
0.25	24	250.6223	248.6949		0.00	0.01
0.275	24	275.1734	273.3579		0.00	0.01
0.3	24	299.8513	297.8974		0.00	0.01
0.325	24	324.8852	323.0695		0.00	0.01
0.35	24	350.7113	348.7406		0.00	0.01
0.375	24	375.1427	373.363		0.00	0.01
0.4	24	399.7972	397.8421	uA	0.00	0.01
0.425	24	425.4742	423.5846		0.00	0.01
0.45	24	450.545	448.5818		0.00	0.01
0.475	24	475.0135	473.1297		0.00	0.01
0.5	24	499.7403	497.8431		0.00	0.01
0.525	24	525.6163	523.7323		0.00	0.01
0.55	24	550.4853	548.5953		0.00	0.01
0.6	24	599.8369	598.0683		0.00	0.01
0.65	24	650.2754	648.435		0.00	0.01
0.7	24	700.0784	698.1349		0.00	0.01
0.75	24	750.4581	748.4394		0.00	0.01
0.8	24	800.3334	798.2528		0.00	0.01
0.85	24	850.3316	848.1239		0.00	0.01
0.9	24	900.9573	898.7574		0.00	0.01
0.95	24	950.4535	948.152		0.00	0.01
1	24	1.00106	0.99878		0.00	0.01
1.25	24	1.2503	1.24782	mA	0.00	0.01
1.5	24	1.50128	1.49842		-0.01	0.01
1.75	24	1.75177	1.7489		-0.01	0.00
2	24	2.00065	1.99792		0.00	0.01

2.25	24	2.25099	2.24837		0.00	0.01
2.5	24	2.50126	2.49877		-0.01	0.01
2.75	24	2.75001	2.748		0.00	0.01
3	24	3.00052	2.99879		0.00	0.01
3.25	24	3.25078	3.24911		0.00	0.00
3.5	24	3.49965	3.49839		0.00	0.01
3.75	24	3.74993	3.74915		0.00	0.00
4	24	3.99997	3.99927		0.00	0.00
4.25	24	4.2491	4.2488		0.00	0.00
4.5	24	4.49975	4.49949		0.00	0.00
4.75	24	4.75023	4.74932		0.00	0.00
5	24	4.99961	4.99857		0.00	0.01
5.5	24	5.50068	5.49864		0.00	0.01
6	24	6.00088	5.99849		0.00	0.01
6.5	24	6.50069	6.49785		0.00	0.01
7	24	7.00177	6.9984		-0.01	0.01
7.5	24	7.50223	7.49835		-0.01	0.01
8	24	8.00155	7.99778		-0.01	0.01
8.5	24	8.50197	8.49848		-0.01	0.01
9	24	9.00175	8.99894		-0.01	0.00
9.5	24	9.501	9.49875		0.00	0.01
10	24	10.00156	9.99948		-0.01	0.00
10.5	24	10.50149	10.49982		-0.01	0.00
11	24	11.0014	10.99895		-0.01	0.00
11.5	24	11.50253	11.49921		-0.01	0.00
12	24	12.0019	11.99914		-0.01	0.00
12.5	24	12.5016	12.4973	mA	-0.01	0.01
13	24	13.0027	12.9976		-0.01	0.01
13.5	24	13.5026	13.4969		-0.01	0.01
14	24	14.0025	13.9968		-0.01	0.01
14.5	24	14.5027	14.4975		-0.01	0.01
15	24	15.0018	14.9973		-0.01	0.01
15.5	24	15.5014	15.4975		-0.01	0.01
16	24	16.0017	15.9983		-0.01	0.01
16.5	24	16.5011	16.498		0.00	0.01
17	24	17.0012	16.9974		-0.01	0.01
17.5	24	17.5024	17.4976		-0.01	0.01
18	24	18.0022	17.9972		-0.01	0.01
18.5	24	18.5023	18.4967		-0.01	0.01
19	24	19.0033	18.9968		-0.01	0.01
19.5	24	19.5034	19.4964		-0.01	0.01
20	24	20.0029	19.9951		-0.01	0.02
20.25	24	20.253	20.2467		-0.01	0.01
20.5	24	20.5036	20.4971		-0.01	0.01
20.75	24	20.7525	20.7464		-0.01	0.01
21	24	21.0031	20.9973		-0.01	0.01
21.25	24	21.2536	21.2477		-0.01	0.01
21.5	24	21.5023	21.4968		-0.01	0.01
21.75	24	21.7526	21.7474		-0.01	0.01
22	24	22.003	21.9978		-0.01	0.01

22.25	24	22.2518	22.2468	mA	-0.01	0.01
22.5	24	22.5024	22.4976		-0.01	0.01
22.75	24	22.7532	22.7477		-0.01	0.01
23	24	23.0024	22.9969		-0.01	0.01
23.25	24	23.253	23.2472		-0.01	0.01
23.5	24	23.5038	23.4975		-0.02	0.01
23.75	24	23.7529	23.7464		-0.01	0.01
24	24	24.0035	23.9971		-0.01	0.01

7.2.4 Analog Output, AO1, and AO2 Configured as Voltage Output 0- to 10-V DC and 0- to 5-V DC

SET OUTPUT VOLTAGE, V	DAC OUTPUT RANGE	MEASUREMENT VALUE			AO1 DAC1 % FULL SCALE ERROR	AO2 DAC2 % FULL SCALE ERROR
		AO1 DAC1 MEASURED	AO2 DAC2 MEASURED	UNIT		
0.005	0-5 V	4.868999	5.035156	mV	0.00	0.00
0.01		9.916587	10.0263		0.00	0.00
0.025		24.84763	25.00812		0.00	0.00
0.05		49.86011	49.94755		0.00	0.00
0.075		74.95734	74.99169		0.00	0.00
0.1		100.0181	99.92604		0.00	0.00
0.125		124.9826	124.8608		0.00	0.00
0.15		149.9522	149.9081		0.00	0.00
0.175		174.8383	174.9206		0.00	0.00
0.2		199.8471	199.776		0.00	0.00
0.225		224.9545	224.8137		0.00	0.00
0.25		250.0344	249.8705		0.00	0.00
0.275		275.0932	274.7323		0.00	0.01
0.3		300.0721	299.7377		0.00	0.01
0.325		324.9859	324.8477		0.00	0.00
0.35		349.9569	349.8584		0.00	0.00
0.375		375.052	374.8493		0.00	0.00
0.4		400.1325	399.9271		0.00	0.00
0.425		425.1966	424.9536		0.00	0.00
0.45		450.1701	449.9747		0.00	0.00
0.475		475.0512	475.0025		0.00	0.00
0.5		500.0287	500.0953		0.00	0.00
0.55		550.1817	550.1099		0.00	0.00
0.6		600.1024	600.2095		0.00	0.00
0.65		649.9283	650.3012		0.00	–0.01
0.7		700.1171	700.4237		0.00	–0.01
0.75		750.1227	750.4047		0.00	–0.01
0.8		799.8744	800.5901		0.00	–0.01
0.85		850.0331	850.6152		0.00	–0.01
0.9		900.1051	900.6636		0.00	–0.01
0.95		949.9529	950.8422		0.00	–0.02
1		1.000061	1.000719	V	0.00	–0.01
1.25		1.25006	1.25051		0.00	–0.01
1.5		1.50025	1.50027		0.00	–0.01
1.75		1.75023	1.75043		0.00	–0.01
2		2.0002	2.00071		0.00	–0.01

2.25	0-5 V	2.25021	2.25094	V	0.00	–0.02
2.5		2.50018	2.50086		0.00	–0.02
2.75		2.75031	2.75056		–0.01	–0.01
3		3.00023	3.00082		0.00	–0.02
3.25		3.25025	3.25119		0.00	–0.02
3.5		3.50042	3.50139		–0.01	–0.03
3.75		3.75034	3.75127		–0.01	–0.02
4		4.00038	4.00102		–0.01	–0.02
4.25		4.25052	4.25123		–0.01	–0.02
4.25	0-10 V	4.25176	4.25337		–0.02	–0.03
4.5		4.50183	4.50349		–0.02	–0.03
4.75		4.75172	4.7534		–0.02	–0.03
5		5.0019	5.00353		–0.02	–0.03
5.25		5.25184	5.25318		–0.02	–0.03
5.5		5.50228	5.50311		–0.02	–0.03
5.75		5.75231	5.75331		–0.02	–0.03
6		6.00224	6.0038		–0.02	–0.04
6.25		6.25246	6.25431		–0.02	–0.04
6.5		6.50241	6.50473		–0.02	–0.05
6.75		6.75268	6.75525		–0.03	–0.05
7		7.00287	7.00531		–0.03	–0.05
7.25		7.25294	7.25295		–0.03	–0.03
7.5		7.50284	7.50525		–0.03	–0.05
7.75		7.75288	7.75507		–0.03	–0.05
8		8.00306	8.00494		–0.03	–0.05
8.25		8.25336	8.25497		–0.03	–0.05
8.5		8.50347	8.50554		–0.03	–0.05
8.75		8.75323	8.756		–0.03	–0.06
9		9.0034	9.00636		–0.03	–0.06
9.25		9.25336	9.25681		–0.03	–0.07
9.5		9.50339	9.50679		–0.03	–0.07
9.75		9.75365	9.75679		–0.04	–0.07
10		10.00343	10.00678		–0.03	–0.07

7.3 Test for Drift in Accuracy With Temperature Variation

7.3.1 Temperature Test at 65°C and –15°C for Analog Input (Voltage) and Analog Output (Voltage)

SET VALUE, V	CHANGE IN %ERROR WITH CHANGE IN TEMPERATURE			
	65°C	–15°C	65°C	–15°C
	AIN0 Δ Δ%ERROR / ΔT	AIN0 Δ%ERROR / ΔT	AIN1 Δ%ERROR / ΔT	AIN1 Δ%ERROR / ΔT
0.2	–0.002	–0.001	0.004	–0.009
0.3	–0.001	0.000	0.001	–0.007
0.4	–0.001	0.000	0.002	–0.004
0.5	0.000	0.000	0.001	–0.004
0.6	–0.001	0.000	0.002	–0.002
0.7	0.000	0.001	0.001	–0.002
0.8	0.000	0.000	0.002	–0.002
0.9	0.000	0.000	0.002	–0.001
1	0.000	0.000	0.002	–0.001
1.5	0.000	0.000	0.002	0.000
2	0.000	0.000	0.001	0.000
2.5	0.001	0.001	0.001	0.000
3	0.001	0.001	0.001	0.000
3.5	0.000	0.000	0.001	0.000
4	0.001	0.000	0.001	0.000
4.5	0.001	0.001	0.001	0.000
5.5	0.001	0.001	0.001	0.000
6	0.001	0.001	0.001	0.001
6.5	0.001	0.000	0.001	0.000
7	0.001	0.000	0.001	0.000
7.5	0.001	0.000	0.001	0.000
8.25	0.001	0.001	0.001	0.000
8.5	0.001	0.000	0.001	0.000
8.75	0.001	0.001	0.001	0.000
9	0.001	0.000	0.001	0.000
9.25	0.001	0.001	0.001	0.000
9.5	0.001	0.000	0.001	0.000
9.75	0.001	0.000	0.001	0.000
10	0.001	0.000	0.001	0.000

7.3.2 Temperature Test at 65°C and –15°C for Analog Input (Current) and Analog Output (Current)

SET VALUE, mA	CHANGE IN %ERROR WITH CHANGE IN TEMPERATURE	
	65°C	–15°C
	AIN3 Δ%ERROR / ΔT	AIN3 Δ%ERROR / ΔT
1	0.008	–0.011
2	0.007	–0.009
3	0.007	–0.010
4	0.006	–0.009
5	0.006	–0.009
6	0.006	–0.010
7	0.006	–0.009
8	0.006	–0.010
9	0.006	–0.010
10	0.009	–0.010
11	0.006	–0.010
12	0.006	–0.010
13	0.006	–0.010
14	0.006	–0.010
15	0.006	–0.010
16	0.006	–0.010
17	0.006	–0.010
18	0.006	–0.010
19	0.006	–0.010
20	0.006	–0.010
22	0.006	–0.010
23	0.006	–0.010
24	0.006	–0.010
24	0.006	–0.011

7.4 ESD Test

This TI Design has been tested for ESD as per the IEC61000-4-2 standard with a ±4-kV contact discharge. Discharge was applied to:

- Connector for analog outputs AO1 and AO2
- Connector for analog inputs AIN0-AIN3

Board functionality is tested before and after the test. This board received a Pass Class B.

7.5 Relay Drive Outputs

The relay drive outputs are tested with a 15-V supply input using the GUI. All of the output responds to the changes in the GUI.

7.6 Test With Isolated Communication Module (TIDA-00300)

This design integrates with the TIDA-00300 TI design, which provides isolated, SPI, and I2C communication; and a power supply at +15 V, –15 V, and ground.

For further design details, see the design files at TIDA-00300.

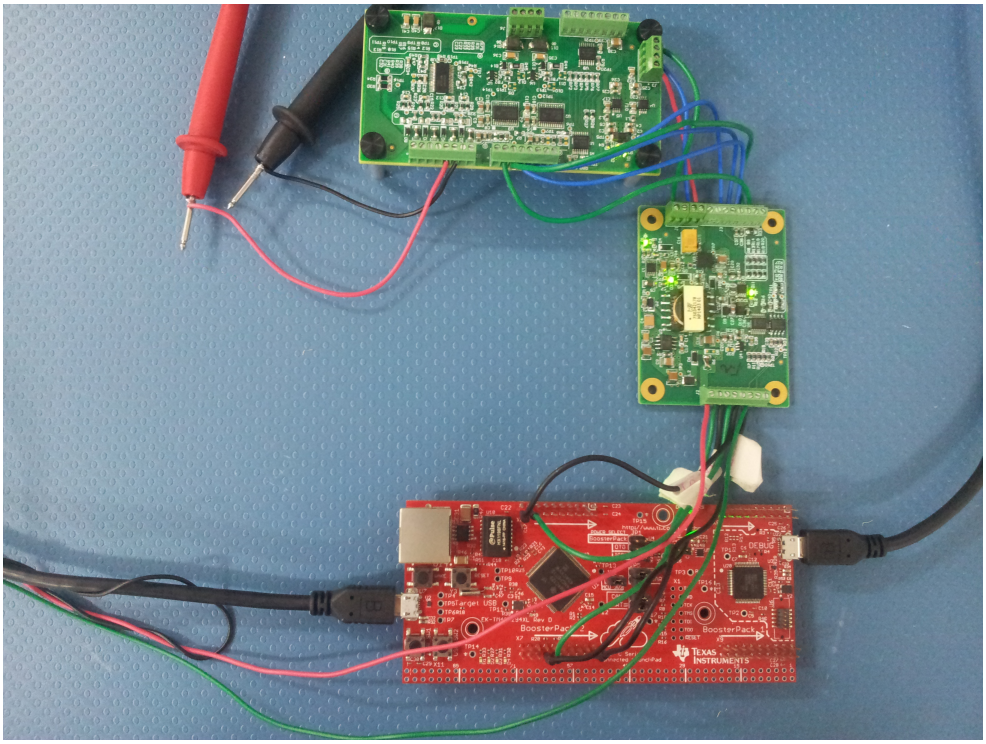


Figure 38. Interface With TIDA-00300 TI Design Board

This design uses an ISO7141CC (quad-channel digital isolator with a noise filter), which has a propagation delay time of 35 ns. To account for propagation delay, the SPI communication speed for ADC channels is adjusted to 12 MHz and the sampling rate to 300 kSPS.

This test is designed for analog input with the integration of the isolated communication module TIDA-00300. To test the analog output module, the use of an additional TIDA-00300 board is required, as only one SPI slave interfaces per board.

Table 34. Testing of Analog Input Current Channels (TIDA-00300)

SOURCE CURRENT, A	MEASURED CURRENT				BURDEN OHMS	VOLTAGE INPUT AT ADC, V	AIN2 READ ON GUI, V	AIN3 READ ON GUI, V	FSV, V	%FS ERROR AIN2	%FS ERROR AIN3
	AIN3 INPUT	UNIT	AIN4 INPUT	UNIT							
0.000100	99.66216		99.62533		200	0.02000	0.02011	0.02030	5.12	0.00	–0.01
0.000200	199.6694		199.6699		200	0.04000	0.04010	0.04029	5.12	0.00	–0.01
0.000300	299.6724		299.6776		200	0.06000	0.06009	0.06029	5.12	0.00	–0.01
0.000400	399.6885		399.7152		200	0.08000	0.08007	0.08026	5.12	0.00	0.00
0.000500	499.6995	µA	499.735	µA	200	0.10000	0.10006	0.10024	5.12	0.00	0.00
0.000600	599.7178		599.7549		200	0.12000	0.12004	0.12023	5.12	0.00	0.00
0.000600	699.7423		699.7799		200	0.14000	0.14004	0.14022	5.12	0.00	0.00
0.000800	799.7313		799.772		200	0.16000	0.16001	0.16018	5.12	0.00	0.00
0.000900	899.7295		899.7803		200	0.18000	0.18001	0.18016	5.12	0.00	0.00
0.001000	999.7378		999.860		200	0.20000	0.19999	0.19988	5.12	0.00	0.00
0.001500	1.49976		1.49983		200	0.30000	0.29990	0.29978	5.12	0.00	0.00
0.002000	1.99999		2.00001		200	0.40000	0.39984	0.39971	5.12	0.00	0.01
0.002500	2.50005		2.50008		200	0.50000	0.49974	0.49963	5.12	–0.01	0.01
0.003000	3.0001		3.00017		200	0.60000	0.59969	0.59958	5.12	–0.01	0.01
0.003500	3.5002		3.50027		200	0.70000	0.69960	0.69949	5.12	–0.01	0.01
0.004000	4.00033		4.0004		200	0.80000	0.79952	0.79942	5.12	–0.01	0.01
0.004500	4.50056		4.50063		200	0.90000	0.89947	0.89936	5.12	–0.01	0.01
0.005000	5.00054		5.00065		200	1.00000	0.99936	0.99927	5.12	–0.01	0.01
0.005500	5.50071		5.5008		200	1.10000	1.09929	1.09920	5.12	–0.01	0.02
0.006000	6.00075		6.00081		200	1.20000	1.19922	1.19911	5.12	–0.02	0.02
0.006500	6.50089		6.501		200	1.30000	1.29916	1.29906	5.12	–0.02	0.02
0.007000	7.00079		7.00097		200	1.40000	1.39905	1.39895	5.12	–0.02	0.02
0.007500	7.5011		7.50119		200	1.50000	1.49901	1.49891	5.12	–0.02	0.02
0.008000	8.0012		8.00126		200	1.60000	1.59895	1.59883	5.12	–0.02	0.02
0.008500	8.50121		8.50133		200	1.70000	1.69883	1.69874	5.12	–0.02	0.02
0.009000	9.00138		9.00144		200	1.80000	1.79876	1.79866	5.12	–0.02	0.03
0.009500	9.50135		9.50145		200	1.90000	1.89869	1.89859	5.12	–0.03	0.03
0.010000	10.00156		10.00178		200	2.00000	1.99861	1.99853	5.12	–0.03	0.03
0.010500	10.50152		10.50167		200	2.10000	2.09851	2.09843	5.12	–0.03	0.03
0.011000	11.00105		11.00117		200	2.20000	2.19840	2.19833	5.12	–0.03	0.03
0.011500	11.50116		11.50121		200	2.30000	2.29829	2.29826	5.12	–0.03	0.03
0.012000	12.0006		12.0006		200	2.40000	2.39829	2.39822	5.12	–0.03	0.03
0.012500	12.5007	mA	12.5009	mA	200	2.50000	2.49822	2.49815	5.12	–0.03	0.04
0.013000	12.999		12.9991		200	2.60000	2.59781	2.59773	5.12	–0.04	0.04
0.013500	13.4994		13.4994		200	2.70000	2.69782	2.69771	5.12	–0.04	0.04
0.014000	13.9995		13.9995		200	2.80000	2.79769	2.79762	5.12	–0.05	0.05
0.014500	14.4993		14.4995		200	2.90000	2.89757	2.89754	5.12	–0.05	0.05
0.015000	14.9993		14.9996		200	3.00000	2.99754	2.99747	5.12	–0.05	0.05
0.015500	15.4998		15.5		200	3.10000	3.09755	3.09747	5.12	–0.05	0.05
0.016000	16.0001		16.0001		200	3.20000	3.19884	3.19740	5.12	–0.02	0.05
0.016500	16.5004		16.5005		200	3.30000	3.29884	3.29758	10.24	–0.01	0.02
0.017000	17.0007		17.0009		200	3.40000	3.39883	3.39752	10.24	–0.01	0.02
0.017000	17.5007		17.5009		200	3.50000	3.49869	3.49742	10.24	–0.01	0.03
0.018000	18.0008		18.0009		200	3.60000	3.59864	3.59735	10.24	–0.01	0.03
0.018500	18.5008		18.501		200	3.70000	3.69861	3.69728	10.24	–0.01	0.03
0.019000	19.0012		19.0013		200	3.80000	3.79856	3.79722	10.24	–0.01	0.03

Table 34. Testing of Analog Input Current Channels (TIDA-00300) (continued)

SOURCE CURRENT, A	MEASURED CURRENT				BURDEN OHMS	VOLTAGE INPUT AT ADC, V	AIN2 READ ON GUI, V	AIN3 READ ON GUI, V	FSV, V	%FS ERROR AIN2	%FS ERROR AIN3
	AIN3 INPUT	UNIT	AIN4 INPUT	UNIT							
0.019500	19.5015	mA	19.5016	mA	200	3.90000	3.89853	3.89722	10.24	–0.01	0.03
0.020000	19.9995		19.9998		200	4.00000	3.99809	3.99674	10.24	–0.02	0.03
0.020500	20.4996		20.4998		200	4.10000	4.09799	4.09667	10.24	–0.02	0.03
0.021000	20.9997		20.9999		200	4.20000	4.19795	4.19660	10.24	–0.02	0.03
0.021500	21.5		21.5002		200	4.30000	4.29791	4.29658	10.24	–0.02	0.03
0.022000	22.0004		22.0005		200	4.40000	4.39791	4.39654	10.24	–0.02	0.03
0.022500	22.5003		22.5005		200	4.50000	4.49787	4.49647	10.24	–0.02	0.03
0.023000	23.0005		23.0008		200	4.60000	4.59786	4.59642	10.24	–0.02	0.03
0.023500	23.5007		23.5009		200	4.70000	4.69777	4.69636	10.24	–0.02	0.04
0.024000	24.0009		24.0012		200	4.80000	4.79772	4.79629	10.24	–0.02	0.04

7.7 Test Result Summary

Table 35. Test Result Summary

TEST RESULT SUMMARY		
ANALOG INPUT	AIN0-3 Tested as voltage channel	Accuracy is < ±0.1% full scale value at 25°C
	AIN2 and AIN3 used as current channel	Accuracy is < ±0.1% full scale value at 25°C
ANALOG OUTPUT	AO1 and AO2 used as current output	Accuracy is < ±0.1% full scale value at 25°C
	AO1 and AO2 used as voltage output	Accuracy is < ±0.1% full scale value at 25°C
RELAY DRIVE OUTPUT		Pass
INTEGRATION WITH TIDA-00300		Communication : Okay with 12-MHz speed and 300-kSPS sampling rate. Analog input accuracy tested for current channel is < ±0.1% full scale value at 25°C
EMC	ESD Immunity IEC61000-4-2	Pass

8 Design Files

8.1 Schematics

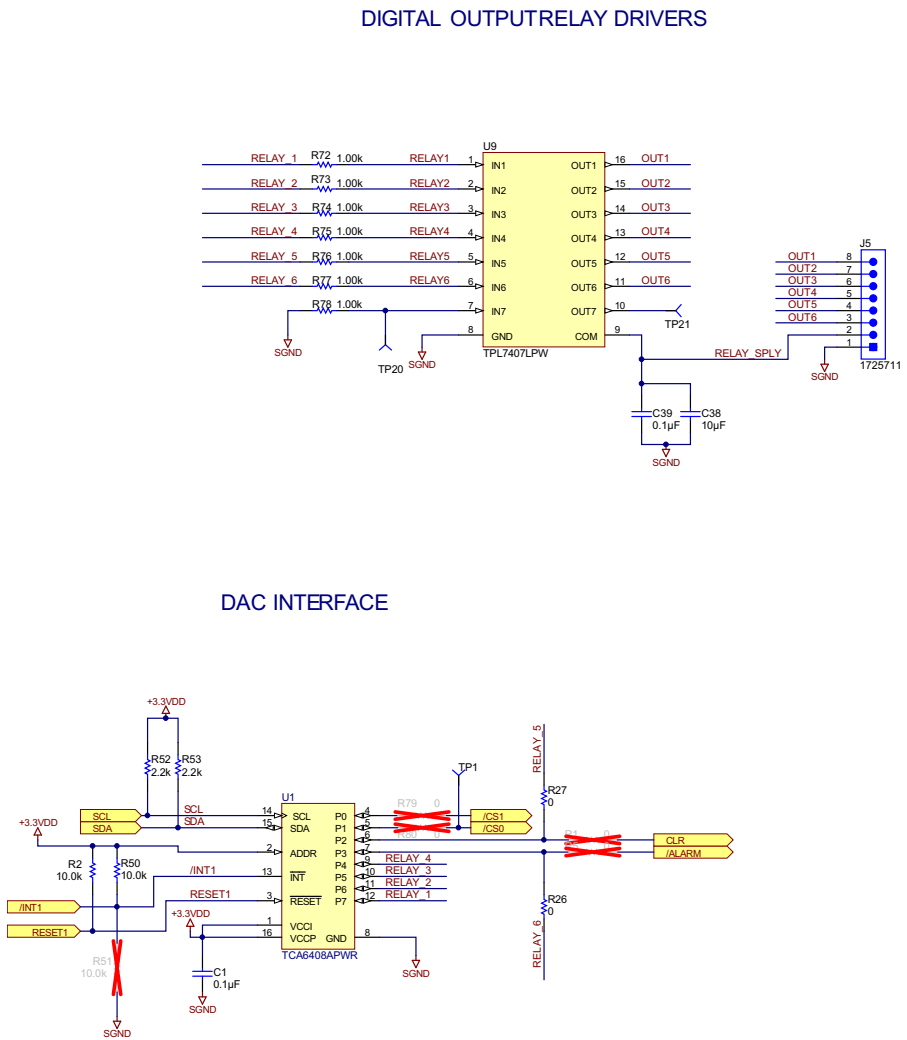


Figure 39. Digital Output and DAC Interface Schematic

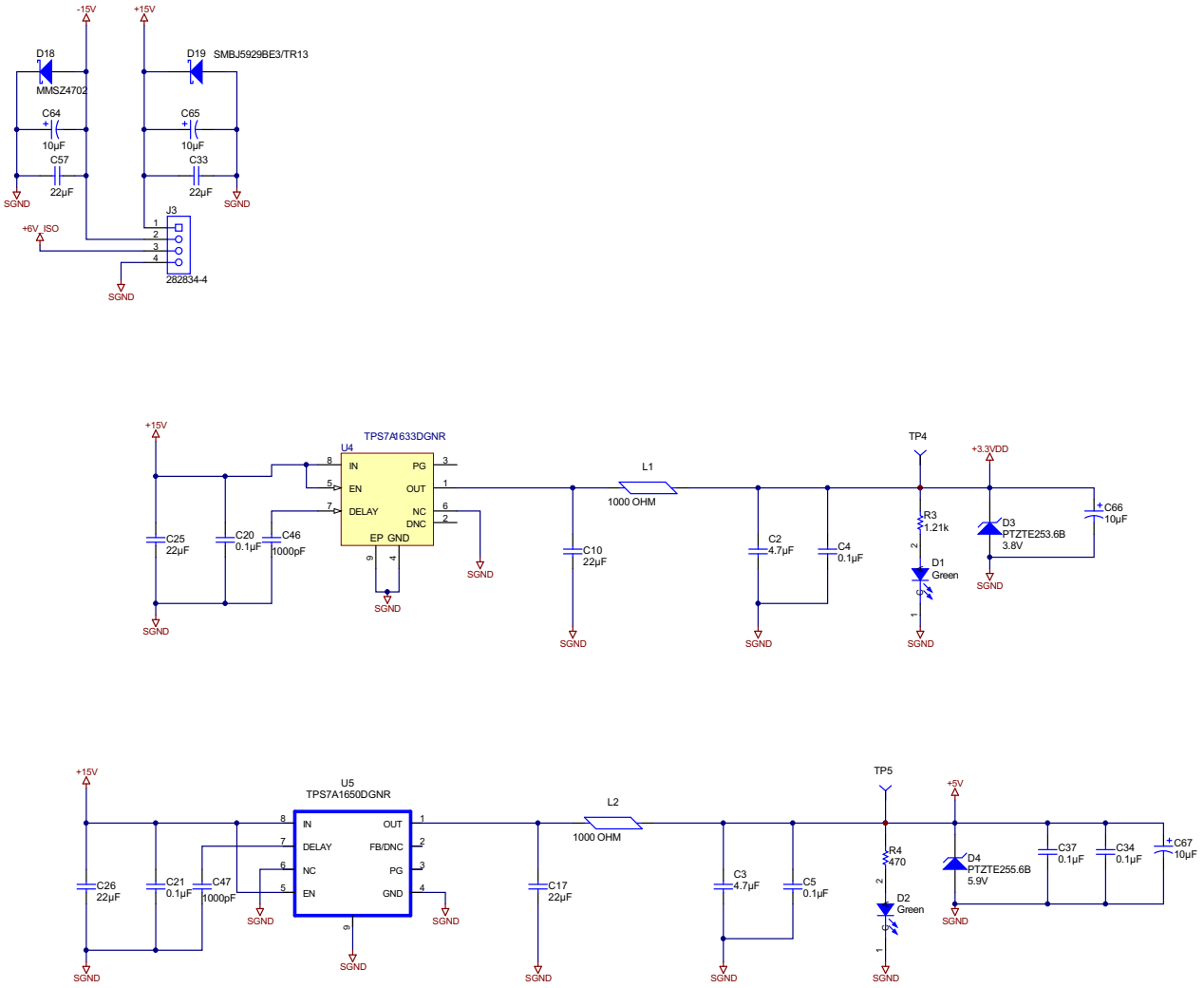


Figure 40. Digital Power Supply and Analog Power Supply Schematic

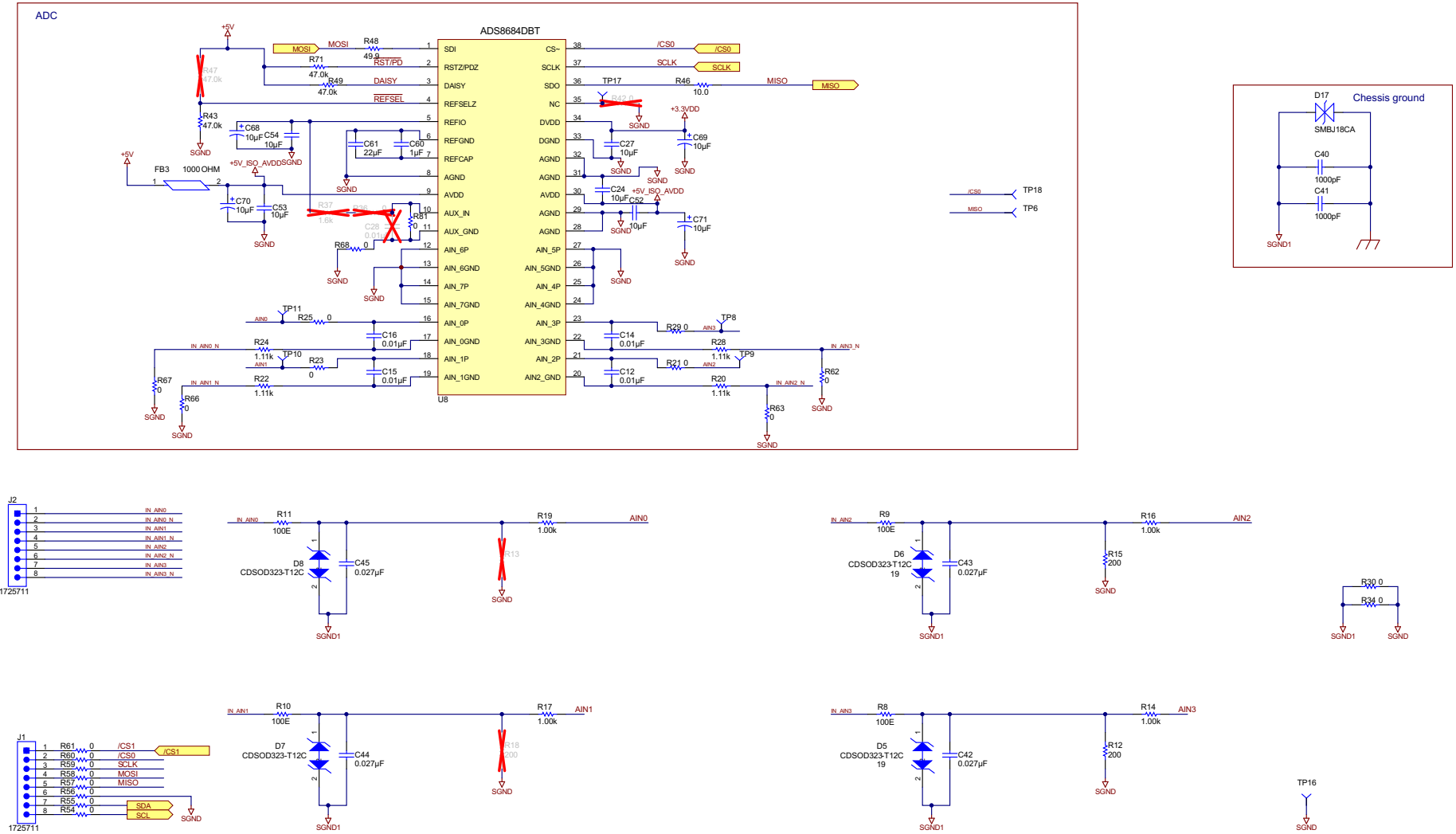


Figure 41. Analog Inputs Schematic

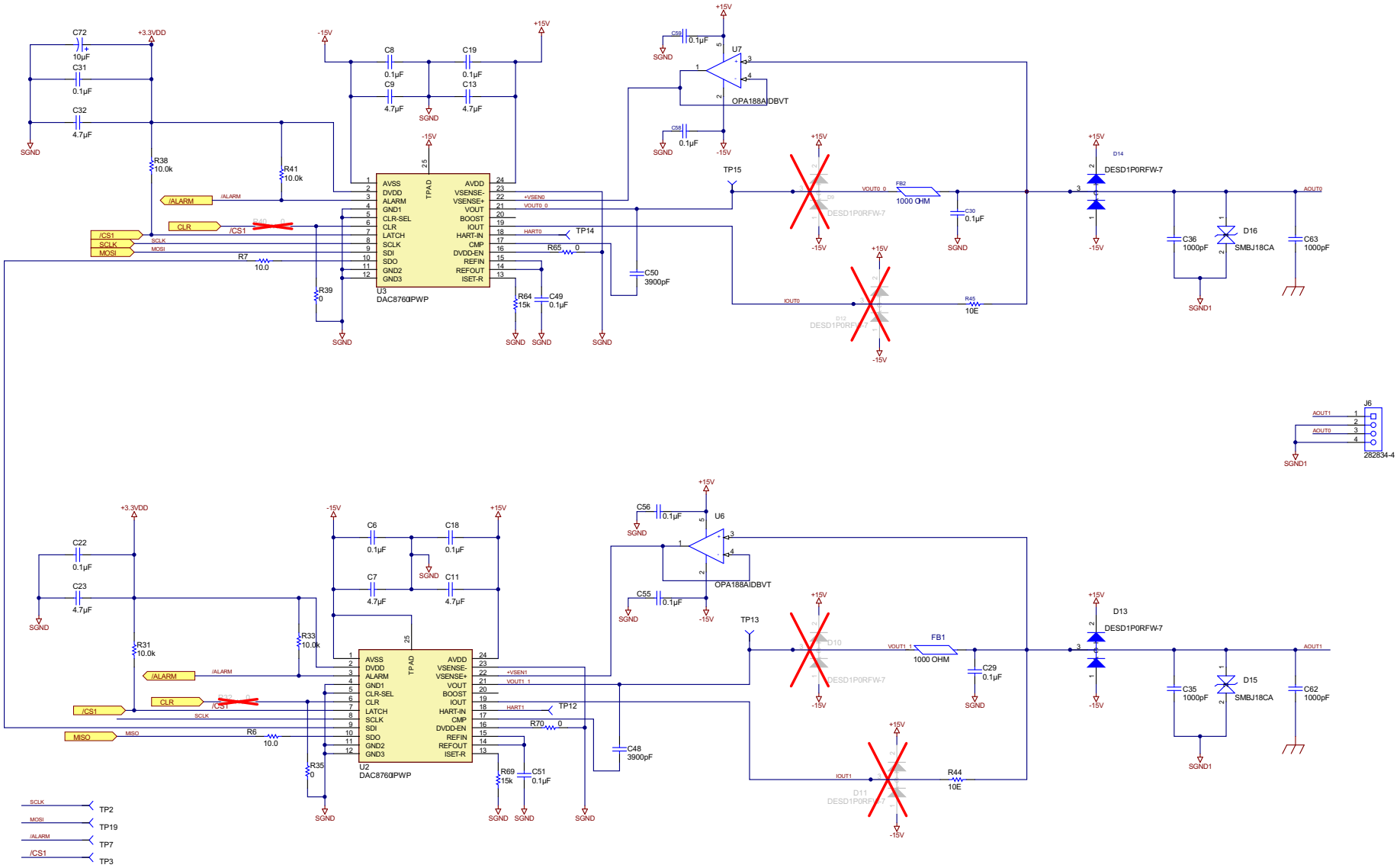


Figure 42. Analog Outputs Schematic

Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00310.

Table 36. BOM

FITTED	DESCRIPTION	DESIGNATOR	PART NUMBER	QUANTITY	MANUFACTURER	VALUE	FOOTPRINT
Fitted	Printed Circuit Board	!PCB	T	1	Any		
Fitted	CAP, CERM, 0.1 µF, 50 V, ±10%, X7R, 0603	C1, C4, C5, C6, C8, C18, C19, C20, C21, C22, C29, C30, C31, C34, C37, C39, C49, C51, C55, C56, C58, C59	06035C104KAT2A	22	AVX	0.1 µF	0603
Fitted	CAP, CERM, 4.7 µF, 50 V, ±10%, X5R, 0805	C2, C3, C7, C9, C11, C13, C23, C32	C2012X5R1H475K125AB	8	TDK	4.7 µF	0805_HV
Fitted	CAP, CERM, 22 µF, 16 V, ±20%, X5R, 0805	C10, C17, C25, C26, C33, C57	GRM21BR61C226ME44	6	MuRata	22 µF	0805_HV
Fitted	CAP, CERM, 0.01 µF, 100 V, ±5%, X7R, 0603	C12, C14, C15, C16	06031C103JAT2A	4	AVX	0.01 µF	0603
Fitted	CAP, CERM, 10 µF, 16 V, ±20%, X5R, 0603	C24, C52, C53	EMK107BBJ106MA-T	3	Taiyo Yuden	10 µF	0603
Fitted	CAP, CERM, 10 µF, 25 V, ±20%, X5R, 0603	C27	C1608X5R1E106M080AC	1	TDK	10 µF	0603
Fitted	CAP, CERM, 1000 pF, 2 kV 10% X7R 1206	C35, C36, C40, C41, C62, C63	202R18W102KV4E	6	Johanson Dielectrics Inc	1000 pF	1206
Fitted	CAP, CERM, 10 µF, 50 V, ±10%, X7R, 1210	C38	GRM32ER71H106KA12L	1	MuRata	10 µF	1210
Fitted	CAP, CERM, 0.027 µF, 50 V, ±5%, C0G/NP0, 1206	C42, C43, C44, C45	GRM3195C1H273JA01D	4	MuRata	0.027 µF	1206
Fitted	CAP, CERM, 1000 pF, 100 V, ±5%, X7R, 0603	C46, C47	06031C102JAT2A	2	AVX	1000 pF	0603
Fitted	CAP, CERM, 3900 pF, 50 V, ±10%, X7R, 0603	C48, C50	GRM188R71H392KA01D	2	MuRata	3900 pF	0603
Fitted	CAP, CERM, 10 µF, 16 V, ±20%, X5R, 0805	C54	0805YD106MAT2A	1	AVX	10 µF	0805_HV
Fitted	CAP, CERM, 1 µF, 16 V, ±10%, X7R, 0603	C60	EMK107B7105KA-T	1	Taiyo Yuden	1 µF	0603
Fitted	CAP, CERM, 22 µF, 16 V, ±10%, X5R, 0805	C61	C2012X5R1C226K125AC	1	TDK	22 µF	0805_HV
Fitted	CAP, TA, 10 µF, 25 V, ±10%, 1.5 Ω, SMD	C64	293D106X9025C2TE3	1	Vishay-Sprague	10 µF	6032-28
Fitted	CAP, TA, 10 µF, 25 V, ±10%, 0.3 Ω, SMD	C65	TPSC106K025R0300	1	AVX	10 µF	6032-28

Table 36. BOM (continued)

Fitted	CAP, TA, 10 µF, 20 V, ±10%, 1 Ω, SMD	C66, C67	TPSB106K020R1000	2	AVX	10 µF	3528-21
Fitted	CAP, TA, 10 µF, 10 V, ±20%, 1.8 Ω, SMD	C68, C69, C70, C71, C72	TPSA106M010R1800	5	AVX	10 µF	3216-18
Fitted	LED SmartLED Green 570 NM	D1, D2	LG L29K-G2J1-24-Z	2	OSRAM	Green	LED0603AA
Fitted	DIODE ZENER 3.8 V ,1 W PMDS	D3	PTZTE253.6B	1	Rohm Semiconductor	3.8 V	powerDI123
Fitted	DIODE ZENER 5.9 V, 1 W PMDS	D4	PTZTE255.6B	1	Rohm Semiconductor	5.9 V	powerDI123
Fitted	Diode, TVS, ARRAY, 19 V, SOD323	D5, D6, D7, D8	CDSOD323-T12C	4	Bourns Inc.	19	sod-323
Fitted	Diode, P-N, 70 V, 0.2 A, SOT-323	D13, D14	DESD1P0RFW-7	2	Diodes Inc	DESD1P0RFW-7	SOT-323
Fitted	TVS 18 V 600 W Bi-Dir SMB	D15, D16, D17	SMBJ18CA	3	Littelfuse Inc	SMBJ18CA	DIO_SMB_BIAAAA
Fitted	Diode Zener 15 V ,500 mW SOD123	D18	MMSZ4702	1	Fairchild semiconductor	15 V	SOD-123
Fitted	Diode Zener 15 V, 2 W D0214AA	D19	SMBJ5929BE3/TR13	1	Microsemi Commercial Component Group	15 V	SMB
Fitted	Ferrite Chip 1000 Ω, 300 mA 0603	FB1, FB2	MMZ1608Y102B	2	TDK Corporation	1000 Ω	FB0603
Fitted	Ferrite Chip 1000 Ω, 300 mA 0603	FB3, L1, L2	MMZ1608B102C	3	TDK Corporation	1000 Ω	FB0603
Not Fitted		FID1, FID2, FID3, FID4, FID5, FID6		6			FID_TOP_40_80BA
Fitted	Machine Screw, Round, #4-40 x ¼, Nylon, Philips Panhead	H1, H2	NY PMS 440 0025 PH	2	B&F Fastener Supply		NY PMS 440 0025 PH
Fitted	Terminal Block, 8 x 1, 2.54 mm, TH	J1, J2, J5	1725711	3	Phoenix Contact		CONN_1725711
Fitted	Receptacle, 100 mil, 4 × 1 TH	J3, J6	282834-4	2	TE Connectivity		TEC_282834-4
Fitted	Mount-In Hole, NPTH Drill 3.2 mm	MH1, MH2		2			MH3.2_H5_W6_KO8_STARHEAD
Fitted	RES, 10.0 kΩ, 0.1%, 0.1 W, 0603	R2, R31, R33, R38, R41, R50	RG1608P-103-B-T5	6	Susumu Co Ltd	10.0 k	0603
Fitted	RES, 1.21 kΩ, 0.1%, 0.1 W, 0603	R3	RT0603BRD071K21L	1	Yageo America	1.21 k	0603
Fitted	RES, 470 Ω, 5%, 0.1 W, 0603	R4	CRCW0603470RJNEA	1	Vishay-Dale	470	0603
Fitted	RES, 10.0 Ω, 1%, 0.1 W, 0603	R6, R7, R46	CRCW060310R0FKEA	3	Vishay-Dale	10.0	0603
Fitted	RES 100 Ω .4 W 1% 0204 MELF	R8, R9, R10, R11	MMA02040C1000FB300	4	Vishay Beyschlag	100 E	1206
Fitted	RES, 200 Ω, 0.1%, 0.125 W, 0805	R12, R15	RG2012P-201-B-T5	2	Susumu Co Ltd	200	0805
Fitted	RES, 1.00 kΩ, 1%, 0.1 W, 0603	R14, R16, R17, R19, R72, R73, R74, R75, R76, R77, R78	CRCW06031K00FKEA	11	Vishay-Dale	1.00 k	0603
Fitted	RES, 1.11 kΩ, 0.1%, 0.1 W, 0603	R20, R22, R24, R28	RT0603BRD071K11L	4	Yageo America	1.11 k	0603

Table 36. BOM (continued)

Fitted	RES, 0 Ω, 5%, 0.1 W, 0603	R21, R23, R25, R26, R27, R29, R35, R39, R54, R55, R56, R57, R58, R59, R60, R61, R65, R68, R70, R81	RC0603JR-070RL	20	Yageo America	0	0603
Fitted	RES, 0 Ω, 5%, 0.25 W, 1206	R30, R34	RC1206JR-070RL	2	Yageo America	0	1206
Fitted	RES, 47.0 kΩ, 0.1%, 0.1 W, 0603	R43, R49, R71	RT0603BRD0747KL	3	Yageo America	47.0 k	0603
Fitted	RES, 10 Ω, 5%, 0.25 W, 1206	R44, R45	CRCW120610R0JNEA	2	Vishay-Dale	10 E	1206
Fitted	RES, 49.9 Ω, 0.1%, 0.1 W, 0603	R48	RT0603BRD0749R9L	1	Yageo America	49.9	0603
Fitted	RES, 2.2 kΩ, 5%, 0.1 W, 0603	R52, R53	CRCW06032K20JNEA	2	Vishay-Dale	2.2 k	0603
Fitted	RES 0.0 Ω, .5 W, JUMP 1206 SMD	R62, R63, R66, R67	CRCW12060000Z0EAHP	4	Vishay Dale	0	1206
Fitted	RES, 15 kΩ, 1/10 W, 0.1% 0603	R64, R69	RT0603BRB0715KL	2	Vishay-Dale	15 k	0603
Fitted	Test Point 40 mil Pad 20 mil Drill	TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10, TP11, TP12, TP13, TP14, TP15, TP16, TP17, TP18, TP19, TP20, TP21	STD	21	STD	STD	TP1_PD40_D0.5_S50
Fitted	Low-Voltage 8-Bit I2C and SMBus I/O Expander, 1.65 to 5.5 V, –40 to 85°C, 16-Pin TSSOP (PW), Green (RoHS and No Sb/Br)	U1	TCA6408APWR	1	Texas Instruments		PW0016A_N
Fitted	1-Channel, 16-Bit, Programmable Current/Voltage Output DAC for 4 - to 20-mA Current Loop Applications	U2, U3	DAC8760IPWP	2	Texas Instruments		PWP24-DIE84X166
Fitted	Single Output LDO, 100 mA, Fixed 3.3-V Output, 3- to 60-V Input, with Enable and Power Good, 8-Pin MSOP (DGN), –40 to 125°C, Green (RoHS and No Sb/Br)	U4	TPS7A1633DGNR	1	Texas Instruments		DGN0008C_N
Fitted	IC, 60 V, 6-A IQ, 100 mA, LDO Voltage Regulator With Enable and Power-Good Functions	U5	TPS7A1650DGNR	1	TI	TPS7A1650DGNR	DGN_8P
Fitted	Precision, Low-Noise, Rail-to-Rail Output, 36-V Zero-Drift Operational Amplifier	U6, U7	OPA188AIDBVT	2	Texas Instruments	OPA188AIDBVT	DBV0005A_L
Fitted	16-Bit 400 KSPS 4-Channel SAR ADC	U8	ADS8684DBT	1	TI		DBT0038A_M
Fitted	40-V 7-Channel Low Side Driver, PW0016A	U9	TPL7407LPW	1	Texas Instruments		PW0016A_N
Not Fitted	CAP, CERM, 0.01 µF, 100 V, ±5%, X7R, 0603	C28	06031C103JAT2A	0	AVX	0.01 µF	0603

Table 36. BOM (continued)

Not Fitted	Diode, P-N, 70 V, 0.2 A, SOT-323	D9, D10, D11, D12	DESD1P0RFW-7	0	Diodes Inc	DNP	SOT-323
Not Fitted	RES, 0 Ω, 5%, 0.1 W, 0603	R1, R5, R32, R36, R40, R42, R79, R80	RC0603JR-070RL	0	Yageo America	0	0603
Not Fitted	RES, 200 Ω, 0.1%, 0.125 W, 0805	R13	RG2012P-201-B-T5	0	Susumu Co Ltd		0805
Not Fitted	RES, 200 Ω, 0.1%, 0.125 W, 0805	R18	RG2012P-201-B-T5	0	Susumu Co Ltd	200	0805
Not Fitted	RES, 1.6 kΩ, 5%, 0.1 W, 0603	R37	CRCW06031K60JNEA	0	Vishay-Dale	1.6 k	0603
Not Fitted	RES, 47.0 kΩ, 0.1%, 0.1 W, 0603	R47	RT0603BRD0747KL	0	Yageo America	47.0 k	0603
Not Fitted	RES, 10.0 kΩ, 0.1%, 0.1 W, 0603	R51	RG1608P-103-B-T5	0	Susumu Co Ltd	10.0 k	0603

8.2 Layer Plots

To download the layer plots, see the design files at TIDA-00310.

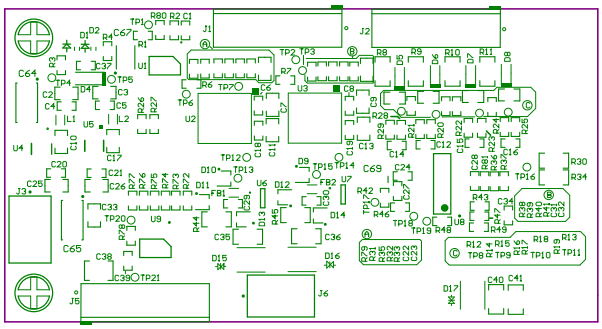


Figure 43. Top Overlay

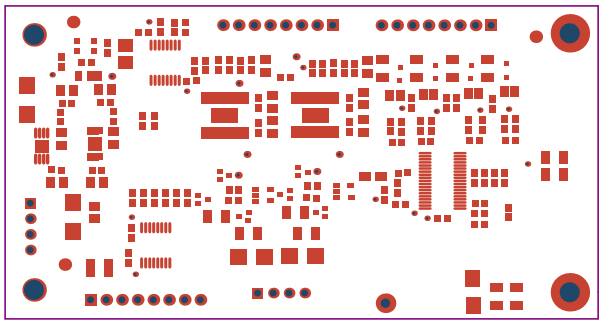


Figure 44. Top Solder Mask

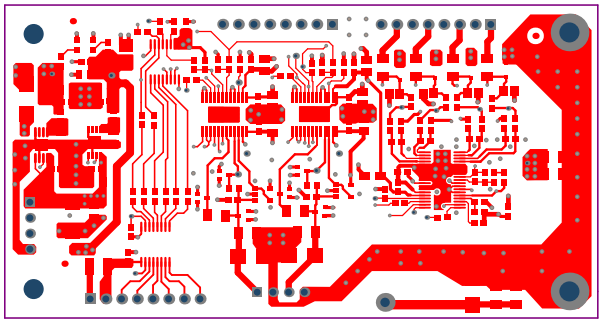


Figure 45. Top Layer

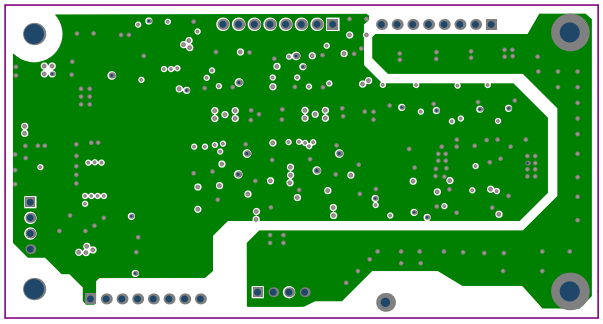


Figure 46. Midlayer 1

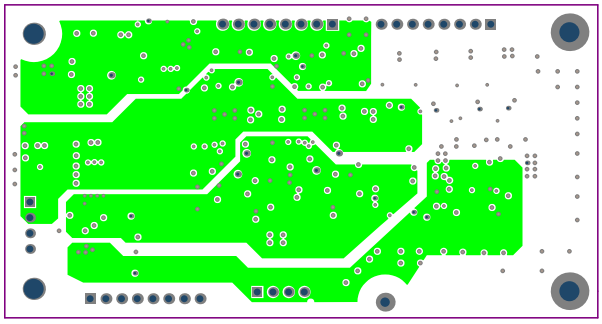


Figure 47. Midlayer 2

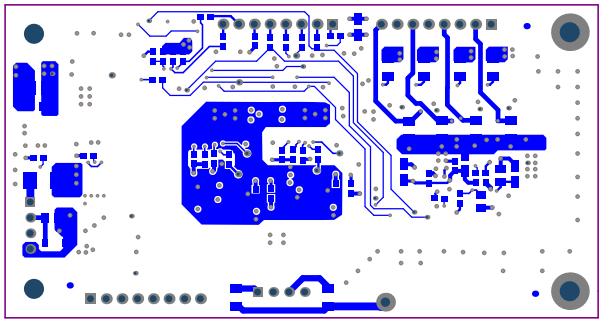


Figure 48. Bottom Layer

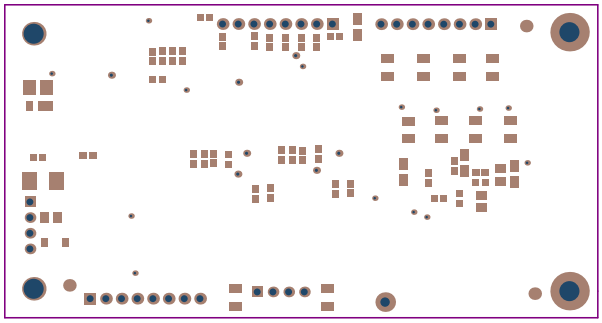


Figure 49. Bottom Solder Mask

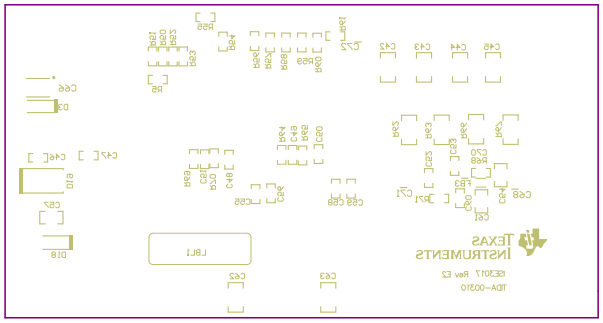


Figure 50. Bottom Overlay

Figure 51. Board Outline

8.3 Gerber Files

To download the Gerber files, see the design files at TIDA-00310.

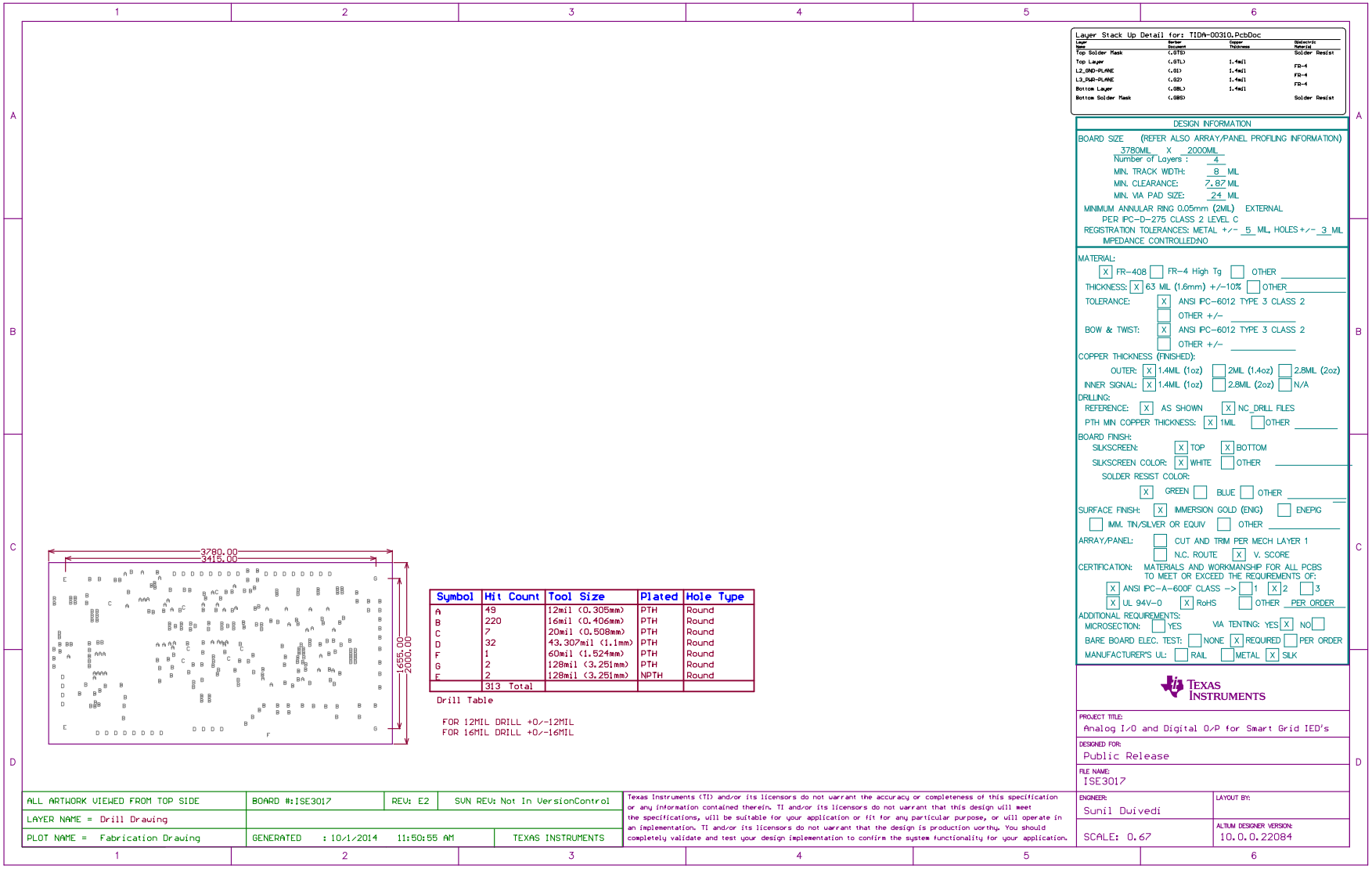


Figure 52. Fabrication Drawing

8.4 Assembly Drawings

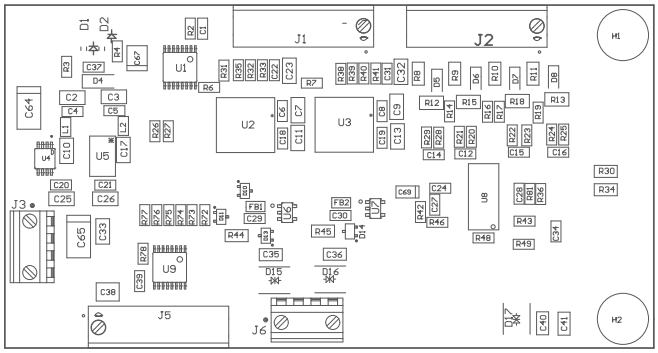


Figure 53. Top Assembly Drawing

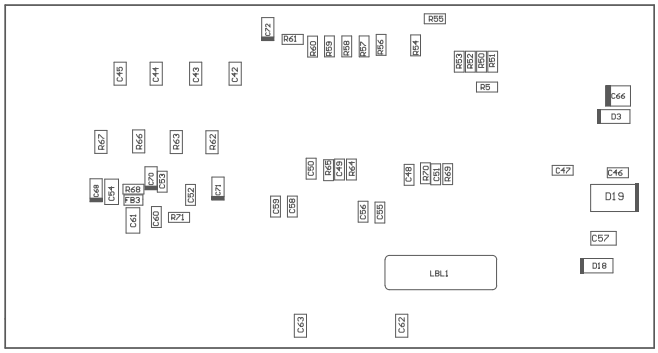


Figure 54. Bottom Assembly Drawing

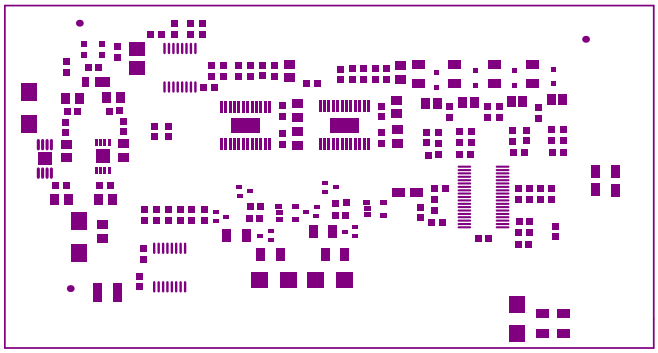


Figure 55. Top Paste

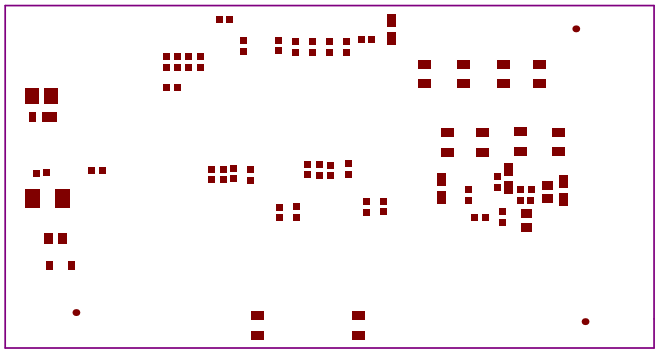


Figure 56. Bottom Paste

8.5 Software Files

To download the software files, see the design files at TIDA-00310.

9 References

1. Texas Instruments, *ADS868x 16-Bit, 500-kSPS, 4- and 8-Channel, Single-Supply, SAR ADCs with Bipolar Input Ranges*, Data Sheet (SBAS582).
2. Texas Instruments, *Single-Channel, 12- and 16-Bit Programmable Current Output and Voltage Output Digital-to-Analog Converters for 4-mA to 20-mA Current Loop Applications*, Data Sheet (SBAS528).
3. Texas Instruments, *Low-Voltage 8-Bit I_2C and SMBus I/O Expander With Interrupt Output, Reset, and Configuration Registers*, Data Sheet (SCPS192).
4. Texas Instruments, *16-Bit Analog Output Module Reference Design for Programmable Logic Controllers (PLCs)*, Reference Guide (TIDU189).
5. Texas Instruments, *TPL7407L 40-V 7-Channel Low Side Driver*, Data Sheet (SLRS066).
6. Texas Instruments, *60-V, 5-μA I_Q, 100-mA, Low-Dropout Voltage Regulator With Enable and Power-Good*, Data Sheet (SBVS171).
7. Texas Instruments, *16-Bit, 8-Channel, Software Configurable Analog Input Module for Programmable Logic Controllers (PLCs)*, User Guide (TIDU365).

10 About the Author

SUNIL DWIVEDI is a systems engineer at Texas Instruments where he is responsible for developing reference design solutions for the industrial segment. Sunil brings to this role his experience in high-speed digital and analog systems design. Sunil earned his bachelor of electronics (BE) in electronics and instrumentation engineering (BE E&I) from SGSITS, Indore, India.

VIVEK G is a firmware architect at Texas Instruments where he is responsible for developing reference design solutions for the industrial systems segment. Vivek brings to this role his experience in developing firmware architecture design in substation protection and automation. Vivek earned his bachelor of electronics (BE) in electrical & electronics engineering (EEE) and masters in sensor system technology.

IMPORTANT NOTICE FOR TI REFERENCE DESIGNS

Texas Instruments Incorporated ("TI") reference designs are solely intended to assist designers (“Buyers”) who are developing systems that incorporate TI semiconductor products (also referred to herein as “components”). Buyer understands and agrees that Buyer remains responsible for using its independent analysis, evaluation and judgment in designing Buyer’s systems and products.

TI reference designs have been created using standard laboratory conditions and engineering practices. **TI has not conducted any testing other than that specifically described in the published documentation for a particular reference design.** TI may make corrections, enhancements, improvements and other changes to its reference designs.

Buyers are authorized to use TI reference designs with the TI component(s) identified in each particular reference design and to modify the reference design in the development of their end products. HOWEVER, NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY THIRD PARTY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT, IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI REFERENCE DESIGNS ARE PROVIDED "AS IS". TI MAKES NO WARRANTIES OR REPRESENTATIONS WITH REGARD TO THE REFERENCE DESIGNS OR USE OF THE REFERENCE DESIGNS, EXPRESS, IMPLIED OR STATUTORY, INCLUDING ACCURACY OR COMPLETENESS. TI DISCLAIMS ANY WARRANTY OF TITLE AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, QUIET ENJOYMENT, QUIET POSSESSION, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS WITH REGARD TO TI REFERENCE DESIGNS OR USE THEREOF. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY BUYERS AGAINST ANY THIRD PARTY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON A COMBINATION OF COMPONENTS PROVIDED IN A TI REFERENCE DESIGN. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, SPECIAL, INCIDENTAL, CONSEQUENTIAL OR INDIRECT DAMAGES, HOWEVER CAUSED, ON ANY THEORY OF LIABILITY AND WHETHER OR NOT TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES, ARISING IN ANY WAY OUT OF TI REFERENCE DESIGNS OR BUYER’S USE OF TI REFERENCE DESIGNS.

TI reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques for TI components are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

Reproduction of significant portions of TI information in TI data books, data sheets or reference designs is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards that anticipate dangerous failures, monitor failures and their consequences, lessen the likelihood of dangerous failures and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in Buyer’s safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed an agreement specifically governing such use.

Only those TI components that TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components that have ***not*** been so designated is solely at Buyer's risk, and Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265