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Analog Input Module for Industrial Outputs and Temperature Sensors Reference Design

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Circuit Description

This design accepts inputs from standard voltage and current industrial outputs along with RTD and thermocouple temperature sensors. The industrial input ranges include: 4-20 mA, 0-20 mA, +/-25 mA, 0-5 V, 0-10 V, +/-5 V, +/-10 V. The design includes conditioning and level-shift circuitry which converts the large industrial outputs into a proper input range for a +5V delta-sigma ADC. The ADC has features to directly acquire information from the RTD and thermocouple sensors over their full temperature range.

Design Resources

Design Archive	All Design files
ADS1248	Product Folder
INA826	Product Folder
INA159	Product Folder
REF5025	Product Folder

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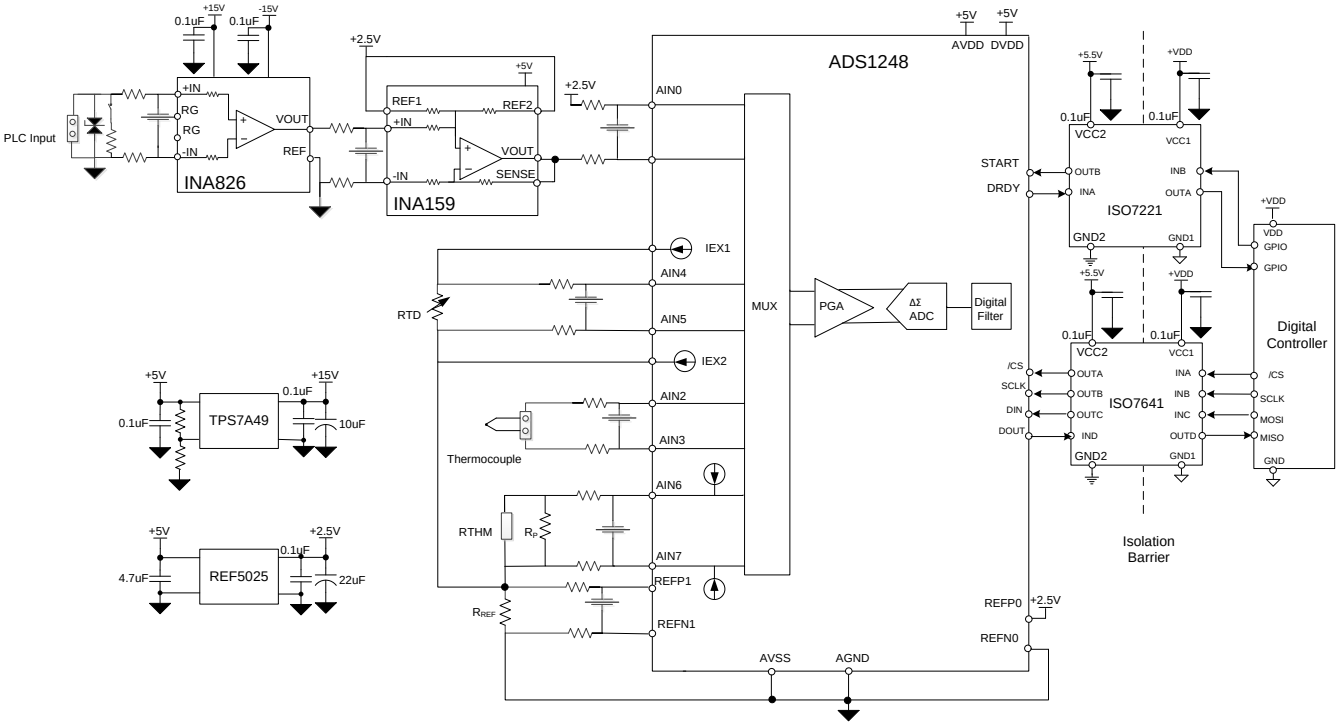

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1 Design Summary

The design requirements are as follows:

- Supply Voltage: +/-15 V
- Digital Output: 4-Wire SPI
- Digital Isolation: 4 kV
- Resolution: 24-Bit
- Industrial Inputs: Voltage +/-10 V, 0-5 V, 0-10 V, +/-5 V; Current +/-25 mA, 4-20 mA, 0-20 mA
- Temperature input: RTD -200°C ~850°C, Thermocouple -200°C~1200°C, Thermistor 0°C~50°C
- Ambient Temperature: 25 °C

The design goals and performance are summarized in Table 1. The results for the industrial voltage input circuit are shown in Figure 1.

Table 1: Comparison of Design Goals, Simulated, and Measured Performance

		Goals	Calculated	Measured
Voltage (+/-10 V)	**TUE (%FSR)**	0.1%	0.052%	0.021%
	Calibrated Error	0.01%	-	0.0005%
Current (+/-25mA)	**TUE (%FSR)**	0.1%	0.128%	0.0044%
	Calibrated Error	0.01%	-	0.0015%
Thermocouple	**TUE (%FSR)**	0.1%	0.064%	0.039%
	Calibrated Error	0.01%	0.007%	0.0071%
Thermistor	**TUE (%FSR)**	0.25%	0.183%	0.22%
	Calibrated Error	0.05%	-	0.044%
RTD	**TUE (%FSR)**	0.1%	0.074%	0.032%
	Calibrated Error	0.01%	0.0011%	0.001%

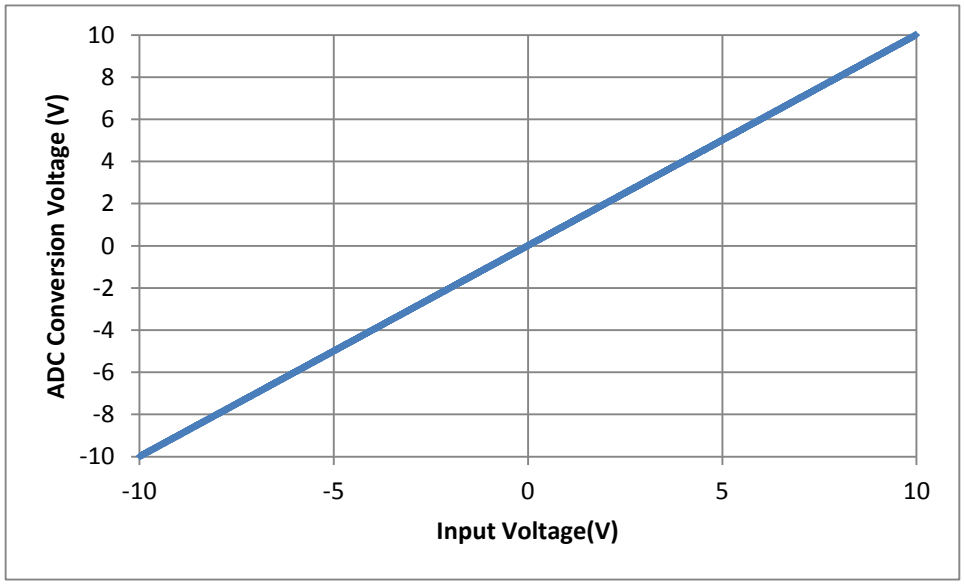

Figure 1: Measured Industrial Voltage Input Results

2 Theory of Operation

This analog input module can accept the standard industrial voltage and current inputs along with temperature inputs from RTDs, thermocouples, and thermistors. The circuitry for this input module revolves around a highly integrated 24-bit delta-sigma converter which includes the required excitation and biasing circuitry to directly acquire the temperature input signals. A high impedance instrumentation amplifier (INA) and attenuating difference amplifier are used to reduce the large industrial voltage and current inputs to levels within range of the +5 V ADC. A detailed schematic for this design is shown in Figure 2.

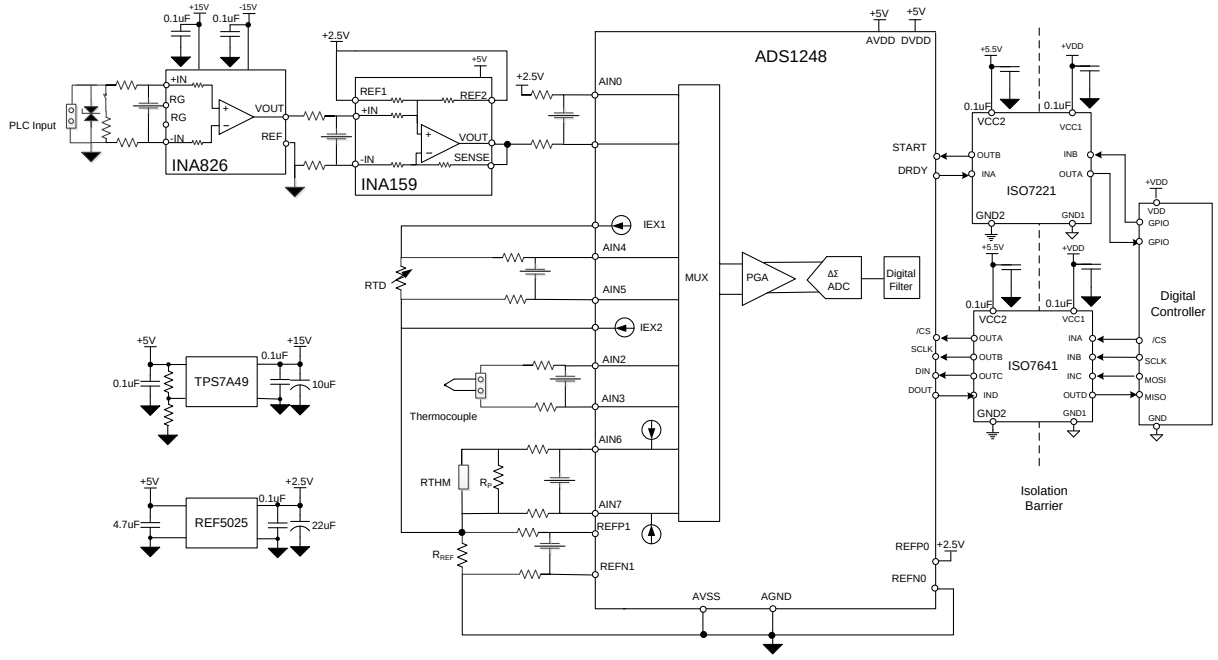

Figure 2: Detailed Analog Input Schematic

2.1 Industrial Voltage and Current Inputs

As shown in Figure 3, the input circuit for industrial voltages and currents is composed of an instrumentation amplifier INA826 and a difference amplifier INA159. The INA826 is used as a high-impedance buffer for the input signals. This prevents the input impedance of the difference amplifier from causing errors due to interactions with the input source impedance. The INA159 is a precision gain of 0.2 V/V difference amplifier which is used to attenuate and level-shift the large industrial voltage signals to a proper input range for the +5V ADC. Switch S1 closes when acquiring industrial current inputs. This places placing a sense resistor in series with the current flow roducing a voltage proportional to the input current.

The output of the INA159 connects to the AIN0 input of the ADS1248 and the mid-supply reference connects to AIN1. The external reference voltage connected between REFP0 and REFN0 is used as the reference voltage for the ADC. The transfer function for the ADC output is shown in Equation (**1**) where "GAIN" is the ADS1248 PGA gain setting.

Due to the effects of aliasing, any ADC, regardless of architecture, need some amount of filtering on its inputs to reduce noise in the system. The filters are important for rejecting any noise that might be subjected to the ADC inputs that are near the modulator sampling speed. The simple RC filter shown in Figure 2 offers adequate performance.

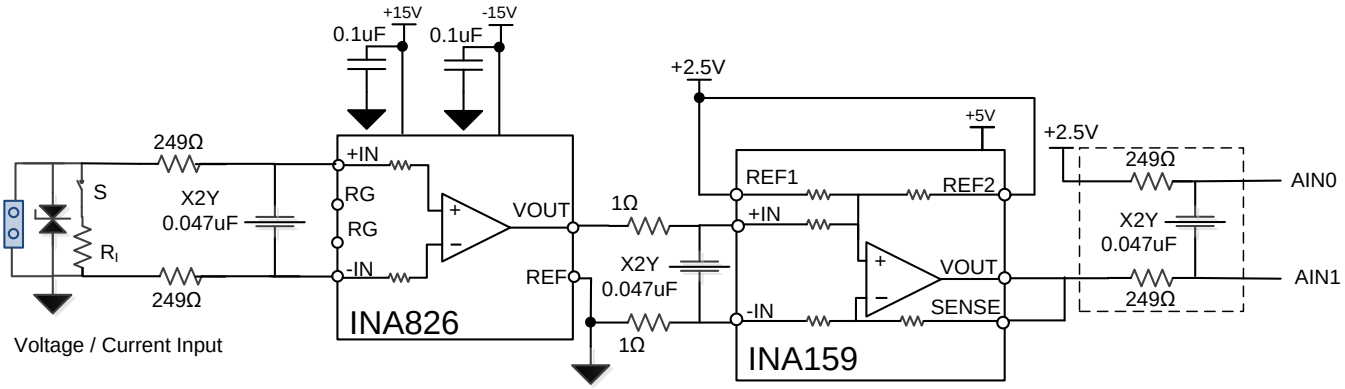

Figure 3: Industrial Input Circuit

$$Code_{OUTPUT} = Codes_{TOTAL}\left(\frac{0.2 \cdot V_{IN} \cdot GAIN}{2 \cdot V_{REF}}\right) = Codes_{TOTAL}\left(\frac{0.2 \cdot V_{TC} \cdot GAIN}{5\ V}\right) \quad (1)$$

2.2 Thermocouple Circuitry

A thermocouple is a temperature-measuring device consisting of two dissimilar conductors joined at their ends. Thermocouples are inexpensive, rugged and can measure a wide range of temperatures. They are self-powered and require no external form of excitation. The main limitation with thermocouples is accuracy. The thermocouple is based on the See beck effect; it produces a voltage when the temperature of measuring junction differs from the reference junction. The implication of this effect is that thermocouples do not actually measure an absolute temperature; they only measure the temperature difference between two points, commonly known as the hot and cold junctions. Therefore, in order to determine the temperature at hot junction, we also need to know the cold junction temperature which can be obtained by thermistor, as explained in the following section.

The ADS1248 includes internal circuitry to directly acquire the voltage from thermocouple sensors. The thermocouple is connected to the inputs of the ADC through a standard input filter. An internal bias voltage, V_{BIAS}, is used to bias the negative thermocouple connection to a mid-supply voltage. This shifts the small thermocouple output voltage to a range within the common-mode input range of the ADC. The external 2.5V reference is used for the ADC reference for thermocouple inputs.

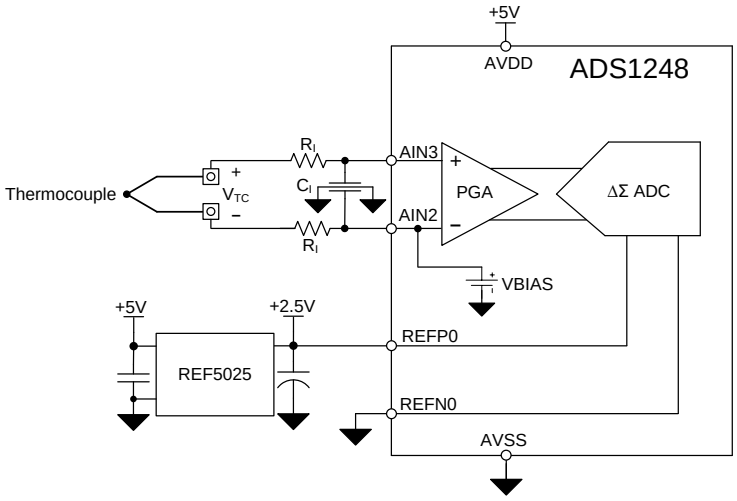

Figure 4: Thermocouple Input Circuitry

The resulting input voltage, reference voltage, and final output code transfer function for this circuit are shown in Equations (**2**) - (**4**).

$$V_{IN} = V_{AIN3} - V_{AIN2} = V_{TC} \quad (2)$$

$$V_{REF} = 2.5\,V \quad (3)$$

$$Code_{OUTPUT} = Codes_{TOTAL} \left(\frac{V_{IN} \cdot GAIN}{2 \cdot V_{REF}} \right) = Codes_{TOTAL} \left(\frac{V_{TC} \cdot GAIN}{5\,V} \right) \quad (4)$$

Because the thermocouple voltage is very small compared to the 2.5V reference voltage, the internal PGA gain stage is set to a high value to increase the signal at the ADC inputs.

2.3 Thermistor Circuitry

A thermistor is a silicon element whose resistance varies significantly with temperature. This design uses negative temperature coefficient (NTC) thermistors, meaning that the sensor resistance will decrease as the temperature increases. The non-linearity in the resistance versus temperature characteristic of thermistors limits their usable temperature range. Placing a resistor in parallel with the thermistor (R_P) helps reduce the non-linearity of the thermistor.

The thermistor resistance can be measured by passing a known current source through the thermistor while measuring the voltage. Figure 3 shows the ratiometric measurement configuration used for this design. In the configuration, the excitation current returns to ground through a low-side reference resistor, R_{REF}. The voltage potential developed across R_{REF}, V_{REF}, is fed into the positive and negative reference pins (REFP and REFN) of the ADC. V_{REF} serves three purposes in this design: it sets the input common-mode voltage (VCM), the differential ADC input range (typically $\pm V_{REF}$), and it is also used to convert the input voltage into digital output codes.

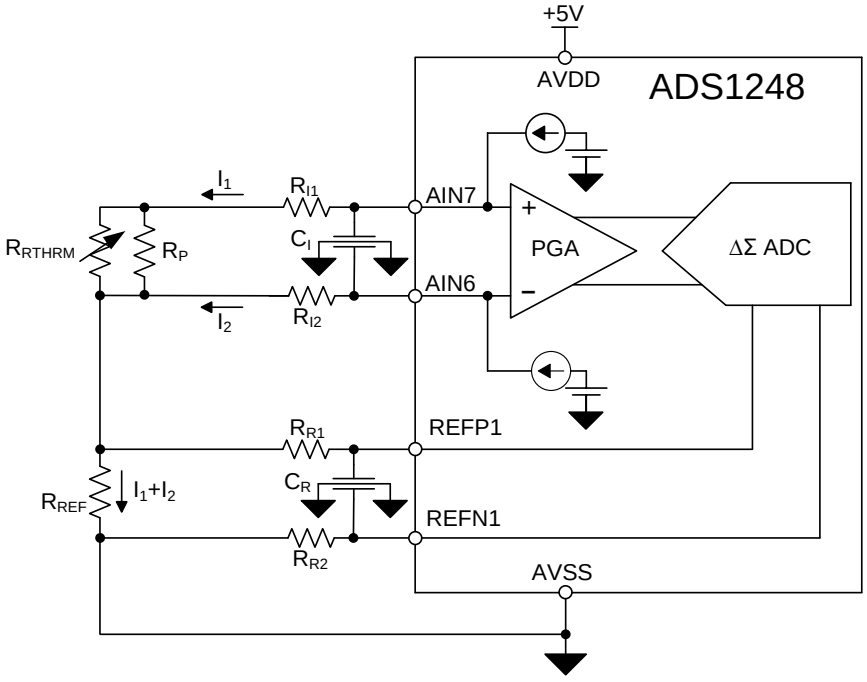

Figure 5: Thermistor Input Circuitry

The voltage drop across the thermistor and R_{REF} resistors produced by excitation source in the ratiometric configuration are shown as Equations below. Two precision current sources are used to cancel the differential filter resistances. Because the input voltage and reference voltage are produced by the same currents, the ADC output code simplifies to the ratio of the thermistor and R_{REF} resistances. This is shown in Equations (5) - (8). Consequently, inaccuracies due to magnitude, temperature drift, and noise of the current source cancel without affecting the final conversion result. This technique works best when the two current sources are well-matched, both in initial accuracy and temperature drift.

$$I_1 = I_2 = I \tag{5}$$

$$V_{DIFF} = V_{IN+} = I \times (R_{RTHD} // R_P) \tag{6}$$

$$V_{REF} = 2 \times I \times R_{REF} \tag{7}$$

$$Code_{OUTPUT} = Codes_{TOTAL} \left(\frac{V_{IN} \cdot GAIN}{2 \cdot V_{REF}} \right) = Code_{TOTAL} \left(\frac{(R_{RTHM} // R_P) \cdot Gain}{4 \times R_{REF}} \right) \tag{8}$$

2.4 RTD Circuitry

Resistive Temperature Detectors, RTDs, are temperature sensing elements that have a predictable resistance versus temperature. Therefore by measuring the resistance, the temperature can be calculated. For more information on RTD sensors please review References 1, 2, 3, and 4. Figure 6 displays the ratiometric 3-wire RTD circuit used in this design. Two precision current sources are typically used in 3-wire RTD applications to cancel the RTD lead resistances. The design and theory for this circuit are based on TIPD120: 3-Wire RTD Measurement System Reference Design, -200°C to 850°C. TIPD120 uses the ADS1247, the two-channel version of the ADS1248, so the circuit configuration and component values work well in this design.

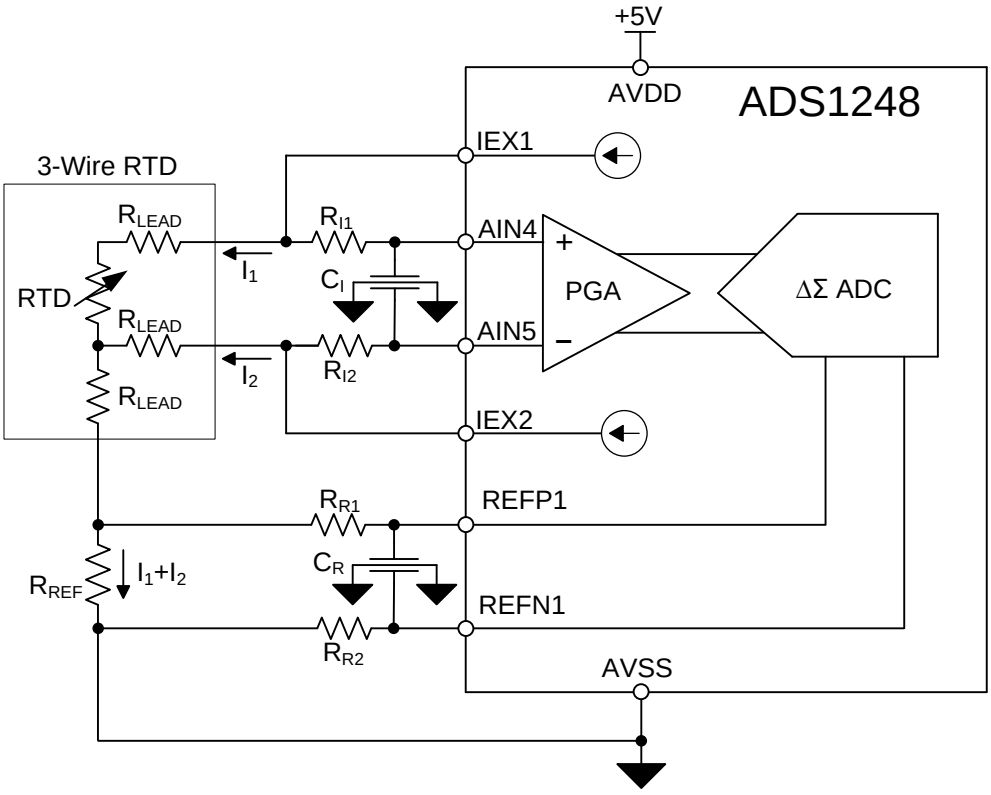

Figure 6: Ratiometric 3-Wire RTD Input Circuitry

The two dedicated current source outputs, IEXC1 and IEXC2, connect directly at the 3-Wire RTD connections. This prevents the current sources from flowing through the input filter which is used to reduce extrinsic noise.

The resulting input voltage, reference voltage, and final output code transfer function for this circuit are shown in Equations (**9**) - (**11**).

$$V_{IN} = V_{AIN4} - V_{AIN5} = I \times R_{RTD} \quad (9)$$

$$V_{REF} = 2 \times I \times R_{REF} \quad (10)$$

$$Code_{OUTPUT} = Codes_{TOTAL} \left(\frac{V_{IN} \cdot GAIN}{2 \cdot V_{REF}} \right) = Codes_{TOTAL} \left(\frac{R_{RTD} \cdot GAIN}{4 \times R_{REF}} \right) \quad (11)$$

Using differential and common-mode low-pass filters at the input and reference paths improves the cancellation of excitation and environmental noise. However, it is important to note that the corner frequency of the two differential filters must be well-matched as stated in Reference 2. The differential filter cutoff frequencies for the input and the reference voltage are shown in Equations (**12**) and (**13**) respectively.

$$f_{INPUT\_-3dB\_DIFF} = \frac{1}{2 \times \pi \times C_{I\_DIFF} \times (R_{I1} + R_{RTD} + R_{I2})} \quad (12)$$

$$f_{REF\_-3dB\_DIFF} = \frac{1}{2 \times \pi \times C_{R\_DIFF} \times (R_{R1} + R_{REF} + R_{R2})} \quad (13)$$

2.5 Digital Isolation

Most AI modules require isolation from the backplane and other AI modules. This is typically accomplished by isolating the digital signals between the host processor/controller and the ADC in the AI circuit. There are many topologies available to achieve the isolation but galvanic (capacitive) isolation has many advantages over other topologies and will be selected for this design.

3 Component Selection

3.1 ADC – ADS1248

As shown in Figure 2, ADS1248 is chosen for this application. This device not only has the resolution and accuracy needed to achieve the aforementioned design goals, but also features all the internal sub-circuits required to realize the design.

The ADS1248 is a 24-bit, delta-sigma (ΔΣ) ADC that offers a complete front-end solution for temperature detection applications. It comes from a product family of highly integrated precision data converters, featuring a low-noise programmable gain amplifier (PGA), a precision ΔΣ modulator, a digital filter, an internal oscillator, and two digitally controlled precision current sources (IDACs). It is a popular industry choice for precision temperature measurement applications.

3.2 Digital Isolator – ISO7641 and ISO7221

The four serial data signals required to communicate bi-directionally with the ADS1248 are serial communication signals SCLK, DIN, SDO, CS and start, DRDY. In order to maintain isolation from the host controller, these signals must be isolated through a digital isolator. The ISO7641 is chosen for the SPI communication with a 25Mbps digital isolator and ISO7221is chosen for the start control and DRDY with 5 Mbps signal rate. Both of them feature >4 kV galvanic isolation.

3.3 Industrial Voltage and Current Circuitry

Instrumentation amplifiers are the appropriate choice to buffer the analog input module due to their high input impedance. DC errors from the INA will directly contribute to the final accuracy, therefore an instrumentation amplifier with low offset voltage (V_{OS}), low V_{OS} drift ($V_{OS(DRIFT)}$), low gain error and gain nonlinearity, high common-mode rejection ratio (CMRR), and high power-supply rejection ratio (PSRR) will help keep the error contribution of the amplifier as low as possible. The INA826 was chosen because it achieves 240uV typical, V_{OS} and 2.4 uV/°C typical, $V_{OS(DRIFT)}$, +/-0.003% typical gain error and 1ppm typical gain nonlinearity. It also features a typical CMRR of 95 dB and a typical PSRR of 124dB. Wide input and output voltage ranges are also required in this application. INA826 has a wide supply range from 2.7V to 36V and rail- to -rail output stage which makes it suitable in this design.

The difference amplifier is added to attenuate the input signal into a proper input range of the ADC. The on-chip resistors are laser-trimmed for accurate gain and high common-mode rejection. For ADS1248, the input range is +/-V_{REF}/GAIN. For gain =1, the maximum input range is +/-2.5V. The maximum input voltage for this design is +/-10v, so a gain of 0.25 maximum is required. INA159 is a fixed gain of 0.2 with +/-100uV typical, V_{OS} and +/-0.002% typical, $V_{OS(DRIFT)}$, +/-0.005% typical gain error and +/-0.0002%FS typical gain nonlinearity which makes it an appropriate choice. It also features a typical CMRR of 96dB.

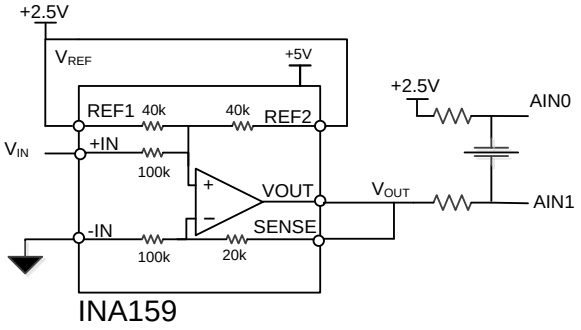

Figure 7: Detailed INA159 Circuitry

The transfer function for the INA159 circuit is shown in Equation 15. For +/-10V input, the output is from 0.5V to 4.5V.

$$V_{OUT} = V_{IN} * \left(\frac{20k}{100k}\right) + V_{REF} * \left(\frac{100k}{100k + 40k//40k}\right) * (1 + \frac{20k}{100k}) = 0.2V_{IN} + V_{REF} \quad (14)$$

The ADS1248 register configuration for industrial inputs is displayed in Table 2. The PGA gain can be set according to the input range by changing the contents of the SYS0 registers. The data rate was set to 40SPS.

Table 2: Register Settings for Industrial Voltage and Current Inputs

Register (Address)	Resister Values	Comment
MUX0 (00h)	0x08	Positive input channel AIN0, negative input channel AIN1
MUX1 (02h)	0x00	REF0 input pair selected as VREF
SYS0(03h)	0x03	Data rate=40SPS,PGA gain =1 (I_{IN}: +/-25 mA, V_{IN}: 0-10 V, +/-10 V)
	0x13	Data rate=40SPS,PGA gain =2 (I_{IN}: 0-20 mA, 4-20 mA, V_{IN}: 0-5 V, +/-5 V)

3.4 Thermocouple input

There are many types of thermocouples, each with its own unique characteristics. Selection of the combination is driven by cost, availability, convenience, melting point, chemical properties, stability, and output. Different types are best suited for different applications. They are usually selected on the basis of the temperature range and sensitivity needed. Type J, K, T, & E are “Base Metal” thermocouples, the most common types of thermocouples. Type R, S, and B thermocouples are “Noble Metal” thermocouples, which are used in high temperature applications. In this design, a Type J (iron – constantan) was selected for testing which has higher sensitivity of about 50 µV/°C.

Table 3 lists the register settings for the thermocouple input. Set the data rate at or below 20 SPS to reduce the influence of 50/60Hz noise on the small thermocouple input voltages.

Table 3: Register Settings for Thermocouple Inputs

Register (Address)	Resister Values	Comment
MUX0 (00h)	0x1A	Positive input channel AIN3, negative input channel AIN2
VBIAS(01h)	0x04	Bias voltage is applied on AIN2
MUX1 (02h)	0x00	REF0 input pair selected as VREF
SYS0(03h)	0x50	Data rate=5SPS,PGA gain =32 (Temperature>700°C)
	0x60	Data rate=5SPS,PGA gain =64 (Temperature<700°C)

3.5 Thermistor input

To meet the design goals for the cold junction temperature range of 0°C to 50°C, the NTCS0603E3222FMT thermistor has been chosen with resistance of 2.2k at 25°C, ± 1 % tolerance, and K of 3520. The datasheet specifies a resistance value of 886.05 Ω at 50°C and 6378.5 Ω at 0°C.

Shunting the thermistor with a resistor drastically improves the linearity across temperature. However the output voltage range is reduced as the shunt resistor is reduced in value. The best compromise between linearity and output voltage is achieved when the shunt resistor is equal to the thermistor resistance at the median temperature of the system. Therefore, choose R_P to be 2.2 kΩ in parallel with the thermistor. The parallel combination results in a measurement resistance range from 631.652 Ω to 1635.799 Ω and is equal to 1004.147 Ω at 25°C.

The excitation currents are set to 1 mA to maximize the thermistor sensor output while keeping the errors due to self-heating low.

The maximum allowable PGA gain setting is based on the reference voltage, the thermistor resistance change, and the excitation current as shown in Equations (**15**) through (**17**).

$$R_{RTHM@0C}//R_P = 6378.5//2200 = 1635.799\ \Omega \quad (15)$$

$$V_{IN\_MAX\_THRM} = R_{RTHM@0C}//R_P \times I_{IDAC} = 1635.799\ \Omega \times 1\ mA$$
$$V_{IN\_MAX\_THRM} = 1.6358V \quad (16)$$

$$Gain_{MAX} = \frac{V_{REF}}{V_{IN\_MAX}} \quad (17)$$

As shown in Figure 5, the excitation current sources must flow out the AIN6 and AIN7 pins and therefore through the input filter before reaching the thermistor. Therefore, the input resistors will be set to 249 Ω to keep the voltage drop across them less than 0.25 V. This will prevent the voltage drop across them from interfering with the input common-mode limitations or the IDAC compliance.

For the IDACs to remain operational, the inputs of the ADS1248 must satisfy the IDAC compliance voltage of 0.7V as specified in the product datasheet. Therefore the maximum voltages that can occur at the AIN6 and AIN7 inputs is calculated in Equation (**18**).

The voltage at AIN6 is equal to the sum of V_{REF}, V_{IN_MAX} and the voltage drop across the input filter as shown in Equation (19). This voltage must remain less than the compliance voltage of 4.3V. The maximum reference voltage can therefore be calculated as shown in Equation (**19**).

$$AIN6_{MAX} \le AVDD - 0.7\ V = 4.3\ V$$
$$AIN7_{MAX} \le AVDD - 0.7\ V = 4.3\ V \quad (18)$$

$$V_{REF\_MAX} = AIN6_{MAX} - V_{IN\_MAX} - I * R_{filter} = 4.3V - 1.636V - 249\Omega * 0.001A = 2.415\ V \quad (19)$$

Combining Equations **(17)**and **(19)**, the gain set to 1V/V. Choosing V_{REF} close to $V_{IN\_MAX\_THRM}$ will improve the circuit performance and measurement resolution. Equations **(16)** and **(19)** define the allowable range for the V_{REF} voltage as displayed in Equation **(20)**.

$$1.6358V \le V_{REF} \le 2.415\ V \quad (20)$$

V_{REF} will be selected in Section 3.6 to fulfill both the thermistor and RTD input circuitry requirements.

Table 4 displays the register settings when configured for thermistor inputs.

Table 4: Register Settings for Thermistor Inputs

Register (Address)	Resister Values	Comment
MUX0 (00h)	0x3E	Positive input channel AIN7, negative input channel AIN6
MUX1 (02h)	0x28	REF1 input pair selected as VREF
SYS0(03H)	0x02	PGA gain=1; data rate=20sps
IDAC0(0Ah)	0x06	IDAC=1000uA
IDAC1(0Bh)	0x76	Current source connect to AIN7 and AIN6

3.6 RTD Input Circuitry Selection

The RTD excitation current will first be set to 1 mA to limit the self-heating errors of the RTD to an acceptable level. This results in a maximum input voltage of 390.48 mV as shown in Equations (**21**) and (**22**).

$$R_{RTD@850^{\circ}C} = 390.48\ \Omega \quad (21)$$

$$V_{IN\_MAX\_RTD} = R_{RTD@850^{\circ}C} \times I_{IDAC} = 390.48\Omega \times 1\ mA$$

$$V_{IN\_MAX\_RTD} = 390.48\ mV \quad (22)$$

The PGA gain setting should be selected such that the full-scale range of the RTD input is close to the full-scale input of the thermistor input, Equation (**16**) design to optimize the reference voltage for both circuits. Table 5 lists the resulting full-scale ADC input voltages, V_{IN_FS}, for several PGA gain settings.

Table 5: Full Scale ADC Voltages vs. PGA Gain Settings with RTD Input

PGA Gain	$V_{IN\_MAX\_RTD}$
1	0.39048
2	0.78096
4	1.56192
8	3.12304
16	6.24768

The PGA gain will be set to 4V/V so $V_{IN\_MAX\_RTD}$ is close to $V_{IN\_MAX\_THRM}$. This will allow both circuits to achieve good resolution while sharing a common V_{REF} voltage.

The RTD input must also satisfy the IDAC compliance voltage as shown in Equation (**23**).

$$AIN0 = V_{REF} + V_{IN\_MAX} = V_{REF} + 1.56192V < 4.3V \quad (23)$$

V_{REF} will be set to 1.64V to maximize the resolution for both circuits while using a standard value resistor of 820Ω The value of R_{REF} it is selected based on the IDAC setting and the desired V_{REF} voltage, as shown in Equation (**24**).

$$R_{REF} = \frac{V_{REF}}{2 \times I_{IDAC}} \quad (24)$$

An 820 Ω R_{REF} resistor was chosen based on the results of Equation (**24**). Since the voltage across the R_{REF} sets the reference voltage for the ADC, the tolerance and temperature drift of R_{REF} directly affect the measurement gain error. Therefore, a resistor with 0.02% maximum tolerance was selected.

Table 5 displayed the configuration for the thermocouple input.

Table 5. Register Settings for RTD input

Register (Address)	Resister Values	Comment
MUX0 (00h)	0x25	Positive input channel AIN4, negative input channel AIN5
MUX1 (02h)	0x28	REF1 input pair selected as VREF
SYS0(03h)	0x22	PGA gain=4; data rate=20sps
IDAC0(0Ah)	0x06	IDAC=1000uA
IDAC1(0Bh)	0x89	Current source connect to IEXT1 and IEXT2

4 Circuit Performance Calculations

4.1 Industrial Voltage and Current Inputs

The PLC input circuit performance is based on the specifications of INA826, INA159 and ADS1248.

Due to the high differential impedance of 20G Ω of the INA826, the offset caused by the input bias current flowing through the filter resistor is negligible. INL, offset voltage, gain error and CMRR of the INA826 at room temperature are displayed in Table 6. The gain for INA826 is 1, V_{OSI} (Input stage offset voltage) and V_{OSO}(output stage offset voltage) can be added together directly and get the final V_{OS} as 240uV.

Table 6: Calculated Performance of the INA826

	Typ	**Voltage (ppm)** (+/-10 V)	**Current (ppm)** (+/-25mA)
Offset (mV)	0.24	12	19
CMRR(db)	95	9	9
INL (ppm)	1	1	1
Gain error (%FSR)	+/-0.003	30	30
TUE		37	41
Calibrated Error		1	1

The error analysis method is the same for both voltage input and current input. Take +/-10V voltage as an example, the offset, INL, and gain error can be transformed into ppm directly. The offset error caused by CMRR can be calculated as Equation (**25**).

$$V_{CMRR} = 10V * \frac{1}{10^{95/20}} = 0.177mv \quad (25)$$

$$V_{CMRR}(FS) = 0.177mV/20V * 10^3 = 9ppm$$

Total error caused by INA826 can be calculated using Equation (**26**).The error in ppm for the current input can be calculated similarly.

$$V_{INA826} = \sqrt{12^2 + 9^2 + 1^2 + 30^2} = 34ppm \quad (26)$$

The INA159 errors include offset voltage, gain error and gain nonlinearity. As shown in Equation (**14**), the V_{REF} voltage will also affect the final output of the INA159 and will be included as well. These errors are listed in Table 7.

The input filter resistor of INA159 is 1 Ω, compare to 10k input resistor of the INA159, it will also cause gain errors.

$$V_{Filter\_ERROR} = \frac{1}{1+10k} * 10^6 = 100ppm \quad (27)$$

V_{REF} initial error will cause offset, the offset voltage is 1.25mV with 0.05% maximum error.

$$V_{REF\_ERROR} = 2.5V * 0.05\% = 1.25mV \quad (28)$$

Table 7: Calculated Performance of INA159

		Typ	**Voltage (ppm)** (+/-10 V)	**Current (ppm)** (+/-25mA)
Filter	**Gain error**	NA	100	100
V_{REF}	**Offset (mV)**	1.25	62.5	88
INA159	**Offset (mV)**	0.1	5	8
	CMRR(db)	96	8	8
	INL (%FSR)	+/-0.0002	2	2
	Gain error (%FSR)	+/-0.005	50	50
TUE			128	143
Calibrated Error			2	2

The total error is calculated in using the same root sum of squares method used in Equation (**26**).

The main ADS1248 error contributors are the offset voltage, gain error and gain nonlinearity. They are listed in Table 8. The total error in voltage mode caused by ADS1248 can be calculated as Equation (**29**).

Table 8: Calculated Performance of ADS1248

		Typ	**Voltage (ppm)** (+/-10 V)	**Current (ppm)** (+/-25mA)
ADS1248	**Offset (mV)**	0.015	3.75	6
	INL (ppm)	6	7.5	12
	Gain error (%FSR)	+/-0.005	50	50
V_{REF}	**Gain error**	0.05%	500.25	500.25
R_{shunt}	**Gain error**	0.1%	0	1000

TUE			503	1119

$$V_{ADS1248} = \sqrt{(0.75)^2 + (7.5)^2 + (50)^2} = 50.6ppm \quad (29)$$

The tolerance of the REF5025 will produce gain errors in the ADC transfer function as shown in Equation (**30**).

$$V_{REF\,Tol} = 0.05\%$$

$$\text{Gain Error}V_{REF} = \frac{\pm V_{REF\,Tol}}{1 \pm V_{REF\,Tol}} \times 100 = \frac{\pm 0.05\%}{1 \pm 0.05\%} \times 100 = 500.25\text{ppm} \quad (30)$$

In current mode, the shunt resistor is a 0.1% precision resistor which will also introduce gain error.

The INL is typically specified in either number of ADC codes or in ppm FSR. Because INL is not a gain error, it must be multiplied by the full-scale input voltage of the ADC rather than V_{IN_MAX}, as shown in Equation (**31**). In the +/-10 V Voltage mode, V_{IN_MAX} range is 4V.

$$\text{INL Error}_{ADC}(V) = \frac{\text{INL}}{1{,}000{,}000} \times \frac{2 \times V_{REF}}{\text{Gain}} = \frac{6\ \text{ppm}}{1{,}000{,}000} \times \frac{2 \times 2.5V}{1\ \frac{V}{V}} = 30\ \mu V$$

$$\text{INL Error}_{ADC}(\text{ppm}) = \frac{30\ \mu V}{4V} = 7.5\text{ppm} \quad (31)$$

Since the INA826, INA159 and ADS1248 errors are uncorrelated, a probable total TUE of the industrial input range of +/-10V output can be calculated by taking the root of the sum of squares (RSS) of their individual errors, as shown in Equation (**32**).

$$V_{TUE\_PLC} = \sqrt{V_{INA826}{}^2 + V_{INA159}{}^2 + V_{ADS1248}{}^2} = \sqrt{37^2 + 128^2 + 503^2} = 520\text{ppm} \quad (32)$$

Multiply V_{TUE_PLC} by the full-scale input range to calculate the total error in volts. For +/-10V output range, the output error voltage is 10.38mV as calculated in Equation (**33**).

$$V_{error\_PLC} = V_{FS} * V_{TUE\_PLC} = 20V * 520\text{ppm} = 10.38\text{mV} \quad (33)$$

The total current error caused by INA826, INA159, ADS1248, reference voltage and shunt resistor tolerance in current mode is calculated as Equation (**34**).

$$I_{TUE\_PLC} = \sqrt{I_{INA826}{}^2 + I_{INA159}{}^2 + I_{ADS1248}{}^2} = \sqrt{41^2 + 143^2 + 1119^2} = 1129 \text{ ppm} \quad (34)$$

Total error is as calculated in Equation (**35**) and output current error is roughly 54uA.

$$I_{error\_PLC} = I_{FS} * 1129\text{ppm} = 50\text{mA} * 1129\text{ppm} = 54.19\mu\text{A} \quad (35)$$

The errors for the different input ranges can be calculated using the same methods.

4.2 Thermocouple Input performance

The errors of the ADS1248 affect the final thermocouple accuracy. In the configuration, the filter resistor won't contribute any significant errors due to high input impedance of ADS1248. Again, the offset voltage, gain error and gain nonlinearity will cause errors as shown in Table 9. For the K-type thermocouple, the FS is 77.648mV which ranges from -8.095mV to 69.553mV when the temperature changes from -200°C to 1200°C.

Table 9. Calculated Circuit Performance of ADS1248

	Voltage (FS=77.648mV)	**Typ**	**Calculated (FS ppm)**
ADS1248	**Offset (mV)**	0.015	193
	INL (LSB)	6	63
	Gain error (%FSR)	+/-0.02	200
V_{REF}	**Gain error**	0.05%	500.25
	TUE		576
	Calibrated Error		63

Offset FS error is 193 ppm as calculated in Equation (**36**).

$$V_{OS\_ppm} = \frac{15\ \mu V}{77.648\text{mV}} * 10^6 = 193\text{ppm} \quad (36)$$

Total error caused by ADS1248 and reference voltage can be calculated as Equation (**37**).

$$V_{TUE\_thermocouple} = \sqrt{V_{offset}{}^2 + V_{INL}{}^2 + V_{gain\ error}{}^2 + \text{GainerrorV}_{REF}{}^2} = \sqrt{(193)^2 + (63)^2 + (200)^2 + (500.25)^2} = 576\text{ppm} \quad (37)$$

Total voltage error can be calculated by multiplying the full-scale range as shown in Equations (**38**) and . The voltage error can be translated to temperature error using the thermocouple sensitivity as shown in Equation (**41**).

$$V_{errror\_thermocouple} = V_{FS} * V_{TUE\_thermocouple} = 77.648mV * 576ppm = 44.7\mu V \quad (38)$$

$$V_{errror\_thermocouple\_CAL} = V_{FS} * V_{TUE\_thermocouple} = 77.648mV * 63ppm = 4.89\mu V \quad (39)$$

$$T_{error\_thermocouple} = \frac{44.7\mu V}{50\mu V/^{\circ}C} = 0.89^{\circ}C \quad (40)$$

$$T_{error\_thermocouple\_CAL} = \frac{4.89\mu V}{50\mu V/^{\circ}C} = 0.0978^{\circ}C \quad (41)$$

4.3 Thermistor Input performance

The temperature error in the thermistor circuit, it not only caused by offset voltage ,INL, gain error of ADS1248, but also the current source mismatch, current mismatch drift, and the resistors R_p , R_{f1}, R_{f2} tolerant errors. Current source initial error and temperature drift won't affect the performance due to the ratiometric measurement. The full ADC output code is calculated in Equation (**42**), and the ideal code output is simplified as Equation (**43**). The full-scale code span code can be calculated using Equation (**44**).

$$Code_{OUTPUT} = Code_{TOTAL} \frac{I_1 * (R_{RTHM} // R_P + R_{f1}) - I_2 * (R_{f2})}{(I_1 + I_2) \times R_{REF}} \quad (42)$$

$$Code_{ideal} = Code_{TOTAL} \frac{R_{RTHM} // R_P}{2 \times R_{REF}} \quad (43)$$

$$Code_{FS} = Code_{TOTAL} \frac{(R_{RTHM@0} // R_P) - (R_{RTHM@50} // R_P)}{2 \times R_{REF}} \quad (44)$$

Resistor tolerance errors in R_p,R_{f1},R_{f2} introduce errors as shown in Appendix B.1.

The full-scale code value is derived in Equation (**45**).

$$Code_{FS} = Code_{TOTAL} \frac{(R_{RTHM@0} // R_P) - (R_{RTHM@50} // R_P)}{2 \times R_{REF}} \quad (45)$$

The tolerance of R_{REF} will produce gain errors in the ADC transfer function. Assuming the tolerance is specified as a percentage, the transfer function gain error from the R_{REF} tolerance can be calculated from Equations 50.

$$R_{REF\,Tol} = 0.02\%$$

$$\text{Gain Error}_{R_{REF}\ Tol}(\%) = \frac{\pm R_{REF\,Tol}}{1 \pm R_{REF\,Tol}} \times 100 = \frac{\pm 0.02\%}{1 \pm 0.02\%} \times 100 = 0.020004\% \quad (46)$$

Errors introduced by current mismatch /mismatch drift and resistors tolerances are listed in Table 10 at 0°C, 25°C and 50°C. Compared to them, the gain error, INL and offset of ADS1248 can be ignored.

Table 9: Calculated Performance of the Thermistor Input Circuitry

Temperature	Mismatch error	R_p tolerance error	R_{f1} tolerance error	R_{f2} tolerance error	R_{REF} tolerance error	Total error
0°C	0.159%	0.080%	0.0249%	0.0249%	0.0200%	0.183%
25°C	0.119%	0.036%	0.0249%	0.0249%	0.0200%	0.131%
50°C	0.084%	0.0096%	0.0249%	0.0249%	0.0200%	0.094%

4.4 RTD Input performance

The temperature error in the 3-wire RTD circuit is not only caused by offset voltage ,INL, gain error of ADS1248, but also the current source mismatch, current mismatch drift. Similar to the thermistor circuit, Current source initial error and temperature drift won't affect the performance due to the ratiometric measurement. The ideal ADC output code is derived in Equations (**47**) and (**48**).

$$\text{Code}_{OUTPUT} = \text{Code}_{TOTAL}\ \frac{I_1 * R_{RTD}}{2 \cdot (I_1 + I_2) \times R_{REF}} \quad (47)$$

$$\text{Code}_{ideal} = \text{Code}_{TOTAL}\ \frac{R_{RTD}}{2 \times R_{REF}} \quad (48)$$

The gain error introduced by current mismatch is shown in Equation (**49**).

$$\text{GainError}_{I_1 mis} = \frac{\text{Code}_{TOTAL}\ \frac{I(1+mis) * R_{RTD}}{I(2+mis) \times R_{REF}} - \text{Code}_{ideal}}{\text{Code}_{ideal}} = \frac{mis}{(2+mis)}$$

OR (49)

$$\text{GainError}_{I_2 mis} = \frac{\text{Code}_{TOTAL}\ \frac{I * R_{RTD}}{I(2+mis) \times R_{REF}} - \text{Code}_{ideal}}{\text{Code}_{ideal}} = \frac{-mis}{(2+mis)}$$

The INL has to be multiplied by the full-scale input voltage of the ADC rather than V_{IN_MAX}, as shown in Equation (**50**).

$$\text{INL Error}_{ADC}(V) = \frac{\text{INL}}{1{,}000{,}000} \times \frac{2 \times V_{REF}}{\text{Gain}} = \frac{6 \text{ ppm}}{1{,}000{,}000} \times \frac{2 \times 1.64 \text{ V}}{4 \frac{\text{V}}{\text{V}}} = 4.92 \text{ µV} \quad (50)$$

$$\text{INL Error}_{ADC}(\text{ppm}) = \frac{4.92 \text{ µV}}{390.48 \text{ mV}} = 12.6\text{ppm}$$

Table 11 lists the errors caused by the current mismatch, mismatch drift, gain error, INL and offset of ADS1248. Applying a two-point calibration removes the effects of the offset and gain errors, leaving only the INL error.

Table 10: Calculated Circuit Performance of 3-Wire RTD Input Circuitry

		Typ	Calculated(FS)(ppm)
3-wire RTD	**Offset (mV)**	0.015	38
	INL (LSB)	6	12.6
	Gain error (%FSR)	+/-0.005	50
	R_{REF} tolerance error(%FSR)	+/-0.02	200
	Current Mismatch(ppmFSR)	0.15%	749
	TUE(ppm FSR)		778
	Calibrated Error (ppm FSR)		12.6

The magnitude of the IDAC source can be used to convert the calculated voltage error into a calculated resistance error as shown in Equations (**51**) and (**52**).

$$\text{Error } (\Omega) = \frac{\text{Error } (V)}{I_{IDAC}} = \frac{390.48\text{mV} * 778\text{ppm}}{1\text{mA}} = 0.304\Omega \quad (51)$$

$$\text{Error}_{CAL}(\Omega) = \frac{\text{Error } (V)}{I_{IDAC}} = \frac{390.48\text{mV} * 12.6\text{ppm}}{1\text{mA}} = 0.00492\Omega \quad (52)$$

The temperature accuracy can be calculated by dividing the resistance accuracy by the RTD sensitivity (α). The results in Equations (**53**) and (**54**) display the temperature error in degrees Celsius using the α value for 0°C.

$$\text{Error } (°C) = \frac{\text{Error } (\Omega)}{\alpha_{@0°C}} = \frac{0.304\Omega}{0.39083 \frac{\Omega}{°C}} = 0.78°C \quad (53)$$

$$\text{Error } (°C) = \frac{\text{Error } (\Omega)}{\alpha_{@0°C}} = \frac{0.00492\Omega}{0.39083 \frac{\Omega}{°C}} = 0.0125°C \quad (54)$$

5 PCB Design

The PCB schematic and bill of materials can be found in Appendix A.1.

5.1 PCB Layout

For optimal performance of this design follow standard precision PCB layout guidelines, including proper decoupling very close to all mixed signal integrated circuits and providing adequate power and GND connections with large copper pours. The layout for the design is shown in Figure 8.

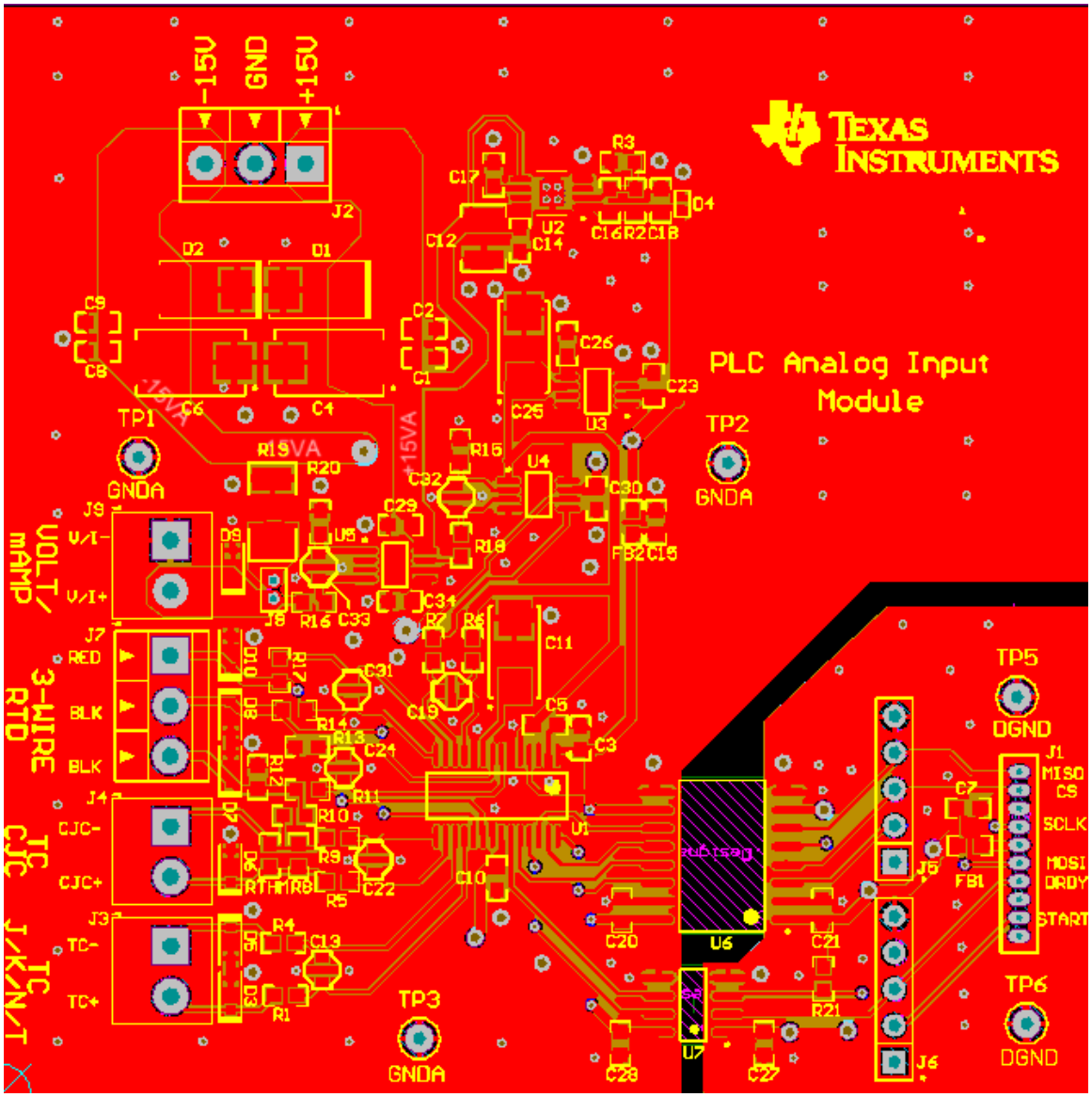

Figure 8: Altium PCB Layout

6 Verification and Measured Performance

6.1 V_{IN} Circuit

DC transfer function data for the PLC V_{IN} circuit in +/- 10 V modes was collected by converting the ADC digital code into voltage. The measurement results and error are shown in Figure 9 and Figure 10.

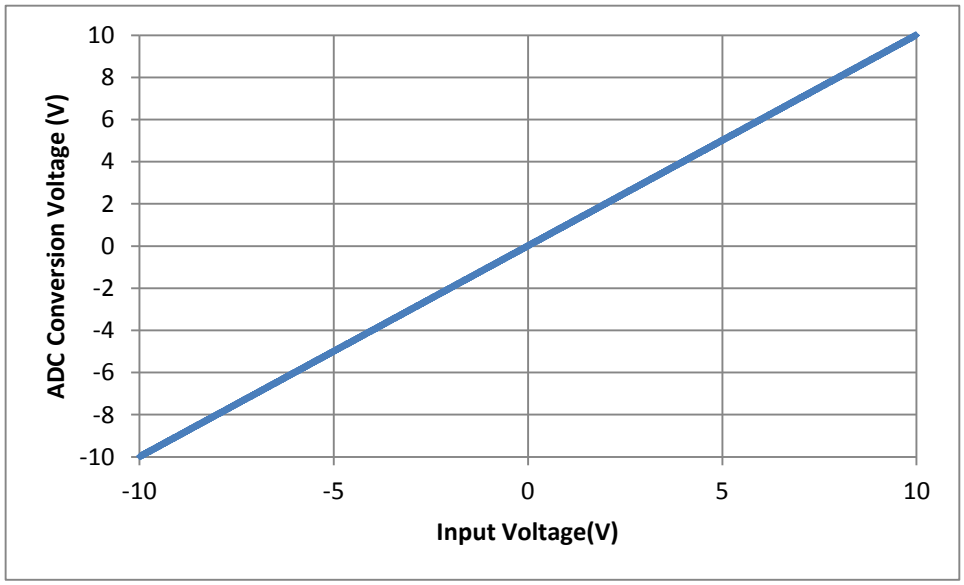

Figure 9: Measured Industrial Voltage Input Transfer Function

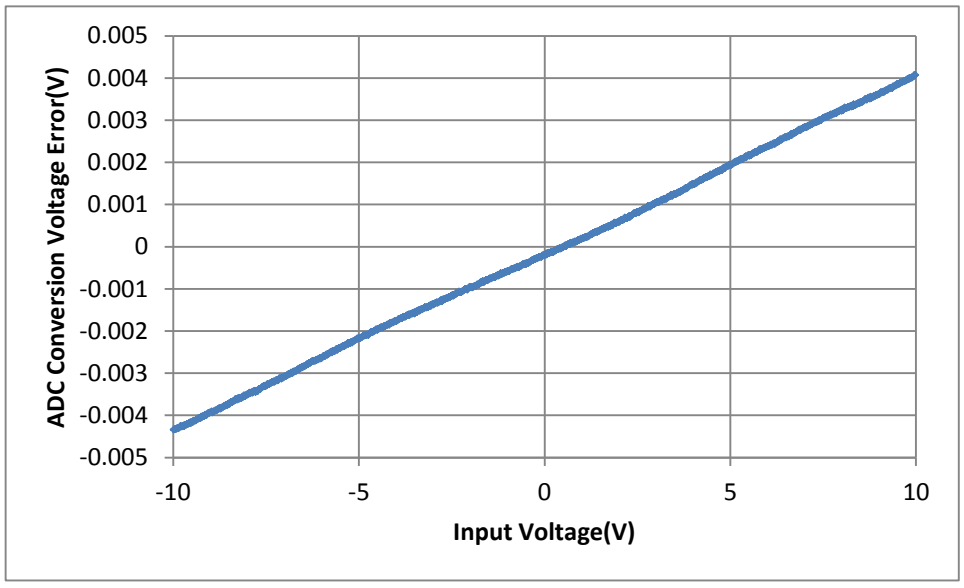

Figure 10: Measured Industrial Voltage Input Error

The results after at two-point gain and offset calibration are shown in Figure 11.

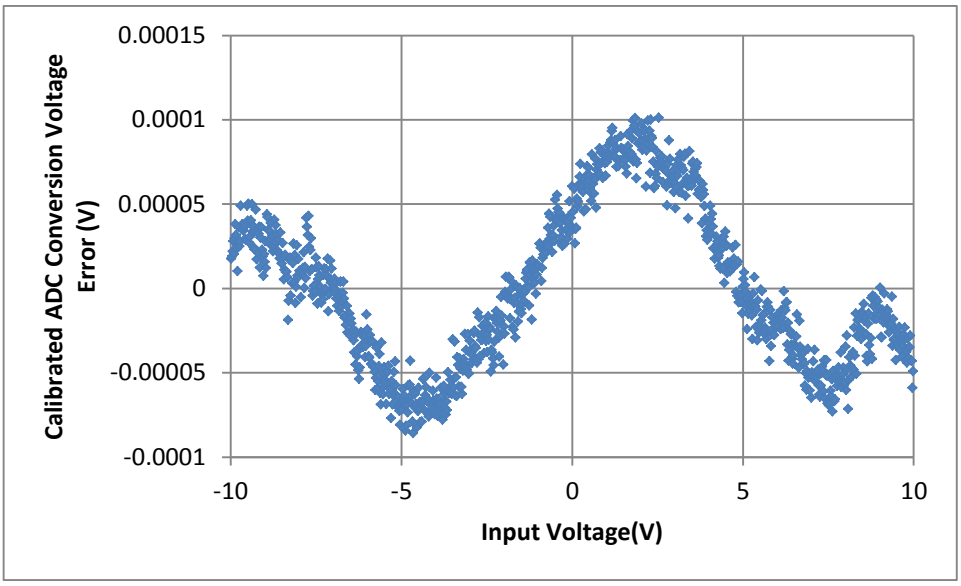

Figure 11: Measured Calibrated Industrial Voltage Input Error

6.2 I_{IN} Circuit

DC transfer function data for the PLC I_{IN} circuit in +/- 25mA modes was collected by converting the ADC digital code into current. The measurement results and error are shown in Figure 12 and Figure 13.

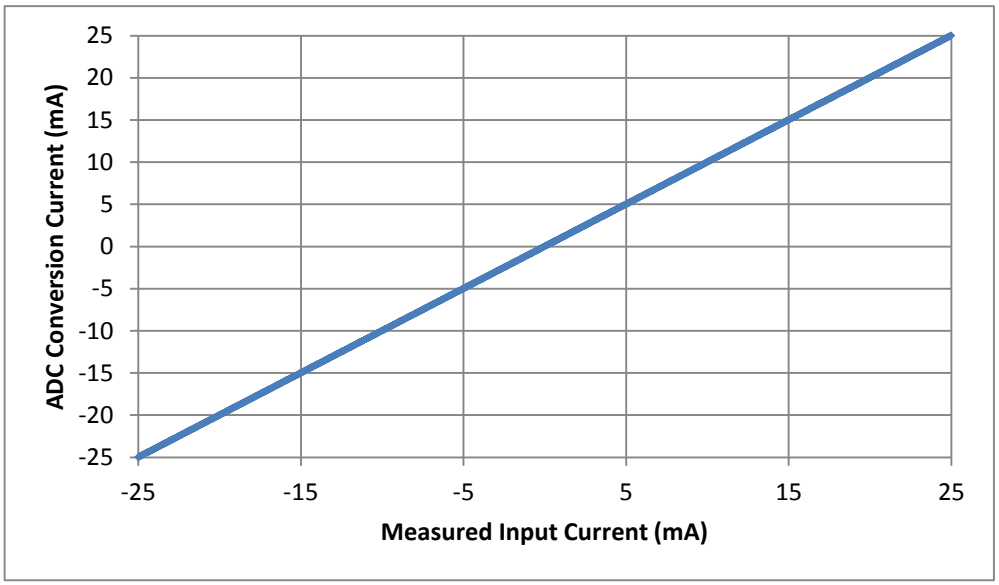

Figure 12: Measured Industrial Current Input Transfer Function

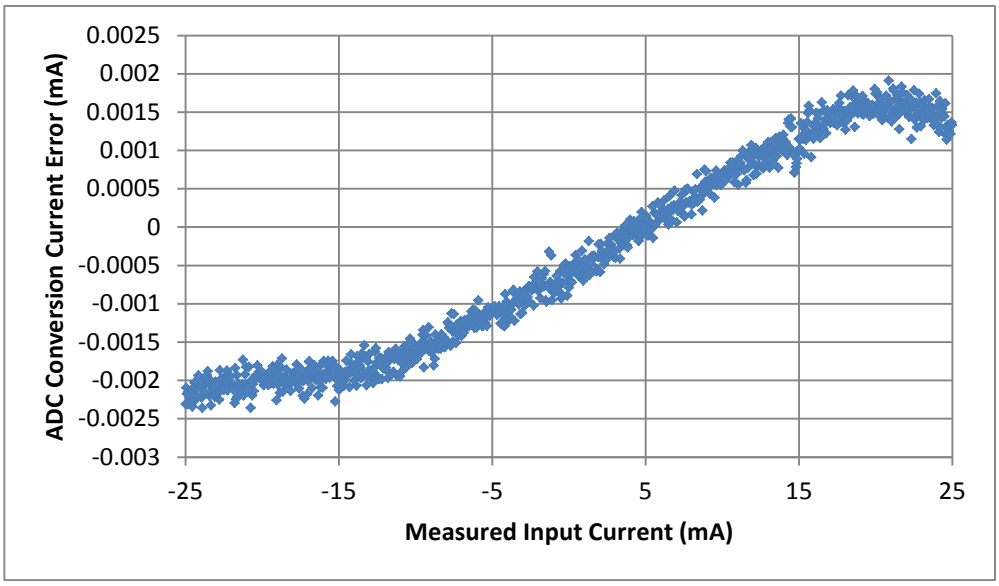

Figure 13: Measured Industrial Measured Input Error

The results after a two-point offset and gain calibration are shown in Figure 14.

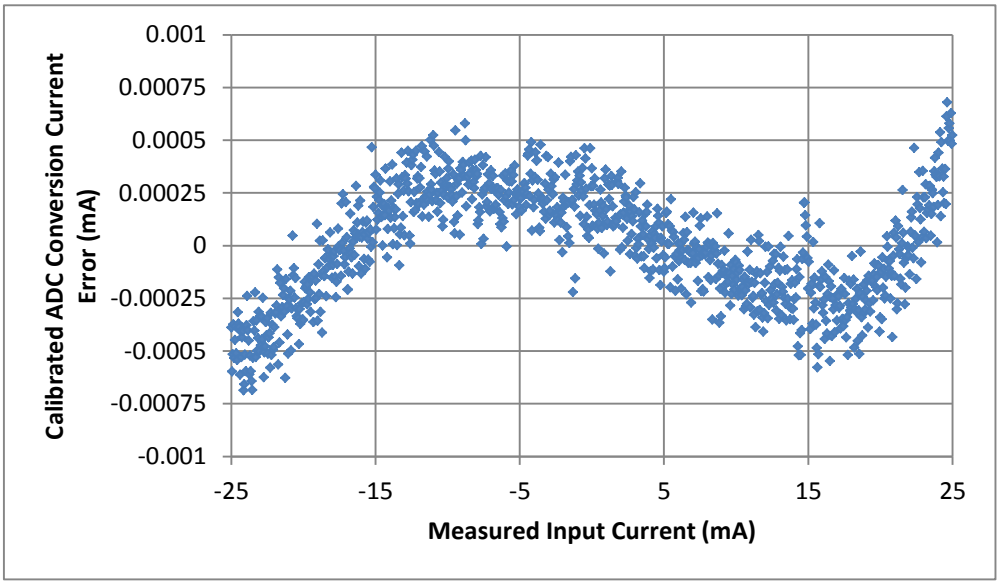

Figure 14: Calibrated Industrial Current Input Error

6.3 Thermocouple with Thermistor cold junction compensation

Thermocouple and thermistor performance are tested individually at first.

Simulating the thermocouple voltage using Keithley and it can be read back accurately by 8 ½ voltmeter. Measured result can be got by converting the ADS1248 digital code to voltage. Inverse Polynomials provide the temperature from the known thermocouple voltage (translate error by Inverse Polynomials is limited to 0.05°C which can be ignored). Figure 12, 13 show the measured voltage and error actual from ADS1298 with voltage generated by Keithley. Figure 14, 15 show the measured temperature and temperature error and temperature error using Inverse Polynomials. After calibration, the voltage error is less than +/-2.5uV and temperature error is less than +/-0.1° C.

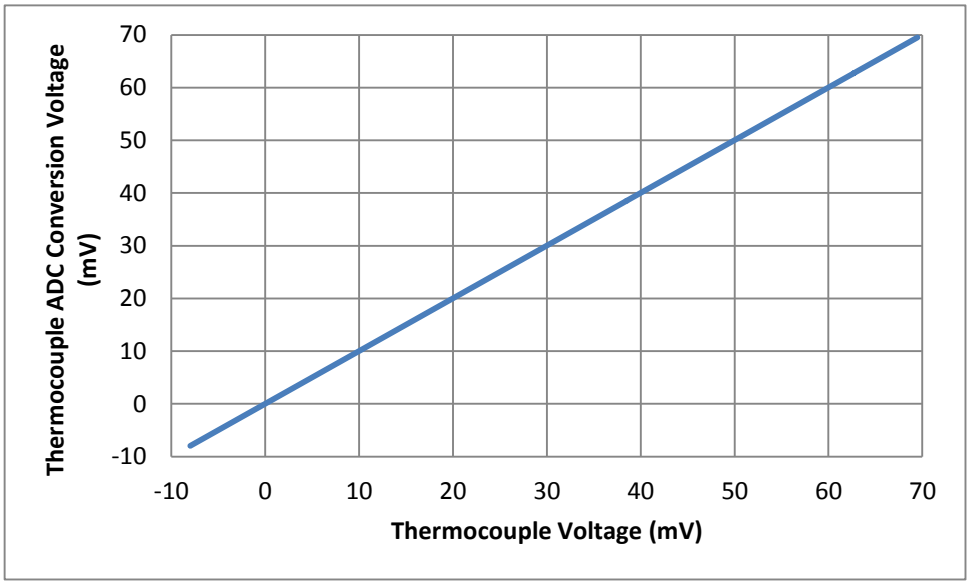

Figure 15: Measured Thermocouple Input Circuitry Transfer Function

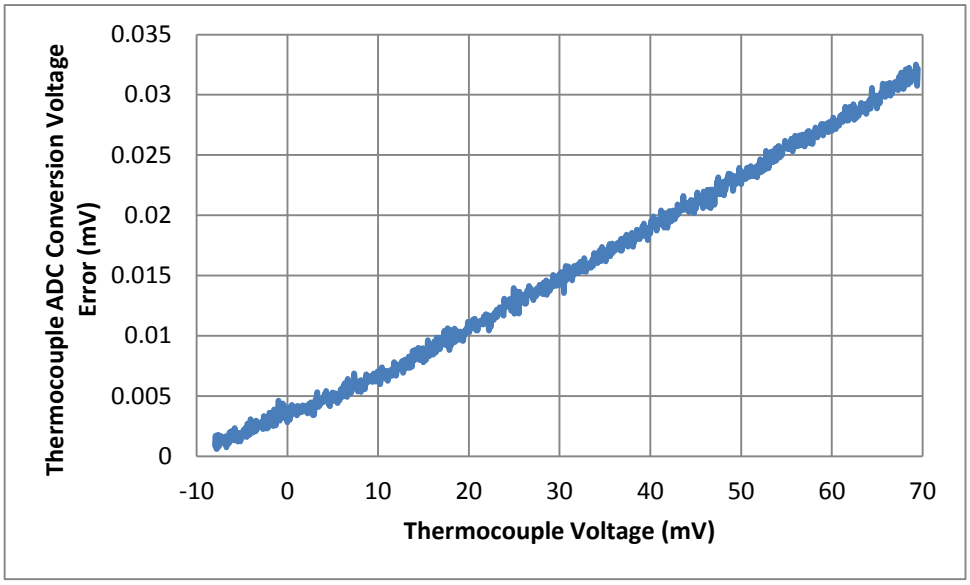

Figure 16: Measured Thermocouple Voltage Error

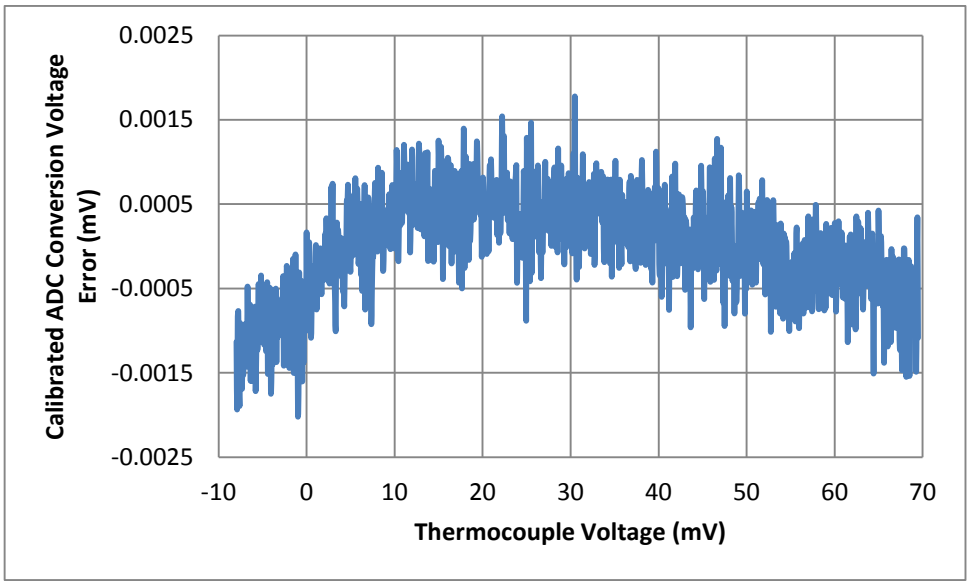

Figure 17: Calibrated Thermocouple Voltage Error

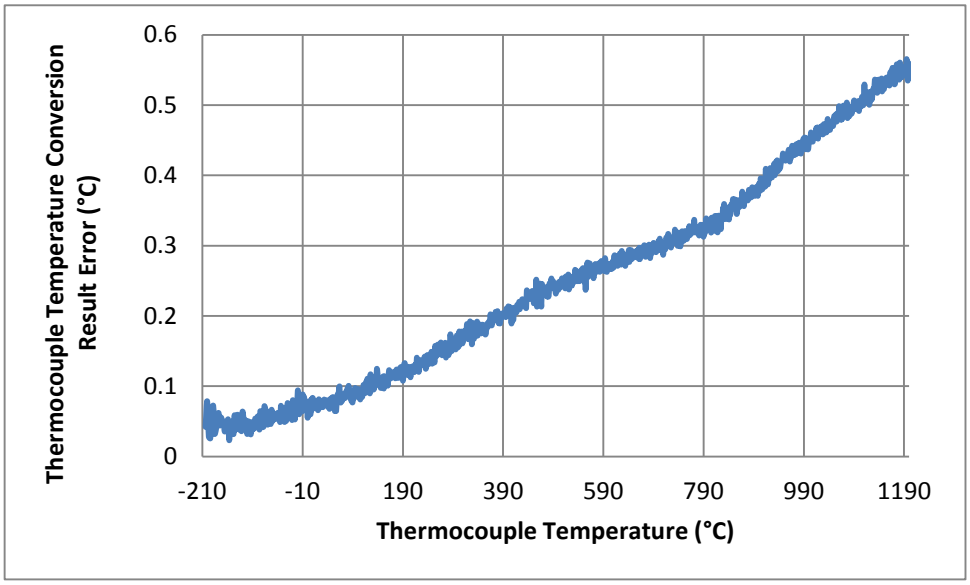

Figure 18: Measured Thermocouple Temperature Error

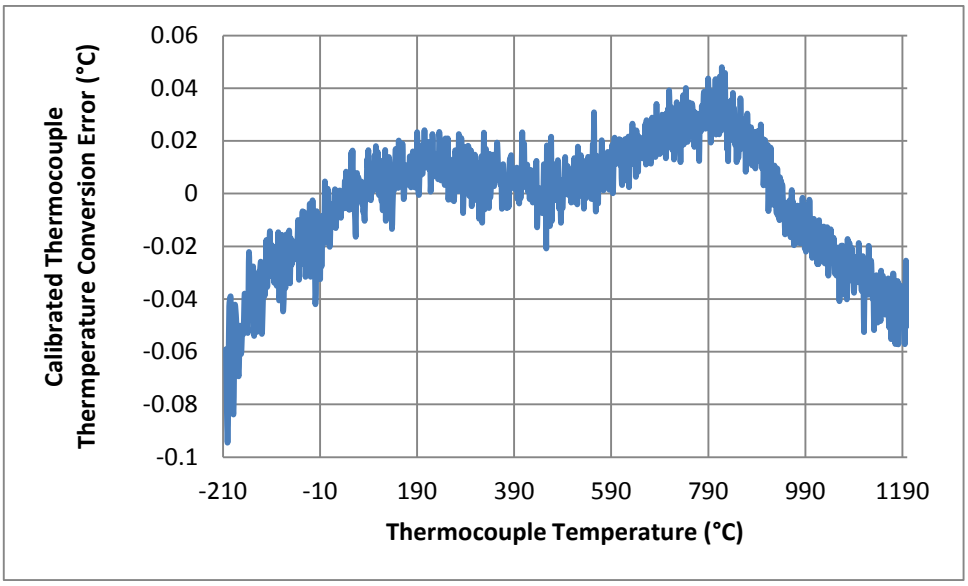

Figure 19: Calibrated Thermocouple Temperature Error

Similarly, measuring the thermistor performance by converting the ADS1248 code into resistor value based on equation 8. At the same time, using 8 ½ voltmeter to read back the actual thermistor value. In this way, the measured resistance and resistance error can be measured as shown is figure 17, 18. Steinhart–Hart equation can be used to convert the thermistor resistance into temperature. The measured temperature and temperature error are shown in figure 19, 20.

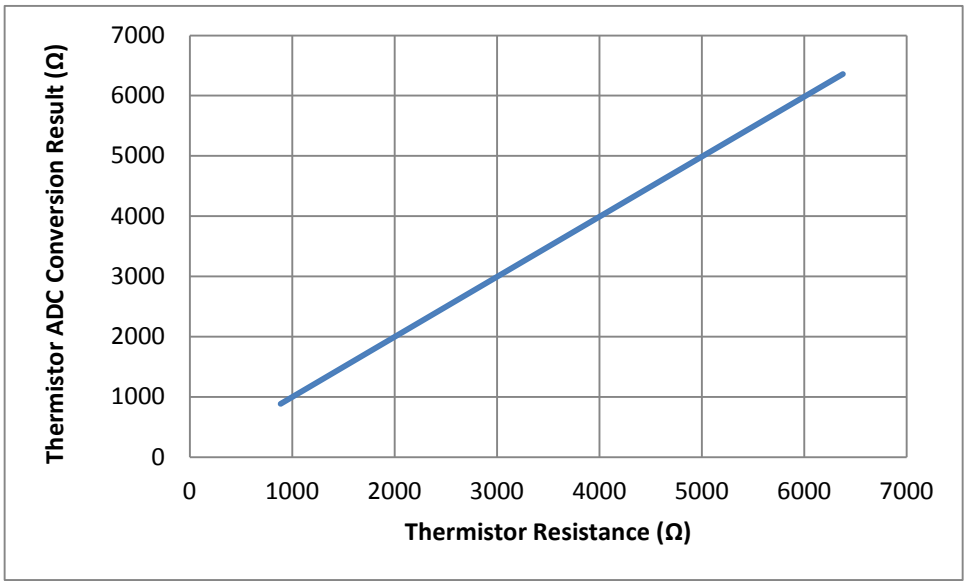

Figure 20: Measured Thermistor Input Transfer Function

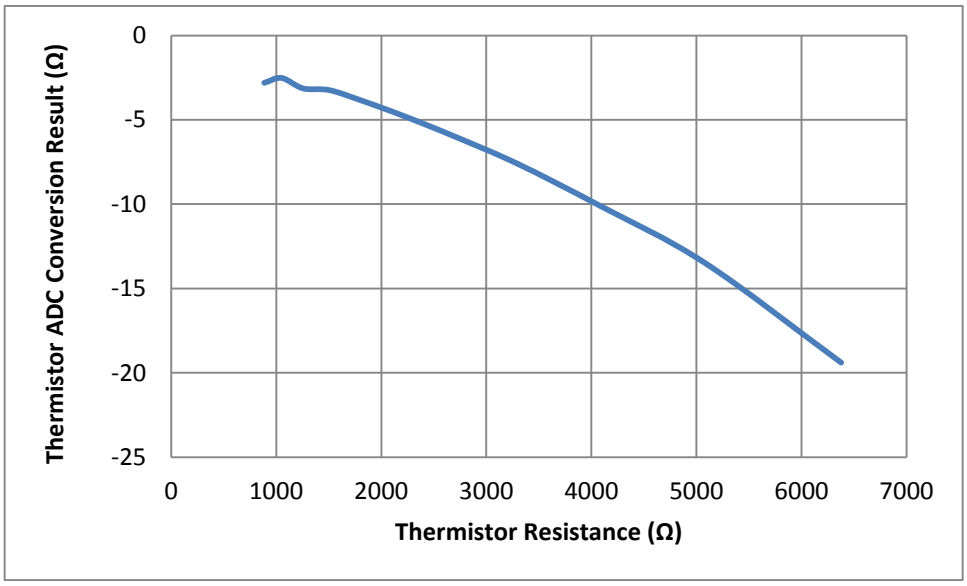

Figure 21: Measured Thermistor Input Circuitry Error

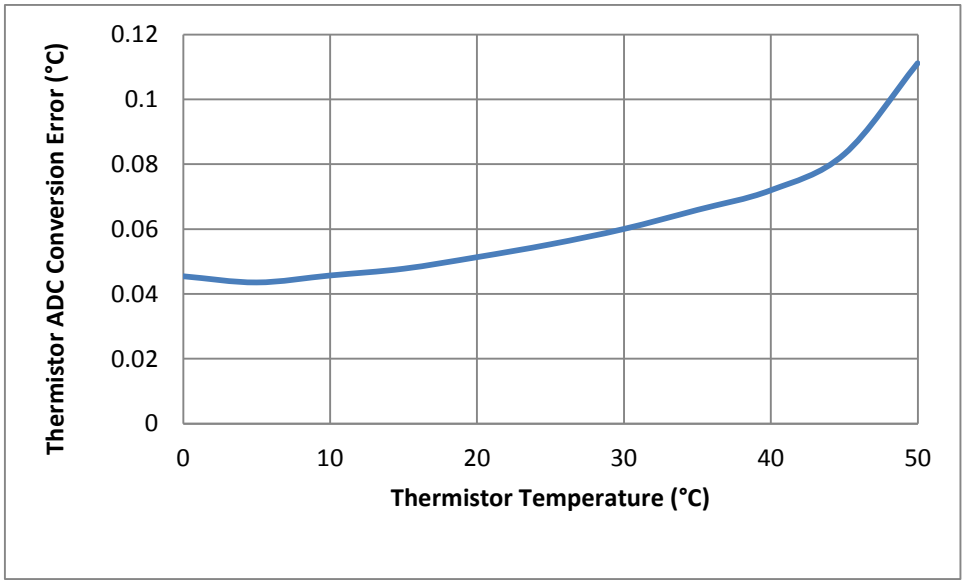

Figure 22: Measured Thermistor Input Circuitry Temperature Error

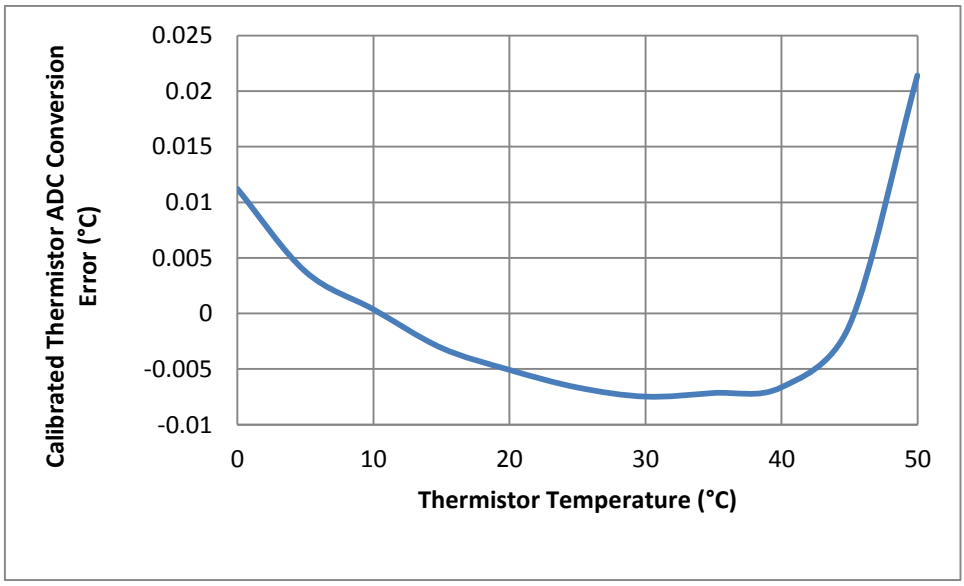

Figure 23: Calibrated Thermistor Input Temperature Error

The calculation procedure to achieve cold junction compensation is simple as shown in figure 21. Interleave readings between the thermocouple inputs and the thermistor input. If the cold junction is in a very stable environment, more periodic cold junction measurements may be sufficient. The thermistor voltage should be converted into the CJC temperature according to the Steinhart–Hart equation. Then, the cold junction temperature need to convert to a voltage that is proportional to the thermocouple currently being used, to yield V_{CJC}. This process can be accomplished by performing a reverse lookup table used for the thermocouple voltage-to- temperature conversion or using high-order polynomial. Adding the two voltages then yields the thermocouple-compensated voltage V_{Actual}, where $V_{CJC} + V_{TC} = V_{Actual}$. V_{Actual} is then converted to temperature using the same method before, and yields T_{Actual} .

The performance of thermocouple with cold junction compensation is shown is figure 22.

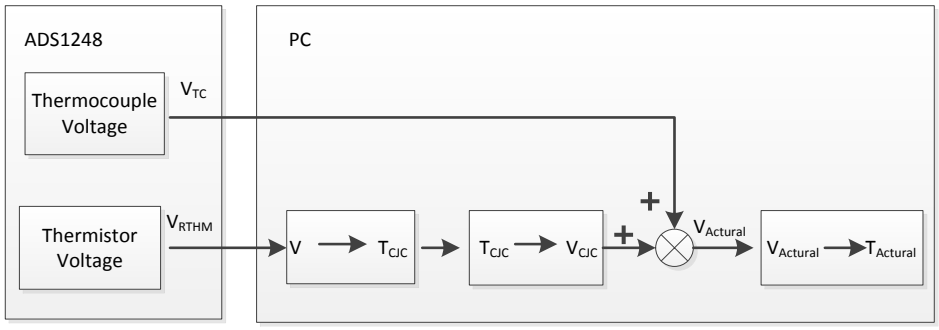

Figure 24: Software Flow Block Diagram

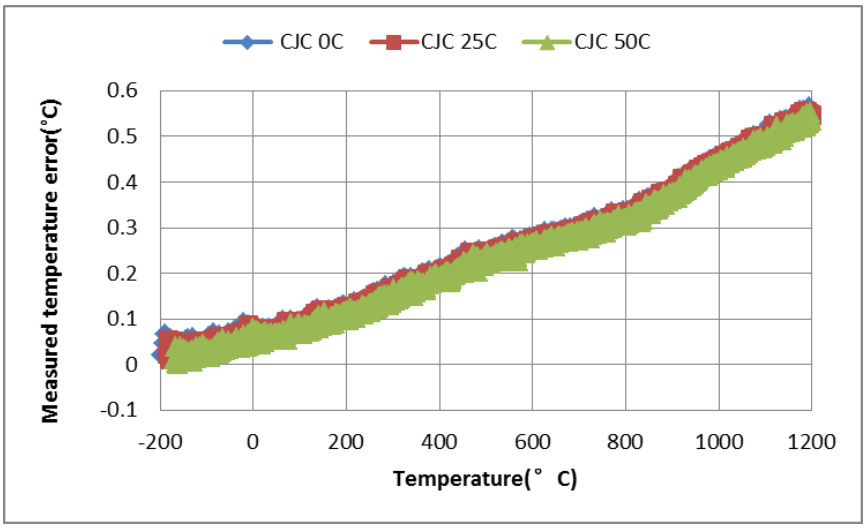

Figure 25: Thermocouple Temperature Error with CJC

6.4 RTD circuit

To test the accuracy of the acquisition circuit, a series of calibrated high-precision discrete resistors were used as the input to the system. Figure 26 and Figure 27display the unadjusted resistance measurement accuracy of the system over an input span from 20 Ω to 400 Ω, which represents a -200 – 850 C temperature range. The offset error can be attributed to the offset of the ADC, while the gain error can be attributed to the accuracy of the R_{REF} resistor and the ADC.

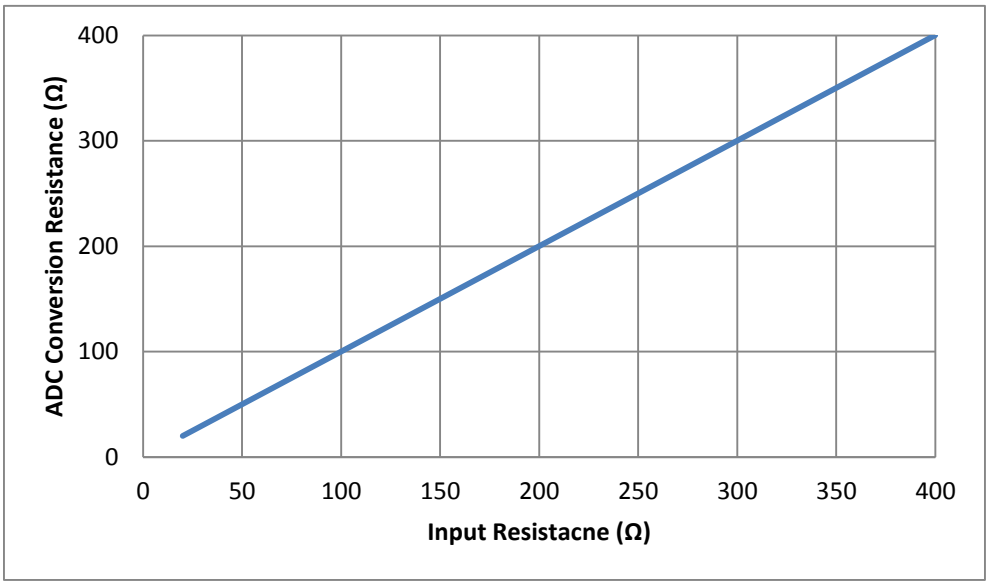

Figure 26: Measured Resistance Results with Precision Resistors

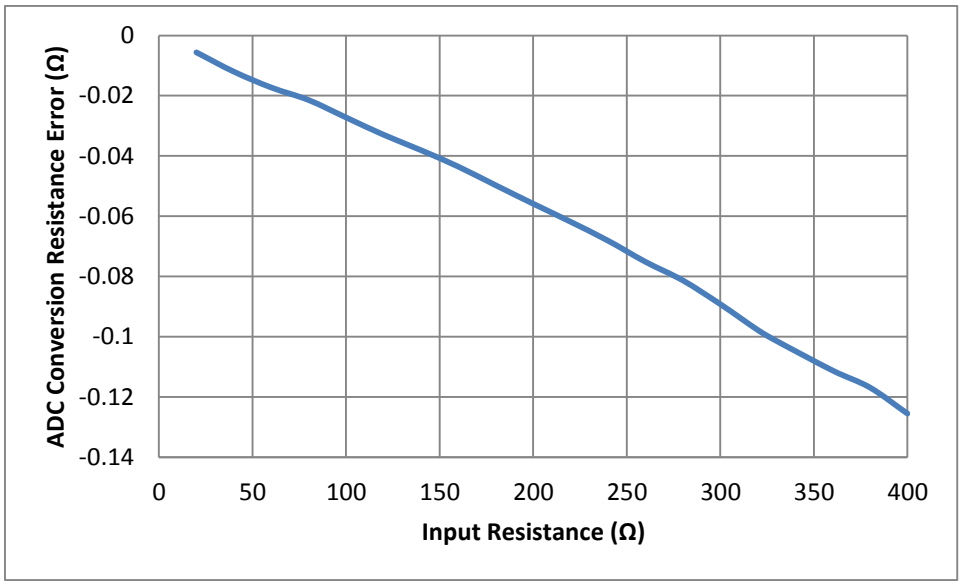

Figure 27: Measured Resistance Error with Precision Resistor Input

Precision temperature measurement applications are typically calibrated to remove the effects of gain and offset errors, which generally dominate the total system error. The simplest calibration method is a linear, or two-point, calibration which applies an equal and opposite gain and offset term to cancel the measured system gain and offset errors. Applying a gain and offset calibration yields the calibrated results shown in Figure 28.

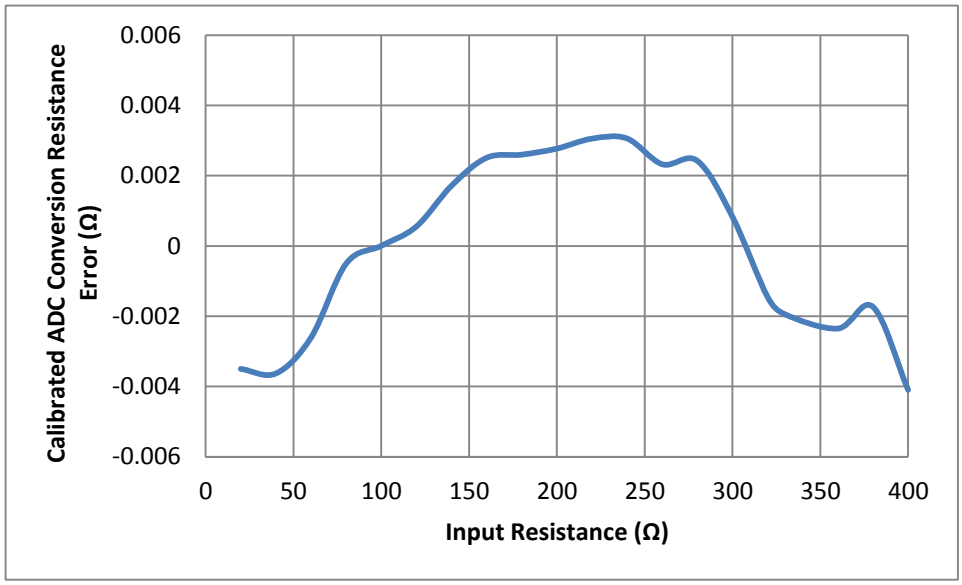

Figure 28: Calibrated RTD Input Circuitry Error

The results in Figure 28 can be converted to temperature accuracy by dividing the results by the RTD sensitivity (α) at the measured resistance. Figure 29 displays the calculated temperature accuracy of the circuit, not including any linearization related errors of the RTD.

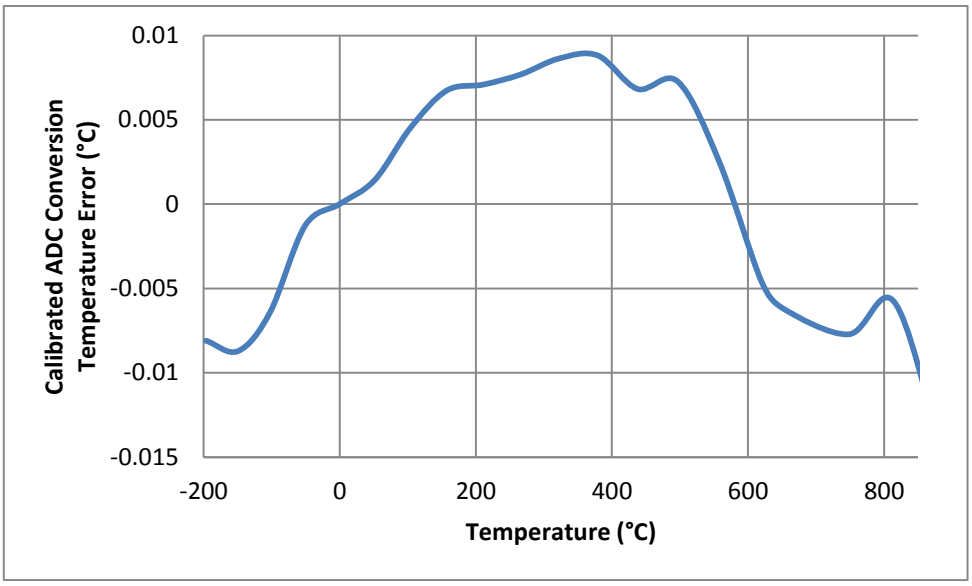

Figure 29: Calibrated RTD Input Circuitry Temperature Error

7 Modifications

For the temperature detecting, there are a few other fully integrated products available from TI that offer the same required building blocks as the ADS1248 but feature different performance, channel count, and cost. Several of these devices are listed in Table 11.

Table 11: Alternate Fully Integrated ADC Solutions

ADC	Resolution	Differential Inputs	PGA Range	IDACs Magnitude	Noise	Power Consumption
ADS1147(1)	16	2	1 – 128 V/V	50 µA – 1.5 mA	15.63 μV_{RMS}	1.4 mW
ADS1247(1)	24	2	1 – 128 V/V	50 µA – 1.5 mA	1.07 μV_{RMS}	1.4 mW
ADS1148(1)	16	4	1 – 128 V/V	50 µA – 1.5 mA	15.63 μV_{RMS}	1.4 mW
ADS1120(1)	16	2	1 – 128 V/V	10 µA – 1.5 mA	15.63 μV_{RMS}	1.4 mW
ADS1220(1)	24	2	1 – 128 V/V	10 µA – 1.5 mA	1.15 μV_{RMS}	1.4 mW
LMP90100(2)	24	4	1 – 128 V/V	100 µA – 1 mA	4.29 μV_{RMS}	5.1 mW

(1) AVDD = 3.3 V, AVSS = 0 V, Internal Reference = 2.048 V, Data Rate = 20 SPS, PGA = 4 V/V

(2) AVDD = 3 V, AVSS = 0 V, Internal Reference = 3 V, Data Rate = 13.42 SPS, PGA = 4 V/V

Any 36 V instrumentation amplifiers with unity gain stable can be used as the buffer amplifier in the PLC input module. However, as mentioned in Section 3.23, dc errors from the offset voltage (V_{OS}), V_{OS} drift ($V_{OS(DRIFT)}$), gain error and gain nonlinearity, CMRR, and PSRR affecting the V_{OUT} performance. Therefore, selecting an instrumentation amplifier with low offset voltage, low offset drift, high CMRR, and high PSRR will prevent the amplifier from reducing the performance of the ADC. Table 12 lists several optional instrumentation amplifiers that will work well in this application.

Table 12: Alternate Instrumentation Amplifiers

Amplifier	Typical Offset Voltage (µV)	Typical Offset Drift (µV/°C)	CMRR (dB)	PSRR (µV/V)	Gain error (gain=1)	Nonlinearity error	Quiescent Current (mA)
INA121	400	4	86	25	0.01%	0.0002%	0.45
INA118	60	2.2	90	11	0.01%	0.0003%	0.35
INA111	600	12	90	12	0.01%	0.0005%	3.3

INA114	30	0.6	96	2.5	0.01%	0.0001%	2.2

8 About the Authors

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9 Acknowledgements & References

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2. *Luis Chioye, “RTD Ratiometric Measurement and Filtering Using the ADS1148 and ADS1248 Family of Devices” SBAA201, March 2013.*
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4. *Omega ®, “The Omega ® Temperature Measurement Handbook™ and Encyclopedia, Vol MMXIV™, 7th Edition.*
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6.

Appendix A.

A.1 Electrical Schematic

The schematic for this design can be seen in Figure 30.

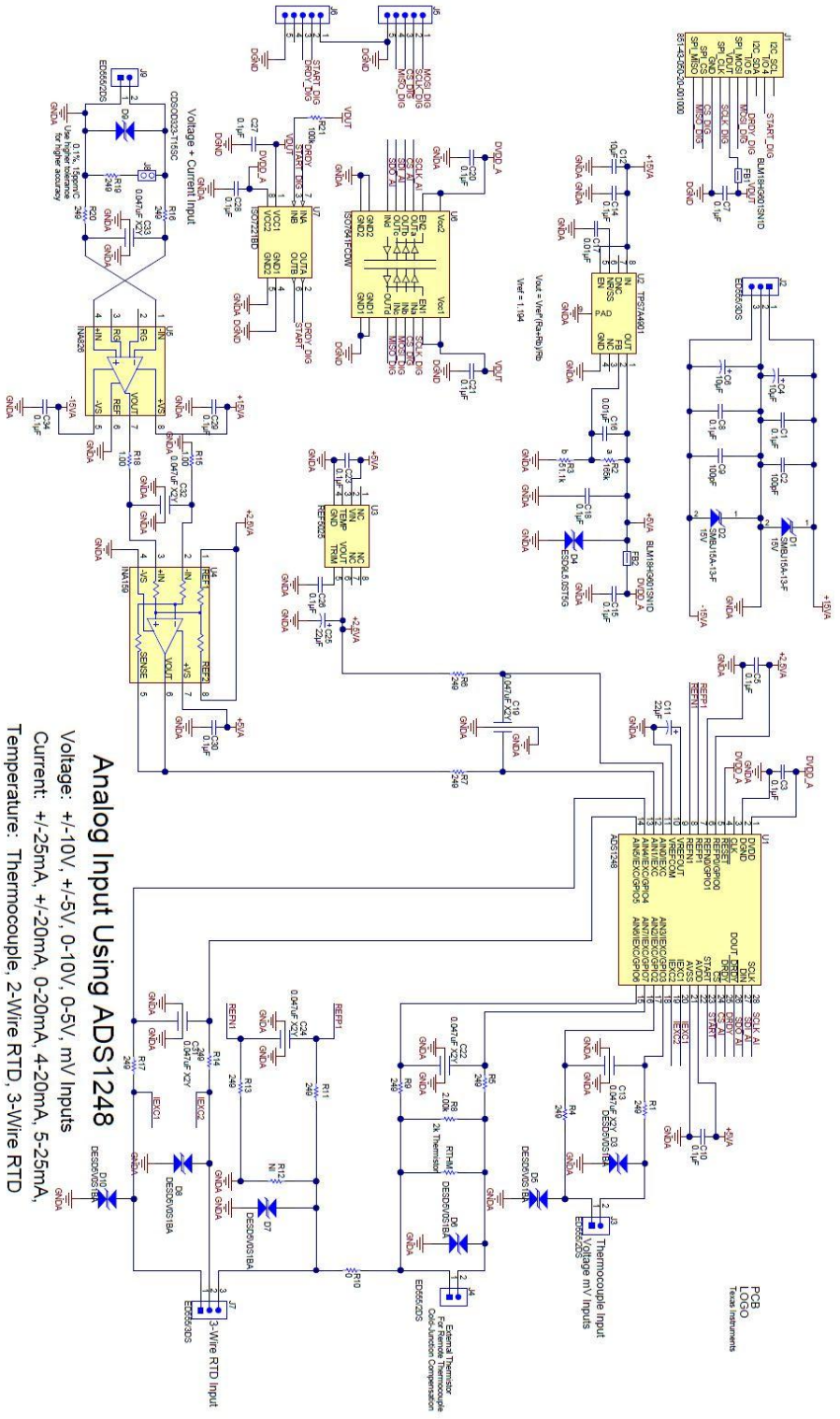

Figure 30: Altium Schematic

A.2 Bill of Materials

The bill of materials for this circuit can be seen in Figure 31.

Item #	Quantity	Designator	Value	Description	Manufacturer	Part Number
1	18	C1, C3, C5, C7, C8, C10, C14, C15, C18, C20, C21, C23, C26, C27, C28, C29, C30, C34	0.1uF	CAP, CERM, 0.1uF, 50V, +/-10%, X7R, 0603	MuRata	GRM188R71H104KA93D
2	2	C2, C9	100pF	CAP, CERM, 100pF, 50V, +/-5%, C0G/NP0, 0603	AVX	06035A101JAT2A
3	2	C4, C6	10uF	CAP, TANT, 10uF, 50V, +/-10%, 0.8 ohm, 7343-43 SMD	Vishay-Sprague	293D106X9050E2TE3
4	2	C11, C25	22uF	CAP, TANT, 22uF, 10V, +/-10%, 1.5 ohm, 6032-28 SMD	Vishay-Sprague	293D226X9010C2TE3
5	1	C12	10uF	CAP, CERM, 10uF, 25V, +/-20%, X7R, 1210	TDK	C3225X7R1E106M
6	7	C13, C19, C22, C24, C31, C32, C33	0.047uF	CAP CER 0.047UF 16V 20% X7R 0603	Johanson Dielectrics Inc	160X14W473MV4T
7	2	C16, C17	0.01uF	CAP, CERM, 0.01uF, 50V, +/-5%, X7R, 0603	Kemet	C0603C103J5RACTU
8	2	D1, D2	15V	Diode, TVS, Uni, 15V, 600W, SMB	Diodes Inc.	SMBJ15A-13-F
9	6	D3, D5, D6, D7, D8, D10		DIODE TVS 5.0V 130W	Diodes.inc	DESD5V0S1BA
10	1	D4		TVS ESD PROT ULT LOW CAP SOD-923	ON Semiconductor	ESD9L5.0ST5G
11	1	D9		DIODE TVS ARRAY 15V SOD323	Bourns	CDSOD323-T15SC
12	2	FB1, FB2		FERRITE CHIP 600 OHM 200MA 0603	MuRata	BLM18HG601SN1D
13	1	J1		CONN SOCKET 50PIN .050 R/A SNGL	Mill-Max Manufacturing Corp.	851-43-050-20-001000
14	2	J2, J7		Terminal Block, 6A, 3.5mm Pitch, 3-Pos, TH	On-Shore Technology	ED555/3DS
15	3	J3, J4, J9		Terminal Block, 6A, 3.5mm Pitch, 2-Pos, TH	On-Shore Technology	ED555/2DS
16	2	J5, J6		Header, TH, 100mil, 5x1, Gold plated, 230 mil above insulat	Samtec, Inc.	TSW-105-07-G-S
17	1	J8		CONN HEADER 2POS .050 T/H GOLD"	Samtec	TMS-102-02-G-S
18	10	R1, R4, R6, R7, R11, R13, R14, R16, R17, R20	249	RES, 249 ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW0603249RFKEA
19	1	R2	165k	RES 165K OHM 1/10W .1% 0603 SMD	Panasonic Electronic Components	ERA-3AEB1653V
20	1	R3	51.1k	RES, 51.1k ohm, 0.1%, 0.1W, 0603	Susumu Co Ltd	RG1608P-5112-B-T5
21	2	R5, R9	249	RES 249 OHM 1/10W .1% 0603 SMD	Susumu	RG1608P-2490-B-T5
22	1	R8	2.00k	RES, 2.00k ohm, 0.1%, 0.1W, 0603	Susumu Co Ltd	RG1608P-202-B-T5
23	1	R10	0	RES, 0 ohm, 5%, 0.1W, 0603	Vishay-Dale	CRCW06030000Z0EA
24	1	R12	820	RES 8.2k OHM 1/16W .02% 0805	Susumu	RG2012V-822-P-T1
25	2	R15, R18	1	RES 1.00 OHM 1/8W 1% SMD 0603	Vishay Beyschlag	MCT06030C1008FP500
26	1	R19	249	RES 249 OHM 1/2W .1% 2010 SMD	Yageo	RT2010BKC07249RL
27	1	R21	100k	RES, 100k ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW0603100KFKEA
28	1	RTHM	2k	THERMISTOR NTC 2K 5% 0603	Vishay-Dale	NTCS0603E3202JLT
29	1	U1		IC ADC 24BIT DEL/SIG LN 28TSSOP	Texas Instruments Inc	ADS1248IPW
30	1	U2		IC REG LDO ADJ .15A 8MSOP	Texas Instruments Inc	TPS7A4901DGNR
31	1	U3		IC VREF SERIES PREC 2.5V 8-MSOP	Texas Instruments Inc	REF5025IDGKT
32	1	U4		IC OPAMP DIFF 1.5MHZ SGL 8MSOP	Texas Instruments Inc	INA159AIDGKT
33	1	U5		IC OPAMP INSTR 1MHZ 8MSOP	Texas Instruments Inc	INA826AIDGKR
33	1	U6		ISOLATOR DGTL 25MBPS 4CH 16SOIC	Texas Instruments Inc	ISO7641FCDW
33	1	U7		5 Mbps Dual Channels, 1 / 1, Digital Isolator	Texas Instruments	ISO7221BD

Figure 31: Bill of Materials

Appendix B.

B.1 Electrical Schematic

Equations (**55**) - (**57**)show how the R_p,R_{f1},R_{f2} tolerant errors affect the result relative to the full-scale range individually. For better performance, R_p,R_{f1},R_{f2} are 0.1% resistors.

$$\begin{aligned} Code_{R_pERROR} &= Code_{TOTAL}\frac{I*(R_{RTHM}//(1+e)R_P+R_{f1})-I*R_{f2}}{2I\times R_{REF}} - Code_{ideal} \\ &= Code_{TOTAL}\frac{\dfrac{R_{RTHM}{}^2*R_P*e}{(R_{RTHM}+R_P)(R_{RTHM}+R_P(1+e))}}{2*R_{REF}} \end{aligned} \quad (55)$$

$$\begin{aligned} Code_{R_{f1}ERROR} &= Code_{TOTAL}\frac{I*(R_{RTHM}//R_P+R_{f1}(1+e))-I*R_{f2}}{2I\times R_{REF}} - Code_{ideal} \\ &= Code_{TOTAL}\frac{R_{f1}*e}{2*R_{REF}} \end{aligned} \quad (56)$$

$$Code_{R_{f1}OS} = Code_{R_{f1}ERROR} = Code_{TOTAL}\frac{R_{f1}*e}{2*R_{REF}}$$

$$\begin{aligned} Code_{R_{f2}ERROR} &= Code_{TOTAL}\frac{I*(R_{RTHM}//R_P+R_{f1})-I*R_{f2}(1+e)}{2I\times R_{REF}} - Code_{ideal} \\ &= Code_{TOTAL}\frac{R_{f2}*e}{2*R_{REF}} \end{aligned} \quad (57)$$

$$Code_{R_{f2}OS} = Code_{R_{f2}ERROR} = Code_{TOTAL}\frac{R_{f2}*e}{2*R_{REF}}$$

The current mismatch will introduce gain error and offset error as shown in Equation (**58**). We can also apply the same equation to get the current mismatch drift errors.

$$Code_{I_1ERROR} = Code_{TOTAL}\frac{I(1+mis)*(R_{RTHM}//R_P+R_{f1})-I*R_{f2}}{I(2+mis)\times R_{REF}} - Code_{ideal}$$

$$= Code_{TOTAL}\frac{mis(R_{RTHM}//R_P+2R_{f1})}{2*(2+mis)\times R_{REF}}$$

$$Code_{I_1OS} = Code_{TOTAL}\frac{2*mis*R_{f1}}{2*(2+mis)\times R_{REF}}$$

$$Code_{I_1GAIN} = \frac{Code_{I_1ERROR}-Code_{I_1OS}}{Code_{ideal}} = \frac{mis}{2+mis}$$

OR

$$Code_{I_2ERROR} = Code_{TOTAL}\frac{I*(R_{RTHM}//R_P+R_{f1})-I(1+mis)*R_{f2}}{I(2+mis)\times R_{REF}} - Code_{ideal}$$

$$= Code_{TOTAL}\frac{-mis*(R_{RTHM}//R_P+2R_f)}{2*(2+mis)\times R_{REF}}$$

$$Code_{I_2OS} = Code_{TOTAL}\frac{-2*mis*R_{f1}}{2*(2+mis)\times R_{REF}}$$

$$Code_{I_2GAIN} = \frac{Code_{I_2ERROR}-Code_{I_2OS}}{Code_{ideal}} = \frac{-mis}{2+mis}$$

(58)

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