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120-V AC, 200-W, 90% Efficiency, Interleaved Flyback for Battery Charging Applications Reference Design

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Design Resources

TIDA-00200	Tool Folder Containing Design Files
LM5032	Product Folder
TLC272	Product Folder

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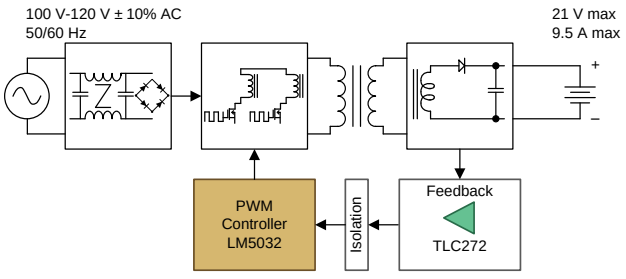
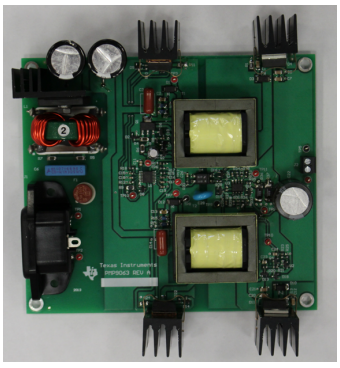
Design Features

- Input: 100 V to 120 V ±10%; AC 50 Hz or 60 Hz
- Output Voltage 21 V (5 Li-Ion Battery Cells)
- 9.5 A Charge Current
- 90% Efficiency
- Interleaved-Flyback Topology Based on LM5032 High-Voltage, Dual-Interleaved, Current-Mode Controller
- Programmable-Line Undervoltage Lockout (UVLO)
- Cycle-by-Cycle Current Limit
- Feedback Based on TLC272 Dual Single-Supply Operational Amplifier

Featured Applications

- Battery Chargers for
  - Power Tools
  - Garden Tools
  - Robotic Vacuum Cleaner
  - Robotic Mower





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1 System Description

This TI Design uses an interleaved flyback topology for battery-charger applications that require an output power level of approximately 200 W with a minimized bill of materials (BOM). The design is specified for 21-V output voltage as required for a 5-cell Li-Ion battery charger. Typical applications for this design are cordless screw drivers, impact drillers, robotic vacuum cleaners, and robotic mowers.

Besides the actual electronic components, cooling efforts are a major contributor to the overall system cost. By taking advantage of the LM5032 High-Voltage, Dual-Interleaved, Current-Mode Controller, the design accomplishes a great efficiency of 90% at full load. At the same time, the LM5032 spreads out the heat for greatly-reduced cooling efforts. A fan is typically not needed. The need for smaller form-factor heat sinks provides additional design flexibility.

The test data provided in this design guide shows that the design is fully functional and stable across the specified input and output range.

Thermal data taken at room temperature and still air from the non-enclosed design at different power levels indicate the required cooling method for a specific end product.

The design gives a proof of concept to an interleaved flyback for cost-sensitive charger applications at 200 W. However, the design is not intended to meet all the requirements of a specific end-product such as EMC, relevant safety standards, or quality. The important steps needed to turn this concept into a product design are discussed in Section 4.6.

The charging profile of a Li-Ion type battery consists of a constant-current phase until the battery voltage reaches the maximum voltage. The constant-current phase is followed by a constant-voltage phase with current decreasing until the termination current. This profile is the reason why a constant-current and constant-voltage topology is chosen for this design.

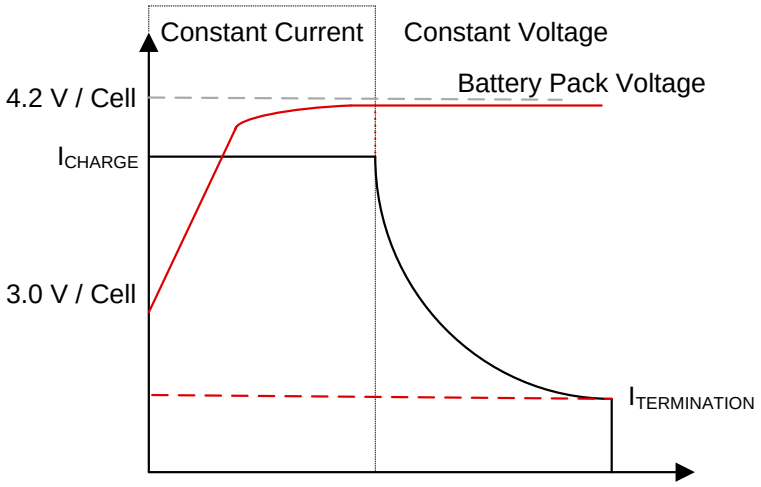


Figure 1. Li-Ion Charging Profile

2 Design Features

The design is intended for operation at any country specific *Lo-Line* voltages between 100-V and 120-V AC ±10%, at 50Hz or 60Hz.

The output voltage is fixed to 21 V. The output current is limited by hardware settings to 9.5 A.

A single optocoupler is used to return the feedback information on current and voltage to the LM5032 controller.

The programmable-line undervoltage lockout level is HW-configured to start the controller for voltages above 70-V AC and stop when the input voltage drops below 56-V AC.

The LM5032 cycle-by-cycle current limit feature prevents currents above 3.3 A on either primary-side path. The current on the secondary side is limited by the current-control loop.

3 Block Diagram

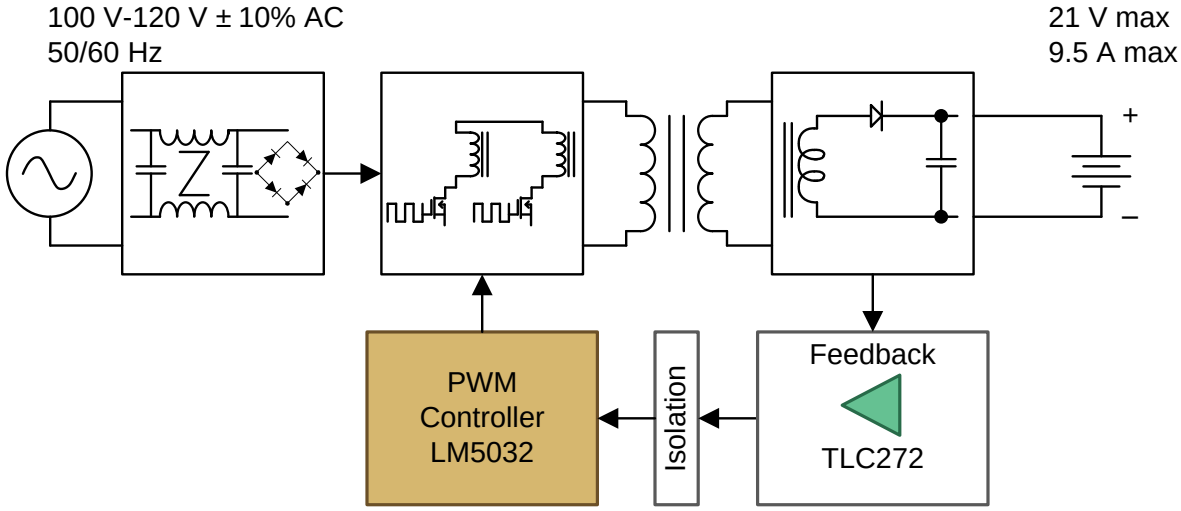


Figure 2. Block Diagram

4 Circuit Design and Component Selection

This design was originally created for a 120-W (21 V at 6 A, the PMP9063 design) charger application.

This design has been reconfigured to a 200-W (21 V at 9.5 A) charger application. Section 4.1 describes the parameters of this reconfigured design and how the components were chosen.

4.1 Topology and Device Selection

Designers typically use a flyback topology in cost-sensitive applications up to approximately 100 W. By using an interleaved topology, it is possible to double the power to the 200-W range by spreading the power losses across two paths.

The LM5032 High-Voltage, Dual-Interleaved, Current-Mode Controller supports a dual path implementation in an ideal and cost-efficient way. Besides having all features integrated to support an interleaved topology, LM5032 provides advanced capabilities for stability, startup behavior, protection, and powerful output drivers needed for a high-power charger design.

The LM5032 chip offers two fully-integrated, current-mode controlled channels. The channels are 180° out-of-phase with each other to minimize input-current ripple. Minimizing current ripple keeps the cost for the input capacitors as low as possible. Special care has been taken by the designers to assure stable operation during continuous-current mode as well. Furthermore, fast comparators allow for minimal duty cycle as needed for the typically very-low charging currents near the end of a charging cycle.

The startup and stop operation of the LM5032 device is well-defined. The LM5032 startup and stop operation assures stable and predictive operation for a wide range of input-voltage levels. The wide range of input-voltage levels is needed to configure the support of several countries' line voltages and a full spectrum of load situations. Maximum load means an empty battery is plugged into the charger. Mininum load means no battery or an already-charged battery is plugged into the charger.

In order to assure the quality and safety for the end-product design, designers can take advantage of several protection features integrated into LM5032. Thermal shutdown, UVLO, and overcurrent protection prevent damage to the circuitry, but are not latching events so the end-product can recover without interaction of the user in most cases.

Switching losses are reduced by powerful compound-gate drivers with CMOS and bipolar-output transistors in parallel, providing a faster turnoff of the primary switch. The gate drivers provide 1.5-A sourcing and 2.5-A sinking current to fit the requirements of this high-powered charger application.

The topology requires two reasonably-fast operational amplifiers. The TLC272 device is an ideal fit since the device matches the electrical requirements and provides two quality amplifiers in a single package. TLC272 has a high offset stability that helps to avoid any instability in this charger design. Being able to operate from a single-supply rail keeps the BOM low at a system level. The TLC272's popularity allows for attractive pricing and various temperature and packaging options. The integrated electrostatic discharge (ESD) protection may not be a mandatory requirement for the described use case. However, ESD helps to reduce yield issues in manufacturing.

4.2 Device Setting

The first step in this design is to set the LM5032 device correctly. First, set the switching frequency. The two gate drivers (OUT1 and OUT2) are switching at 180° out of phase, and at half of the LM5032 oscillator frequency. Therefore, to obtain a 100-kHz switching frequency (Fsw), the oscillator frequency (Fosc) is set at 200 kHz.

$$R_T = \frac{17100}{F_{osc}} - 0.001 \times (F_{osc} - 400) \quad (1)$$

With R_T in kΩ and Fosc in kHz.

Once the switching frequency is set, setting the LM5032 maximum duty cycle (D_{max}) allowed is now possible. The LM5032 is capable of an 80% maximum duty cycle. By correctly setting R_{DCL}, according to Equation 2, the LM5032 maximum duty cycle value can be decreased. Such a limitation is not needed in this design so this feature is disabled by setting $R_{DCL} > R_T$.

$$D_{max} = 80\% \times \frac{R_{DCL}}{R_T} \quad (2)$$

The next step is setting UVLO. To set UVLO, calculate the resistor divider needed to define the voltage at which LM5032 starts working (V_{PWR}) and the voltage at which LM5032 stops (V_{PWR}-V_{Hys}). In the present design, the LM5032 device is enabled when the voltage reaches 100 V and the LM5032 device is disabled when the voltage goes below 80 V. The LM5032 enable and disable voltages are DC voltages.

$$R_{UVLO1} = \frac{V_{Hys}}{20\ \mu A} \quad (3)$$

$$R_{UVLO2} = \frac{1.25 \times R_{UVLO1}}{V_{PWR} - 1.25} \quad (4)$$

The next step is to take care of the soft start (SS). Once V_{CC} reaches the UVT threshold (approximately 7.6 V), each SS output starts charging the soft start capacitors. The soft start time is defined by Equation 5.

$$t_{soft\_start} = 3 \times 10^4 \times C_{SS} \quad (5)$$

The maximum voltage allowed at the LM5032 pins is 100 V. As the input voltage is higher, the LM5032 is supplied either through a linear regulator or from the auxiliary winding of the first transformer. During start up, the discrete linear regulator formed by Q1, D2, and R4 is active. Once the system is up and running, LM5032 is then supplied by the auxiliary winding. The LM5032 internal regulator is not used.

4.3 Power Stage

4.3.1 Input

To start, calculate the input current and its influence on the diode bridge as shown in Equation 6.

$$Pin = \frac{Vout \times Iout}{\eta} \quad (6)$$

With η the target efficiency (in this case, 90%).

$$Iin_{rms\_max} = \frac{Pin}{Vin\_min \times PF} \quad (7)$$

With PF the estimated power factor (in this case, 0.5)

$$Iin_{peak} = Iin_{rms\_max} \times \sqrt{2} \quad (8)$$

$$Iin_{avg} = \frac{Iin_{peak}}{\pi} \quad (9)$$

$$Pbridge = V_{forward\_bridge} \times Iin_{avg} \quad (10)$$

With $V_{forward\_bridge}$ the forward voltage of the diode bridge.

The next step is to choose the input capacitors.

$$V_{bulk\_min} = \text{input ripple factor} \times Vin_{min} \quad (11)$$

$$t_{storage} = \frac{1}{4 \times F_{line\_min}} \times \left(1 + \frac{V_{bulk\_min}}{Vin\_min}\right) \quad (12)$$

With F_{line_min} the minimum line frequency.

$$Cin_{AC} = \frac{2 \times Pin \times t_{storage}}{\left(Vin_{min}^{2} - V_{bulk\_min}^{2}\right)} \quad (13)$$

$$Cin_{DC} = \frac{2 \times Pin}{\left(Vin_{min}^{2} - V_{bulk\_min}^{2}\right) \times Fsw} \quad (14)$$

Cin is chosen to fit the higher value of Cin_{AC} and Cin_{DC}.

4.3.2 Transformer

As discussed in Section 4, the original design was targeted to be in boundary mode at 120 W, 21 V at 6 A. As the design is interleaved, each leg provides 3 A. The transformer is designed according to those goals.

The parameters that are important to define the transformer in this design are the turn ratio and the minimum inductor value to achieve boundary mode at average-input voltage.

$$Vin_{avg} = \frac{Vin_{min} + Vin_{max}}{2} \quad (15)$$

$$n = \frac{Vin_{avg}}{Vout + V_{forward}} \quad (16)$$

With n the turn ratio between the primary and the secondary side and $V_{forward}$ is the forward voltage of the rectifying diode.

$$n_{aux} = \frac{Vin_{avg}}{Vaux} \quad (17)$$

With n_{aux} the turn ratio between the primary and the auxiliary side.

$$L_{pri\_min} = \frac{Vin_{avg}^{2}}{8 \times (Vout + V_{forward}) \times Iout \times Fsw} \quad (18)$$

Once the turn ratio and the primary inductor are set, the relevant parameters can be calculated for this 200-W design such as the duty cycle, the reflected voltage, the average current, the current ripple, the peak current, and the RMS current for both the primary and secondary side.

$$D = \frac{n \times (Vout + V_{forward})}{Vin + n(Vout + V_{forward})} \quad (19)$$

$$V_{fly} = (Vout + V_{forward}) \times n \quad (20)$$

With V_{fly} the reflected voltage.

$$V_{DS} = Vin + V_{fly} \quad (21)$$

With V_{DS} the maximum voltage on the switch node (without ringing).

$$V_{diode} = \frac{Vin}{n} + Vout \quad (22)$$

With V_{diode} the diode voltage, without ringing.

$$I_{pri\_avg} = \frac{Iout}{(1-D) \times n} \quad (23)$$

With I_{pri_avg} the average primary current.

$$\Delta I_{pri} = \frac{Vin \times D}{L_{pri} \times Fsw} \quad (24)$$

With ΔI_{pri} the primary current ripple.

$$I_{pri\_peak} = \frac{I_{pri\_avg} + \frac{\Delta I_{pri}}{2}}{\eta} \quad (25)$$

$$I_{pri\_valley} = \frac{I_{pri\_avg} - \frac{\Delta I_{pri}}{2}}{\eta} \quad (26)$$

$$I_{pri\_rms} = \sqrt{D \times \left[I_{pri\_peak} \times I_{pri\_valley} + \frac{1}{3}\left(I_{pri\_peak} - I_{pri\_valley}\right)^{2} \right]} \quad (27)$$

For the secondary side, the calculations are as follows:

$$L_{sec} = \frac{L_{pri}}{n^{2}} \quad (28)$$

$$I_{sec\_avg} = I_{pri\_avg} \times n \quad (29)$$

$$\Delta I_{sec} = \Delta I_{pri} \times n \quad (30)$$

$$I_{sec\_peak} = I_{sec\_avg} + \frac{\Delta I_{pri}}{2} \times n \quad (31)$$

$$I_{sec\_valley} = I_{sec\_avg} - \frac{\Delta I_{pri}}{2} \times n \quad (32)$$

$$I_{sec\_rms} = \sqrt{(1-D) \times \left[I_{sec\_peak} \times I_{sec\_valley} + \frac{1}{3}\left(I_{sec\_peak} - I_{sec\_valley}\right)^{2} \right]} \quad (33)$$

Table 1 shows the worst-case parameters of this design.

Table 1. Design Parameters

n	7.2	n_{aux}	9
L_{pri}	500 µH	L_{sec}	9.645 µH
D_{min}	0.45	D_{max}	0.563
V_{fly}	154.8 V	V_{DS} (1)	344.8 V
V_{diode} (1)	47.389 V		
I_{pri_avg} (2)	1.511 A	I_{sec_avg} (2)	10.88 A
ΔI_{pri} (2)	1.35 A	ΔI_{sec} (2)	9.734 A
I_{pri_peak} (2)	2.43 A	I_{sec_peak} (2)	15.74 A
I_{pri_rms} (2)	1.3 A	I_{sec_rms} (2)	7.42 A

(1) V_{DS} and V_{diode} are calculated with Vin_{max}.
(2) All currents are calculated with Vin_{min}.

4.3.3 Output

The output capacitor is designed to withstand load step as shown in Equation 34.

$$Cout > \frac{0.5 \times I_{loadstep}}{V_{step} \times Fco} \tag{34}$$

Once the value of the output capacitor is chosen, it is necessary to make sure that the current ripple is within the capacitor specification. First, calculate the AC current on the secondary side.

$$I_{sec\_AC} = \sqrt{I_{sec\_rms}^2 - Iout^2} \tag{35}$$

Then, calculate the impedance of each capacitor on the output as well as the total impedance.

$$Z_C = ESR + \frac{1}{2 \times \pi \times Fsw \times C} \tag{36}$$

$$Z_{Cout\_total} = \frac{1}{\sum \frac{1}{Z_C}} \tag{37}$$

The designer has to ensure that the AC current through each output capacitor is within the capacitor specification.

$$I_{AC\_C} = I_{sec\_AC} \times \frac{Z_{Cout\_total}}{Z_C} \tag{38}$$

4.3.4 MosFETs and Snubber

The current and the voltage that applies to the MosFET are calculated in Section 4.3.2.

NOTE: The V_{DS} calculated previously is without taking the ringing into account.

The ringing is also influenced by the snubber networks. The snubber should be optimized in the lab to find a fitting tradeoff between the overshoot allowed and the power dissipated by the snubber.

Another way of limiting the overshoot on the switch node is to add a diode in parallel to a small resistor between the gate driver and the gate of the MosFET. The resistor slows down the turn-on time of the FET, increasing the switching losses, but decreasing the overshoot. The diode allows a quick turn-off time. The value (or the need) of the gate resistor also needs to be optimized empirically in the lab.

4.3.5 Diode

As shown in Section 4.3.2, the current and the voltage that applies to the diode are calculated.

4.4 Voltage and Current loop

The charging cycle of a Li-Ion Battery (or a similar battery), consists of a constant-current phase and a constant-voltage phase. To reflect this behavior, this reference design contains two feedback paths.

The first feedback path regulates the voltage in the constant-voltage phase through the resistor divider formed by R26 and R31. The voltage obtained is compared with the reference set by R27 and R32.

The second feedback path regulates the current in the constant-current phase, once the output current reaches the output-current limit. The output-current limit is set by the value of the two parallel shunt resistors R36 and R37. The voltage across those resistors is compared with the reference set by R33 and R38.

The designer can change the output voltage by changing the value of R27 and R32. The designer can change the output current limit by changing R36 and R37. If the temperature dissipated by the shunt resistors is too high, the designer may either increase the number of shunt resistors in parallel or tune the voltage reference set by R33 and R38.

4.5 Layout guideline

The LM5032 current sense and PWM comparators are very fast and respond to short duration noise pulses. The components at the CS, COMP, SS, DCL, UVLO, and the RT/SYNC pins should be physically as close as possible to the IC, to minimize noise pickup in the PC board tracks.

Low-inductance resistors should be used for the sense resistors in the drive-transistor sources. In this case, all the noise-sensitive, low-current ground tracks should be connected in common near the IC. Then a single connection should made to the power ground (sense-resistor ground point). The outputs of the LM5032 should have short direct paths to the power MOSFETs in order to minimize inductance in the PC board traces.

The two ground pins (GND1, GND2) must be connected together with a short direct connection to avoid jitter due to relative ground bounce in the operation of the two regulators.

If the internal dissipation of the LM5032 produces high junction temperatures during normal operation, the use of wide PC board traces can help conduct heat away from the IC. Judicious positioning of the PC board within the end product, along with the use of any available air flow (forced or natural convection) can help reduce the junction temperatures.

4.6 Production Considerations

This design gives proof of concept for an interleaved flyback for cost-sensitive charger applications at 200 W but is not intended to be used *as is*, in production.

As mentioned in Section 4, this design was originally created for 120 W. Some parameters may not be optimal for a production-ready, 200-W application. The designer should make sure that all the parameters of the design fit his requirements.

The following is a non-exhaustive list for consideration.

- The maximum current ripple at the output capacitor is higher than the maximum value defined in the capacitor data sheet, Rubycon: Capacitor Data Sheet, *Miniature Aluminum Electrolytic Capacitors, ZL Series, 105°C High Ripple Current, Low Impedance*, (Capacitor Data Sheet). The higher value is not problem for a prototype or a proof of concept. However, the lifetime of the capacitor will be impacted and therefore, not fit for production. Using two capacitors instead or using a different capacitor may be needed.
- The electrolytic capacitors at the input should be kept away from thermal sources in order to increase the lifetime of the capacitors. Increasing the distance between the electrolytic capacitors and the diode bridge may be needed for production.
- The current design cannot provide the full load when the input voltage is lower than 95-V AC. The current design can be improved either by decreasing the maximum output power below 180 W, by increasing the input capacitors (to reduce the input voltage ripple), or by decreasing the UVLO.
- Thermal management should be adapted to fit the end-equipment requirements
- Depending on the end-product requirements, effort will be needed to verify compliancy with standards (such as safety, EMC, and so forth).

5 Getting Started

The input must be connected to connector J1. The voltage applied should be between 95-V and 132-V AC (startup at 70-V AC and shutdown at 56-V AC) or between 120-V and 190-V DC (startup at 100-V DC and shutdown at 80-V DC).

The load should be connected to the connector J2.

NOTE: The RTN pin of J2 is not the ground. Connecting the ground to RTN or to TP5 will short circuit the output current sensing, which is not advised.

6 Test Results

6.1 Efficiency

The efficiency is determined with the help of the measurements of the input voltage, input current and power factor at connector J1, as well as output voltage and current at connector J2. The input voltage is set to 120-V AC.

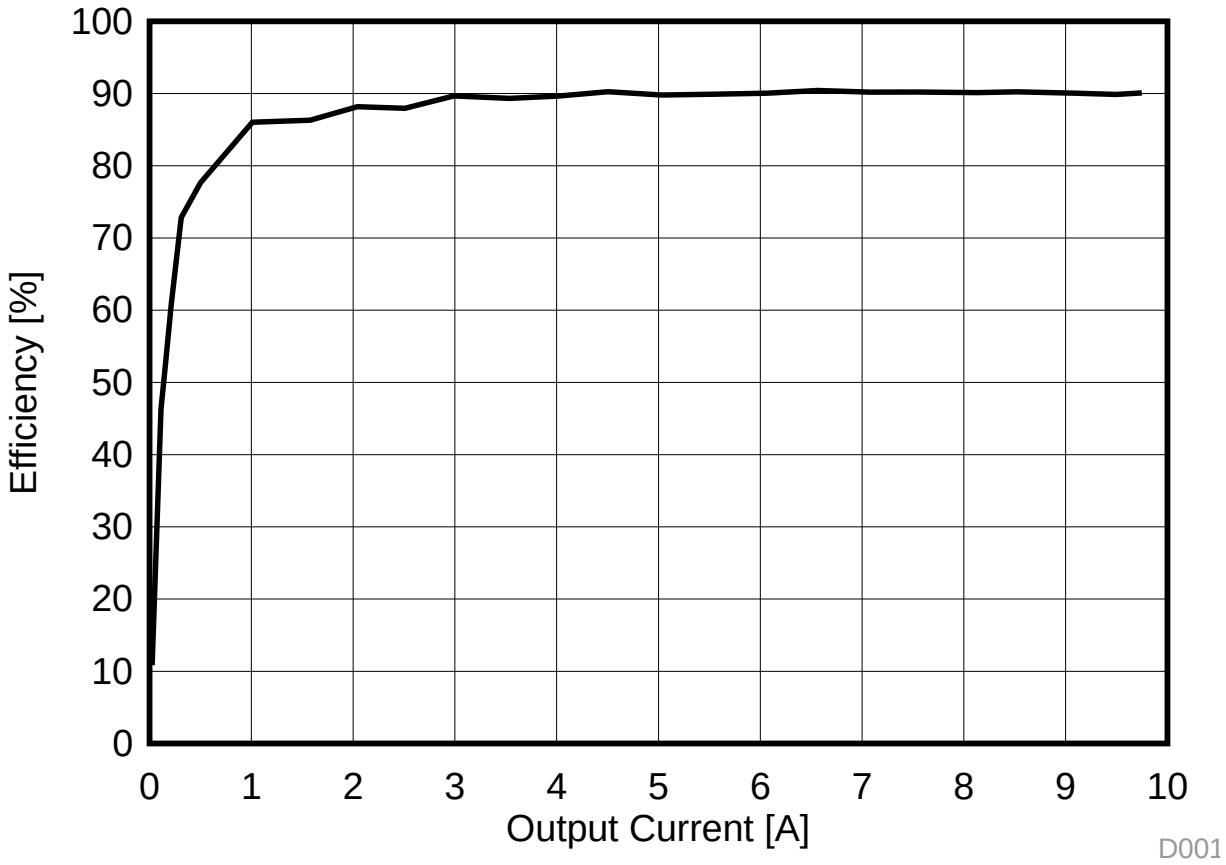


Figure 3. Efficiency

6.2 Output Load Characteristics

In Figure 4, the expected charger behavior with a constant-voltage phase and a constant-current phase can be clearly seen. The input voltage is set to 120-V AC.

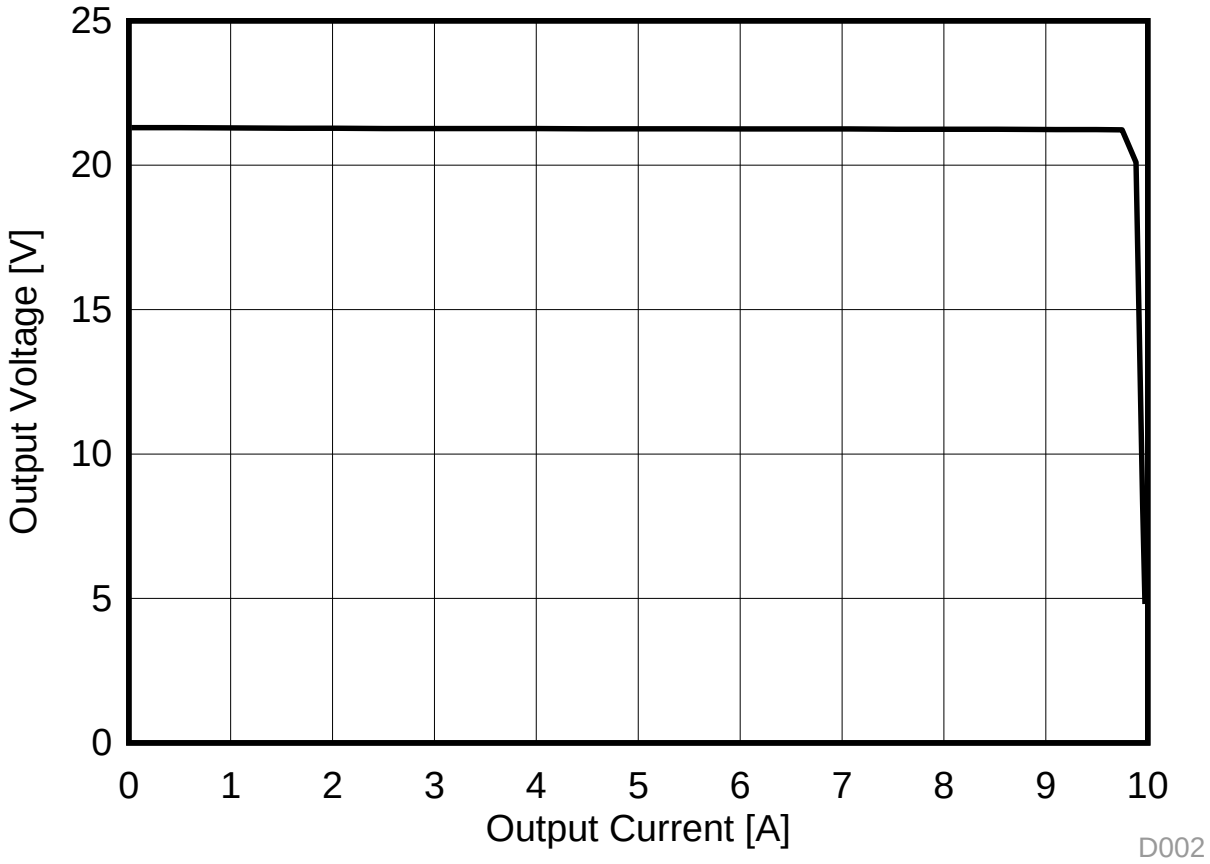


Figure 4. Output Load Characteristics

6.3 Vout versus Vin

The following measurements as shown in Figure 5 were done with 9 A at the output.

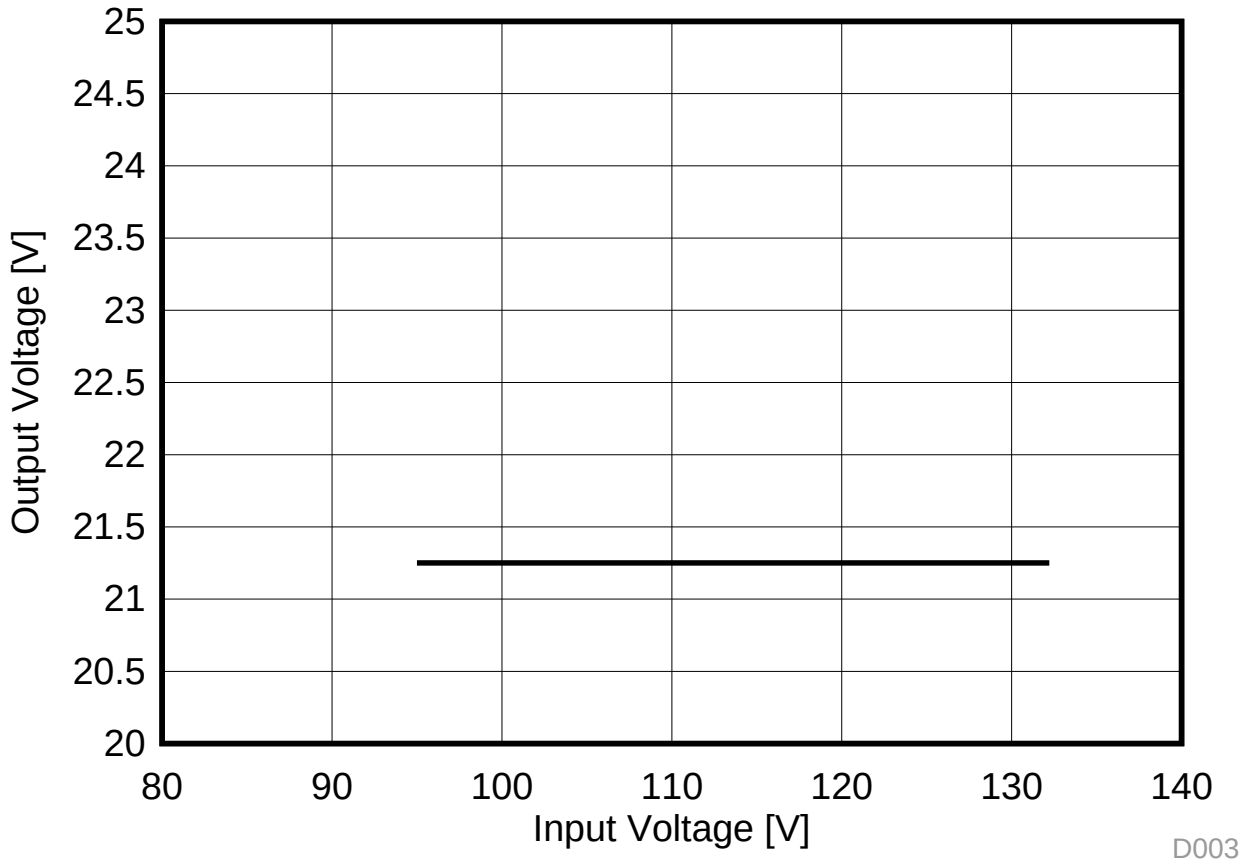


Figure 5. Output Voltage versus Input Voltage

6.4 Stand By Power

With no load draw at the output, 1.42 W is measured at the input, with 120-V AC.

6.5 Input line

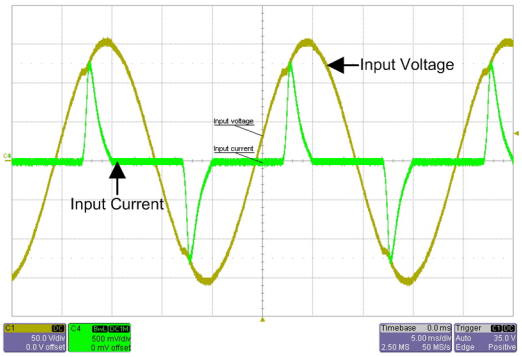


Figure 6. Input Line with 9-A Output Current, at 108-V AC Input Voltage

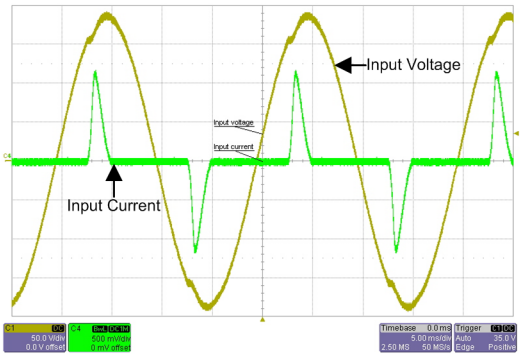


Figure 7. Input Line with 9-A Output Current, at 132-V AC Input Voltage

6.6 Thermal Image

The thermal picture was taken at 25°C room temperature, with 120-V AC input and 21-V at 9.5 A output. All the hot spots (>75°C) are identified in Figure 8. The rest of the board is less than 75°C.

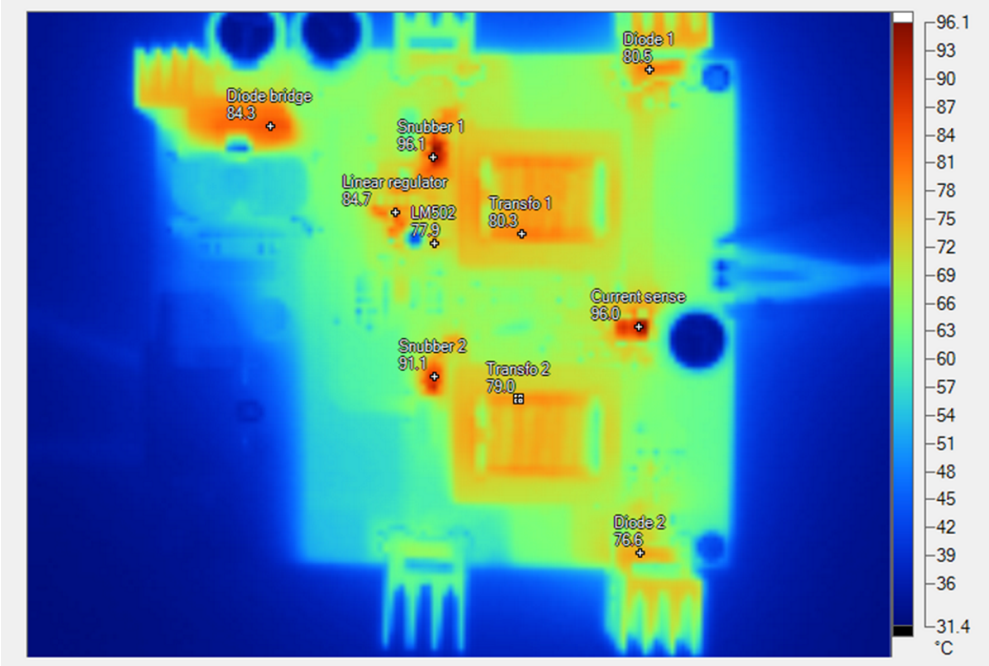


Figure 8. Thermal Image

Table 2. Hot Spots

	DIODE BRIDGE	LINEAR REGULATOR	SNUBBER1	TRANSFO1	DIODE1	SNUBBER2	TRANSFO2	DIODE2	CURRENT SENSE	LM5032
120W	62.8°C	74.3°C	78.8°C	65.9°C	59.1°C	74.6°C	64.4°C	55.2°C	62.8°C	68.1°C
160W	74.1°C	78.1°C	86.7°C	72.8°C	70.3°C	80.5°C	71.3°C	66.7°C	78.6°C	71.8°C
200W	84.3°C	84.7°C	96.1°C	80.3°C	80.5°C	91.1°C	79°C	76.6°C	96.6°C	77.9°C

6.7 Switch Node Waveforms

Figure 9 and Figure 10 are the Switch Node waveforms at full load. Figure 11 and Figure 12 are the Switch Node waveforms at light load. These curves were measured at the test points TP3 (SW node 1) and TP7 (SW node 2).

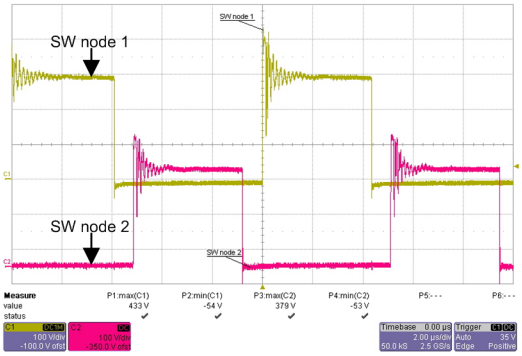


Figure 9. Switch Node at 9-A Output and 120-V DC Input Voltage

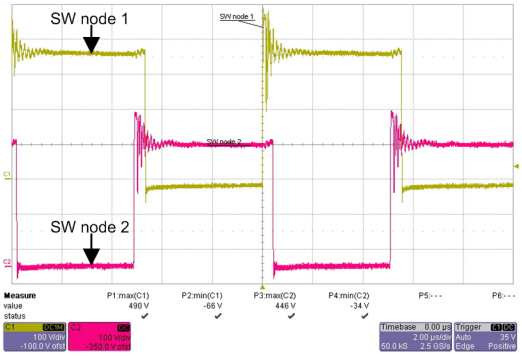


Figure 10. Switch Node at 9-A Output and 190-V DC Input Voltage

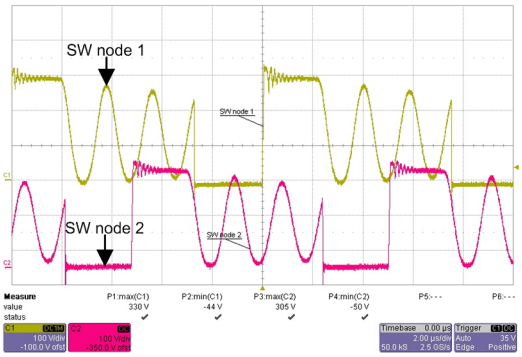


Figure 11. Switch Node at 0.9-A Output and 120-V DC Input Voltage

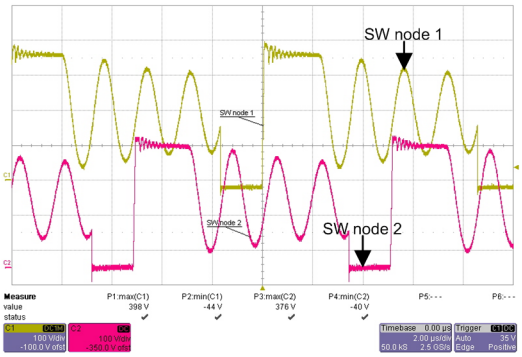


Figure 12. Switch Node at 0.9 A Output and 190-V DC Input Voltage

6.8 Constant-Voltage Mode Load-Step Response

The load-step response was measure across the output capacitor C22 with 120-V AC and 190-V AC input and a current step from 1 A to 9 A at the output.

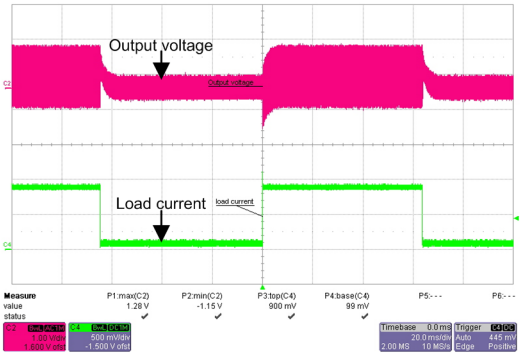


Figure 13. Load-Step Response from 1 A to 9 A at 120-V DC Input Voltage

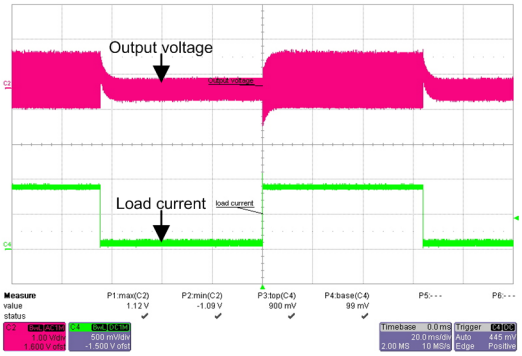


Figure 14. Load-Step Response from 1 A to 9 A at 190-V DC Input Voltage

6.9 Output Ripple

The output ripple was measured across the output capacitor C22 with 120-V AC and 190-V AC input and 9 A at the output.

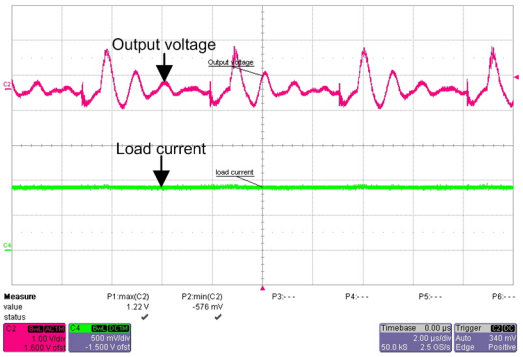


Figure 15. Output Voltage Ripple at 9-A and 120-V DC Input Voltage

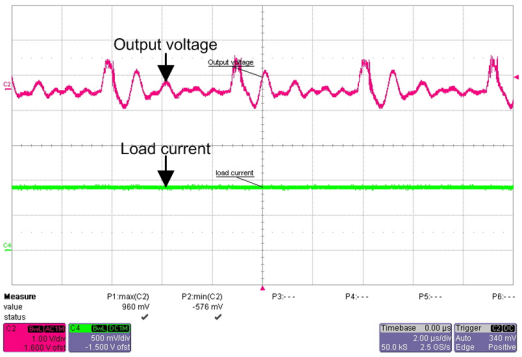


Figure 16. Output Voltage Ripple at 9-A and 190-V DC Input Voltage

6.10 Frequency response

The Bode plots in Figure 17 verify that the loop is stable. The Bode plots have been measured for minimum, nominal, and maximum input voltages, with 8.5 A of output current. The design has sufficient phase and gain margin, as show in Table 3.

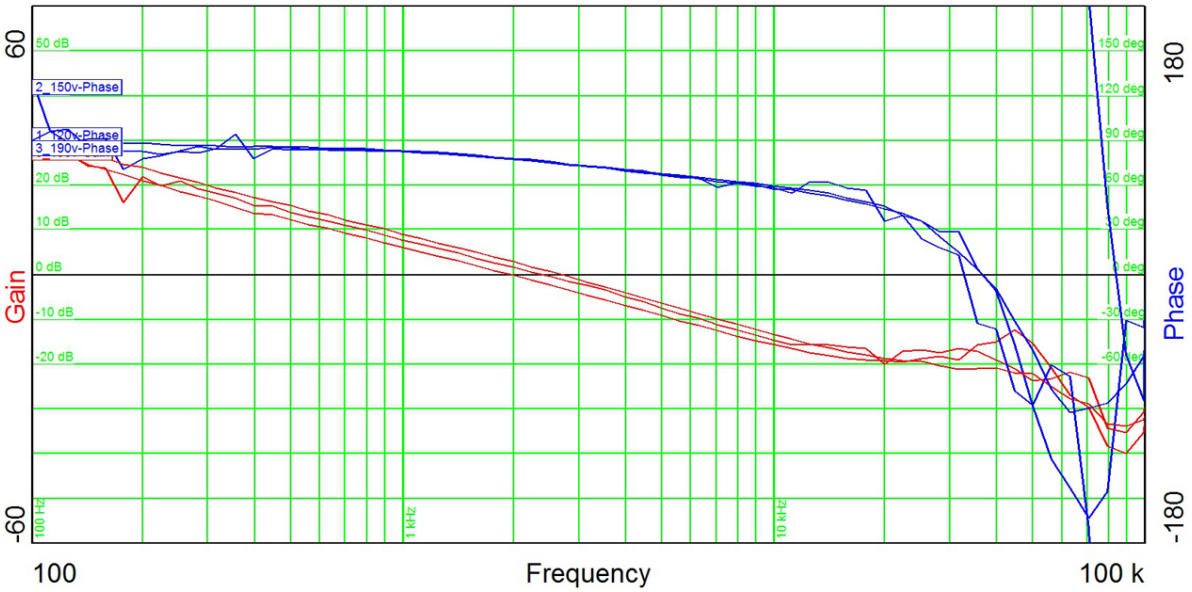


Figure 17. Bode Plot

Table 3. Gain and Phase Margin

	PHASE MARGIN	GAIN MARGIN
120-V DC	77.56°	-15.61 dB
150-V DC	75.39°	-16.77 dB
190-V DC	74.73°	-21.01 dB

7 Design Files

7.1 Schematics

To download the Schematics, see the design files at TIDA-00200.

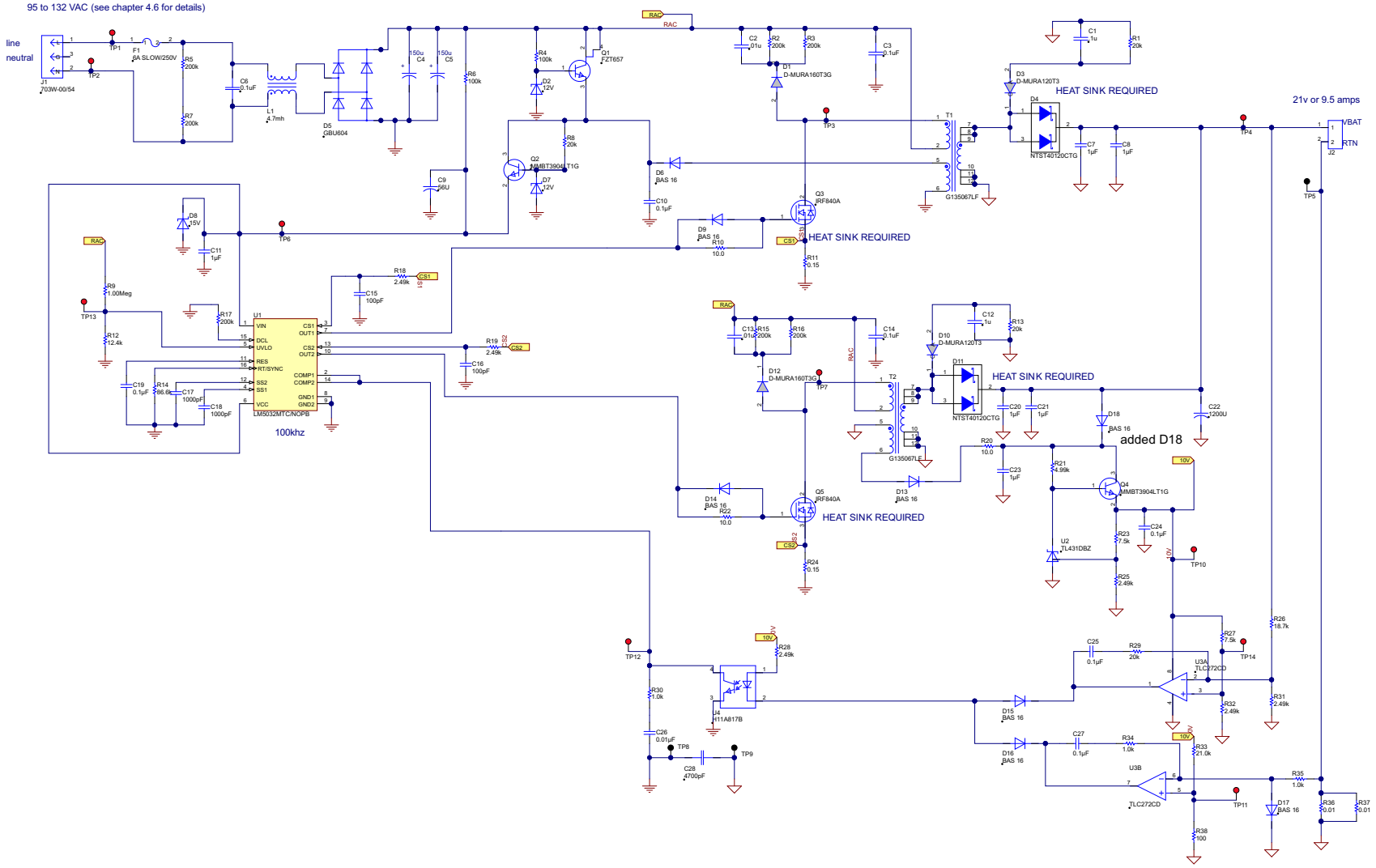


Figure 18. Schematics

7.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00200.

Table 4. BOM

DESIGNATOR	DESCRIPTION	MANUFACTURER	PARTNUMBER	QUANTITY
C1, C12	Capacitor, Ceramic, 250V, [temp], [tol]	muRata	GRM42-6yyyxxxKvv	2
C2, C13	Capacitor, Ceramic Chip, 250V, ±10%, Capacitor	STD	STD	4
C3, C14	Capacitor, Polyester, 400V, 10%	Panasonic	ECQ-E2104KB	2
C4, C5	Capacitor, multi pattern, TH 0.080 to 0.200	panasonic	EEUEB2D151	2
C6	Capacitor, Leaded, 0.10 uF, 275 VAC, X2		B81130-C1104-Mxxx	1
C7, C8, C20, C21	CAP, CERM, 1uF, 25V, +/-10%, X7R, 1206	Kemet	C1206C105K3RACTU	4
C9	Capacitor, Aluminum Electrolytic, vvV	Rubycon	16ZL56 5X11	1
C10, C19, C25, C27	CAP, CERM, 0.1uF, 50V, +/-10%, X7R, 0603	Kemet	C0603C104K5RACTU	4
C11	CAP, CERM, 1uF, 16V, +/-10%, X7R, 0805	Kemet	C0805C105K4RACTU	1
C15, C16	CAP, CERM, 100pF, 50V, +/-5%, C0G/NP0, 0603	Kemet	C0603C101J5GACTU	2
C17, C18	CAP, CERM, 1000pF, 50V, +/-10%, X7R, 0603	Kemet	C0603C102K5RACTU	2
C22	Capacitor, multi pattern, SM 1210 to E case + F THole	Rubycon	35ZL1200 12.5X20	1
C23	CAP, CERM, 1uF, 25V, +/-10%, X7R, 0805	TDK	C2012X7R1E105K	1
C24	CAP, CERM, 0.1uF, 25V, +/-10%, X7R, 0805	Kemet	C0805C104K3RACTU	1
C26	CAP, CERM, 0.01uF, 50V, +/-10%, X7R, 0603	Kemet	C0603C103K5RACTU	1
C28	Capacitor, Ceramic Disc, 250WV, 4700pF, Y5U ±20%	Panasonic	DE2EKY472MA2BM01	1
D1, D12	Rectifier, SMD Ultrafast Power, 600V 1A	On Semi	MURA160T3G	2
D2, D7	Diode, Zener, 12V, yy-mA	Diodes	MMBZ5242BLT1	2
D3, D10	Diode, UltraFast Rectifier, 1-A, 200-V	On Semi	MURA120T3	2

Table 4. BOM (continued)

DESIGNATOR	DESCRIPTION	MANUFACTURER	PARTNUMBER	QUANTITY
D4, D11	Diode, Schottky, 60V, 20A, TH	Vishay-Semiconductor	NTST40120CTG	2
D5	Diode, Bridge Rectifier, 6 A, 400V	Fairchild	GBU604	1
D6, D9, D13, D14, D15, D16, D17, D18	Diode, Switching, 200mA, 100V, 300mW	Vishay-Liteon	BAS16	8
D8	Diode, Zener, 15V, yy-mA	Diodes	MMBZ5245BLT1	1
F1	Fuse, TR5 Series, 6 slow, 250V	Wickmann	370 1400 041	1
J1	Connector, AC Board mount, 9mm	Qualtek Electronics	703W-00/54	1
J2	Terminal Block, 2-pin, 6-A, 3.5mm	OST	ED555/2DS	1
L1	Inductor, Common Mode Choke,	GCI	GVTM1-472	1
Q1	Trans, NPN Midium Power, 300V 3A	Zetex	FZT657	1
Q2, Q4	Trans, NPN, xx-V, yy-mA, zz-W	On Semi	MMBT3904LT1G	2
Q3, Q5	MOSFET, N-ch, 500-V, yy-A, 85-milliOhms	STD	STD	2
R1, R13	RES, 20k ohm, 5%, 0.25W, 1206	Vishay-Dale	CRCW120620K0JNEA	2
R2, R3, R5, R7, R15, R16	RES, 200k ohm, 5%, 0.25W, 1206	Vishay-Dale	CRCW1206200KJNEA	6
R4, R6	RES, 100k ohm, 5%, 0.25W, 1206	Vishay-Dale	CRCW1206100KJNEA	2
R8, R29	RES, 20k ohm, 5%, 0.1W, 0603	Vishay-Dale	CRCW060320K0JNEA	2
R9	RES, 1.00Meg ohm, 1%, 0.25W, 1206	Vishay-Dale	CRCW12061M00FKEA	1
R10, R20, R22	RES, 10.0 ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW060310R0FKEA	3
R11, R24	RES, 0.15 ohm, 5%, 0.25W, 1206	Panasonic	ERJ-8RSJR15V	2
R12	RES, 12.4k ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW060312K4FKEA	1
R14	RES, 86.6k ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW060386K6FKEA	1
R17	RES, 200k ohm, 5%, 0.1W, 0603	Vishay-Dale	CRCW0603200KJNEA	1
R18, R19, R25, R28, R31, R32	RES, 2.49k ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW06032K49FKEA	6
R21	RES, 4.99k ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW06034K99FKEA	1
R23, R27	RES, 7.5k ohm, 5%, 0.1W, 0603	Vishay-Dale	CRCW06037K50JNEA	2
R26	RES, 18.7k ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW060318K7FKEA	1
R30, R34, R35	RES, 1.0k ohm, 5%, 0.1W, 0603	Vishay-Dale	CRCW06031K00JNEA	3
R33	RES, 21.0k ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW060321K0FKEA	1
R36, R37	RES, 0.01 ohm, 1%, 1W, 2512	Vishay-Dale	WSL2512R0100FEA	2
R38	RES, 100 ohm, 5%, 0.1W, 0603	Vishay-Dale	CRCW0603100RJNEA	1
T1, T2	Transformer, Flyback, 500uH, TH	GCI Technologies	G135067LF	2
TP1, TP2, TP3, TP4, TP6, TP7, TP10, TP11, TP12, TP13, TP14	Test Point, Miniature, Red, TH	Keystone	5000	11

Table 4. BOM (continued)

DESIGNATOR	DESCRIPTION	MANUFACTURER	PARTNUMBER	QUANTITY
TP5, TP8, TP9	Test Point, Miniature, Black, TH	Keystone	5001	3
U1	High Voltage Dual Interleaved Current Mode Controller, 16-pin TSSOP, Pb-Free	National Semiconductor	LM5032MTC/NOPB	1
U2	IC, Precision Adjustable Shunt Regulator	TI	TL431DBVZ	1
U3	IC, Precision Dual Operational Amplifiers	TI	TLC272CD	1
U4	IC, Optocoupler, 5300-V, 80-160% CTR	QT Optoelectronics	H11A817B	1

7.3 Layer Plots

To download the layer plots, see the design files at TIDA-00200.

NOTE: All layer plots are viewed from the top side.

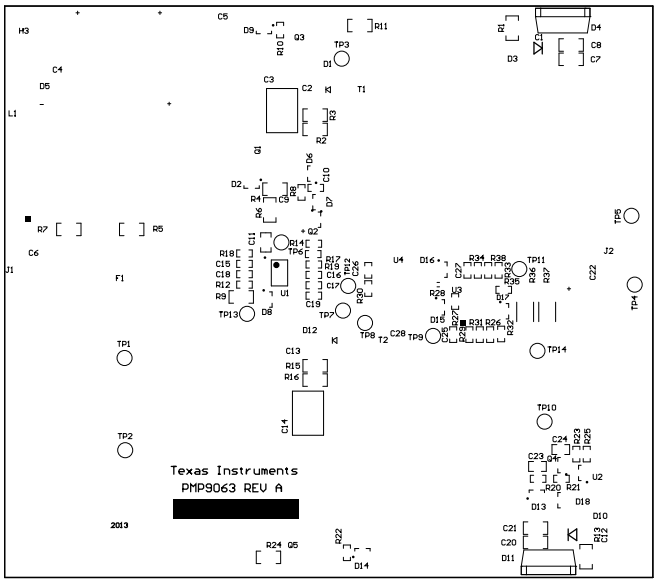


Figure 19. Top Overlay

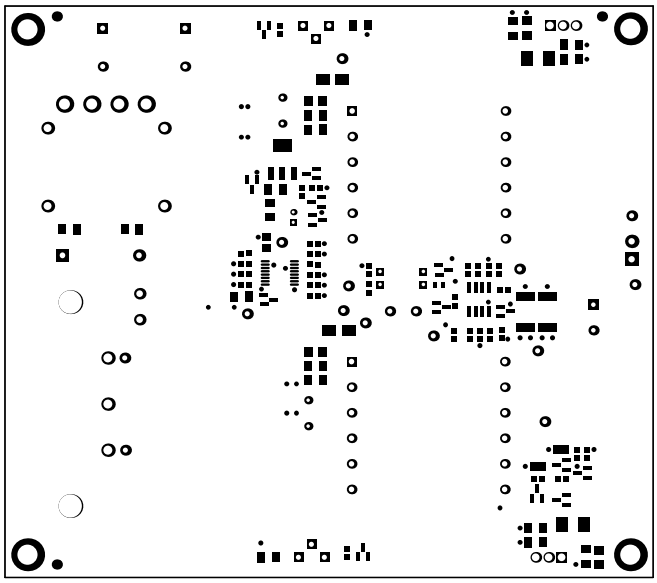


Figure 20. Top Solder Mask

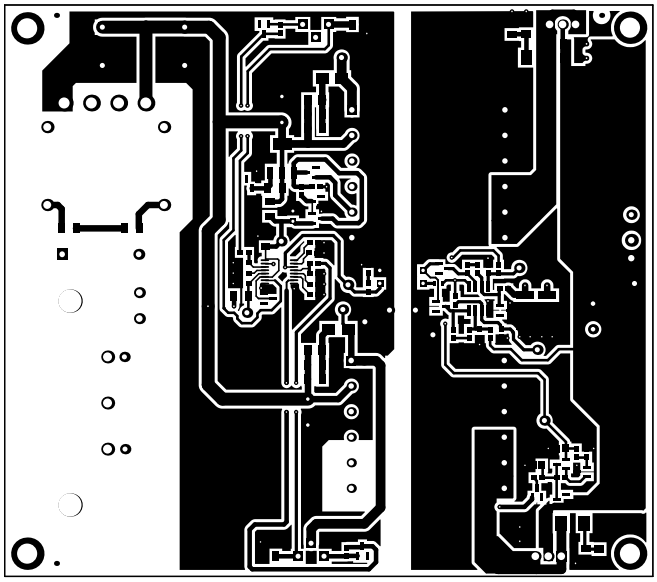


Figure 21. Top Layer

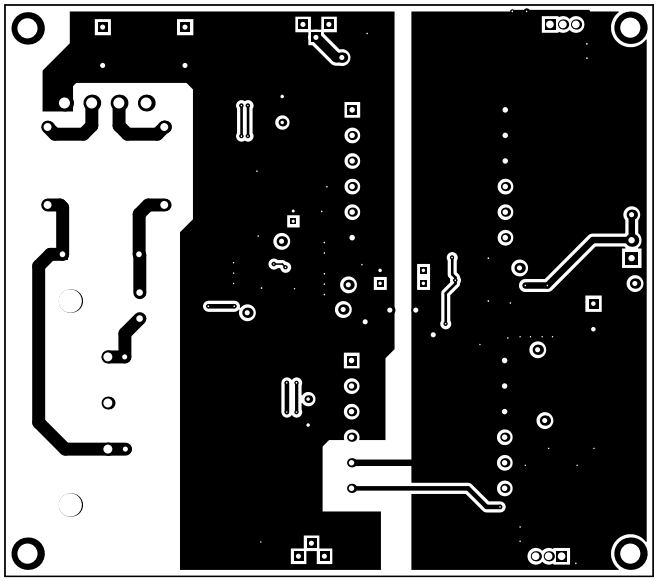


Figure 22. Bottom Layer

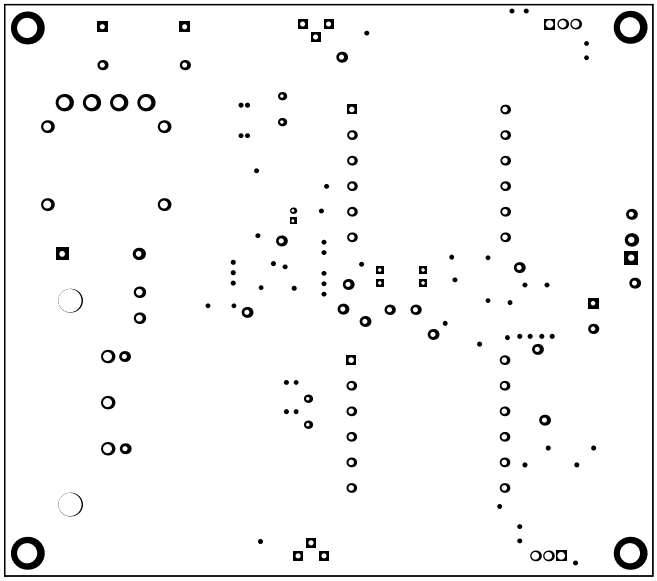
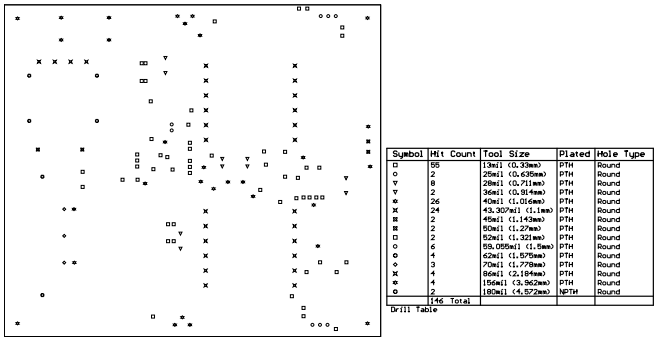


Figure 23. Bottom Solder Mask

Figure 24. Bottom Overlay



Symbol	Hit Count	Tool Size	Plated	Hole Type
□	55	13mil (0.33mm)	PTH	Round
○	2	25mil (0.635mm)	PTH	Round
▽	8	28mil (0.711mm)	PTH	Round
▽	2	36mil (0.914mm)	PTH	Round
✱	26	40mil (1.016mm)	PTH	Round
✕	24	43.307mil (1.1mm)	PTH	Round
⊠	2	45mil (1.143mm)	PTH	Round
⊞	2	50mil (1.27mm)	PTH	Round
□	2	52mil (1.321mm)	PTH	Round
○	6	59.055mil (1.5mm)	PTH	Round
○	4	62mil (1.575mm)	PTH	Round
◇	3	70mil (1.778mm)	PTH	Round
✕	4	86mil (2.184mm)	PTH	Round
✱	4	156mil (3.962mm)	PTH	Round
○	2	180mil (4.572mm)	NPTH	Round
	146 Total			

Drill Table

Figure 25. Drill Drawing

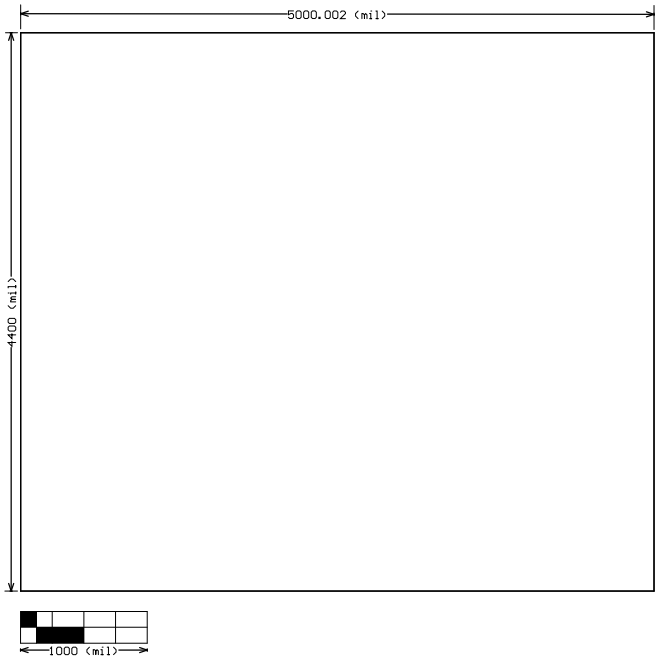


Figure 26. Board Dimensions

7.4 Altium Project

To download the Altium project files, see the design files at TIDA-00200.

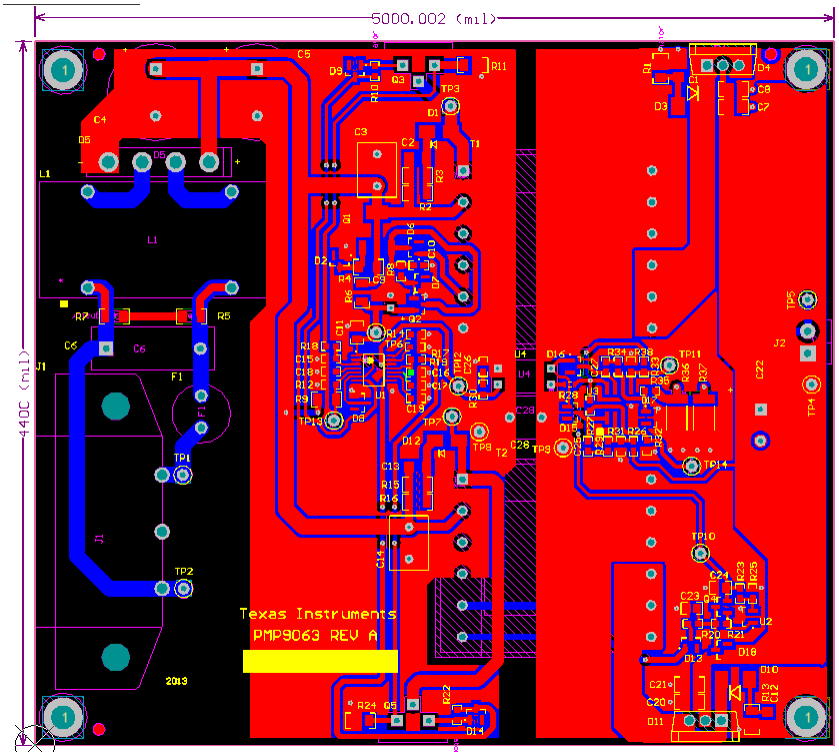


Figure 27. Top Side

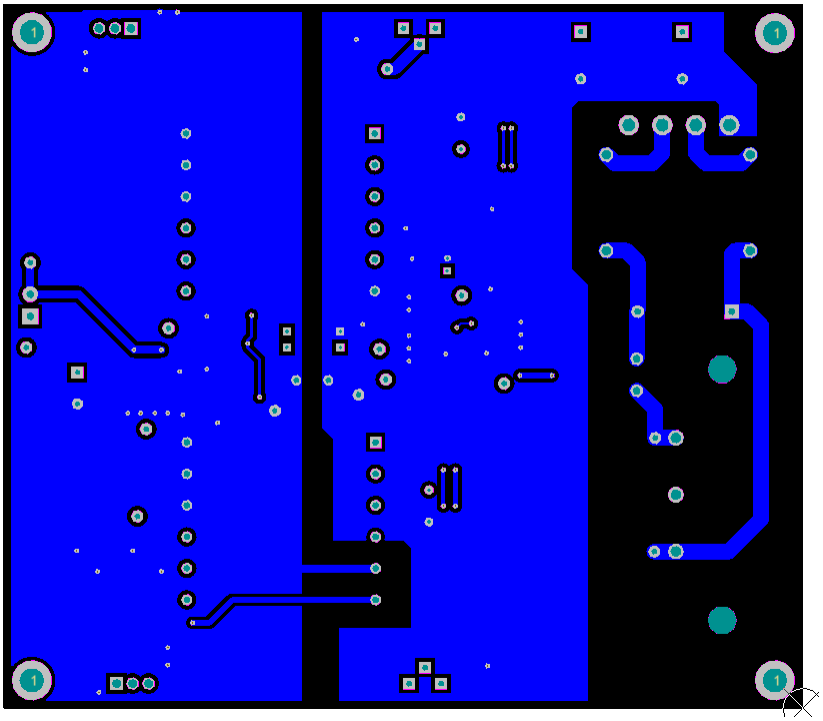


Figure 28. Bottom Side

7.5 Gerber Files

To download the Gerber Files, see the design files at TIDA-00200.

7.6 Assembly Drawings

To download the Assembly Drawings, see the design files at TIDA-00200.

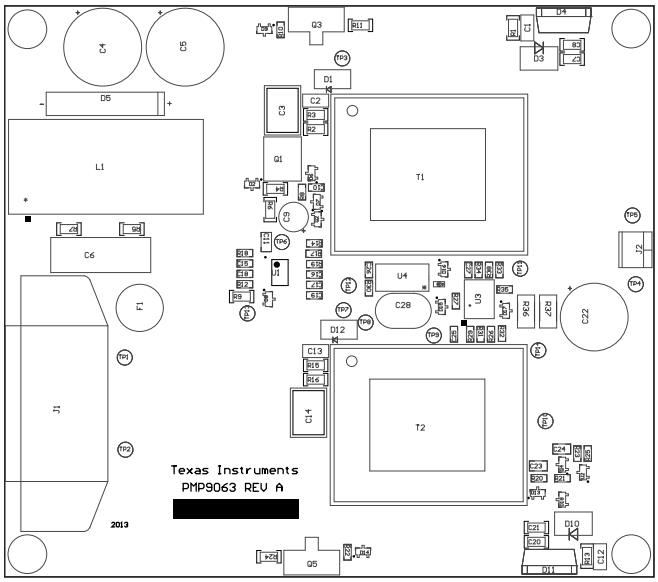


Figure 29. Top Assembly Drawing

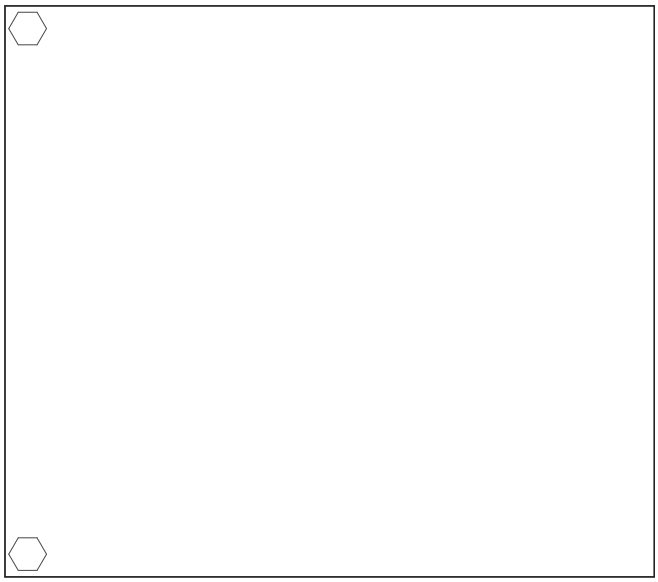


Figure 30. Bottom Assembly Drawing

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (July 2014) to A Revision	Page
• Changed title from *120-V AC Input, 200-W Interleaved Flyback for Battery Charging Applications* to *120-V AC, 200-W, 90% Efficiency, Interleaved Flyback for Battery Charging Applications Reference Design*	1

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