

TI Designs Half-Duplex, Non-Isolated RS-485 BoosterPack Reference Guide



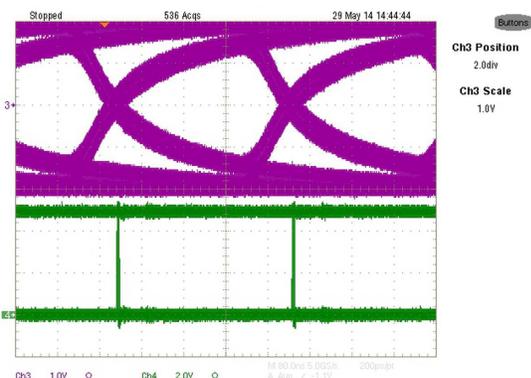
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Design Resources

TIDA-00214	Tool Folder Containing Design Files
SN65HVD24	Product Folder
TPS61220	Product Folder

**Eye Diagram at 3-Mbps Data Rate
Over 1024 Feet of Cable**



Design Features

The RS-485 Booster Pack enables any 20- and 40-pin TI LaunchPad with half-duplex, non-isolated RS-485 bus communication port.

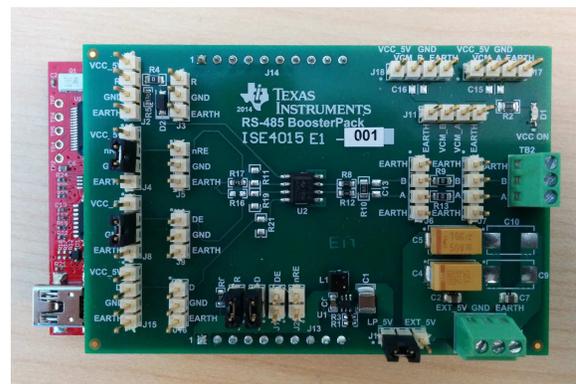
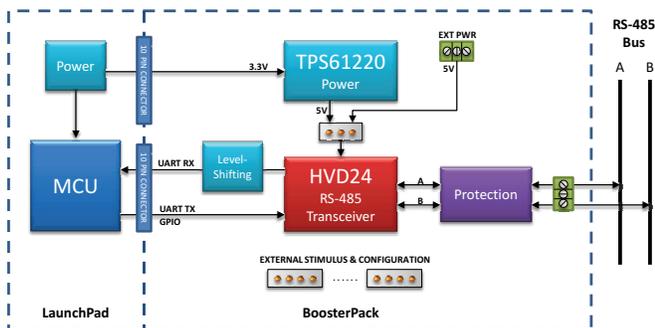
- Supports 1.25 Mbps data rates with cable lengths up to 1000 feet and a total of 32 nodes
- Multiple configuration options: on-board or external power source, external data stimulus and monitoring, common-mode voltage injection, configurable failsafe and bus termination loading
- IEC61000-4-4 (EFT): ± 2 kV, Class C
- IEC61000-4-5 (Surge): ± 0.5 kV, Class C
- IEC61000-4-2 (ESD): ± 8 kV, contact discharge, Class C
- Compatible with any 20- and 40-pin TI LaunchPad

Featured Applications

- Building Management Systems
- Factory Automation
- Building Automation
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1 Key System Specifications

Table 1. System Specifications

Specification	Value	Details
Nodes Supported	32	See Section 6.1
Data Rate (Mbps)	1.25 Mbps	See Section 6.1
Cable Length	1000 ft	See Section 6.1
Duplex	Half-Duplex	See Section 4.2
Node Topology	Daisy Chain	See Section 6.1
Isolation	None	See Section 4.2
Input Voltage	3.3-V/5-V	See Section 4.3
Temperature Rating	-40°C to 85°C	See Section 4.2
Visual Indicators	Power on LED	See Section 4.3
IEC 61000-4-2, Electro Static Discharge, Contact, Signal Lines	±8 kV - Class C	See Section 6.2
IEC 61000-4-4, Electrical Fast Transients, Signal Lines	±2 kV - Class C	See Section 6.2
IEC 61000-4-5, Surge, Signal Lines	±0.5 kV - Class C	See Section 6.2

2 System Description

The RS-485 BoosterPack enables any 20- and 40-pin TI LaunchPad with half-duplex, non-isolated RS-485 communication. The BoosterPack is designed and tested to support data rates up to 1.25 Mbps for cable lengths up to 1000 feet and a total of 32 nodes. The SN65HVD24 extended common-mode RS-485 transceiver is used to interface to the RS-485 bus.

The RS-485 BoosterPack can be powered from two different sources: the 3.3-V supply provided by the TI LaunchPad or an external 5-V power source. The TPS61220 boost converter is used to derive the 5-V source needed for the transceiver from the existing 3.3-V supply provided by the TI LaunchPad. An external 5-V power supply source can also be used to provide power directly to the RS-485 BoosterPack.

With the use of an external power supply and a signal generator, the RS-485 BoosterPack can be used to completely characterize an RS-485 system, independently of the TI LaunchPad. Multiple jumpers and test points allow for complete characterization of different RS-485 specifications such as multiple data rates, common-mode voltages, and termination configurations.

NOTE: The RS-485 BoosterPack is populated with the SN65HVD24 extended common-mode RS-485 transceiver. However the transceiver can easily be removed and replaced with any TI half-duplex, 8-pin SOIC RS-485 transceiver. This allows the system designer to evaluate many different transceivers with varying performance targets. The setup instructions and performance data in this document refer to the SN65HVD24.

2.1 SN65HVD24

The transceivers in the SN65HVD2x family offer performance far exceeding typical RS-485 devices. In addition to meeting all requirements of the TIA/EIA-485-A standard, the HVD2x family operates over an extended range of common-mode voltage, and has features such as high ESD protection, wide receiver hysteresis, and failsafe operation. This family of devices is ideally suited for long-cable networks, and other applications where the environment is too harsh for ordinary transceivers.

These devices are designed for bidirectional data transmission on multipoint twisted-pair cables. Example applications are digital motor controllers, remote sensors and terminals, industrial process control, security stations, and environmental control systems.

These devices combine a 3-state differential driver and a differential receiver, which operate from a single 5-V power supply. The driver differential outputs and the receiver differential inputs are connected internally to form a differential bus port that offers minimum loading to the bus. This port features an extended common-mode voltage range making the device suitable for multipoint applications over long cable runs with large ground potential differences (GPD).

The 'HVD20 provides high signaling rate (up to 25 Mbps) for interconnecting networks of up to 64 nodes.

The 'HVD21 allows up to 256 connected nodes at moderate data rates (up to 5 Mbps). The driver output slew rate is controlled to provide reliable switching with shaped transitions which reduce high-frequency noise emissions.

The 'HVD22 has controlled driver output slew rate for low radiated noise in emission-sensitive applications and for improved signal quality with long stubs. Up to 256 'HVD22 nodes can be connected at signaling rates up to 500 kbps.

The 'HVD23 implements receiver equalization technology for improved jitter performance on differential bus applications with data rates up to 25 Mbps at cable lengths up to 160 meters.

The 'HVD24 implements receiver equalization technology for improved jitter performance on differential bus applications with data rates up to 2 Mbps at cable lengths up to 500 meters.

The receivers also include a failsafe circuit that provides a high-level output within 250 microseconds after loss of the input signal. The most common causes of signal loss are disconnected cables, shorted lines, or the absence of any active transmitters on the bus. This feature prevents noise from being received as valid data under these fault conditions. This feature may also be used for Wired-Or bus signaling.

The SN65HVD2X devices are characterized for operation over the temperature range of -40°C to 85°C .

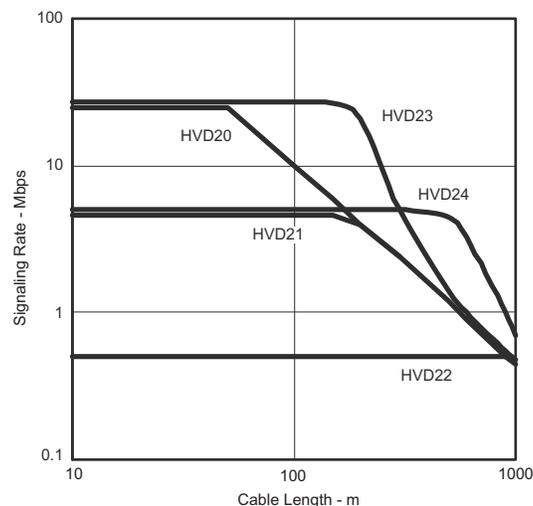


Figure 1. HVD2x Application Space

2.2 TPS61220

The TPS6122x family devices provide a power-supply solution for products powered by either a single-cell, two-cell, or three-cell alkaline, NiCd or NiMH, or one-cell Li-Ion or Li-polymer battery. Possible output currents depend on the input-to-output voltage ratio. The boost converter is based on a hysteretic controller topology using synchronous rectification to obtain maximum efficiency at minimal quiescent currents. The output voltage of the adjustable version can be programmed by an external resistor divider, or is set internally to a fixed output voltage. The converter can be switched off by a featured enable pin. While being switched off, battery drain is minimized. The device is offered in a 6-pin SC-70 package (DCK) measuring 2 mm x 2 mm to enable small circuit layout size.

The TPS6122x family of devices is characterized for operation over the temperature range of -40°C to 85°C .

3 Block Diagram

The RS-485 BoosterPack block diagram is shown in [Figure 2](#).

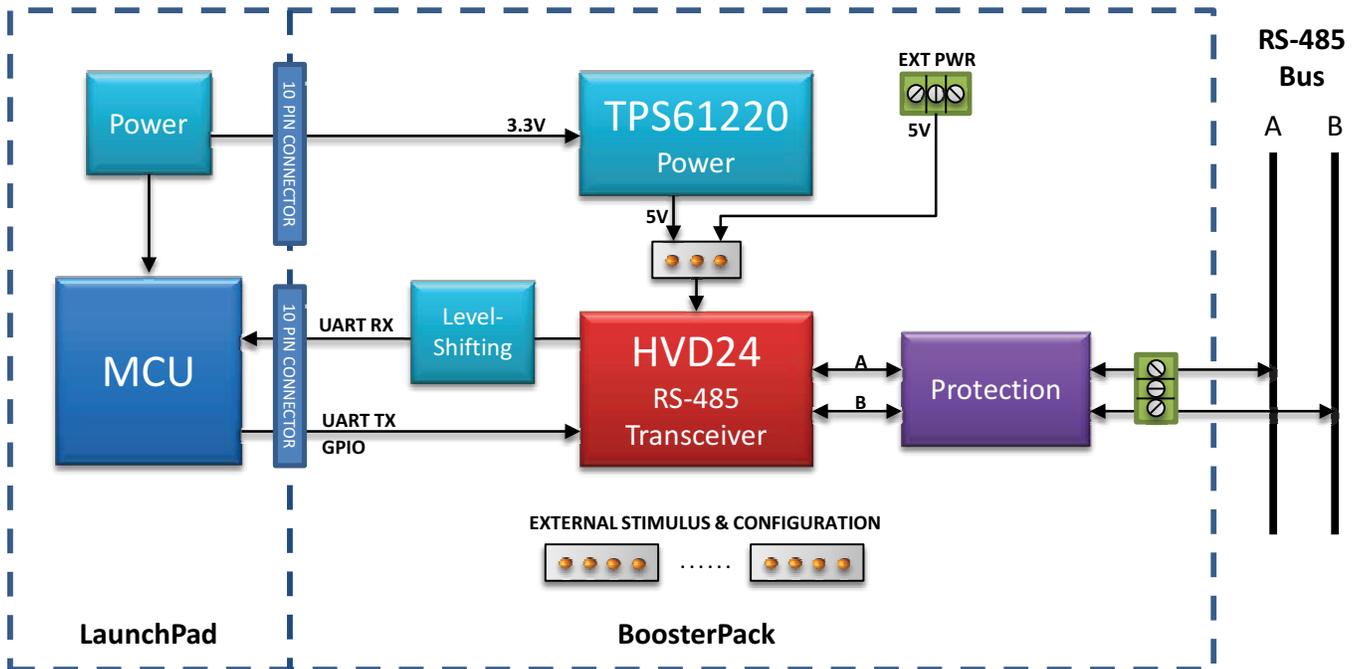


Figure 2. BoosterPack Block Diagram

3.1 Highlighted Products

The RS-485 BoosterPack features the following devices:

- **SN65HVD24**
 - Extended common-mode RS-485 transceiver with receiver equalization
- **TPS61220**
 - Low input voltage, 0.7-V boost converter with 5.5- μ A quiescent current

For more information on each of these devices, see the respective product folders at www.TI.com.

3.1.1 SN65HVD24

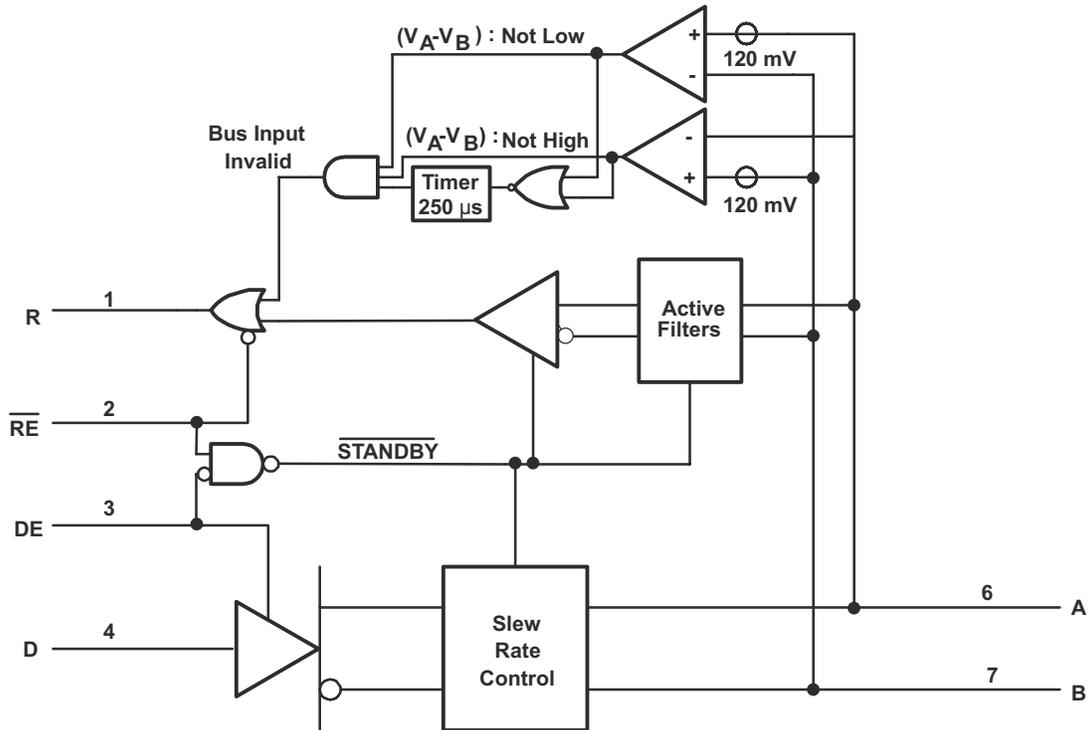
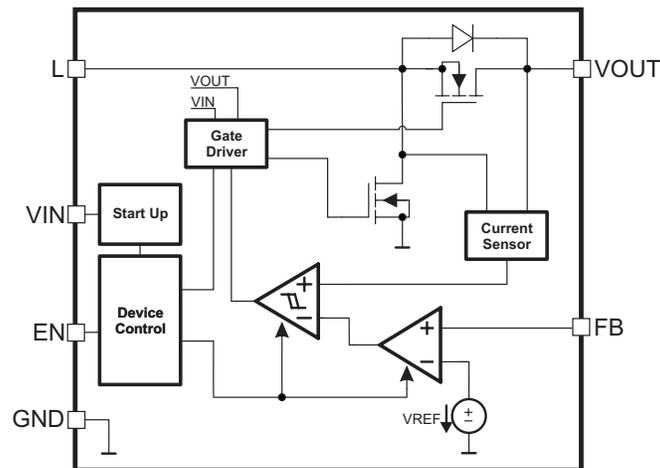


Figure 3. SN65HVD24 Functional Block Diagram

- Common-Mode Voltage Range (–20 V to 25 V) More Than Doubles TIA/EIA-485 Requirement
- Receiver Equalization Extends Cable Length at Faster Signaling Rates (HVD23, HVD24)
- Reduced Unit-Load for up to 256 Nodes
- Bus I/O Protection to Over 16-kV HBM
- Failsafe Receiver for Open-Circuit, Short-Circuit and Idle-Bus Conditions
- Low Standby Supply Current 1- μ A Max
- More Than 100 mV Receiver Hysteresis

3.1.2 TPS61220

Figure 4. TPS61220 Functional Block Diagram

- Up to 95% Efficiency at Typical Operating Conditions
- 5.5 μ A Quiescent Current
- Startup Into Load at 0.7 V Input Voltage
- Operating Input Voltage from 0.7 V to 5.5 V
- Pass-through Function during Shutdown
- Minimum Switching Current 200 mA
- Protections:
 - Output Overvoltage
 - Overtemperature
 - Input Undervoltage Lockout
- Adjustable Output Voltage from 1.8 V to 6 V
- Fixed Output Voltage Versions
- Small 6-pin SC-70 Package

4 System Design Theory

This section gives a brief discussion about important aspects of the RS-485 standard. The section then describes the thought process followed during the design of the RS-485 BoosterPack.

4.1 RS-485 Introduction

In 1983, the Electronics Industries Association (EIA) approved a new balanced transmission standard called RS-485. Finding widespread acceptance and usage in industrial, medical, and consumer applications, RS-485 has become the industry's interface workhorse.

RS-485 is an electrical-only standard. In contrast to complete interface standards, which define the functional, mechanical, and electrical specifications, RS-485 only defines the electrical characteristics of drivers and receivers that could be used to implement a balanced multipoint transmission line.

This standard, however, is intended to be referenced by higher level standards, such as DL/T645, for example, which defines the communication protocol for electronic energy-meters in China, specifying RS-485 as the physical layer standard.

Key features of RS-485 are:

- Balanced interface
- Multipoint operation from a single 5-V supply
- -7-V to +12-V bus common-mode range
- Up to 32 unit loads
- 10-Mbps maximum data rate (at 40 feet)
- 4000-foot maximum cable length (at 100 kbps)

RS-485 is well suited for long-distance networking in noisy environments. One reason for this is that RS-485 drivers provide a differential output of a minimum 1.5 V across a 54-Ω load, whereas receivers detect a differential input down to 200 mV. This provides sufficient margin for a reliable data transmission even under severe signal degradation across the cable and connectors.



Figure 5. RS-485 Specified Minimum Bus Signal Levels

Differential signaling over twisted-pair cable also benefits RS-485 applications because noise from external sources couples equally into both signal lines as common-mode noise, which is rejected by the differential receiver input.

The RS-485 standard suggests that its nodes be networked in a daisy-chain, also known as party line or bus topology (see Figure 6). In this topology, the participating drivers, receivers, and transceivers connect to a main cable trunk by way of short network stubs. The interface bus can be designed for full-duplex or half-duplex transmission (see Figure 7).

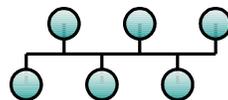


Figure 6. RS-485 Bus Structure

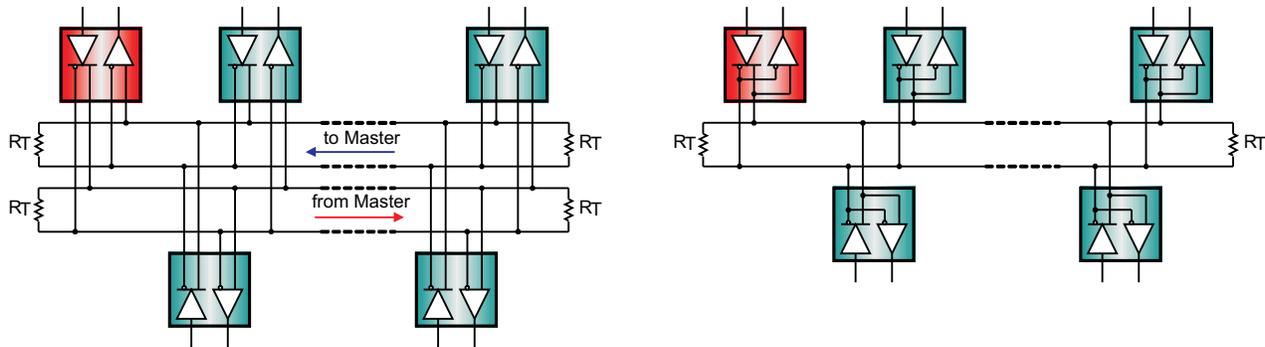


Figure 7. Full-duplex and Half-duplex Bus Structures in RS-485

Data transmission lines should always be terminated and stubs should be as short as possible to avoid signal reflections on the line. Proper termination requires the matching of the terminating resistors, R_T , to the characteristic impedance, Z_0 , of the transmission cable. Because the RS-485 standard recommends cables with $Z_0 = 120 \Omega$, the cable trunk is commonly terminated with 120- Ω resistors, one at each cable end.

The maximum bus length is limited by the transmission line losses and the signal jitter at a given data rate.

4.2 Transceiver Selection

The key requirements for the transceiver used on the RS-485 BoosterPack were:

- Data rate up to 1.2 Mbps
- Cable length up to 1000 feet
- Total number of nodes up to 32
- Half-duplex support, no bus isolation
- Temperature rating of -40 to 85°C

The SN65HVD24 extended common-mode RS-485 transceiver is well suited for meeting the specifications of this design.

The SN65HVD24 only supports 5-V outputs, therefore the receive output pin, R, of the SN65HVD24 must be level-shifted to meet the 3.3-V levels of the MCU. A Schottky diode and two pull-up resistors are used to implement a simple level-shifter. When the transceiver pin is high, the diode will be reverse bias and the 3.3-V pull-up will drive the input to the MCU. When the transceiver pin is low, the diode will be forward bias and the voltage on the MCU pin will be equal to the forward voltage of the diode.

The SN65HVD24 input pins (D, DE, and $\overline{\text{RE}}$) support both 3.3-V and 5-V levels, therefore level-shifting is not required and these pins can be connected directly to the MCU.

Figure 8 shows the final connection of the transceiver on the RS-485 BoosterPack.

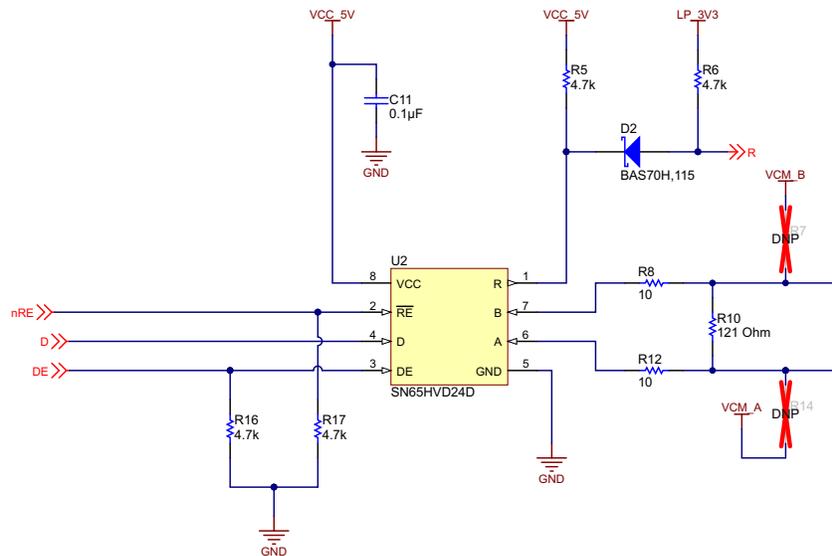


Figure 8. Transceiver Final Design

4.3 Power Supply Design

The key requirements for the power supply on the RS-485 BoosterPack were:

- Ability to power from the 3.3-V supply on the TI LaunchPad
- Ability to bypass on-board power supply and use 5-V external power source

Sections [Section 4.3.1](#) through [Section 4.3.2](#) detail the component selection and design process followed to meet these requirements.

4.3.1 Boost Converter Design

A boost converter was used to derive the 5-V source needed for the transceiver from the existing 3.3-V supply provided by the TI LaunchPad.

The TPS6122x family of switching boost converters offers the following features relevant to the design of the RS-485 BoosterPack:

- Up to 95% efficiency at typical operation conditions
- Operating input voltage from 0.7 V to 5.5 V
- Minimum switching current 200 mA
- Adjustable output voltage from 1.8 V to 6 V

The application circuit for an adjustable output voltage boost converter is shown in [Figure 9](#).

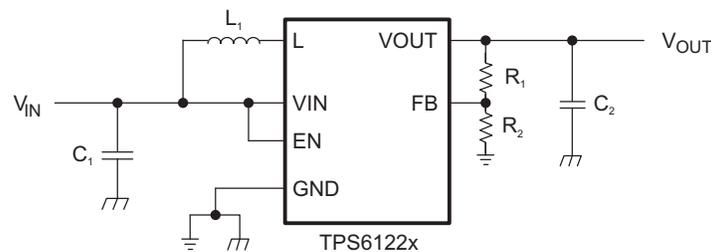


Figure 9. Application Circuit For Adjustable Output Voltage Option

4.3.1.1 Output Voltage Selection

The TPS61220 has an adjustable output voltage from 1.8 V to 6 V. An external resistor divider (R_1 and R_2) is used to select the output voltage as shown in Figure 9. When the output voltage is regulated properly, the typical voltage value at the FB pin is 500 mV for the adjustable devices. The recommended value for R_2 should be lower than 500 k Ω , in order to set the divider current to 1 μ A or higher. The value of the resistor R_1 can be calculated using the feedback voltage, V_{FB} , the desired output voltage, V_{OUT} , and Equation 1:

$$R_1 = R_2 \times \left(\frac{V_{OUT}}{V_{FB}} - 1 \right)$$

$$R_1 = 200 \text{ k}\Omega \times \left(\frac{5 \text{ V}}{500 \text{ mV}} - 1 \right)$$

$$R_1 = 1.8 \text{ M}\Omega \tag{1}$$

4.3.1.2 Inductor Selection

A 4.7 μ H inductor was selected for this design as recommended by the boost converter data sheet. This value shows a good performance over the whole input voltage range.

4.3.1.3 Capacitor Selection

The boost converter data sheet recommends a small ceramic capacitor placed as close as possible to the VOUT and GND pins of the boost converter. The data sheet requires a capacitor value at least half the inductance value of L_1 . A value of 10 μ F was selected for this design as recommended by the boost converter data sheet.

4.3.1.4 Boost Converter Final Implementation

The final implementation is shown in the snapshot of the RS-485 BoosterPack schematic shown Figure 10.

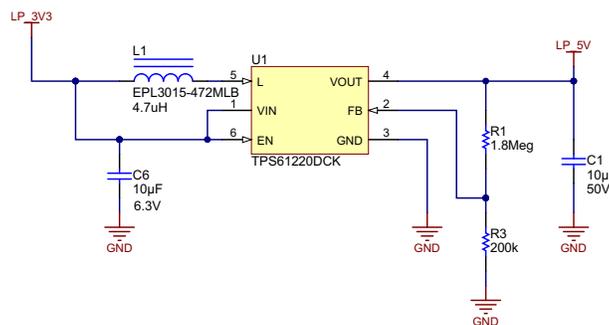


Figure 10. Power Supply Implementation

4.3.2 External Power and Source Configuration

A terminal block was used to allow for an external 5-V power supply source to provide power to the RS-485 BoosterPack. Filtering capacitors were added to clean the external power source. A jumper is used to select between the boost converter power source and the external power source. An LED indicates the presence of 5-V power on the board.

Figure 11 and Figure 12 show the final implementation of these two features.

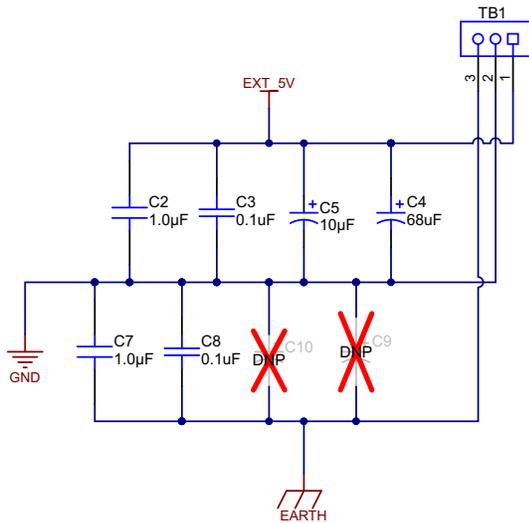


Figure 11. External Power Supply Implementation

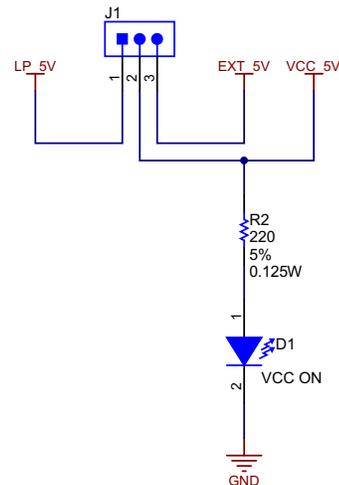


Figure 12. Power Source Selection and Power Indicator

4.4 ESD, Surge, and Transient Protection

Two Bourns® transient voltage suppressor (TVS) diodes were selected for surge and ESD protection on the RS-485 bus lines. The TVS diodes are designed to meet IEC 61000-4-2 (ESD), IEC 61000-4-4 (EFT) and will assist in meeting IEC 61000-4-5 (Surge) requirements. Each diode is rated up to ±30-kV ESD protection for both contact and air discharge. Both diodes support a working peak voltage of 24 V and are temperature rated from -55°C to 150°C.

Figure 13 shows the ESD, surge, and transient protection design of the RS-485 BoosterPack.

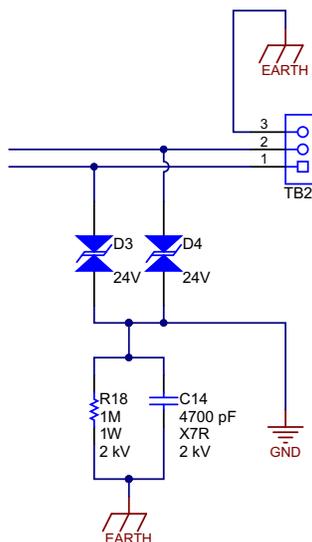


Figure 13. ESD, Surge and Transient Protection

5 Hardware Overview

5.1 BoosterPack Setup and Precautions

Figure 31 shows the schematic of the RS-485 BoosterPack. The BoosterPack has headers labeled from J1 to J20 and two 3-pin terminal blocks labeled TB1 and TB2. These headers support a wide range of system configurations. The BoosterPack can be used with a 20- or 40-pin TI LaunchPad or standalone.

NOTE: The RS-485 BoosterPack is populated with the SN65HVD24 extended common-mode RS-485 transceiver. However the transceiver can easily be removed and replaced with any TI half-duplex, 8-pin SOIC RS-485 transceiver. This allows the system designer to evaluate many different transceivers with varying performance targets. The setup instructions and performance data in this document refer to the SN65HVD24.

5.1.1 Using the BoosterPack with a TI LaunchPad

The RS-485 BoosterPack has been designed to interface with a 20- or 40-pin TI Launchpad. The BoosterPack can be powered directly from the 3.3-V supply provided by the BoosterPack. Two UART pins and two GPIO pins are used to interface to the RS-485 transceiver. The pin-out for the BoosterPack is shown in Table 2.

Table 2. RS-485 BoosterPack Connector Pin-Out

J13		J14	
1	LP_3V3	1	GND
2	NC	2	NC
3	R	3	NC
4	D	4	NC
5	DE	5	NC
6	NC	6	NC
7	NC	7	NC
8	\overline{RE}	8	NC
9	NC	9	NC
10	NC	10	NC

Refer to the TI LaunchPad documentation to determine the correct orientation of the BoosterPack before connecting the two boards together. Use J10, J12, J19, and J20 to connect the MCU pins to the transceiver pins. Use J1 to select between LaunchPad power and external power for the BoosterPack. Jumpers J2, J4, J8, and J15 must be disconnected to avoid contention with the MCU pins.

For proper operation, the MCU must meet the high-level input voltage $V_{IH} \geq 2$ V and the low-level input voltage $V_{IL} \leq 0.8$ V specification of the transceiver input pins. The BoosterPack implements a level-shifter on the transceiver output pin to generate a 3.3-V signal back to the MCU.

5.1.2 Using the BoosterPack Standalone

With the use of an external power supply and a signal generator, the RS-485 BoosterPack can be used independently of the TI LaunchPad.

The terminal block TB1 is used to connect an external power supply unit (PSU) to the BoosterPack. Jumpers J4, J8, and J15 can be used to control the input signals of the transceiver.

- TB1, Pin 1 (EARTH) is a second ground pin that allows applying an external voltage between GND and EARTH to simulate common-mode voltage conditions.
- TB1, Pin 2 (GND) is connected to the negative output or ground terminal of the PSU. This pin represents the ground potential of the device-under-test and the entire RS-485 BoosterPack. It also connects to various jumpers on the board.
- TB1, Pin 3 (VCC) is connected to the positive output of a regulated power supply unit (PSU) as it represents the positive supply voltage of the device-under-test and also connects to various jumpers on the board.

For the most measurements, the common-mode simulation is not needed and EARTH can be connected to GND through a wire-bridge between pin 1 and pin 2 of TB1.

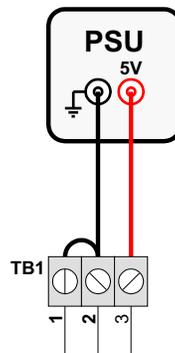


Figure 14. Bridging DUT_GND with EARTH_GND

While J4, J8, and J15 are stimulation points, or headers through which the control and data signals for the RS485 BoosterPack are applied, J3, J5, J9, and J16 are probe points, or headers at which transceiver signals can be measured.

Note that the 50-Ω resistors, R11, R19, and R21, have the index DNP, indicating that these components are not assembled. Because signal generators have a typical source impedance of 50 Ω, their output signal is twice the required signal voltage, and assumes that the on-board 50-Ω resistors divide this voltage down to the correct signal level.

Without these resistors; however, this voltage divider action is not accomplished, and the generator output voltage must be reduced to match the VCC requirements of the RS-485 device.

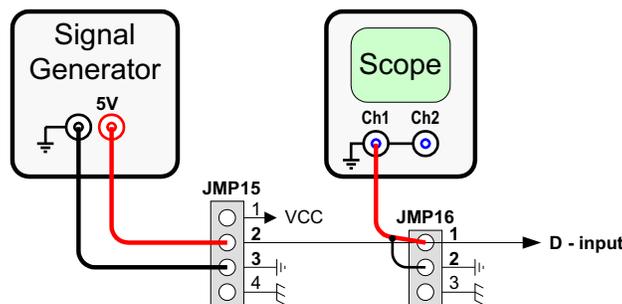


Figure 15. Example of Stimulus and Probe Points with JMP4 and JMP14

Figure 15 gives an example for entering a data signal into the driver section of the transceiver. The signal output of the generator is adjusted to match the device VCC power supply requirements. The generator's ground terminal is connected with pin 3, and the signal output terminal with pin 2 of J15. The data signal is measured through an oscilloscope with its signal input connected to pin 1 and its ground wire connected to pin 2 of J16.

The same setup applies to the DE and $\overline{\text{RE}}$ inputs through their corresponding headers J8 and J9 and J4 and J5. J2 however, must not receive a signal stimulus. Like J3, it represents the receiver output, R, of the half-duplex RS-485 device.

When using a TI LaunchPad the non-assembled 50- Ω resistors are of no concern. However, for proper operation, it must be assured that the high-level input voltage $V_{\text{IH}} \geq 2 \text{ V}$ and the low-level input voltage $V_{\text{IL}} \leq 0.8 \text{ V}$.

5.2 Powering Up the BoosterPack and Taking Measurements

Follow the procedure below for taking measurements on the RS-485 BoosterPack:

1. Install the required ground connections.
2. Connect the oscilloscope with the respective probe points you want to measure.
3. Configure J1 to power BoosterPack from external PSU or TI LaunchPad.
4. If using TI Launchpad, populate J10, J12, J19, and J20 accordingly to have the MCU drive the transceiver pins.
5. If using external signal generator, connect signal generator to J15 and use J4 and J8 to tie off the transceiver control pins.
6. Turn on the external PSU or TI LaunchPad and observe the blue LED (D1) turning on.

Figure 16 shows two RS-485 BoosterPacks setup for a standard measurement configuration. The BoosterPack on the right is configured as a transmitter with a signal generator driving the D-input terminal. The BoosterPack on the left is configured as a receiver. An oscilloscope is used to monitor the output of the receiver.

Section 5.2.1 and Section 5.2.2 give two configuration examples for the transceiver.

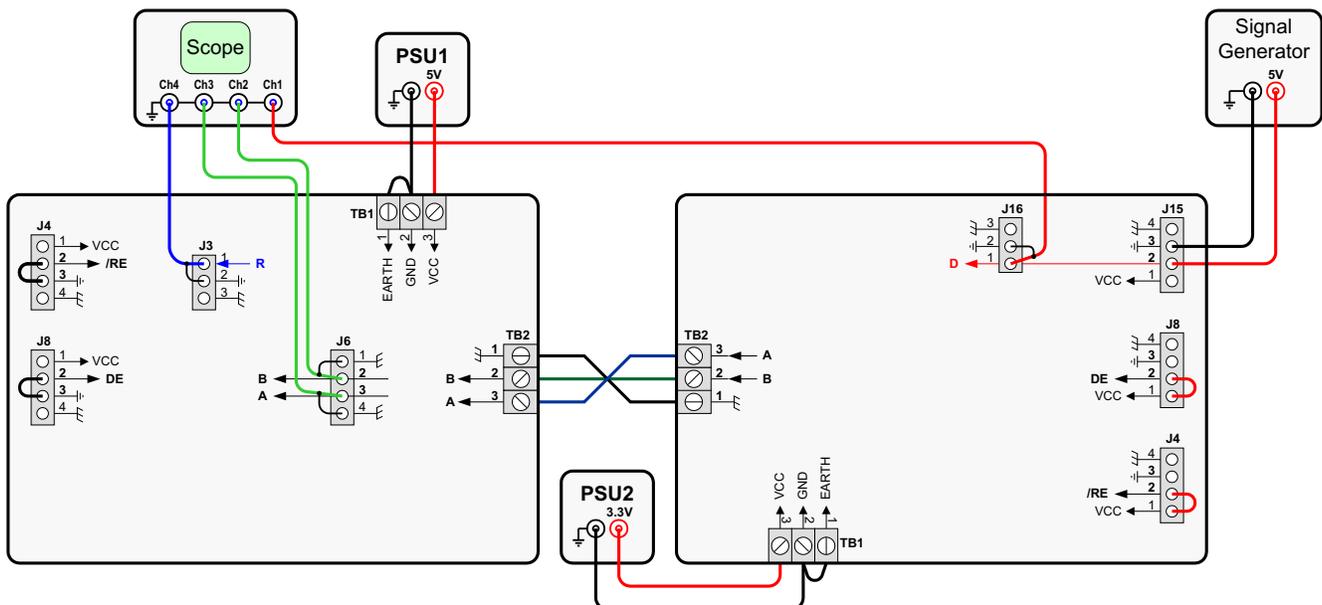


Figure 16. RS-485 BoosterPack Setup for Standard Measurement Configuration

5.2.1 Example 1: Standard Transceiver Configuration

Normal transceiver operation requires both the driver and the receiver sections being active. Therefore, the receiver enable pin (\overline{RE}) must be at logic low potential and the driver enable pin (DE) at logic high.

As shown in Figure 17, transmit data entering at the D-input terminal appear as the differential output voltage ($V_{OD} = V_A - V_B$) on the bus wires, A and B. By way of the active receiver, it is possible to sense the data traffic in transmit direction.

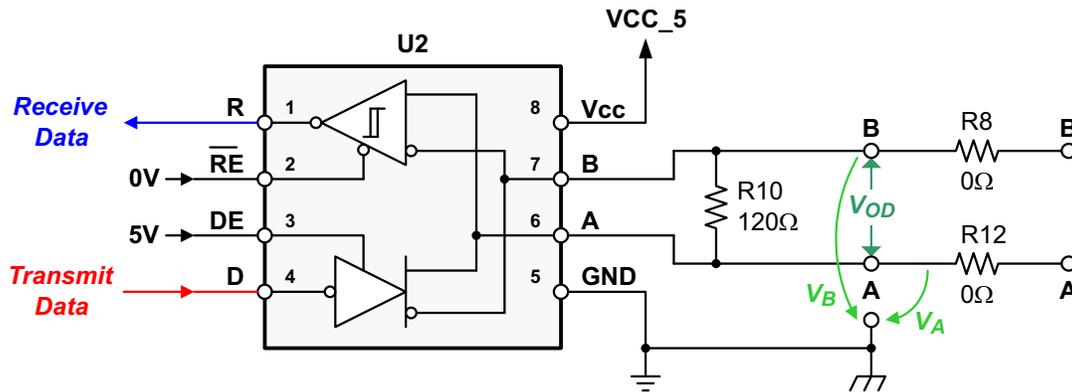


Figure 17. Transceiver Configuration for Normal Operation

Figure 17 shows the RS-485 BoosterPack setup for normal transceiver operation. EARTH and GND receive the same reference potential, PSU-ground, through the wire-bridge from pin 1 to pin 2 at the terminal block, TB1, while pin 3 (VCC) is connected to the 5-V output of a power-supply unit (PSU).

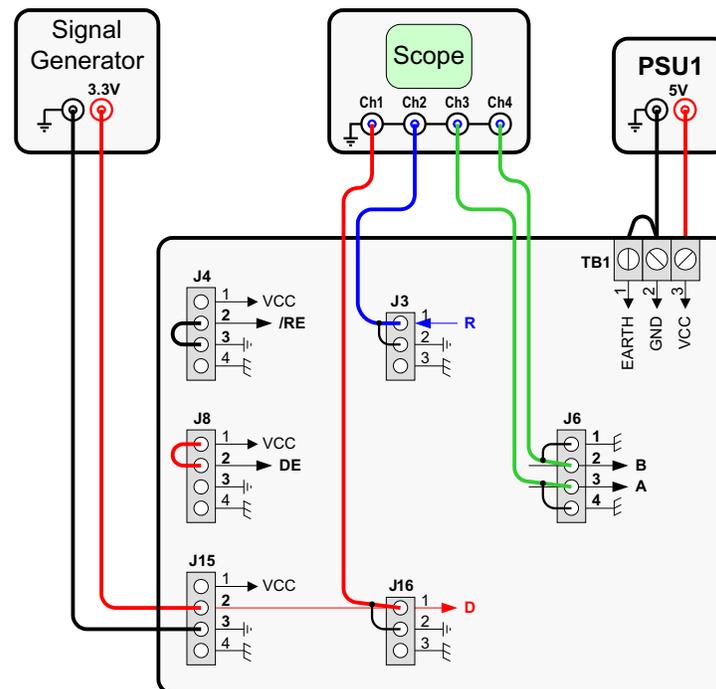


Figure 18. RS-485 BoosterPack Setup for Normal Transceiver Operation

The low potential for \overline{RE} is provided by the wire-bridge from pin 2 to pin 3 at J4, and the high potential for DE through a wire-bridge from pin 2 to pin 1 at J8. Data from the signal generator enter the board at pin 2 and pin 3 of J15. This data is measured by way of channel 1, which is connected to pin 1 and pin 2 of J16. Channel 2 measures the receive data at J3, and channels 3 and 4 the bus voltages, V_A and V_B , at J6.

5.2.2 Example 2: Operation Under Maximum Load

EIA-485 (RS-485) specifies three maximum load parameters: a maximum differential load of $60\ \Omega$, a maximum common-mode load of $375\ \Omega$ for each bus wire, and a receiver common-mode voltage range from $-7\ \text{V}$ to $+12\ \text{V}$. Figure 19 reflects these requirements through R10, R8, R12, and VCM. Note that under maximum load conditions the transceiver must be capable of sourcing and sinking bus currents of up to 55 mA. The purpose of this test is to show the robustness of V_{OD} over the entire common mode voltage range at maximum load.

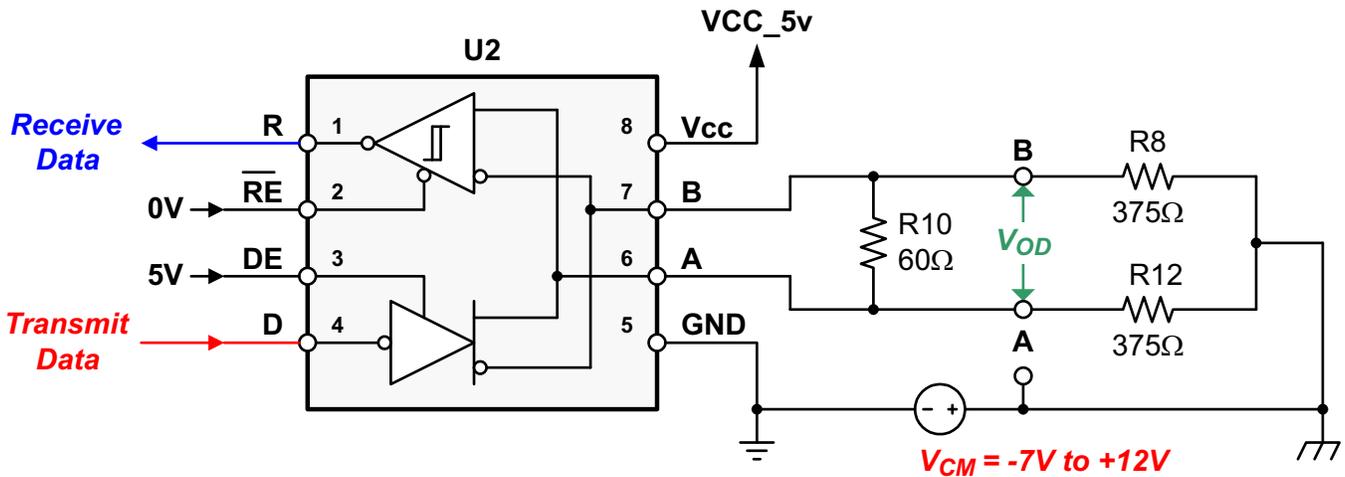


Figure 19. Configuration for Maximum Loading

While the cable connections of the signal generator and the oscilloscope remain the same as in the previous example, the following board changes need to be implemented to reflect maximum load conditions:

- replace R10 (120- Ω default) with 60 Ω
- replace R8 and R12 (0- Ω default) with 375 Ω
- connect pin 2 of J7 with pin 1 and pin 3 with pin 4
- replace the previous wire-bridge at TB1 with a second power supply unit (PSU2) and connect the ground terminals of both, PSU1 and PSU2 with a wire-bridge

Figure 20 shows the RS-485 BoosterPack setup for maximum loading.

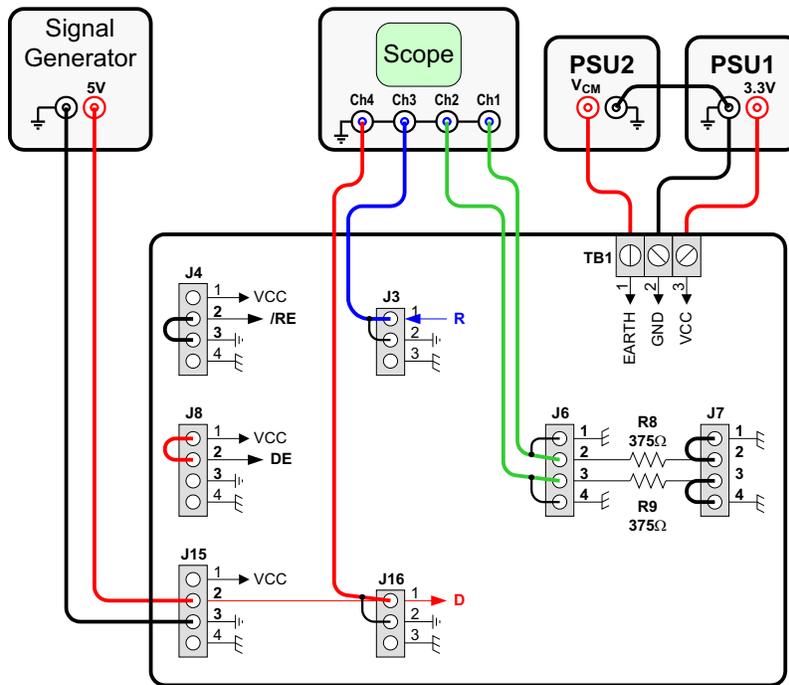


Figure 20. RS-485 BoosterPack Setup for Maximum Loading

Note that [Figure 20](#) only shows the wiring of PSU2 for positive common-mode voltages. For negative V_{CM} , connect the ground terminal of PSU2 with pin 1 of TB1 (EARTH), and the V_{CM} -output of PSU2 with the ground terminal of PSU1.

6 Test Data

6.1 System Performance Test

The performance of the RS-485 BoosterPack was verified through a live test. A total of 33 nodes were wired to a single bus using CAT5e cable. The nodes were equidistant from each other at 32 feet, for a total of 1024 feet of wire. [Figure 21](#) shows a picture of the setup used for the live test.

At the beginning of the bus, a sender node was connected directly to a pseudo-random bit sequence (PRBS) generator. At the end of the bus, a receiver node was connected to an oscilloscope such that the data output of the transceiver could be observed. The receiver node was terminated with a 120 Ohm resistor. All nodes were powered from a single bench-top power supply providing 5 V. None of the nodes were connected to a TI LaunchPad for this test.

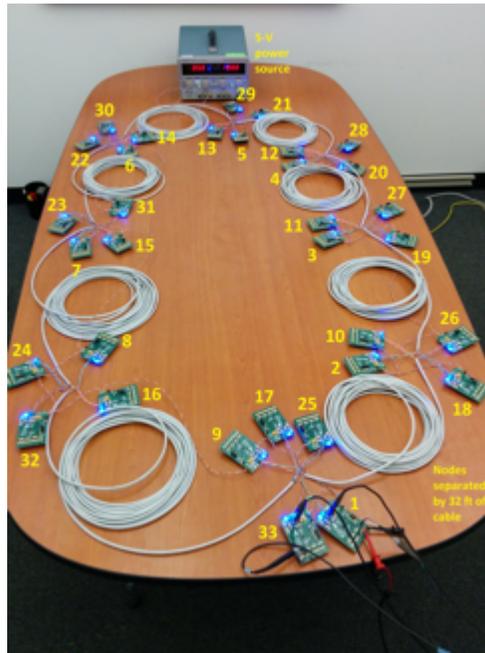


Figure 21. RS-485 Test Setup

In the test setup, 256 feet of CAT5e cable was cut into eight 32-foot segments. Since CAT5e cable consists of four twisted pairs of wires, each of these segments carried enough wire for 128 feet of RS-485 bus. Each twisted pair was used carry the A and B line of the RS-485 bus. All nodes are separated by a 32-foot segment of twisted pair wire. [Figure 22](#) shows the cross-section of CAT5e cable used for the live test.

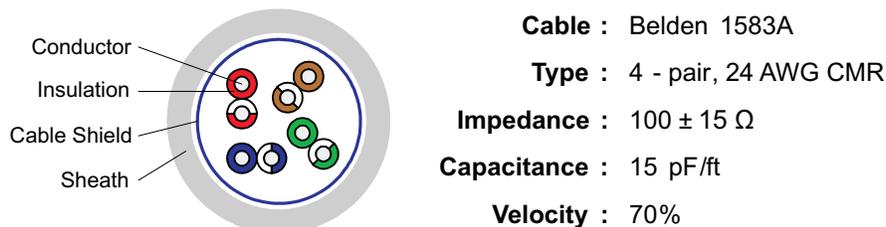


Figure 22. CAT5e Cable Cross-Section and Specifications

6.1.1 Eye Diagrams and Output Jitter Measurements

The test setup was used to collect eye diagrams and output jitter measurements. The output of the transceiver on the receiver node was measured directly on the pins of the device using a single-ended oscilloscope probe. This reduced the inductance of the probe which eliminates overshoot/undershoot spikes on the signal. The output of the transceiver was also measured at the output of the level shifter; see Section 6.1.2 for more details.

Figure 23 shows the eye diagram of the differential signals on the bus at the input to the receiver node with a PRBS data rate of 3 Mbps (channel 3). The output of the transceiver at the receiver node is also shown (channel 4). Figure 24 shows the output jitter measurement for the same setup. At this data rate, the transceiver was able to achieve 5.6 ns jitter, which corresponds to an eye opening of over 98%.

$$\text{eye_opening} = \left(1 - \frac{\text{output_jitter}}{\text{data_period}} \right) \times 100\%$$

$$\text{eye_opening} = \left(1 - \frac{5.6}{333.33} \right) \times 100\%$$

$$\text{eye_opening} = 98.32\%$$

(2)

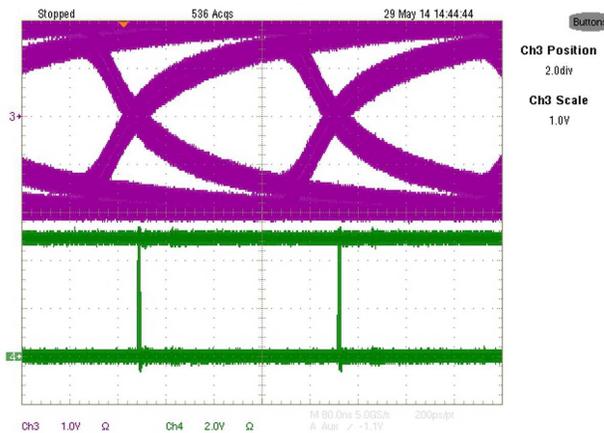


Figure 23. Eye Diagram at 3-Mbps Data Rate Over 1024 Feet of Cable

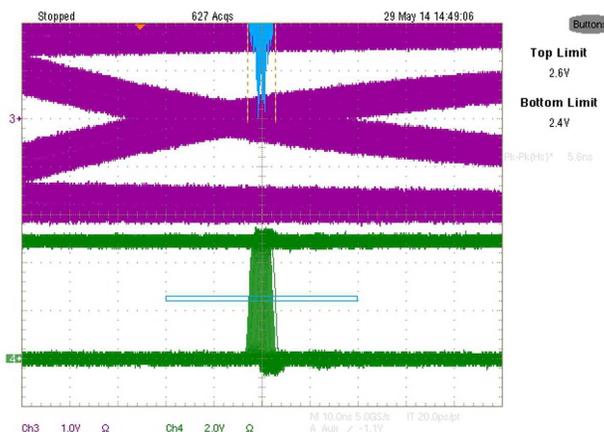


Figure 24. Output Jitter at 3-Mbps Data Rate Over 1024 Feet of Cable

The next goal was to increase the PRBS data rate to the point at which the output jitter stayed within 80% of the UI. The data rate was incremented to 12.5 Mbps, at which point the jitter was 17 ns, giving an eye opening close to 79%.

$$\text{eye_opening} = \left(1 - \frac{\text{output_jitter}}{\text{data_period}} \right) \times 100\%$$

$$\text{eye_opening} = \left(1 - \frac{17}{80} \right) \times 100\%$$

$$\text{eye_opening} = 78.5\%$$

(3)

Figure 25 shows the jitter measurement performed at 12.5 Mbps.

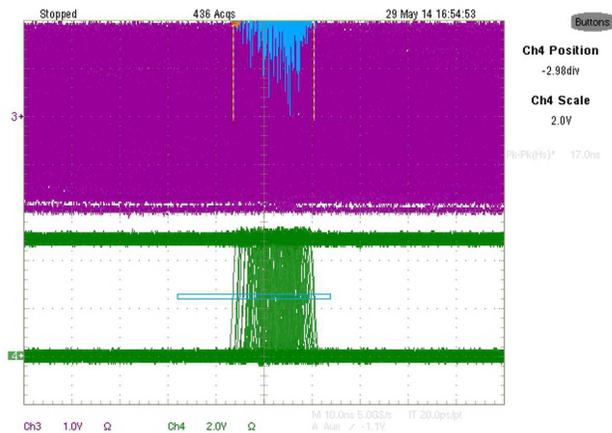


Figure 25. Output Jitter at 12.5-Mbps Data Rate Over 1024 Feet of Cable

The results indicate that the transceiver is able to extract a good signal from an eye that was completely “closed” at the input of the bus.

Although the output of the transceiver produced good results at high speeds, it should be noted that the final data rate supported on a full system will depend on several factors. One factor is the maximum data rate supported by the MCU serial port. The other factor is the performance of the level-shifting logic used to translate the 5-V output of the transceiver to the 3.3-V input required by the MCU. The performance of the level-shifting logic used on the BoosterPack is discussed in the next section.

6.1.2 Level-Shifter Performance

The level-shifter used in the RS-485 BoosterPack was adequate for the target data rate of 1.25 Mbps. However, at higher data rates, the slow rise time of the circuit started to degrade the output signal from the transceiver.

Figure 26 shows the output of the transceiver on the receiver node at a PRBS data rate of 1.25 Mbps (channel 4), the target data rate for the design. The differential bus signal at the input to receiver node is also shown (channel 3). The output of the transceiver is clean, with small rise/fall times and no overshoot/undershoot spikes.

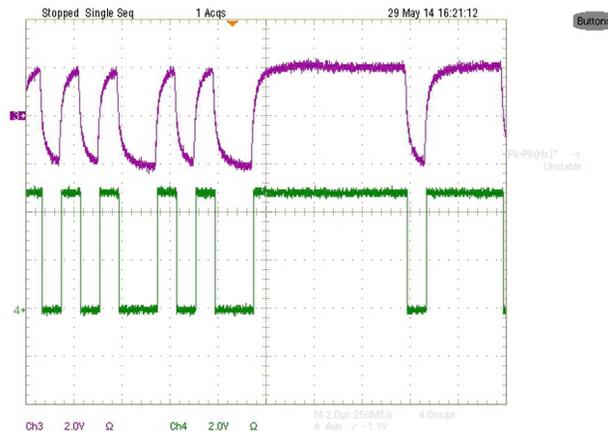


Figure 26. Transceiver Output at 1.25-Mbps

Figure 27 shows the output of the level-shifter on the receiver node at 1.25 Mbps (channel 4). The output of the level-shifter shows a slow rise time.



Figure 27. Level-Shifter Output at 1.25-Mbps

6.2 IEC Tests

The RS-485 BoosterPack was submitted to IEC61000-4-4 EFT, IEC61000-4-5, and IEC61000-4-2 tests. [Table 3](#) summarizes the results from those tests. [Section 6.2.1](#), [Section 6.2.2](#), and [Section 6.2.3](#) provide more details on the test setup and results.

Table 3. IEC61000 Test Results

Immunity Test	Standard	Port	Target Voltage	Target Level	Result
Burst (EFT)	IEC 61000-4-4: (5 kHz / 15 ms duration through capacitive clamp)	Signal lines	±2 kV	4	Pass, Class C
Surge	IEC 61000-4-5: (1.2 / 50 μs–8 / 20 μs), 42 Ω–0.5 μF	Signal lines	±0.5 kV	1	Pass, Class C
ESD	IEC 61000-4-2, contact	Signal lines	±8 kV	4	Pass, Class C

6.2.1 IEC61000-4-4 EFT Test

The IEC61000-4 electrical fast transients (EFT) test consists of coupling electrical bursts into the power supply, control, and signal ports of electronic equipment. The goal of the test is to demonstrate immunity to transient disturbances caused by interruption of inductive loads, relay contact bounce, and so on.

The setup for this test consisted of two nodes connected together through approximately 2.5 meters of Belden 1583A CAT5e cable. Each node consisted of an RS-485 BoosterPack and an MSP-EXP430G2 LaunchPad. The “sender” node was configured for continuous data transmission, while the “receiver” node continuously verified the received data. During the test the receiving node flashed a green LED to indicate correct data reception and red LED to indicate incorrect data reception. The receiver node was set up as the equipment under test (EUT). The EFT bursts were coupled into the CAT5e cable through a capacitive coupling clamp.

[Figure 28](#) shows the test setup used for IEC61000-4 EFT tests.

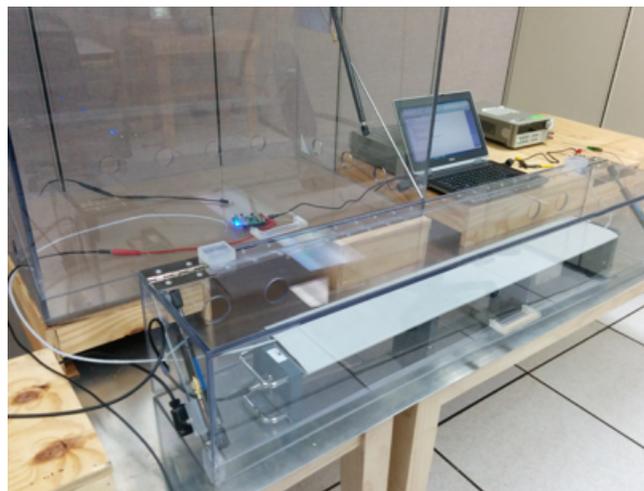


Figure 28. IEC61000-4-4 EFT Test Setup

The test results show the EUT was able to withstand up to ±2 kV bursts for 60 seconds. The EUT indicated data error during the test and in some cases had to be reset to regain functionality. However, the EUT was not permanently damaged. The result was noted as passing with Class C.

Class C accepts loss of function, such as a latch-up event, but without device damage. Per Class C, a manual restart or toggling of the power supply is necessary to return the system to normal operation after the test.

6.2.2 IEC61000-4-5 Surge Test

The IEC61000-4-5 surge test simulates switching transients caused by lightning strikes or the switching of power systems including load changes and short circuits. The test requires 5 positive and 5 negative surge pulses with a time interval between successive pulses of 1 minute or less.

The unshielded symmetrical data line setup as defined by the IEC61000-4-5 specification was used for this test. An RS-485 BoosterPack was connected to a test generator through a Belden 1583A CAT5e cable. The test generator was connected to another BoosterPack to simulate a two-node system. The test generator was configured for 1.2/50 μ s surges and diode clamps were used for line-to-ground coupling. A series of 5 negative and positive pulses, with 10 seconds spacing between each pulse, were applied during the test. After each test, the BoosterPacks were attached to MSP-EXP430G2 LaunchPads to verify functionality.

Figure 29 shows the test setup used for IEC61000-4-5 surge tests.

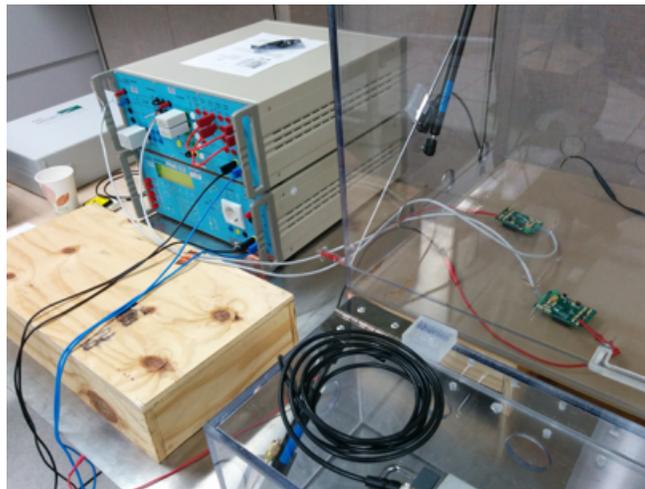


Figure 29. IEC61000-4-5 Surge Test Setup

The test results show the EUT was able to withstand up to ± 500 V bursts. The EUT was able to perform normally after each test. Because functionality could not be verified during the test, the result was noted as passing with Class C.

6.2.3 IEC61000-4-2 ESD Test

The IEC61000-4-2 electrostatic discharge (ESD) test simulates the electrostatic discharge of an operator directly onto an adjacent electronic component. Electrostatic charge usually develops in low relative humidity, and on low-conductivity carpets, or vinyl garments. To simulate a discharge event, an ESD generator applies ESD pulses to the equipment-under-test (EUT), which can happen through direct contact with the EUT (contact discharge), or through an air-gap (air-discharge).

The setup for this test consisted of two nodes connected together through a twisted pair cable. Each node consisted of an RS-485 BoosterPack and an MSP-EXP430G2 LaunchPad. The “sender” node was configured for continuous data transmission, while the “receiver” node continuously verified the received data. During the test the receiving node flashed a green LED to indicate correct data reception and red LED to indicate incorrect data reception. The receiver node was set up as the equipment under test (EUT). A series of 10 negative and positive pulses were applied directly on the RS-485 bus terminal block screws during the test (contact discharge).

Figure 30 shows the test setup used for IEC61000-4-2 ESD tests.

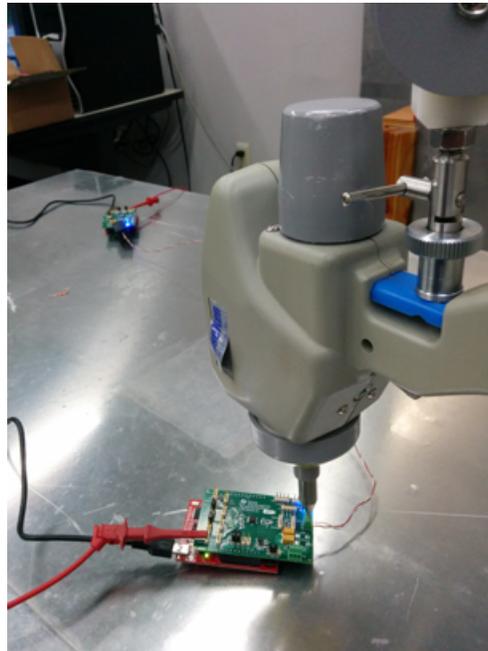


Figure 30. IEC61000-4-2 ESD Test Setup

The test results show the EUT was able to withstand up to ± 8 -kV discharges. The EUT indicated data error during the test and in some cases had to be reset to regain functionality. However, the EUT was not permanently damaged. The result was noted as passing with Class C.

7 Schematics

The schematics for the RS-485 BoosterPack are shown in [Figure 31](#).

To download the schematics, see the design files at [TIDA-00214](#).

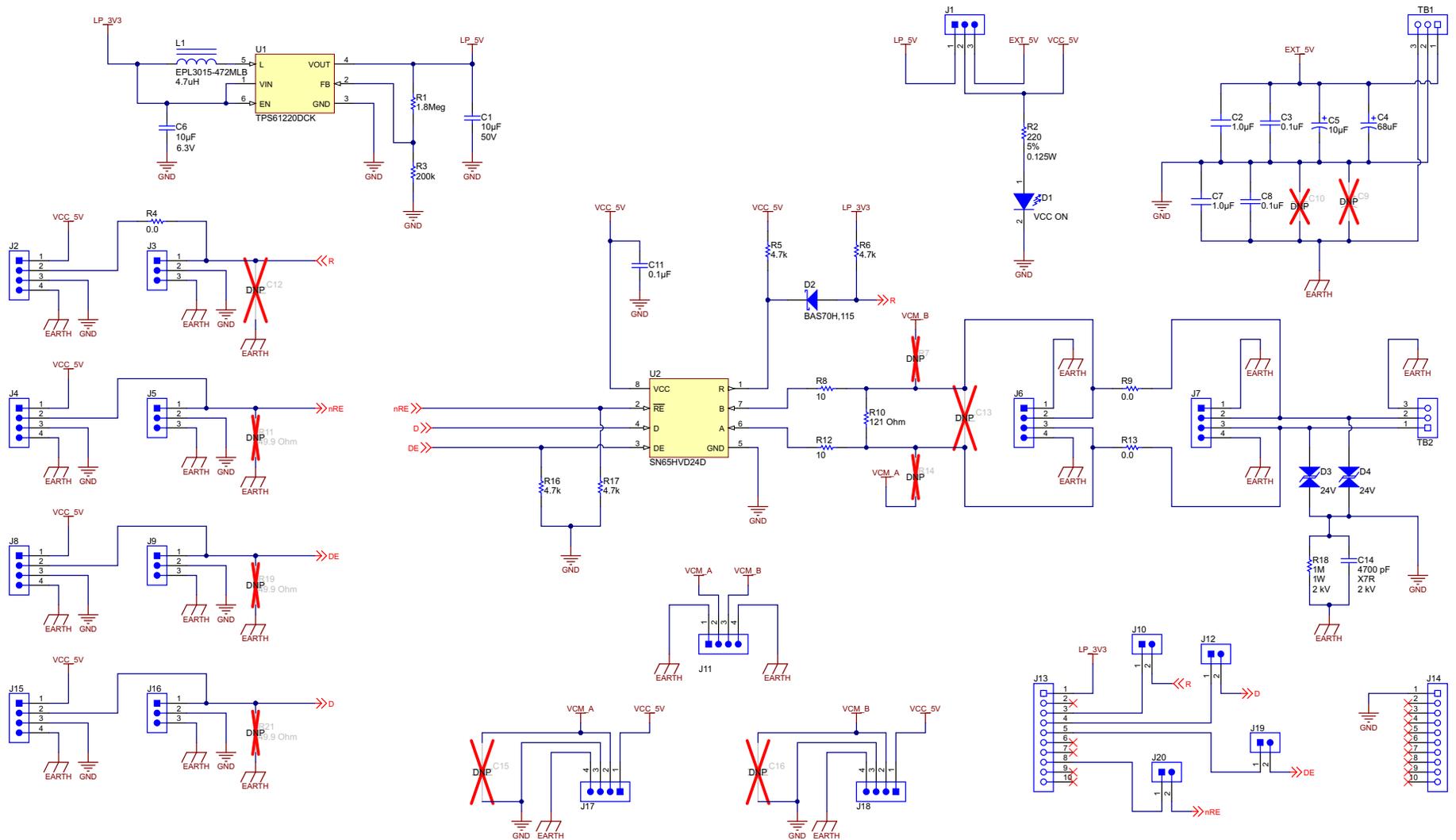


Figure 31. RS-485 BoosterPack Schematics

8 Bill of Materials

To download the bill of materials (BOM), see the design files at [TIDA-00214](#). Table 4 shows the BOM for the Half-Duplex, Non-Isolated RS-485 BoosterPack Reference Guide.

Table 4. BOM

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
IPC B1	1		Printed Circuit Board		ISE4015	Any
C1	1	10uF	CAP, CERM, 10uF, 50V, +/-10%, X7R, 1210	1210	GRM32ER71H106KA12L	MuRata
C2, C7	2	1.0µF	CAP CER 1UF 50V 10% X7R 0805	0805 (2012 Metric)	GRM21BR71H105KA12L	Murata Electronics North America
C3, C8	2	0.1uF	General Purpose Ceramic Capacitors	0805	C0805X7R500-104KNE	Venkel
C4	1	68uF	Low ESR Tantalum Capacitors		TA020TCR686KER	Venkel
C5	1	10µF	CAP TANT 10UF 50V 10% 2917	2917 (7343 Metric)	T495X106K050ATE300	Kemet
C6	1	10uF	CAP, CERM, 10uF, 6.3V, +/-20%, X5R, 0603	0603	GRM188R60J106ME47D	MuRata
C11	1	0.1µF	CAP, CERM, xxxF, xxV, [TempCo], xx%, [PackageReference]	0805 (2012 Metric)	C0805C104K5RACTU	Kemet
C14	1	4700pF	CAP, CERM, xxxF, xxV, [TempCo], xx%, [PackageReference]	1812 (4532 metric)	1812B472K202NT	Novacap
D1	1		VCC ON	2-SMD, No Lead, Exposed Pad	LTST-S220TBKT	Lite-On Inc
D2	1	1V @ 15mA	DIODE SCHOTTKY 70V 0.07A SOD123F	SOD-123F	BAS70H,115	NXP Semiconductors
D3, D4	2	24V	Diode, TVS, Bi, 24V, 350W, SOD-323	SOD-323	CDSOD323-T24C-DSL	Bourns
J1, J3, J5, J9, J16	5		Header, TH, 100mil, 3x1, Gold plated, 230 mil above insulator	3x1 Header	TSW-103-07-G-S	Samtec
J2, J4, J6, J7, J8, J11, J15, J17, J18	9		Header, TH, 100mil, 4x1, Gold plated, 230 mil above insulator	4x1 Header	TSW-104-07-G-S	Samtec
J10, J12, J19, J20	4		Header, TH, 100mil, 2x1, Gold plated, 230 mil above insulator	2x1 Header	TSW-102-07-G-S	Samtec
J13, J14	2		Samtec Socket Strip 10 POS 2.54mm Thru-Hole		SSW-110-23-F-S	Samtec Inc
L1	1	4.7uH	Inductor, Shielded, Ferrite, 4.7uH, 1.2A, 0.14 ohm, SMD	Inductor, 3x1.55x3mm	EPL3015-472MLB	Coilcraft
R1	1	1.8Meg	RES, 1.8Meg ohm, 5%, 0.063W, 0402	0402	CRCW04021M80JNED	Vishay-Dale
R2	1	220	RES, 220 ohm, 5%, 0.125W, 0805	0805	ERJ-6GEYJ221V	Panasonic
R3	1	200k	RES, 200k ohm, 5%, 0.063W, 0402	0402	CRCW0402200KJNED	Vishay-Dale
R4, R9, R13	3	0.0	RES 0.0 OHM 1/8W JUMP 0805 SMD	0805 (2012 Metric)	RC0805JR-070RL	Yageo
R5, R6, R16, R17	4	4.7k	RES, xxx ohm, x%, xW, [PackageReference] 0603	(1608 Metric)	RT0603FRE074K7L	Yageo
R8, R12	2	10	RES, xxx ohm, x%, xW, [PackageReference] 0603	(1608 Metric)	CRCW060310R0FKEAHP	Vishay Dale
R10	1	121 Ohm	RES 121 OHM 0.1W 1% 0805 SMD	0805 (2012 Metric)	CR0805-10W-1210FT	Venkel
R18	1	1M	RES, xxx ohm, x%, xW, [PackageReference]	2512 (6432 Metric)	HVC2512T1004JET	Ohmite
SH-J1, SH-J10, SH-J12, SH-J19, SH-J20	5	1x2	Shunt, 100mil, Gold plated, Black	Shunt	SNT-100-BK-G	Samtec
TB1, TB2	2		CONN TERM BLOCK 2.54MM 3POS		1725669	Phoenix Contact
U1	1		LOW INPUT VOLTAGE STEP-UP CONVERTER IN 6 PIN SC-70 PACKAGE, DCK0006A	DCK0006A	TPS61220DCK	Texas Instruments
U2	1		Extended Common-Mode RS-485 Transceivers, Up to 500 m at 3 Mbps, D0008A	D0008A	SN65HVD24D	Texas Instruments
C9	0	68uF	Low ESR Tantalum Capacitors		TA020TCR686KER	Venkel
C10	0	10µF	CAP TANT 10UF 50V 10% 2917 2917 (7343 Metric)		T495X106K050ATE300	Kemet
C12, C13, C15, C16	0	1.0µF	CAP CER 1UF 50V 10% X7R 0805	0805 (2012 Metric)	GRM21BR71H105KA12L	Murata Electronics North America
FID1, FID2, FID3, FID4, FID5, FID6	0		Fiducial mark. There is nothing to buy or mount.	Fiducial	N/A	N/A
R7, R14	0	0.0	RES 0.0 OHM 1/8W JUMP 0805 SMD	0805 (2012 Metric)	RC0805JR-070RL	Yageo
R11, R19, R21	0	49.9 Ohm	RES 49.9 OHM 0.1W 1% 0805 SMD	0805 (2012 Metric)	CR0805-10W-49R9FT	Venkel

9 Layer Plots

To download the layer plots for the Half-Duplex, Non-Isolated RS-485 BoosterPack Reference Guide, see the design files at [TIDA-00214](http://www.ti.com/lit/zip/TIDA-00214).

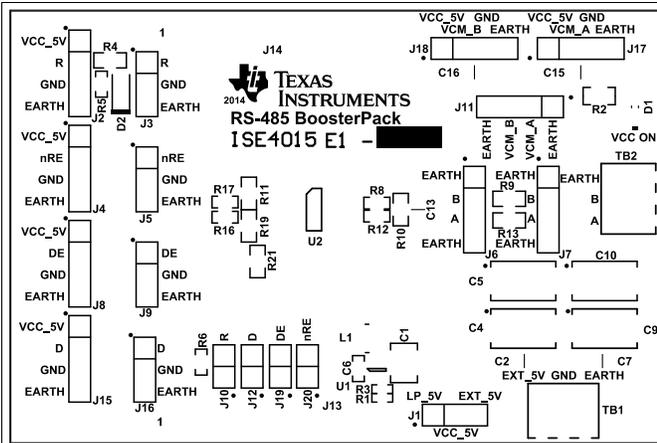


Figure 32. Top Overlay

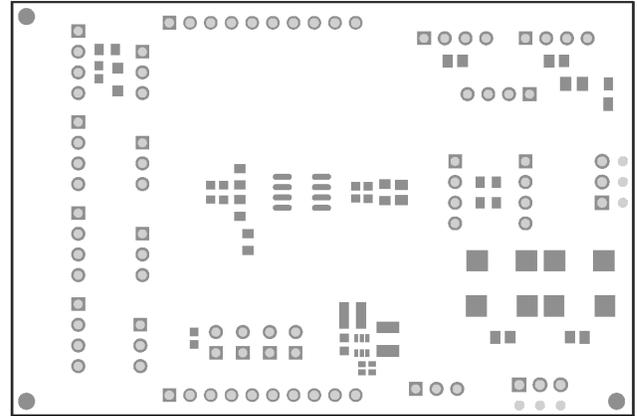


Figure 33. Top Solder Mask

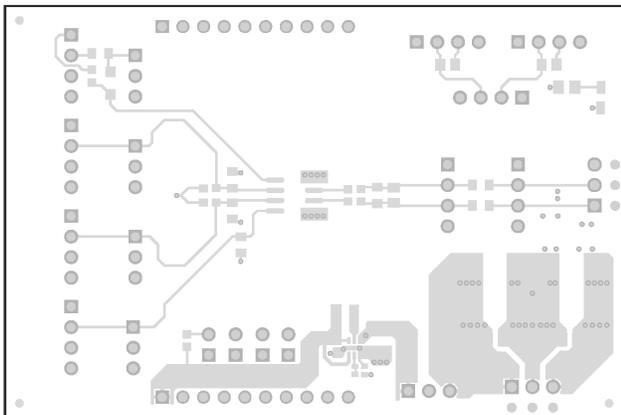


Figure 34. Top Layer

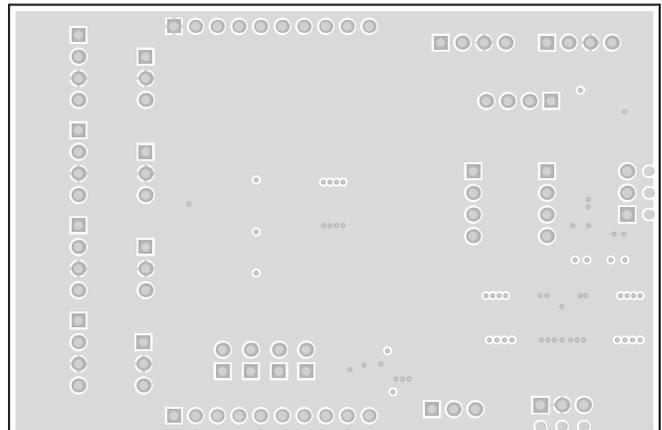


Figure 35. Mid Layer 1

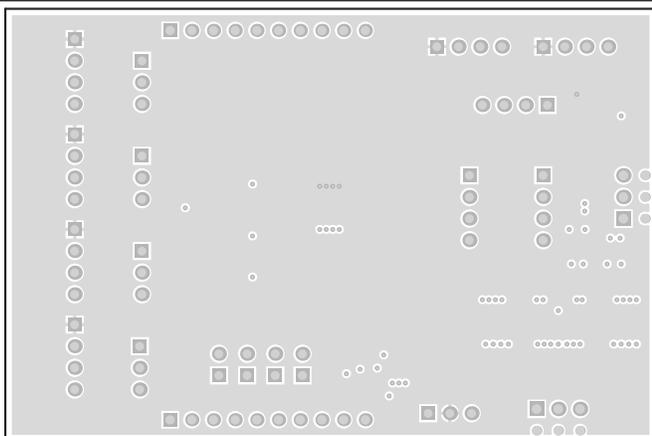


Figure 36. Mid Layer 2

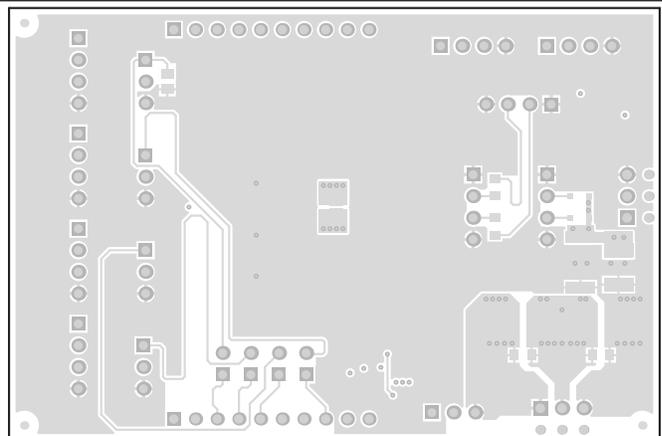


Figure 37. Bottom Layer

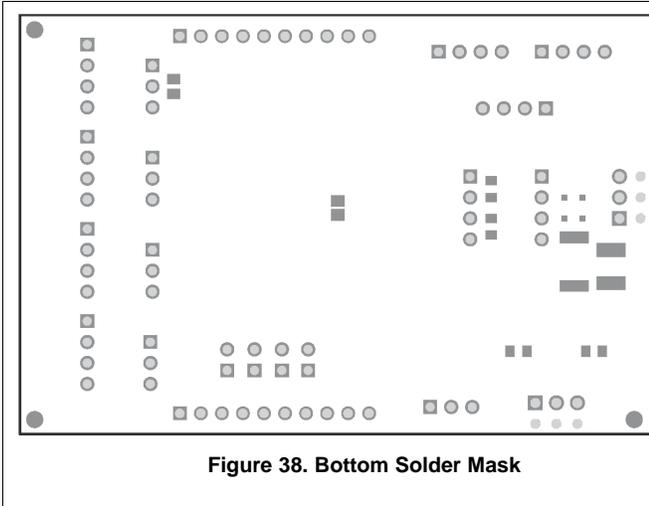


Figure 38. Bottom Solder Mask

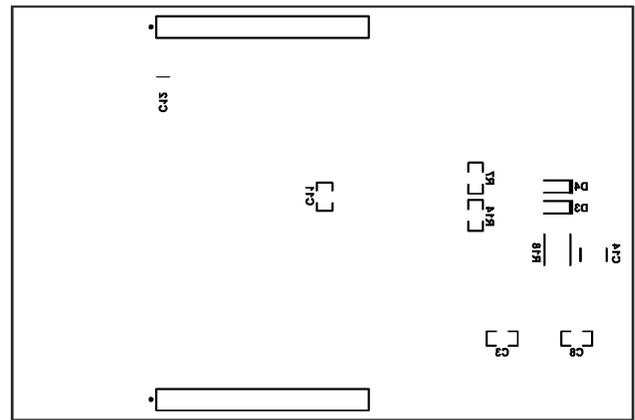
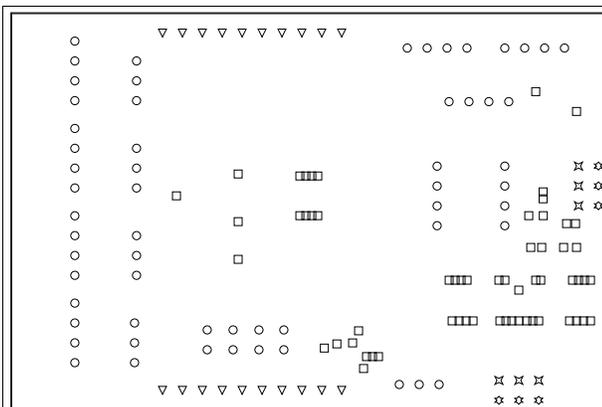


Figure 39. Bottom Overlay



Symbol	Hit Count	Tool Size	Plated	Hole Type
□	60	10mil (0.254mm)	PTH	Round
○	59	40mil (1.016mm)	PTH	Round
▽	20	41.339mil (1.05mm)	PTH	Round
×	6	43.307mil (1.1mm)	PTH	Round
☆	6	43.307mil (1.1mm)	NPTH	Round
	151 Total			

Drill Table

Figure 40. Drill Drawing

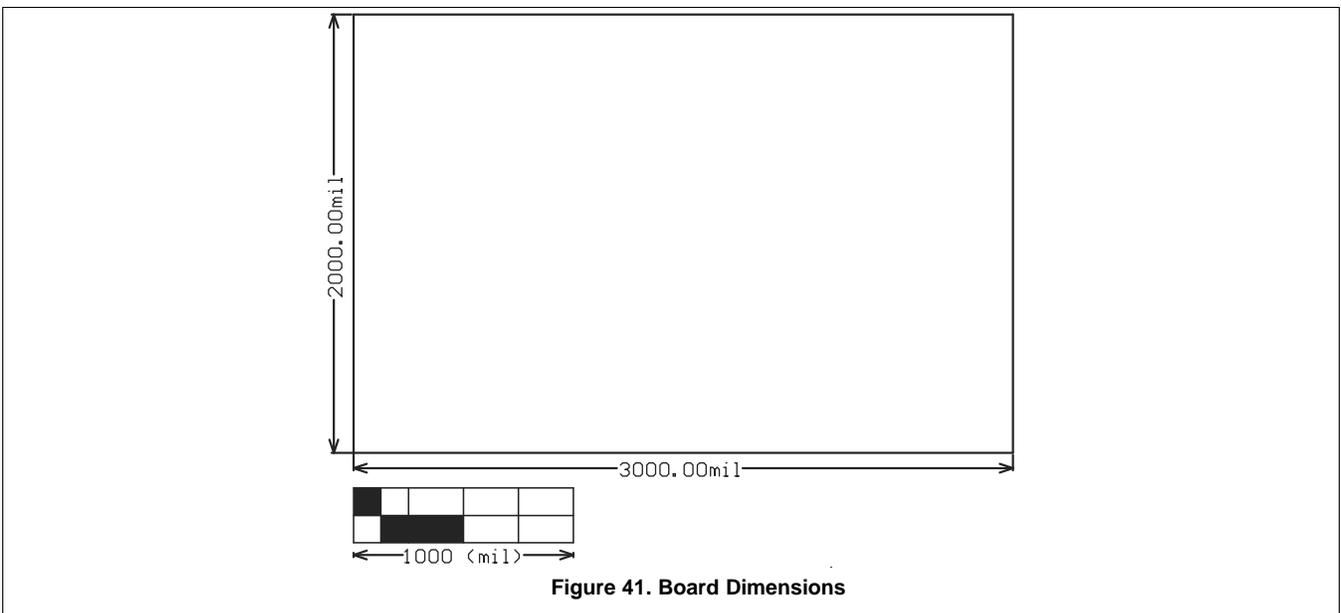


Figure 41. Board Dimensions

10 Altium Project

To download the Altium project files, see the design files at [TIDA-00214](#). Figure 42 through Figure 46 show the layout for the Half-Duplex, Non-Isolated RS-485 BoosterPack Reference Guide.

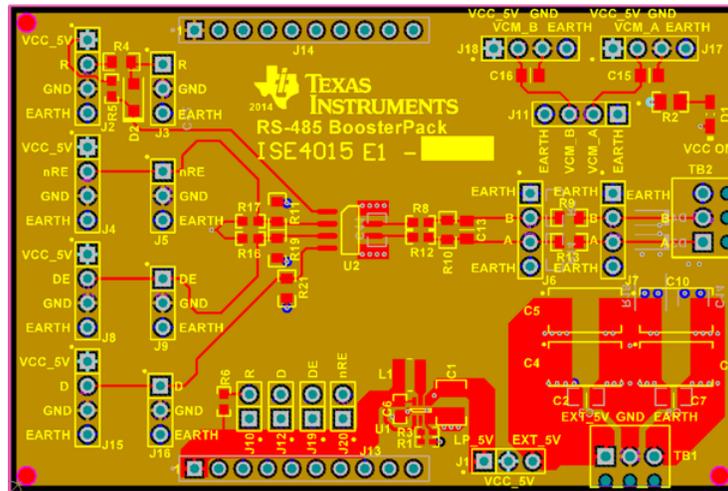


Figure 42. All Layers

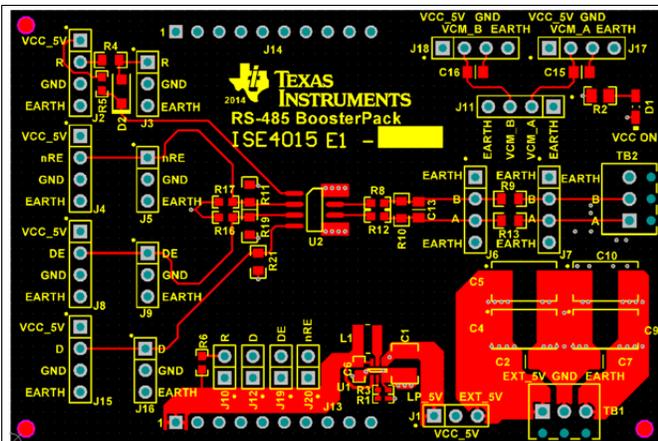


Figure 43. Top Layer

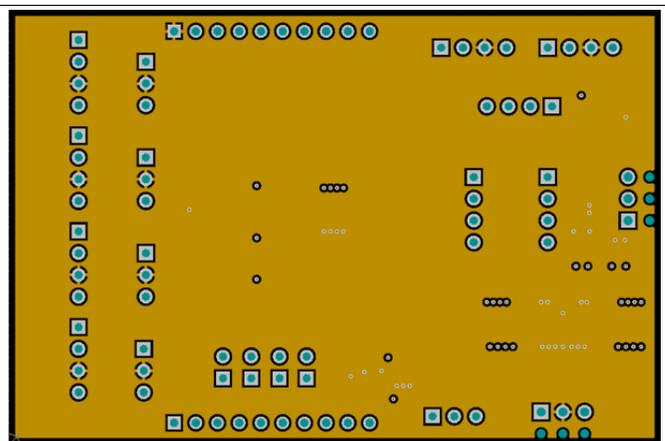


Figure 44. Ground Layer (Mid Layer 1)

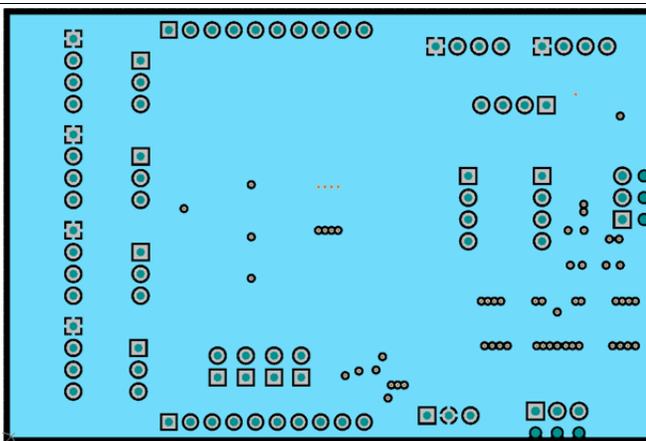


Figure 45. Power Layer (Mid Layer 2)

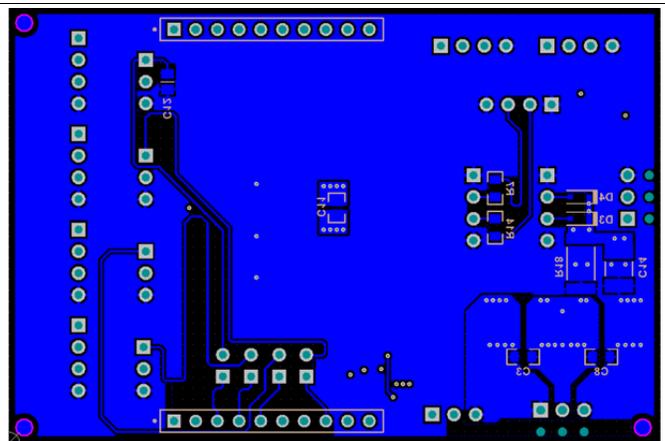


Figure 46. Bottom Layer

11 Gerber Files

To download the Gerber files for the Half-Duplex, Non-Isolated RS-485 BoosterPack Reference Guide, see the design files at [TIDA-00214](http://www.ti.com/TIDA-00214)

12 Assembly Drawings

To download the assembly drawings for the Half-Duplex, Non-Isolated RS-485 BoosterPack Reference Guide, see the design files at [TIDA-00214](http://www.ti.com/TIDA-00214).

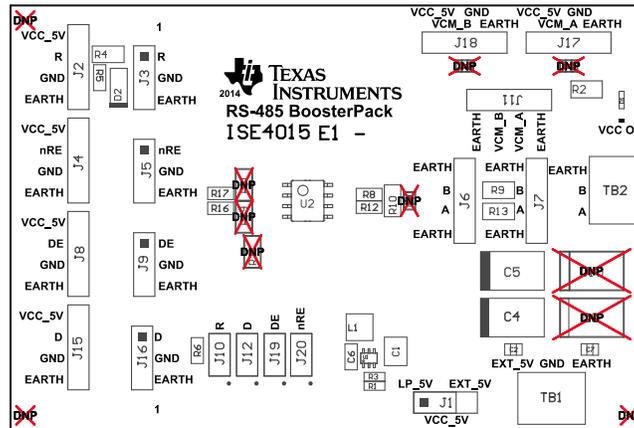


Figure 47. Top Assembly Drawing

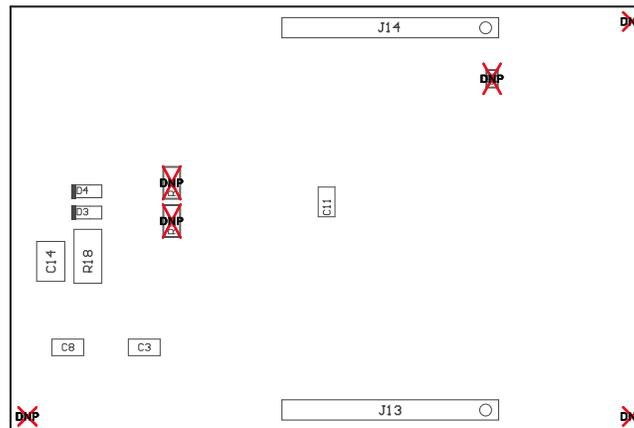


Figure 48. Bottom Assembly Drawing

13 Software Files

To download the software files for the reference design, see the design files at [TIDA-00214](#)

14 References

For additional references, see the following:

1. TPS61220 Data Sheet, *Low Input Voltage, 0.7-V Boost Converter with 5.5- μ A Quiescent Current* ([SLLS552](#))
2. SN65HVD24 Data Sheet, *Extended Common-mode RS-485 Transceiver* ([SLVS776](#))
3. Application Report, *The RS-485 Design Guide* ([SLLA272](#))
4. Application Report, *Protecting RS-485 Interfaces Against Lethal Electrical Transients* ([SLLA292](#))

15 About the Author

GUSTAVO MARTINEZ is a senior systems applications engineer at Texas Instruments where he is responsible for developing reference designs for industrial applications. Gustavo has ample experience developing system reference designs for the Smart Grid and home automation segments which include high-performance application processors, floating-point digital signal processors, and RF technology. Gustavo obtained his Bachelor of Science degree from the University of Texas at El Paso.

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