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TI Designs – Precision: CerTIfied Design

Low Cost Loop-Powered 4-20mA Transmitter EMC/EMI Tested Reference Design

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Design Resources

Design Archive	All Design files
TINA-TI™	SPICE Simulator
DAC7311	Product Folder
OPA317	Product Folder
TL431B	Product Folder

Circuit Description

This low cost loop-powered transmitter can accurately source currents from 4 mA to 20 mA. The circuit also includes an output protection circuit for IEC61000-4 immunity and a diode bridge to enable functionality regardless of the polarity of supply connections.

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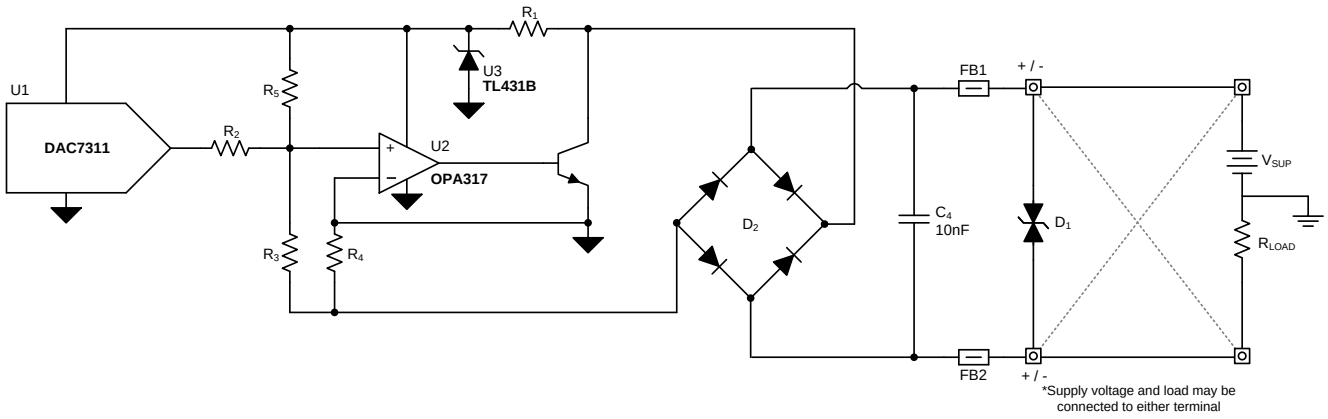

1 Design Summary

The design requirements are as follows:

- Supply Voltage: ≤36 V
- Input: 3-Wire SPI
- Output: 4-20 mA, 1% FSR Total Unadjusted Error (TUE)
- Loop Compliance Voltage: V_S-12 V
- Component Cost (1 ku): <$5

In addition to the parametric goals above, the design is expected to deliver immunity to the IEC61000-4 suite of tests with minimum impact on the accuracy of the system. The design goals, simulated results, and measured performance are summarized in Table 1. Figure 1 depicts the measured transfer function and accuracy of the design, illustrating results collected from 10 boards.

Table 1. Comparison of Design Goals, Simulated Results, and Measured Performance

	Goal	Simulated	Measured
Supply Voltage	≤36 V	≤36 V	≤36 V
Output TUE	1% FSR	0.525% FSR	0.173% FSR
Loop Compliance Voltage	12 V	10.61 V	9.7 V
Cost	<$5	n/a	$3.71 (at time of purchase)
IEC61000-4 Immunity	Pass	n/a	Pass

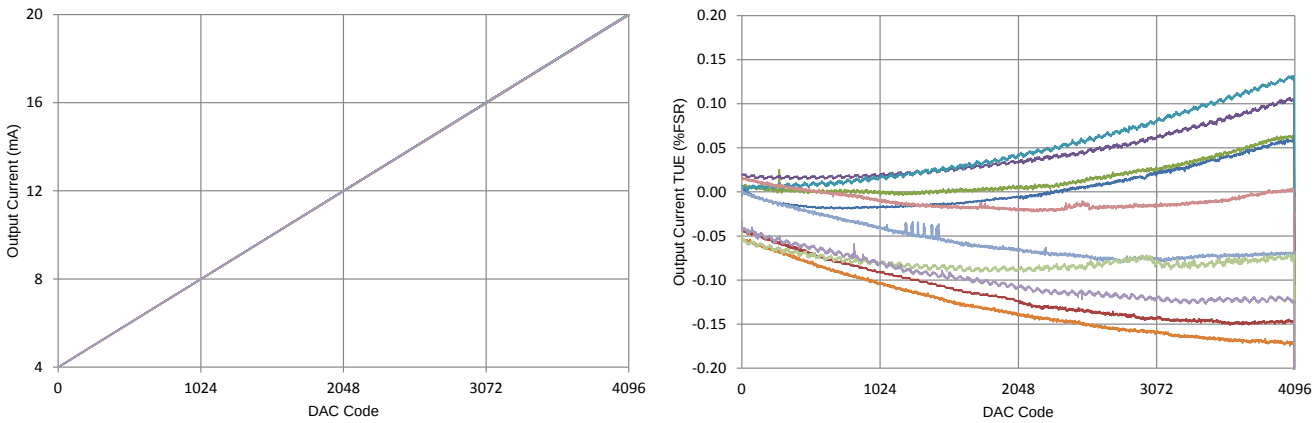

Figure 1: Measured Transfer Function & TUE

2 Theory of Operation

2.1 Voltage to Current Converter

A simplified schematic for the voltage to current converter is shown in Figure 2. This design is commonly referred to as a loop-powered, or 2-wire, 4-20 mA transmitter. The transmitter has only two external input terminals; a supply connection and a ground, or return, connection. The transmitter communicates back to its host, typically a PLC analog input module, by precisely controlling the magnitude of its return current. In order to conform to the 4-20 mA communication standard, the complete transmitter must consume less than 4 mA of current. Since one of the goals for this design is to maintain a low cost solution, this diagram assumes that the DAC uses its supply voltage as its reference voltage instead of including an external reference or selecting a more expensive DAC that features an internal reference.

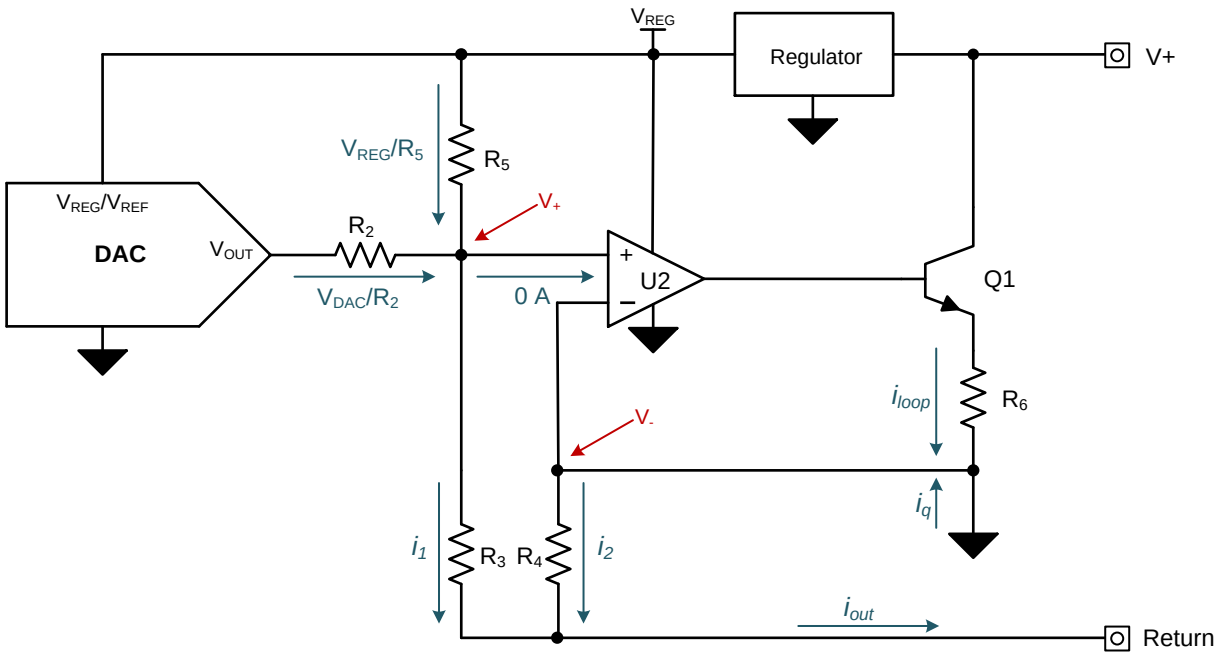

Figure 2: Simplified Voltage to Current Converter Circuit

Amplifier U2 uses negative feedback to ensure that the potentials at its inverting (V_-) and non-inverting (V_+) input terminals are equal. In this configuration V_- is directly tied to the local GND, therefore the potential at the non-inverting input terminal will be driven to local ground. This means that the voltage difference across R_2 is the DAC output voltage, V_{OUT}, and the voltage difference across R_5 is the regulator voltage, V_{REG}. These voltage differences cause current to flow through R_2 and R_5, as illustrated in Figure 2. These currents sum into i_1, defined in Equation (1), which flows through R_3.

$$i_1 = \frac{V_{DAC}}{R_2} + \frac{V_{REG}}{R_5} \quad (1)$$

U2 drives the base of the NPN BJT, Q1, to allow current to flow through R_4 such that the voltage drop across R_3 and R_4 remain equal, ensuring that the inverting and non-inverting terminals are at the same potential. A small part of the current through R_4 is sourced by the quiescent current of all of the components used in the transmitter design (regulator, amplifier, and DAC).

Since the voltage drops across R_3 and R_4 are equal, different sized resistors will cause different current flow through each resistor. This can be used to apply gain to the current flow through R_4 by controlling the ratio of resistor R_3 to R_4, as shown in Equation (2).

$$\begin{aligned} V_+ &= i_1 \cdot R_3 \\ V_- &= i_2 \cdot R_4 \Rightarrow i_2 = \frac{i_1 \cdot R_3}{R_4} \\ V_+ &= V_- \end{aligned} \quad (2)$$

This current gain is helpful to allow a majority of the output current to come directly from the loop through Q1 instead of from the voltage to current converter. This, in addition to low-power components, keeps the current consumption of the voltage to current converter low. The currents i_1 and i_2 sum to form the output current i_{out}, as shown in Equation (3).

$$i_{out} = i_1 + i_2 = \frac{V_{DAC}}{R_2} + \frac{V_{REG}}{R_5} + \frac{R_3}{R_4} \cdot \left(\frac{V_{DAC}}{R_2} + \frac{V_{REG}}{R_5} \right) = \left(\frac{V_{DAC}}{R_2} + \frac{V_{REG}}{R_5} \right) \cdot \left(1 + \frac{R_3}{R_4} \right) \quad (3)$$

The complete transfer function, arranged as a function of input code, is shown in Equation (4) below. The remaining sections divide this circuit into blocks for simplified discussion.

$$i_{out}(Code) = \left(\frac{V_{REG} \cdot Code}{2^{Resolution} \cdot R_2} + \frac{V_{REG}}{R_5} \right) \cdot \left(1 + \frac{R_3}{R_4} \right) \quad (4)$$

R_6 is included to reduce the gain of transistor Q1 and therefore reduce the closed loop gain of the voltage to current converter to ensure a stable design. Resistors R_2, R_3, R_4, and R_5 should be sized based on the full-scale range of the DAC, regulator voltage, and the desired current output range of the design.

2.2 Loop Regulator

LDOs or DC/DC converters along with series voltage regulators are often preferred devices for the voltage regulator and voltage reference in loop powered transmitter designs, however cost constraints eliminate them from consideration for this design.

Discrete Zener diodes are a low cost alternative to LDOs or DC/DCs that are often used as regulators or references in applications that prioritize cost. However, to properly regulate the Zener voltage they frequently require large amounts of cathode current, relative to the 4 mA quiescent current constraint of this design, to begin regulating to their Zener voltage. Zener diodes also show considerable deviation in their Zener voltage as loading conditions change since changes in load current change the cathode current. These limitations make the Zener approach unacceptable for this design.

Integrated shunt voltage references are another solution for the voltage regulator and voltage reference needs of this design. Like the Zener diode solution, shunt voltage regulators are often low-cost but they also offer improvements in load regulation, initial accuracy, and require very minimal current to begin regulation.

Figure 3 illustrates a simplified shunt voltage reference whose output voltage is programmable based on feedback resistors R_a and R_b. When supplied with enough current the shunt reference's internal band-gap reference turns on along with the internal amplifier. The output of the voltage divider formed by R_a and R_b is connected to the non-inverting input of the internal amplifier. In order to drive the non-inverting input to the same voltage as the inverting input, V_{REF}, the output of this voltage divider must also be V_{REF}. To accomplish this, the amplifier drives the base of the BJT to regulate the voltage drop across R_{in} and thereby control the input voltage, V_{OUT}, to the R_a and R_b voltage divider.

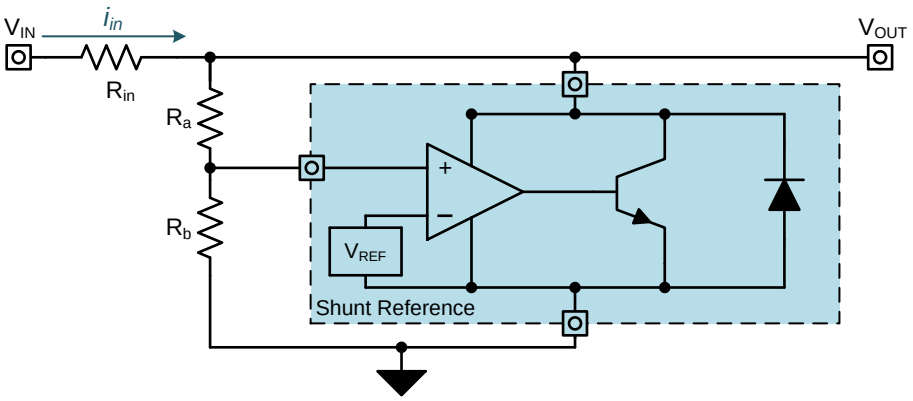

Figure 3: Simplified Programmable Shunt Voltage Reference

2.3 Diode Bridge & Protection Circuit

The industrial environment can be very dangerous for sensitive electronic components so systems are frequently designed to be very robust, including protection against incorrect wiring and immunity to environmental hazards that may lead to electrical overstress or undesired performance. Figure 4 shows the circuit used to protect this design from these events.

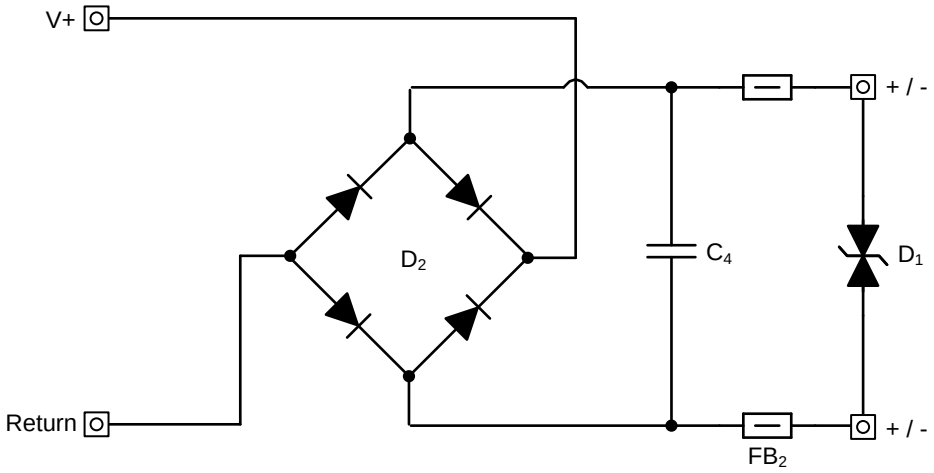

Figure 4: Diode Bridge & Protection Circuit

To protect against incorrect terminal connections a diode bridge is implemented. Two diodes are placed with cathode facing the positive node of the loop transmitter and anode facing each of the terminal blocks. Similarly, two diodes are placed with anode facing the return node of the loop transmitter and cathode facing each of the terminal blocks. This arrangement ensures that the loop connections will be rectified regardless of which terminal is connected to the supply and which is connected to the return.

The following sections discuss the test standards the protection circuit is tested against and the design of the protection circuit.

2.3.1 IEC61000-4 Test Standard

Many transient signals or radiated emissions common in industrial applications can cause electrical over-stress (EOS) damage or other disruptions to unprotected systems. IEC61000-4 is a test suite that simulates these transient and emission signals and awards a certification to systems that prove to be immune. During each of the IEC61000-4 tests, the output of the equipment under test (EUT) is monitored for deviations or total failure. Results are assigned one of four class ratings for each test. The classes are listed and described in Table 2.

Table 2. IEC61000-4 Result Classes

Grade	Description
Class A	Normal performance within an error band specified by the manufacturer.
Class B	Temporary loss of function or degradation of performance which ceases after the disturbance is removed. The equipment under test recovers its normal performance without operator interference.
Class C	Temporary loss of function or degradation of performance, correction of performance requires operator intervention.
Class D	Loss of function or degradation of performance which is not recoverable, permanent damage to hardware or software, or loss of data.

See Appendix B for photos of conventional test setups for each of the tests mentioned in this section. Full details of each of the IEC61000-4 tests are licensed by the IEC and must be purchased.

2.3.1.1 IEC61000-4-2: Electrostatic Discharge

The electrostatic discharge (ESD) immunity test emulates the electrostatic discharge of an operator directly onto an electrical component. To simulate this event, an ESD generator applies ESD pulses to the EUT either through air discharge or through vertical and horizontal coupling planes. Air discharge tests are conducted near any exposed I/O terminal.

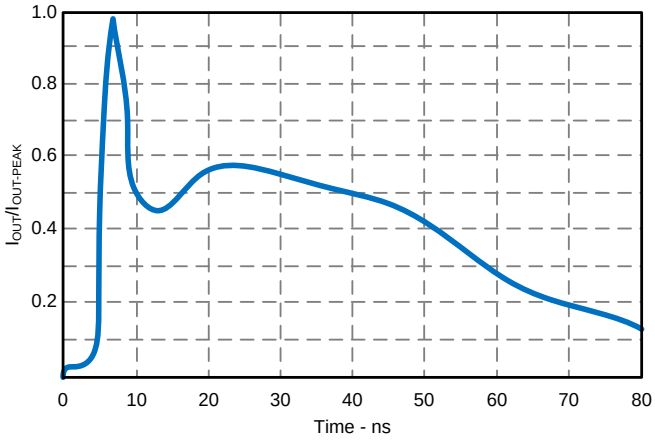

Figure 5: IEC61000-4 ESD Test Pulse

The ESD test pulse is pictured in Figure 5. The ESD test pulse is a high frequency transient with a pulse period of less than 100ns. The pulse is a high-voltage signal, ranging from 4 kV to 15 kV depending on the threat level appropriate for the EUT. The complete ESD test requires 10 sequential discharges of each positive and negative polarity for each test configuration.

2.3.1.2 IEC61000-4-3: Radiated Immunity

The radiated immunity (RI) test emulates exposure to high frequency radiated emissions, such as radio devices or other emissions common in industrial processes. The frequency range and field strength of the radiated signals vary in this test based on the type of EUT. For this design the tested frequency range was 80 MHz – 1 GHz and the field strength was 20 V/m.

2.3.1.3 IEC61000-4-4: Electrically Fast Transient

The burst immunity, or electrically fast transient (EFT) emulates day to day switching transients from various sources in a typical industrial application space. The test is performed on power, signal, and earth wires – or a subset depending on what is appropriate for the EUT.

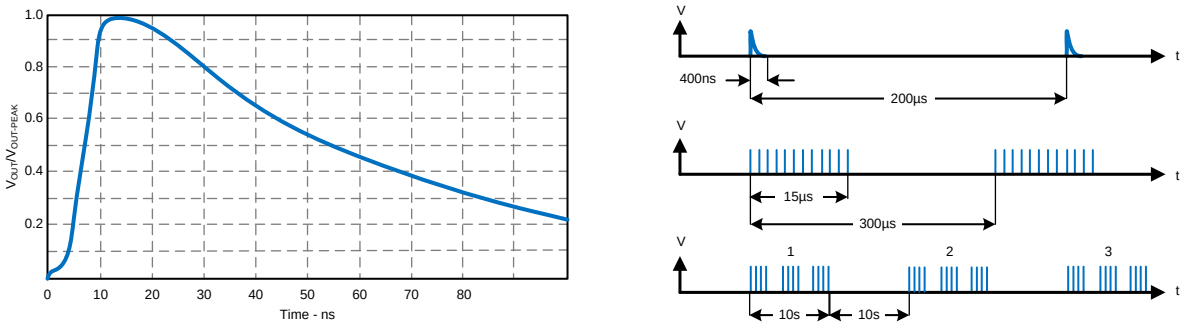

Figure 6: IEC61000-4 EFT Test Pulses

In this test a burst generator produces a series of EFT bursts, each lasting 15ms with 300ms in between bursts. The pulse rate of each burst is approximately 5 kHz. A typical test will expose the EUT to 1 – 3 minutes of EFT bursts. Similar to the ESD test pulse, the EFT pulses are a high frequency signal but the magnitude of the EFT test pulse only ranges from 0.25 kV to 4 kV. Bursts of both positive and negative polarity are applied.

2.3.1.4 IEC61000-4-6: Conducted Immunity

The conducted immunity (CI) test simulates exposure to radio frequency transmitters in the range of 15 kHz to 80 MHz. Like the RI test, the field strength of the CI transmitter can vary, ranging from 3 V/m to 10 V/m.

2.3.2 Protection Circuitry

The IEC61000-4 transients have two main components: a high frequency component and a high energy component. These two properties can be leveraged with a strategy of attenuation and diversion by the protection circuitry to deliver robust immunity.

Attenuation uses passive components, primarily resistors and capacitors, to attenuate high-frequency transients and to limit series current. Ferrite beads are commonly used with voltage outputs to maintain dc accuracy while still limiting series current, but they can also be useful for current outputs since they do not add any additional compliance voltage headroom at dc. A ferrite is included in series between each of the terminal blocks and the diode bridge along with a parallel capacitor to attenuate the high-frequency transients and limit current flow during exposure to transients.

Diversion capitalizes on the high voltage properties of the transient signals by using diodes to clamp the transient within supply voltages or to divert the energy to ground or the return path. Transient voltage suppressor (TVS) diodes are helpful to protect against the IEC transients because they break down very quickly and often feature high power ratings which are critical to survive multiple transient strikes. A TVS diode is included in between the two terminal block connections, positioned close to the terminal blocks in the PCB layout.

2.4 Loop Compliance Voltage

Loop compliance voltage defines the maximum voltage that may be present at the point of load of the current output for the loop transmitter to remain in the linear region of operation. Equation (5) can be used to express the maximum load that the loop transmitter can drive or the minimum supply voltage the transmitter needs to drive a given load

$$Compliance Voltage \leq V_{SUP} - I_{OUT} R_{LOAD} \quad (5)$$

The primary limitation for compliance voltage in this design is ensuring that there is enough current flowing across R_1 and to the shunt regulator meet its current requirements to continue to regulate as intended. If the compliance voltage is violated the output may be non-linear or completely non-functional as the shunt regulator cannot continue regulating the supply voltage to the transmitter.

Series elements on both sides of R_1 lower the voltage drop across R_1 and therefore lower the current flow through R_1 and to the regulator.

A diode from the bridge rectifier is in series with R_1 on its high-side and decreases the high-side voltage by the diode's forward voltage. The loop regulator, R_4, another diode from the bridge rectifier, and the load resistor are in series with R_1 on its low-side. The loop regulator increases the voltage on the low-side by the voltage across the regulator, which is its output voltage. The majority of the output current flows through R_4 and causes a voltage drop that further increases the low-side voltage. Finally, the series diode from the bridge rectifier increases the low-side voltage by the diode's forward voltage.

These factors, along with the size of resistor R_1, will impact how much cathode current is available to keep the shunt regulator biased appropriately. Keeping R_1 very small would maximize the current available to the regulator, but it must be large enough to ensure less than 4 mA of current is flowing into the regulator and loop transmitter at maximum loop supply voltage to comply to the 4-20 mA standard.

3 Component Selection

Component selection for all devices used in this design is limited to low power and low cost devices in order to comply with the 4-20 mA standard and meet the budget constraints of this design. Figure 7 shows a detailed diagram of the complete design including final values for discrete components and the specific integrated circuits used.

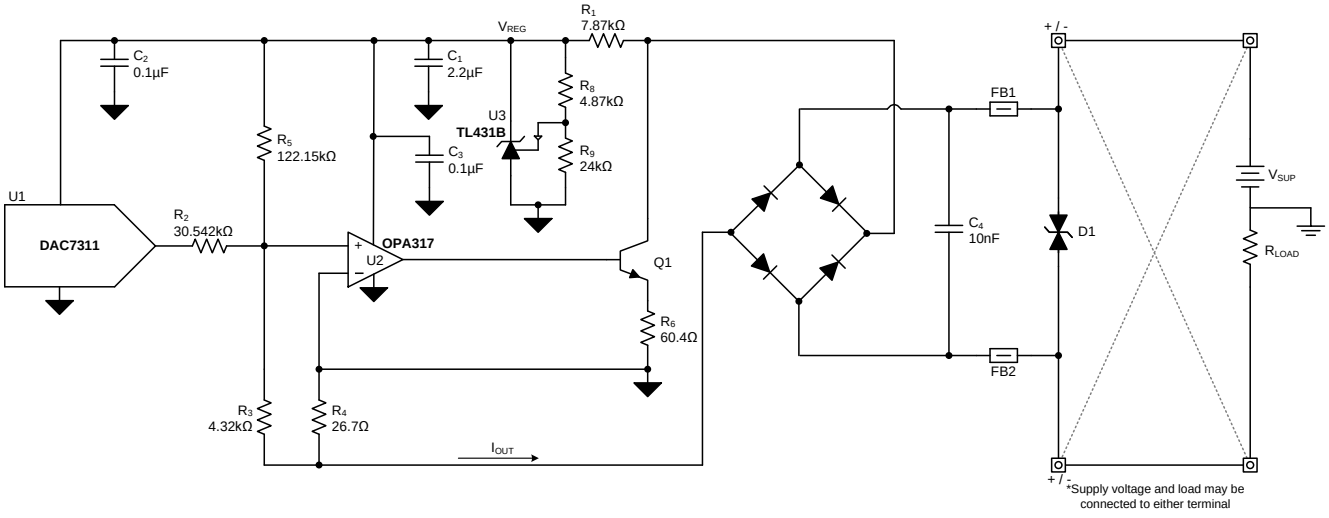

Figure 7: Detailed Design Diagram

3.1 DAC

Accuracy errors associated with the DAC will propagate through the rest of the signal chain and decrease the accuracy of the solution, so the DAC effectively sets the base line of performance for the rest of the design. A DAC with minimal offset error, gain error, and linearity errors (INL and DNL) to achieve dc error of less than 1% FSR TUE should be chosen. In order to minimize loop compliance voltage a DAC with low minimum supply voltage is also beneficial.

DAC7311 was chosen for this design because it delivers good dc performance, at 0.085% FSR TUE typical, while consuming a maximum of 150 µA under normal operating conditions. Additionally the DAC7311 minimum supply voltage is just 2.0V.

3.2 Amplifier

The amplifier chosen for this design should contribute minimum error to the signal chain compared to the accuracy of the DAC to maintain system accuracy. The most important dc accuracy specification of the amplifier in this design is low input offset voltage. Low input bias current is also relevant to ensure that the amplifier inputs are not sourcing or sinking any substantial current through resistor R_3 since this current is gained up by the ratio of R_3 to R_4 to generate the output current. Auxiliary specifications are power supply rejection ratio, common-mode rejection ratio and bandwidth. It should be noted that while increased bandwidth may be desired in some applications, low-power devices are also typically low bandwidth which may limit availability of higher bandwidth options.

OPA317 was chosen for this design because it delivers very low input offset voltage and input bias current, 20 µV and 155 pA respectively, with only 35 µA quiescent current. Like the DAC7311, the OPA317 minimum supply voltage is very low at 1.8V.

3.3 Regulator

Since the regulator voltage is used as the DAC reference voltage to save cost in this design the regulator must have good initial accuracy and perform well as loading conditions change. Cost constraints eliminate using an LDO for the regulator and poor load regulation eliminate using a simple Zener diode regulator.

Instead the TL431B was chosen because of its low cost and once it has reached the required cathode current to regulate its internal reference voltage, the regulator output will remain relatively consistent even as loading conditions change. This regulator is also used as the DAC reference voltage leading to some system performance losses due to the 0.5% initial accuracy specification of the TL431B.

The loop regulator uses the TL431B programmable shunt regulator to provide a 3 V supply to the loop transmitter using the rectified supply voltage from the diode bridge. Figure 8 shows the loop regulator section of the design.

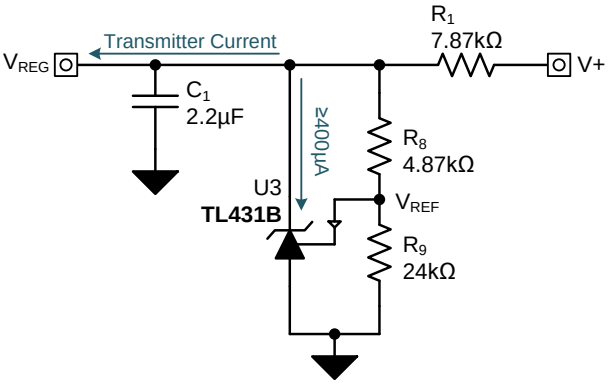

Figure 8: Loop Regulator Circuit

The cathode current supplied to the TL431B directly impacts the accuracy of the internal band-gap reference, which in turn impacts the accuracy of the regulator output. The TL431B typical characteristics curve, inserted below, shows that only 400 µA of cathode current is required to begin regulating the internal reference. As cathode current increases the V_{KA}, or internal reference, voltage remains nearly constant, however the cathode current must remain under 4 mA for the transmitter to comply with the 4-20 mA standard.

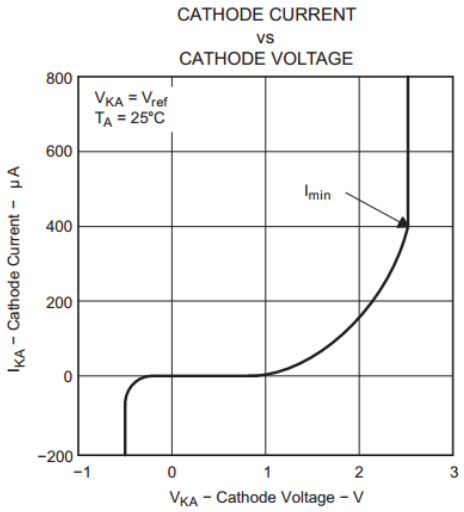

Figure 9: TL431B Cathode Current vs. V_{REF}

The regulator must always have 400 µA of cathode current or more, even when the transmitter is set to full-scale output and the transmitter current consumption is at its highest. If this condition is violated the V_{REF} voltage will begin to drift as the output approaches full-scale. Because the DAC7311 uses this supply voltage as its reference voltage this drift will create a gain error on the transmitter output.

Assuming adequate cathode current, the regulator output voltage can be defined by Equation (6), where V_{REF} is nominally 2.495 V. For more information regarding setting the shunt voltage on this family of programmable shunt regulators refer to application report SLVA445.

$$V_{REG} = \left(1 + \frac{R_8}{R_9}\right) \cdot V_{REF} \quad (6)$$

The final consideration for the loop regulator is to understand the stability boundaries of the TL431B to size bulk and local decoupling capacitors appropriately. Application report SLVA482 explains the stability criteria of the TL431B and indicates that load capacitance of less than 0.01 µF or greater than 2.2 µF provide significant phase margin and ensure that the output does not oscillate. To satisfy this condition a bulk 2.2 µF decoupling capacitor is placed at the regulator output in addition to the local decoupling capacitors for the DAC7311 and OPA317.

3.4 Diodes

3.4.1 TVS Diode

A bidirectional TVS diode is used to divert high voltage transients to ground. Selection of this diode should be based on working voltage, breakdown voltage, leakage current and power rating. The working voltage specification defines the largest reverse voltage that the diode is meant to be operated at continuously without it conducting. This is the voltage at the “knee” of the reverse breakdown curve where the diode begins to break down and exhibits some small leakage current. As the voltage increases above the working voltage, more current will begin to flow through the diode. The breakdown voltage defines the reverse voltage at which the diode is fully allowing current to flow. It is important to keep in mind that if excessive current flows through a diode, the breakdown voltage will rise.

The diode breakdown voltage should be low enough to protect all components connected to the output terminals and to provide headroom to continue providing this protection as the breakdown voltage rises with large currents. In this design the working voltage of the TVS diode should be at or above the upper limit of the allowed supply voltages since any higher voltage would cause leakage through the diode. In this case a diode with working voltage of 36V, breakdown voltage of 40 V, and power rating of 400 W was chosen.

An additional parameter to consider for TVS diode selection is leakage current. At the working voltage, when the diode is not operating in its breakdown region, some current will flow through the diode and can affect system accuracy. The diode selected for this design features 1 µA maximum leakage current at the working voltage.

3.4.2 Diode Bridge

A diode bridge, or bridge rectifier, is used in this design to ensure that the design will always function as intended regardless of the arrangement of terminal block connections. Selection of this diode should be based on low reverse leakage current and low forward voltage. Low reverse leakage current should also be considered because two diodes in the bridge configuration will always be reverse biased and allowing some leakage current and will directly impact accuracy. Low forward voltage is helpful because this allows for the design to achieve lower compliance voltage.

The DSRHD10 was chosen for this design because it offers 4 diodes in the desired arrangement in a single package. This device features 0.1 µA reverse leakage current at peak reverse bias of 1000V and 1.15 V forward voltage at peak forward current of 1 A. Reverse leakage current improves to less than 0.01 µA under the operating conditions defined by this design. Similarly forward voltage improves to ~0.6 V.

3.5 Passives

Series ferrites and a parallel capacitor are used to attenuate transient signals that may remain after passing the TVS diode. The ferrites are chosen based on their current rating, impedance at dc, and impedance at high frequency. In this design the chosen ferrites feature 42 mΩ max impedance at dc, 600 Ω impedance at 100MHz, and 3 A current rating. The capacitor chosen has a voltage rating of 100V.

Several of the resistors used in this design must have tight tolerances in order to achieve high accuracy. This includes the current setting resistor R_2, the offset resistor R_5, the gain setting resistors R_3 and R_4, and the regulator output voltage setting resistors R_8 and R_9. In this design each of these components are 0.1% tolerance. The remaining resistors, R_1 and R_6, may be components with loose tolerance.

The ratio of resistors R_3 and R_4 determine the primary path of the output current flow. Typically a majority of the output current will come through Q1 and R_4, so the power rating of R_4 should be chosen accordingly. In this case R_4 is a 0.25 W resistor.

R_1 is the series pass element that sets the current provided to the TL431B. Though this resistor passes small amounts of current, it is typically a very large resistor which will require sufficient power rating. In this design R_1 is a 0.25 W resistor.

4 Simulation

Models are available for each of the components used in this design, allowing a complete SPICE model to simulate most performance parameters. Figure 12 shows the complete TINA-TI ® schematic used to model the design with the circuit values obtained in the design process.

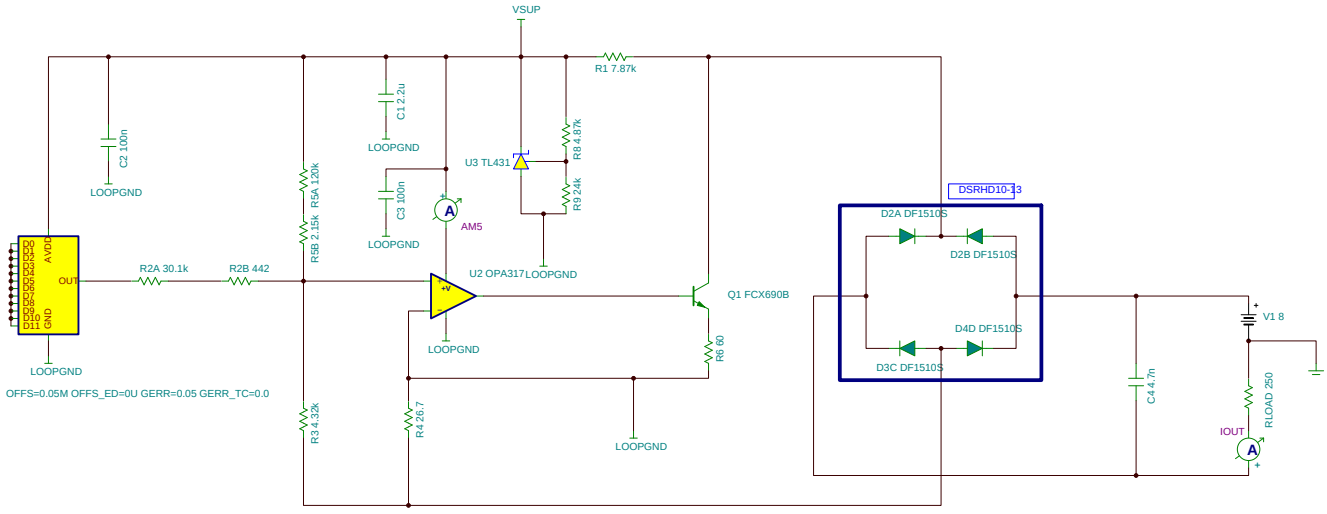

Figure 10: TINA-TI ® SPICE Simulation Model

Simulated results are broken into sections to understand the performance of each block. The uncorrelated error sources from each section are root-sum-squared together to estimate TUE of the complete design.

Results in sections 4.1 through 4.4 are simulated over the linear region of operation of the DAC7311 as defined by the code set used to characterize INL and DNL. Additional errors will be observed near the positive and negative supply rails due to output voltage swing to rail limitations of the DAC7311 output amplifier.

4.1 Regulator Simulation

Regulator performance is simulated using the model shown in Figure 10. The TL431B model simulates the loaded output voltage of the TL431B and Monte Carlo analysis is performed on the resistor network, R_8 and R_9, used to set the output voltage of the regulator. Error in the regulator voltage generates offset and gain errors on the 4-20 mA transmitter output, described in Table 3.

Table 3. Regulator Simulation Results

Parameter	Simulated Results
Regulator Output Voltage Error (mV)	+/-15.02
Offset Error (%FSR)	0.1304
Gain Error (%FSR)	0.4976
TUE (%FSR)	0.5144

4.2 DAC Simulation

DAC performance is simulated using the model shown in Figure 10 with the OPA317 replaced by an ideal amplifier. This model is included in the design file associated with this document. The DAC7311 model has input parameters to model offset, offset drift, gain, and gain drift that are each loaded with their typical values from the DAC7311 datasheet. INL is not included in the TINA-TI SPICE model, so INL errors must be hand-calculated. Table 4 summarizes the DAC simulation results.

Table 4. DAC Simulation Results

Parameter	Simulated Results
INL Error (%FSR)	0.00000732471
Offset Error (%FSR)	0.01028167
Gain Error (%FSR)	0.0431875
TUE (%FSR)	0.044394515

4.3 OPA317, Diode Bridge, & Resistor Simulation

Performance of the remaining components in the design is simulated using the model shown in Figure 10 with the DAC7311 replaced by an ideal voltage source. This model is included in the design file associated with this document. The OPA317 model simulates important dc parameters like input offset voltage and input bias current. The diode bridge model simulates reverse leakage current. The resistor network tolerance is simulated with Monte Carlo analysis. This portion of the circuit is assumed to be completely linear and therefore contributes no linearity error.

Table 5. Front-End Simulation Results

Parameter	Simulated Results
Offset Error (%FSR)	0.020525811
Gain Error (%FSR)	0.09647914
TUE (%FSR)	0.096535019

4.4 System Results

Each set of results in sections 4.1, 4.2, and 4.3 can be root-sum-squared together to express cumulative system performance. In this design the regulator and reference architecture is a key contributor to reducing cost, but also a large contributor of system error. Table 6 summarizes all simulation results.

Table 6. System Simulation Results

Parameter	Regulator Simulation	DAC Simulation	Front-End Simulation	System Simulation
INL Error (%FSR)	n/a	0.00000732471	n/a	0.00000732471
Offset Error (%FSR)	0.1304	0.01028167	0.020525811	0.130922862
Gain Error (%FSR)	0.4976	0.0431875	0.09647914	0.508703396
TUE (%FSR)	0.5144	0.044394515	0.096535019	0.525671441

4.5 Loop Compliance Voltage

To simulate loop compliance voltage the load resistor, R5 in Figure 10, is replaced with a 0 Ω resistor and the supply voltage is swept from 40 V to 0 V while the loop current is measured. The system output is set to full-scale which should be the worst case for loop compliance voltage since maximum current is flowing through the transmitter instead of to the TL431B cathode. Compliance voltage is the point when the TL431B loses regulation due to cathode current below 400 µA, which occurs at ~10.61 V loop supply.

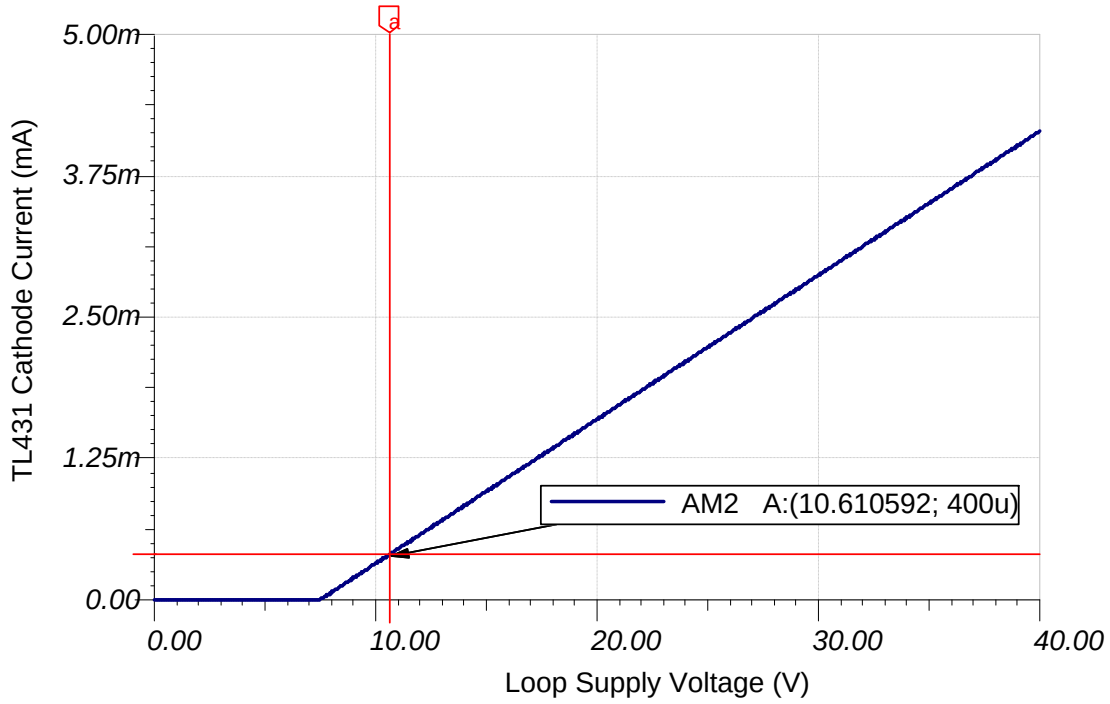

Figure 11: Loop Compliance Voltage Simulation Results

4.6 Error Equations

This section shows the equations used to calculate offset error, gain error, and TUE in sections 4.1, 4.2, 4.3, and 4.4.

$$OffsetError_{(\%FSR)} = \frac{IOUT_{Sim}(LowCode) - (LSB_{Sim} \times LowCode) - IOUT_{Ideal}(0)}{IOUT_{Ideal}(2^{bits}) - IOUT_{Ideal}(0)} \times 100 \quad (7)$$

$$GainError_{(\%FSR)} = \frac{(IOUT_{Sim}(HighCode) - IOUT_{Sim}(LowCode)) - (IOUT_{Ideal}(HighCode) - IOUT_{Ideal}(LowCode))}{IOUT_{Ideal}(2^{bits}) - IOUT_{Ideal}(0)} \times 100 \quad (8)$$

$$INLError_{(\%FSR)} = \frac{\frac{INLError_{DAC}}{R2} \times \left(1 + \frac{R3}{R4}\right)}{IOUT_{Ideal}(2^{bits}) - IOUT_{Ideal}(0)} \times 100 \quad (9)$$

$$TUE_{(\%FSR)} = \sqrt{OffsetError_{(\%FSR)} + GainError_{(\%FSR)} + INLError_{(\%FSR)}} \quad (10)$$

$$SystemTUE_{(\%FSR)} = \sqrt{RegError_{(\%FSR)} + DACError_{(\%FSR)} + FrontEndError_{(\%FSR)}} \quad (11)$$

5 PCB Design

The PCB schematic and bill of materials can be found in Appendix A.

5.1 PCB Layout

For optimal performance of this design follow standard PCB layout guidelines, including proper decoupling close to all integrated circuits and adequate power and ground connections with large copper pours.

Additional considerations must be made for providing robust EMC/EMI immunity. All protection elements should be placed as close to the output connectors as possible to provide a controlled return path for transient currents that does not cross sensitive components. To allow optimum current flow wide, low-impedance, low-inductance traces should be used along the output signal path and protection elements. When possible copper pours are used in place of traces. Stitching the pours provides an effective ground return path around the PCB and helps reduce the impact of radiated emissions.

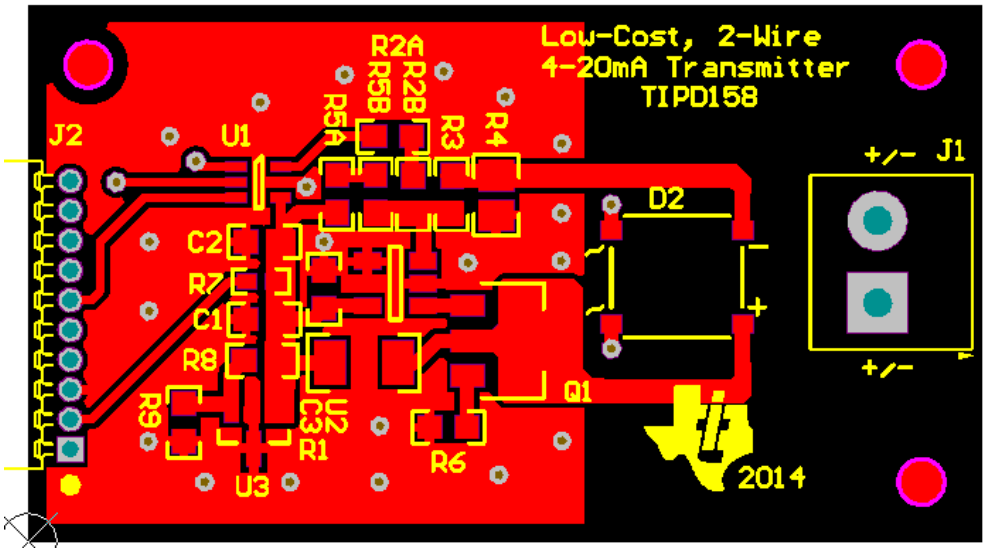

Figure 12: PCB Layout, Top Layer

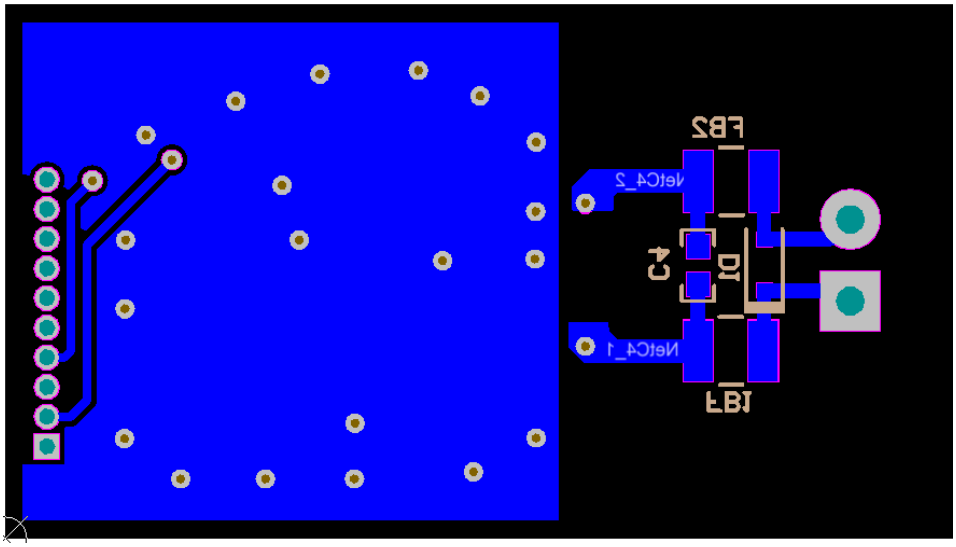

Figure 13: PCB Layout, Bottom Layer

6 Verification & Measured Performance

6.1 Current Output Results

DC transfer function data for the system current output was collected using a 6 ½ digit digital multi-meter while driving a 250 Ω load with 24 V loop supply voltage. The measured results, including end-point performance, are shown in Figure 14.

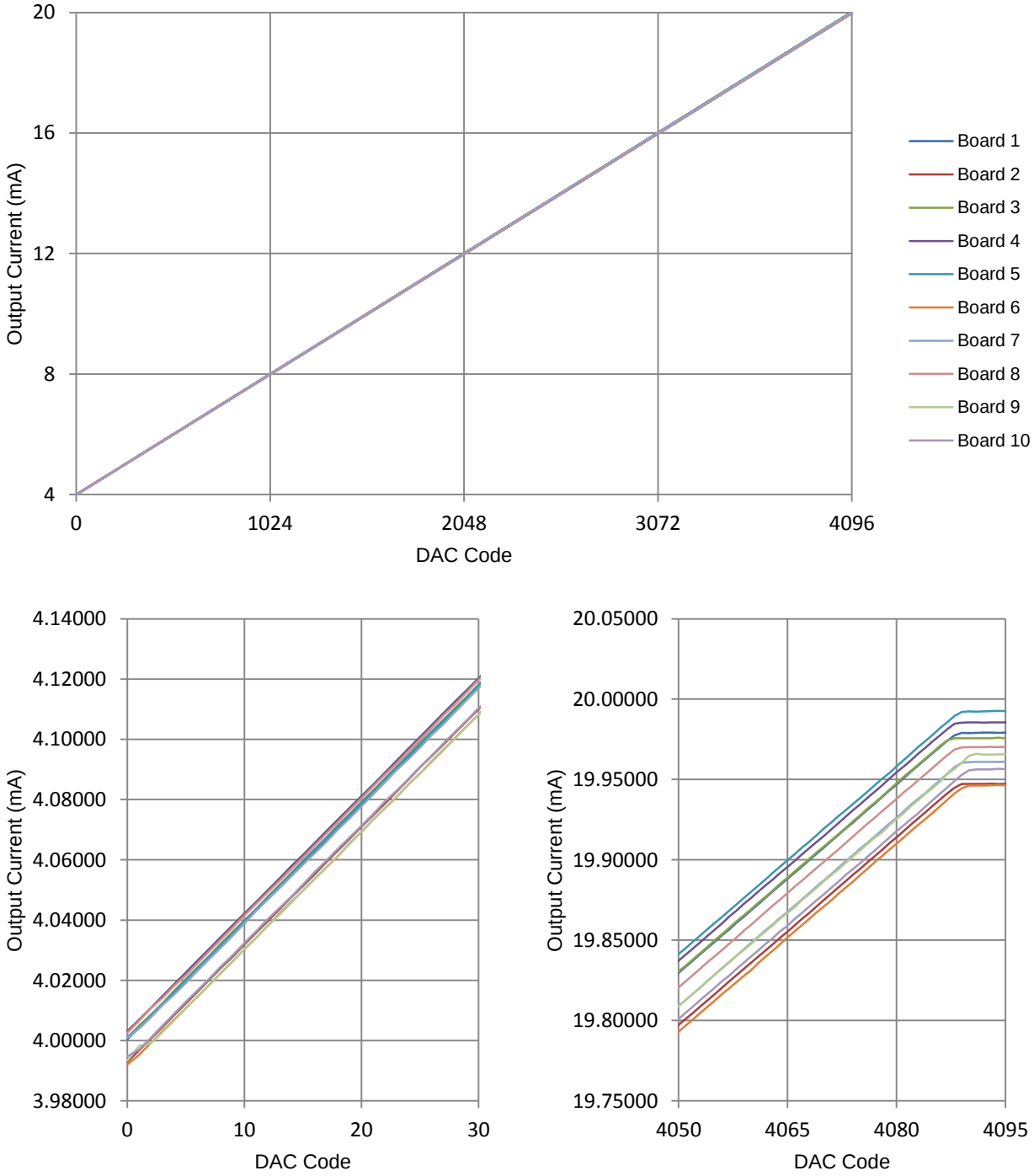

Figure 14: Output Current vs. Input Code

The calculated total unadjusted output current error in % FSR is shown in Figure 15. The worst-case measured results show TUE of 0.173%. Additional measured results and observations are available in Appendix C.

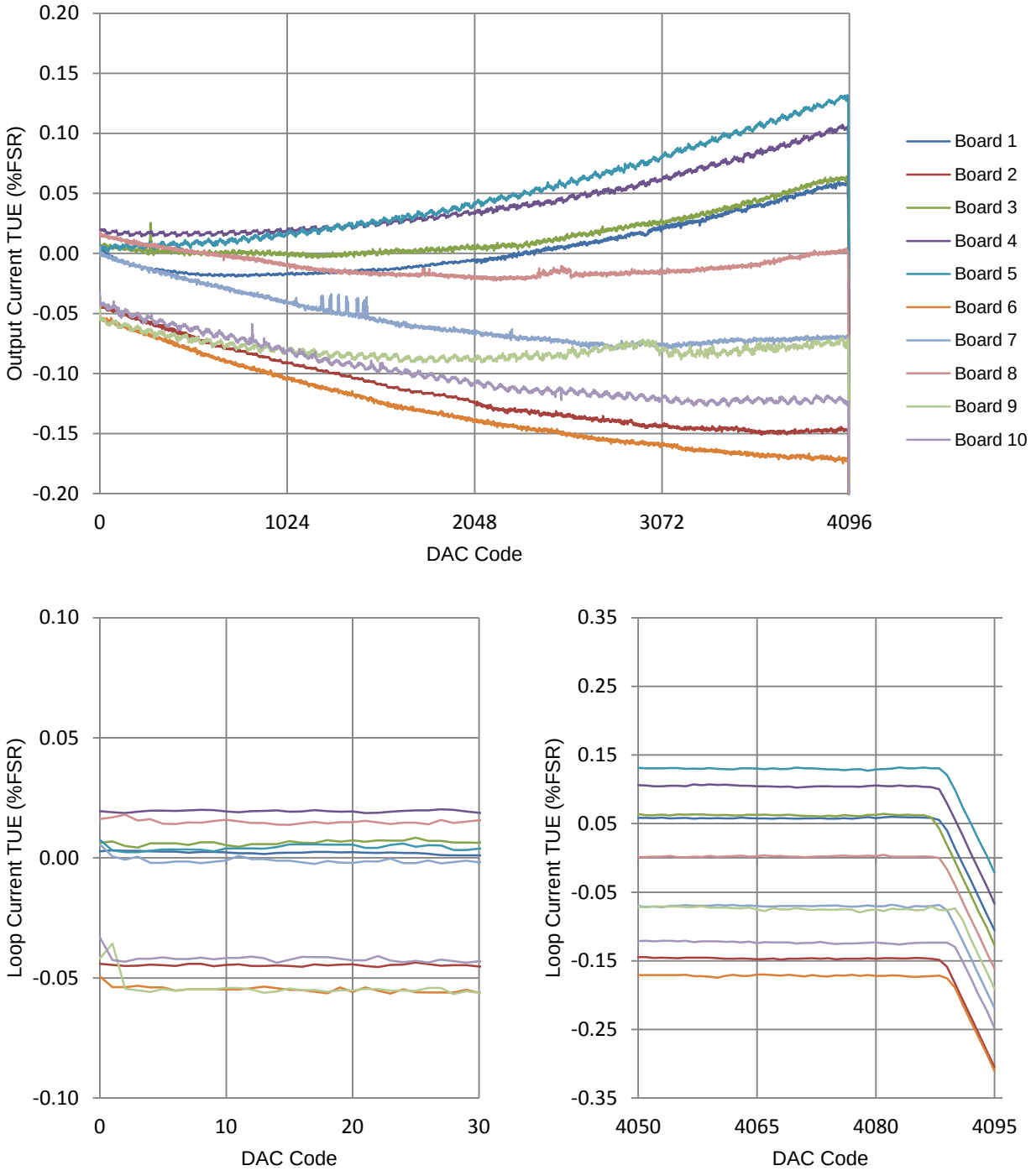

Figure 15: Output Current TUE vs. Input Code

$$TUE_{MEAS} = \frac{IOUT_{MEAS} - IOUT_{IDEAL}}{FSR_{IDEAL}} * 100 \quad (12)$$

6.2 Loop Compliance Voltage

To determine the loop compliance voltage the output current is set to full-scale and measured while the loop supply voltage decreases from 36 V to 0 V. The headroom the loop supply voltage provides to the system is dependent on the load and the output current and can be calculated using Equation (13). The voltage headroom when the output current begins to sharply decline is the transmitter compliance voltage, in this case approximately 9.7 V. Transmitter supply headroom curve is shown in Figure 16.

$$TransmitterHeadroom = V_{SUP} - I_{OUT} R_{LOAD} \quad (13)$$

Figure 16: Output Current vs. Loop Supply Voltage

6.3 Measured Results Summary

The accuracy goals, simulated results, and measured performance for output current TUE and loop compliance voltage are summarized in Table 7. Measured results showed much stronger performance than simulated results because no measured unit exhibited the worst-case initial accuracy error of the shunt regulator, DAC errors, or analog front-end errors.

Table 7. Comparison of Design Goals, Simulated Results, and Measured Performance

	Goal	Simulated	Measured
Output Current TUE	1% FSR	0.525% FSR	0.173% FSR
Loop Compliance Voltage	12 V	10.61 V	9.7 V

7 Certification Testing Results

The IEC61000-4 certifications clearly define conditions for class B, C, and D performance but do not provide an explicit definition for class A. Class A conditions are defined by the manufacturer. For this EUT class A performance will be assigned for outputs that stay within 0.1% FSR of their intended value during exposure to each disturbance indicating that the test has insignificant impact on the system. For all tests the system output is set to mid-scale to avoid anomalous behavior when the system is operating near its supply rails.

The IEC61000-4 certifications do not specify what supporting equipment is used to monitor the output of the EUT. For this design, an Agilent 34401A 6 ½ digit digital multi-meter with its resolution set to fast 5 ½ digit mode was selected to monitor the output with ferrites on its input to protect the equipment from interference caused by the IEC61000-4 tests.

7.1 IEC 61000-4-2: Electrostatic Discharge

ESD tests were conducted at ±15 kV air discharge and ±8 kV coupling plane discharges. ESD had no significant effect on the current output of the system. During and after the tests the output stayed within 0.1% FSR of the intended output value. Table 12 summarizes the ESD test results. Figure 17, Figure 18, and Figure 19 show the measured output during each test.

Table 8. IEC61000-4-2 Results

Orientation	Result	Class
Coupling Plane Discharge	Pass	A
Air Discharge	Pass	A

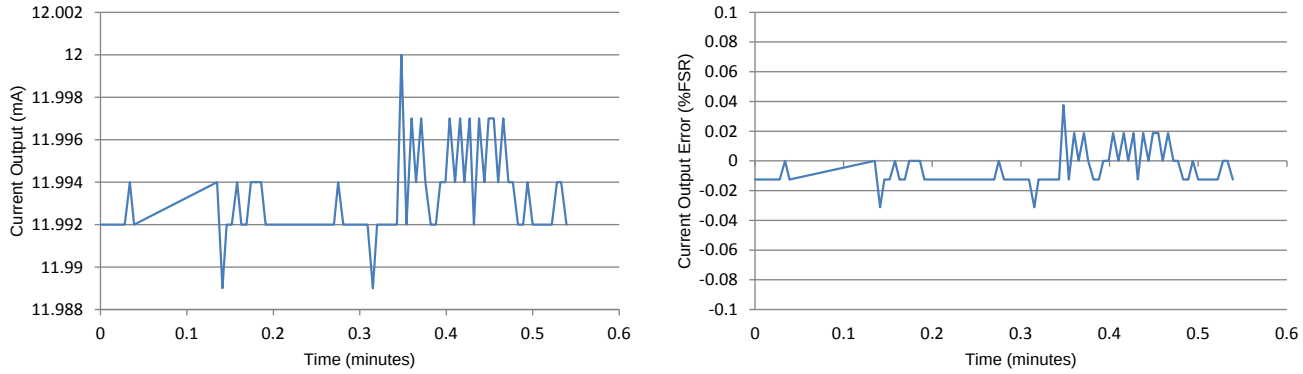

Figure 17: Current Output - ±8 kV Horizontal Coupling Plane ESD Measurements

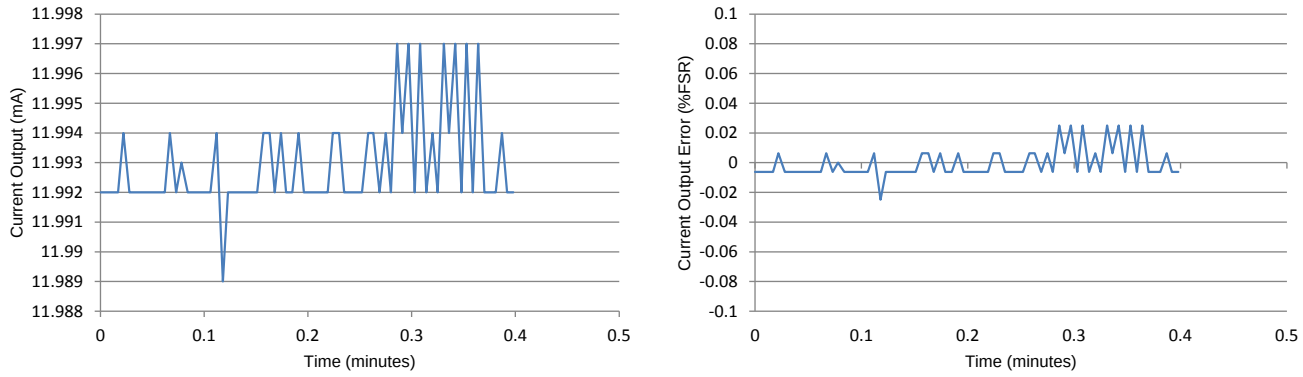

Figure 18: Current Output - ±8 kV Vertical Coupling Plane ESD Measurements

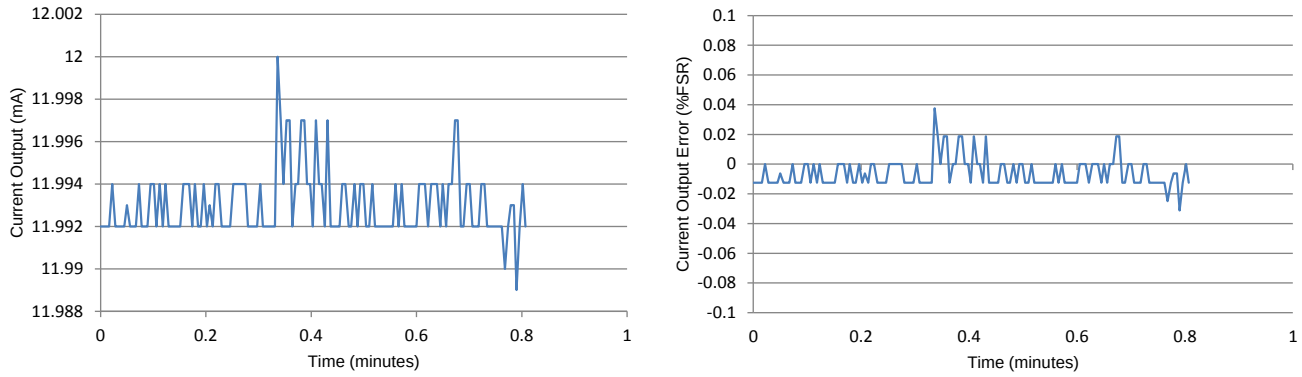

Figure 19: Current Output - ±15 kV Air Discharge ESD Measurements

7.2 IEC 61000-4-3: Radiated Immunity

Exposure to radiated emissions with field strength of 20 V/m in both vertical and horizontal antenna orientations had no effect on the current output of the system during or after the test. Table 9 summarizes the results. Figure 20 and Figure 21 show the measured output during the tests.

Table 9. IEC61000-4-3 Results

Orientation	Result	Class
Vertical	Pass	A
Horizontal	Pass	A

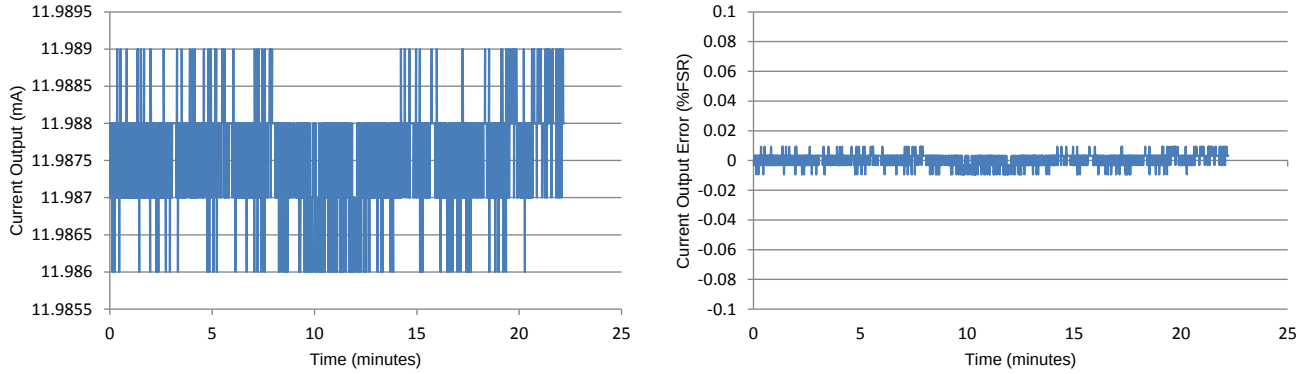

Figure 20: Current Output – 20 V/m Horizontal RI Measurements

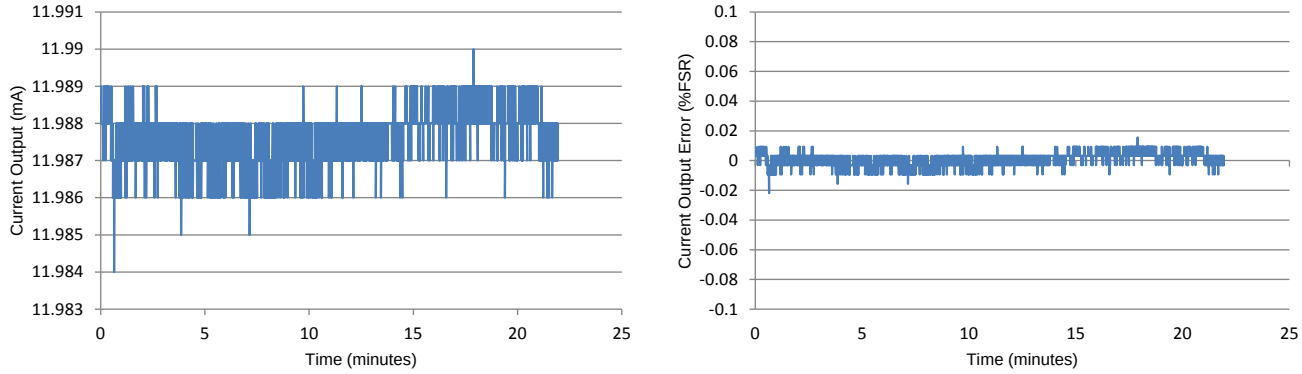

Figure 21: Current Output – 20 V/m Vertical RI Measurements

7.3 IEC 61000-4-4: Electrically Fast Transient

The positive polarity electrically fast transient bursts had no effect on the current output but deviations over 0.1% FSR were observed during exposure to negative polarity electrically fast transient bursts. This is because the TL431B is unable to provide any PSRR to a negative going pulse since the Zener-regulator architecture is only able to sink current in this design. In order to achieve class A performance against a negative EFT burst the regulator portion of this design would need to be modified or a reference solution should be included.

Table 10. IEC61000-4-4 Results

Orientation	Result	Class
Positive	Pass	A
Negative	Pass	B

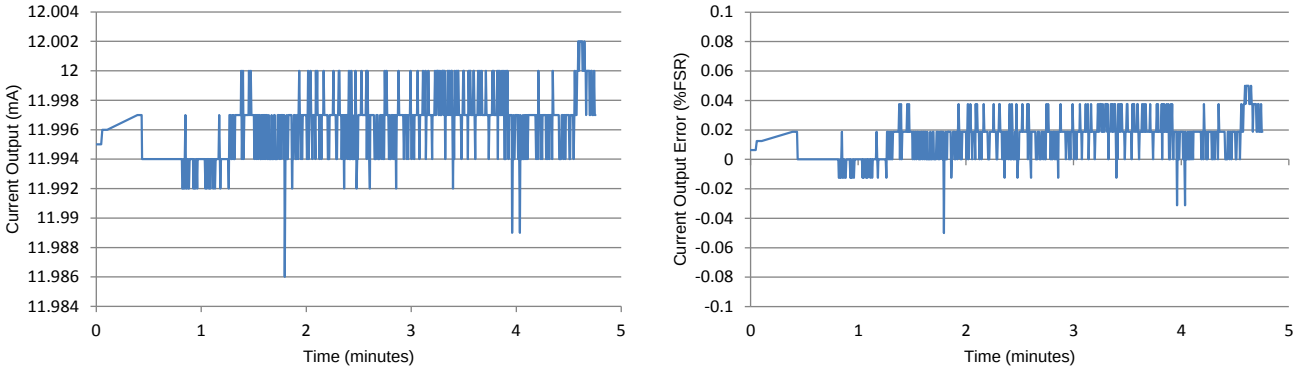

Figure 22: Current Output – +4kV EFT Pulse Measurements

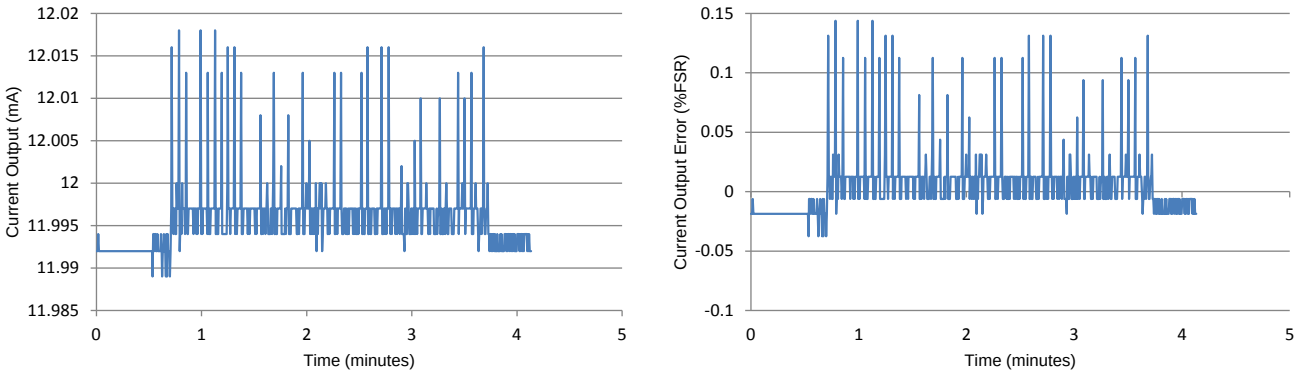

Figure 23: Current Output – -4kV EFT Pulse Measurements

7.4 IEC 61000-4-6: Conducted Immunity

The conducted immunity tests at 10 V/m field strength caused no significant deviations in the current output. The system passed the conducted immunity test with a class A rating. Figure 24 shows the measured output during the CI tests.

Table 11. IEC61000-4-6 Results

Test	Result	Class
10 V/m CI	Pass	A

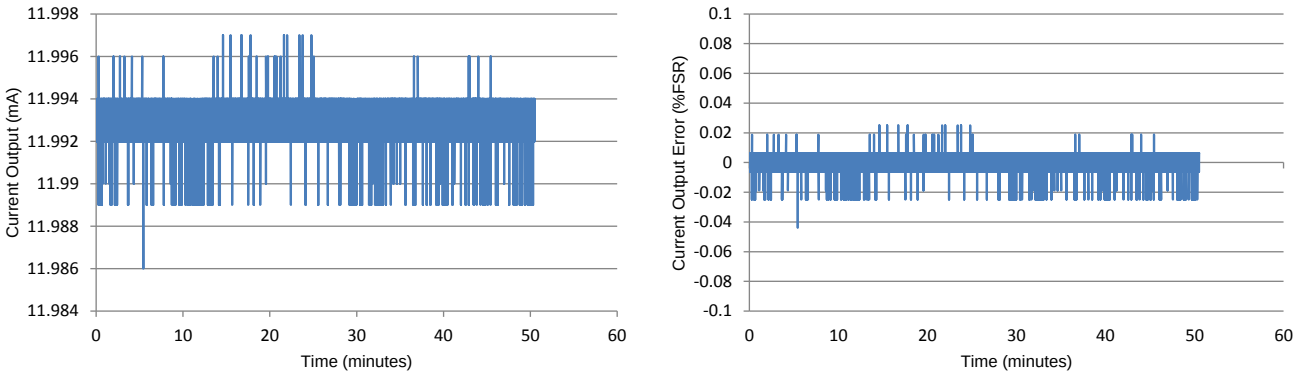

Figure 24: Current Output – 10 V/m CI Measurements

8 Modifications

The DAC7311 is part of a family of DACs that provides options for 8, 10, 12, 14, and 16 bits of resolution enabling other tiers of performance. These sibling devices are pin-to-pin compatible and implement compatible serial interfaces.

Table 12. Directly Compatible DACs

Device	Resolution	Offset Error (Typ)	Gain Error (Typ)	DNL Error (Typ)	INL Error (Typ)
DAC5311	8-Bits	0.05 mV	0.05 %FSR	0.01 LSB	0.01 LSB
DAC6311	10-Bits	0.05 mV	0.05 %FSR	0.03 LSB	0.06 LSB
DAC7311	12-Bits	0.05 mV	0.05 %FSR	0.2 LSB	0.3 LSB
DAC8311	14-Bits	0.05 mV	0.05 %FSR	0.125 LSB	1 LSB
DAC8411	16-Bits	0.05 mV	0.05 %FSR	0.5 LSB	4 LSBs

There are several alternate amplifiers that can be used in place of the OPA317 that offer lower input offset voltage (V_{OS}), lower input offset voltage drift, increased gain-bandwidth product (GBW), higher common-mode rejection ratio (CMRR), or higher power-supply rejection ratio (PSRR) that may provide marginal performance enhancements to this system for increased cost. Some alternate devices are shown in Table 13.

Table 13. Alternate Amplifiers

Device	V_{OS} (MAX)	V_{OS} Drift (Typ)	GBW (Typ)	CMRR (Min)
OPA317	0.1 mV	0.05 µV/C	300 kHz	95 dB
OPA330	0.05 mV	0.02 µV/C	350 kHz	100 dB
OPA333	0.01 mV	0.02 µV/C	350 kHz	106 dB
OPA334	0.005 mV	0.02 µV/C	2 MHz	110 dB
OPA335	0.005mV	0.02 µV/C	2 MHz	110 dB

The primary contributor to error in this system is the initial accuracy of the TL431B shunt regulator since the DAC7311 uses its supply voltage as a reference voltage. However, the use of a simple regulator is also a key contributor to keep system cost low. In systems that require greater accuracy a higher accuracy regulator solution or reference device can be included at increased system cost.

An option to enhance system performance without increasing component cost is to modify the resistor values of R_2, R_3, R_4, and R_5 such that the output span is wider than 4-20 mA and use a two-point offset calibration to remove gain and offset errors at the cost of some input codes (decreased resolution) while still covering the full 4-20 mA span. In this case the only remaining error is caused by the INL performance of the DAC7311 and the non-linearity of the TL431B regulator voltage caused by changes in cathode current across the system transfer function. Figure 25 illustrates the performance of a system calibrated for offset and gain errors, achieving TUE within 0.04% FSR.

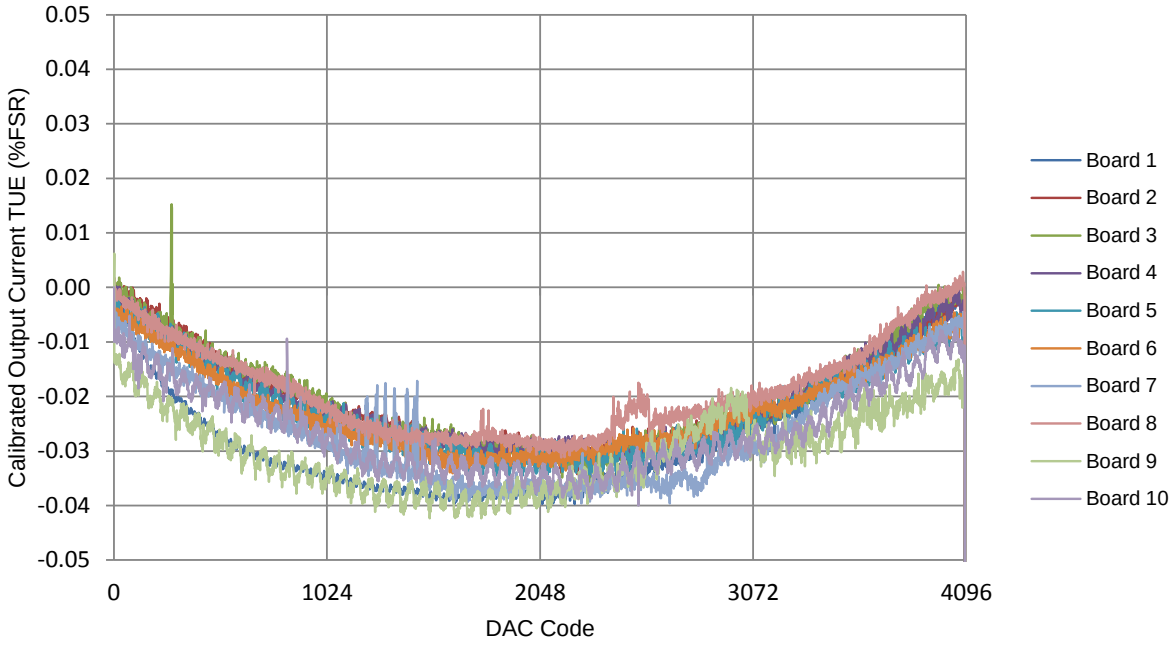

Figure 25: Calibrated Output Current Error

9 About the Author

Kevin Duke is an applications engineer in the precision digital to analog converters group at Texas Instruments where he supports industrial and catalog products and applications. Kevin received his BSEE from Texas Tech University.

10 Acknowledgements & References

The author wishes to acknowledge NTS (National Technical Systems) in Plano, TX for their assistance performing the electromagnetic compatibility tests.

Additional thanks to Collin Wells and Tim Green for their contributions to this design.

1. *IEC Publication 61000-4-2 "Electromagnetic Compatibility (EMC) – Part 4-2: Testing and Measurement Techniques – Electrostatic Discharge Immunity Test," International Electrotechnical Commission, 2008.*

2. *IEC Publication 61000-4-3 "Electromagnetic Compatibility (EMC) – Part 4-3: Testing and Measurement Techniques – Radiated, Radio-Frequency, Electromagnetic Field Immunity Test," International Electrotechnical Commission, 2006.*

3. *IEC Publication 61000-4-4 "Electromagnetic Compatibility (EMC) – Part 4-4: Testing and Measurement Techniques – Electrical Fast Transient/Burst Immunity Test," International Electrotechnical Commission, 2012.*

4. *IEC Publication 61000-4-6 "Electromagnetic Compatibility (EMC) – Part 4-6: Testing and Measurement Techniques – Immunity to Conducted Disturbances, Induced by Radio-Frequency Fields," International Electrotechnical Commission, 2008.*

5. *IEC Publication 61000-4-5 "Electromagnetic compatibility (EMC) - Part 4-5: Testing and measurement techniques - Surge immunity test," International Electrotechnical Commission, 2012.*

6. *H. Ott, Electromagnetic Compatibility. John Wiley & Sons Inc., 2009.*

Appendix A.

A.1 Electrical Schematic

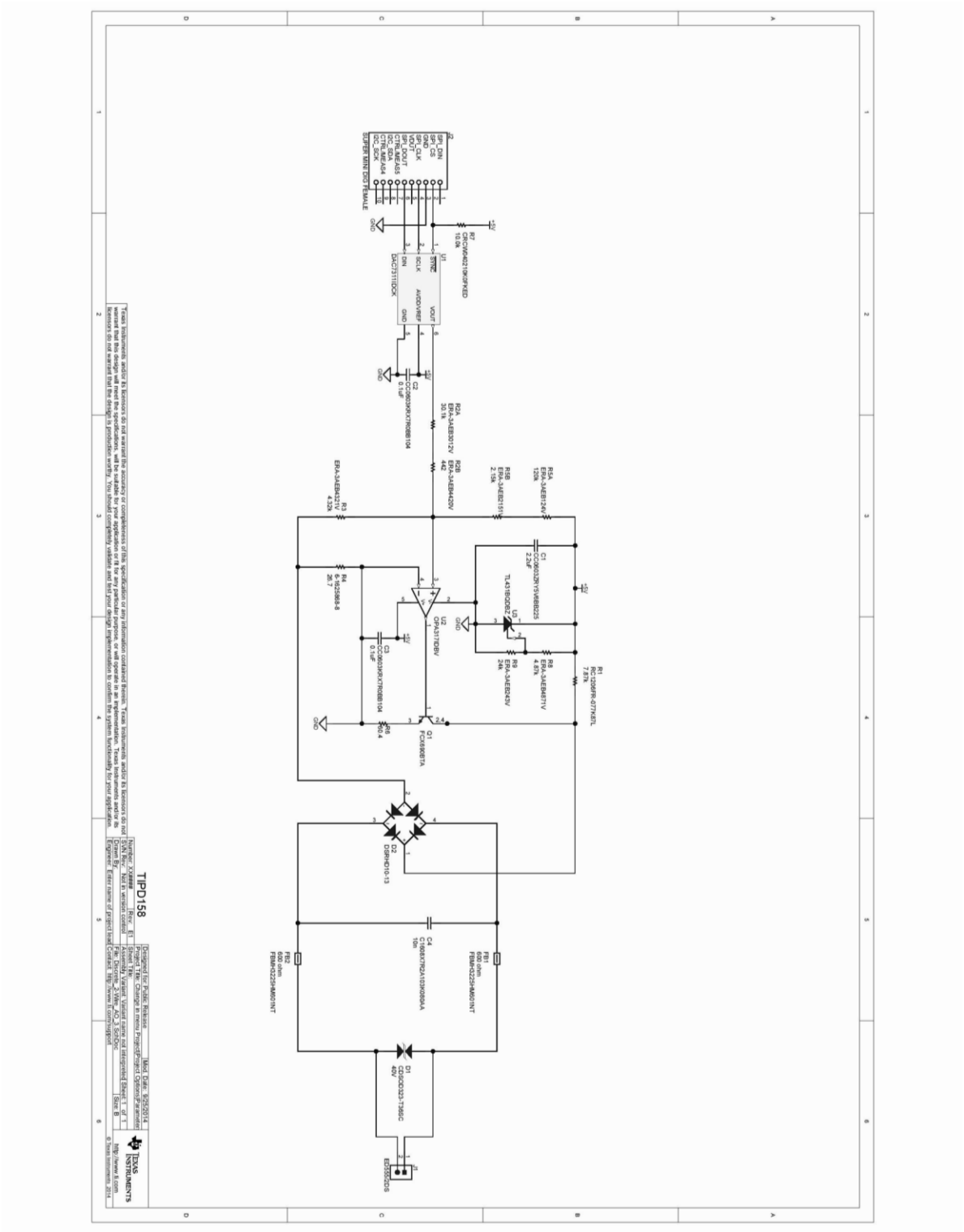

Figure A-1: Electrical Schematic

A.2 Bill of Materials

TEXAS INSTRUMENTS

Bill of Materials

TI DESIGNS

TIPD158: Low Cost Loop-Powered 4-20mA Transmitter, EMC/EMI Tested

Item	Quantity	Designator	Description	Manufacturer	PartNumber
0	1	C1	CAP CER 2.2UF 10V Y5V 0603	Yageo	CC0603ZRY5V6BB225
1	2	C2, C3	CAP CER 0.1UF 100V 10% X7R 0603	Yageo	CC0603KRX7R0BB104
2	1	C4	CAP CER 10000PF 100V X7R 0603	TDK	C1608X7R2A103K080AA
3	1	D1	TVS DIODE 36VWM 60VC SOD323	Bourns Inc	CDSOD323-T36SC
4	1	D2	Diode, Switching-Bridge, 1000V, 1A, 5.0x1.21x6.2mm	Diodes Inc.	DSRHD10-13
5	2	FB1, FB2	3A Ferrite Bead, 600 ohm @ 100MHz, SMD	Taiyo Yuden	FBMH3225HM601NT
6	1	J1	Terminal Block, 6A, 3.5mm Pitch, 2-Pos, TH	On-Shore Technology	ED555/2DS
7	1	J2	Receptacle, 50mil 10x1, R/A, TH	Mill-Max	851-43-010-20-001000
8	1	Q1	Transistor, NPN, 45V, 1A, SOT-89	Diodes Inc.	FCX690BTA
9	1	R1	RES 7.87K OHM 1/4W 1% 1206 SMD	Yageo	RC1206FR-077K87L
10	1	R2A	RES 30.1K OHM 1/10W .1% 0603 SMD	Panasonic	ERA-3AEB3012V
11	1	R2B	RES 442 OHM 1/10W .1% 0603 SMD	Panasonic	ERA-3AEB4420V
12	1	R3	RES 4.32K OHM 1/10W .1% 0603 SMD	Panasonic	ERA-3AEB4321V
13	1	R4	RES 26.7 OHM 1/4W 0.1% 0805	TE Connectivity	6-1625868-8
14	1	R5A	RES 120K OHM 1/10W .1% 0603 SMD	Panasonic	ERA-3AEB124V
15	1	R5B	RES 2.15K OHM 1/10W .1% 0603 SMD	Panasonic	ERA-3AEB2151V
16	1	R6	RES 60.4 OHM 1/10W 1% 0603 SMD	Vishay-Dale	CRCW060360R4FKEA
17	1	R7	RES, 10.0k ohm, 1%, 0.063W, 0402	Vishay-Dale	CRCW040210K0FKED
18	1	R8	RES 4.87K OHM 1/10W .1% 0603 SMD	Panasonic	ERA-3AEB4871V
19	1	R9	RES 24K OHM 1/10W .1% 0603 SMD	Panasonic	ERA-3AEB243V
20	1	U1	2.0V to 5.5V, 80µA, 12-Bit, Low-Power, Single-Channel, Digital-to-Analog Converters in SC70 Package, DCK0006A	Texas Instruments	DAC7311IDCK
21	1	U2	Low-Offset, Rail-to-Rail I/O Operational Amplifier, DBV0005A	Texas Instruments	OPA317IDBV
22	1	U3	PRECISION PROGRAMMABLE REFERENCE, DBZ0003A	Texas Instruments	TL431BQDBZ

Figure A-2: Bill of Materials

Appendix B.

B.1 IEC61000-4 Photos

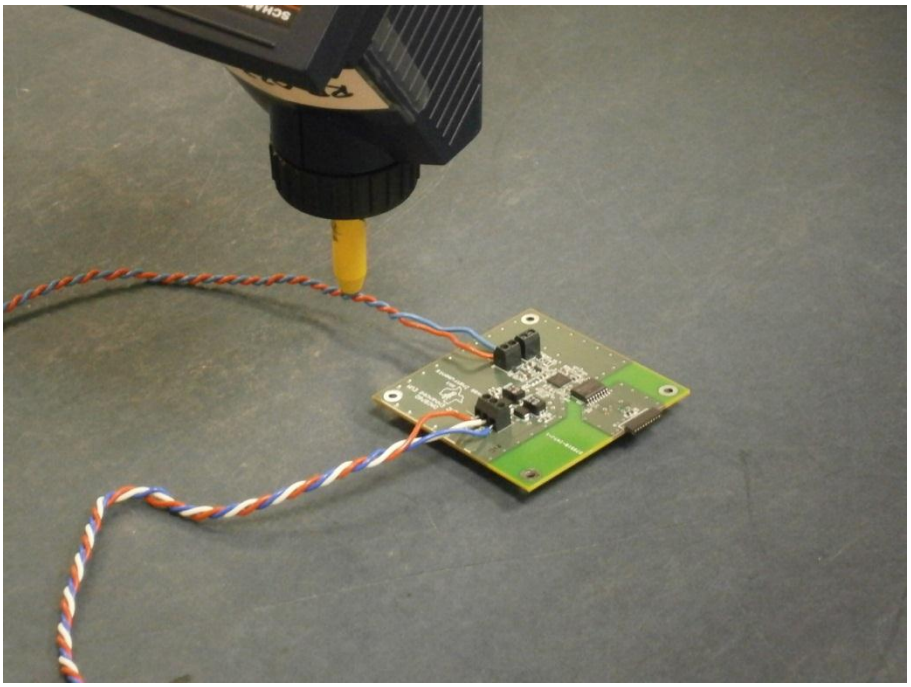

Figure B-1: 15kV ESD Air Discharge

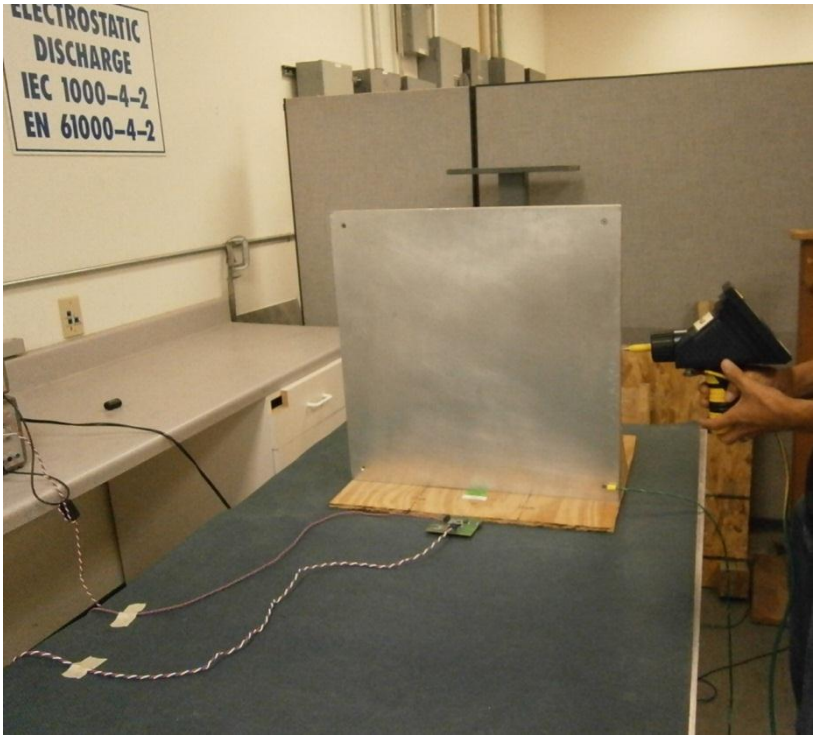

Figure B-2: 8kV ESD Vertical Contact Discharge

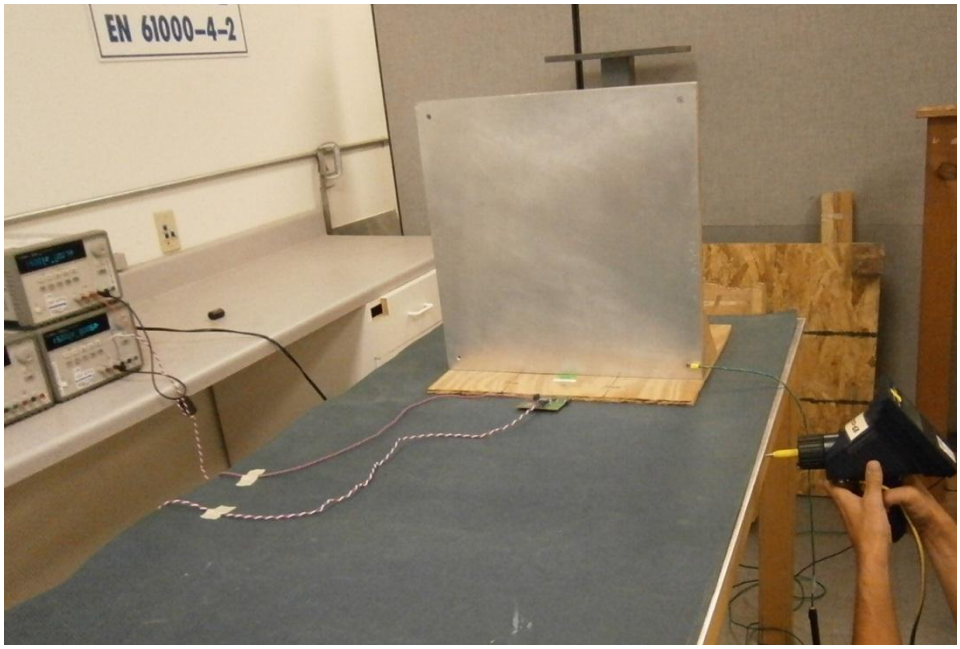

Figure B-3: 8kV ESD Horizontal Contact Discharge

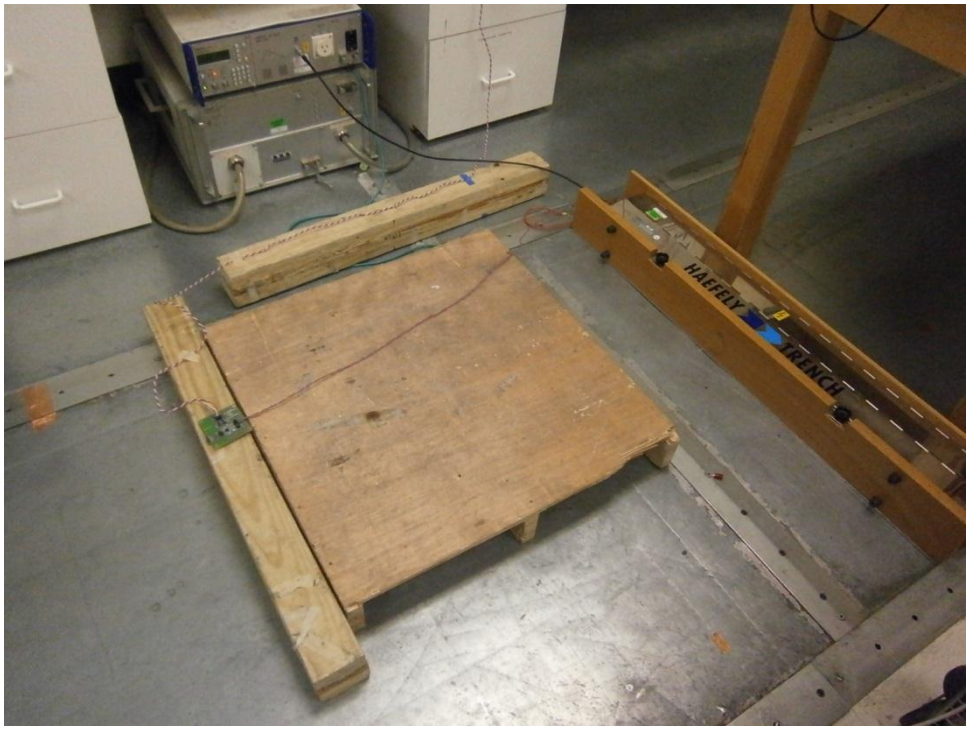

Figure B-4: EFT Test Setup

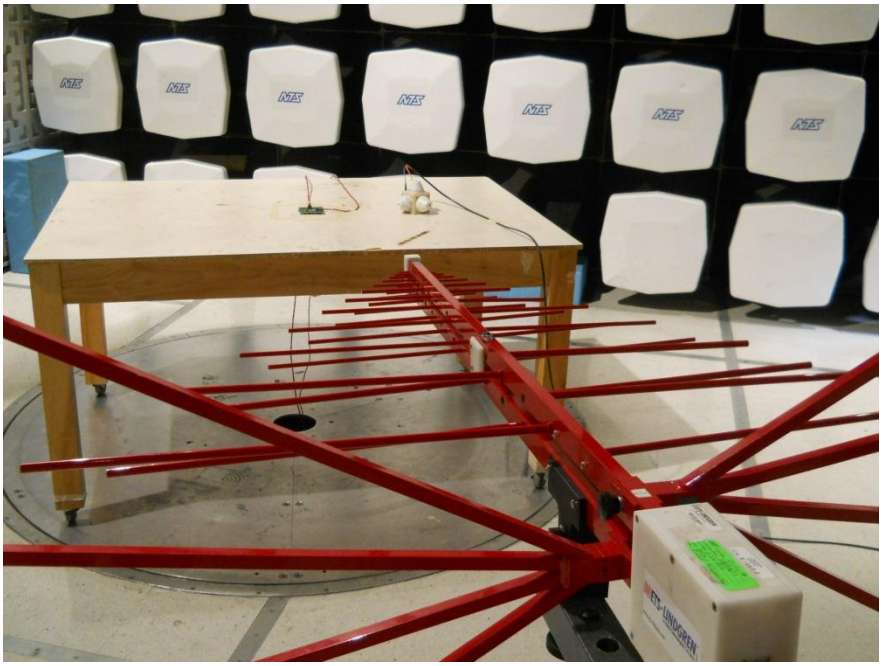

Figure B-5: Horizontal Radiated Immunity

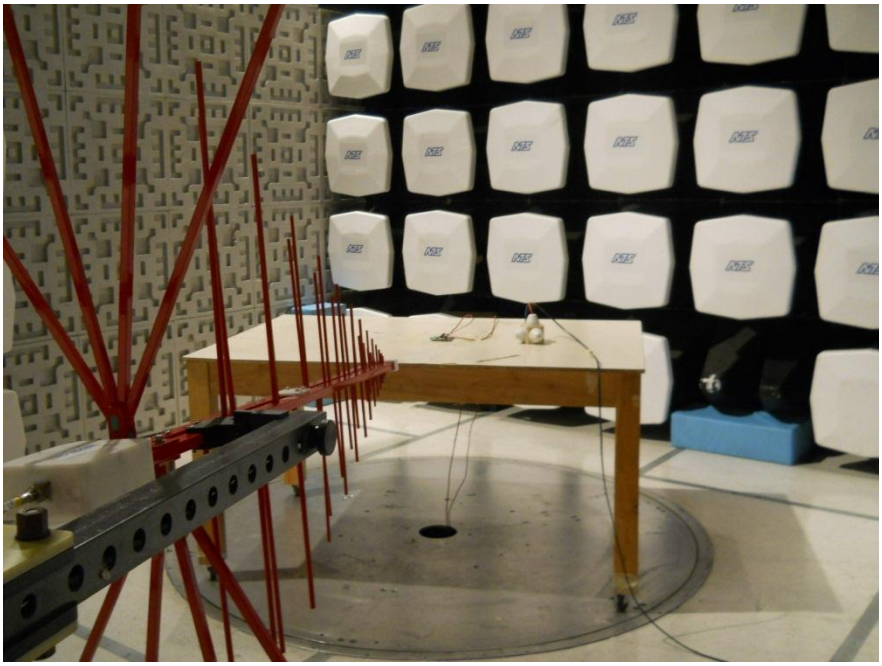

Figure B-6: Vertical Radiated Immunity

Appendix C.

C.1 Measured Differential and Integral Non-Linearity

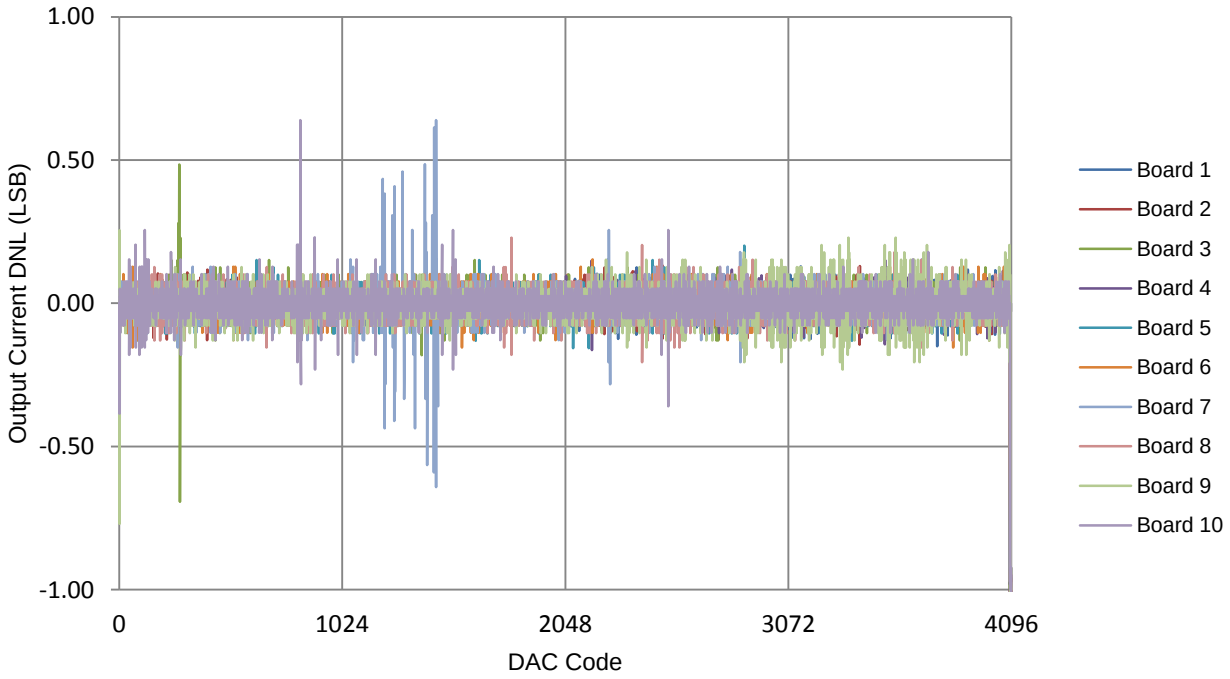

Figure C-1: Current Output Differential Non-Linearity (DNL)

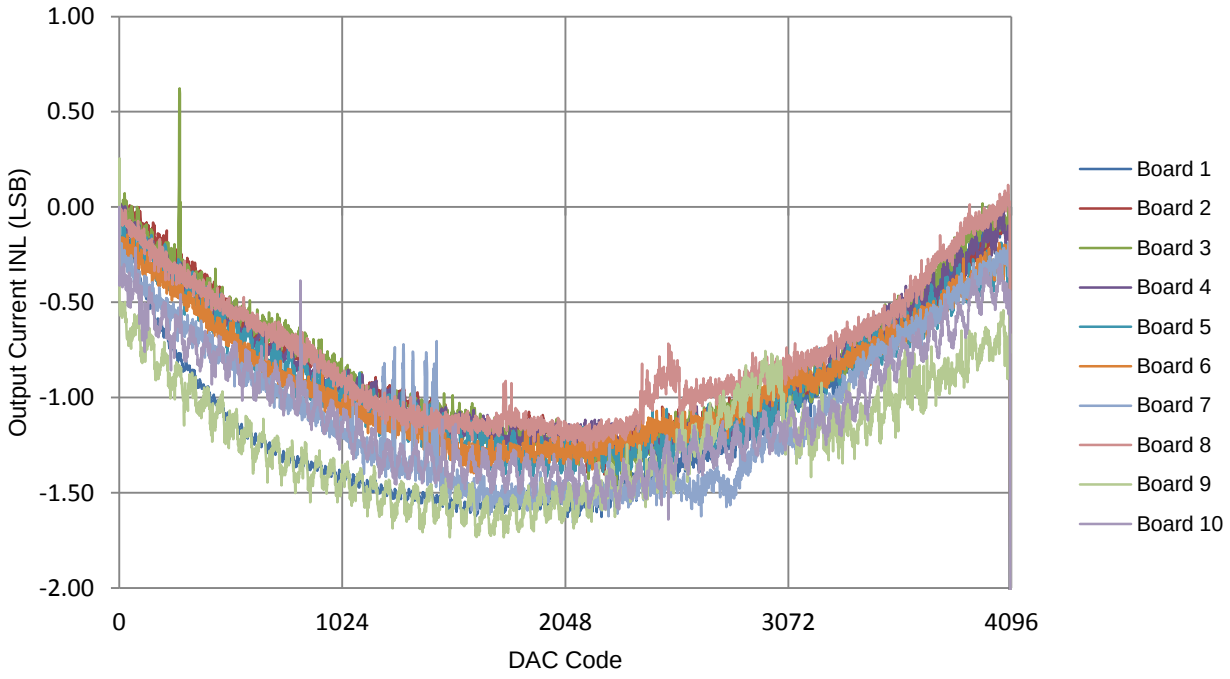

Figure C-2: Current Output Integral Non-Linearity (INL)

System DNL performance is as expected but a second-order non-linearity is revealed by studying the INL of the system. To understand the source of this INL error further measurement must be made. Figure C-3 below shows several error curves collected on a single unit.

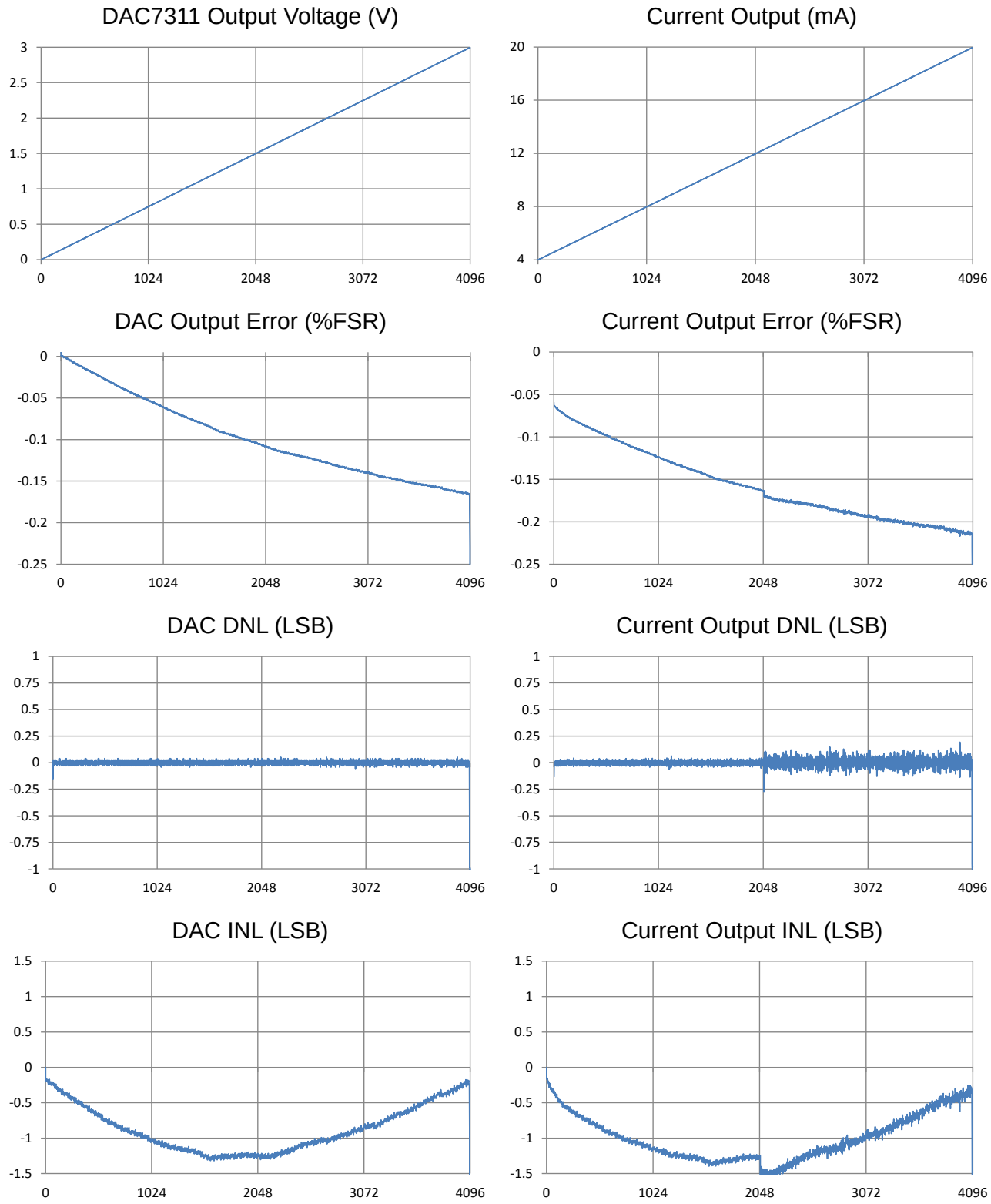

Figure C-3: DAC7311 Output and System Output Curves vs. Input Code

The results in Figure C-3 indicate that the second-order INL error of the system output can be linked back to the DAC7311 voltage output exceeding the maximum INL error specified in its datasheet around mid-scale. Further measurement on the TL431B regulator voltage across the transfer function provides more insight to the cause of this error.

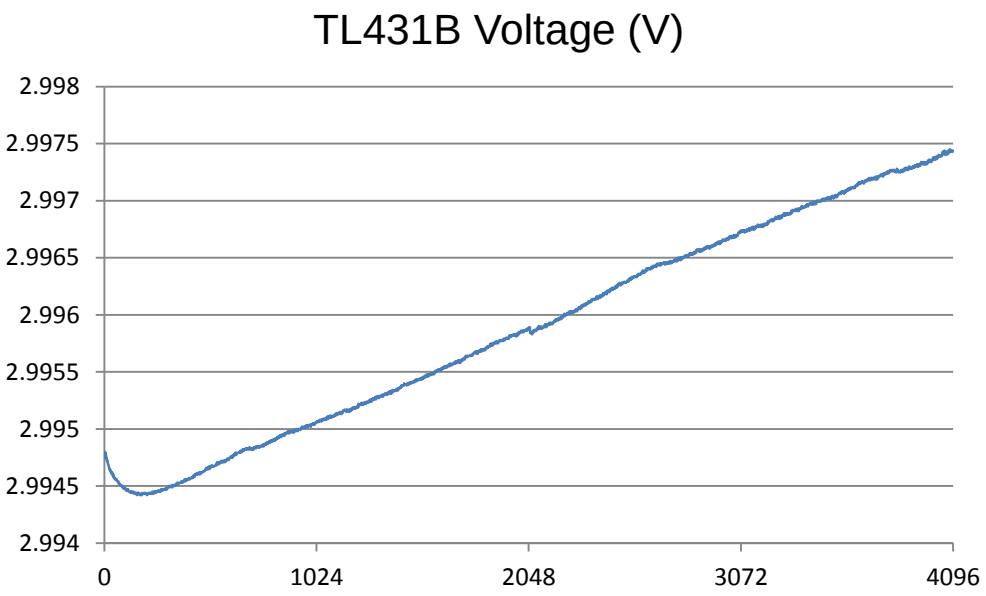

Figure C-4: TL431B Regulator Voltage vs. Input Code

The results in Figure C-4 show regulator voltage drift of 3 mV across the system transfer function. The error curves shown in Figure C-5 are generated by using these regulator voltage values of V_{REG} in the system transfer function defined by Equation (4) where the resistor values, op amp parameters, and DAC parameters are all ideal and therefore removed as potential sources of non-linearity error.

The curves in Figure C-5 align very well with the curves in Figure C-3, confirming that the regulator voltage drift of the TL431B is the source of the non-linearity error observed at the system output.

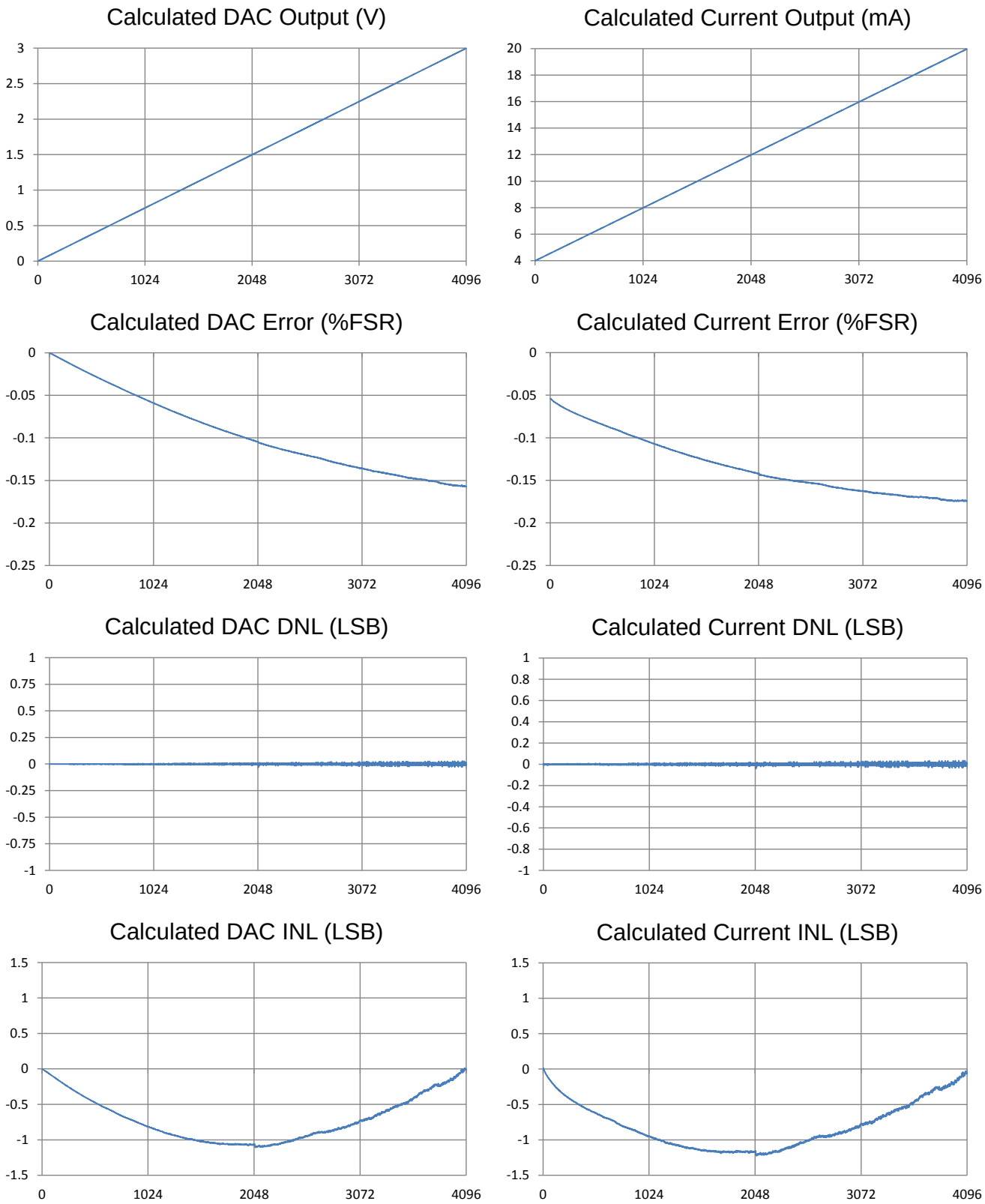

Figure C-5: Calculated DAC7311 Output & Calculated System Output Curves vs. Input Code

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