TEXAS INSTRUMENTS INC.

HIGH SPEED AMPLIFIERS

Design Guide

Versatile Sample & Hold Circuit for Industrial and T&M Applications

Pavol Balaz

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1. Introduction

The OPA615 is a complete subsystem for very fast and precise DC restoration, offset clamp-ing and low-frequency hum suppression of wideband amplifiers or buffers. The IC has been originally designed to stabilize the performance of video signals but it can be used in a variety of applications, for example as a high-speed integrator or as a peak detector for nanosecond pulses. The OPA615 can also be used as a sample and hold (S&H) amplifier. This design guide provides a basic description of the functionality of a S&H circuit and later focuses on S&H using the OPA615 providing detailed information on the circuit's operation and parameters. Also included are bench measurements and data analysis. Finally, this design guide discusses circuit and implementation limitations and possible improvements.

2. Basic Sample and Hold Amplifier Operation

A Sample & Hold (S&H) circuit consists of four major components: the input amplifier, energy storage device, output buffer and a switching component. The energy storage device - a capacitor - is the heart of the S&H circuit and it strongly affects the circuit's performance. The input buffer presents high impedance to the signal source and provides a current gain to charge the hold capacitor (C_H). This can be achieved with either current or voltage mode amplifiers. The latter will provide a constant voltage to charge C_H, resulting in a RC charge/discharge pattern:

$$V_{C_H} = V_{SRC}(1 - e^{-\frac{t}{RC_H}}) \tag{2.1}$$

V_{C_H} is the voltage on the hold capacitor and V_{SRC} is the constant voltage at the output of the amplifier. After three RC_H time constants, the voltage at C_H would reach approx. 90% of V_{SRC}. It would converge to V_{SRC} for $t \to \infty$.

A current mode amplifier would charge the hold capacitor using a constant current (I_{SRC}), thus resulting in a linear increase of the capacitor voltage:

$$\frac{dV_{C_H}}{dt} = \frac{I_{SRC}}{C_H} \tag{2.2}$$

Consequently, current mode (transconductance) implementations will have faster settling than voltage mode variants.

As the name of the circuit suggests, there are two modes of operation. In the **Sample** (also commonly known as **Track**) mode, the voltage on the hold capacitor (C_H) follows the input signal - with a certain delay and bandwidth limitation. In the **Hold** mode, the capacitor is disconnected from the input signal and it is supposed to hold the voltage present before it was disconnected. The output buffer's high input impedance keeps the capacitor from discharging prematurely and the switching component controls the mode of operation.

Figure 2.1.: Block diagram of a voltage mode S&H circuit
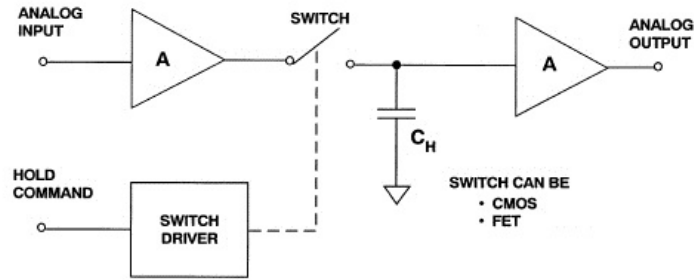
3. Sample and Hold with OPA615

The OPA615 features a wideband operational transconductance amplifier (OTA) and a fast and precise sampling OTA (SOTA), offering 710 and 730 MHz of bandwidth, respectively. The self-biased, bipolar OTA can be viewed as an ideal voltage-controlled current source and is optimized for low input bias current. The SOTA has two identical high-impedance inputs and a current source output optimized for low input bias current and offset voltage. Being current mode, the OPA615 intrinsically promises better AC performance than voltage mode architectures (see discussion in section 2). The schematic of a S&H circuit using the OPA615 is shown in figure 3.1.

In the sample (or track) mode, the voltage on C_H is adjusted to the real-time voltage level at the analog input by charging / discharging the capacitor using the constant current output of the SOTA (voltage controlled current source). Since the current charging / discharging the capacitor is constant, the resulting voltage change is linear (see section 2). The voltage feedback loop ensures that the SOTA slews fast enough to capture the correct voltage level at V_{IN}.

During the hold mode, the hold capacitor C_H is disconnected from the SOTA and is expected to retain the voltage present prior to the disconnection. The high input impedance of the OTA prevents the capacitor from discharging prematurely. Nevertheless, the voltage on C_H invariably changes due to parasitic elements. (see section 3.2).

The voltage on C_H is always reflected at the output V_{OUT} (2, emitter of the OTA). The mode of operation is controlled by a TTL-compatible switching stage (Hold Control pin).

Both the input and the output were matched to 50 Ω source / load respectively. The 100 Ω resistors between pin (3) and (4) and at pin (7) serve for de-Q-ing of the parasitic LC created by the trace (L) and package parasitic (C). The 125 Ω series at pin 10 serves dual purpose. Firstly, it is de-Q-ing parasitic LC (as above), secondly, it was selected to cancel output offset due to input bias current.

Figure 3.2 displays the S&H function being performed on a 100 kHz, 1 V_{PP} sine wave, using a sampling frequency of 1 MHz and a sampling period of 100 ns.

Figure 3.1.: Schematic of the S&H circuit using OPA615
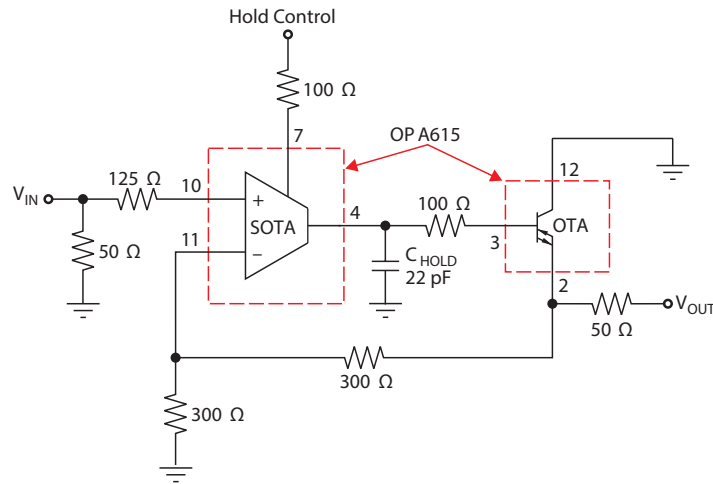

3.1. Track Mode Operation

In this mode, the main concerns are going to be bandwidth and stability. The S&H circuit in track mode behaves as a voltage feedback (VFB) amplifier. For more information on VFB behaviour and stability, please refer to [Man01].

In a simplified way, the SOTA acts as the input stage and the OTA as the output stage while the hold capacitor at the same times also provides dominant pole compensation and thus greatly affects the stability of the circuit. It also determines the available bandwidth. Other static and dynamic specifications in this mode are similar to those of any amplifier. Gain, offset, bandwidth, slew rate and settling time are among the main track mode specifications. Also, keep an eye on the internal node specifications such as the output voltage compliance of ± 3.5 V at the C_H pin (4), as it determines the maximum input signal voltage swing as well as the gain selection.

As mentioned above, the value of the hold capacitor C_H affects the available bandwidth as well the stability of the circuit. The circuit has been tested for bandwidth and stability with respect to the value of C_H. The results showing the available bandwidth and minimal possible gain are shown in table 3.1.

Figure 3.2.: S&H of a 100 kHz 1 V_{PP} sine wave,
sampling frequency = 1 MHz, sampling period = 100 ns, C_H = 22 pF
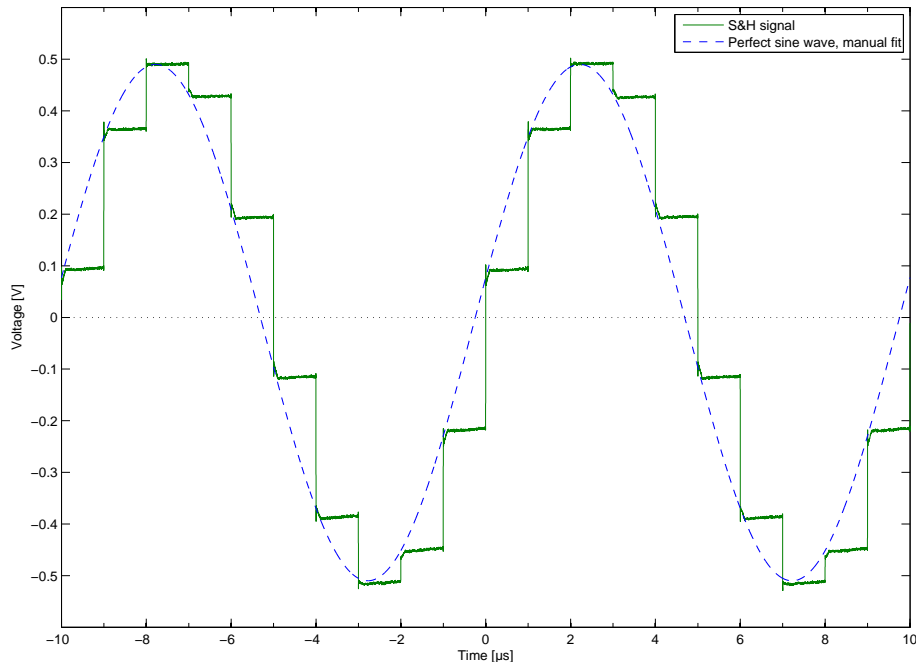
By reducing the value of C_H, which, as previously mentioned, provides dominant pole compensation, the S&H amplifier gets decompensated. This impacts the stability of the circuit and it begins to oscillate. To regain stability, other methods have to be applied to compensate the amplifier. The easiest and most straightforward approach is to increase the gain. This technique has been applied in the table above. The S&H amplifier at a gain of 2 $\frac{V}{V}$ was stable for a C_H value as low as 22 pF. Going below 22 pF required the gain to be increased. The gain shown in table 3.1 for $C_H < 22pF$ is the minimal gain required to achieve a peaking of < 2 dB and thus > approx. 50° phase margin. Since we have a voltage feedback loop (and thus a gain-bandwidth product), the increase in gain automatically results in a decrease in bandwidth. One has to achieve an acceptable compromise between stability and available bandwidth.

The gain of 2 $\frac{V}{V}$ (6 dB) was the center of attention throughout testing since the output has been matched to 50 Ω impedance, thus creating a -6 dB attenuation, resulting in an overall unity gain from input to load.

The circuit has been tested for unity gain as well and it was determined that throughout the tested C_H values, unconditional stability and flat frequency response were achieved for $C_H \geq$ 47 pF.

Furthermore, in addition to the value of C_H, the parasitic capacitance values of the output of the SOTA and the input of the OTA as well as parasitic layout capacitances have to be taken into account. This results in an additional capacitance of approximately 6.7 pF (1.2 pF SOTA out, 1.7 pF OTA in, 2*2 pF layout capacitance).

Table 3.1.: Bandwidth vs. C_H

| C_H [pF]	Gain [$\frac{V}{V}$]	BW [MHz]	R_F [Ω]	R_G [Ω]	Peaking [dB]
C_H vs. minimal possible gain & BW					
2	5	321.2	300	75	–
6	3	302.3	300	150	1.9
10	2.5	262.3	300	200	1.2
22	2	148.6	300	300	–
47	2	47.7	300	300	–
100	2	17.3	300	300	–
470	2	4.9	300	300	–
1000	2	2.2	300	300	–
Unity Gain Stability & BW					
22	1	273	300	N/A	7.5
47	1	145.6	300	N/A	0.32

The signal propagation delay is typically 1.9 ns and the output offset current is ±50 mA (track mode, S/H In± = 0 V).

3.2. Hold Mode Operation

Once the hold control pin turns low, the circuit enters the hold mode and the hold capacitor is disconnected from the input buffer. Ideally, the voltage at the hold capacitor C_H should retain the value present just prior to the disconnection. A simplified model of the S&H circuit in hold mode is shown in figure 3.3.

Figure 3.3.: Model schematic of the S&H circuit in the Hold mode
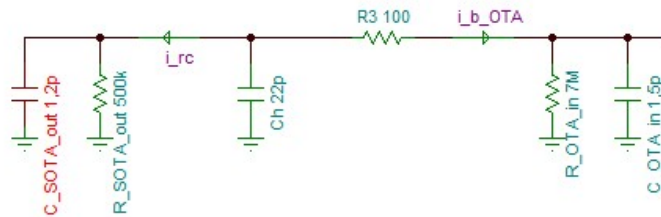
If a leakage current flows in or out of the hold capacitor C_H, it will slowly charge or discharge - depending on its polarity - and its voltage will change. This effect is known as droop and is expressed in $\frac{V}{\mu s}$. There are several factors causing the droop:

1. Input bias current of the OTA

2. RC discharge over SOTA output impedance

3. Leakage across PC board

4. Leaky capacitor

The dominant factor causing the droop is the input bias current of the OTA. Assuming it is a constant current, droop rate at the capacitor would result in:

$$\frac{dV_{C_H}}{dt} = \frac{i_b}{C_H} \tag{3.1}$$

Looking at the RC discharge and its derivative results in a time-variant droop rate at the capacitor:

$$V_{C_H} = V_{C_{H_0}} e^{-\frac{t}{RC_H}} \tag{3.2}$$

$$\frac{dV_{C_H}}{dt} = -\frac{1}{RC_H} V_{C_{H_0}} e^{-\frac{t}{RC_H}} \tag{3.3}$$

$$\frac{dV_{C_H}}{dt} = \frac{\pm i_b}{C_H} - \frac{1}{RC_H} V_{C_{H_0}} e^{-\frac{t}{RC_H}} \tag{3.4}$$

R is the output impedance of the SOTA (500 kΩ). It is evident that decreasing the capacitor value increases the droop rate. The other factors mentioned above also increase their effect with decreasing capacitor value. Also, depending on the length of the hold period and the RC_H time constant, the droop rate could show an exponential, time-variant character.

Droop rate measurements were performed using different C_H values. A sine wave with a frequency of 20 kHz and an amplitude of 500 mV was continuously sampled at its top (500 mV) and its bottom (-500 mV) respectively. The sampling period was 20 ns and the sampling rate 20 kHz, so that the same point was sampled every time.

Figure 3.4.: Droop rate vs. C_H

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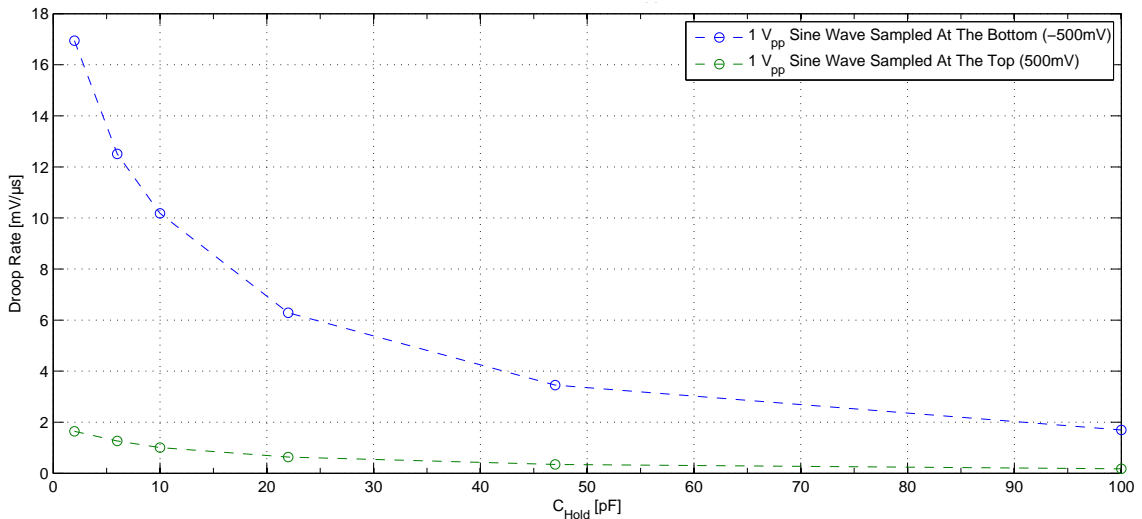
It was observed that the droop rate at the bottom of the sine wave was approximately ten-fold compared with the droop rate observed at the top of the sine wave. This is mainly due to the 2 reasons. First, the polarity of the input bias current of the OTA either reinforces or suppresses the other effects causing the droop. Since the input bias current of the OTA moves in a range of ± 0.9 μA, the opposite behavior could be observed with another device due to the Gaussian distribution of the input bias current values within the specified range. The second reason is the variation of the absolute value of the input bias current with the base voltage. Appendix A offers a more detailed discussion on input bias current of the OTA and droop rate. Additionally, it compares theory, simulation and bench measurements.

The capacitors used for the hold capacitor should have low leakage, but the dielectric absorption of the applied capacitor is equally important. It describes the fact that a capacitor recovers some of its charge when charged, discharged and then left open circuit. This phenomenon causes the remains of a previous sample to contaminate a new one and may introduce random errors of tens or even hundreds of mV. Different capacitor materials have differing amounts of dielectric absorption. Mica, polystyrene and polypropylene capacitors show the lowest rates of dielectric absorption (0.05% to 0.1%) while electrolytic capacitors show the highest rates (2% to 15%). Ceramic capacitors are placed in between with rates of 0.3 to 0.6% for class-1, NP0 and 2.0 to 2.5% for class-2, X7R capacitors. Please note that polarized capacitors cannot be used here.

Another important factor is the feedthrough, which is an effect caused by strayed capacitance where small amount of the ac input is coupled to the output during hold. The feedthrough rejection is given as 100 dB for a input signal of 1 V_{PP} and f < 20 MHz. However, this is not expected to be the main contributor of the error observed in hold mode.

3.3. Track/Hold and Hold/Track Transitions

During the Track/Hold transition, when the S&H circuit switches from track to hold, there is a small amount of charge dumped on the hold capacitor due to non-ideal switches. This hold mode DC offset voltage is called pedestal error. The typical charge injected on the hold capacitor by the OPA615 during this transition is 40 fC. The resulting offset voltage can be calculated as:

$$\Delta V_{C_H} = \frac{\Delta Q}{C_H} \tag{3.5}$$

This would result in an offset voltage of approx. 2 mV for a 22 pF hold capacitor with 40 fC of injected charge.

Furthermore, it should be considered that there is a propagation delay between the hold control input of the OPA615 and the switch connecting / disconnecting the hold capacitor. This delay is called control propagation delay and it gives the time from the edge of the hold control signal to the completion of the corresponding action at the switch (signal runtime plus time to close / open the switch). It is typically 2.5 ns. Given the signal propagation delay of 1.9 ns there

is a resulting timing error of 0.6 ns. Thus, this establishes when the input signal is actually sampled with respect to the sampling clock edge.

When switching from Hold to Track mode, the S&H circuit must reacquire the input signal. The interval of time required to reacquire the signal to a desired accuracy is called acquisition time. The interval starts at the 50% point of the sampling clock edge and ends when the S&H amplifier output voltage falls within the specified error band. The settling time depends on the voltage difference between the old and the new sample, the value of the hold capacitor and the stability of the S&H circuit. The latter causes overshoot and ringing which increase the acquisition time. The first part of the acquisition consists of charging / discharging the hold capacitor to the value of the new sample. The charging / discharging is performed by the constant current at the SOTA's output. This results in a linear increase of voltage at the hold capacitor. The transconductance of the SOTA is typically 35 $\frac{mA}{V}$ (see figure 19 and 22 in the OPA615 datasheet), the maximal output current at the C_{HOLD} pin is at least ± 3 mA.

Below is an example of a hold to track transition showing the S&H being performed on a 100 kHz, 1 V_{PP} sine wave with a sampling frequency of 1 MHz and a sampling period of 20 ns. The hold capacitor was 22 pF and the gain was 2 (RF = RG = 300 Ω). Doing a simple analytical approach, the linear increase of the hold capacitor voltage is due to the constant current at the output of the SOTA, hence:

$$\frac{dV_{C_H}}{dt} = \frac{i_{SOTA}}{C_H} \tag{3.6}$$

C_H is the capacitor value and i_{SOTA} is the current at the output of the SOTA. Using the values give above, this would result in a slope of approx. 130 $\frac{V}{\mu s}$ which corresponds to the value shown in the figure, given the fact that there is constant leakage the capacitor. In the figure, there is a voltage increase of approx. 0.36 V within a time period of approx. 4 ns, resulting in the shown value of 90 $\frac{V}{\mu s}$.

4. Conclusion and Outlook

This application report describes a simple and straightforward way to build a S&H circuit using TI's OPA615 wide-bandwidth, DC restoration circuit. Using the information provided in this report, the user should be able to rebuild this circuit and adjust it according to the given requirements. This circuit still leaves room for improvements, for example when it comes to the droop rate / precision of the hold period. The relatively high bias current of the OTA is based on its bipolar manufacturing process. The OTA could be replaced by an operational amplifier with a FET input stage, thus reducing the bias current by three orders of magnitude (pA compared to μA). Suitable devices would be, for example, the OPA656 or OPA659, depending on the speed and quiescent current requirements.

Figure 3.5.: Example showing the Hold / Track transition,
$C_H = 22$ pF, G = 2, $f_{IN} = 100$ kHz, $f_S = 1$ MHz
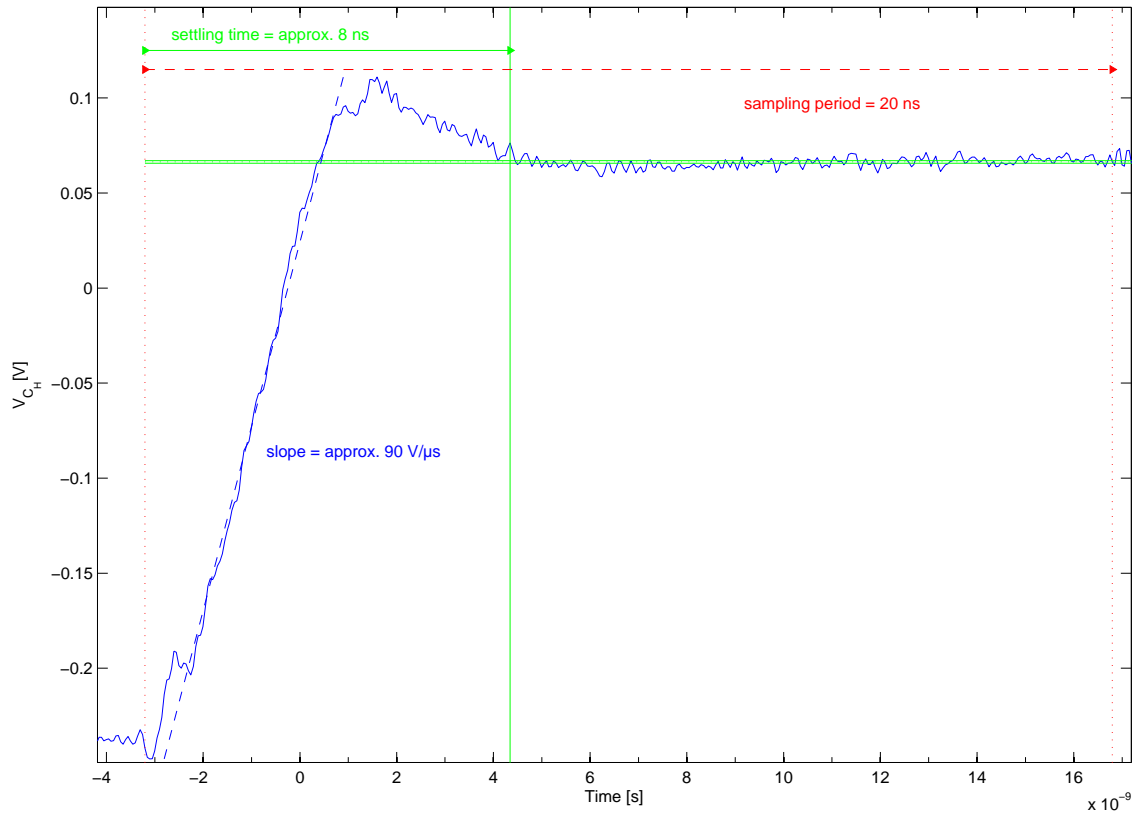
Using guard rings would further improve the droop rate by reducing the leakage current in the PCB. A guard ring is a ring of conductor which surrounds a sensitive node and is at the same potential, thus denying the flow of leakage current. The surface resistance of PCB material is much lower than its bulk resistance, so guard rings must always be placed on both sides of a PCB. On multilayer boards, guard rings should be present in all layers.

One possible application of the described circuit with the aforementioned improvements is settling time measurement with a precision of above 0.1%, as described in [RL12].

Appendix A.

Droop Rate and OTA Bias Current - Theory, Simulation, Measurements

This appendix discusses in detail the difficulties during Hold Mode Operation (see chapter 3.2), especially those related to the voltage droop during hold. It reiterates the theory, shows and discusses multiple simulations, provides bench measurements and eventually theory, simulation and bench results.

A.1. Theory

As stated in section 3.2, leakage current flowing in or out of the hold capacitor during hold mode will charge or discharge the capacitor and thus change its voltage. This effect is called voltage droop. There are several factors causing the droop:

1. Input bias current of the OTA

2. RC discharge over SOTA output impedance

3. Leakage across PC board

4. Leaky capacitor

The dominant factor causing the droop is the input bias current of the OTA. **Assuming it is a constant current**, droop rate at the capacitor would result in:

$$\frac{dV_{C_H}}{dt} = \frac{i_b}{C_H} \tag{A.1}$$

Looking at the RC discharge and its derivative results in a time-variant droop rate at the capacitor:

$$V_{C_H}(t) = V_{C_{H_0}} e^{-\frac{t}{RC_H}} \tag{A.2}$$

$$\frac{dV_{C_H}(t)}{dt} = -\frac{1}{RC_H} V_{C_{H_0}} e^{-\frac{t}{RC_H}} \tag{A.3}$$

$$\frac{dV_{C_H}(t)}{dt} = \frac{\pm i_b}{C_H} - \frac{1}{RC_H} V_{C_{H_0}} e^{-\frac{t}{RC_H}} \tag{A.4}$$

These equations provide a very simple first order model (ignoring leakage through PC board and capacitor). Simulations, were performed to further verify this model. The said simulations were explicitly defined to address and emphasize this problem.

A.2. Simulation

Figure A.1 shows the TINA schematic of the Sample and Hold circuit which has been used during the simulations. The gain was set to 2 $(1+\frac{300\Omega}{300\Omega})$, the output is terminated to 50 Ω. The hold capacitor has been set to 28.7 pF. This value results from adding 6.7 pF parasitic capacitance on top of a standard 22 pF capacitor (1.2 pF SOTA output + 1.7 pF OTA input + 2*2 pF layout capacitance = 6.7 pF).

Figure A.1.: TINA schematic showing the circuit used for droop rate measurements
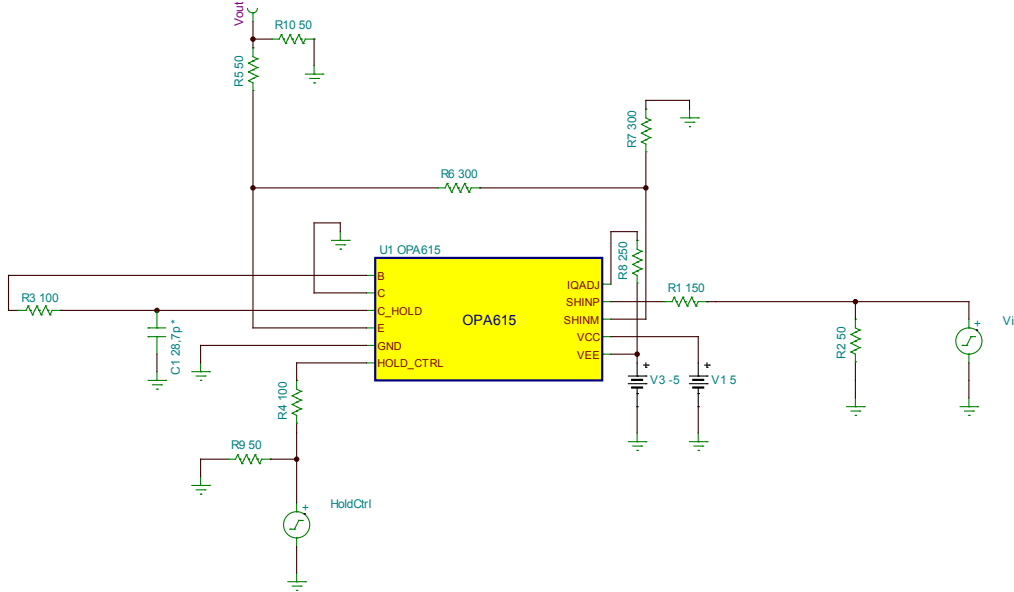
Figure A.2 shows the simulation results sampling a 2 kHz, 1 V_{PP} sine wave at a sampling frequency of 20 kHz, using a sampling period of 20 ns and a rise and fall time of the mode control signal of 5 ns.

The plot shows the sine wave input (red curve), the sample and hold output curve (green) and the mode control signal (grey). Looking at the sample and hold curve, it becomes obvious that the droop rate changes with the voltage taken sample. Also, the voltage drop (regarding one

Figure A.2.: Simulation - 2 kHz Sine Wave Sampled at 20 kHz, 20 ns Sampling Time, $C_H = 28.7$ pF
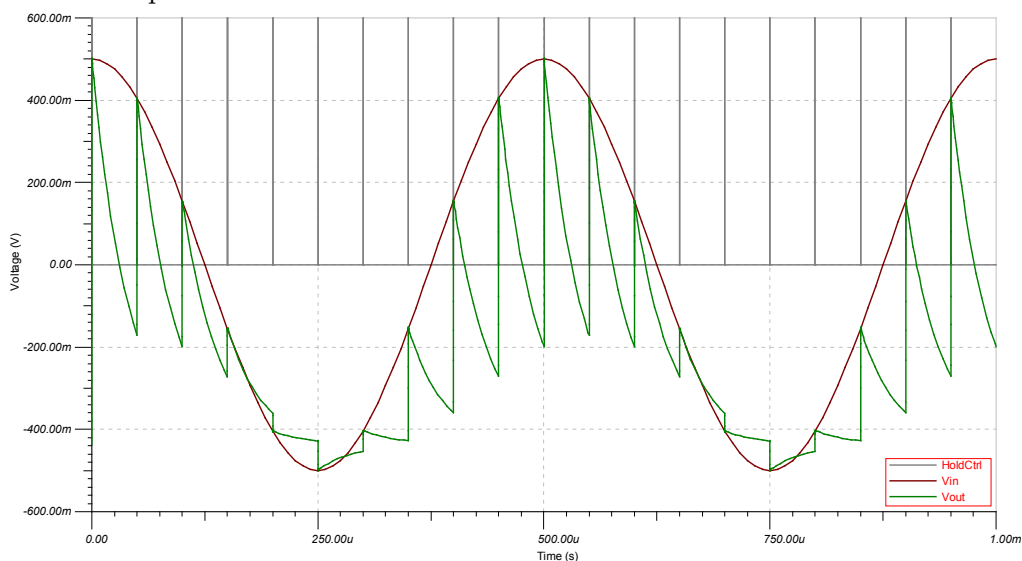
hold period) is not linear. Given the fact that the equations have an exponential part (RC discharge) to them would explain that fact. However, the big change in droop rate across the voltage values of the sine wave (-1 ... 1V at the hold capacitor - keep in mind the gain of 2)) is curious. Looking back at the enumeration of factors causing the droop, on the first glance, only the first two factors (input bias current of the OTA, RC discharge) seem to be relevant in the simulation since leakage across the PC board and capacitor are not part of the TINA simulations.

For this reason, an ideal buffer has been added between the hold capacitor and the OTA base input to nullify the effect of the OTA base input bias current. The circuit can be seen in figure A.3. Simulations have been performed sampling a 20 kHz, 1 V_{PP} sine wave using a sampling frequency of 20 kHz. The phase of the sine wave has been adjusted so that the sine wave is sampled at its positive peak (since figure A.2 shows that the droop rate is highest when sampling at 500 mV).

The simulation results using different hold capacitor values can be seen in figure A.4. It becomes evident that the droop rate drops to (almost) zero. The glitches which can be seen at the sampling points are most probably due to the charge injection (see chapter 3.3). This means that, in simulation, the only source of droop is the bias current of the OTA base input. From this follows that the **base current is not constant and that there is a correlation between the voltage at the base of the OTA and the base bias current**.

Following this, further investigations have been performed in regard to the bias current of the base of the OTA and its dependency towards the base voltage. Figure A.4 shows the simulation circuit. The SOTA inputs have been grounded as well as its output and the collector of the OTA. The feedback looped has been opened, completely isolating the OTA from the SOTA. The base voltage has been varied from -3 to 3 V and the bias current has been measured using an ammeter. Since, on the bench, the input current would be measured as a voltage drop across

Figure A.3.: Schematic including an ideal buffer in front of the OTA Base Input
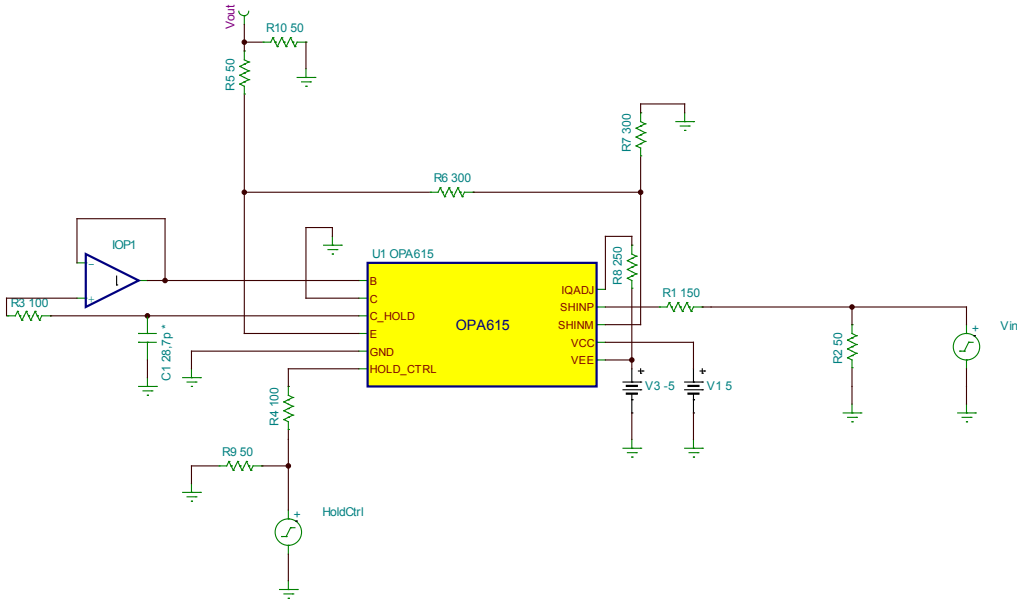
a resistor, additional simulations including a series resistor (100k and 2M, respectively) have been performed to verify the effect of the added series resistance on the input bias current.

Figure A.6 shows the results. It becomes evident that the input bias current of the base changes its absolute value and its polarity depending on the base voltage. The change in polarity occurs at a base voltage of around -1 V. This is also evident when looking at figure A.2. The droop rate shown there is negative for every sample except for the one at -500 mV (-1 V at the capacitor; Gain = 2 V/V). The droop rate increases with the sample voltage. The absolute value of the bias current does the same. This means that the non-linear and voltage-dependent nature of the droop rate is solely dependant on the base voltage dependent nature of the base input bias current; at least in simulation.

To conclude the simulations, the actual droop rate values have been calculated. A 20 kHz, 1 V_{PP} sine wave has been sampled using a sampling frequency of 20 kHz. The phase of the sine wave has been adjusted so that it was sampled at its maximum (500 mV) and its minimum (-500 mV), respectively. When it comes to droop rate, sampling at 500 mV (1 V at the hold capacitor; Gain = 2) is the worst case scenario for a 1 V_{PP} sine wave whereas sampling at -500 mV (-1 V at the hold capacitor; Gain = 2 V/V) is the best case scenario overall (see figure A.6). The droop rates have been calculated for different hold capacitor values (2, 6, 10, 22, 47, 100 pF) while always adding 6.7 pF parasitic capacitance. The droop rate has been calculated as difference between the sampled voltage and the voltage at the end of the adjacent hold period and the divided by the hold period duration (50 μs - 20 ns). As expected, the droop rate is also dependent on the hold capacitor value - the lower the cap value, the higher the droop rate (see equations in section A.1).

Figure A.4.: Simulation - 20 kHz Sine Wave Sampled at 20 kHz, 20 ns Sampling Time, $C_H =$ 2 pF ... 100 pF, **Ideal Buffer at OTA Base Input**
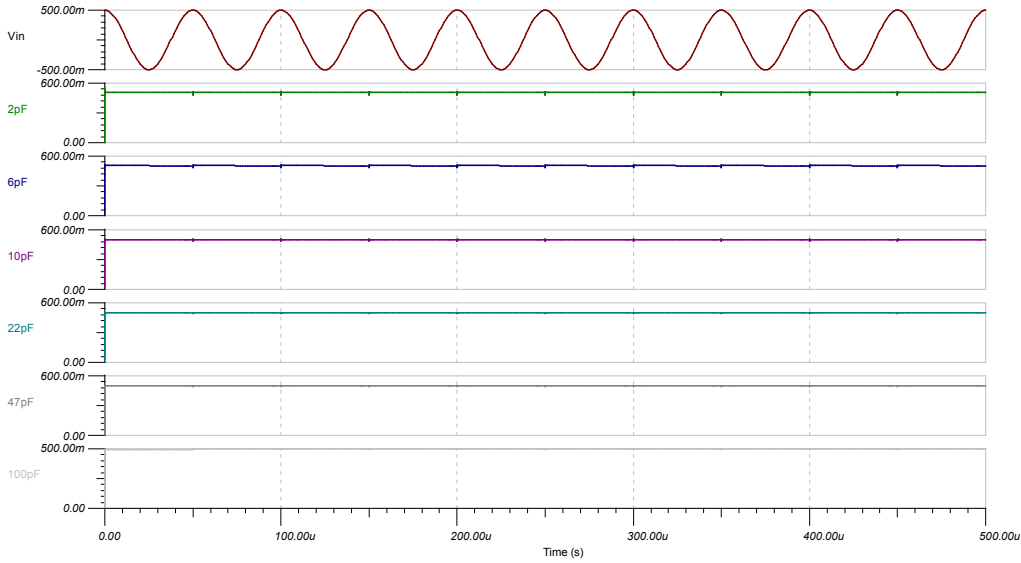
A.3. Relationship Theory - Simulation

To verify the equations in section A.1, the bias current values determined by the simulations were inserted into equation A.1. As an example, values have been taken when sampling a 20 kHz, 1 V_{PP} sine wave at its maximum (500 mV). The hold capacitor value was 28.7 pF (22 pF + 6.7 pF). The sample voltage is 500 mV and during the hold period, it droops down to -84.89 mV, resulting in a ΔV of 584.89 mV. The hold period duration is 50 μs (20 kHz) minus 20 ns (sample period).

$$\text{Droop-Rate} = \frac{\Delta V}{\Delta t} = \frac{-584.89}{49.98} \frac{mV}{\mu s} = -11.7 \frac{mV}{\mu s} \tag{A.5}$$

Using equation A.1 from section A.1, a proper term has to be found for the value of i_b (input bias current). As stated above, the droop starts at 500 mV and ends at -84.89 mV. This results in 1 V and -169.78 mV at the hold capacitor, respectively (Gain = 2). Looking at figure A.6 and using data taken without a resistor (green line), this results in bias currents of approx. -1.15 μA and -490 nA, respectively. Assuming a possible linear approximation in the region between 1 V and -170 mV (see figure A.6), this would result in a mean current (during the droop) of

$$i_{b_{MEAN}} = \frac{(-1.15\mu A + (-490nA))}{2} = -820nA \tag{A.6}$$

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Figure A.5.: TINA schematic showing the circuit used for measuring the OTA Base Bias Current
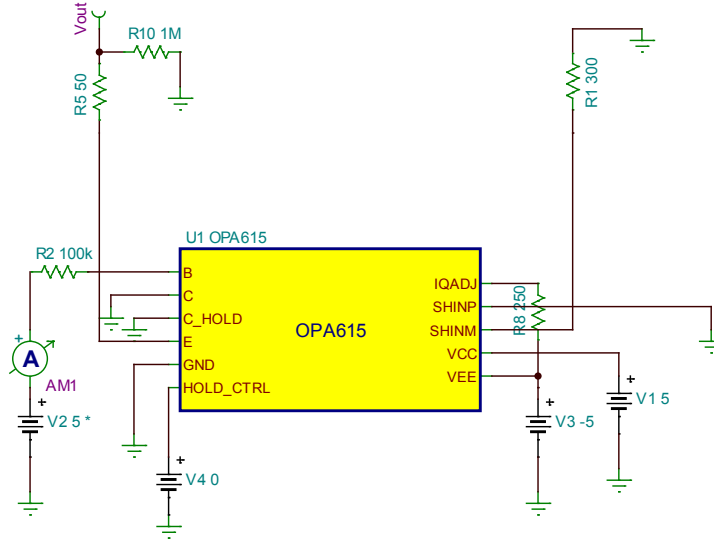
Figure A.6.: Simulation - OTA Base Bias Current vs. OTA Base Voltage
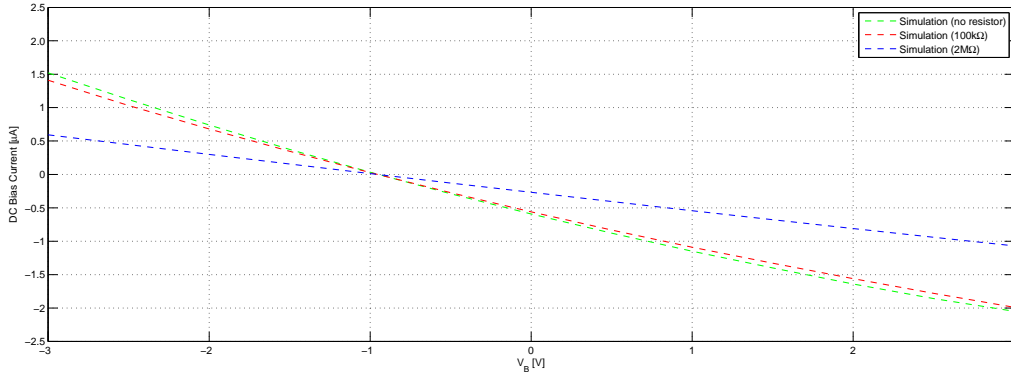
Using equation A.1, this would result in a droop rate of

$$\frac{dV_{C_H}}{dt} = \frac{i_b}{C_H} \tag{A.7}$$

$$\frac{dV_{C_H}}{dt} = \frac{-820}{28.7}\frac{nA}{pF} \tag{A.8}$$

$$\frac{dV_{C_H}}{dt} = -28.57 \times 10^3 \frac{V}{s} \tag{A.9}$$

Eventually, correcting for the 6 dB loss due to the termination (the ΔV in equation A.5 was measured at V_{OUT}), this results in a final calculated droop rate of

$$\frac{dV_{C_H}}{dt} = \frac{-28.57 \times 10^3}{2}\frac{V}{s} = -14.28\frac{mV}{\mu s} \tag{A.10}$$

Figure A.7.: Droop Rate vs. C_{Hold} Capacitor Value - Simulation
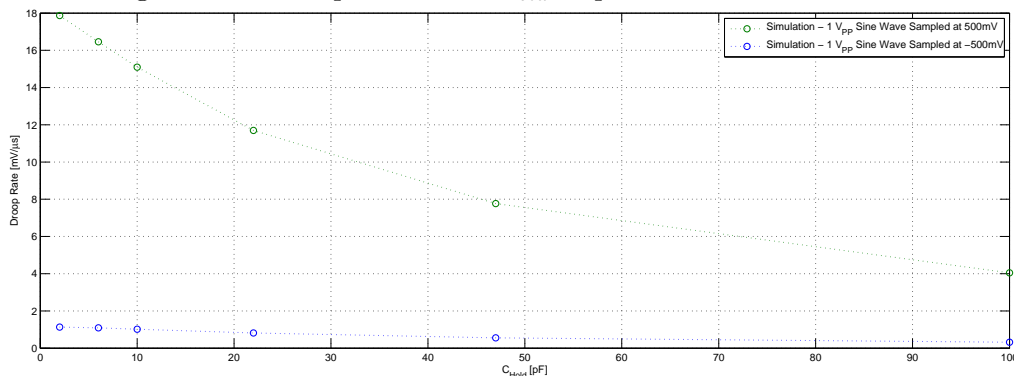
Given the calculation error due to the non-linear behaviour of the base bias current versus base voltage, the equations in section A.1 provide an acceptable first order approximation for the voltage droop model.

A.4. Measurements

The procedure applied during simulation has been repeated on the bench. Figure A.8 shows a 2 kHz, 1 V_{PP} sine wave being sampled at 20 kHz, the hold capacitor value was 22 pF. Please note that in simulaton, 28.7 pF was used as a corresponding value since 6.7 pF of parasitic capacitance are added to the actual 22 pF of the capacitor. The circuit used corresponds to the schematic shown in figure A.1.

Figure A.8.: Bench - Sampled 2 kHz, 1 V_{PP} Sine Wave, 20 kHz Sampling Rate, 20 ns Sampling Time, $C_H = 22$ pF
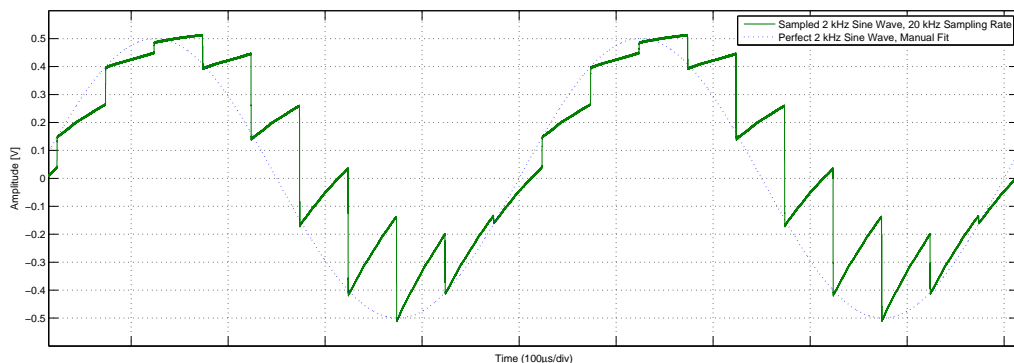
After examining figure A.8 and comparing it to its simulation counterpart (figure A.2), it becomes obvious that the behaviour of the droop rate is different. The most striking difference is the fact that the droop rate is higher at the sine wave's minimum as opposed to the simulation, where the droop rate was highest at its maximum. The though process described in section A.2 was also applied in regard to bench measurements and following that, the input bias current of the base of the OTA has been examined regarding its dependency towards the base voltage.

Figure A.9 shows the circuit used for i_b measurements on the bench. Unlike in the simulation, the current was measured as a voltage drop across a resistor (100 $k\Omega$ or 2 $M\Omega$, respectively).

Figure A.9.: Circuit used for measuring the OTA Base Bias Current on the bench
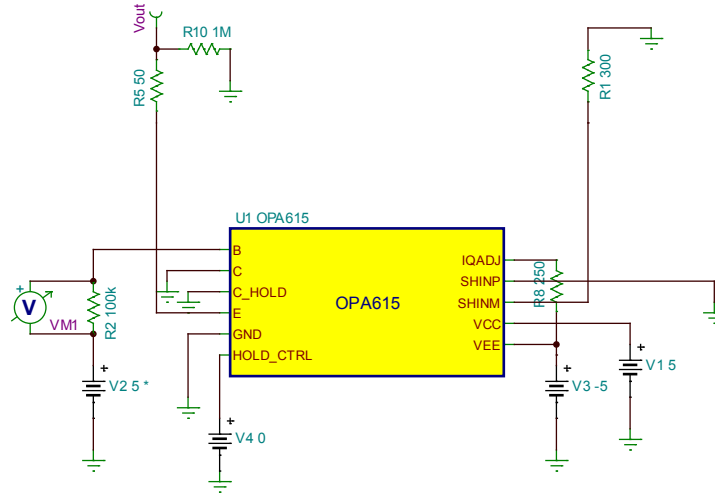
Figure A.10 shows the results of the bench i_b measurements and compares them with the simulation results shown earlier. Examining the plot, the reason for the opposite droop behaviour at the bench when compared to simulation becomes obvious. Another difference that stands out is the fact that the absolute values of the i_b measured on the bench are lower compared to the simulation.

Figure A.10.: OTA Base Bias Current vs. OTA Base Voltage - Bench vs. Simulation
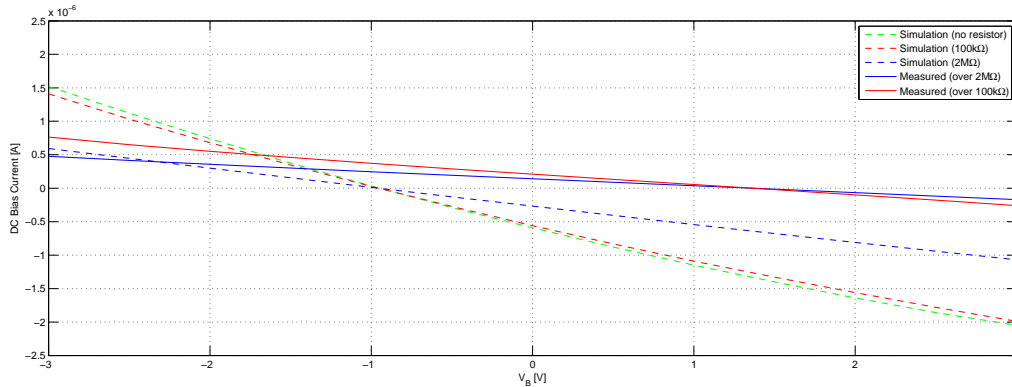
Following the i_b measurements, the droop rate values for different hold capacitors have been determined. Figure A.11 shows the results. As expected, the droop rate values are lower than their equivalents determined during simulation. Also, the droop rates of samples taken from around the minimum of the sine wave (-500 mV; -1 V at the hold capacitor - Gain = 2 V/V) are much higher than those taken at its maximum (500 mV; 1 V at the hold capacitor - Gain = 2 V/V). These droop rate difference can be explained by examining figure A.10.

Figure A.11.: Droop Rate vs. C_{Hold} Capacitor Value - Bench
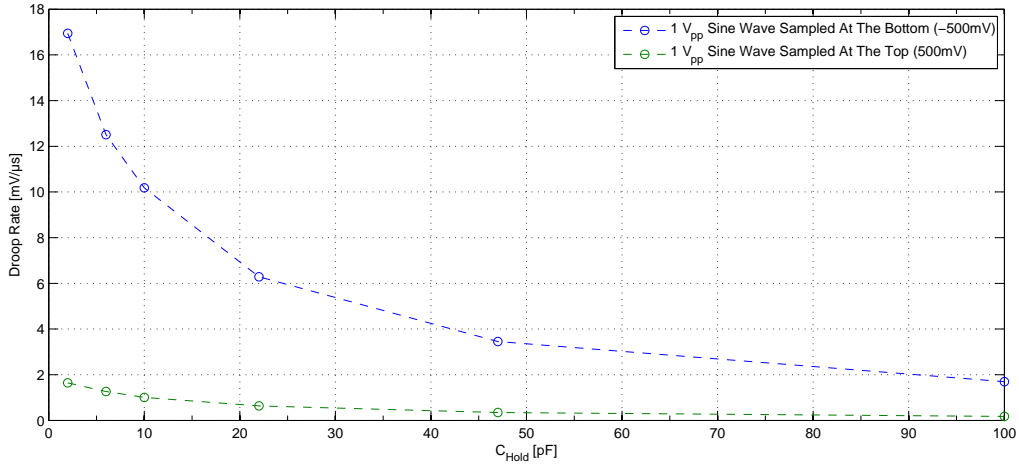
A.5. Relationship Theory - Bench

The equations from section A.1 have once again been verified for their validity in respect to bench measurements. Bias current values measured on the bench were inserted into equation A.1. As an example, values from the bench have been taken when sampling a 20 kHz, 1 V_{PP} sine wave at its **minimum** (-500 mV, -1 V at the hold capacitor). The hold capacitor value was 22 pF and the estimated additional parasitic capacitance 6.7 pF. The sample voltage is -500 mV and during the hold period, it droops down to -183.87 mV, resulting in a ΔV of 316.13 mV. The hold period duration is 50 μs (20 kHz) minus 20 ns (sample period).

$$\text{Droop-Rate} = \frac{\Delta V}{\Delta t} = \frac{316.13}{49.98}\frac{mV}{\mu s} = 6.33\frac{mV}{\mu s} \tag{A.11}$$

Using equation A.1 from section A.1, a proper term has to be found for the value of i_b (input bias current). As stated above, the droop starts at -500 mV and ends at -183.87 mV. This results in -1 V and -367.74 mV at the hold capacitor, respectively (Gain = 2 V/V). Looking at figure A.10 and using the data taken with the 100 kΩ resistor, this results in bias currents of approx. 372 nA and 268 nA, respectively. Assuming a possible linear approximation in the region between -1 V and -367 mV (see figure A.10), this would result in a mean current (during the droop) of

$$i_{b_{MEAN}} = \frac{(372nA + 268nA)}{2} = 320nA \tag{A.12}$$

Using equation A.1, this would result in a droop rate of

$$\frac{dV_{C_H}}{dt} = \frac{i_b}{C_H} \tag{A.13}$$

$$\frac{dV_{C_H}}{dt} = \frac{320}{28.7} \frac{nA}{pF} \tag{A.14}$$

$$\frac{dV_{C_H}}{dt} = 11.15 \times 10^3 \frac{V}{s} \tag{A.15}$$

Eventually, correcting for the 6 dB loss due to the termination (the ΔV in equation A.5 was measured at V_{OUT}), this results in a final calculated droop rate of

$$\frac{dV_{C_H}}{dt} = \frac{11.15 \times 10^3}{2} \frac{V}{s} = 5.58 \frac{mV}{\mu s} \tag{A.16}$$

This results in a 6.33 $\frac{mV}{\mu s}$ droop rate using data taken when sampling a sine wave and a 5.58 $\frac{mV}{\mu s}$ when using the equations shown in section A.1 and inserting the measured values of i_b. This proves that the presented theory is a viable first order approximation for calculating droop rate values. Using the correct value of i_b is the most important factor. The difference in measurement versus calculation (6.33 $\frac{mV}{\mu s}$ versus 5.58 $\frac{mV}{\mu s}$) comes from the error introduced by assuming a possible linear approximation of the bias current over the droop voltage range and by not taking into account second and third order effects (see enumeration in section A.1).

References

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