TEXAS INSTRUMENTS INC.
HIGH PERFORMANCE ANALOG

HIGH SPEED AMPLIFIERS

Design Guide

Load Sharing Concepts: Implementation for Large-Signal Applications

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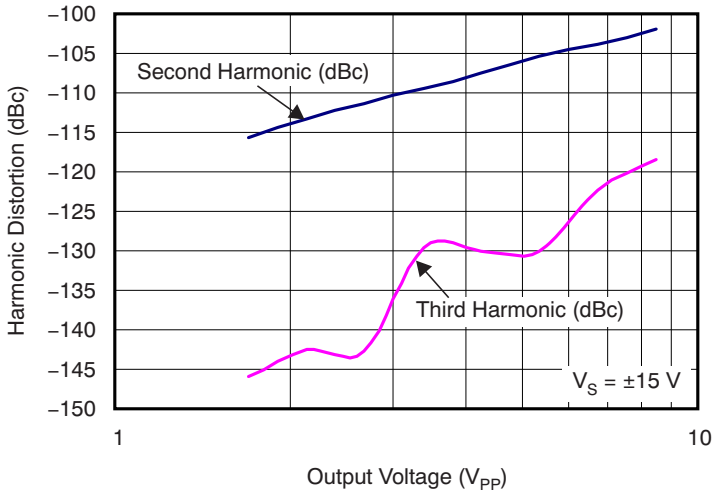
1 What Constitutes a Large Signal?

Most operational amplifier data sheets define *large signal* as any output signal that swings greater than 2 V_{PP} for ±5-V amplifiers and 5 V_{PP} for ±15-V amplifiers. However, the performance that is specified as *large signal* depends on the intended application as well as the internal architecture of the specific device. For example, analog-to-digital converter (ADC) driver amplifiers - such as the low-voltage, ±5-V, fully-differential, voltage-feedback architecture **THS4521** - specify a 2-V_{PP} large-signal bandwidth because 2 V_{PP} is a common ADC analog input range. On the other hand, a high-voltage, +28-V, current-feedback architecture, high output power line driver device such as the **THS6204** specifies large-signal performance for 4-V_{PP} to 20-V_{PP} output.

In fact, the output voltage swing of an amplifier can affect the bandwidth by more than 50% at 20-V_{PP} output compared to a small-signal (200 mV_{PP}) bandwidth as a direct result of slew rate limitation or loading. For a detailed discussion on the parameter affected by the output voltage swing, please refer to the application note *Large-Signal Specifications for High-Voltage Line Drivers* (SBOA126) available for download from the TI website. As a first-order rule, distortion performance is also degraded by 6 dB for second-harmonic and 12 dB for third-harmonic distortion every time the signal amplitude doubles. This behavior is shown in figure 1.1 for a 1 kHz signal using the **THS6182**.

Figure 1.1: 1 kHz Harmonic Distortion vs. Output Voltage (THS6182, G = -1 $\frac{V}{V}$, 1 kHz)



Slew rate, output voltage swing and output current are key operational amplifier parameters to consider for large signals applications, especially when targeting low distortion as key design parameter. As a reminder, here is a brief summary of these three specific parameters and the respective relationships to bandwidth, distortion and amplifier architecture.

1. Slew rate is directly related to the large-signal bandwidth of an operational amplifier. Slew rate limitation may also be a factor in the distortion of the amplifier. As a rule of thumb, to be able to support 80 dBc for a given frequency, the amplifier achievable slew rate must be 20x the slew rate requirement to support the signal at that frequency.
2. The amplifier output current sourcing and sinking ability into the load determine the output voltage swing range of the device. As the load current increases, distortion suffers. Additionally, high-speed large signal swings into a capacitive load require the amplifier to quickly charge and discharge the load. Depending on the load capacitance, the limited amplifier current sourcing and sinking ability may lead to a lower effective slew rate into the capacitive load.
3. The amplifier output is distorted as it approaches the output voltage swing range as a result of compression because the transistor swing is getting too close to the voltage rail.

In high voltage swing applications, where an operational amplifier is pushed to drive close to its supply rail, it is possible to drive several identical operational amplifiers in parallel and combine the outputs to achieve higher bandwidth and lower distortion. The remainder of this design guide develops this concept of load sharing and demonstrates how this technique can be used to reduce current sourcing and sinking requirements towards the amplifier.

2 Load Sharing Amplifiers

2.1 Concepts

The fundamental concept of load sharing is to drive a load using two or of the same operational amplifiers. Each amplifier is driven by the same source. Figure 2.1 shows three **THS3091** amplifiers sharing the same load.

This concept effectively reduces the current load of each amplifier by $\frac{1}{N}$, where N is the number of amplifiers.

The balance of this report focuses on selection of component values and demonstrated performance improvements.

Figure 2.2 shows two **THS3091** devices in a typical load sharing configuration.

In this example, each **THS3091** is configured in a non-inverting gain of $+5\ \frac{V}{V}$ with the two non-inverting inputs connected to a common input signal, V_{IN}. Several items are worth noting:

- In order to provide matching to the 50 Ω load, each output has a 100 Ω resistor in series. Looking from the load, these two resistors appear to be in parallel, providing the desired 50 Ω matching.

Figure 2.1: Load Sharing Conceptual Block Diagram

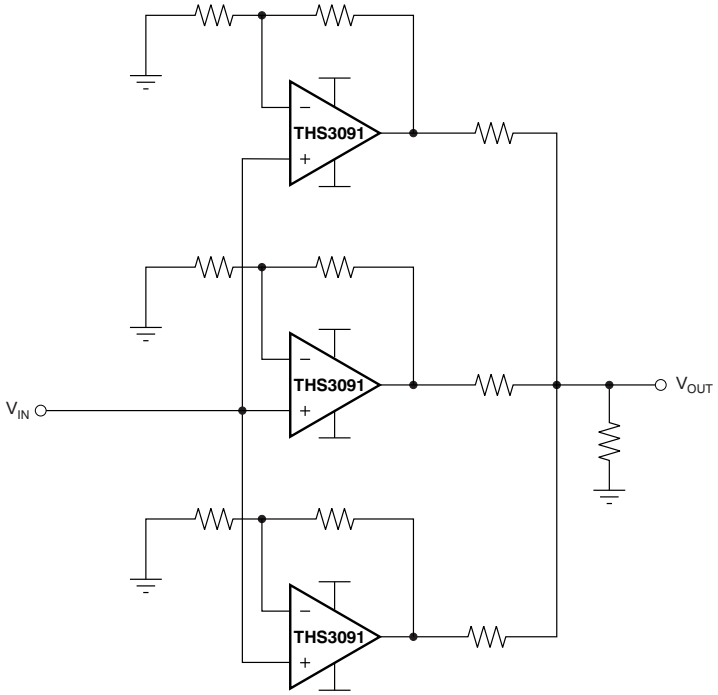
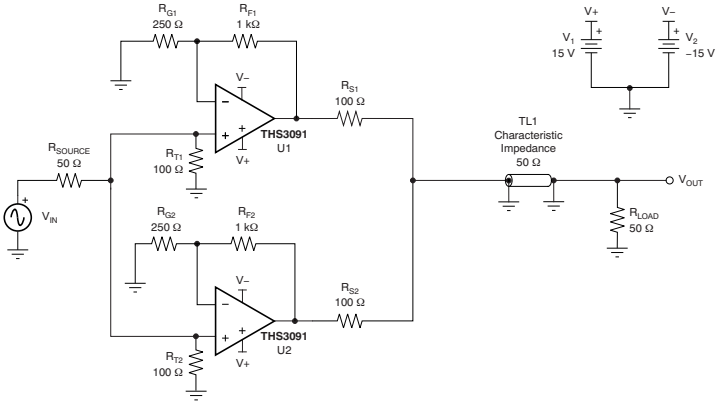


Figure 2.2: Two **THS3091** Amplifiers in Load Sharing Configuration



- The matching minimizes reflections at the load end of the transmission line. This comes at the expense of 6 dB attenuation of the signal that reaches the load.
- The matched input impedance is realized with two 100 Ω resistors that appear to be in parallel with the 50 Ω source.

For applications where back or double terminations is not required or desired, placing a non-zero resistor on each amplifier output is still highly recommended. Doing this ensures that there is a balance in the current load so that each amplifier drives the same current. Since both outputs are low impedance, this also minimizes the tendency of one amplifier output driving the other, as could be the case if the output offset voltages were different.

The next section focuses on unequal load current distribution caused by the DC offset voltage. Differences in gain from one amplifier to the next due to mismatched gain / feedback resistors also lead to imbalanced output voltages and currents. However, please note that this topic is not discussed in this document but may need to be considered depending on the final application.

2.2 Output DC Offset

The goal of the load sharing concept is to reduce the current load of each amplifier by equally distributing the total current load among all the amplifiers ($\frac{1}{N}$). Thus, it has to be ensured that neither amplifier supplies the majority of the load current and that neither amplifier sources / sinks current into / from the output of the other amplifier(s). Failing to achieve this would entirely defeat the purpose of the load sharing concept.

Also, please note that while this concept reduces the output current requirement for a given amplifier, the output voltage swing requirement remains unchanged. This allows us to select from a bigger range of amplifiers, thus possibly achieving a higher bandwidth than would otherwise have been possible with monolithic amplifiers.

Mismatched output voltages can result in imbalanced load currents. One possible source of mismatch is output-referred offset voltage. The worst-case can be calculated using equation 2.1.

$$V_{OS\_RTO} = |V_{OS}| \cdot (1 + \frac{R_F}{R_G}) + |I_{B+}| \cdot R_{NE} \cdot (1 + \frac{R_F}{R_G}) + |I_{B-}| \cdot R_F \tag{2.1}$$

Where V_{OS} is the input offset voltage, $I_{B\pm}$ is the non-inverting / inverting input bias current and R_{NE} is the equivalent resistance looking out of the non-inverting terminal.

For the **THS3091**, the maximum input offset voltage is 4 mV and the maximum non-inverting / inverting input bias current is 20 μA. Looking out of the non-inverting terminal of either amplifier yields in an equivalent series resistance of $R_{T1} \parallel R_{T2} \parallel R_{SOURCE} = 25\Omega$. Using these values in equation 2.1 results in:

$$V_{OS\_RTO} = 4mV \cdot (1 + \frac{1k\Omega}{250\Omega}) + 20\mu A \cdot 25\Omega \cdot (1 + \frac{1k\Omega}{250\Omega}) + 20\mu A \cdot 1k\Omega = 42.5mV \tag{2.2}$$

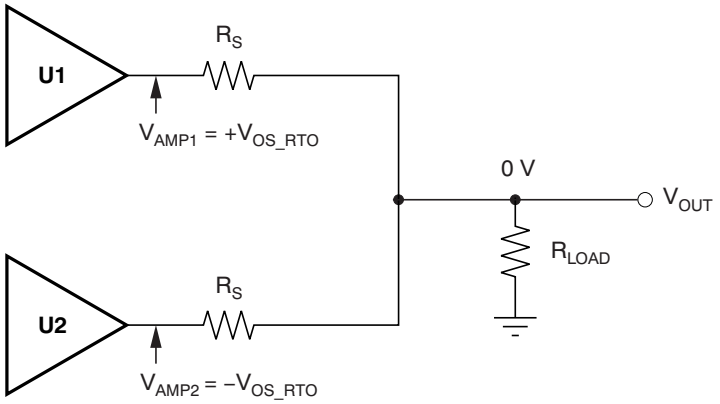
Presuming that the offset can either be positive or negative, the resulting voltage difference at DC can be as high as 85 mV for two amplifiers - assuming the gain resistors are perfectly matched.

Although amplifiers in a dual package should have better matching than single operational amplifiers, a dual package approach is not recommended because of limited power supply rejection isolation in the standard dual footprint package. This is due to the fact that the power supply pins are shared - this could lead to positive feedback on the other amplifier, thus

resulting in oscillations. The other issue which favours single operational amplifiers is thermal dissipation, especially when heavy loads are concerned.

The circuit shown in figure 2.2 can be simplified for further analysis as shown in figure 2.3. Consider a case where the input is at 0 V. Due to the non-ideal offset and bias currents of the amplifiers, the outputs are not 0 V. In the worst case situation, the outputs are at positive / negative worst case, respectively (see equations 2.1 and 2.2).

Figure 2.3: Simplified Load Sharing Circuit



With matched series output resistors (R_S), the voltage at the load (V_{OUT}) is 0 V. The current from amplifier U1 and U2 is $\pm\frac{V_{OS\_RTO}}{R_S}$, respectively.

Amplifier U1 is sourcing current into the output of U2 without generating any signal on the load. This is not a desired behavior. At best, this configuration would dissipate power and at worst, it could damage the amplifiers. R_S is therefore necessary in order to limit the current that one amplifier attempts to drive into the other in this worst-case scenario.

The difference in the two currents is given by equation 2.3.

$$I_{DIFF} = \frac{V_{OS\_RTO}}{R_S} - \left(-\frac{V_{OS\_RTO}}{R_S}\right) = 2 \cdot \frac{V_{OS\_RTO}}{R_S} \tag{2.3}$$

This is best illustrated with an example. If R_S is chosen to be 5 Ω for a configuration with two **THS3091** amplifiers, the worst-case difference in the output currents is $2 \cdot \frac{42.5mV}{5\Omega} = 17mA$. During normal operation, if the nominal output of each amplifier in figure 2.4 is 5 V, the worst case results in the voltages being $5V \pm 42.5mV$ because of the mismatched offset voltages. Figure 2.4 shows the resulting currents. As expected, amplifier U1 supplies 17 mA more than U2. Thus, U1 will have to dissipate more heat and will be more susceptible to failure. Also, due to the higher output current, the harmonic distortion shown by U1 will increase.

The difference in amplifier currents can be plotted against the series resistor R_S. Figure 2.5 shows the difference in amplifier currents for two load sharing **THS3091** amplifiers versus the series resistor R_S. With R_S increased to 10 Ω, the difference in amplifier currents is reduced to 4.25 mA.

Figure 2.4: Example of Mismatched Amplifier Output Voltages

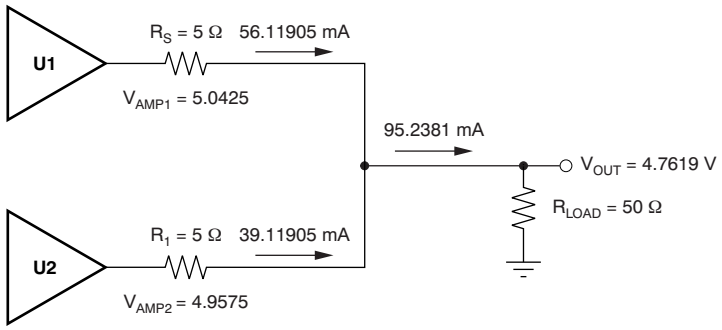
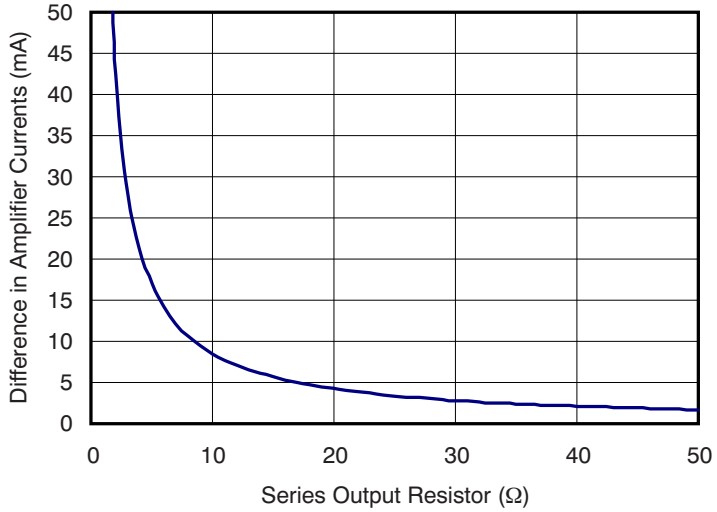


Figure 2.5: Difference in Amplifier Current vs. Series Output Resistor



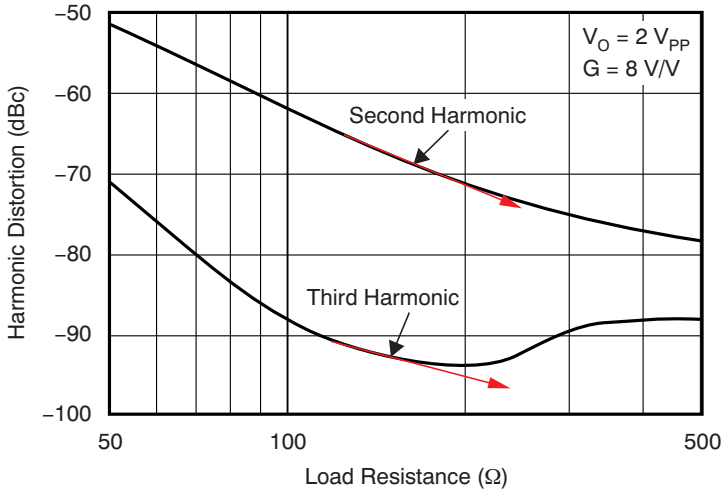
3 Load Sharing Amplifiers and Distortion Performance

In addition to providing higher output current drive to the load, the load sharing configuration can also provide improved distortion performance. In many cases, an operational amplifier shows better distortion performance as the load current decreases (that is, for higher resistive loads) until the feedback resistor starts to dominate the current load. In a load sharing configuration with N amplifiers in parallel, the equivalent current load for each amplifier is $\frac{1}{N}$ times the total load current. Looking at a load sharing configuration of 2 amplifiers with matching resistance (refer to figure 2.2) driving a resistive load R_L, each series resistance is $2 \cdot R_L$ and each amplifier drives $2 \cdot R_L$.

A convenient indicator of whether an operational amplifier will benefit from a load sharing configuration is the characteristic performance graph of harmonic distortion versus load resistance. Such graphs can be found in most of TI's high-speed amplifier data sheets.

For example, figure 3.1 (from the **OPA695** data sheet) provides a figure of 10 MHz harmonic distortion versus load resistance. This graph shows 9 dB improvement in second-order harmonic performance with a load of 200 Ω compared to a 100 Ω load. Third-order harmonic performance shows an improvement of about 6 dB. Consequently, the **OPA695** may be a good candidate for a load sharing configuration of two **OPA695** amplifiers driving a 100 Ω load. The apparent load to each **OPA695** will be double the shared resistive load, or 200 Ω.

Figure 3.1: Harmonic Distortion vs. Load Resistance Graph from OPA695 Data Sheet



However, please note that harmonic distortion does not always improve monotonically as the resistive load increases. For example, figure 3.1 shows that third-harmonic distortion reaches a minimum at a 200 Ω load. With a 500 Ω load, third-harmonic distortion is virtually the same as with a 100 Ω load while second-harmonic distortion continues to improve. Another parameter affecting the distortion performance is the output signal swing. Increasing the latter will typically degrade the distortion performance, though not always monotonically.

Product data sheets that do not include harmonic distortion versus load resistance graphs usually include distortion versus frequency graphs for different load resistances. The typical distortion performance at a specific frequency for two different loads may also be included in the Electrical Specifications table. For example, the **THS3091** data sheet includes typical distortion performance graphs for 100 Ω and 1 $k\Omega$ loads. The distortion performance at 10 MHz for a 2 $\frac{V}{V}$ gain configuration and 2 V_{PP} output are also included in the Electrical Characteristics table for this device and are given in table 3.1. It shows that second-harmonic distortion performance is better with a 1 $k\Omega$ load than with a 100 Ω load while third-harmonic distortion is superior with a 100 Ω load compared to a 1 $k\Omega$ load.

Assuming the **THS3091** has been chosen to drive a 20 V_{PP} signal into a 100 Ω load (a double-terminated, 50 Ω cable) and load sharing is being considered, no definitive conclusion can be reached using the performance data provided by the data sheet and additional characterization would be required.

Table 3.1: Harmonic Distortion for 100 Ω and 1 $k\Omega$ Loads (from **THS3091** Data Sheet)

PARAMETER	CONDITIONS		THS3091 TYP +25°C	THS3091 MIN/MAX OVER TEMPERATURE +25°C	THS3091 MIN/MAX OVER TEMPERATURE 0°C to 70°C	THS3091 MIN/MAX OVER TEMPERATURE –40°C to +85°C	UNIT
Second Harmonic Distortion	G = 2, R_F = 1.21 kΩ, V_O = 2 V_{PP}, f = 10 MHz	R_L = 100 Ω	66				dBc
		R_L = 1 kΩ	77				dBc
Third Harmonic Distortion	G = 2, R_F = 1.21 kΩ, V_O = 2 V_{PP}, f = 10 MHz	R_L = 100 Ω	74				dBc
		R_L = 1 kΩ	69				dBc

4 THS3091 Test Circuit and Load Sharing Performance

4.1 Test Circuit

As in the case in every design, lab evaluation is the best gauge of performance. Two test circuits are shown in figure 4.1, one with a single and the other with two **THS3091** in a load sharing configuration. Both circuits are driving a double-terminated, 50 Ω cable. In the load sharing configuration, the two 100 Ω series output resistors act in parallel to provide 50 Ω back-matching to the 50 Ω cable.

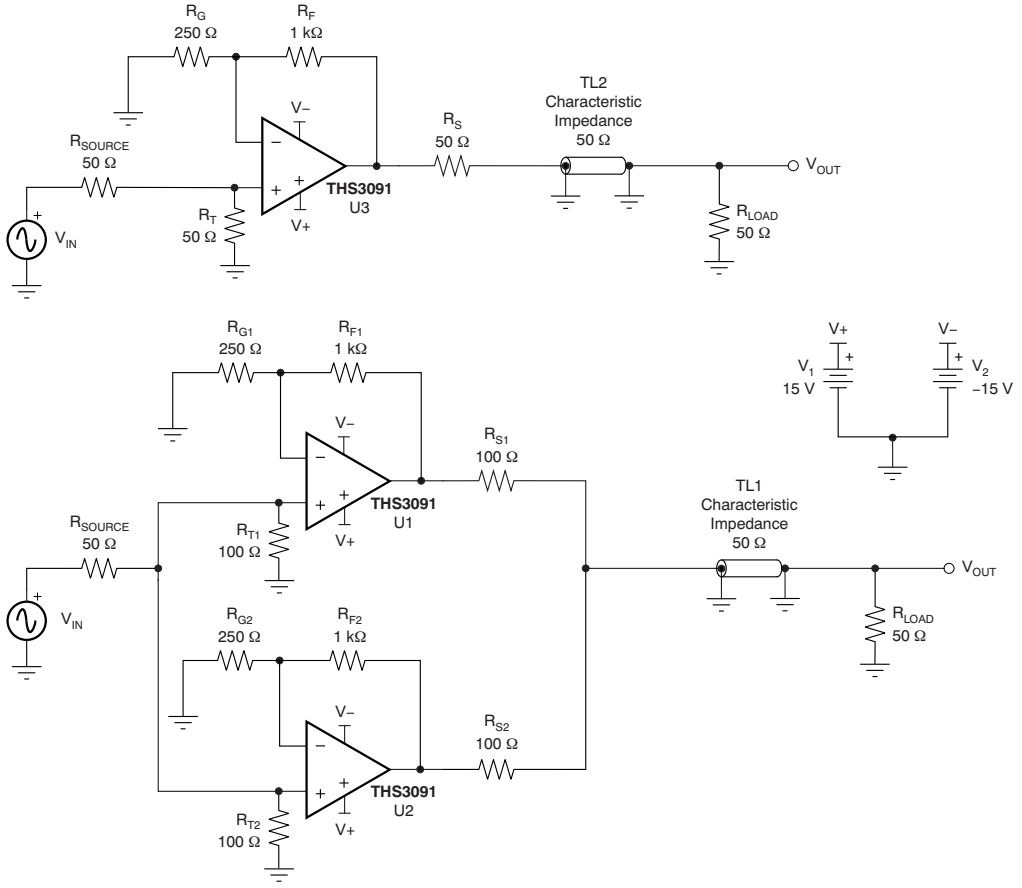
4.2 PCB Design / Thermal Discussion

While designing the PCB, multiple things have to be kept in mind:

- Minimize Parasitics
- Minimize Trace Inductance (Short Traces)
- Maximize heat dissipation

When starting the design, it is important to review the thermal aspects. In the planned bench tests, the **THS3091** is supposed to drive a 20 V_{PP} signal into a double-terminated, 50 Ω cable. The frequency of the signal is supposed to get as high as 70 MHz. In previous tests, it has been determined that a load sharing configuration of two **THS3091** is pulling approx. 100mA from both the +15 V and the -15 V rail of the power supply when driving a 70 MHz 20 V_{PP} signal into a double-terminated, 50 Ω cable. A single **THS3091** is still pulling approx. 70mA from both the +15 V and the -15 V rail. That results in a total power consumption of approx. 3 W for the load sharing and 2.1 W for the single configuration. Assuming a 20 V_{PP} sinusoid signal being driven in a 50 Ω load, the resulting signal power would be 1 W. That

Figure 4.1: Reference **THS3091** Single and Load Sharing Test Configurations



would result in a total power dissipation of $3-1=2W$ for the load sharing and $2.1-1=1.1W$ for the single configuration. To avoid thermal artifacts and shut-down, it has to be made sure that the heat is properly dissipated. For this reason, the THS3091**DDA** version should be used and the PCB should be designed accordingly. The DDA version comes in a thermally enhanced 8-SOIC PowerPAD^{TM} package. Here, the die is mounted on a downset leadframe. This acts as a heatsink and must be connected to a thermally dissipating plane for proper power dissipation. For maximum performance, the junction temperature must not exceed 125 $°C$. Thermal shut-down occurs for junction temperatures over 160 $°C$. In the **THS3091**, the PowerPAD^{TM} is electrically isolated from the silicon and all leads. Hence, connecting the PowerPAD^{TM} to any potential voltage is acceptable. However, regarding devices featuring a PowerPAD^{TM} in general, it is recommended to connect the PowerPAD^{TM} to the lowest supply ($-V_S$ in this case) since this technique is applicable to all devices / process technologies.

In order to minimize parasitic capacitances, the planes below the IC are usually cut out in a high-speed design. However, cutting out the planes when using a PowerPAD^{TM} would reduce the heat sinking efficiency. Therefore, no cut-outs have been performed when designing the board. Figures 4.2 through 4.5 show the 4 layers of the PCB used during bench testing.

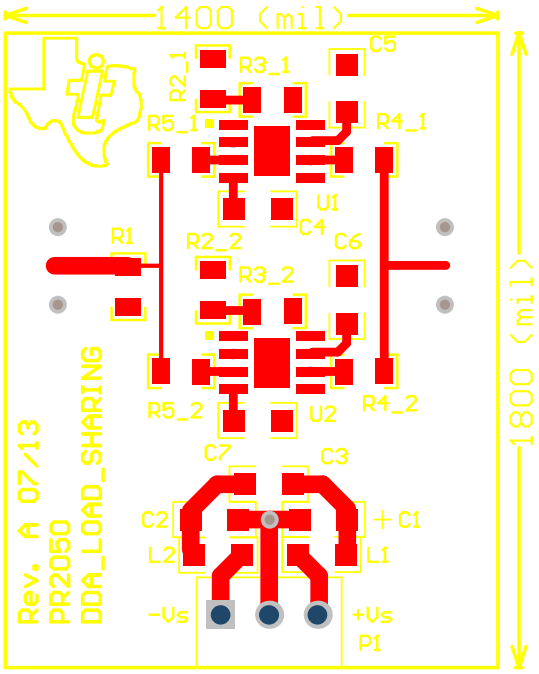


Figure 4.2: Top Layer and Overlay (Signal)

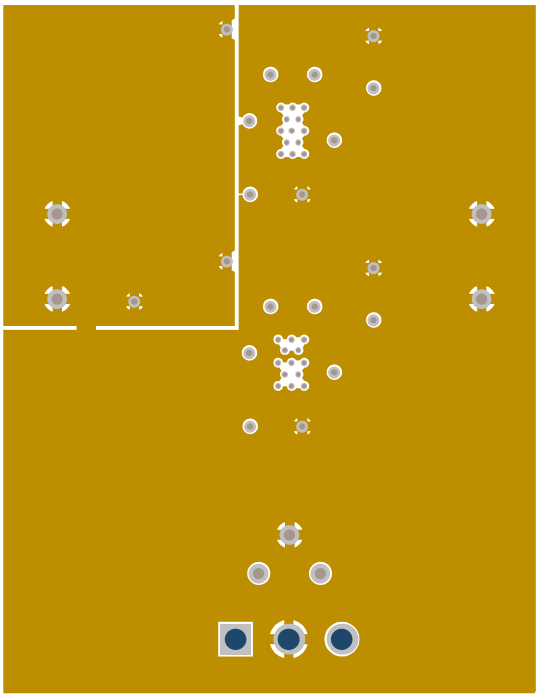


Figure 4.3: Mid Layer 1 (GND)

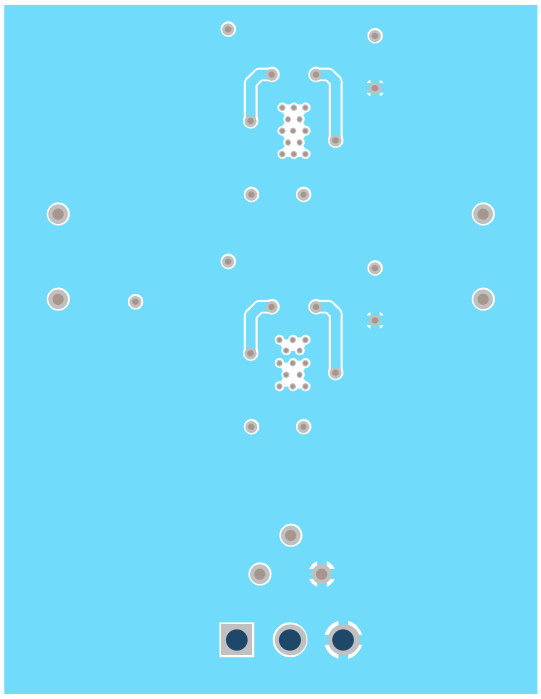


Figure 4.4: Mid Layer 2 ($+V_S$)

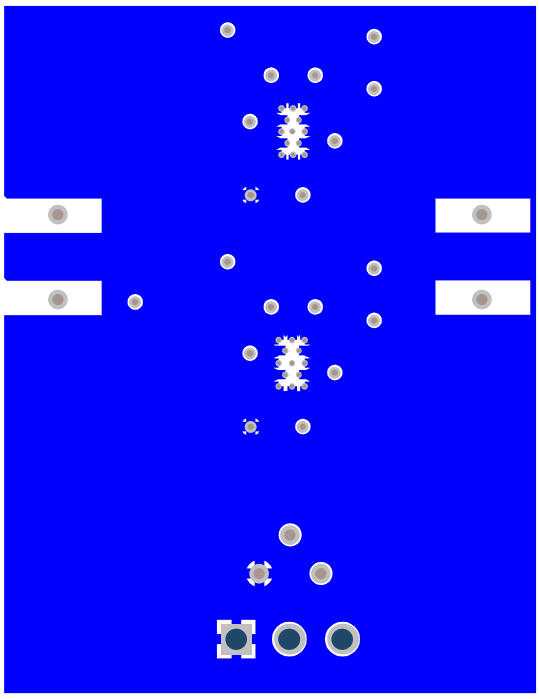


Figure 4.5: Bottom Layer ($-V_S$)

4.3 Measured Performance

Figures 4.6 and 4.7 show a 30 MHz, 20 V_{PP} sine wave output amplitudes for the single and load sharing **THS3091** configuration, respectively, measured using an oscilloscope. An ideal sine wave is included as a visual reference (dashed red line).

Figure 4.6: 30 MHz Sine Wave Output, **Single THS3091** (G = 5 $\frac{V}{V}$, Signal Level Referred to Amplifier Output)

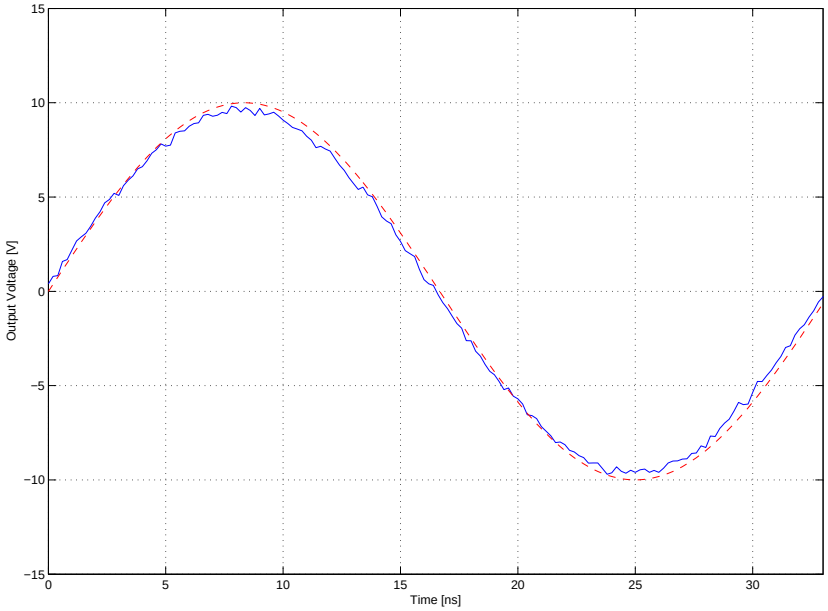
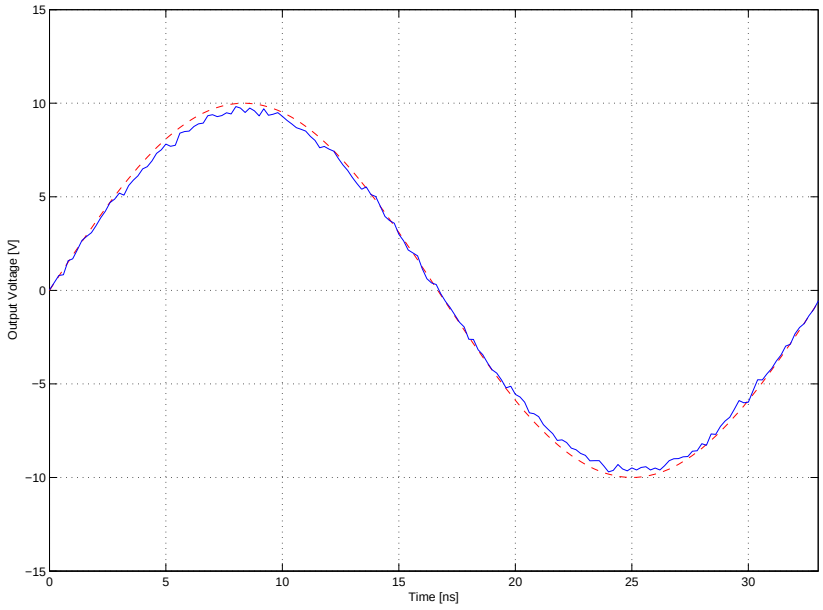


Figure 4.7: 30 MHz Sine Wave Output, **Dual THS3091** Load Sharing (G = 5 $\frac{V}{V}$, Signal Level Referred to Amplifier Output)



Figures 4.8 and 4.9 show a 60 MHz, 20 V_{PP} sine wave output amplitudes for the single and load sharing **THS3091** configuration, respectively, measured using an oscilloscope. An ideal sine wave is included as a visual reference (dashed red line).

Figure 4.8: 60 MHz Sine Wave Output, **Single THS3091** (G = 5 $\frac{V}{V}$, Signal Level Referred to Amplifier Output)

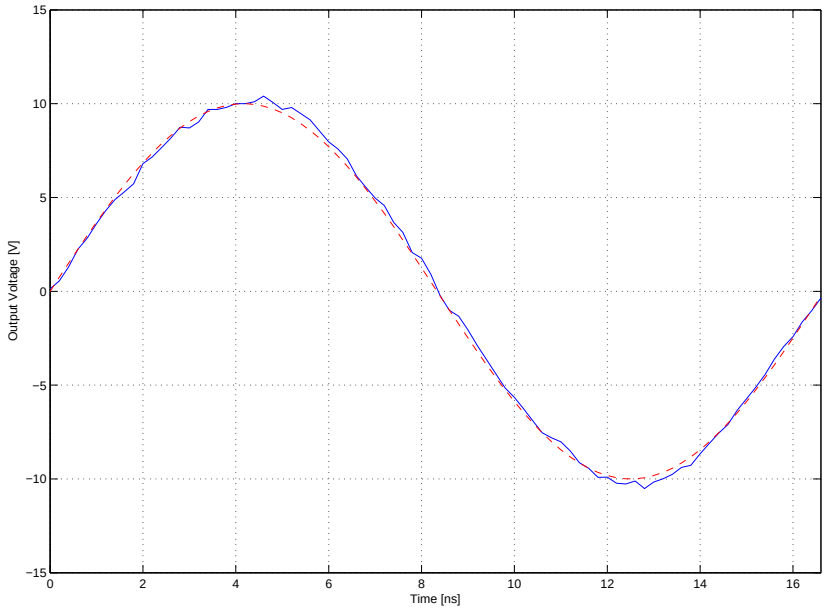
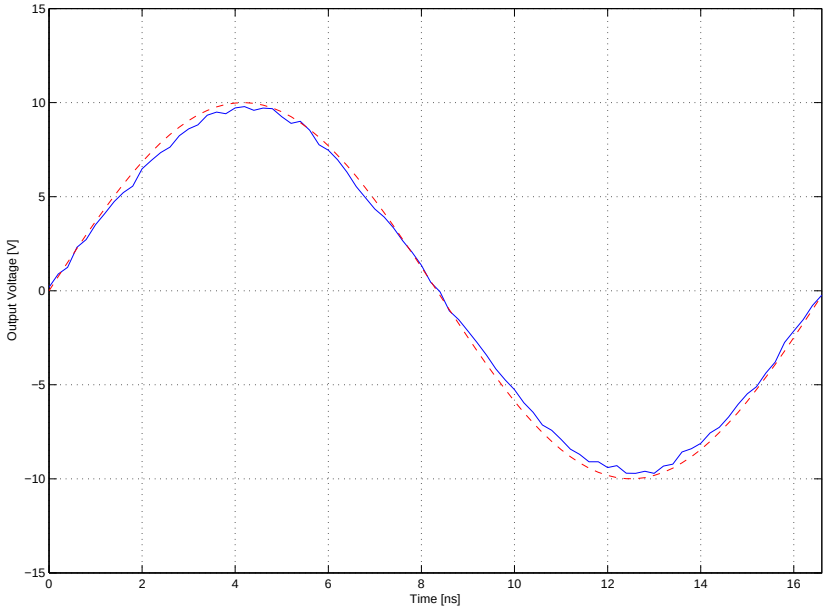


Figure 4.9: 60 MHz Sine Wave Output, **Dual THS3091** Load Sharing (G = 5 $\frac{V}{V}$, Signal Level Referred to Amplifier Output)



Evaluating the sine wave captures, the optical difference might not seem too large. However, measuring the harmonic distortion shows significant improvement when using the load shar-

ing configuration. Figures 4.10 and 4.11 show harmonic distortion performance for a single **THS3091** and a dual load sharing configuration, respectively. In the frequency range from 20 to 70 MHz, the load sharing configuration shows an improvement of approx. 8 dB in average when compared to a single **THS3091**.

Figure 4.10: Harmonic Distortion vs. Frequency, **Single THS3091**

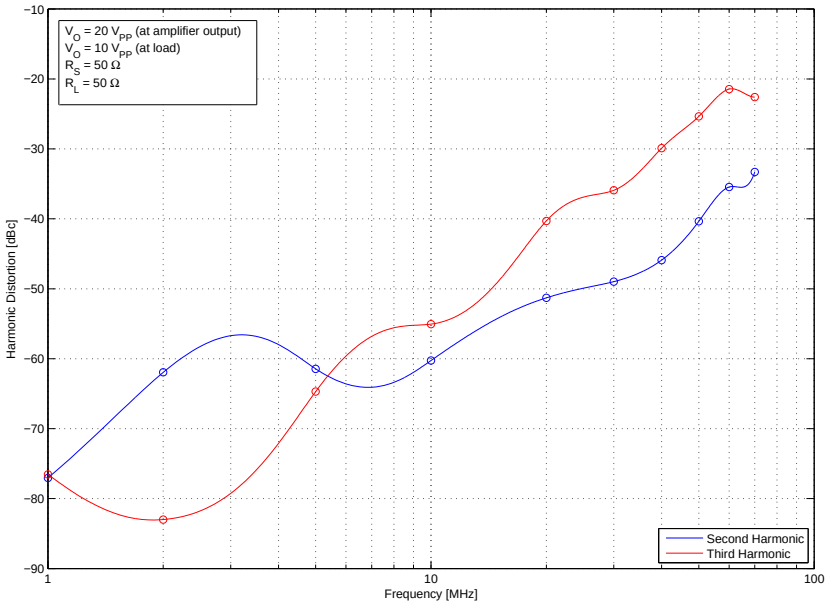
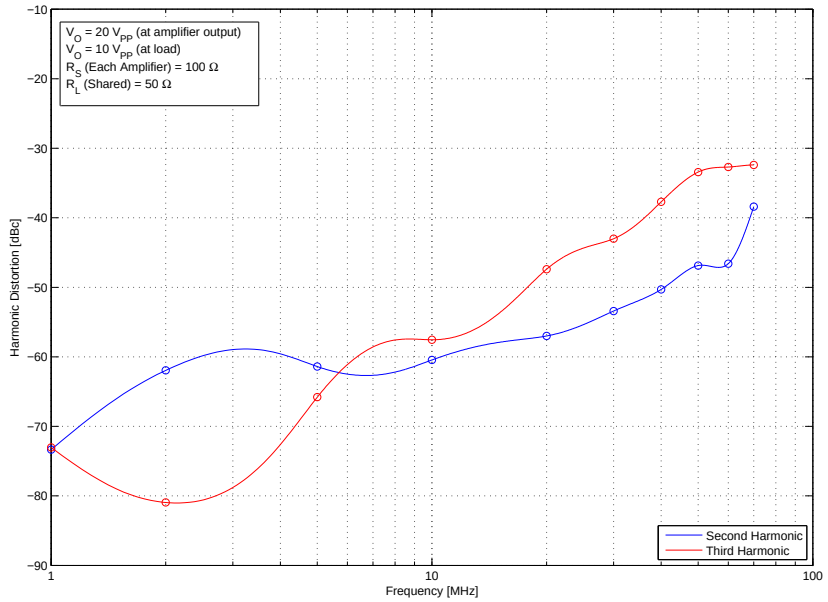


Figure 4.11: Harmonic Distortion vs. Frequency, **Dual THS3091** Load Sharing



Figures 4.12 and 4.13 show direct comparisons of HD2 and HD3 performances, respectively. Figure 4.13 shows a significant improvement in HD3 performance at frequencies greater than 10 MHz when using a load sharing configuration (approx. 8 dB in average). The load sharing

configuration shows improvement in HD2 performance as well, however of a lesser magnitude than HD3.

Figure 4.12: **Second**-Harmonic Distortion vs. Frequency, Single and Dual (Load Sharing) **THS3091**

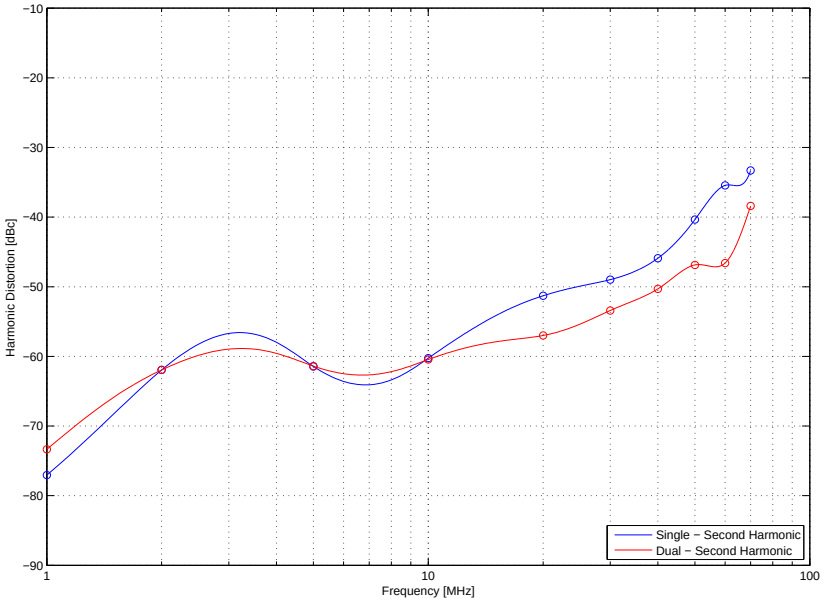
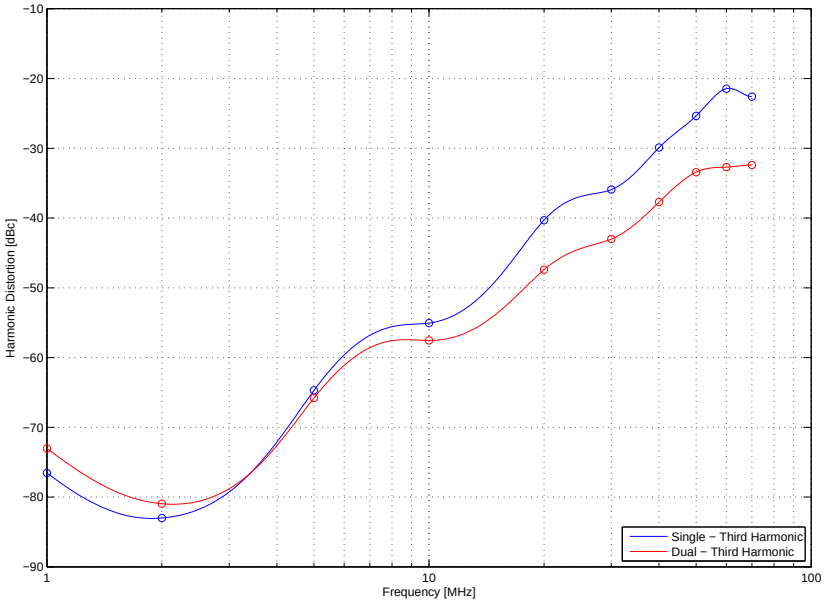


Figure 4.13: **Third**-Harmonic Distortion vs. Frequency, Single and Dual (Load Sharing) **THS3091**



5 Conclusion

The operational amplifier limitations imposed by slew rate and output current must be considered when an application requires large output signal swings. Output current is an especially important factor. This application note reviewed and explained a load sharing method to increase the output current ability of an amplifier and potentially improve distortion performance.

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