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TI Designs – Precision: Verified Design

Capacitive Load Drive Solution using an Isolation Resistor

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Design Resources

Design Archive	All Design files
TINA-TI™	SPICE Simulator
OPA192	Product Folder
OPA140	Product Folder
OPA170	Product Folder
OPA171	Product Folder
OPA172	Product Folder
OPA180	Product Folder
OPA209	Product Folder
OPA320	Product Folder
OPA340	Product Folder
OPA350	Product Folder
OPA365	Product Folder

Circuit Description

This design can be used to drive capacitive loads such as cable shields, reference buffers, MOSFET gates, and diodes. The circuit uses an isolation resistor (R_{iso}) to stabilize the output of an op amp. R_{iso} modifies the open loop gain of the system to ensure the circuit has sufficient phase margin. The OPA192 is highlighted because it can drive large capacitive loads using a small isolation resistor.

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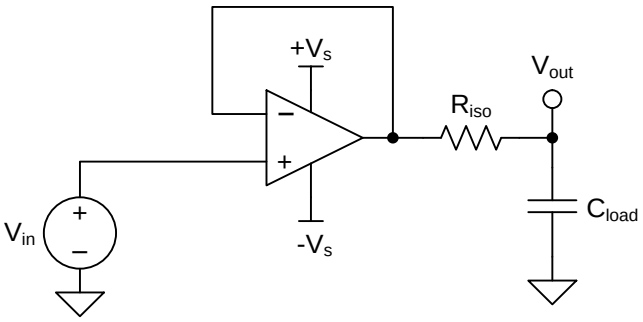

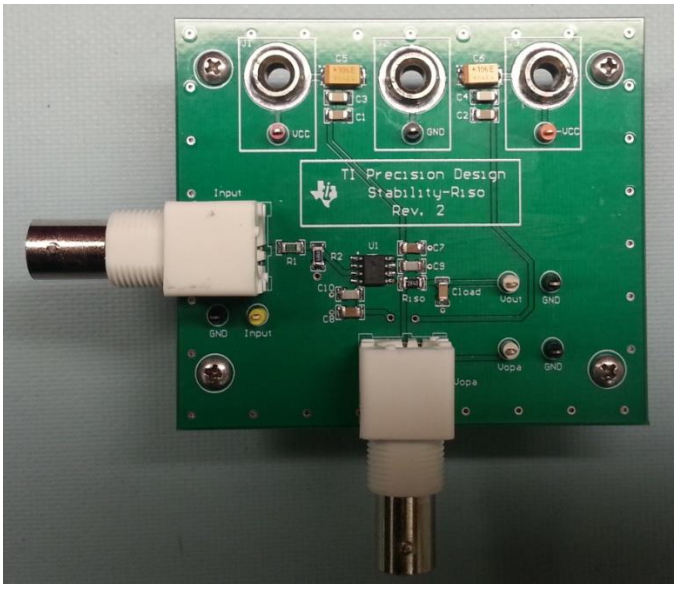

1 Design Summary

The design requirements are as follows:

- Supply Voltage: 30 V (+/-15 V)
- Capacitive Loads: 100 pF, 1000 pF, 0.01 µF, 0.1 µF, 1 µF

The design goals and performance are summarized in Table 1. Figure 1 depicts the transient response of the OPA192 driving a 0.1 µF load capacitance (C_{load}) using an isolation resistor (R_{iso}) of 6.2 Ω to obtain a percent overshoot (PO) of 23.1% and corresponding phase margin (PM) of 45.2°.

Table 1: Comparison of Design Goals and Measured Performance

	Capacitive Load	100 pF		1000 pF		0.01 µF		0.1 µF		1 µF	
OPA192	Phase Margin Goal	45°	60°	45°	60°	45°	60°	45°	60°	45°	60°
	Riso (Ω)	47.0	360.0	24.0	100.0	20.0	51.0	6.2	15.8	2.0	4.7
	Measured Overshoot (%)	23.2	10.4	22.5	9.0	22.1	8.7	23.1	8.6	21.0	8.6
	Calculated PM	45.1°	58.1°	45.8°	59.7°	46.1°	60.1°	45.2°	60.2°	47.2°	60.2°

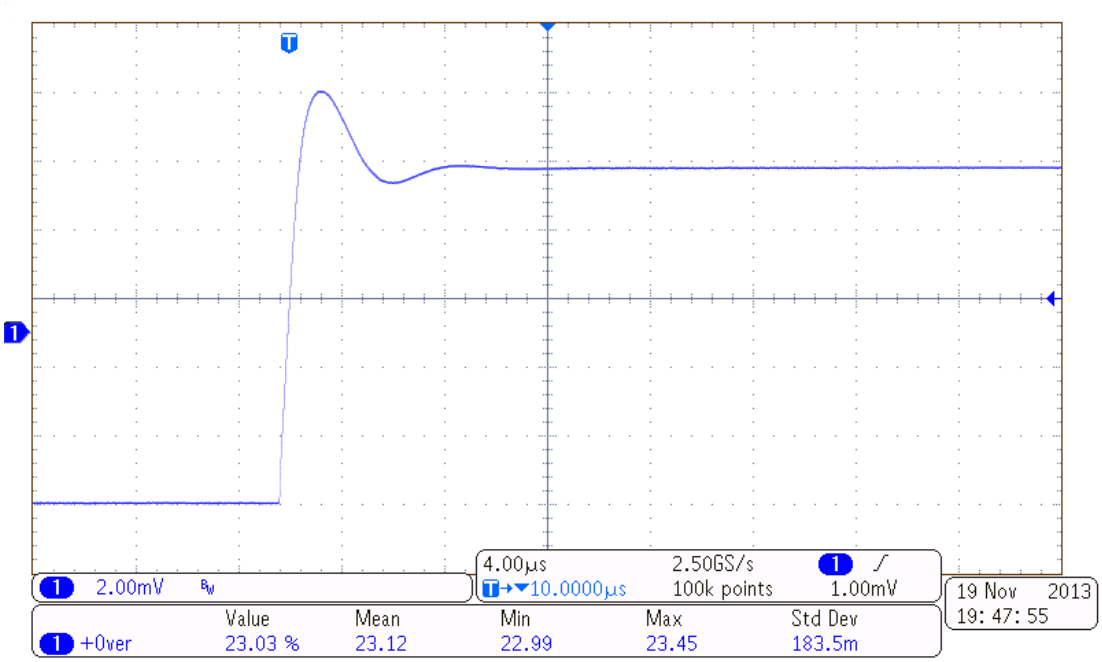

Figure 1: OPA192 Transient Response, C_{load}=0.1 µF, R_{iso}=6.2 Ω, PM=45.2°

2 Theory of Operation

Figure 2 depicts a unity-gain buffer driving a capacitive load. Equation (1) shows the transfer function for the circuit in Figure 2. Not depicted in Figure 2 is the open-loop output impedance of the op amp, R_o.

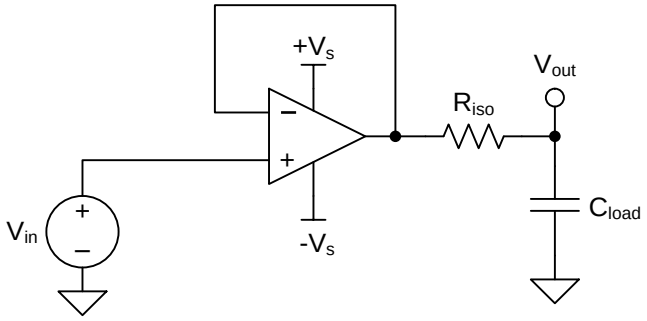

Figure 2: Unity-Gain Buffer with R_{iso} Stability Compensation

$$T(s) = \frac{1 + C_{load} \times R_{iso} \times s}{1 + (R_o + R_{iso}) \times C_{load} \times s} \quad (1)$$

The transfer function in Equation (1) has a pole and a zero. The frequency of the pole (f_p) is determined by (R_o+R_{iso}) and C_{load}. R_{iso} and C_{load} determine the frequency of the zero (f_z). A stable system is obtained by selecting R_{iso} such that the rate of closure (ROC) between the open loop gain (A_{ol}) and 1/β is 20 dB/decade. [1] Figure 3 depicts the concept. For further information, please consult References [1]-[3]. Note that the 1/β curve for a unity-gain buffer is 0 dB.

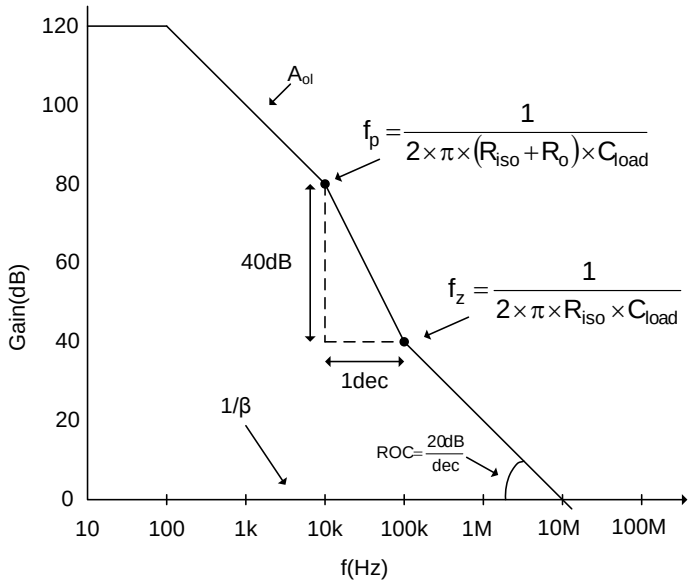

Figure 3: Unity-gain Amplifier with R_{iso} Compensation

ROC stability analysis is typically simulated. The validity of the analysis depends on multiple factors, especially the accurate modeling of the open-loop output impedance of the amplifier (R_o).

In addition to simulating the ROC, a robust stability analysis includes a measurement of the circuit's percent overshoot and ac gain peaking using a function generator, oscilloscope, and gain/phase analyzer. Phase margin is then calculated from these measurements. Table 2 shows the percent overshoot and ac gain peaking that correspond to phase margins of 45° and 60°. The theory behind these values is in Appendix B and the corresponding software simulation is located in the design file.

Table 2: Phase Margin vs. Overshoot and AC Gain Peaking

Phase Margin	Overshoot (%)	AC Gain Peaking (dB)
45°	23.3	2.35
60°	8.8	0.28

3 Component Selection

This Precision Design intends to provide R_{iso} values for a variety of op amps and capacitive loads. Table 3 lists the op amps and some of their characteristics. The OPA192 is featured because of its ability to drive large capacitive loads using a small isolation resistor.

Table 3: Selected Op Amps

Op Amp	V_{supply} Range (V)	I_Q @ 25ºC (max, mA)	V_{OS} @ 25ºC (max, µV)	V_{OS} Drift (max, µV/C)	Vn @ 25ºC (typ, nV/√Hz)	BW (typ, MHz)	Notes
OPA192	4.5 – 36	1.2	25	0.5	5.5	10	RRI/O, Low Noise
OPA140	4.5 – 36	2	120	1	5.1	11	RRO, JFET input, Low Noise
OPA170	2.7 – 36	0.145	1800	2	19	1.2	RRO, Value Line
OPA171	2.7 – 36	0.595	1800	2	14	3.0	RRO, Value Line
OPA172	4.5 – 36	1.8	1000	1.5	7	10	RRO, Low Power
OPA180	4.0 – 36	0.525	75	0.35	10	2	RRO, Low Noise, Zero-Drift
OPA209	4.5 – 36	2.5	150	3	2.2	18	RRO, Low Noise
OPA320	1.8 – 5.5	1.6	150	5	8.5	20	RRI/O, Low Noise
OPA340	2.7 – 5.5	0.95	500	2.5 (typ)	25	5.5	RRI/O. SR=6V/µs
OPA350	2.7 – 5.5	7.5	500	4 (typ)	15	38	RRI/O, SR=22V/µs
OPA365	2.2 – 5.5	5	200	1 (typ)	13	50	RRI/O, SR=25V/µs

4 Simulation

ROC analysis (or ac analysis) is used to determine an approximate value of R_{iso}. Figure 4 depicts the TINA-TI™ schematic topology used in ROC analysis. This topology is thoroughly discussed in [2].

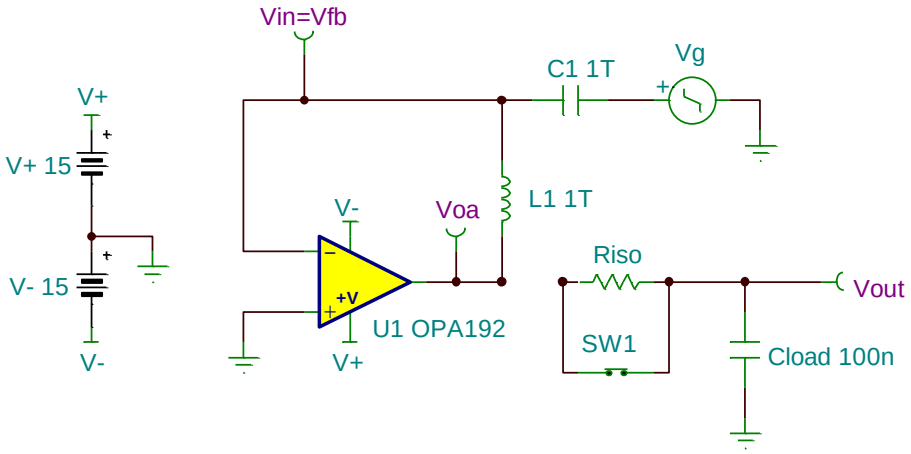

Figure 4: TINA-TI™ Circuit used for ROC Stability Analysis

Figure 5 shows the corresponding ROC analysis of V_{oa} in Figure 4 with SW1 closed. Note that the ROC is ~40 dB/decade and the phase margin is only 8.4º. While a phase margin of 8.4º is technically stable, it is not a robust design. Variation in process and environmental conditions may reduce the phase margin such that the system becomes unstable. Therefore, a phase margin of at least 45º is recommended.

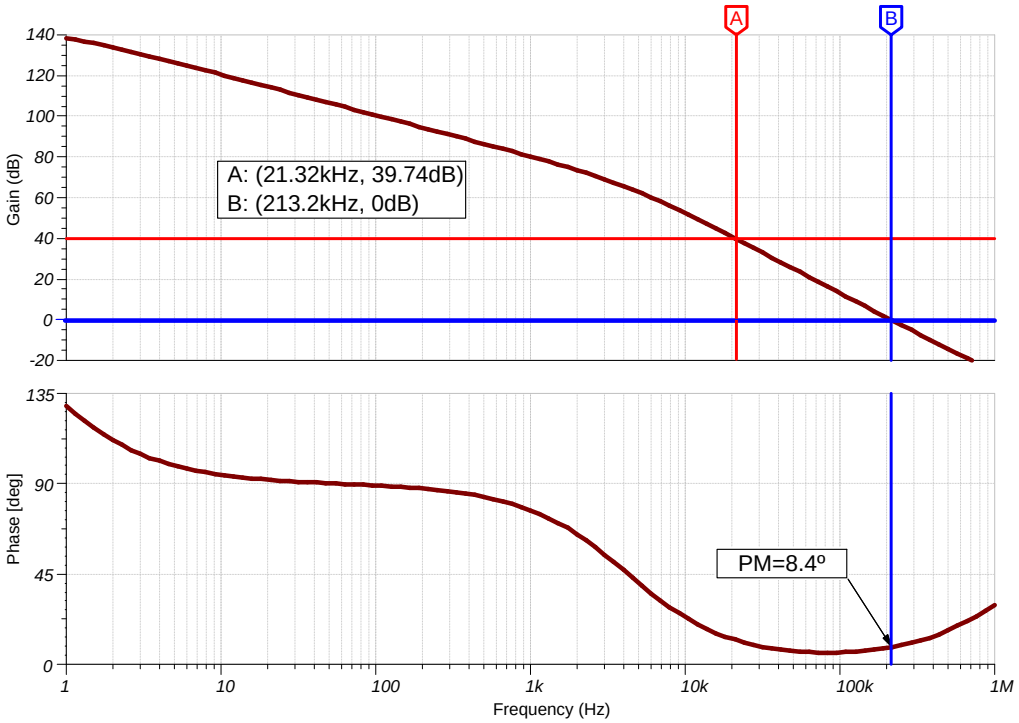

Figure 5: OPA192, C_{load}=0.1 µF, R_{iso}=0.0 Ω, PM=8.4º

Placing a zero at the frequency where A_{ol}=20 dB, as shown in Figure 6, adds ~90º of phase margin. [3] Further analysis will refine the location of the zero to reduce the value of R_{iso} while maintaining a stable system.

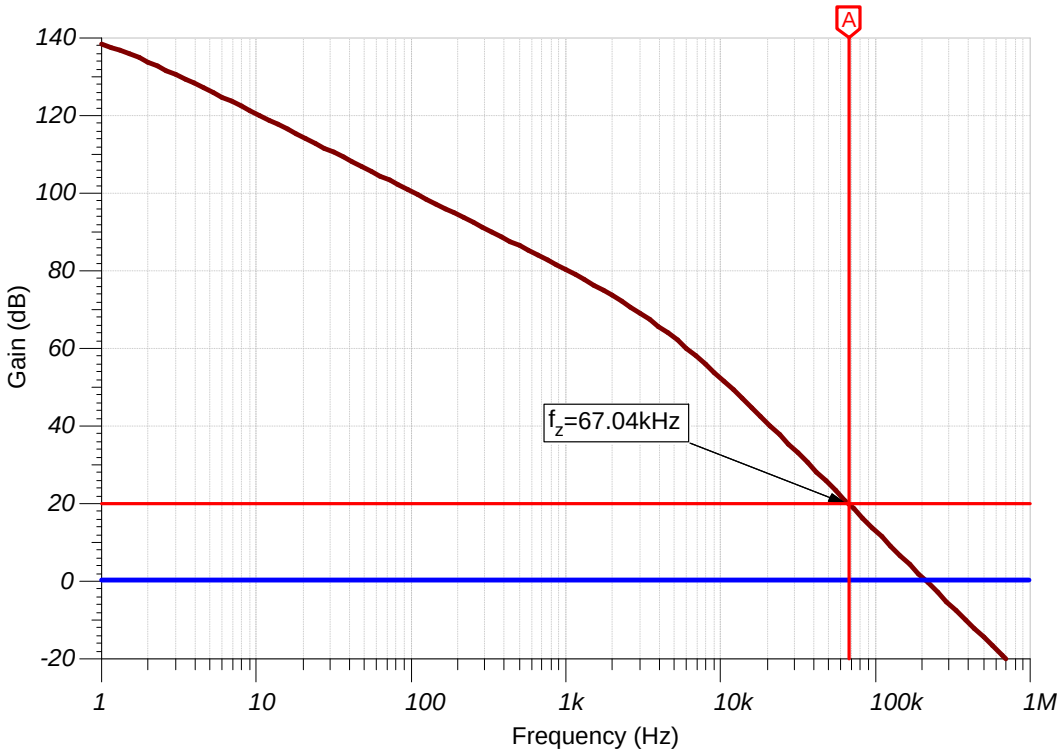

Figure 6: Frequency of Zero for Increased Phase Margin

R_{iso} is calculated as shown in Equation (2).

$$R_{iso} = \frac{1}{2 \times \pi \times f_z \times C_{load}} = \frac{1}{2 \times \pi \times 67.04\text{kHz} \times 0.1\mu\text{F}} = 23.74\Omega \quad (2)$$

Setting R_{iso} in Figure 4 to 23.7 Ω (nearest 1% standard value) and opening SW1 yields the ROC analysis shown in Figure 7. Notice the ROC and phase margin indicate a stable system.

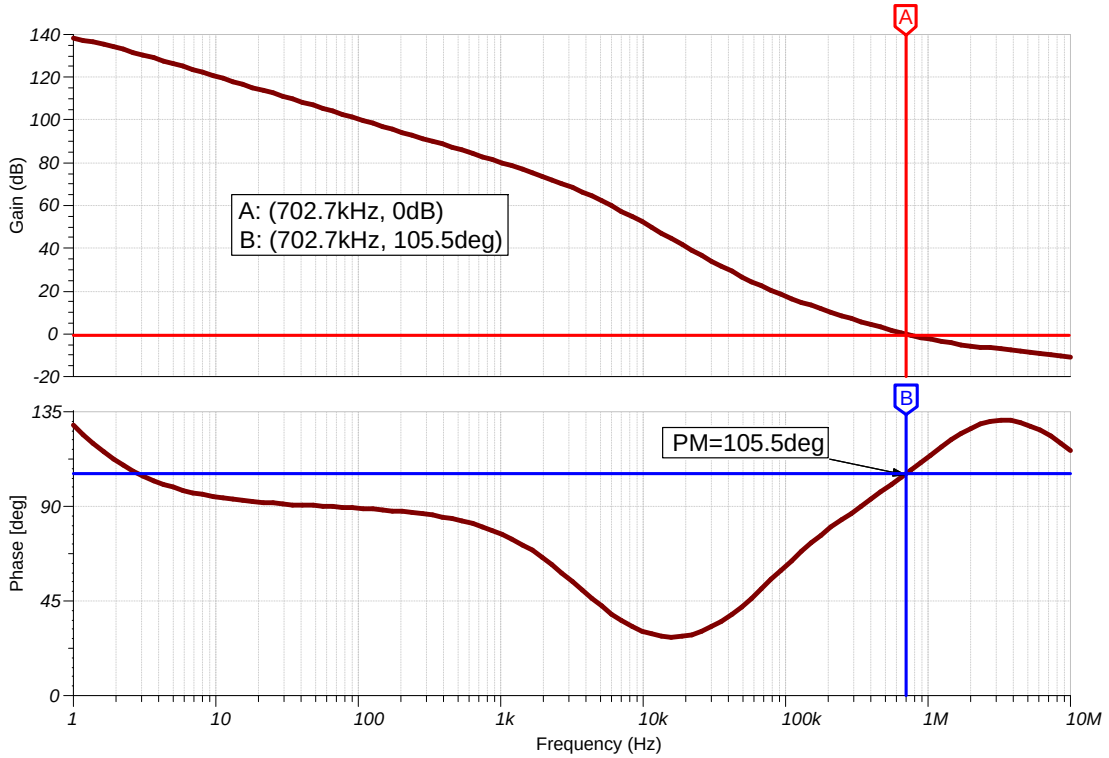

Figure 7: OPA192, C_{load}=0.1 µF, R_{iso}=23.7 Ω, PM=105.5º

One drawback to stabilizing capacitive loads using an isolation resistor is dc accuracy. [2] If the op amp is required to supply significant current, a voltage drop will develop across R_{iso}. Therefore it is recommended to minimize R_{iso} to increase dc accuracy.

However, reducing R_{iso} will also reduce phase margin. 45° and 60° of phase margin are commonly used in practical designs. [1]

The values of R_{iso} that correspond to phase margins of ~45° and ~60° were determined empirically and are depicted in Figure 8 and Figure 9, respectively.

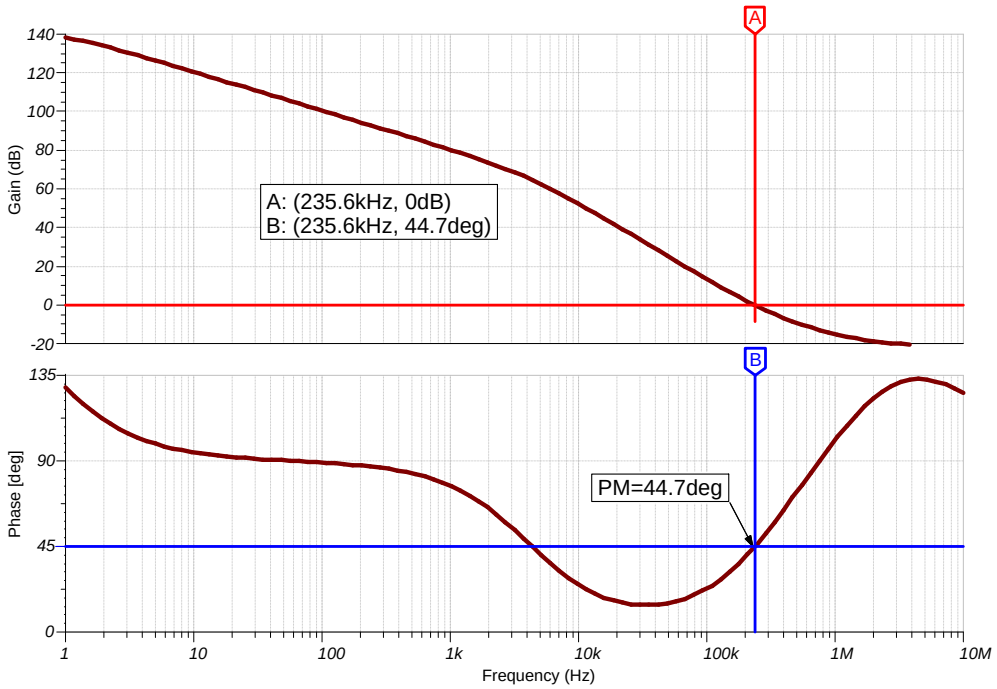

Figure 8: OPA192, C_{load}=0.1 µF, R_{iso}=4.87 Ω, PM=44.7°

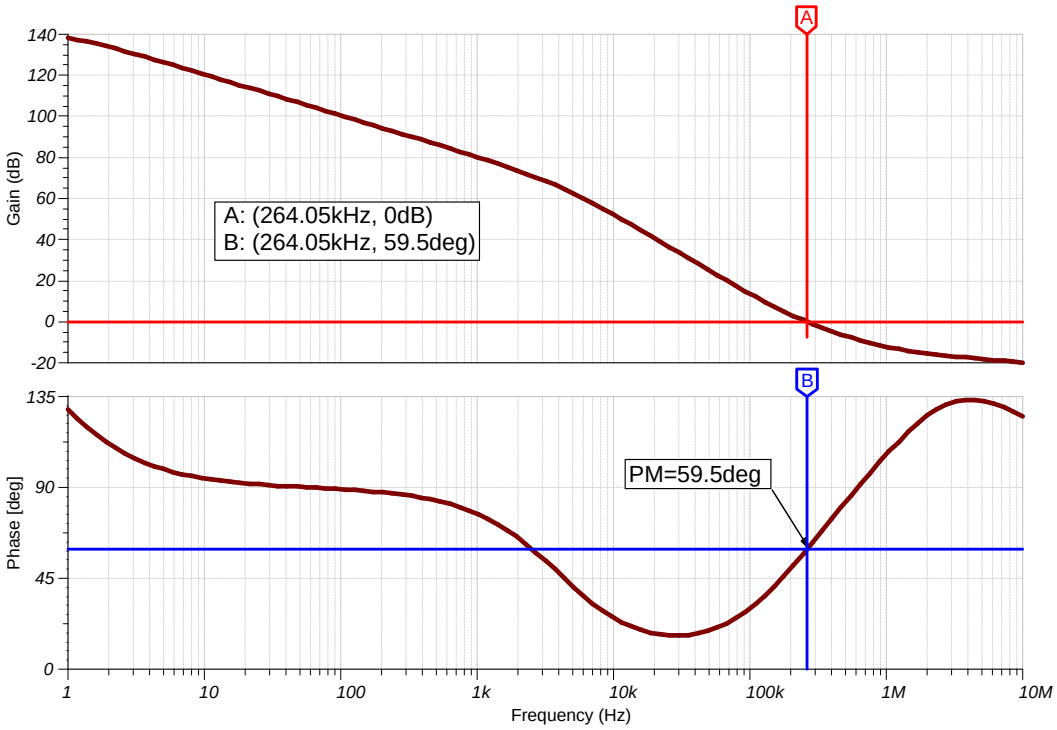

Figure 9: OPA192, C_{load}=0.1 µF, R_{iso}=7.15 Ω, PM=59.5°

Component tolerance also affects the phase margin of the system. The simulation in Figure 10 shows a reduction in phase margin of 1.3º given R_{iso} and C_{load} tolerances of 1% and 5%, respectively. Appendix D contains additional simulations of component tolerance on phase margin.

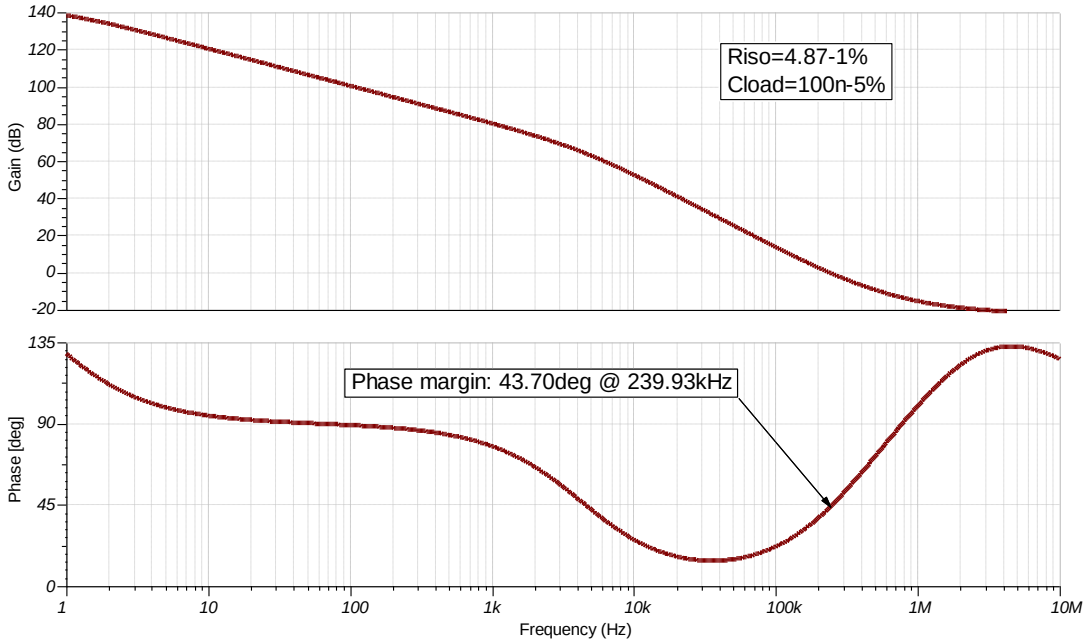

Figure 10: OPA192, C_{load}=100 nF-5%, R_{iso}=4.87 Ω-1%, PM=43.7º

5 PCB Design

The PCB schematic and bill of materials can be found in Appendix A.

5.1 PCB Layout

The PCB shown in Figure 11 is composed of two layers with signals and power routed on the top layer. The remainder of the top layer was poured with ground copper and stitched to a solid ground plane on the bottom layer. The bottom layer is a solid ground plane to ensure a low impedance path for return currents. General guidelines for PCB layout were followed. For example, input signal trace lengths were kept to a minimum and decoupling capacitors were placed close to the power pins of the device.

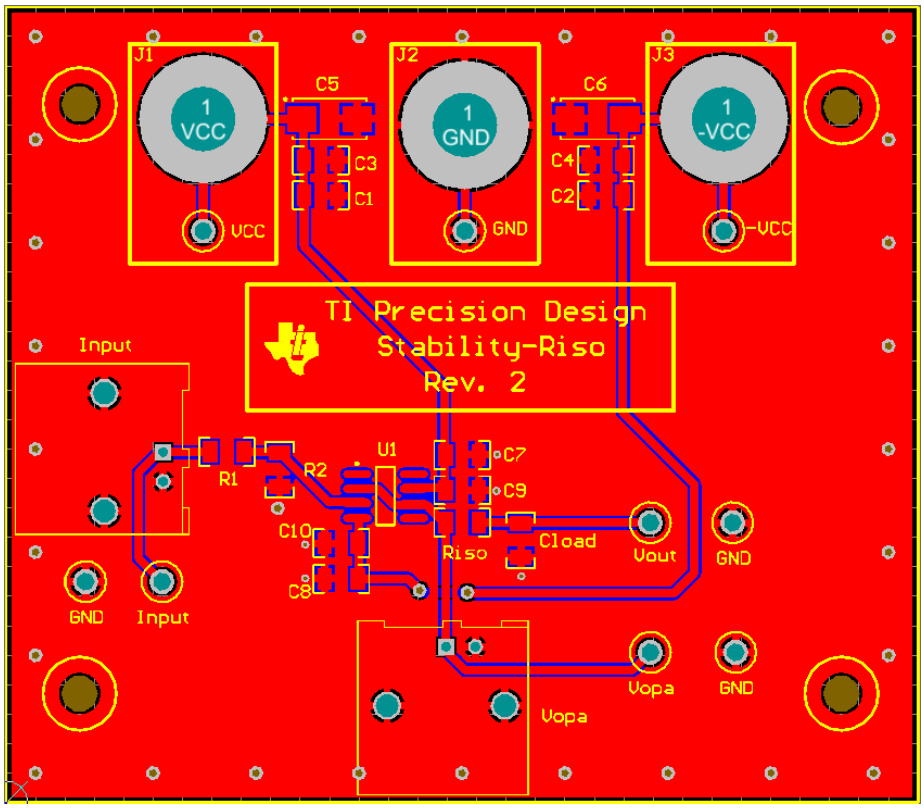

Figure 11: PCB Layout

6 Verification & Measured Performance

6.1 Transient Response

Figure 12 shows the transient response to a 10 mVpp step input where C_{load}=0.1 µF and R_{iso}=4.87 Ω. The overshoot measured at V_{opa} is 29.62%, which corresponds to a phase margin of 39.4°. The equations in Appendix B were used to calculate phase margin given percent overshoot.

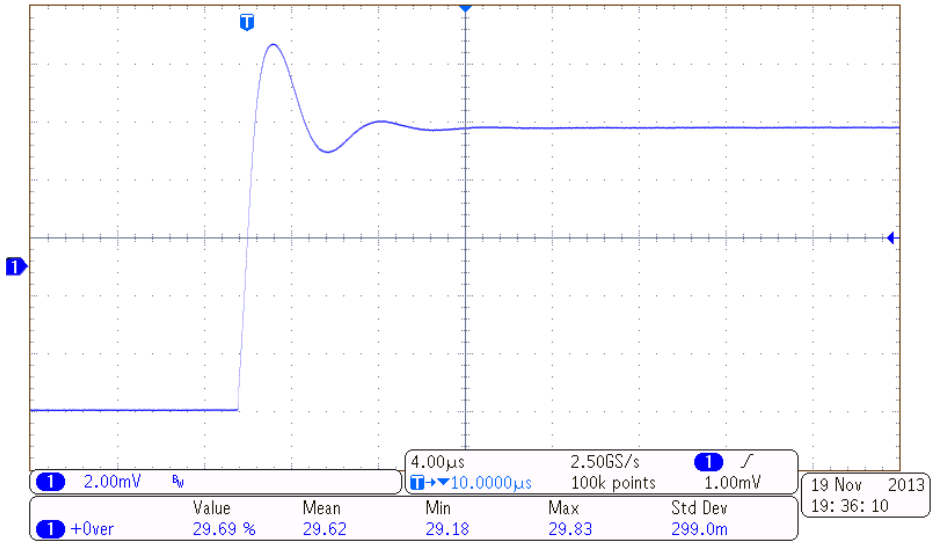

Figure 12: OPA192, C_{load}=0.1 µF, R_{iso}=4.87 Ω, PM=39.4°

Many factors can cause this discrepancy, including passive element tolerances, A_{ol} and R_o variation due to process shifts, and measurement/PCB non-idealities.

To achieve a phase margin of ~45º, R_{iso} was increased to 6.2 Ω. The resulting transient response is shown in Figure 13.

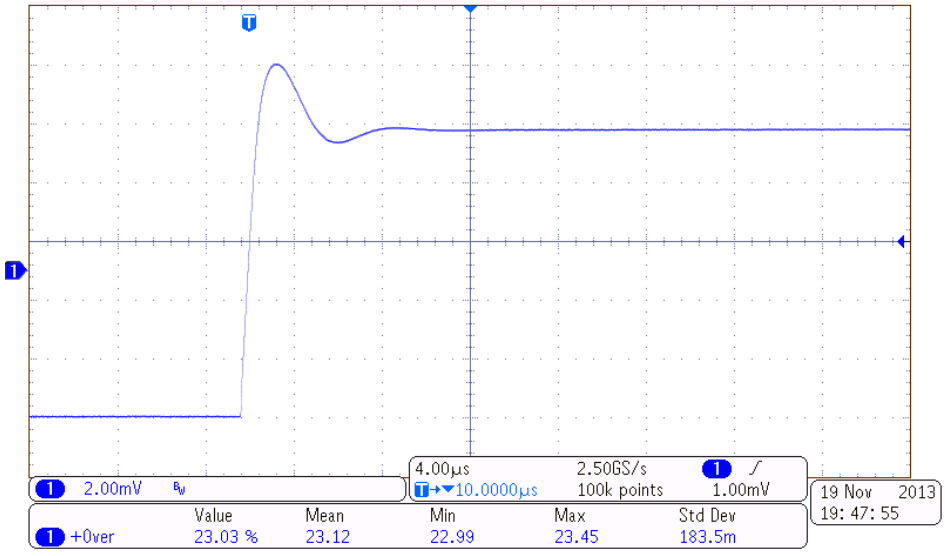

Figure 13: OPA192, C_{load}=0.1 µF, R_{iso}=6.2 Ω, PM=45.2°

For some scenarios (e.g. large capacitive loads), the magnitude of the input stimulus was reduced until the output response had a waveform similar to Figure 13. For more information, please refer to [4].

6.2 AC Response

Figure 14 depicts the ac response of the OPA192 when C_{load}=0.1 µF and R_{iso}=6.2 Ω. The ac gain peaking is 2.5 dB, which corresponds to a phase margin of 44.2°. These results correlate with the phase margin reported in Figure 8.

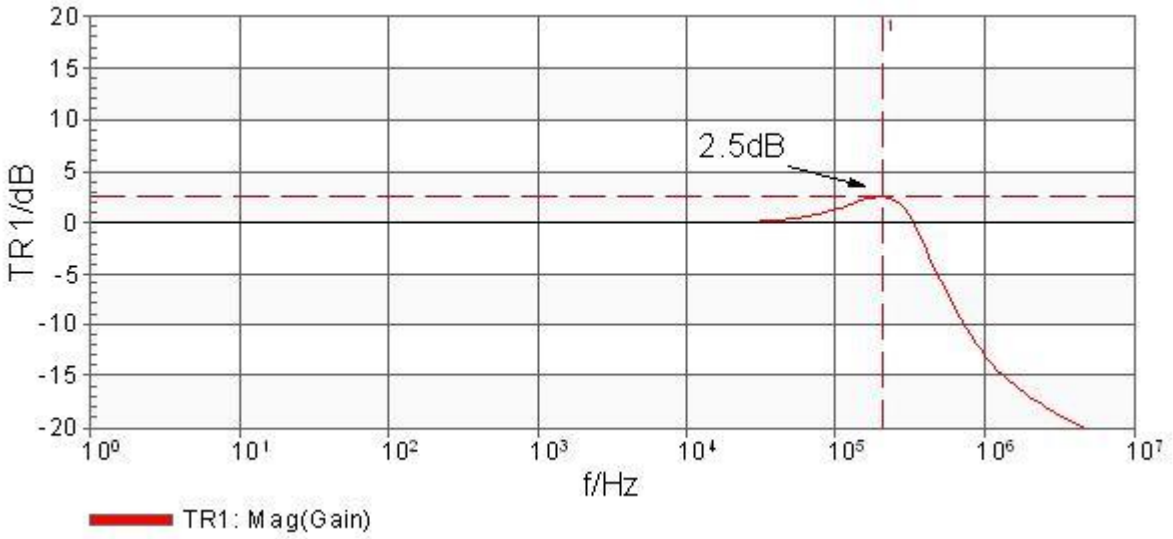

Figure 14: OPA192, C_{load}=0.1 µF, R_{iso}=6.2 Ω, PM=44.2°

6.3 R_{iso} vs. C_{load}

Using the described methodology, the values of R_{iso} that yield phase margins of 45º and 60º for various capacitive loads were determined. The results are shown in Figure 15.

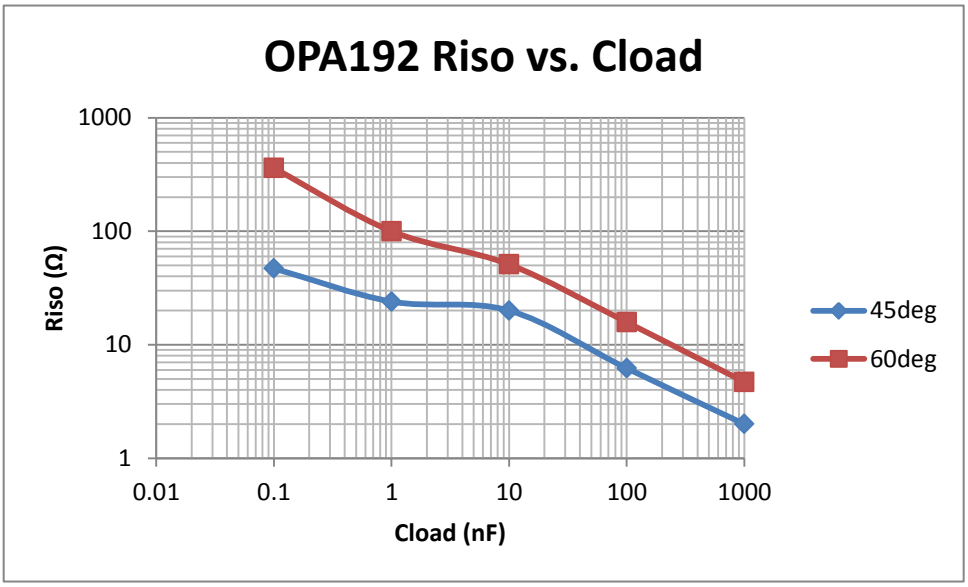

Figure 15: OPA192, R_{iso} vs. C_{load}

Additional R_{iso} vs. C_{load} graphs for various op amps can be found in Appendix C.

It is sometimes desirable to know the phase margin for a capacitive load without R_{iso} compensation. Figure 16 depicts the phase margin for a variety of capacitive loads where R_{iso}=0 Ω. Note that the OPA192 can deliver reasonable PM for larger capacitive loads than most op amps.

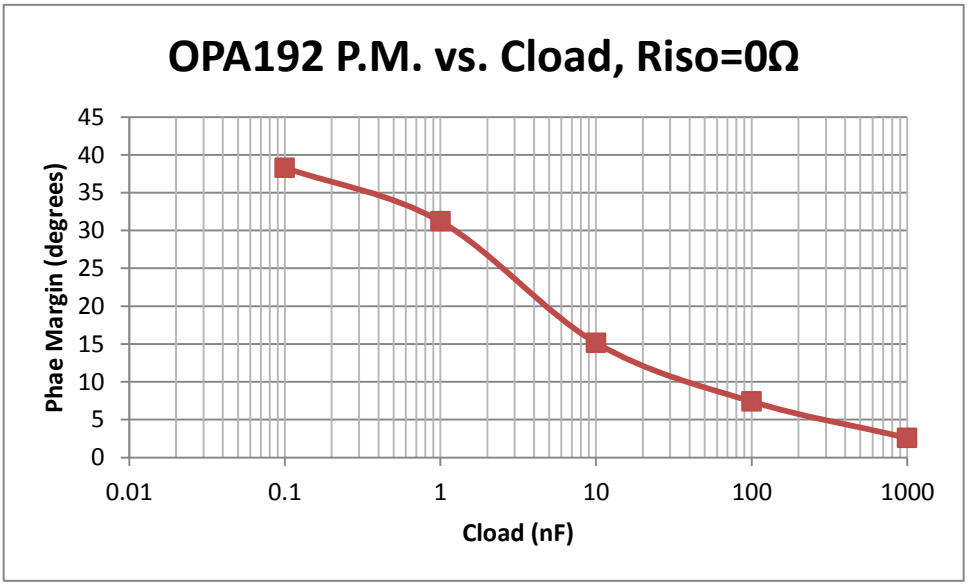

Figure 16: OPA192, PM vs. C_{load}, R_{iso}=0 Ω

7 Modifications

As mentioned earlier, one drawback to R_{iso} compensation is dc accuracy. One alternative is 'R_{iso} with dual feedback' compensation, as shown in Figure 17. This technique has an additional feedback path that corrects for the voltage drop across R_{iso}. The design of this compensation technique is discussed in references [1]-[3].

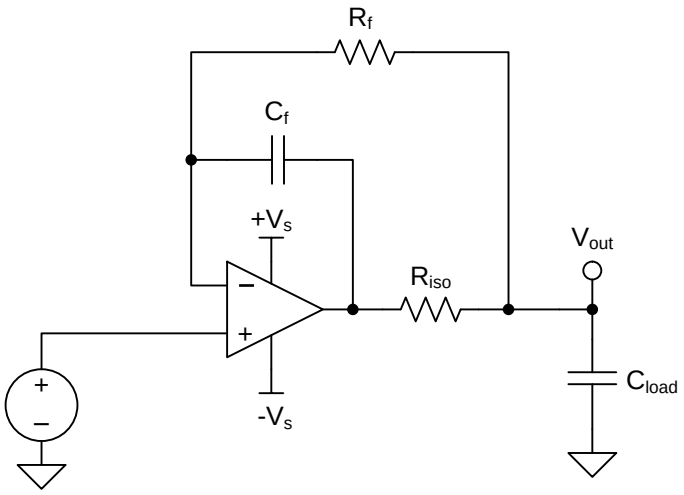

Figure 17: R_{iso} with Dual Feedback

8 About the Authors

Pete Semig is an Analog Applications Engineer in the Precision Linear group at Texas Instruments. He supports Texas Instruments' difference amplifiers & instrumentation amplifiers. Prior to joining Texas Instruments in 2007, he earned his B.S.E.E. and M.S.E.E. from Michigan State University in 1998 & 2001, respectively. From 2001-2007 he was a faculty member in Michigan State University's Department of Electrical & Computer Engineering where he taught a variety of courses and laboratories.

Timothy Claycomb was an intern for the Precisions Linear group at Texas Instruments. He currently is an undergraduate student pursuing a B.S. in Electrical Engineering at Michigan State University and will graduate in December of 2013.

9 Acknowledgements & References

The authors would like to acknowledge Collin Wells and Mike Mock for their technical contributions to this design.

1. *S. Franco, Design with Operational Amplifiers and Analog Integrated Circuits, 3rd Edition. McGraw-Hill, 2002.*

2. *T. Green. (Accessed 2013, October 22). Operational Amplifier Stability Parts 1-10. Available: http://www.en-genius.net/site/zones/acquisitionZONE/technical_notes/acqt_092407*

3. *C. Wells, Operational Amplifier Stability, Technology Day Presentation, 2012.*

4. *C. Wells. (Accessed 2013, December 2). Transient Stability Testing: Watch Your Step. Available: http://www.planetanalog.com/author.asp?section_id=3117&doc_id=560860*

Appendix A.

A.1 Electrical Schematic

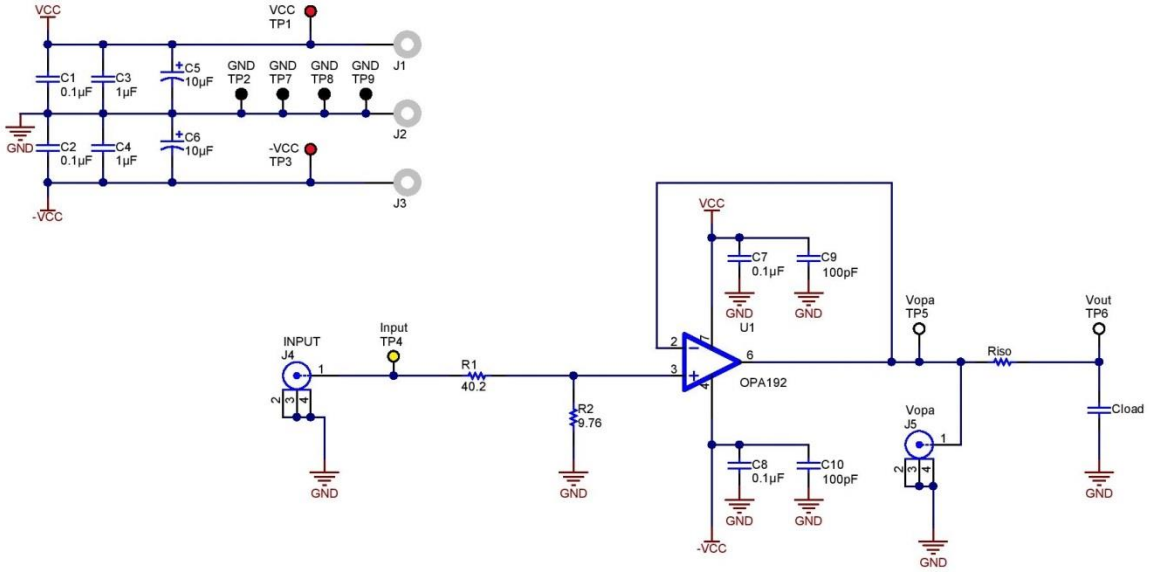

Figure A-1: Electrical Schematic

A.2 Bill of Materials

	QTY	Designator	Value	Description	Manufacturer	Manufacturer PN	DigiKey PN
1	1	U1	OPA192	Op Amp, SOIC-8	Texas Instruments		
2	1	Riso	Various	RES, 0.25W, 1206	Various	Various	Various
3	1	Cload	Various	CAP, CERM, 1206	Various	Various	Various
4	1	TP6	Vout	TEST POINT PC COMPACT .063"D WHT	Keystone	5007	5007K-ND
5	1	TP5	Vopa	TEST POINT PC COMPACT .063"D WHT	Keystone	5007	5007K-ND
6	1	TP4	Input	TEST POINT PC COMPACT .063"D YLW	Keystone	5009	5009K-ND
7	2	TP1, TP3	VCC, -VCC	TEST POINT PC COMPACT .063"D RED	Keystone	5005	5005K-ND
8	4	TP2, TP7, TP8, TP9	GND	TEST POINT PC COMPACT .063"D BLK	Keystone	5006	5006K-ND
9	1	R2	9.76	RES, 9.76 ohm, 1%, 0.25W, 1206	Vishay-Dale	CRCW12069R76FKEA	541-9.76FFCT-ND
10	1	R1	40.2	RES, 40.2 ohm, 1%, 0.25W, 1206	Vishay-Dale	CRCW120640R2FKEA	541-40.2FCT-ND
11	2	J4, J5	Input, Vopa	CONN BNC JACK R/A 50 OHM PCB	TE Connectivity	1-1337543-0	A97553-ND
12	3	J1, J2, J3	VCC, GND, -VCC	JACK NON-INSULATED .218"	Keystone	575-4	575-4K-ND
13	2	C9, C10	100pF	CAP, CERM, 100pF, 100V, +/-5%, C0G/NP0, 1206	AVX	12061A101JAT2A	478-1444-1-ND
14	2	C5, C6	10uF	CAP, TA, 10uF, 25V, +/-10%, 0.5 ohm, SMD	AVX	TPSC106K025R0500	478-1762-1-ND
15	2	C3, C4	1uF	CAP, CERM, 1uF, 100V, +/-10%, X7R, 1206	MuRata	GRM31CR72A105KA01L	490-3909-1-ND
16	4	C1, C2, C7, C8	0.1uF	CAP, CERM, 0.1uF, 100V, +/-20%, X7R, 1206	AVX	12061C104MAT2A	478-3786-1-ND
17	4	U94, U95, U96, U97	N/A	MACHINE SCREW PAN PHILLIPS 4-40	B&F Fastener	PMSSS 440 0025 PH	H703-ND
18	4	U90, U91, U92, U93	N/A	STANDOFF HEX 4-40THR ALUM 1L"	Keystone	2205	2205K-ND

Figure A-2: Bill of Materials

Appendix B.

B.1 Percent Overshoot and AC Gain Peaking vs. Phase Margin

Percent overshoot and ac gain peaking are related to phase margin (φ_m) via damping ratio (ζ). Equation (3) and Figure 18 depict the relationship between ζ and phase margin.

$$\phi_m(\zeta) := \frac{180}{\pi} \operatorname{atan}\left[2\cdot\zeta\cdot\left(\sqrt{\frac{1}{\sqrt{4\cdot\zeta^4+1}-2\cdot\zeta^2}}\right)\right] \tag{3}$$

where

$$\zeta := 0.0, 0.001 .. 0.707 \tag{4}$$

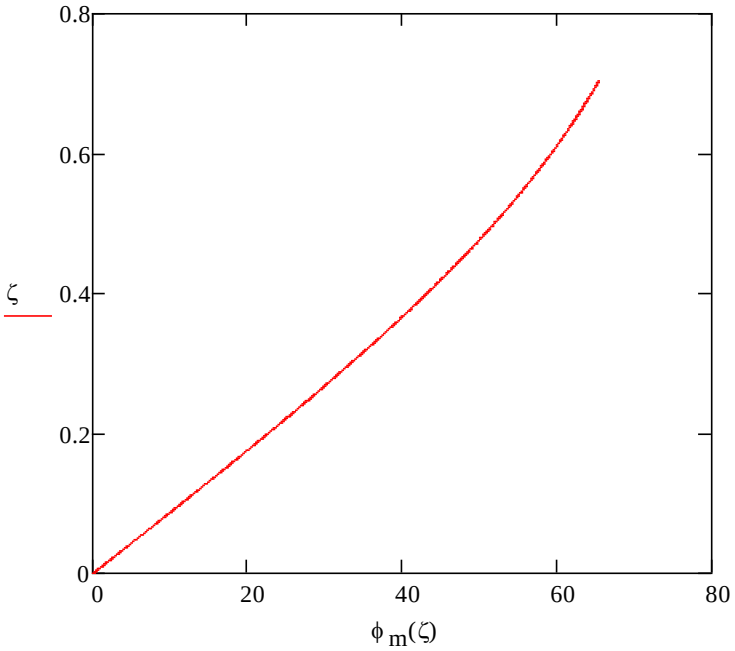

Figure 18: Damping Ratio vs. Phase Margin

Percent overshoot and ac gain peaking relate to phase margin as shown by Equation(5), Equation (6), and Figure 19.

$$PO(\zeta) := 100 \cdot \exp\left(\frac{-1\pi \cdot \zeta}{\sqrt{1-\zeta^2}}\right) \tag{5}$$

$$GP(\zeta) := 20 \cdot \log\left(2 \cdot \frac{Q(\zeta)^2}{\sqrt{4 \cdot Q(\zeta)^2 - 1}}\right) \tag{6}$$

where

$$Q(\zeta) := \frac{1}{2 \cdot \zeta} \tag{7}$$

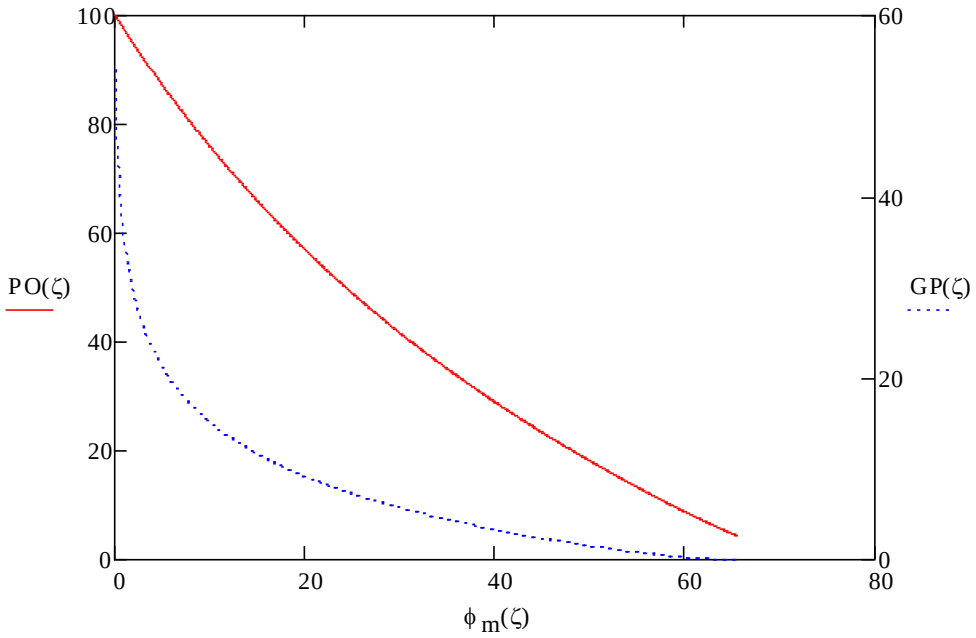

Figure 19: PO and GP vs. Phase Margin

Calculate percent overshoot and ac gain peaking (in dB) for 45° of phase margin as follows:

$$\text{Given} \quad \zeta := 0 \tag{8}$$

$$\frac{180}{\pi} \text{atan}\left[2 \cdot \zeta \cdot \left(\sqrt{\frac{1}{\sqrt{4 \cdot \zeta^4 + 1} - 2 \cdot \zeta^2}}\right)\right] = 45 \tag{9}$$

$$\zeta_{45} := \text{Find}(\zeta) \qquad \zeta_{45} = 0.42 \tag{10}$$

$$PO_{45} := 100 \cdot \exp\left(\frac{-\pi \cdot \zeta_{45}}{\sqrt{1-\zeta_{45}^2}}\right) = 23.321 \tag{11}$$

$$GP_{45} := 20 \cdot \log\left(2 \cdot \frac{Q(\zeta_{45})^2}{\sqrt{4 \cdot Q(\zeta_{45})^2 - 1}}\right) = 2.35 \tag{12}$$

Repeat the calculations to determine percent overshoot and ac gain peaking for 60° of phase margin.

B.2 Phase Margin vs. Percent Overshoot

After measuring the percent overshoot of a transient analysis, Equations 13 to 15 can be used to calculate the corresponding phase margin.

$$PO := 23.321 \tag{13}$$

$$\zeta := \frac{-\ln\left(\frac{PO}{100}\right)}{\sqrt{\pi^2 + \left(\ln\left(\frac{PO}{100}\right)\right)^2}} = 0.42 \tag{14}$$

$$\phi_m := \frac{180}{\pi} \operatorname{atan}\left[2 \cdot \zeta \cdot \left(\sqrt{\frac{1}{\sqrt{4 \cdot \zeta^4 + 1} - 2 \cdot \zeta^2}}\right)\right] = 45 \tag{15}$$

Appendix C.

All measured data values can be found in the design file archive. If no data points exist for 100pF scenario, the amplifier does not require an isolation resistor for stable operation. If no data points exist for 1µF scenario, the isolation resistor required for stable operation is less than 1 Ω.

C.1 OPA140

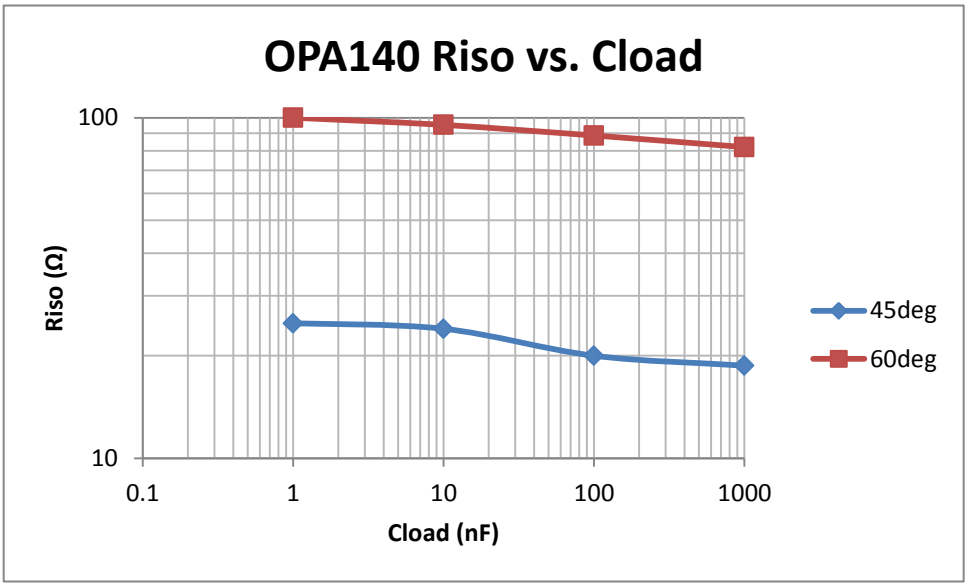

Figure 20: OPA140, R_{iso} vs. C_{load}

C.2 OPA170

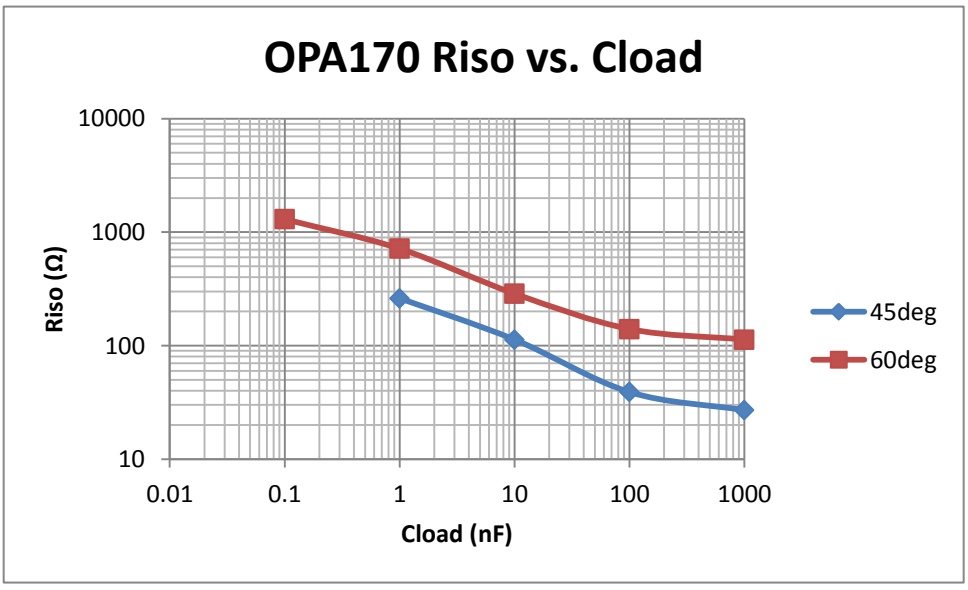

Figure 21: OPA170, R_{iso} vs. C_{load}

C.3 OPA171

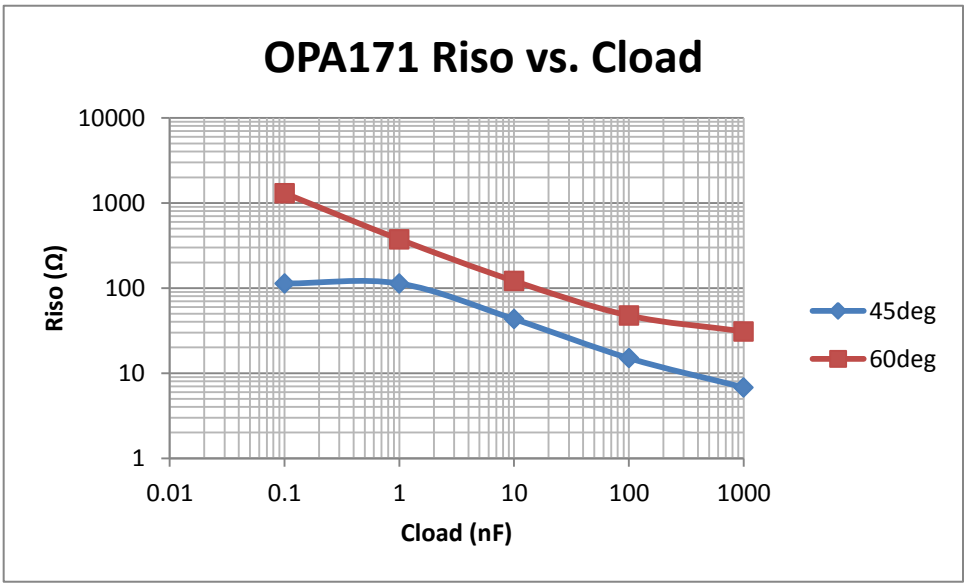

Figure 22: OPA171, R_{iso} vs. C_{load}

C.4 OPA172

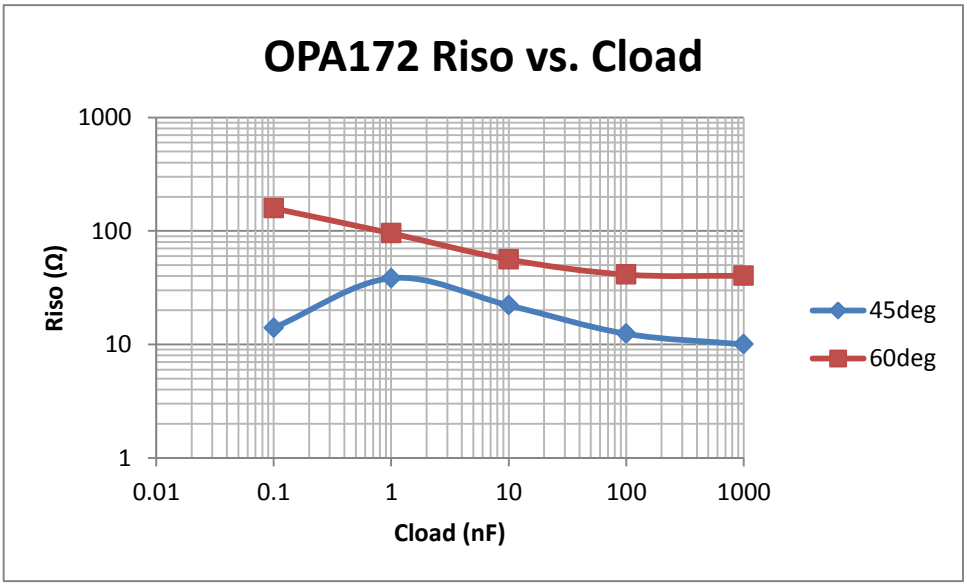

Figure 23: OPA172, R_{iso} vs. C_{load}

C.5 OPA180

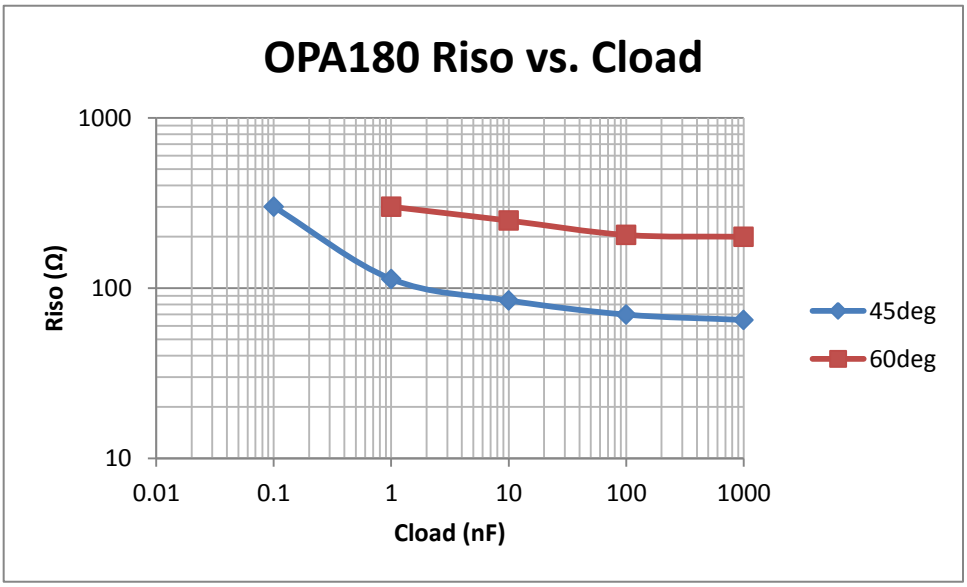

Figure 24: OPA180, R_{iso} vs. C_{load}

C.6 OPA209

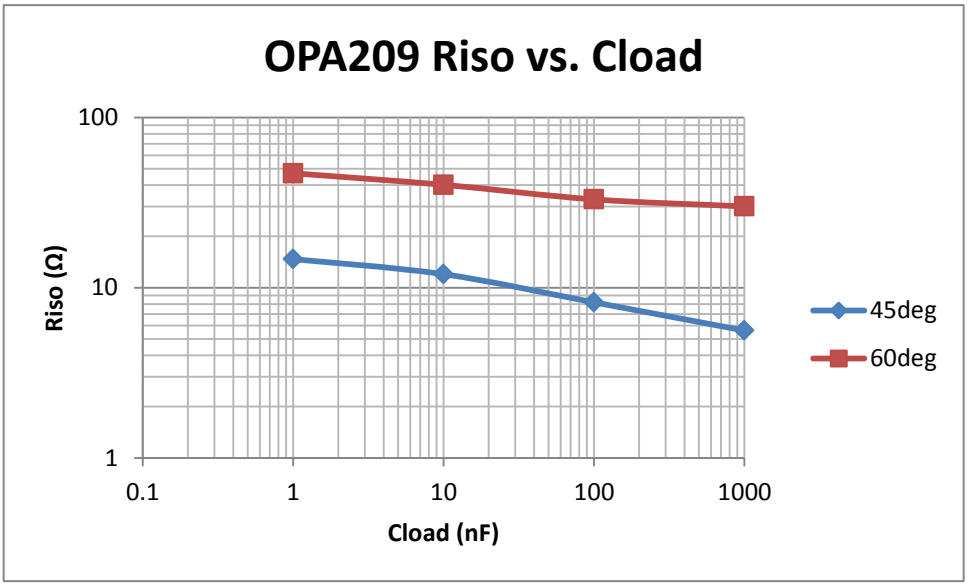

Figure 25: OPA209, R_{iso} vs. C_{load}

C.7 OPA320

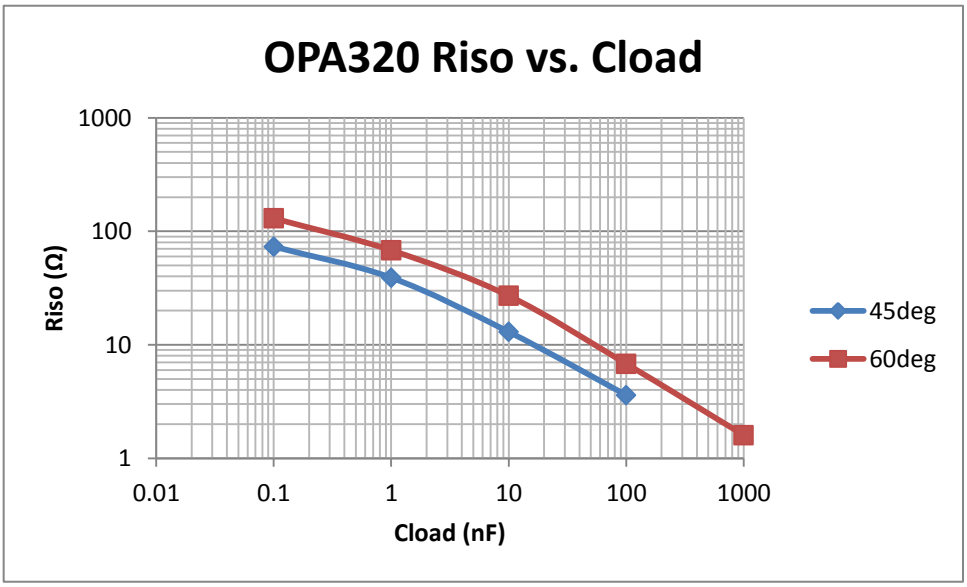

Figure 26: OPA320, R_{iso} vs. C_{load}

C.8 OPA340

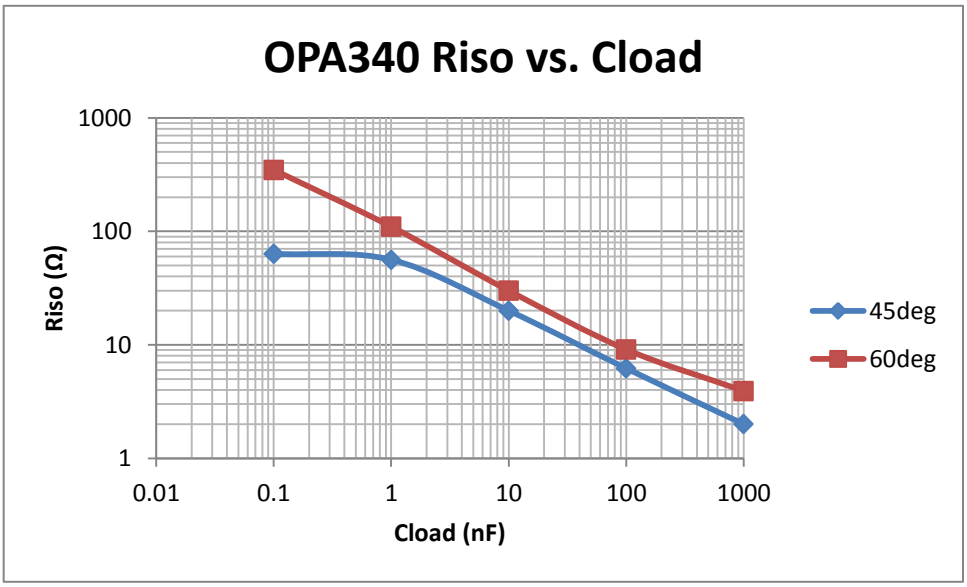

Figure 27: OPA340, R_{iso} vs. C_{load}

C.9 OPA350

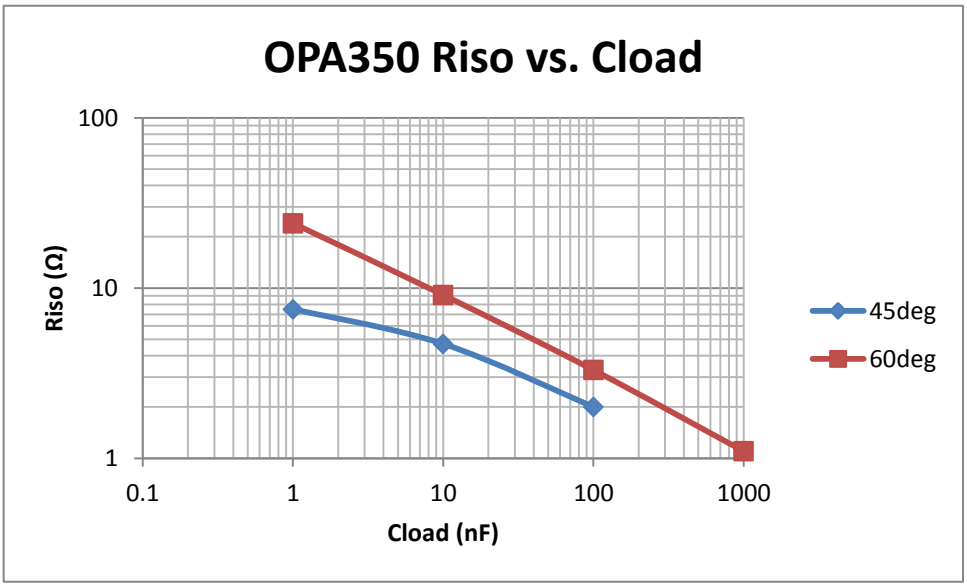

Figure 28: OPA350, R_{iso} vs. C_{load}

C.10 OPA365

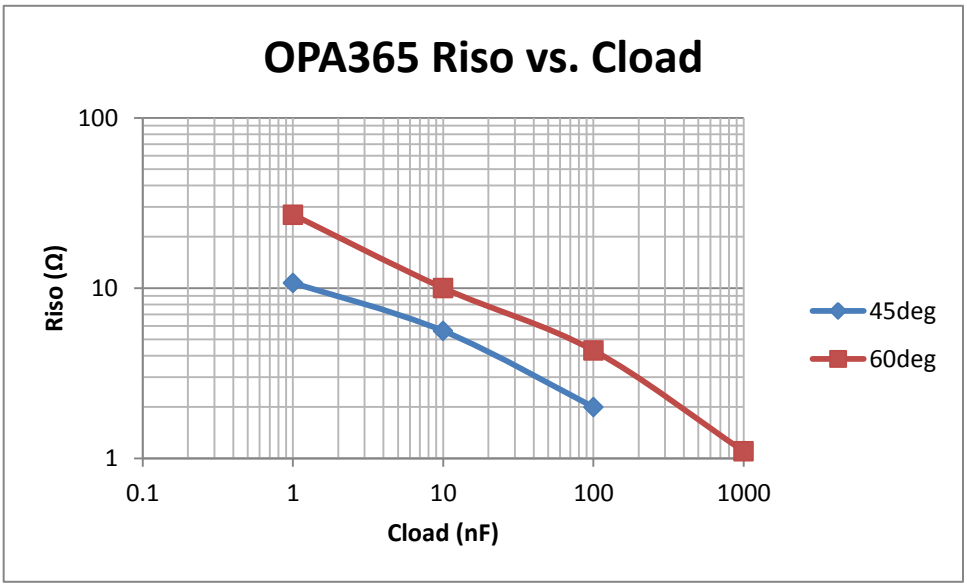

Figure 29: OPA365, R_{iso} vs. C_{load}

Appendix D. Passive Tolerance Simulations

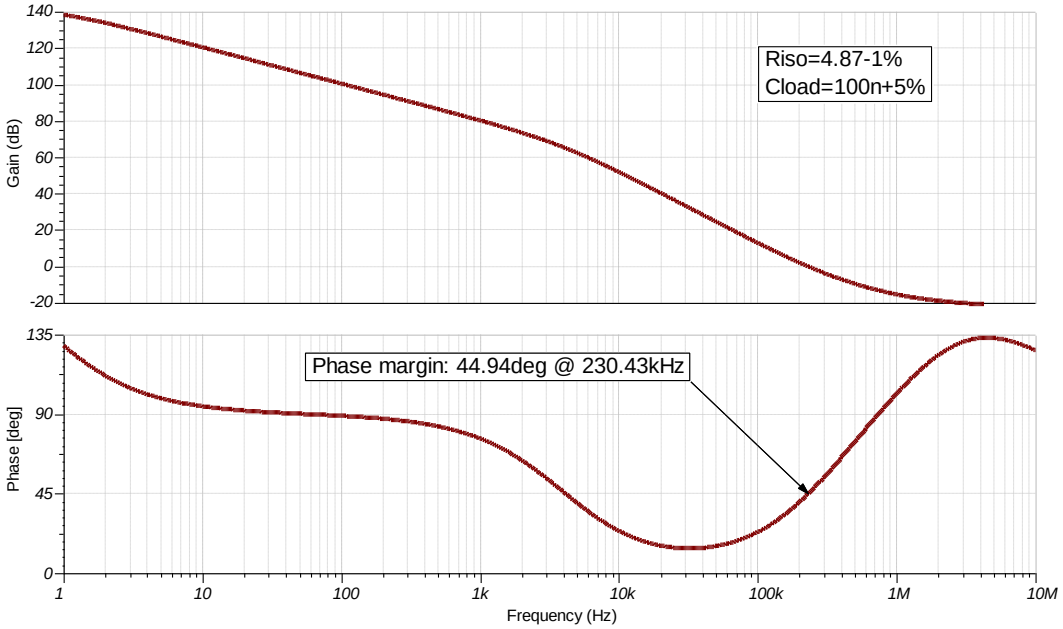

Figure 30: OPA192, C_{load}=100 nF+5%, R_{iso}=4.87 Ω-1%, PM=44.94º

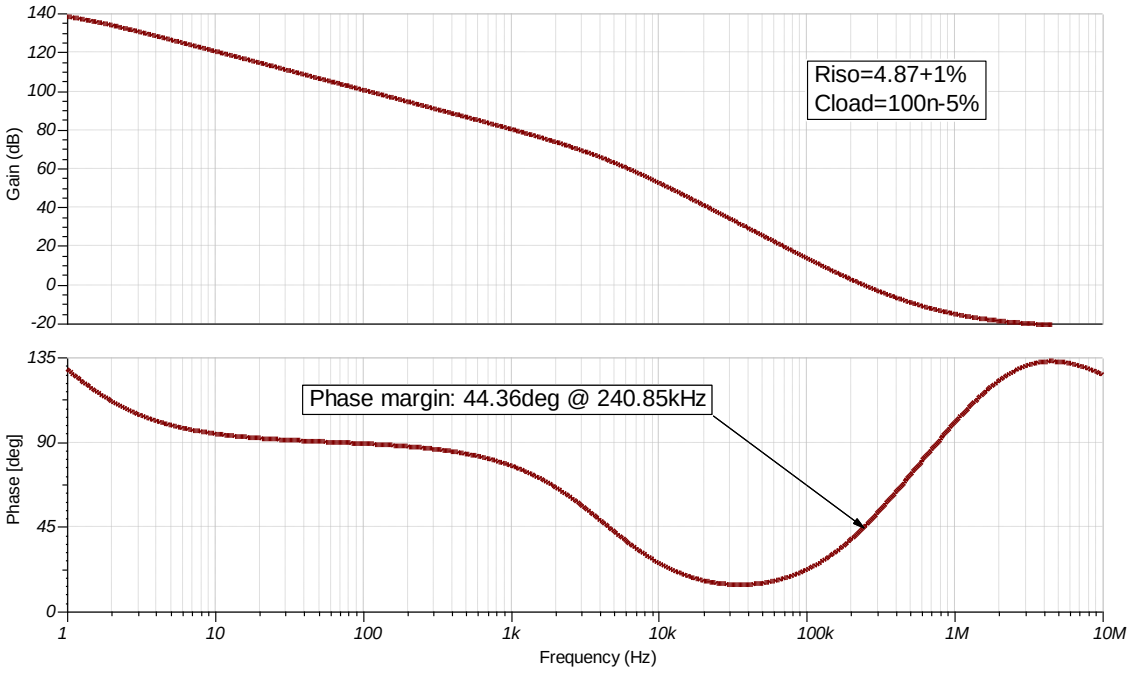

Figure 31: OPA192, C_{load}=100 nF-5%, R_{iso}=4.87 Ω+1%, PM=44.36º

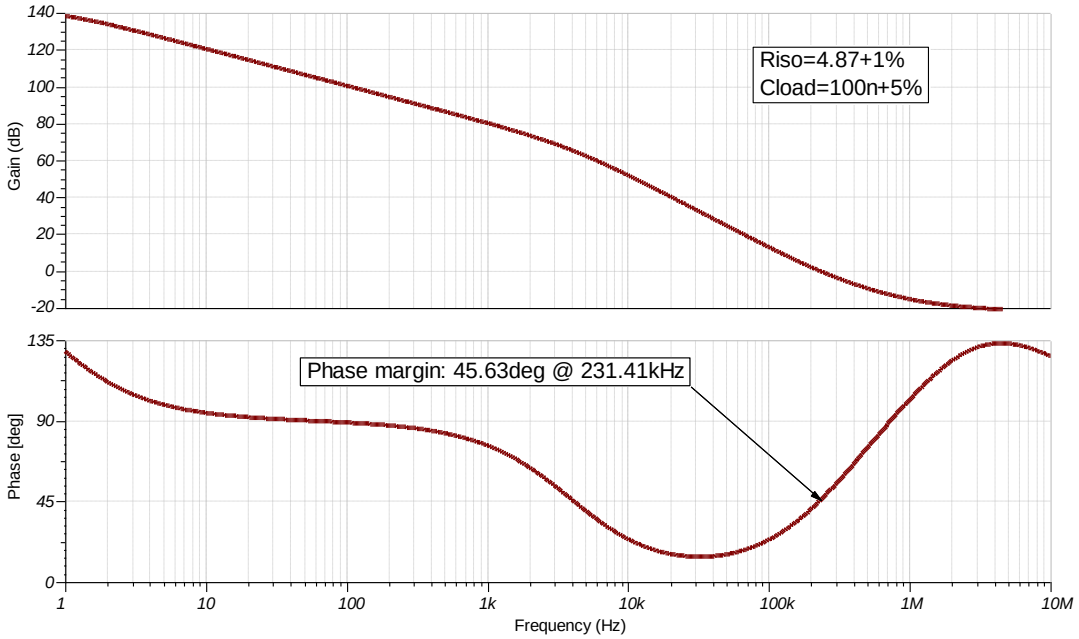

Figure 32: OPA192, C_{load}=100 nF+5%, R_{iso}=4.87 Ω+1%, PM=45.63º

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