

TI Precision Designs: Verified Design 18-Bit Data Acquisition (DAQ) Block Optimized for 1- μ s Full-Scale Step Response



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Design Resources

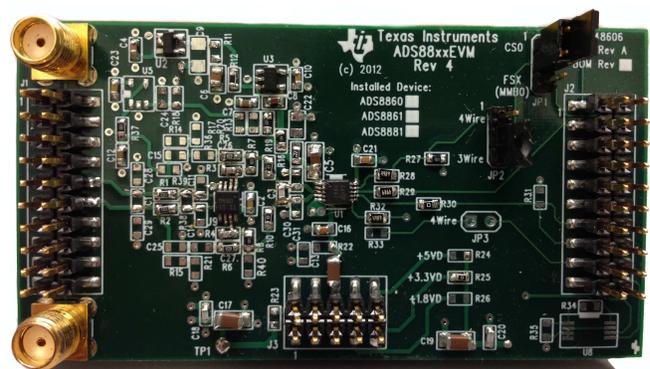
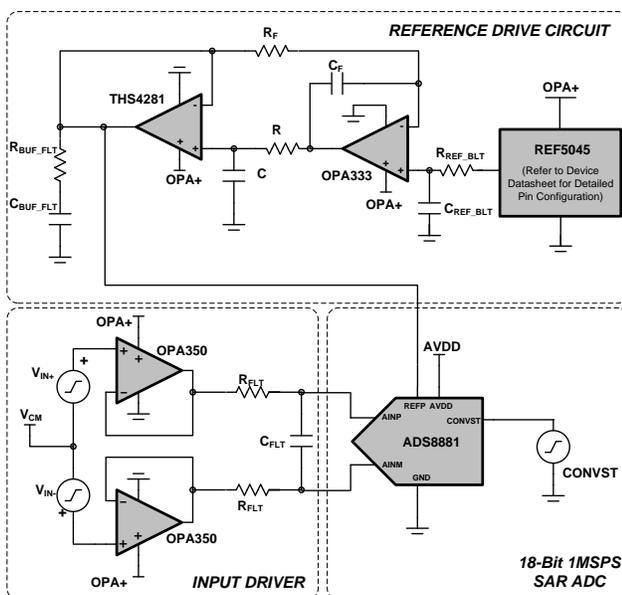
Design Archive	All design files
TINA-TI™	SPICE simulator
ADS8881	Product folder
OPA2350	Product folder
REF5045	Product folder
OPA2333	Product folder
THS4281	Product folder
REF6045	Product Folder

Circuit Description

This circuit describes a data acquisition (DAQ) block comprising of an 18-bit successive-approximation-register (SAR) analog-to-digital converter (ADC); front-end driver circuit for inputs of the ADC; an external reference and driver circuit for the ADC reference input. This design has been optimized to achieve excellent linearity and time-domain settling performance for a full-scale step input signal, which is common in applications using a multiplexer at the input of the ADC. The differential input signal is processed through high bandwidth and fast settling amplifiers configured as unity-gain buffers and low-pass RC-filter before being fed into the ADC.



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1 Design Summary

The primary objective for this TI Precision Design is to create an optimized data acquisition system using the 18-bit ADS8881, which achieves maximum performance for a transient step input signal of the full-scale range, at a throughput of 1 MSPS. The design requirements for this block design are:

- System supply voltage, OPA+: 5 V dc
- ADC supply voltage, AVDD: 3.3 V dc
- ADC sampling rate: 1 MSPS
- ADC reference voltage (V_{REF}): 4.5 V dc
- ADC input signal: Full-scale ($0\text{ V} - V_{REF}$) and out-of-phase step signals are applied to each differential input of the ADC

The design goals and performance are summarized in [Table 1](#). The response in [Figure 1](#) shows the output response of the DAQ block for a full-scale rising step signal at the input.

Table 1. Comparison of Design Goal, Simulation, and Measured Performance

PARAMETER	GOAL	SIMULATED	MEASURED
Power (mW)	≤ 70	NA ⁽¹⁾	58.48
18-bit settling time (ns)	≤ 500	389	Verified ⁽²⁾
Linearity (LSB)	± 2.5	NA ⁽³⁾	0.95/-1.28

⁽¹⁾ Power consumption for SAR ADC is not accurately modeled in the TINA-TI™ models

⁽²⁾ Refer to [Section 6.3](#) and [Section 6.4](#) for detailed measurement results on ADC input settling

⁽³⁾ Linearity is not simulated as TINA-TI™ models for SAR ADC do not have the capability to output digital codes

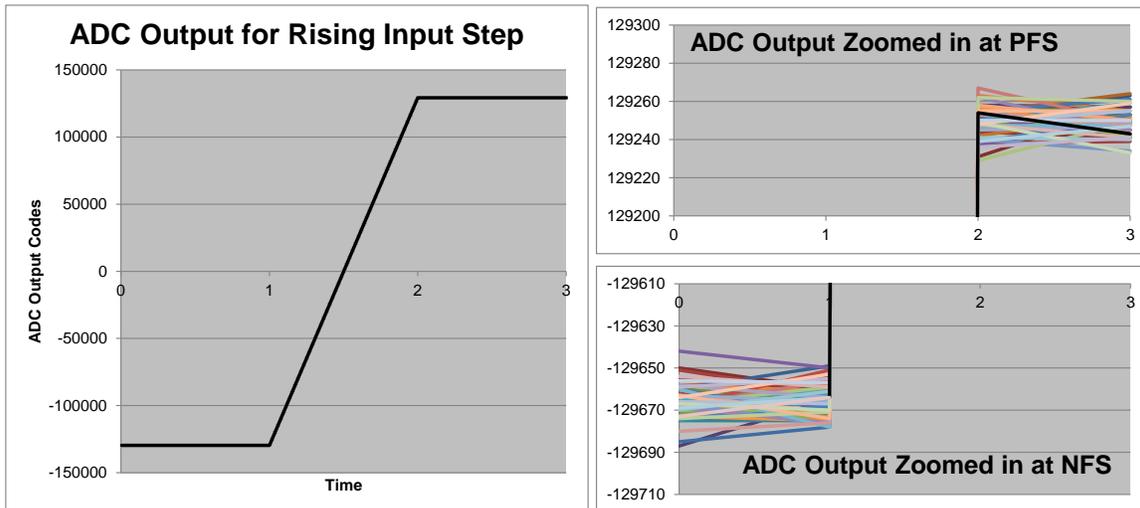


Figure 1. Measurement Data - ADC Transient Output Response for Rising Input Step



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2 Theory of Operation

The two primary design considerations to maximize the performance of a high-resolution SAR ADC are the input driver and the reference driver. Figure 2 shows a block diagram comprised of the critical analog circuit blocks, which should be carefully designed to achieve the design specifications of an 18-bit 1MSPS DAQ block. The figure also includes the most important specifications for each individual analog block in the order of design priority. This order is important because the design criteria for each block is dependent on the desired system performance as well as the input signal type.

This design uses an 18-bit, SAR ADC at a throughput of 1 MSPS and is optimized for a differential full-scale step input signal. The following design steps should be followed in order to meet the performance goals of this design:

- **Step 1:** Design an optimum anti-aliasing RC filter with sufficient bandwidth to allow 18-bit settling of the step signal at the ADC inputs.
- **Step 2:** Select an appropriate driving amplifier that meets the minimum specifications required to drive the ADC inputs.
- **Step 3:** Design a high-precision reference driver circuit, which should provide the required value of V_{REF} with low offset, drift, and noise contributions.

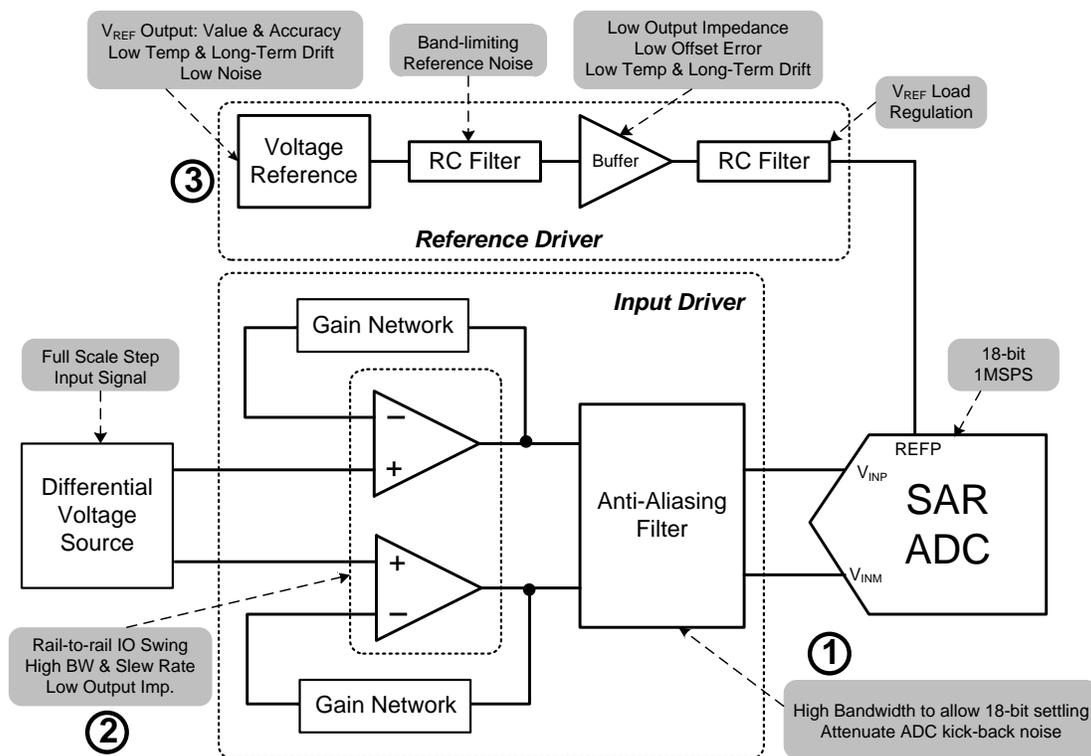


Figure 2. Block Diagram Highlighting Primary Design Criteria for this DAQ Block

2.1 Application Details of Input Signal

This TI Precision Design has been optimized for using TI's high-resolution and high-speed SAR ADCs at their maximum specified throughput for a full-scale step input voltage. Such input step signals are common in a multiplexed application when switching between different channels. In the worst-case scenario, one channel is at the negative full-scale (NFS) and the other channel is at the positive full-scale (PFS) voltage, in which case the step size is the full-scale range (FSR) of the ADC when the MUX channel is switched. An application circuit using a single-ended ADC is shown in Figure 3, but the same principle can be extended to differential input ADCs. In such applications, a constraint must be imposed on the timing of the MUX switching or the occurrence of the voltage step (in case of an independent transient voltage source) to ensure that the ADC input gets sufficient time for settling accurately.

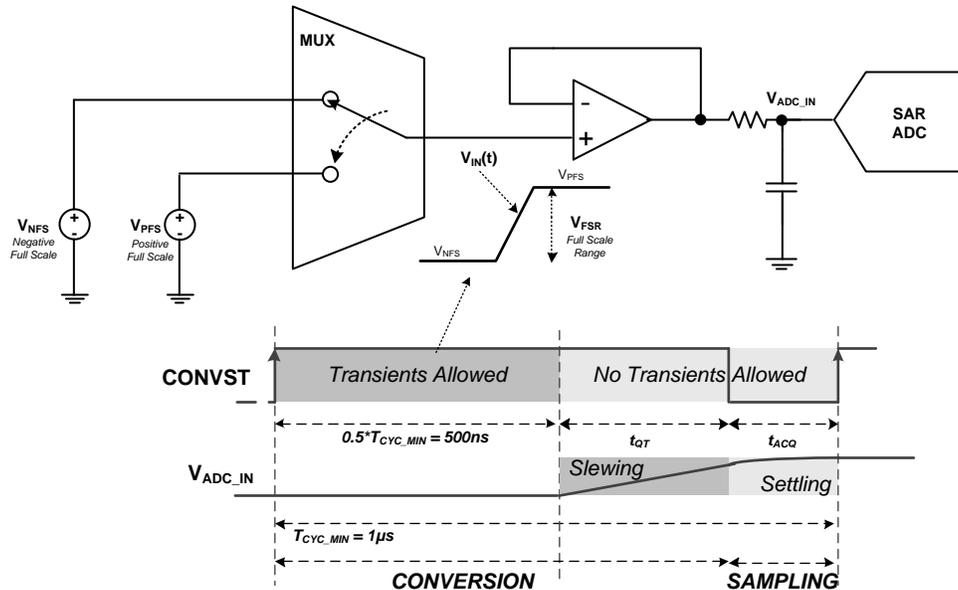


Figure 3. Timing Diagram For Input Stimulus

In order to operate a high-resolution, N -bit ADC at its maximum throughput, the full-scale voltage step must settle to better than N -bit accuracy at the ADC inputs within the minimum specified acquisition time (t_{ACQ}). This settling imposes very stringent requirements on the driver amplifier in terms of large-signal bandwidth, slew rate, and settling time. All these specifications come at the cost of higher-power consumption in the driver amplifier.

To optimize this circuit for power consumption and performance, this design does not allow any large-signal input transients at the inputs of the driver circuit for a small quiet-time period (t_{QT}) towards the end of the previous conversion. The input step voltage can appear anytime from the beginning of conversion ($CONVST$ rising edge) until the elapse of a half cycle time ($0.5 \times t_{CYC}$). This timing constraint on the input step allows a minimum settling time of ($t_{QT} + t_{ACQ}$) for the ADC input to settle within the required accuracy, in the worst-case scenario. This provides more time for the amplifier's output to slew and settle within the required accuracy before the next conversion starts.

2.2 Input Driver Design

An ADC input driver circuit mainly consists of two parts: a driving amplifier and a fly-wheel RC filter. The amplifier is used for signal conditioning of the input voltage and its low output impedance provides a buffer between the signal source and the ADC input. The RC filter helps attenuate the sampling charge-injection from the switched-capacitor input stage of the ADC as well as acts as an anti-aliasing filter to band-limit the wideband noise contributed by the front-end circuit.

The design of the ADC input driver involves optimizing the bandwidth of the circuit, driven primarily by the following requirements:

- The RC filter bandwidth should be low to band-limit the noise fed into the input of the ADC thereby increasing the signal-to-noise ratio (SNR) of the system.
- The overall system bandwidth should be large enough to accommodate optimal settling of the input signal at the ADC input before the start of conversion.

2.2.1 RC-Filter Design

In order to ensure that the output of the ADC is converted accurately, the voltage sampled at the input of the ADC must settle within $\frac{1}{2} \times \text{LSB}$ (least significant bit) during the acquisition time window. For a large differential input step equal to the full-scale range of the ADC, the overall bandwidth of the driver circuit should be higher than a certain minimum value. This value can be calculated by considering how the voltage at the ADC input changes during acquisition. This behavior is analyzed using a simplified single-ended ADC input stage (refer to Figure 4) in this design and the same concept can be extended to differential ADCs as well.

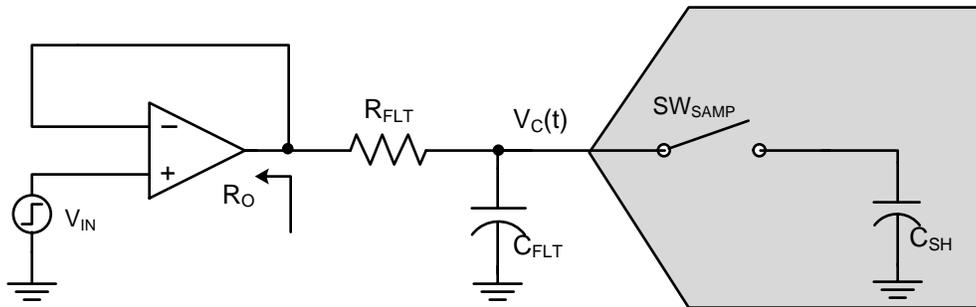


Figure 4. Simplified Schematic of Single-Ended ADC Input Stage

During sampling, the sampling switch SW_{SAMP} is closed and capacitor C_{SH} is charged through the switch. If the input voltage V_{IN} changes by a full-scale step from 0 V to V_{REF} as explained in Figure 3, then the voltage at the ADC input is denoted by Equation 1:

$$V_C(t) = V_{\text{REF}} \times \left(1 - e^{-\left(\frac{t}{\tau}\right)} \right)$$

where $\tau = R_{\text{FLT}} \times C_{\text{FLT}}$ (Assuming $C_{\text{FLT}} \gg C_{\text{SH}}$) (1)

As explained in Section 2.1, in the worst-case scenario the error at the input of the ADC settles within less than $\frac{1}{2} \times \text{LSB}$ in time ($t_{\text{QT}} + t_{\text{ACQ}}$).

$$V_{\text{REF}} - V_C(t) \leq \frac{1}{2} \text{LSB}, \quad \text{where } t = t_{\text{QT}} + t_{\text{ACQ}}$$

$$\Rightarrow V_{\text{REF}} \times e^{-\left(\frac{t}{\tau}\right)} \leq \frac{\text{LSB}}{2}$$

$$\Rightarrow \tau \leq \frac{t}{\ln \left[\frac{2 \times V_{\text{REF}}}{\text{LSB}} \right]}$$

(2)

Equation 2 leads to the minimum required bandwidth for the RC filter as shown in Equation 3:

$$\frac{1}{R_{FLT} \times C_{FLT}} = \frac{1}{\tau} \geq \frac{\ln\left[\frac{2 \times V_{REF}}{LSB}\right]}{t}, \quad \text{where } t = t_{QT} + t_{ACQ} \quad (3)$$

The capacitor C_{FLT} helps reduce the sampling charge-injection at the ADC input and provides a charge bucket to quickly charge the input capacitor C_{SH} during the sampling process. The value of the capacitor C_{FLT} should be chosen such that when switch SW_{SAMP} closes, the voltage droop (ΔV_{FLT}) on C_{FLT} is less than 5% of the input voltage.

The charge required for the ADC sampling capacitor is given by Equation 4:

$$Q_{IN} = C_{SH} \times V_{REF} \quad (4)$$

The charge supplied by the filter capacitor is given by Equation 5:

$$Q_{FLT} = C_{FLT} \times \Delta V_{FLT} \leq C_{FLT} \times (0.05 \times V_{REF}) \quad (5)$$

By the principle of charge conservation, the charge required by the sampling capacitor should be equal to the charge provided by the filter capacitor. Hence, the following equation can be derived:

$$\begin{aligned} Q_{IN} &= Q_{FLT} \\ \Rightarrow C_{FLT} \times (0.05 \times V_{REF}) &\geq C_{SH} \times V_{REF} \end{aligned} \quad (6)$$

$$\Rightarrow C_{FLT} \geq 20 \times C_{SH} \quad (7)$$

Using Equation 3 and Equation 7, the values of R_{FLT} and C_{FLT} can be calculated as a function of the ADC input capacitance and maximum throughput. Note that the minimum bandwidth of the RC filter is proportionally reduced if the ADC is operated at a reduced sampling speed.

At this point, understanding the trade-offs involved in selecting the values of C_{FLT} and R_{FLT} is important. If the value of C_{FLT} is high, it provides better attenuation against the charge-injection noise when the sampling switch closes. However, C_{FLT} cannot be made arbitrarily high because it degrades the phase margin of the driving amplifier, making it unstable. The series resistor R_{FLT} functions as an isolation resistor, which helps stabilize the driving amplifier, as explained in [1] and [2]. A higher value of R_{FLT} is helpful from the amplifier stability perspective, but higher values of R_{FLT} add distortion due to interactions with the non-linear input impedance of the ADC. The distortion increases with source impedance, input signal frequency, and input signal amplitude. Therefore the selection of R_{FLT} requires a balancing of the stability and distortion of the design.

If the output impedance of the driving amplifier is equal to R_O , its stability can be analyzed by evaluating the effect of R_{FLT} and C_{FLT} on the amplifier open-loop gain (A_{OL}) response as shown in Figure 5. In this figure, the amplifier's closed-loop response for a gain of 1 is denoted as A_{CL} and the unity-gain bandwidth is denoted as f_{CL} .

The combination of R_O , R_{FLT} , and C_{FLT} introduces one pole, f_p and one zero, f_z as shown in the amplifier's open-loop response, for which the corner frequencies are given in Equation 8 and Equation 9 respectively:

$$f_p = \frac{1}{2\pi(R_O + R_{FLT})C_{FLT}} \quad (8)$$

$$f_z = \frac{1}{2\pi R_{FLT} C_{FLT}} \quad (9)$$

In order to ensure that the phase change from the zero negates the phase change that the pole initiates, the frequency distance between the pole and zero must be less than or equal to one decade, as shown in Equation 10.

$$\log\left(\frac{f_z}{f_p}\right) \leq 1 \quad (10)$$

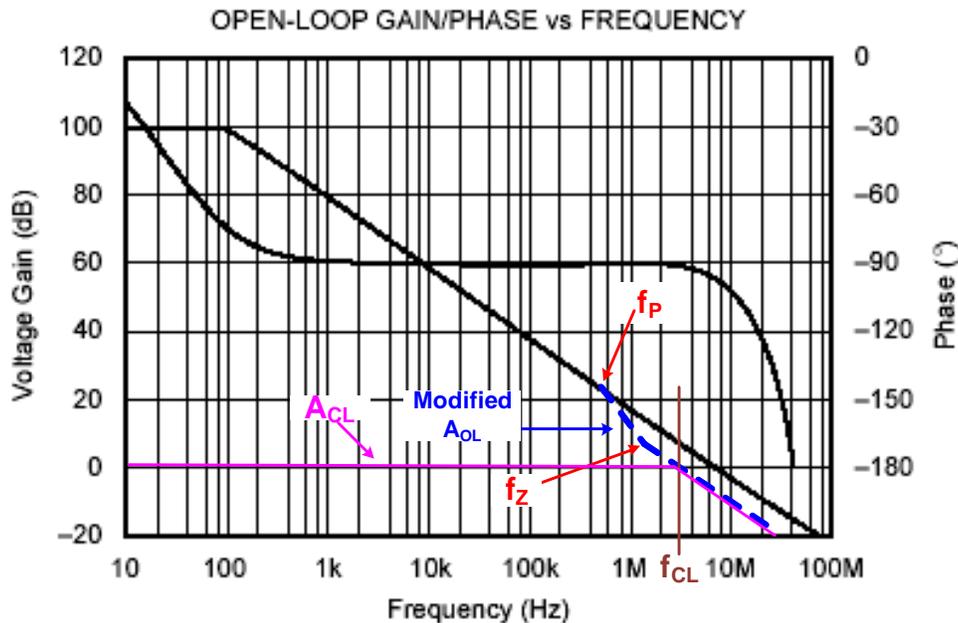


Figure 5. Analyzing Effect of RC-Filter on Op Amp Stability Using A_{OL} Response

In the interest of stability, the effects of f_z must occur at a frequency lower than the closed-loop gain bandwidth of the amplifier (f_{CL}). This requirement is in regard for the stability of the amplifier circuit; the closure rate between the open and closed loop gain curves should not be greater than 20 dB/decade. In order to account for the fabrication process variations associated with the amplifier performance, a good practice is to choose f_z such that the closed-loop gain bandwidth of the amplifier, f_{CL} is at least twice the frequency of the zero, as shown in Equation 11.

$$\frac{f_{CL}}{f_z} \geq 2 \tag{11}$$

Much of this discussion and subsequent results described in Section 3.1.2 and Section 4.1, related to op amp stability are covered in detail in [1].

2.2.2 Input Amplifier Design

Another key aspect in designing the input driver circuit for high-resolution, SAR ADCs is the selection of an appropriate driving amplifier. The amplifier selection process is highly dependent on the input signal and throughput of the ADC. This design is optimized for a full-scale step input signal, so the key amplifier specifications for the selection criteria are as follows:

- **Slew-rate:** The minimum slew-rate for the driving amplifier is dependent on the type and amplitude of the input signal. For a sinusoidal signal with amplitude V_{PK} and frequency f_S , the maximum rate of change of the signal is derived below:

$$\begin{aligned} V_S &= V_{PK} \sin(2\pi f_S t) \\ \Rightarrow \frac{d}{dt}(V_S) &= (2\pi f_S V_{PK}) \cos(2\pi f_S t) \\ \Rightarrow \left\{ \frac{d}{dt}(V_S) \right\}_{MAX} &= 2\pi f_S V_{PK} \end{aligned} \tag{12}$$

Therefore, the minimum required slew rate for the driver amplifier (also specified as *full-power bandwidth* in the data sheet) that prevents any distortion in the signal is shown in Equation 13:

$$\begin{aligned} SR [V/s] &\geq 2\pi f_S V_{PK} \\ \Rightarrow SR [V/\mu s] &\geq 2\pi f_S V_{PK} \times 10^{-6} \end{aligned} \tag{13}$$

- **Small-signal bandwidth:** This bandwidth should be much higher than the bandwidth of the ADC input circuitry to ensure that there is no attenuation of the input signal resulting from the bandwidth limitation of the amplifier. In general, the amplifier should be selected based on [Equation 14](#):

$$\text{Unity - Gain Bandwidth} \geq 4 \times \frac{1}{2\pi R_{\text{FLT}} C_{\text{FLT}}} \quad (14)$$

- **Rail-to-rail input and output voltage swing:** This application uses an input signal with a full-scale voltage swing, therefore an amplifier with support for rail-to-rail input and output (RRIO) swing is required.
- **Open Loop Output impedance** should be as low as possible in order to efficiently drive the switched-capacitor inputs of the SAR ADC as well as to maintain the op amp stability under high capacitive load conditions.
- **Maximum output current drive:** The output peak current drive requirement for the amplifier is dependent on the values of R_{FLT} and C_{FLT} . This is due to the fact that during sampling, the capacitor C_{FLT} charges the internal sampling capacitor (C_{SH}), which causes a voltage drop across C_{FLT} . The recharge current for capacitor C_{FLT} is provided by the output stage of the amplifier, thus imposing a minimum condition on the output drive capability of the amplifier as calculated by [Equation 15](#):

$$I_{\text{OUT}} \geq \frac{\Delta V_{\text{FLT}}}{R_{\text{FLT}}} \quad (15)$$

Using [Equation 4](#) and [Equation 5](#)

$$\Rightarrow I_{\text{OUT}} \geq \frac{C_{\text{SH}} \times V_{\text{REF}}}{C_{\text{FLT}} \times R_{\text{FLT}}} \quad (16)$$

- **Low-power consumption** is a key optimization parameter for this design, so an amplifier must be selected that meets all the requirements of the input driver circuitry for minimum power consumption.

2.3 Reference Driver Design

External voltage reference circuits are used in a data acquisition system if there is no internal reference in the ADC or if the accuracy of the internal reference is not sufficient to meet the performance goals of the system. These circuits provide low-drift and very accurate voltages for ADC reference input. However, the output broadband noise of most references can be in the order of a few $100 \mu\text{V}_{\text{RMS}}$, which degrades the noise and linearity performance of precision ADCs for which the typical noise is in the order of tens of μV_{RMS} . Hence, in order to optimize the ADC performance, the output of the voltage reference must be appropriately filtered and buffered. Advances have also been made in this area, leading to the first available integrated reference and buffer and all-in-one chip with reference and buffer, which is further addressed in [Section 3.2.3](#).

The basic circuit diagram for the reference driver circuit for precision ADCs is shown in [Figure 6](#).

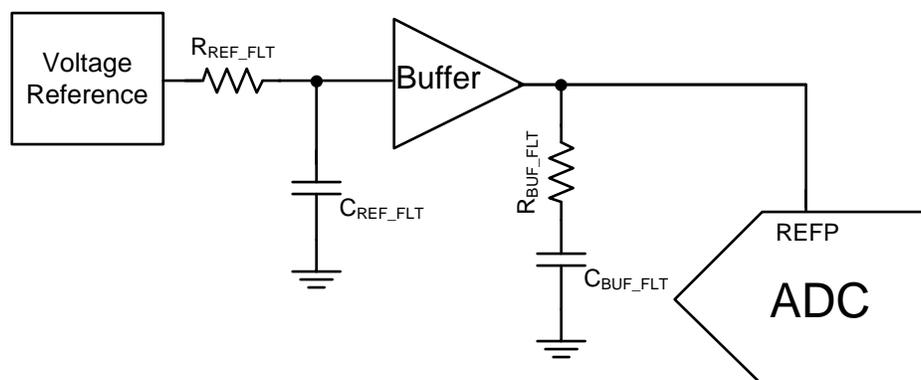


Figure 6. Simplified Schematic of Reference Driver Circuit

The reference noise can be divided into two major categories:

- Low frequency, peak-to-peak flicker or 1/f noise (V_{1/f_REF_PP}) from 0.1-Hz to 10-Hz
- Higher frequency broadband noise, generally specified as a noise spectral density ($e_{n_REF_RMS}$) over a wide range of frequency.

The broadband output noise from the reference circuit is band-limited by the 3-dB cut-off frequency (f_{REF_3dB}) of an RC filter at the output. So, the primary objective for the filter design is to keep the bandwidth low enough such that the intrinsic noise from the reference does not degrade the performance of the ADC. For a high-precision ADC with an input dynamic range of V_{FSR} , the root-mean-square (rms) value of input-referred noise can be calculated from the specified value of SNR in the data sheet by using [Equation 17](#):

$$V_{n_ADC_RMS} = \frac{V_{FSR}}{2\sqrt{2}} \times 10^{-\left(\frac{SNR(dB)}{20}\right)} \quad (17)$$

Hence, the total integrated noise from the reference ($V_{n_REF_RMS}$) should be kept at least one-third of the ADC noise to prevent any degradation in the system performance, as shown in [Equation 18](#):

$$V_{n_REF_RMS} \leq \frac{V_{n_ADC_RMS}}{3} \quad (18)$$

For an RC filter, the effective noise bandwidth is equal to the product of $\pi/2$ and the 3-dB cut-off frequency. The value of total noise contribution from the reference circuit $V_{n_REF_RMS}$, is calculated by the root-sum-square (rss) of the flicker noise and broadband noise, as shown in [Equation 19](#):

$$V_{n_REF_RMS} = \sqrt{\left(\frac{V_{1/f_REF_PP}}{6.6}\right)^2 + e_{n_REF_RMS}^2 \times \frac{\pi}{2} \times f_{REF_3dB}} \quad (19)$$

Substituting [Equation 17](#) and [Equation 19](#) in [Equation 18](#), we get [Equation 20](#):

$$\sqrt{\left(\frac{V_{1/f_REF_PP}}{6.6}\right)^2 + e_{n_REF_RMS}^2 \times \frac{\pi}{2} \times f_{REF_3dB}} \leq \frac{1}{3} \times \frac{V_{FSR}}{2\sqrt{2}} \times 10^{-\left(\frac{SNR(dB)}{20}\right)} \quad (20)$$

The variation in the broadband noise density of the voltage reference ranges from 100 nV/ \sqrt{Hz} to 10000 nV/ \sqrt{Hz} , depending on the reference type and power consumption. In general, the reference noise is inversely proportional to quiescent current (I_{Q_REF}). Because broadband noise density is not always included in the voltage reference data sheet, an approximation of the noise density for band-gap reference circuits is provided in [Equation 21](#)

$$e_{n_REF_RMS} \approx \frac{10000nV}{\sqrt{Hz}} \times \frac{1}{\sqrt{2 \times I_{Q_REF} (in \mu A)}} \quad (21)$$

Equation 21 is derived on the basis of the measured characteristic between the output noise density and quiescent current of several TI reference circuits, as shown in Figure 7.

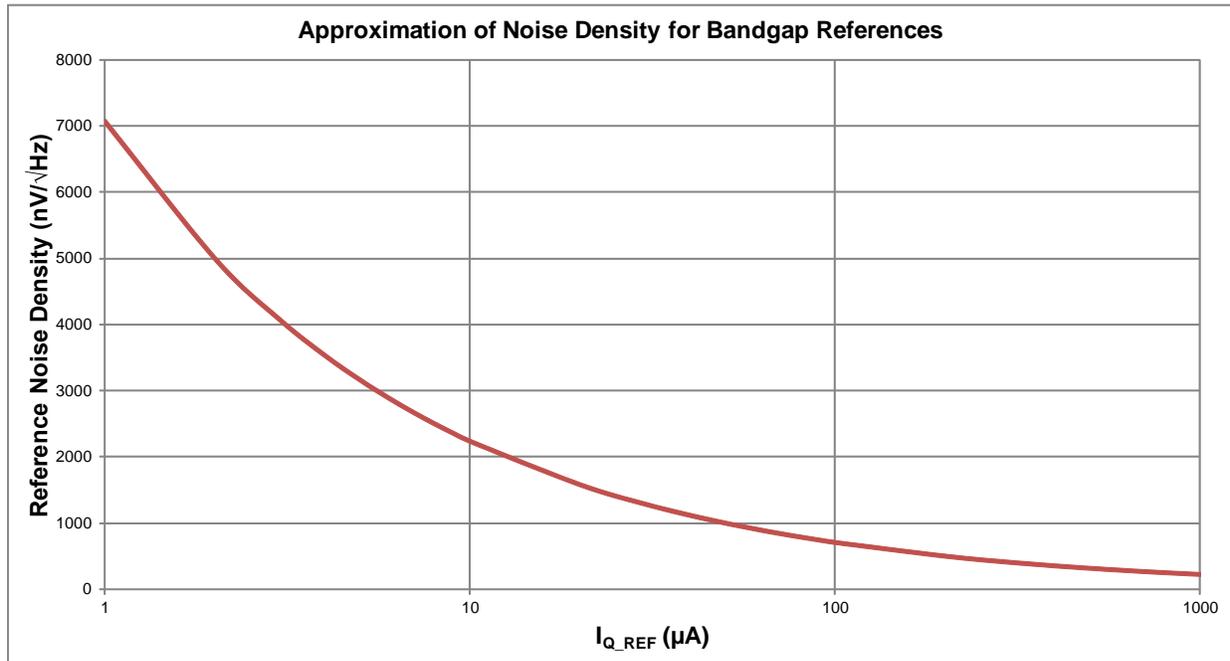


Figure 7. Characteristic Curve: Reference Noise vs Current

Using Equation 20 and Equation 21, the maximum limit for f_{REF_3dB} can be derived as shown in Equation 22:

$$f_{REF_3dB} \leq \frac{2 \times I_{Q_REF} (\mu A)}{(10000 \text{ nV} / \sqrt{Hz})^2} \times \frac{2}{\pi} \times \left[\frac{1}{9} \times \frac{V_{FSR}^2}{8} \times 10^{\frac{-SNR(dB)}{10}} - \left(\frac{V_{1/2_REF_pp}}{6.6} \right)^2 \right] \quad (22)$$

The value of the capacitor for the RC-filter should be kept higher than 100 nF to keep the thermal noise lower than $0.2 \mu V_{RMS}$. Using the selected value for C_{REF_FLT} and f_{REF_3dB} , the value of R_{REF_FLT} can be calculated using Equation 22 as shown in Equation 23:

$$R_{REF_FLT} = \frac{1}{2\pi f_{REF_3dB} \times C_{REF_FLT}} \quad (23)$$

After the noise of the reference block is band-limited, the next important step is to ensure that the reference can drive the dynamic load posed by the ADC reference input. The reference buffer must regulate the voltage such that ΔV_{REF} stays within a 1-LSB error at the start of each conversion. This requirement necessitates the use of a capacitor (C_{BUF_FLT}) at the output of the buffer amplifier to drive the ADC reference pin. The calculations to determine the size of C_{BUF_FLT} are given below:

For an ADC with resolution N, the difference in V_{REF} between two conversions is given by Equation 24:

$$\Delta V_{REF} \leq \frac{V_{REF}}{2^N} \quad (24)$$

Let the total charge consumed during each conversion be Q_{REF} . Due to the configuration of the reference buffer, a big portion of this charge is contributed by the C_{BUF_FLT} capacitor during the fast conversion process and the remaining charge is provided by the buffer amplifier. In general, it is safe to assume that the capacitor provides more than two-thirds of this charge during the fast conversion process. Hence, the minimum value of C_{BUF_FLT} required to regulate the reference voltage is given by Equation 25:

$$C_{BUF_FLT} = \frac{2}{3} \times \frac{Q_{REF}}{\Delta V_{REF}} \geq \frac{2}{3} \times \frac{Q_{REF} \times 2^N}{V_{REF}} \quad (25)$$

The average value of Q_{REF} can be calculated from the maximum ADC conversion time (T_{CONV_MAX}) and the average value of reference input current (I_{REF}) specified in the ADC data sheet as shown in [Equation 26](#):

$$Q_{REF} = I_{REF} \times T_{CONV_MAX} \quad (26)$$

The combination of [Equation 24](#), [Equation 25](#) and [Equation 26](#) yields the expression for the minimum value of C_{BUF_FLT} as derived in [Equation 27](#):

$$C_{BUF_FLT} \geq \frac{2}{3} \times \frac{I_{REF} \times T_{CONV_MAX} \times 2^N}{V_{REF}} \quad (27)$$

The capacitor C_{BUF_FLT} affects the stability of the driving amplifier, therefore it is recommended to use a series resistor, R_{BUF_FLT} to isolate the amplifier output and make it more stable. The value of R_{BUF_FLT} is dependent on the output impedance of the driving amplifier as well as on the signal frequency. Typical values of R_{BUF_FLT} range between 0.1 Ω to 2 Ω and the exact value can be found by using SPICE simulations. It is recommended to use the smallest possible values for R_{BUF_FLT} to avoid any voltage spikes at the reference pin, which can potentially affect the conversion accuracy.

After designing the appropriate passive filter for band-limiting the noise of the reference circuit, the next step is to select an appropriate amplifier for use as a reference buffer. The key specifications to be considered when selecting an appropriate amplifier for the reference buffer are:

- **Open Loop Output impedance** for a reference buffer should be kept as low as possible because the ADC draws current from the reference pin during conversion and the resultant drop in reference voltage is directly proportional to the output impedance of the driving buffer. Impedance also helps keep the amplifier stable while driving a large capacitive load (C_{BUF_FLT}).
- **Input offset:** The initial input offset should be minimized to ensure that the reference voltage driving the ADC is very accurate.
- **Offset drift:** The offset temperature drift of the reference buffer should be as low as possible to make sure that the reference voltage for the ADC does not change significantly over the operating temperature range.

3 Component Selection

This TI Precision Design has been optimized for using TI's high resolution, 18-bit 1MSPS SAR ADC, ADS8881 at its maximum sampling rate, using a full-scale transient step at the differential inputs of the ADC. This section explains the procedure for selecting the various circuit components specific to this design.

3.1 Component Selection for Input Driver Circuit

3.1.1 RC-Filter Passive Components Selection

The critical passive components for this design are the resistor (R_{FLT}) and capacitor (C_{FLT}) for the RC-filter at the input of the ADC. The tolerance of the selected resistor can be chosen as 1% because the use of a differential capacitor at the input balances the effects due to any resistor mismatch. However, special attention needs to be paid in selecting an appropriate capacitor type for this application as it helps to minimize signal distortion at the ADC inputs. The COG (NPO) capacitors are appropriate for this application due to their high Q, low temperature coefficient and stable electrical characteristics under varying voltages, frequency and time.

The values for R_{FLT} and C_{FLT} have been chosen in accordance with the calculations explained in [Section 2.2](#).

$$\frac{1}{R_{FLT} \times C_{FLT}} = \frac{1}{\tau} \geq \frac{\ln\left[\frac{2 \times V_{REF}}{LSB}\right]}{t}$$

According to [Equation 3](#): The LSB size for ADS8881 operating at $V_{REF} = 4.5 \text{ V}$ is given by $LSB = (2 \times 4.5/2^{18}) \text{ V}$. Substituting $t = t_{QT} + t_{ACQ} = 500 \text{ ns}$; we get:

$$\frac{1}{R_{FLT} \times C_{FLT}} \geq \frac{\ln\left[\frac{2 \times 4.5 \times 2^{18}}{2 \times 4.5}\right]}{500 \times 10^{-9}} \quad (28)$$

$$\Rightarrow R_{FLT} \times C_{FLT} \leq 40.07 \times 10^{-9} \quad (29)$$

The specified value of the input capacitance for ADS8881 is 59 pF , so according to [Equation 7](#):

$$\begin{aligned} C_{FLT} &\geq 20 \times C_{SH} \\ \Rightarrow C_{FLT} &\geq 1.18 \text{ nF} \end{aligned} \quad (30)$$

The selected value of capacitance for each input of the ADC is equal to **2 nF** if the filter is designed in a common-mode configuration as shown in [Figure 8](#). However, this design uses a differential configuration for the RC-filter, so a **1 nF** capacitor is connected across the differential inputs of the ADC.

Based on the selected value of C_{FLT} , the maximum value of R_{FLT} can be calculated using [Equation 29](#):

$$R_{FLT} \leq \frac{40.07 \times 10^{-9}}{2 \times 10^{-9}} \approx 20 \Omega \quad (31)$$

The value of the resistor R_{FLT} for each differential input of the ADC has been selected as **10 Ω** for optimum system performance. The two possible configurations for the design of the anti-aliasing RC-filter are shown in [Figure 8](#).

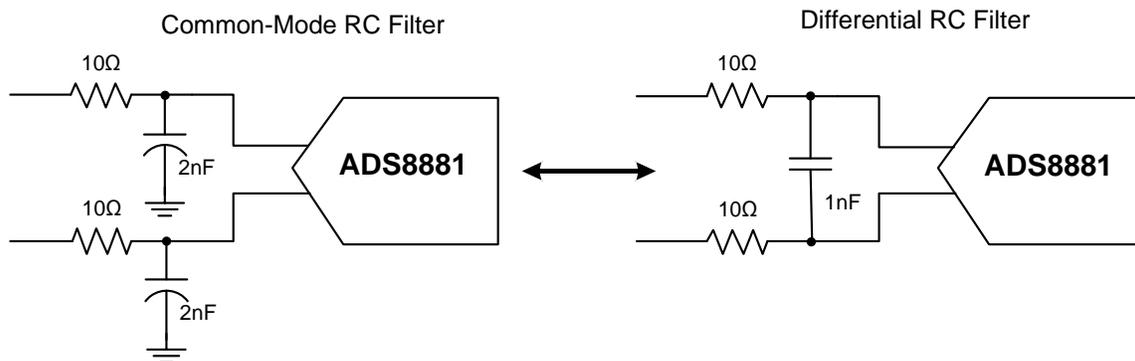


Figure 8. Design Configurations for Anti-aliasing RC-filter at ADC Input

3.1.2 Amplifier Selection

The key amplifier specifications to be considered in order to meet the performance goals for this application are **rail-to-rail input swing**, **high slew rate** and **fast settling time**.

Based on the values of R_{FLT} and C_{FLT} , some of the key specifications for the driving amplifier can be derived as follows:

- **Slew Rate:** The minimum slew-rate of the driving amplifier for this application depends on the time allowed for the slewing of the amplifier's output stage when a full-scale step is applied at input. As explained in [Figure 3](#), the output stage of the amplifier slews during the quiet-time for which the minimum specified value is $t_{QT} = 210$ ns. Hence, the minimum required slew-rate for the amplifier is:

$$SR \geq \frac{V_{REF}}{t_{QT}}$$

$$\Rightarrow SR \geq 21.43 \text{ V}/\mu\text{s} \quad (32)$$

- **Small-Signal Bandwidth:** Using the selected values of C_{FLT} and R_{FLT} , the minimum value of the unity gain bandwidth for the amplifier can be calculated using [Equation 14](#) as:

$$\text{Unity - Gain Bandwidth} \geq 4 \times \frac{1}{2\pi R_{FLT} C_{FLT}} = 31.85 \text{ MHz} \quad (33)$$

- **Output Current Drive:** Using the selected values of C_{FLT} , R_{FLT} and C_{SH} , the output current drive capability of the driving amplifier is calculated using [Equation 16](#) as:

$$I_{OUT} \geq \frac{C_{SH} \times V_{REF}}{C_{FLT} \times R_{FLT}}$$

$$\Rightarrow I_{OUT} \geq \frac{59 \times 10^{-12} \times 4.5}{2 \times 10^{-9} \times 10} = 13.275 \text{ mA} \quad (34)$$

The OPA350 CMOS amplifier is a high precision, low noise and fast settling amplifier optimized for low voltage, single-supply operation with rail-to-rail input and output. In this application, the input signal is a transient step of full-scale ADC input range, which utilizes the rail-to-rail input swing of this amplifier, operating from a single 5 V supply. The high slew rate and low settling time of the amplifier helps to drive the ADC input to required accuracy within the acquisition time window for a sampling speed of 1 MSPS.

The comparison in [Table 2](#) verifies that the OPA350 meets all the requirements to meet the performance of this system based on the calculations explained earlier.

Table 2. Calculated Specifications of Input Driving Amplifier vs. OPA350 Specifications

SPECIFICATION	CALCULATED VALUE	OPA350 SPECIFICATION
Unity Gain Bandwidth	31.85 MHz (Min.)	38 MHz
Slew-Rate	21.43 V/ μ s (Min.)	22 V/ μ s
Output Current Drive	26.55 mA (Min.)	40 mA
Input and Output Swing	Rail-to-rail	Rail-to-rail
Power	As low as possible	37.5 mW @ VDD = 5V (Max.)

After selecting the various design components, it is critical to check the stability of the driving amplifier, using the analysis explained in [Section 2.2](#).

The output impedance of OPA350 is dependent on the frequency of operation. Using the TINA-TI™ Spice simulation models, the value of output impedance (R_o) has been simulated as $50\ \Omega$ at the frequencies of interest. The simulation schematic and results are displayed in [Figure 9](#) and [Figure 10](#) respectively:

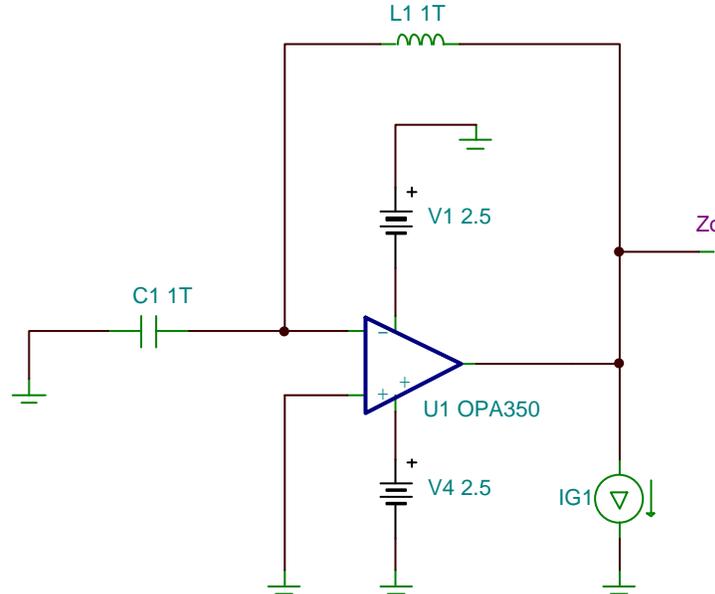


Figure 9. TINA-TI™ Schematic: Measuring Output Impedance of OPA350

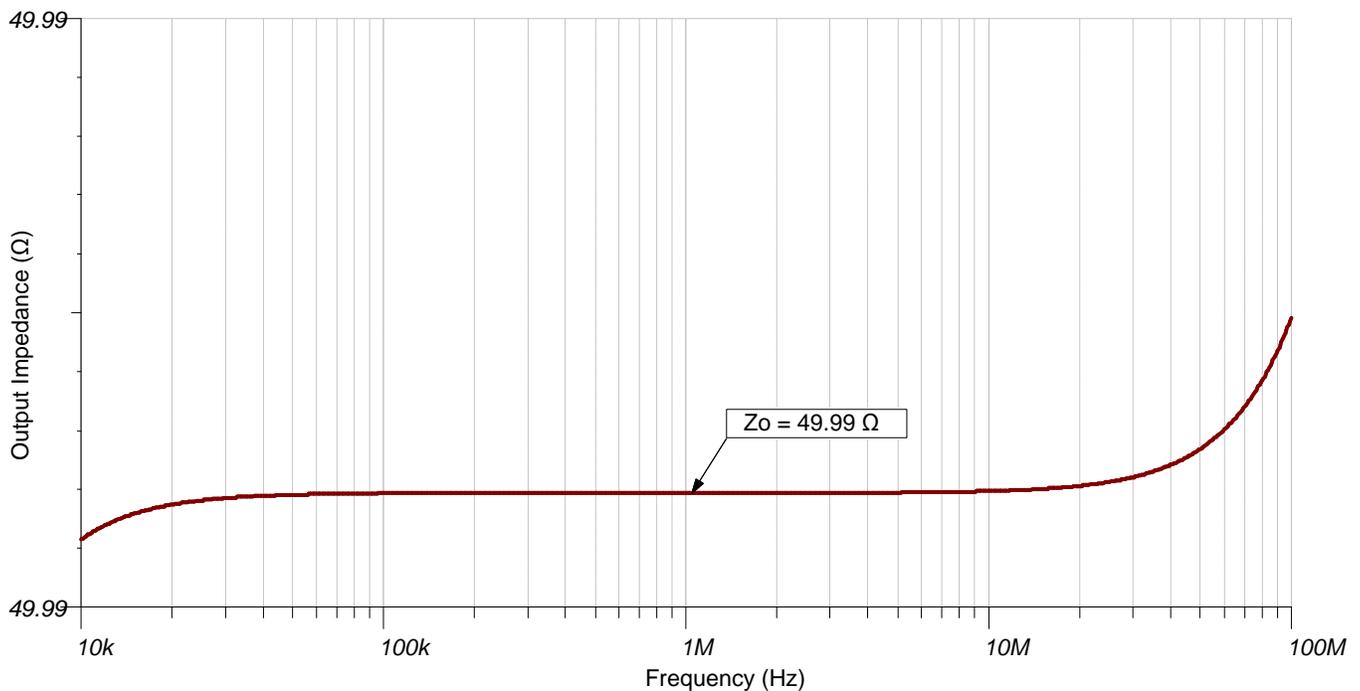


Figure 10. TINA-TI™ Simulation Result: Output Impedance of OPA350

Using Equation 8 and Equation 9, the frequencies of the pole and zero can be calculated respectively, by utilizing the values of R_O , R_{FLT} and C_{FLT} .

$$f_p = \frac{1}{2\pi(R_O + R_{FLT})C_{FLT}} = 1.33\text{MHz} \quad (35)$$

$$f_z = \frac{1}{2\pi R_{FLT} C_{FLT}} = 7.96\text{MHz} \quad (36)$$

The pole and zero are separated by less than a decade in frequency, which satisfies the amplifier stability criteria explained in Equation 10.

In this application, the amplifier is used in a unity-gain configuration, so the closed loop frequency, f_{CL} is 38 MHz, which is more than double the frequency of the zero caused by the RC-filter. This satisfies the amplifier stability criteria explained in Equation 11.

3.2 Component Selection for Reference Driver Circuit

3.2.1 Passive Components Selection

The external reference used to drive the ADS8881 in this design is the REF5045 from TI. This reference has been selected because it provides the highest possible reference voltage of 4.5 V in a system with only a 5 V supply. As mentioned in the datasheet of REF5045, it requires a capacitance of 10 μF at the V_{OUT} pin for stability purposes. A series resistor of 0.2 Ω is used with the 10 μF capacitor for smooth power-up of the reference.

According to the discussion in Section 2.3, the noise from the reference should be bandwidth limited by designing a low-pass RC filter at the reference output. According to Equation 22, the maximum value of the 3-dB bandwidth for this filter can be calculated as:

$$f_{REF_3dB} \leq \frac{2 \times I_{Q_REF}(\mu\text{A})}{(10000 \text{ nV} / \sqrt{\text{Hz}})^2} \times \frac{2}{\pi} \times \left[\frac{1}{9} \times \frac{V_{FSR}^2}{8} \times 10^{-\frac{SNR(\text{dB})}{10}} - \left(\frac{V_{1/f_REF_pp}}{6.6} \right)^2 \right]$$

$$\Rightarrow f_{REF_3dB} \leq 1.75 \text{ kHz} \quad (37)$$

The value of capacitor C_{REF_FLT} has been selected as 1 μF to keep the thermal noise of the capacitor at a low value. The next higher value for a standard capacitor is 10 μF . These capacitors are very bulky and expensive due to which they are generally avoided in a design unless absolutely necessary. The minimum value of R_{REF_FLT} can be calculated using Equation 23 as:

$$R_{REF_FLT} \geq \frac{1}{2\pi \times 1.75 \times 10^3 \times 10^{-6}} = 91 \Omega \quad (38)$$

The value of R_{REF_FLT} has been selected as 1 $\text{k}\Omega$ for this design. The selected value for the resistor is much higher than the calculated minimum value to further reduce the bandwidth of the filter so that the broadband noise contribution from the reference is negligible.

The next important passive element in reference design is the capacitor C_{BUF_FLT} , which helps to regulate the voltage at the ADC reference pin under dynamic load conditions. According to ADS8881 datasheet, the average current drawn into the reference pin (I_{REF}) is 350 μA and for a maximum throughput of 1 MSPS, T_{CONV_MAX} is equal to 710 ns. Hence, according to Equation 27, the value of C_{BUF_FLT} can be calculated as:

$$C_{BUF_FLT} \geq \frac{2 \times 350 \times 10^{-6} \times 710 \times 10^{-9} \times 2^{18}}{3 \times 4.5} = 9.65 \mu\text{F} \quad (39)$$

The value of C_{BUF_FLT} has been selected as 10 μF for this design.

3.2.2 Amplifier Selection

As explained in [Section 2.3](#), the key amplifier specifications to be considered to design a reference buffer for a high-precision ADC are **low offset, low drift, wide bandwidth and low output impedance**. While it is possible to select an amplifier that meets all these requirements, it may come at a cost of excessive power consumption. For example, the OPA350 is a 38 MHz amplifier with an offset of 0.5 mV and low offset drift of 4 $\mu\text{V}/^\circ\text{C}$, but it consumes a quiescent current of 5.2 mA, which is extremely high for this design. This is because offset and drift are dc specifications while bandwidth, output impedance and high capacitive drive capability are ac specifications. Thus, achieving all the performance in one amplifier requires power. A more efficient way to minimize power is to use a composite reference buffer. It utilizes an amplifier with superior high frequency specifications in the feedback loop of a dc precision amplifier to get the best of both worlds at much lower power.

In this design, the reference buffer is designed using two amplifiers, THS4281 and OPA333, in a composite double feedback architecture as shown in [Figure 11](#).

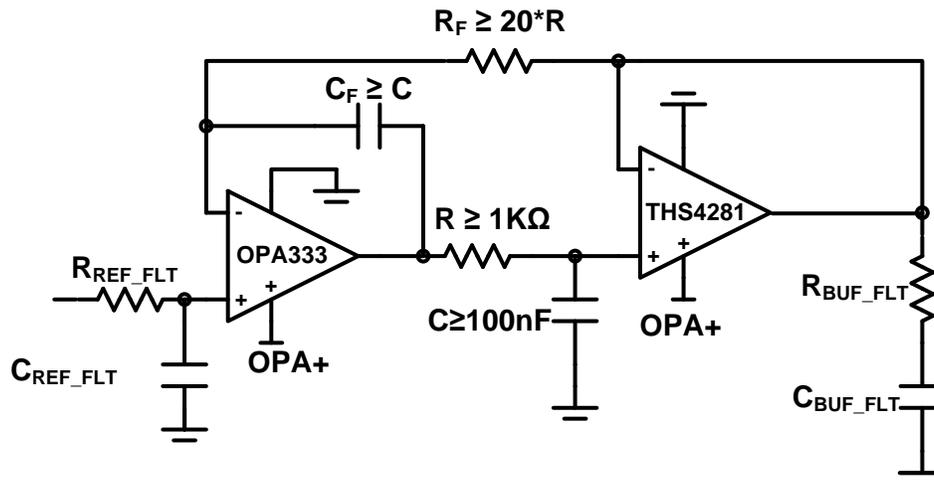


Figure 11. Schematic of Reference Buffer Circuit

The THS4281 has a wide 3-dB bandwidth of 90 MHz at a gain of 1 and output impedance of 1 Ω for 1 MHz operation, with a maximum quiescent current of only 1 mA. This makes it ideal for driving the high capacitor C_{BUF_FLT} and regulating the voltage at the ADC reference input. However, the THS4281 suffers from poor offset (2.5 mV max.) and drift (7 $\mu\text{V}/^\circ\text{C}$ max.) specifications. In order to improve the dc specifications of the reference buffer, the OPA333 is used as a dc correcting amplifier. The OPA333 is a zero-drift (0.05 $\mu\text{V}/^\circ\text{C}$ max.) and low offset (10 μV max.) amplifier with a maximum quiescent current of only 25 μA . Thus, for a much better performance related to reference accuracy and load-regulation, this two amplifier approach consumes only 20% of power compared to a single amplifier buffer.

In this reference buffer design, the noise specifications of the dc amplifier (OPA333) are not very important because it gets heavily filtered by the low frequency RC-filter at its output. The value of C is chosen to be greater than 100 nF to keep the capacitor thermal noise to be less than 0.2 μV_{RMS} and the value of R is selected greater than 1 k Ω to avoid any stability issues due to high capacitive loading.

This amplifier uses a dual feedback in the design, out of which one feedback is active during dc operation and the other feedback is active during higher frequency ac operation. The active feedback during dc operation, as shown in Figure 12 displays the dc model of the circuit, where R_F appears as a short because there is no current flowing in that branch, and C_F appears as an open circuit. This feedback connects the output of THS4281 directly to the inputs of OPA333, which then corrects for its offset and drift. The value of R_F should be at least 20 times greater than R to avoid any stability issues.

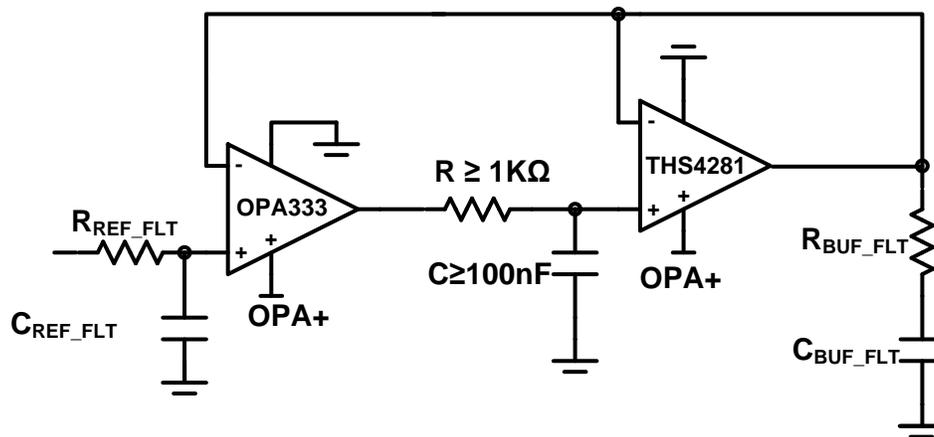


Figure 12. DC Equivalent Schematic of Reference Buffer

The active feedback connection during higher frequency operation is shown in Figure 13. At such frequencies of operation, R_F acts as open connection; C_F acts as a short and the two amplifiers are connected as isolated unity-gain buffers. The value of C_F should be equal to or greater than C to avoid any stability issues.

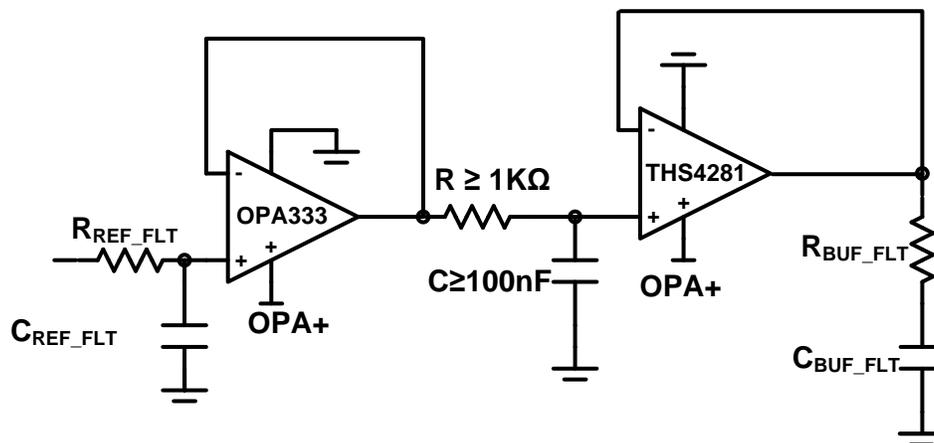


Figure 13. High Frequency Equivalent Schematic of Reference Buffer Circuit

3.2.3 Integrated Reference and Buffer

With new and increased integration among available components, another option to drive the reference on the ADC is an integrated reference and buffer. This option replaces the entire reference driver circuit with one main component, which avoids the long design process of choosing the correct amplifier for the best performance. Even when an amplifier does meet the necessary specifications for a design, such as wide bandwidth, low output impedance, low offset, and low drift, the power consumption still must be considered as well as design time. The REF60xx family is a high-performance line of reference drivers that TI offers, which is the industry's first integrated low-output impedance buffer. Each reference driver is trimmed during production to achieve a max drift of only 5 ppm/°C for both the reference and integrated buffer combined. The device also consumes a low 820- μ A quiescent current, while still being able to replenish a charge of 70 pC on a 47- μ F capacitor in 1 μ s. This integrated device decreases design time by eliminating the requirement of implementing the entire reference driver circuit.

The REF6045 is specifically the ideal choice for this design, with an output of 4.5 V, and simplifies the reference circuitry as shown in Figure 14.

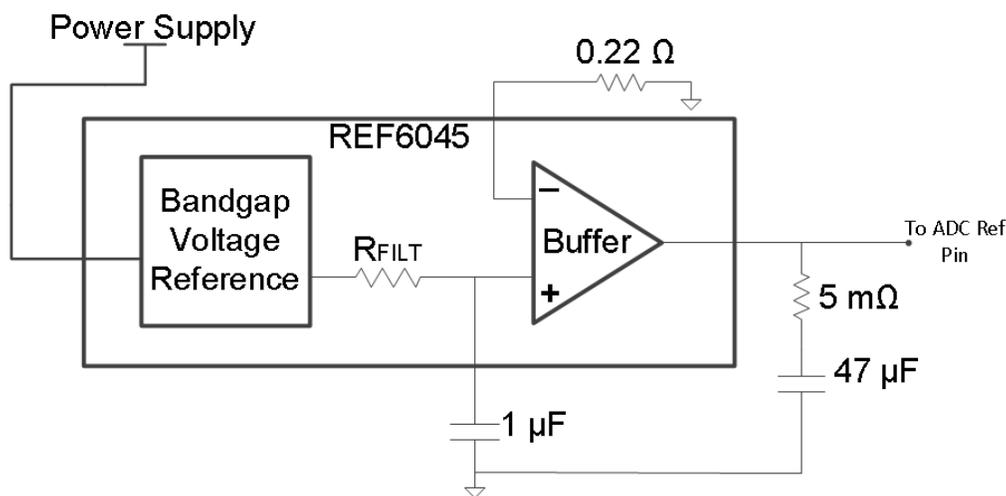


Figure 14. REF6045 Voltage Reference with Integrated Buffer

4 Simulation

The TINA-TI™ schematic shown in Figure 15 includes the final design and circuit component values obtained in the design process.

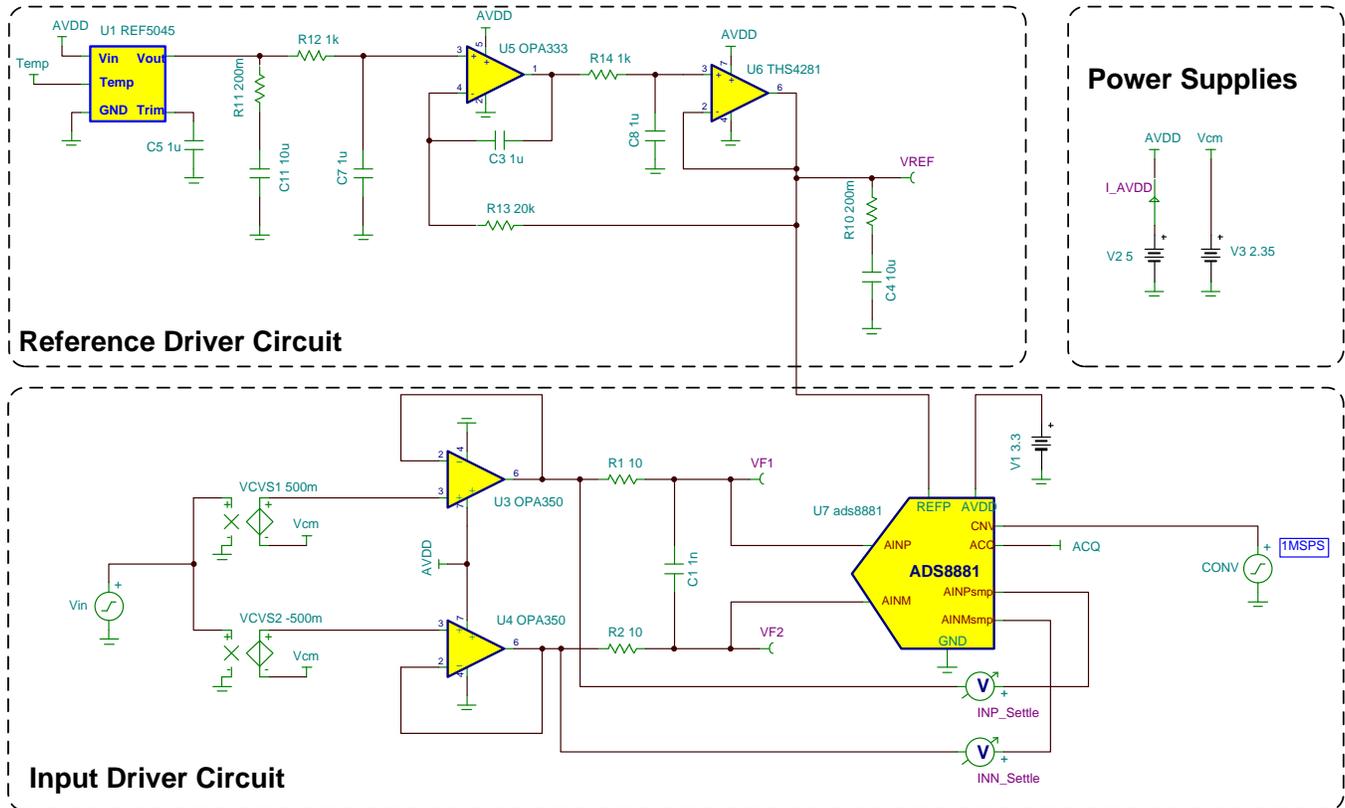


Figure 15. TINA-TI™ Schematic - Complete Data Acquisition Block

The TINA-TI™ SPICE Model for ADS8881 is used to evaluate the performance of the entire signal chain. The SPICE model for the ADC accurately models the input sample-and-hold circuit of the ADC, which is important in designing for an appropriate front-end input driver circuit. It also includes the dynamic loading of the REFP input pin. This is helpful in optimizing the design of the external reference driver circuit. The ADC model outputs two signals called as "AINPsm" and "AINMsm", which represent the output of the internal sample-and-hold stage of the ADC. During sampling these two signals track the corresponding input signals and during conversion these signals are held at a value of the input signal which is getting converted by the ADC.

This circuit above is simulated to check the 18-bit settling of the full-scale step at the inputs of the ADC before start of each conversion; and accurate settling of reference input voltage for each conversion. The simulation details and results are provided in the subsequent sections.

4.1 Stability of Input Driver Amplifiers

The TINA-TI™ schematic shown in Figure 16 is used to check the stability of the amplifiers driving the ADC inputs. Despite paying careful attention to the input amplifier stability during the selection of design components, it is an important first step to check the amplifier stability in simulations. If the input amplifiers are unstable or marginally stable, then the selection of components should be revisited to make the design more robust from stability perspective.

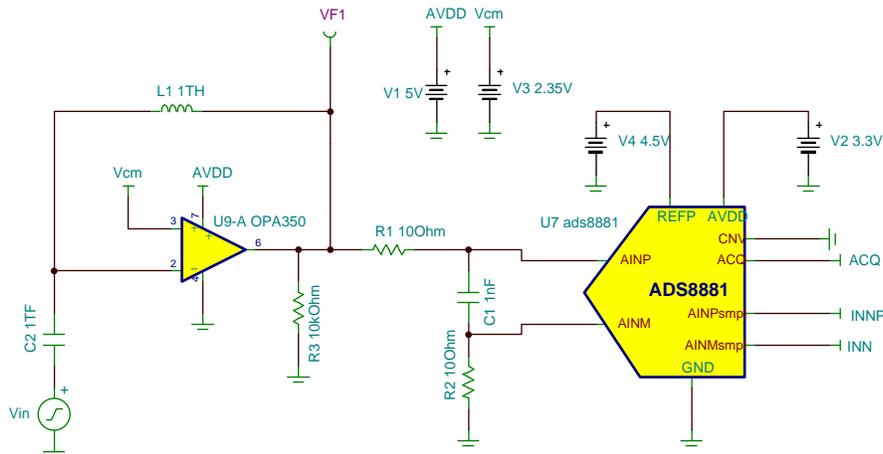


Figure 16. TINA-TI™ Schematic - Checking Input Amplifier Stability

This circuit simulates the loop gain of the input driver to determine the phase margin and hence the stability of the amplifier. A large inductor of value 1 TH is connected in the feedback loop of the amplifier, so it behaves like an open-loop configuration at frequencies higher than dc. The circuit has been simplified by considering only half-circuit of the differential input structure. In order to load the amplifier output appropriately, the ADC is connected with “CNV” pin tie to GND so that it is always sampling the input.

The ac magnitude and phase response for the loop-gain of this circuit is shown in Figure 17. The resulting **phase margin of 62.96°** at the 0-dB cross-over frequency of 29.97 MHz validates the stability of the input drivers for this design.

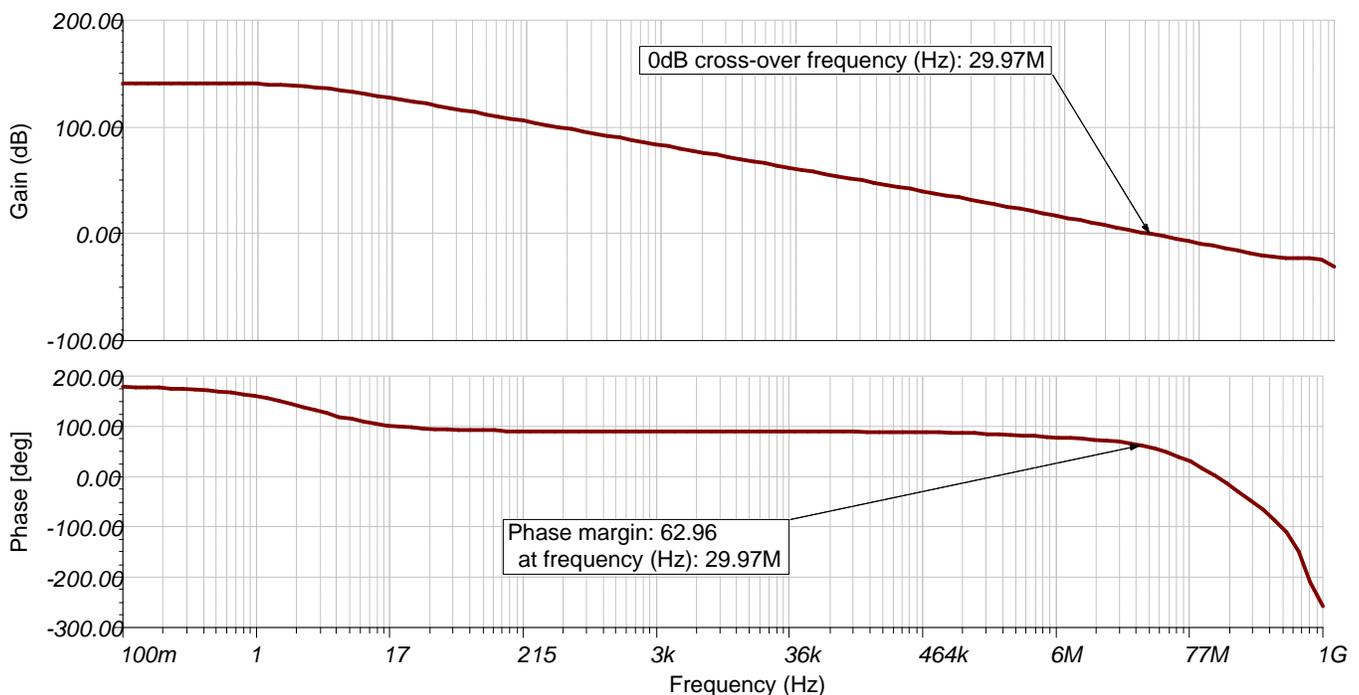


Figure 17. TINA-TI™ Simulation Result - Loop Gain Magnitude and Phase Plot for Input Driver Stability

4.2 Settling Response of ADC Input Signals

The TINA-TI™ schematic shown in Figure 15 is used to check the 18-bit settling of the full-scale step signal at the inputs of the ADC during sampling phase. The simulated transient step response for the circuit is shown in Figure 18.

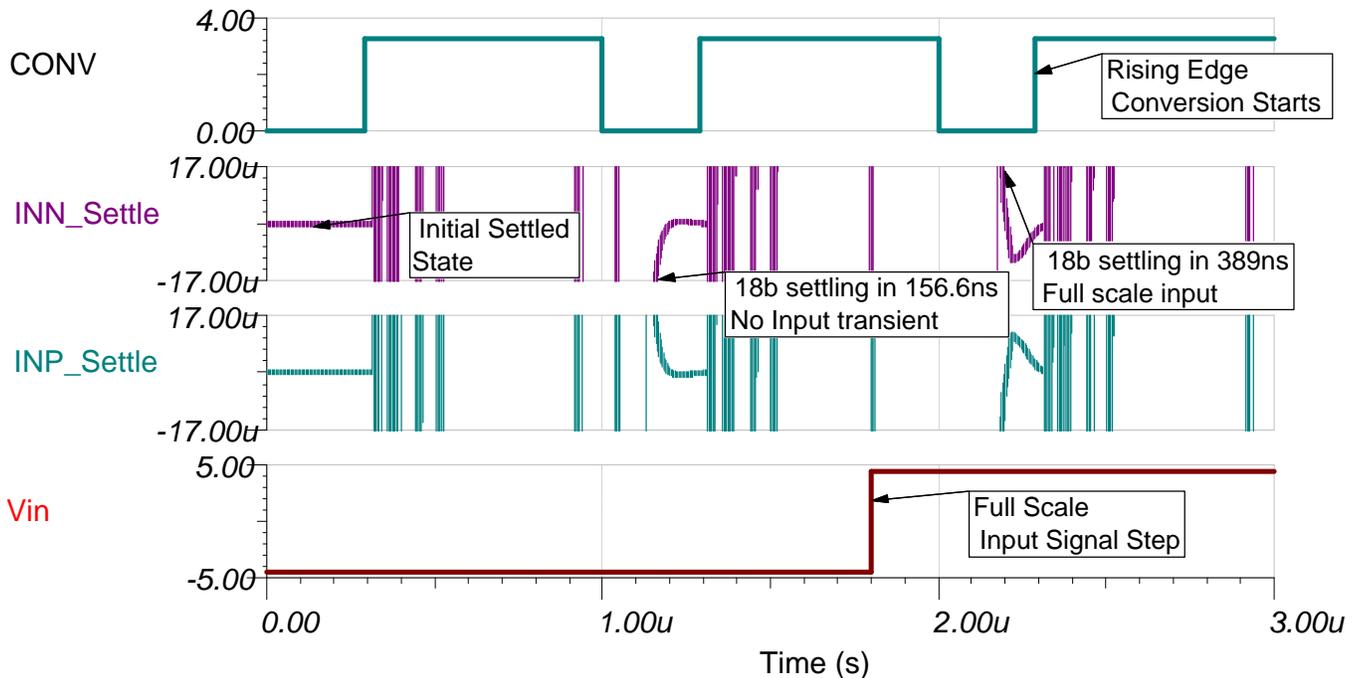


Figure 18. TINA-TI™ Simulation Result - ADC Input Settling

For an 18-bit ADC using $V_{REF} = 4.5\text{ V}$, the LSB is equal to $17\text{ }\mu\text{V}$. As explained in Section 2.1, in order to optimize this design the input step can appear anytime between the start of conversion until half the ADC cycle time, which is 500 ns for 1 MSPS throughput. In this simulation, to check the worst case settling behavior for the ADC input driver a transient step is applied 500 ns before the start of conversion while the previous conversion is ongoing. As shown in Figure 18, both the inputs of the ADC **settle within 1 LSB, 18-bit accuracy in 389 ns**, before the next conversion starts. This result validates that in this design, the ADC inputs settle accurately at the beginning of each conversion.

4.3 Settling Response of ADC Reference Input

The TINA-TI™ schematic shown in Figure 15 is used to check the settling of the reference buffer output, driving the REFP pin of the ADC. As explained in Section 2.3, the voltage at the reference pin should settle to less than the LSB of the ADC for maintaining the overall system performance. The size of LSB for the ADS8881 using $V_{REF} = 4.5\text{ V}$ is equal to $34.3\text{ }\mu\text{V}$. According to the transient simulation plot shown in Figure 19, the voltage error at the REFP pin between two successive conversions is equal to $\Delta V_{REF} = 30.4\text{ }\mu\text{V}$, which is less than the size of the LSB. This validates that the reference voltage has settled to sufficient accuracy that is required to maintain the performance of this design.

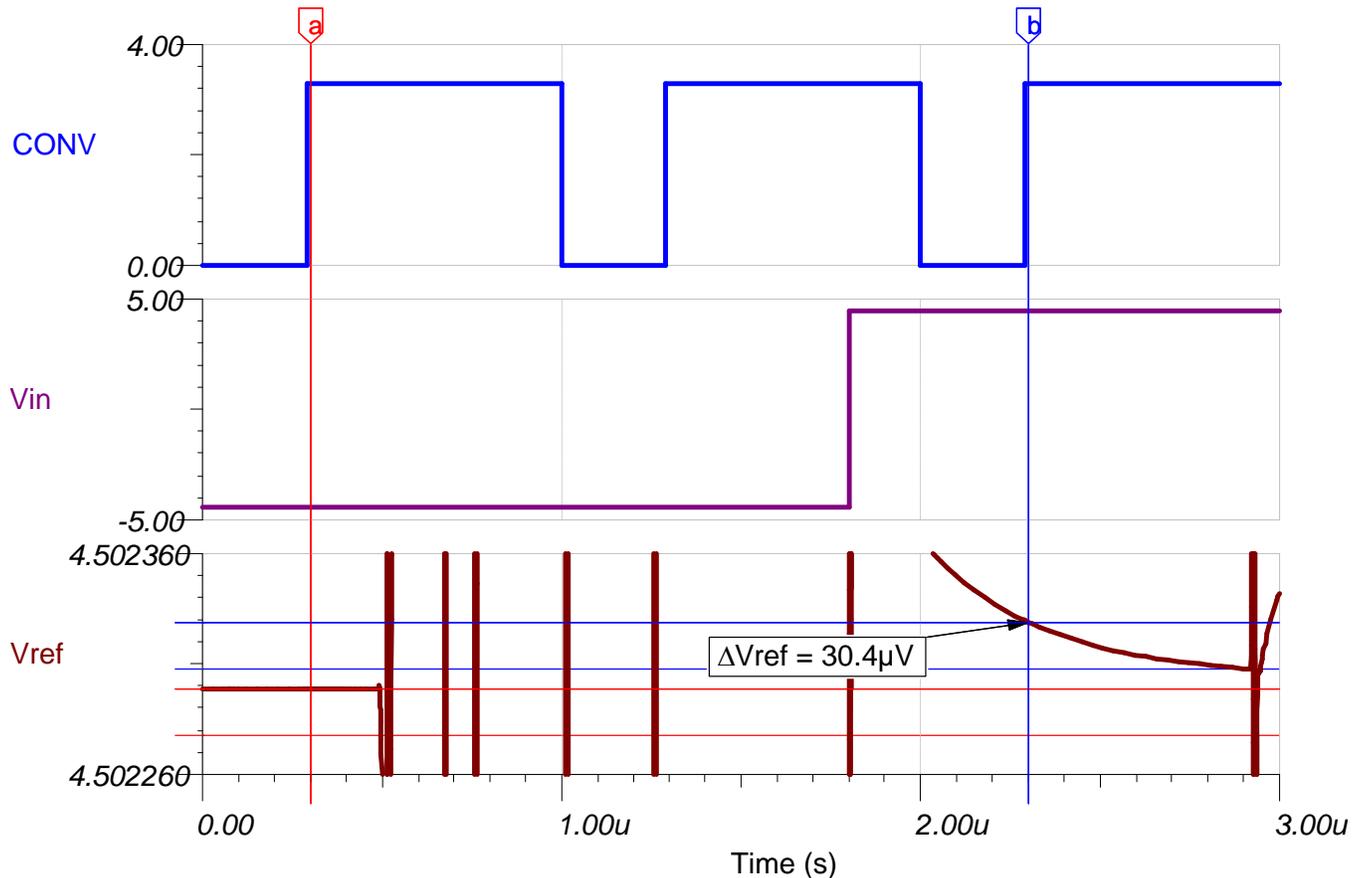


Figure 19. TINA-TI™ Simulation Result - ADC Reference Settling

5 PCB Design

The PCB schematic and Bill of Materials can be found in [Section 10.1](#).

5.1 PCB Layout

The most important considerations in designing the PCB layout for this DAQ block are discussed below:

- The length of traces from the reference buffer circuit (REF5045, THS4281 and OPA333) to the REFP input pin of the ADC should be kept as small as possible to minimize the trace inductance that can lead to instability and potential issues with the accurate settling of the reference voltage.
- The input driver circuit, comprised of OPA350 buffers should be located as close as possible to the inputs of the ADC to minimize loop area, thus making the layout more robust for EMI/RFI rejection. Similarly, the resistors and capacitor of the anti-aliasing filter at the inputs of the ADC should be kept close together and close to the inputs of the ADC to minimize the loop area.
- The traces feeding the differential input voltage from the source up to the differential inputs of the ADC should be kept symmetrical without any sharp turns.

The complete PCB layout for this design is shown in [Figure 20](#).

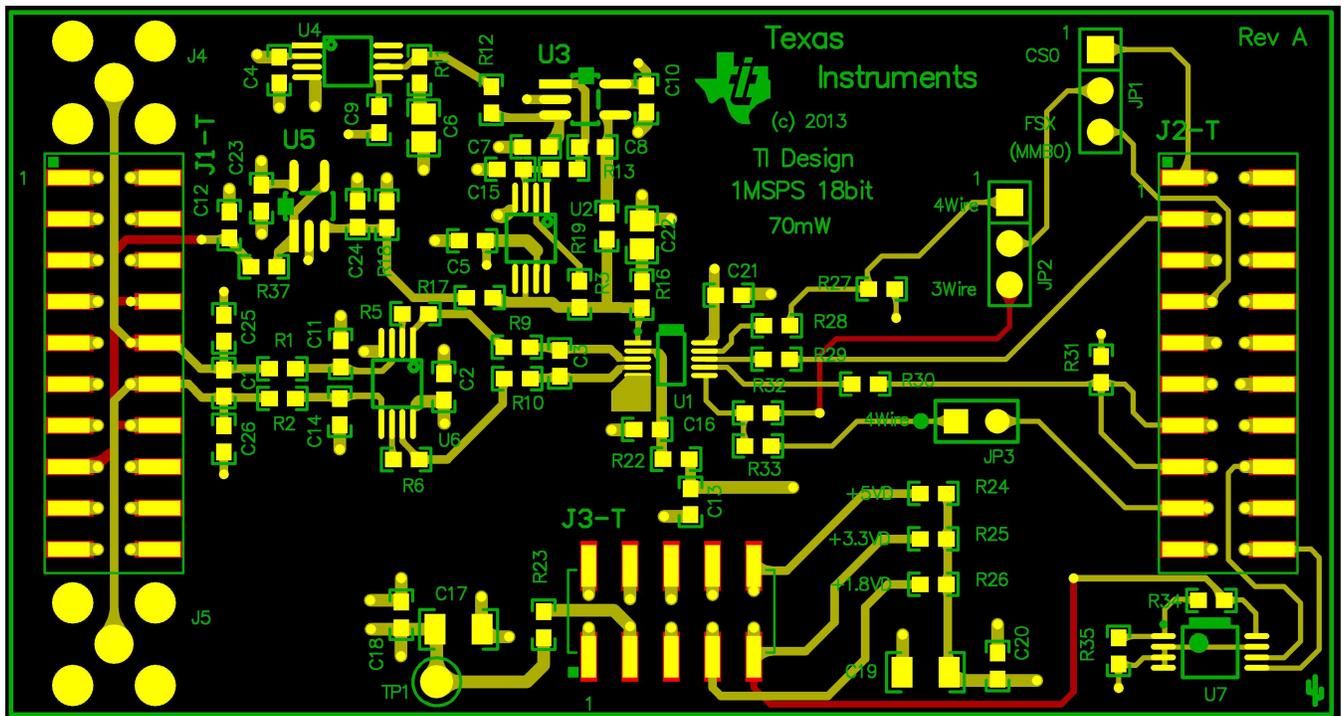


Figure 20. PCB Layout

6 Verification and Measured Performance

The measurement results for verification of this TI Precision Design are listed in this section.

6.1 DC Noise Measurement

All ADC circuits suffer from some amount of inherent broadband noise contributed by the internal resistors, capacitors and other circuitry, which is referred to the inputs of the ADC. The front-end driver circuit also contributes some noise to the system, which can also be referred to the ADC inputs. The cumulative noise, often called as the *input-referred noise* of the ADC has a significant impact on the overall system performance. The most common way to characterize this noise is by using a constant dc voltage as the input signal and collecting a large number of ADC output codes. A histogram can then be plotted to show the distribution of output codes, which can be used to illustrate the impact of noise on the overall system performance. In this design, the dc noise for the system is measured by shorting the inputs of both input amplifiers to a common mode voltage, $V_{CM} = \frac{1}{2} \times V_{REF} = 2.25 \text{ V}$, such that the differential voltage at the inputs of the ADC is equal to $V_{DIFF} = 0 \text{ V}$. The resulting histogram of output codes is shown in [Figure 21](#).

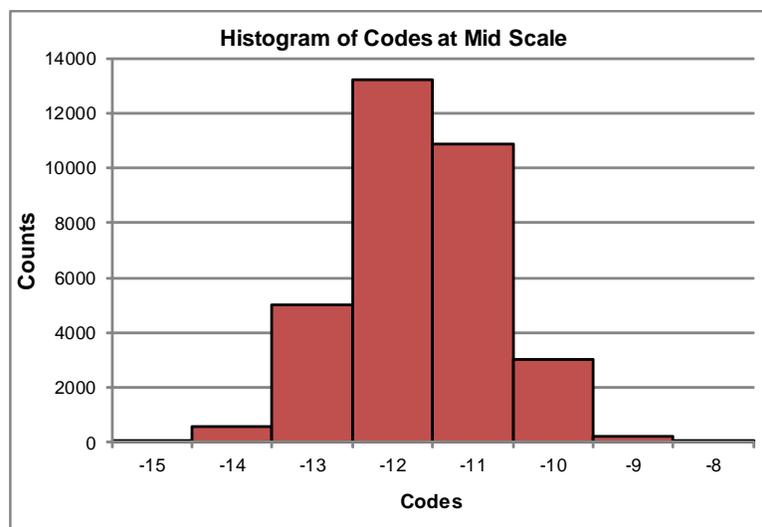


Figure 21. Measurement Data - Histogram Showing DC Noise (Mid Scale)

The distribution of output codes looks like a Gaussian distribution which indicates a properly designed system. However, if the output code distribution has large peaks and valleys which make it distinctly non-Gaussian, then it indicates significant DNL errors in the ADC or issues with the system design like insufficient power supply decoupling, improper ground connections and/or other poor PCB layout effects. For a theoretically perfect ADC system, the histogram of output codes will be a single vertical bar since the ADC output will always be the same for a dc input voltage. However, the noise contributions from the ADC and the front-end circuit leads to a distribution of output codes, which provides a measure of the overall system's dc noise. The measured values of peak-to-peak difference between the codes (N_{pp}) and the standard deviation of codes (N_{σ}) are listed in [Table 3](#).

The **Noise-Free Resolution** of an ADC is defined as the number of steady output bits from the converter beyond which it is not possible to differentiate between individual code transitions. This is an extremely conservative measurement of the ADC's performance because the formula for noise-free resolution is derived from the peak-to-peak code noise, which is dependent on the total number of samples.

A more reliable approach is to use the standard deviation of output codes (N_{σ}) in calculating the **Effective Resolution** of the ADC. Please note that the results shown in [Table 3](#) do not assume a Gaussian based formula in calculating the standard deviation from the peak-to-peak value because the overall dc noise is comparable to the size of the LSB. For an 18-bit ADC used in this design, the measured value of effective resolution is also equal to 18 bits, which indicates that there is no degradation in the converter's performance due to the effects of dc noise.

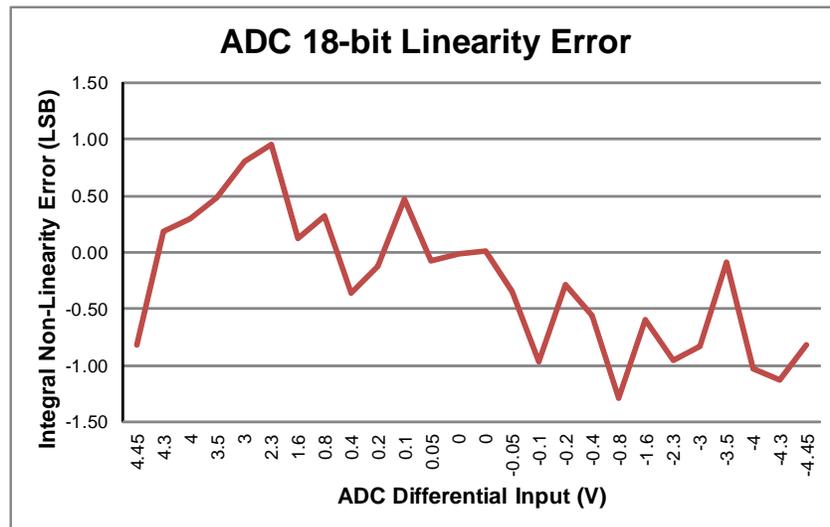
Please note that the *Effective Resolution* and *Effective Number of Bits (ENOB)* shown in [Section 6.5](#) should not be confused with each other as they are two completely different entities. The ENOB for an ADC is measured with an ac sinusoidal input signal and includes the effects due to quantization noise and distortion terms, which have no impact on a dc measurement.

Table 3. Measurement Results for DC Noise

Parameter	Formula	Measured Value
Mean Output Code	NA	-11.66
Peak-to-Peak Code Noise (N_{PP})	Max. Output Code - Min. Output Code + 1	8
Standard Deviation of Codes (N_{σ})	NA	0.94
Noise-Free Bits	$\log_2 \left(\frac{2^{18}}{N_{PP}} \right)$	15
Effective Resolution	$\log_2 \left(\frac{2^{18}}{N_{\sigma}} \right)$	18

6.2 ADC Linearity Measurement

The linearity of the system was measured by sweeping the differential input voltage from -4.45 V to 4.45 V in 26 voltage steps and the integral non-linearity (INL) error is plotted after cancelling the offset and gain errors from the response. This 26-point INL plot is shown in [Figure 22](#). As highlighted in [Table 4](#), this design meets all the performance specifications of the ADC in terms of offset, gain and linearity.


Figure 22. Measurement Data - ADC INL Plot (26-points)
Table 4. Measurement Results for Linearity Test

Parameter	ADC Datasheet Specification	Measured Value
Offset Error (mV)	±4mV (Max.)	-0.299
Gain Error (% FSR)	±0.03 % (Max.)	-0.0014
INL _{MIN} (LSB)	-3	-1.28
INL _{MAX} (LSB)	3	0.95

6.3 Transient Settling for Rising Input Step

In order to measure the settling behavior of the front-end circuit for an 18-bit ADC, the input voltage is changed from negative full-scale (NFS) to positive full-scale (PFS). Since there is no easy way to measure the 18-bit settling of the ADC input, this behavior is validated by looking at the output of the ADC. If the ADC output stays within 1 LSB error, this would imply that the input signal has accurately settled before each conversion.

The response in Figure 23 shows the ADC output behavior for a full-scale rising step signal at the input. The zoomed-in views of the ADC output response near PFS and NFS are shown in the plots on the right. This response has been analyzed at 4 instants of time specified as t_0 , t_1 , t_2 and t_3 . At time t_0 , the differential input of the ADC is completely settled at NFS. The full-scale step appears at time t_1 and the ADC differential input rises up to PFS at time t_2 . At time t_3 , the differential input of the ADC is completely settled at PFS.

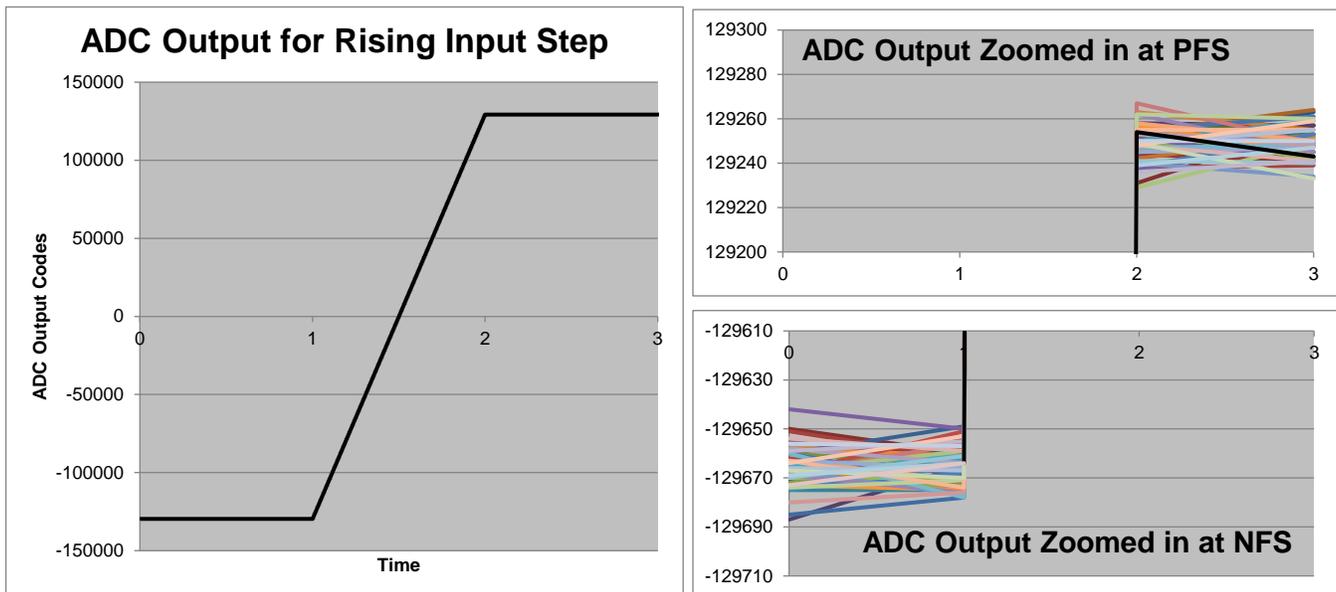


Figure 23. Measurement Data - ADC Transient Output Response for Rising Input Step

Table 5. Average Values of ADC Output Codes w.r.t. Time

Time Instant	t_0	t_1	t_2	t_3
Average Value of Codes	-129665.82	-129664.96	129249.32	129249.00
Standard Deviation	8.4	8.0	8.0	7.0

According to the measurement results described in Table 5, the standard deviation of codes is relatively constant at all time instants. This indicates that we can analyze the change in input signal between any two time instants by looking at the difference between the average code value. Based on this, the measurement results shown in Table 6 imply that the ADC inputs have settled to the required accuracy for every conversion.

Table 6. Time-Domain Results for ADC Input Settling

Difference between Average of ADC Output Codes	Value	Comment
Code (t_1) - Code (t_0)	0.9	Output Settled at NFS within 1 LSB error
Code (t_2) - Code (t_1)	258914.3	Step Change in Output = 98.8% of FSR
Code (t_3) - Code (t_2)	0.3	Output Settled at PFS within 1 LSB error

6.4 Transient Settling for Falling Input Step

The same measurement (as in [Section 6.3](#)) is repeated to measure the settling behavior of the front-end circuit for a full-scale falling step. The response in [Figure 24](#) shows the corresponding ADC output behavior. The zoomed-in views of the ADC output response near PFS and NFS are shown in the plots on the right. This response has been analyzed at 4 instants of time specified as t_0 , t_1 , t_2 and t_3 . At time t_0 , the differential input of the ADC is completely settled at PFS. The full-scale step appears at time t_1 and the ADC differential input falls to NFS at time t_2 . At time t_3 , the differential input of the ADC is completely settled at NFS.

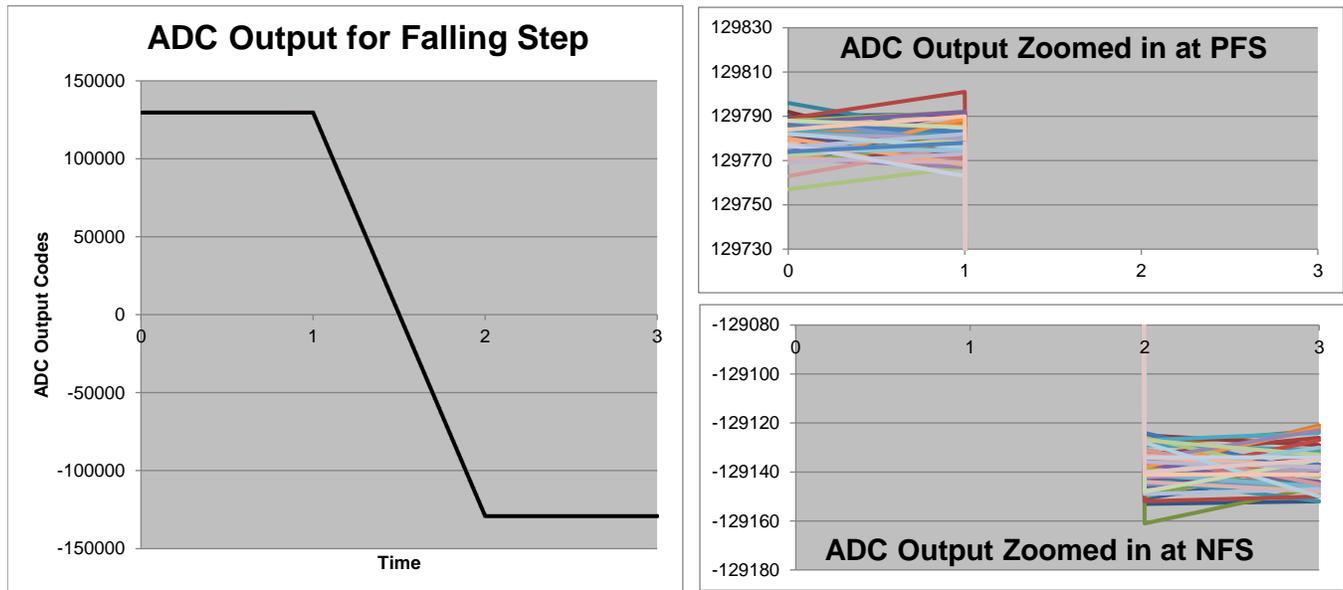


Figure 24. Measurement Data - ADC Transient Output Response for Falling Input Step

Table 7. Average Values of ADC Output Codes w.r.t. Time

Time Instant	t_0	t_1	t_2	t_3
Average Value of Codes	129778.94	129778.40	-129138.00	-129138.22
Standard Deviation	7.5	8.0	8.2	8.1

According to the measurement results described in [Table 7](#), the standard deviation of codes is relatively constant at all time instants. This indicates that we can analyze the change in input signal between any two time instants by looking at the difference between the average code value. Based on this, the measurement results shown in [Table 8](#) imply that the ADC inputs have settled to the required accuracy for every conversion.

Table 8. Time-Domain Results for ADC Input Settling

Difference between Average of ADC Output Codes	Value	Comment
Code (t_1) - Code (t_0)	-0.5	Output Settled at PFS within 1LSB error
Code (t_2) - Code (t_1)	258916.4	Step Change in Output = 98.8 % of FSR
Code (t_3) - Code (t_2)	-0.2	Output Settled at NFS within 1LSB error

6.5 ADC Dynamic Performance Measurement

The TI Precision Design explained in this document has been optimized to achieve maximum performance out of ADS8881 at 1MSPS throughput for a full-scale transient input signal. However, this system also achieves excellent ac noise and distortion performance, as listed in Table 9. The measurements have been performed using a 10 kHz sinusoidal input signal. Figure 25 shows a screen-shot of TI's ADCPro™ tool displaying the measured ac performance of the system. The datasheet specifications are based on $V_{REF} = 5\text{ V}$, but these measurement results indicate the ADC performance for $V_{REF} = 4.5\text{ V}$, which implies that the measured values are approximately 0.9 dB less than the actual ADC performance for SNR, THD and SINAD. Despite this adjustment, the SNR for the system does not meet the specifications of the ADC. This is due to the fact that a higher bandwidth RC-filter was designed at the inputs of the ADC to allow for accurate settling of the full-scale step input signal. This resulted in an increase in the broadband noise contribution from the front-end circuit into the inputs of the ADC thereby degrading the ac performance of the system. The overall noise in this design was dominated by the front-end driving amplifiers, which is the primary cause for degradation in the SNR and subsequently SINAD of the system.

Table 9. Measurement Results for ADC AC Performance

Parameter	ADS8881 Data Sheet Specifications	Measured Value
Signal to Noise Ratio - SNR (dB)	99 @ $V_{REF} = 5\text{ V}$	94.97
Total Harmonic Distortion - THD (dB)	-112 @ $V_{REF} = 5\text{ V}$	-113.96
Signal to Noise and Distortion Ratio - (SINAD) (dB)	98.8 @ $V_{REF} = 5\text{ V}$	94.91

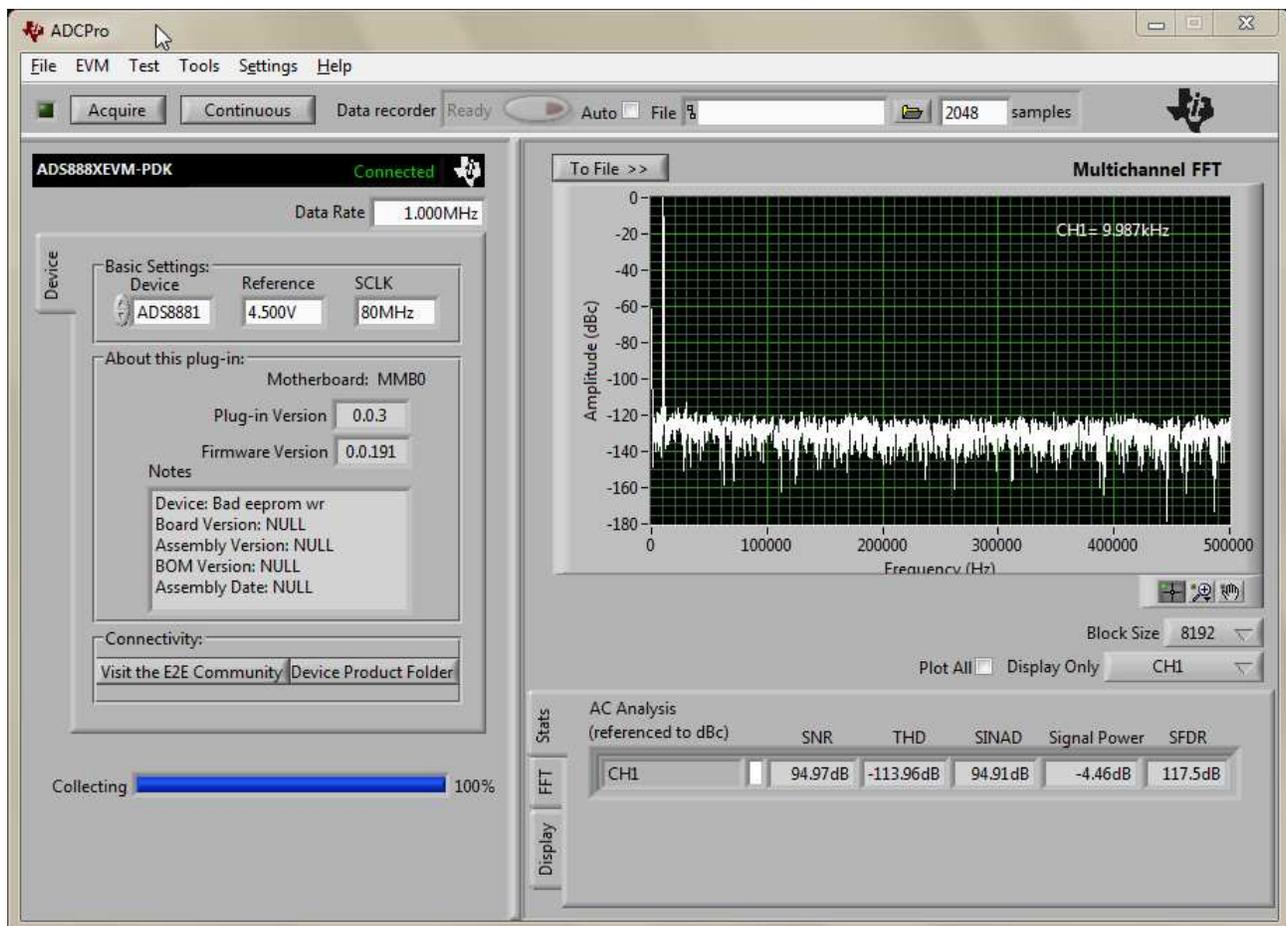


Figure 25. Measurement Data - AC Performance of DAQ Block Using ADCPro™

7 Modifications

The components selected for this design are optimized to meet the design goals mentioned in [Section 1](#) at the beginning of the design. Selecting a high-bandwidth and rail-to-rail input amplifier like the OPA350 helps to achieve the 18-bit settling of a full scale step input signal at a maximum throughput of 1 MSPS.

The bandwidth and settling requirements for the input driver amplifiers get significantly relaxed if the sampling rate for the application is reduced. This is because the conversion time for the ADC stays almost the same and any increase in the converter's cycle time adds to the acquisition time of the ADC, thus allowing a lot more time for the amplifier output to settle to the required accuracy.

The other factor that can help to relax the requirements on the input driver amplifier is the signal swing at the input. If the size of the input step is reduced to a half-scale or a quarter-scale of the ADC full scale input range, then the input driver does not need to support rail-to-rail input and output swing. In addition, the output of the driving amplifier has to settle to a smaller voltage step that relaxes the bandwidth specifications for the op amp, which can be traded off for power.

[Table 10](#) lists some suggested combination of drivers for driving the ADC inputs and for reduced throughput and input signal step.

Table 10. Brief Comparison of Drivers for ADC Input Stage for Modified System Requirements

Input Signal Step	Throughput	Input Driver Amplifier	Amplifier Unity Gain Bandwidth	Amplifier Quiescent Current
½ × Full Scale Voltage	500 Ksps	OPA836	205 MHz	0.95 mA
½ × Full Scale Voltage	100 Ksps	OPA320	20 MHz	1.5 mA
¼ × Full Scale Voltage	500 Ksps	OPA835	56 MHz	0.25 mA
¼ × Full Scale Voltage	100 Ksps	OPA314	3 MHz	0.15 mA

8 About the Author

VINAY AGARWAL is a product definer in the Precision Analog, SAR ADC team at Texas Instruments based in Tucson, Arizona. Prior to this role, he has worked on designing precision data converters and amplifiers at TI. Vinay earned his Master of Science degree from Tufts University, Medford and Bachelors in Technology (Honors) from Indian Institute of Technology, Kharagpur in India.

9 References and Acknowledgments

1. Tim Green; *Operational Amplifier Stability - Parts 1-11*, November 2008, Available: http://www.genius.net/site/zones/acquisitionZONE/technical_notes/acqt_050712
2. Bonnie C. Baker, Miro Oljaca; <http://www.electro-tech-online.com/custompdfs/2013/05/6602451.pdf>
3. Tim Green; *Selecting the right amplifier for precision CDAC SAR A/D* - Internal Presentation, February 2008
4. Credit for this work goes to Rafael Ordonez for designing the PCB board schematic and layout and taking all the measurement data.

10 Appendix

10.1 Schematics

To download the schematics, see the design files at [TIPD112](#).

10.2 Bill of Materials

To download the bill of materials (BOM), see the design files at [TIPD112](#).

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

REVISION	PAGE	DESCRIPTION
TIDU012 (formerly SLAU512)		Initial release
TIDU012A (formerly SLAU512A)	10, 11	Updated Theory of Operation for Reference Driver Design
	15	Updated reference current for ADS8881
TIDU012B (formerly SLAU512B)	1, 16, 17	Updated front page block diagram and Figs. 11, 12, 13; Changed system supply to OPA+ and ADC supply to AVDD
	2	Updated Design Summary; Modified OPA+ and AVDD supply specifications
TIDU012C	8, 18	Updated option to use the REF6045 as an alternate solution (Section 2.3 Reference Driver Design and Section 3.2.3 Integrated Reference and Buffer)
	30	Updated Schematic and BOM to reflect the alternate option of using the REF6045 and removed from write-up. Removed Schematic and BOM images from document, which are available for download at www.ti.com/tool/TIPD112 .

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