Test Report: PMP31273

Automotive Dual Buck Converter Reference Design for C2000™ MCU With Supervisor and Watchdog

Description

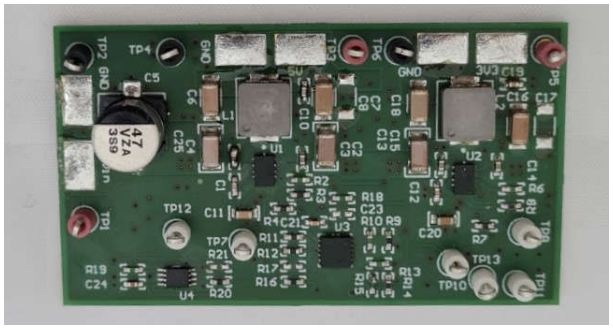
This reference design is a flexible and compact power supply providing 5-V and 3.3-V output rails to supply the C2000™ MCU. The design includes 2 × LMR34206-Q1 devices (an ultra-small synchronous step-down converter) and one TPS3850-Q1 (a precision voltage supervisor with programmable window watchdog timer). In addition, a single D-type flip flop (SN74LVC2G74-Q1) is added to provide the compatibility of the watchdog with the C2000™ MCU start-up behavior.

Features

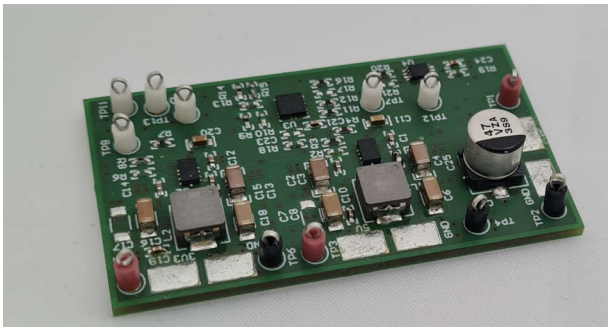
- Dual output (5 V and 3.3 V)
- High-efficiency conversion due to use of synchronous rectification
- Precision voltage supervisor
- Programmable window watchdog timer
- Design was built and tested

Applications

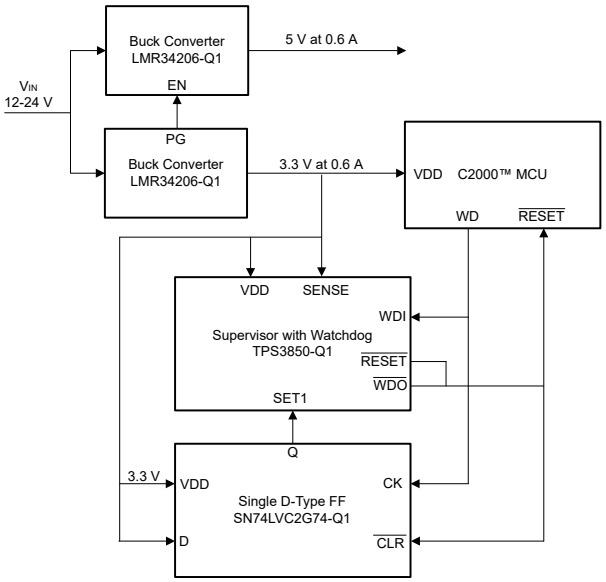
- DC-fast charging
- Traction inverter-high voltage
- Automotive HVAC compressor module



Top of Board



Angled Board Photo



Block Diagram

1 Test Prerequisites

1.1 Voltage and Current Requirements

Table 1-1. Voltage and Current Requirements

Parameter	Specifications
V_{IN}	12.0 V – 24.0 V
V_{OUT1}	5.0 V
I_{OUT1}	0.6 A
V_{OUT2}	3.3 V
I_{OUT2}	0.6 A

1.2 Dimensions

The outline of the board is 28.66 mm × 50.81 mm.

2 Testing and Results

2.1 Efficiency Graphs

Efficiency is shown in the following figures.

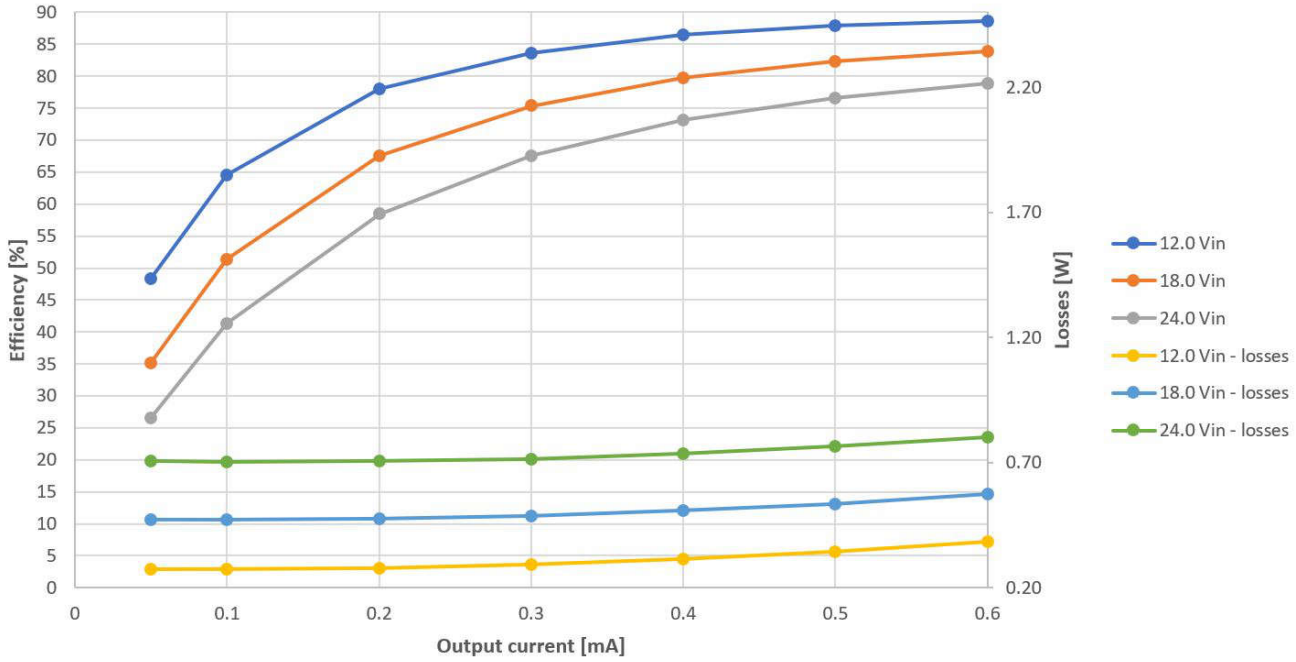


Figure 2-1. Efficiency Graph of V_{OUT1} = 5 V

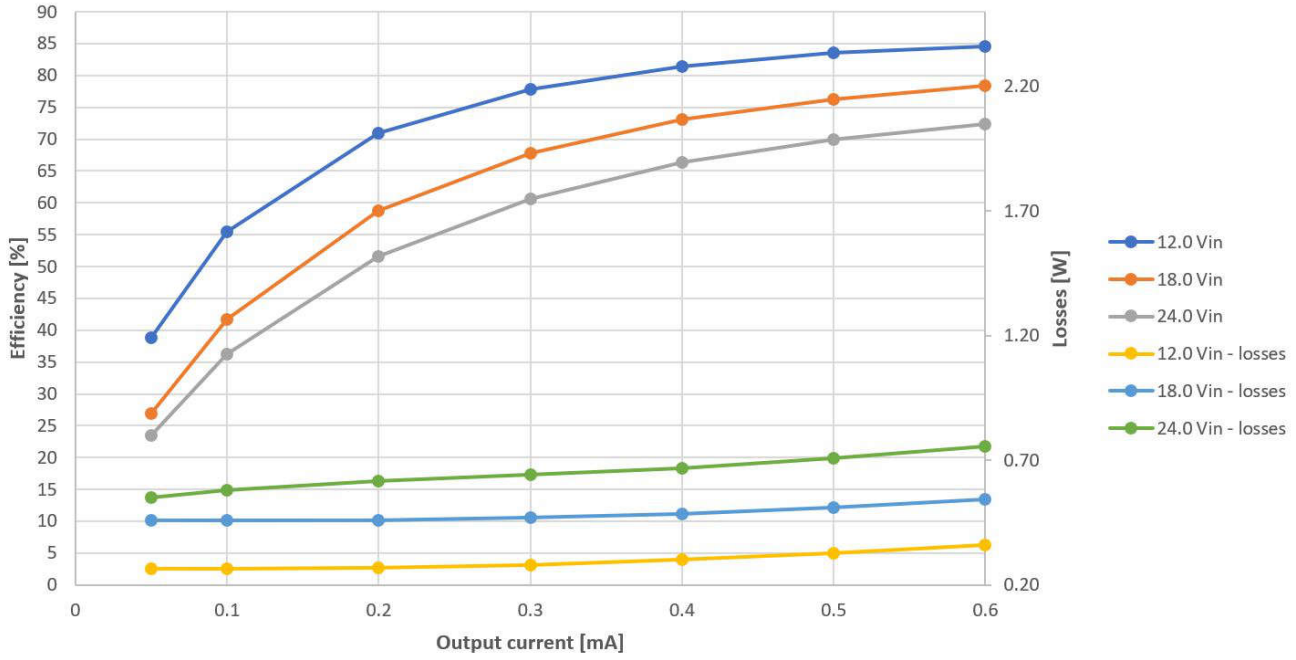


Figure 2-2. Efficiency Graph of V_{OUT2} = 3.3 V

2.2 Efficiency Data

Table 2-1 through Table 2-3 show the efficiency data for V_{OUT1}.

Table 2-1. Efficiency Data V_{OUT1}, V_{IN} = 12 V

V_{IN} (V)	I_{IN} (A)	V_{OUT} (V)	I_{OUT} (A)	P_{IN} (W)	P_{OUT} (W)	P_{LOSS} (W)	Efficiency (%)
12.01	44.00	4.978	51.30	0.53	0.26	0.27	48.3
12.00	64.20	4.978	99.90	0.77	0.50	0.27	64.6
12.00	106.10	4.978	199.70	1.27	0.99	0.28	78.1
11.99	148.80	4.978	299.60	1.78	1.49	0.29	83.6
11.98	193.30	4.977	402.10	2.32	2.00	0.31	86.4
11.98	237.30	4.977	501.90	2.84	2.50	0.34	87.9
11.98	282.10	4.976	601.80	3.38	2.99	0.39	88.6

Table 2-2. Efficiency Data V_{OUT1}, V_{IN} = 18 V

V_{IN} (V)	I_{IN} (A)	V_{OUT} (V)	I_{OUT} (A)	P_{IN} (W)	P_{OUT} (W)	P_{LOSS} (W)	Efficiency (%)
18.02	40.40	4.979	51.30	0.73	0.26	0.47	35.1
18.02	53.80	4.978	99.90	0.97	0.50	0.47	51.3
18.02	81.60	4.978	199.70	1.47	0.99	0.48	67.6
18.02	109.80	4.977	299.60	1.98	1.49	0.49	75.4
18.01	139.30	4.977	402.10	2.51	2.00	0.51	79.8
18.01	168.40	4.977	501.90	3.03	2.50	0.53	82.4
18.00	198.20	4.976	601.80	3.57	2.99	0.57	83.9

Table 2-3. Efficiency Data V_{OUT1}, V_{IN} = 24 V

V_{IN} (V)	I_{IN} (A)	V_{OUT} (V)	I_{OUT} (A)	P_{IN} (W)	P_{OUT} (W)	P_{LOSS} (W)	Efficiency (%)
24.02	40.00	4.978	51.30	0.96	0.26	0.71	26.6
24.02	50.00	4.978	99.80	1.20	0.50	0.70	41.4
24.02	70.80	4.977	199.70	1.70	0.99	0.71	58.4
24.01	91.90	4.977	299.60	2.21	1.49	0.72	67.6
24.01	114.00	4.976	402.10	2.74	2.00	0.74	73.1
24.01	135.90	4.976	501.90	3.26	2.50	0.77	76.5
24.00	158.20	4.975	601.80	3.80	2.99	0.80	78.9

Table 2-4 through Table 2-6 show the efficiency data for V_{OUT2}.

Table 2-4. Efficiency Data V_{OUT2}, V_{IN} = 12 V

V_{IN} (V)	I_{IN} (A)	V_{OUT} (V)	I_{OUT} (A)	P_{IN} (W)	P_{OUT} (W)	P_{LOSS} (W)	Efficiency (%)
12.05	36.00	3.285	51.30	0.43	0.17	0.27	38.8
12.05	49.20	3.285	100.00	0.59	0.33	0.26	55.4
12.05	76.80	3.284	199.80	0.93	0.66	0.27	70.9
12.05	105.00	3.284	299.70	1.27	0.98	0.28	77.8
12.05	134.60	3.284	402.20	1.62	1.32	0.30	81.4
12.04	164.00	3.284	502.00	1.97	1.65	0.33	83.5
12.04	194.10	3.284	602.00	2.34	1.98	0.36	84.6

Table 2-5. Efficiency Data V_{OUT2}, V_{IN} = 18 V

V_{IN} (V)	I_{IN} (A)	V_{OUT} (V)	I_{OUT} (A)	P_{IN} (W)	P_{OUT} (W)	P_{LOSS} (W)	Efficiency (%)
18.06	34.80	3.286	51.40	0.63	0.17	0.46	26.9
18.06	43.60	3.286	100.00	0.79	0.33	0.46	41.7
18.06	61.80	3.285	199.80	1.12	0.66	0.46	58.8
18.06	80.50	3.285	299.70	1.45	0.98	0.47	67.7
18.05	100.10	3.284	402.20	1.81	1.32	0.49	73.1
18.05	119.70	3.284	502.00	2.16	1.65	0.51	76.3
18.05	139.70	3.284	602.00	2.52	1.98	0.54	78.4

Table 2-6. Efficiency Data V_{OUT2}, V_{IN} = 24 V

V_{IN} (V)	I_{IN} (A)	V_{OUT} (V)	I_{OUT} (A)	P_{IN} (W)	P_{OUT} (W)	P_{LOSS} (W)	Efficiency (%)
24.00	29.90	3.292	51.30	0.72	0.17	0.55	23.5
24.01	37.80	3.288	99.90	0.91	0.33	0.58	36.2
24.01	53.00	3.286	199.80	1.27	0.66	0.62	51.6
24.01	67.70	3.285	299.70	1.63	0.98	0.64	60.6
24.01	82.90	3.285	402.20	1.99	1.32	0.67	66.4
24.00	98.20	3.285	502.00	2.36	1.65	0.71	70.0
24.00	113.80	3.285	601.90	2.73	1.98	0.75	72.4

2.3 Thermal Images

The thermal image is shown in the following figure for V_{IN} = 18 V.

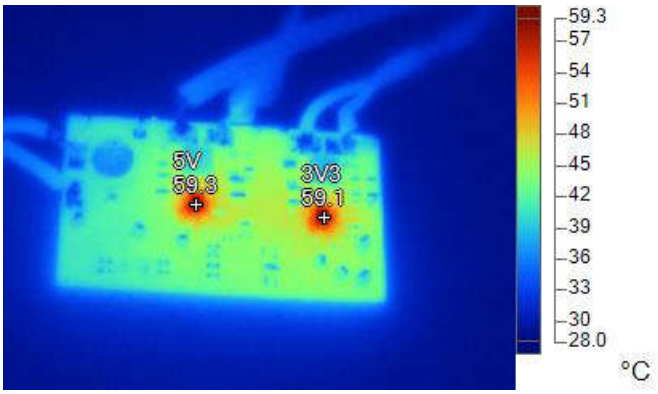
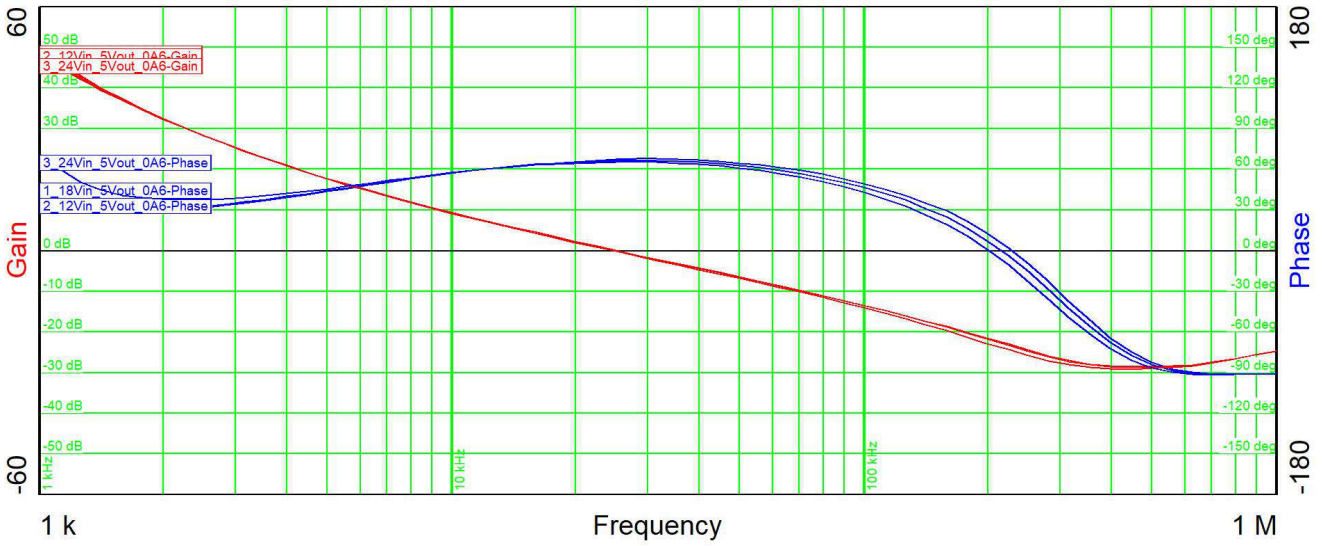


Figure 2-3. Thermal Image at Full Load (I_{OUT1} = 0.6 A, I_{OUT2} = 0.6 A)

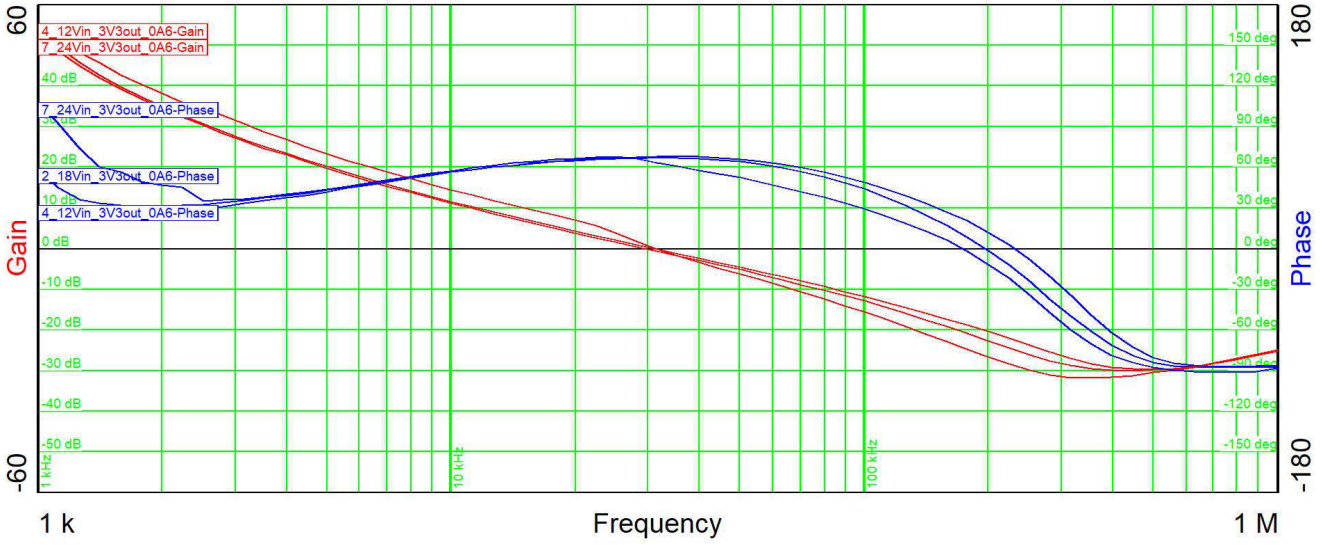
2.4 Bode Plots

Bode plots are shown in the following figures.



12 V_{IN}, 0.6-A load current: fco 25.2 kHz, 66 deg phase margin, –23 dB gain margin
18 V_{IN}, 0.6-A load current: fco 24.7 kHz, 67 deg phase margin, –23 dB gain margin
24 V_{IN}, 0.6-A load current: fco 24.4 kHz, 65 deg phase margin, –23 dB gain margin

Figure 2-4. Bode Plot V_{OUT1} = 5 V



12 V_{IN}, 0.6-A load current: fco 31.0 kHz, 68 deg phase margin, –23 dB gain margin
18 V_{IN}, 0.6-A load current: fco 29.3 kHz, 66 deg phase margin, –22 dB gain margin
24 V_{IN}, 0.6-A load current: fco 31.1 kHz, 63 deg phase margin, –24 dB gain margin

Figure 2-5. Bode Plot V_{OUT2} = 3.3 V

3 Waveforms

3.1 Switching

Switching behavior is shown in the following figures.

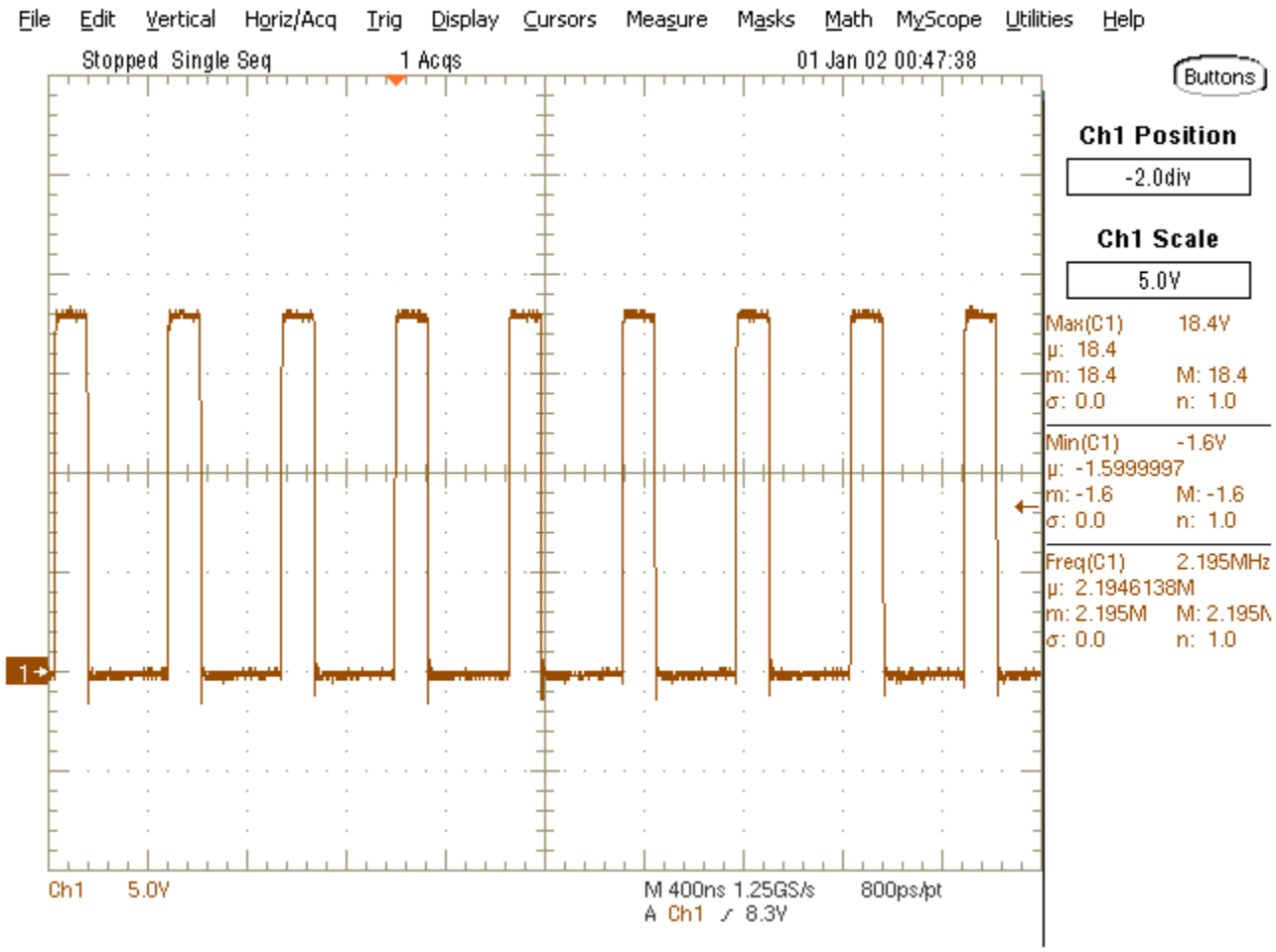


Figure 3-1. Switching 1 (V_{IN} = 18 V, V_{OUT1} = 5 V, I_{OUT1} = 0.6 A)

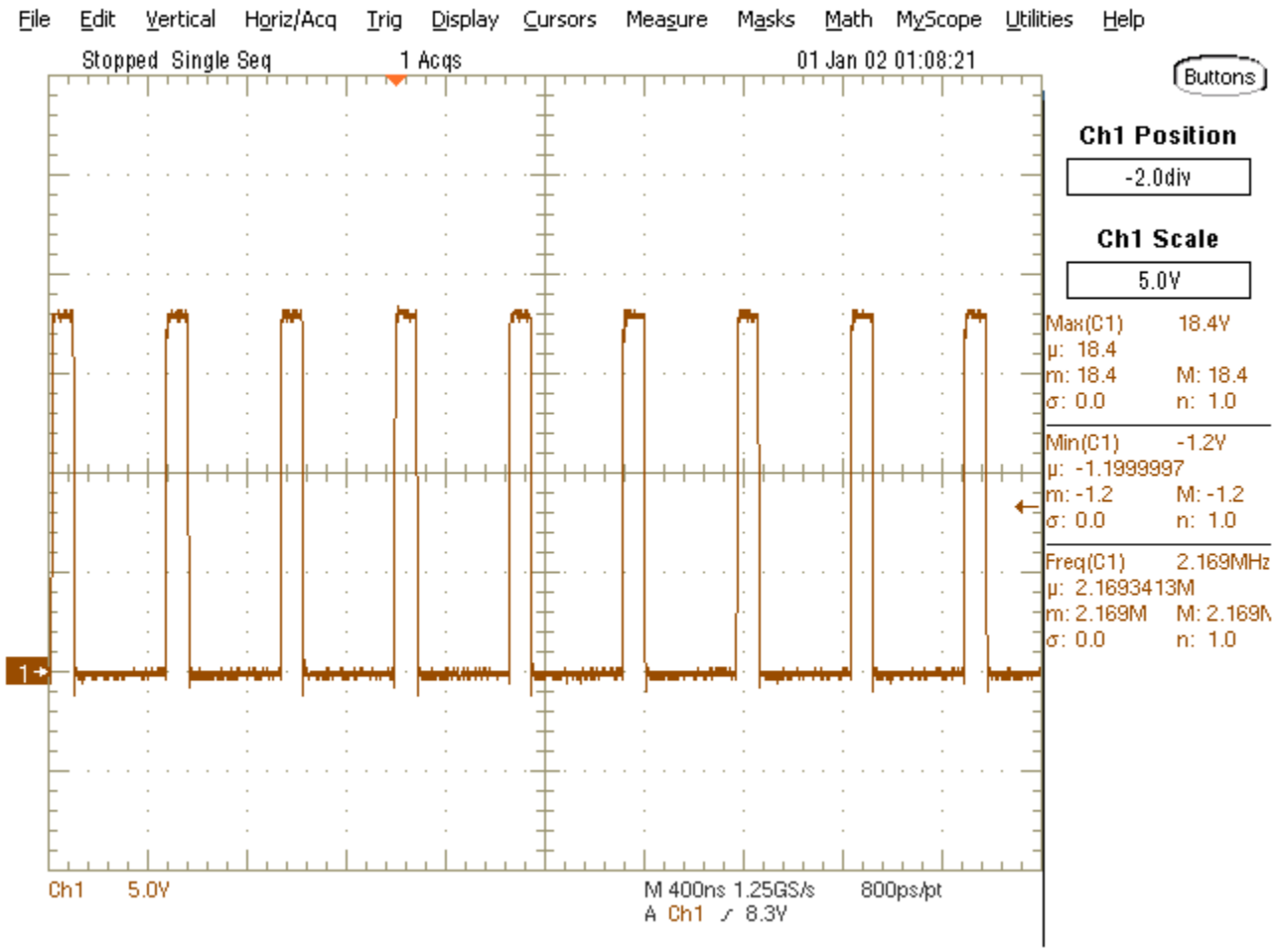


Figure 3-2. Switching 2 (V_{IN} = 18 V, V_{OUT2} = 3.3 V, I_{OUT2} = 0.6 A)

3.2 Output Voltage Ripple

Output voltage ripple is shown in the following figures.

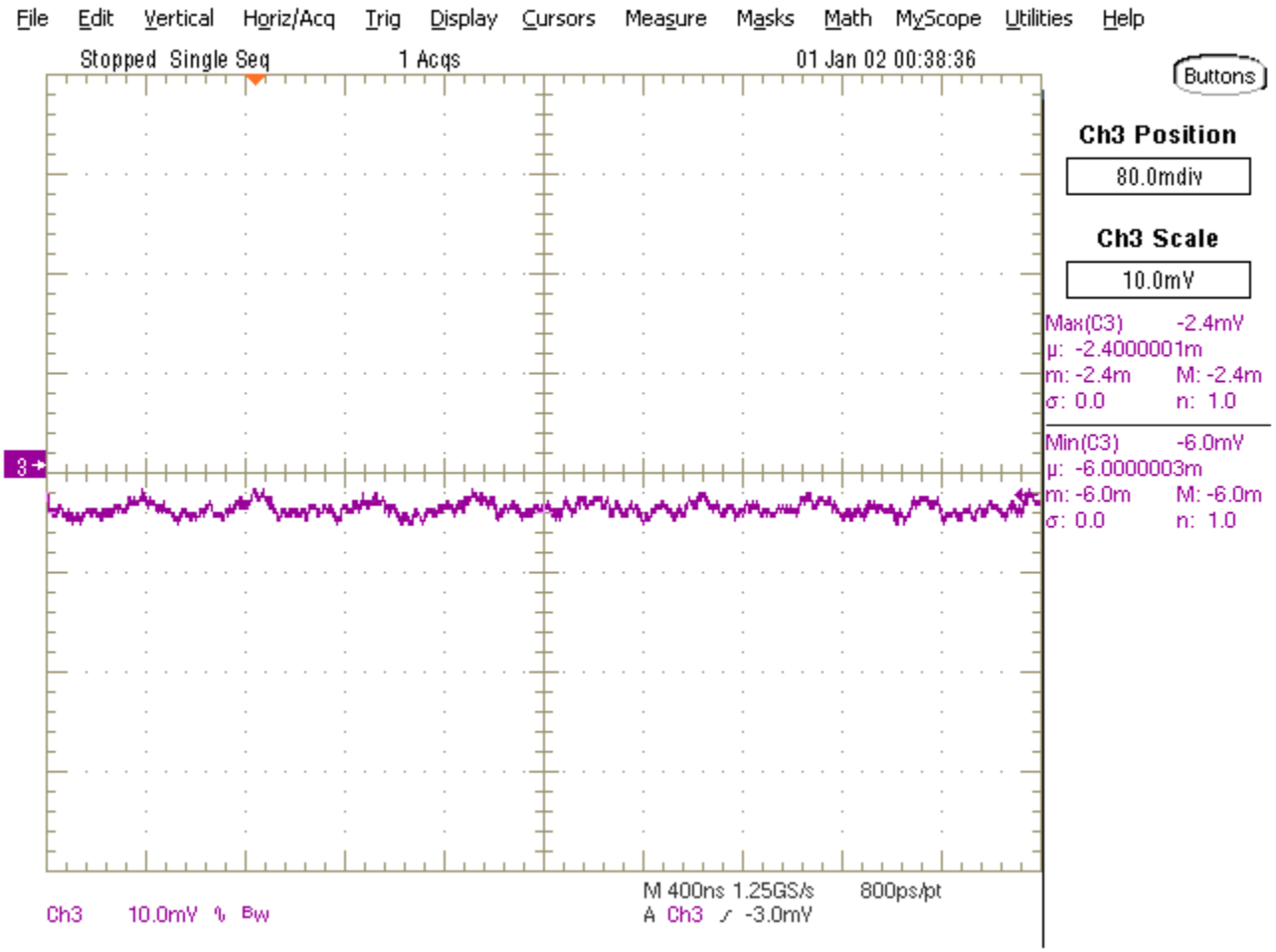


Figure 3-3. Output Voltage Ripple 1 (V_{IN} = 18 V, V_{OUT1} = 5 V, I_{OUT1} = 0.6 A), 20-MHz Bandwidth Limited

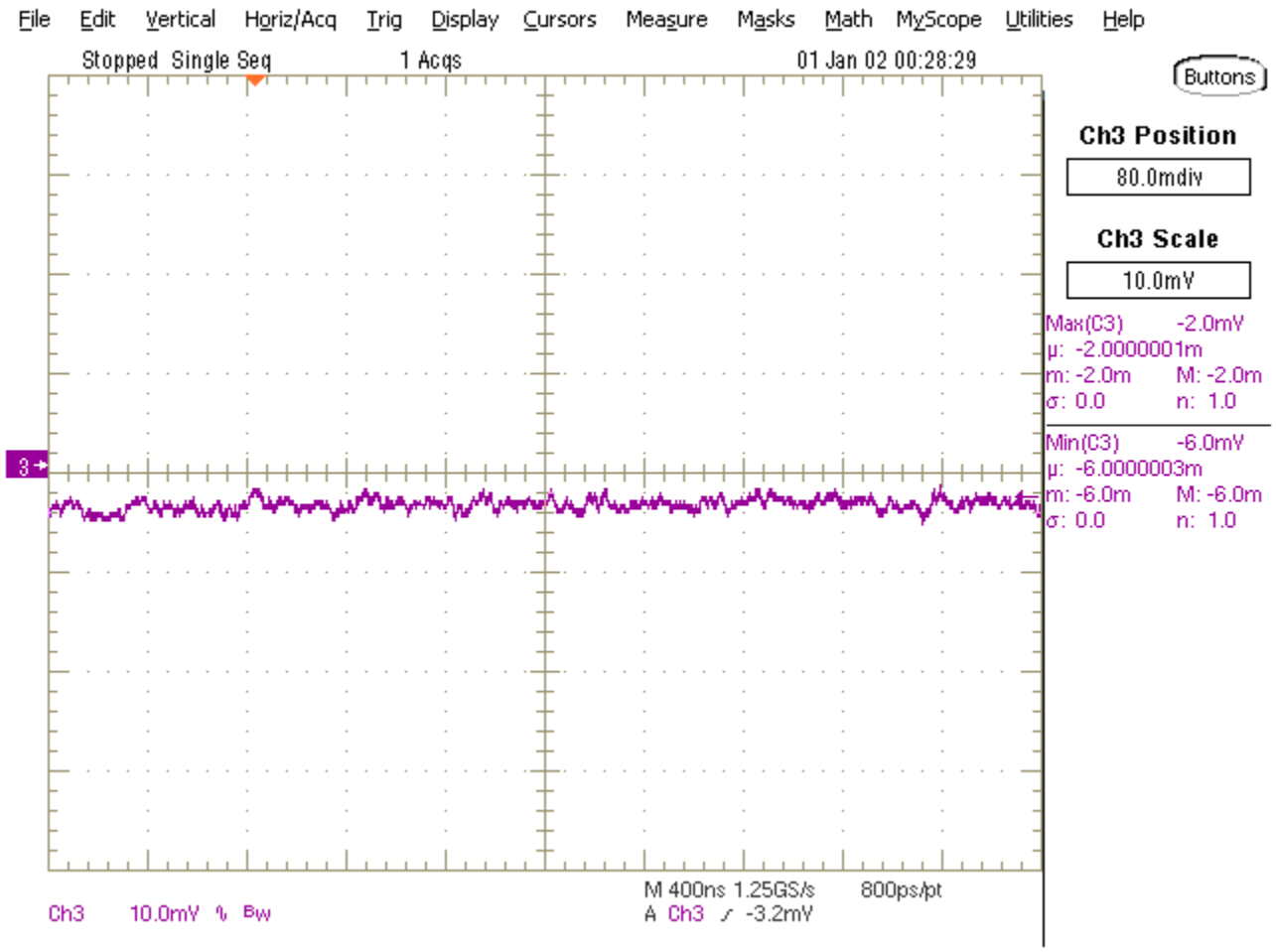


Figure 3-4. Output Voltage Ripple 2 (V_{IN} = 18 V, V_{OUT2} = 3.3 V, I_{OUT2} = 0.6 A), 20-MHz Bandwidth Limited

3.3 Input Voltage Ripple

Input voltage ripple is shown in the following figures.

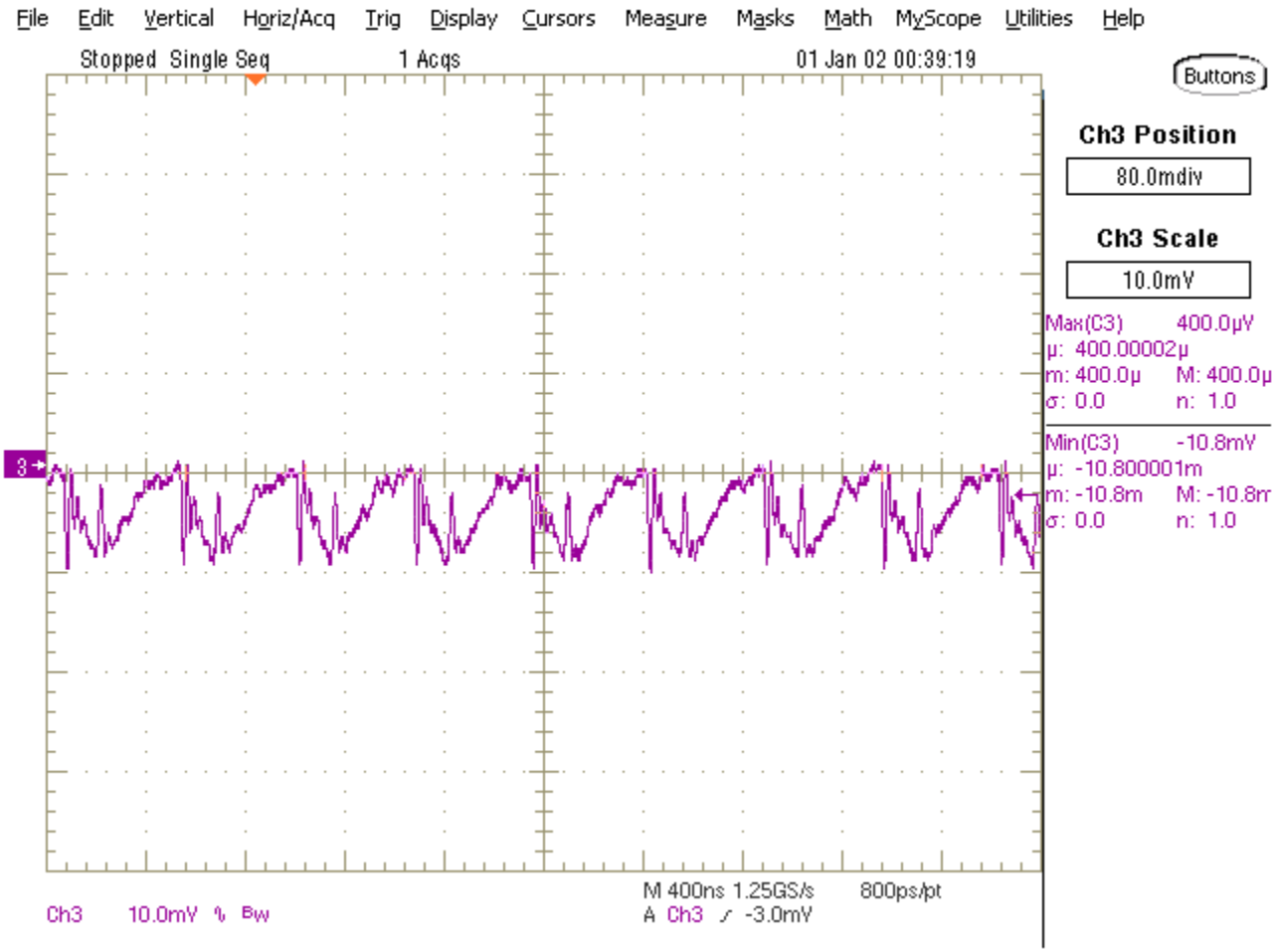


Figure 3-5. Input Voltage Ripple 1 (V_{IN} = 18 V, V_{OUT1} = 5 V, I_{OUT1} = 0.6 A), 20-MHz Bandwidth Limited

Figure 3-6. Input Voltage Ripple 2 (V_{IN} = 18 V, V_{OUT2} = 3.3 V, I_{OUT2} = 0.6 A), 20-MHz Bandwidth Limited

3.4 Load Transients

Load transient response is shown in the following figures.

Electronic load was used to create the load steps.

The output capacitors need to be optimized according to the worst-case load step to meet the specific C2000 MCU supply requirements.

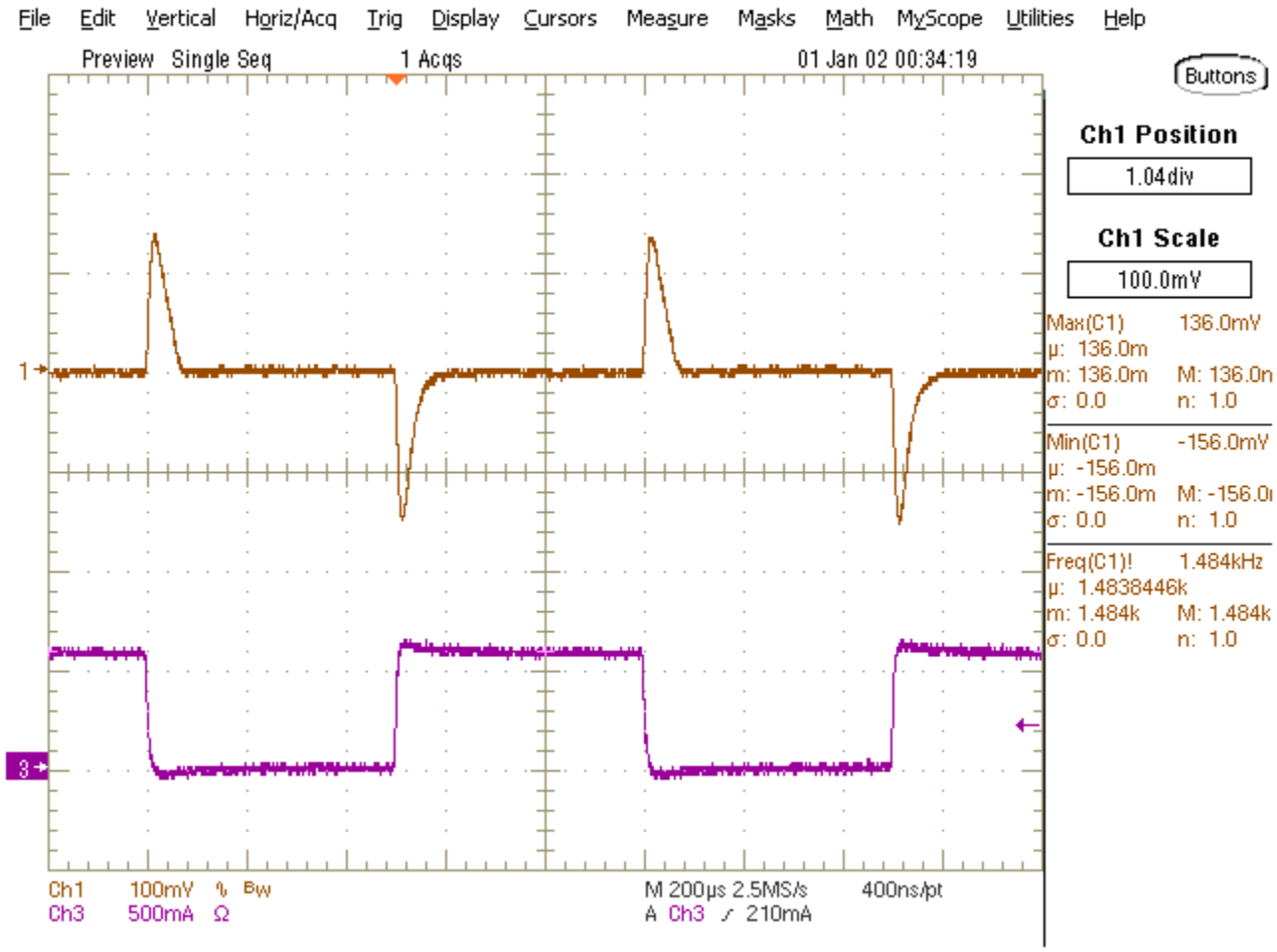


Figure 3-7. Load Transients 1 (V_{IN} = 18 V, CH1: V_{OUT1} = 5 V, CH3: I_{OUT1} = 0 → 0.6 A), 20-MHz Bandwidth Limited

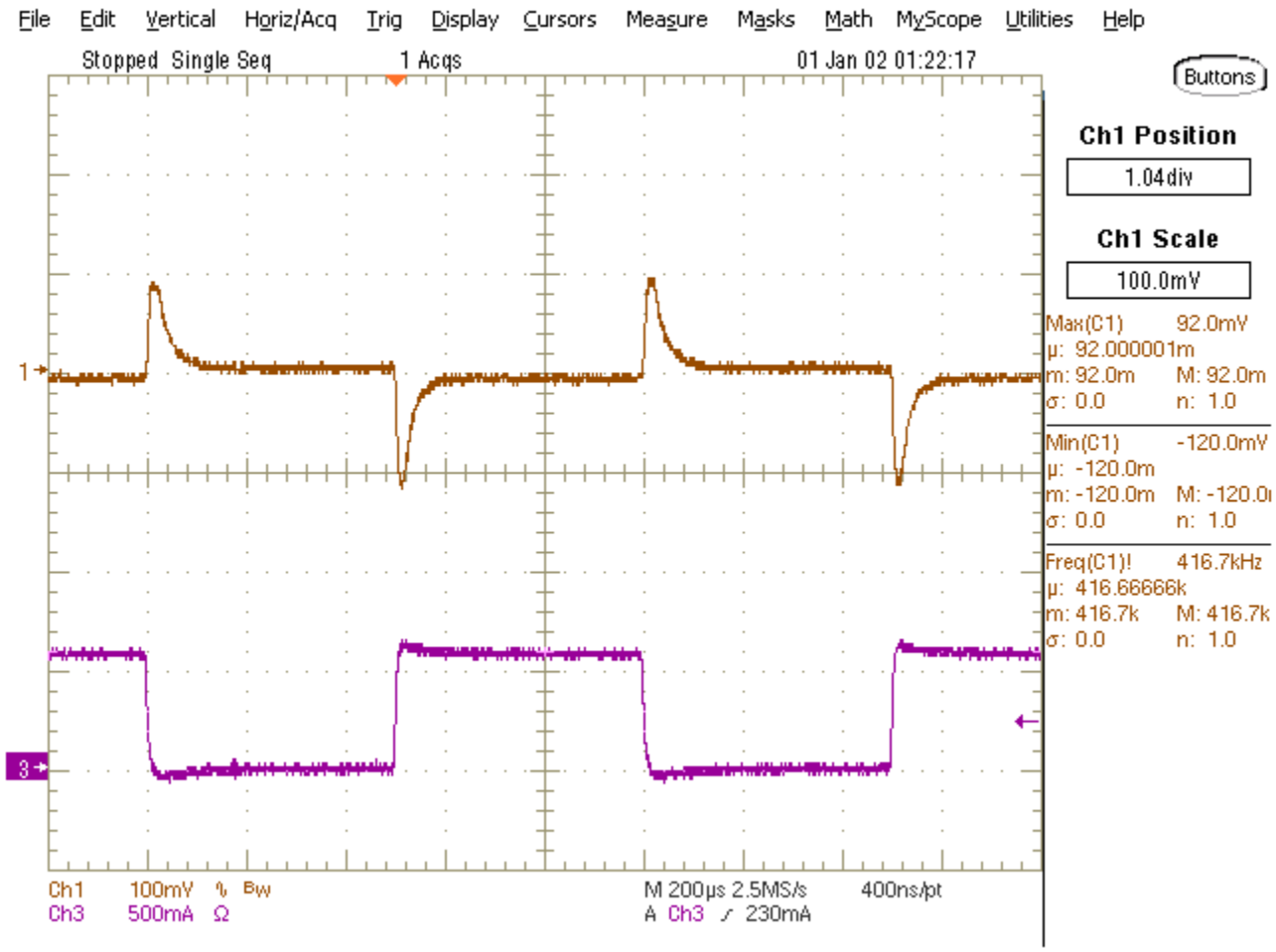


Figure 3-8. Load Transients 2 (V_{IN} = 18 V, CH1: V_{OUT2} = 3.3 V, CH3: I_{OUT2} = 0 → 0.6 A), 20-MHz Bandwidth Limited

3.5 Start-Up Sequence

Start-up behavior is shown in the following figure.

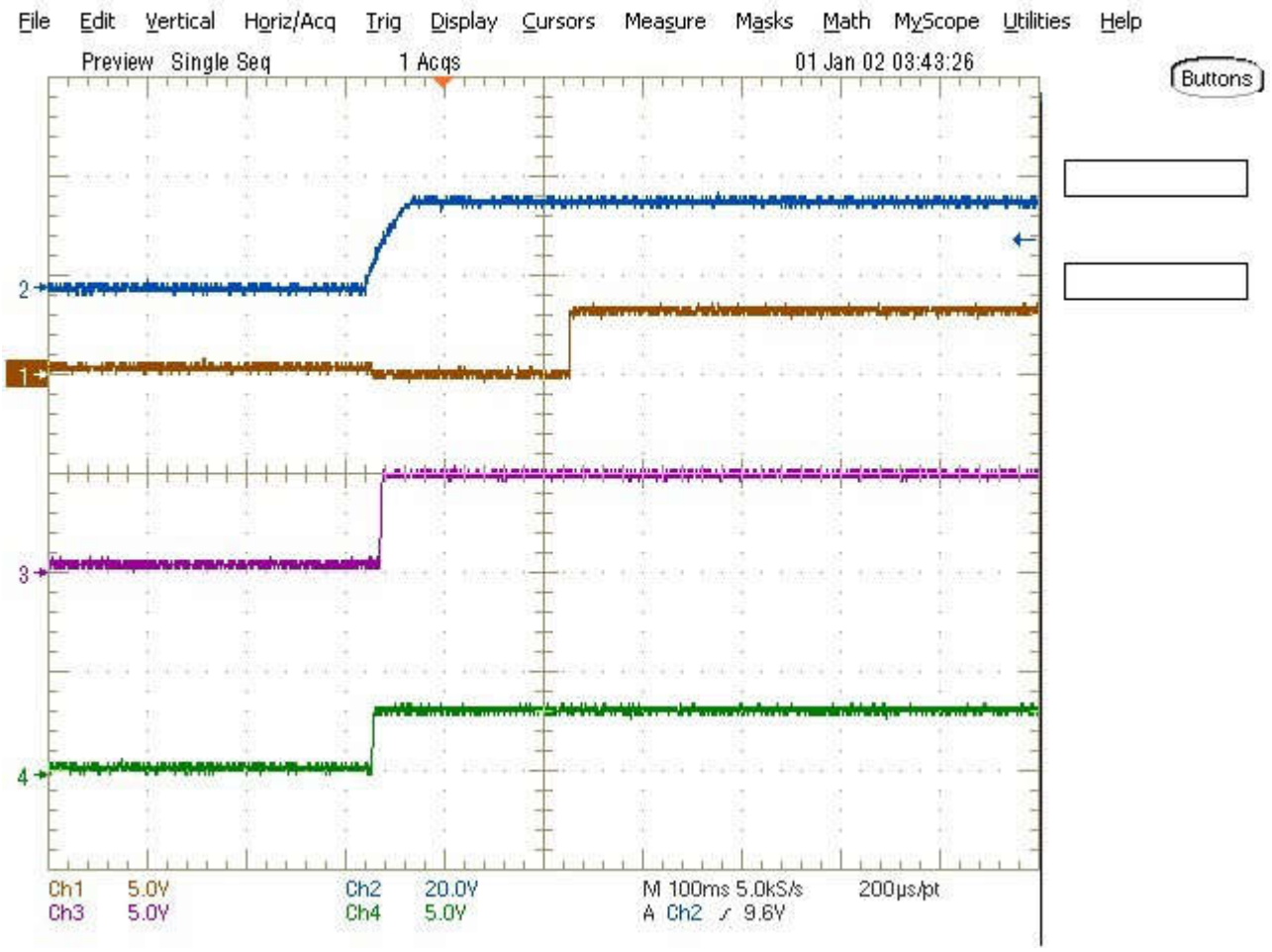


Figure 3-9. Start-Up (CH1: $\overline{\text{RESET}}$, CH2: V_{IN}, CH3: V_{OUT1}, CH4: V_{OUT2})

3.6 Voltage Supervisor

The voltage supervisor behavior is shown in the following figure. The device has ±7% overvoltage and undervoltage thresholds on the SENSE pin with respect to the nominal voltage of 3.3 V.

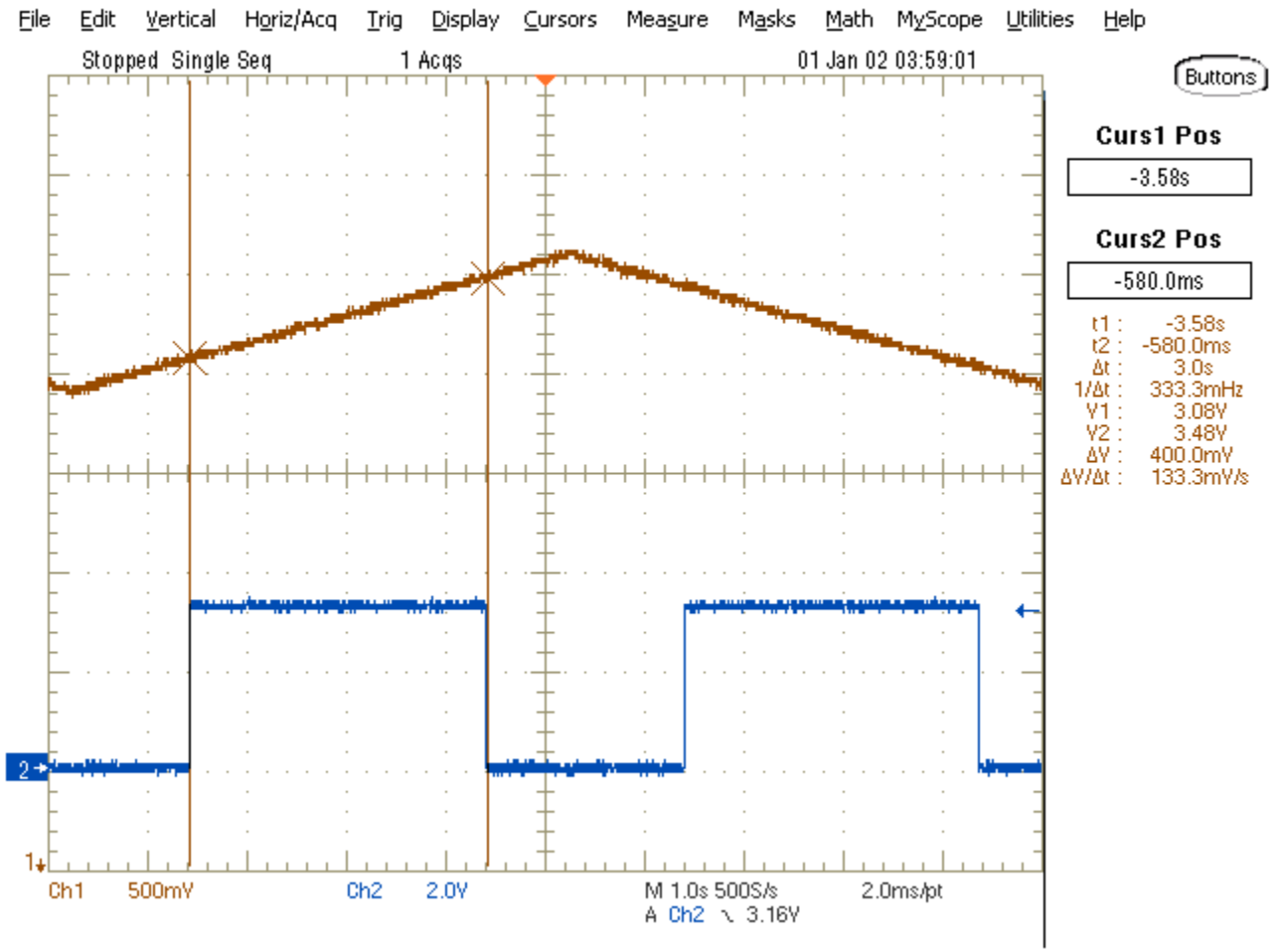
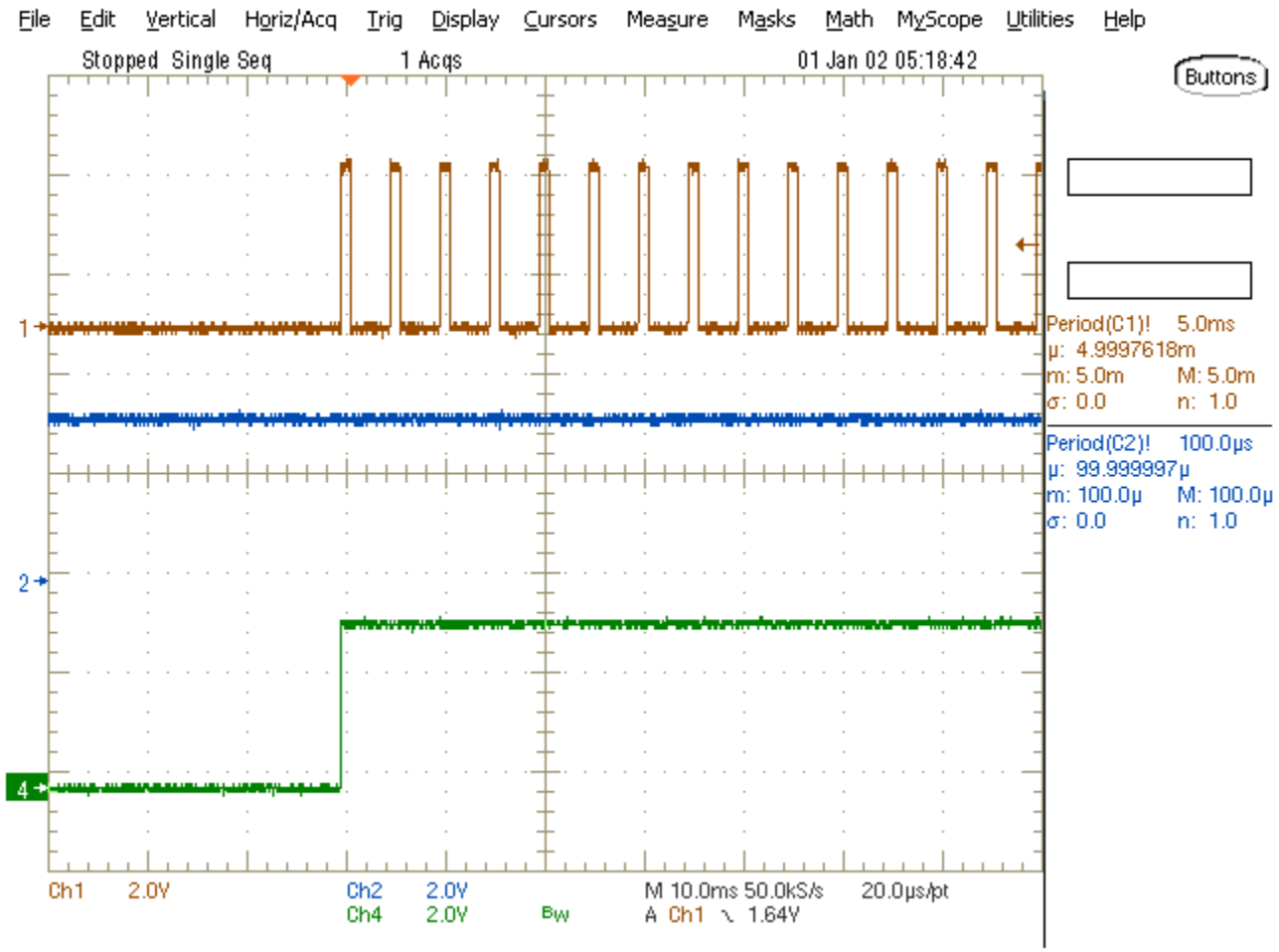


Figure 3-10. Voltage Supervisor (CH1: SENSE, CH2: $\overline{\text{RESET}}$)

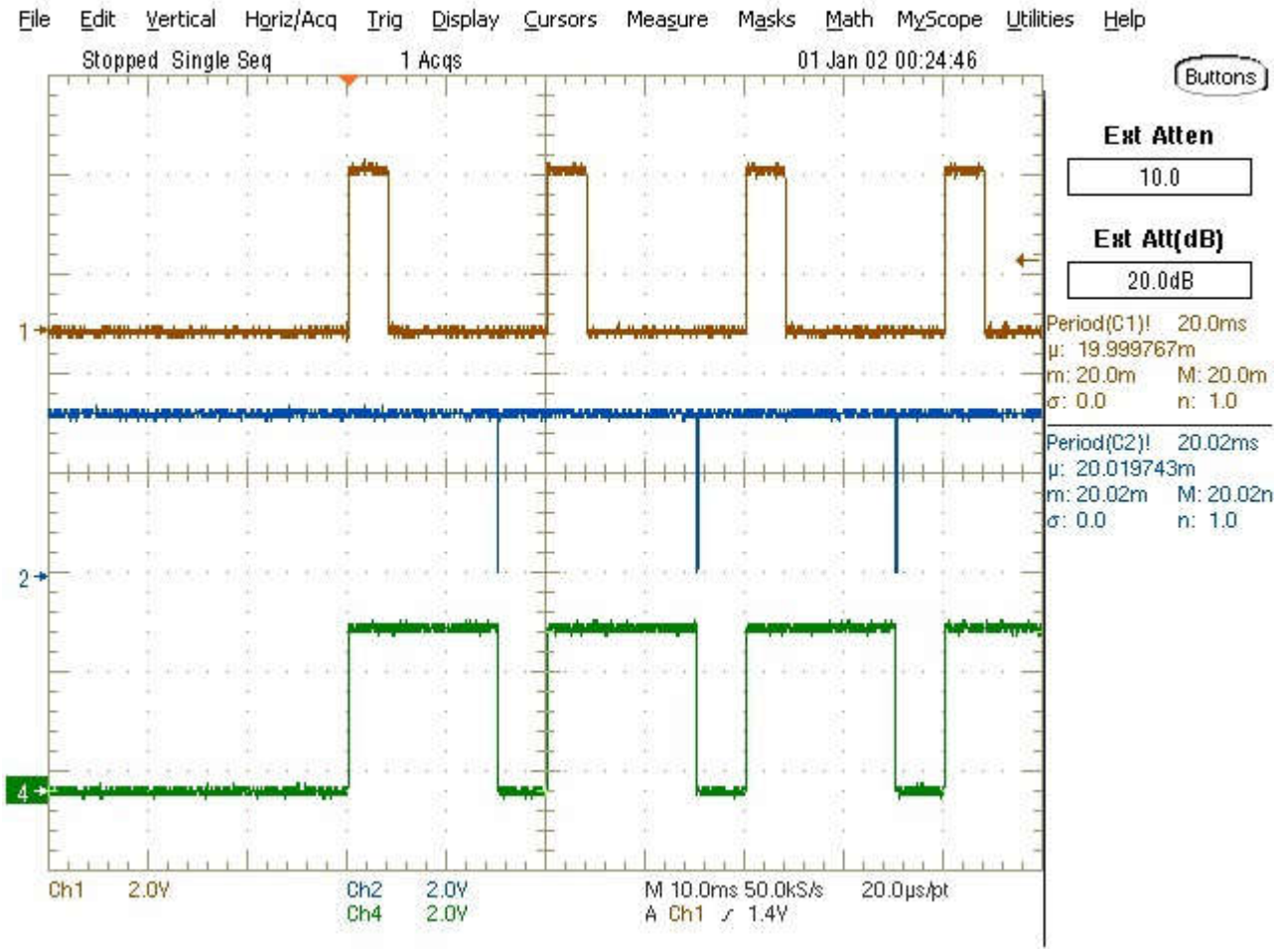
3.7 Watchdog

The watchdog timer behavior is shown in the following figures. The selected window watchdog is between 1.85 ms and 11.0 ms (typical values).



The watchdog is disabled (SET1 = LOW) until the first pulse on the input signal (WDI) occurs. After that, the watchdog is enabled via the flip flop (SET1 = HIGH). The watchdog does not output any errors since the WDI period is inside the allowed time window.

Figure 3-11. Watchdog at Start-Up (CH1: WDI at 5.0-ms Period, CH2: $\overline{\text{WDO}}$, CH4: SET1)



The watchdog is disabled (SET1 = LOW) until the first pulse on the input signal (WDI) occurs. After that, the watchdog is enabled via the flip flop (SET1 = HIGH). The watchdog outputs an error since the input signal period is outside the allowed time window. This resets the flip flop (SET1 = LOW), and the cycle starts again.

Figure 3-12. Watchdog at Start-Up (CH1: WDI at 20.0-ms Period, CH2: $\overline{\text{WDO}}$, CH4: SET1)

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