Test Report: PMP30819

Automotive Power Supply Reference Design With Three Outputs Using PMIC and LDOs

Description

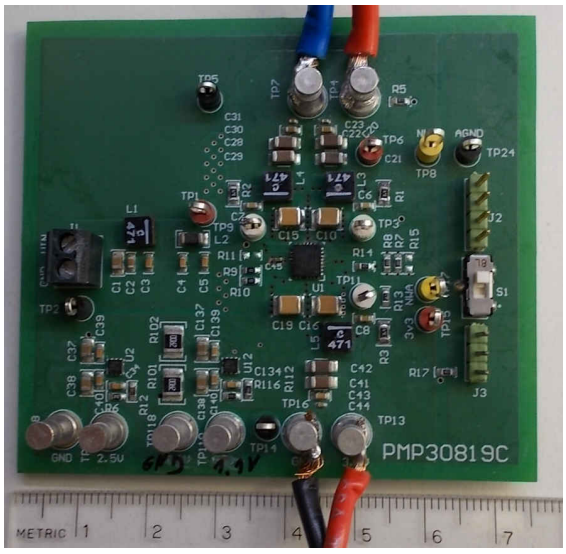
This multi-output supply powers a custom ASIC out of 5-V input voltage via multichannel IC (PMIC) LP87653-Q1. Despite this PMIC having four rails, phase #3 is unused and 1.1 V_A ("A" ⇒ analog; for sensitive loads) is generated via low-dropout regulator (LDO) on customer demand. LDO is used for 2.5 V_A and the 1.1 V_A is TPS745-Q1. Both LDOs are powered out of 3.3 V. To lower the losses of the LDO 1.1 V_A, two power resistors are added to the input.

Features

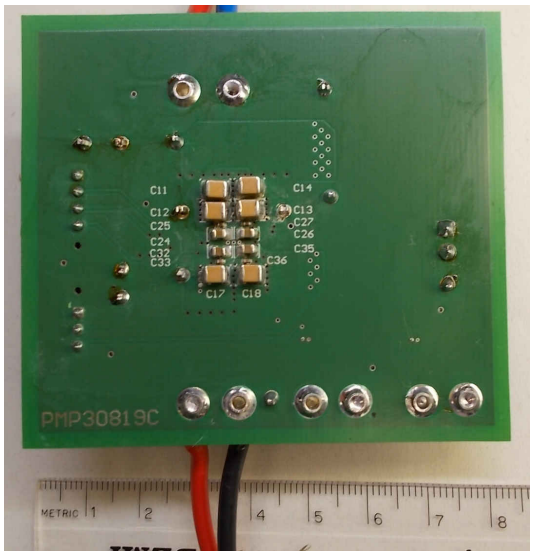
- Automotive power supply to energize a custom ASIC out of 5-V input
- I/O, to enable a LMK00804 level translator, for example
- Individual sequencing, first 3.3 V, then 2.5 V, and then 1.1 V (buck and LDO), the start-up of the 1.1-V outputs are delayed 11 ms
- Dual-stage differential input filter to attenuate switching frequency and harmonics as well as RF noise
- I²C bus for control and monitoring on the fly

Applications

- Mechanically scanning LIDAR



Top Photo



Bottom Photo

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1 Test Prerequisites

1.1 Voltage and Current Requirements

Table 1-1. Voltage and Current Requirements

Parameter	Specifications
Input Voltage Range	5 V
Output Voltage 1	1.1 V at 6 A_{MAX}
Output Voltage 2	3.3 V
Output Voltage 3	2.5 V at 0.4 A_{MAX}
Output Voltage 4	1.1 V at 0.4 A_{MAX}
Switching Frequency	2 MHz

1.2 Considerations

- Unless otherwise mentioned, electronic load were used for Output Voltage 1 and a variable resistor were used for Output Voltage 2
- All measurements were done with 5-V input voltage
- Switching frequency of prototype measured at 2.032 MHz

Note

The device itself is one time programmable (= OTP) – dedicated directly for customer application; this allows best performance, easy design and lowest part count just by customer specification. Beside comfortable control and monitoring via I^2C bus, this OTP feature basically enables a custom device for any individual design. Multiple designs could be covered with a single controller. For sensitive designs, this results in a copy protection as well.

By OTP file current at:

- Phase #0 and #1 providing 1.1 V_D is limited at 8.5 A
- Phase #2 providing 3.3 V is limited to 1.3 A

1.3 Dimensions

The size of the board is 73.7 mm × 66 mm. The four-layer board was manufactured with 35-µm copper thickness on each layer.

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2 Testing and Results

2.1 Efficiency Graphs

Output current were raised simultaneously for Output Voltage 1 (1.1 V) and Output Voltage 2 (3.3 V). Output Voltage 3 and Output Voltage 4 (= both LDOs) were left open with no load.

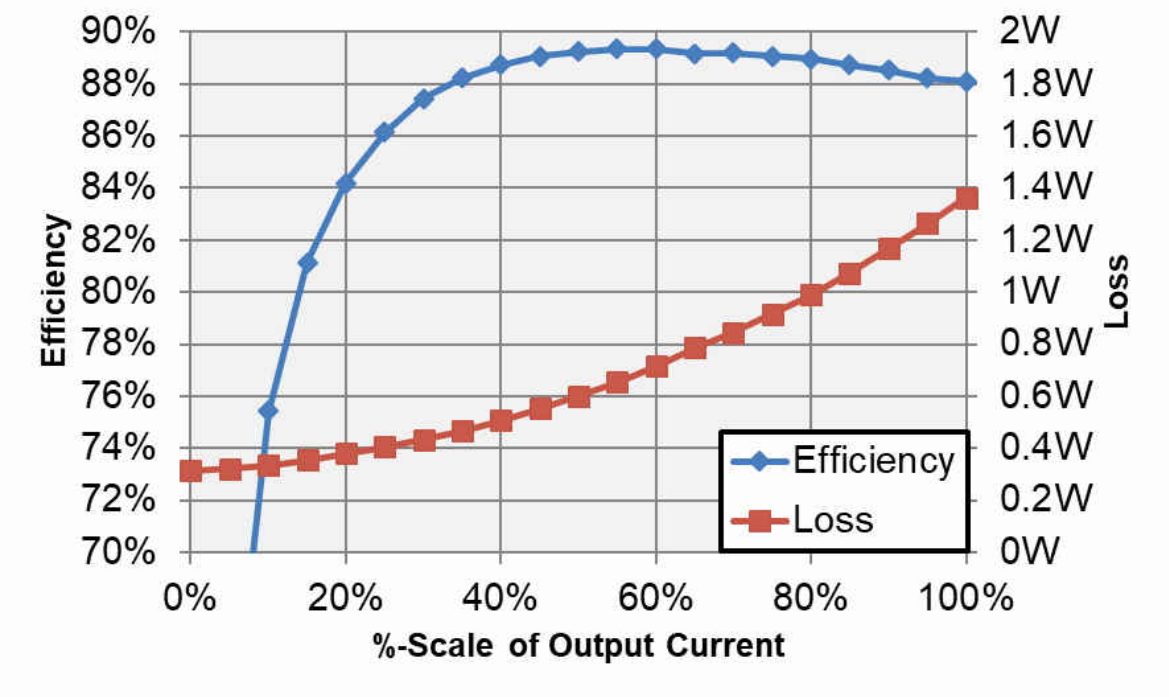

Figure 2-1. Efficiency and Loss vs Percentage of Output Current

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2.2 Load Regulation

2.2.1 Output Voltage 1 (1.1 V)

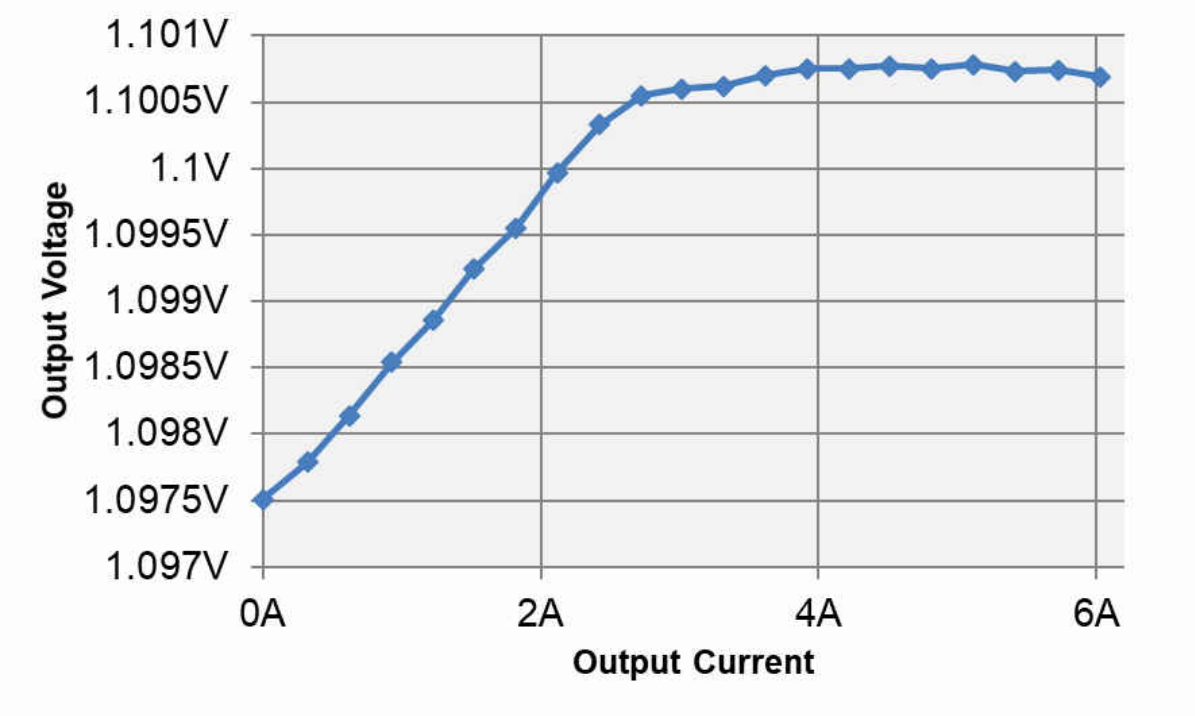

Figure 2-2. Load Regulation for Output Voltage 1

2.2.2 Output Voltage 2 (3.3 V)

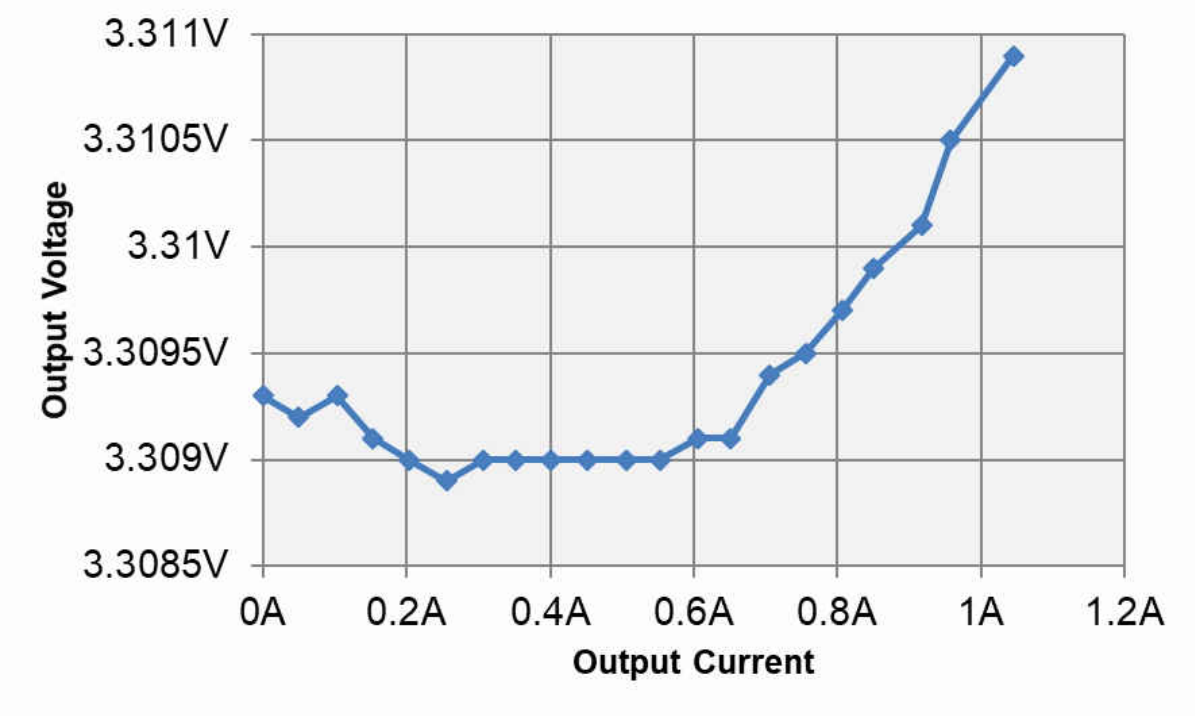

Figure 2-3. Load Regulation for Output Voltage 2

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2.3 Thermal Images

Table 2-1 lists the used output currents for Figure 2-4.

Table 2-1. Output Currents Used for Thermal Image

	Voltage	Current
Output Voltage 1	1.1 V	6 A
Output Voltage 2	3.3 V	0.3 A
Output Voltage 3	2.5 V	0.3 A
Output Voltage 4	1.1 V	0.4 A

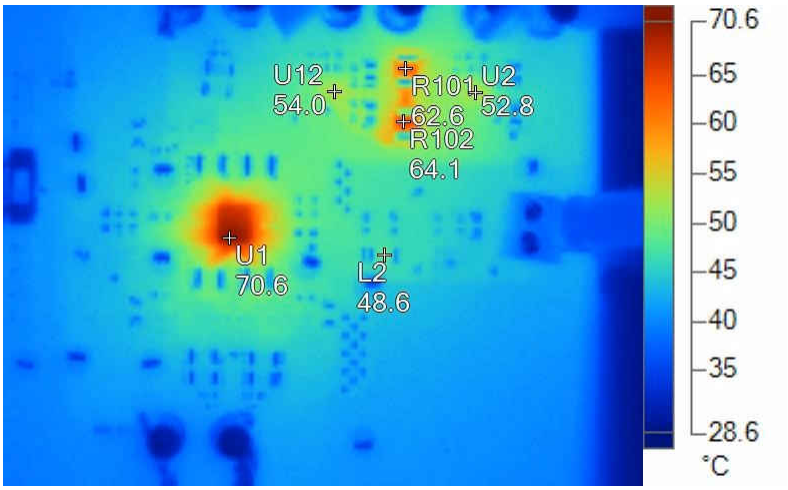

Figure 2-4. Thermal Image

Name	Temperature
L2	48.6°C
R101	62.6°C
R102	64.1°C
U1	70.6°C
U12	54.0°C
U2	52.8°C

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2.4 Bode Plots

2.4.1 Output Voltage 1 (1.1 V at 6 A)

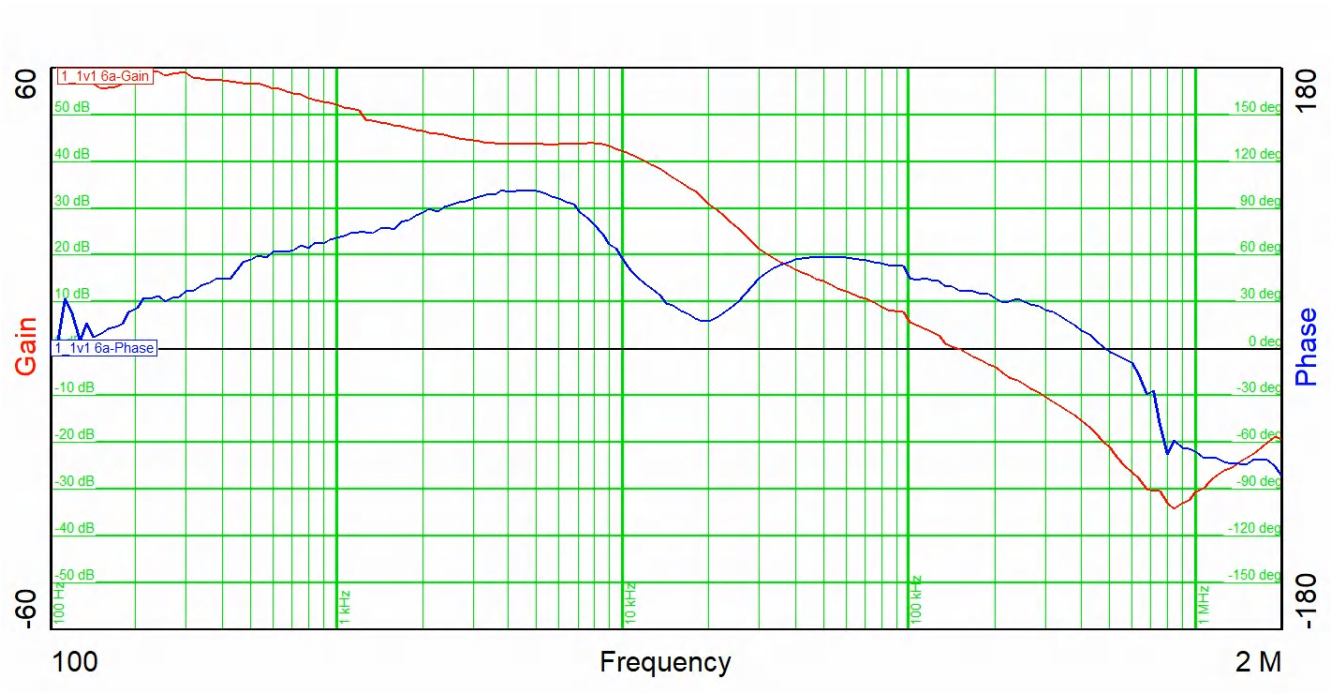

Figure 2-5. Bode Plot for Output Voltage 1

Input Voltage	5 V
Bandwidth (kHz)	148
Phase margin	37.9°
Slope (20 dB / decade)	–0.95
Gain margin (dB)	–20.3
Slope (20 dB / decade)	–3.1
Freq (kHz)	488

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2.4.2 Output Voltage 2 (3.3 V at 1 A)

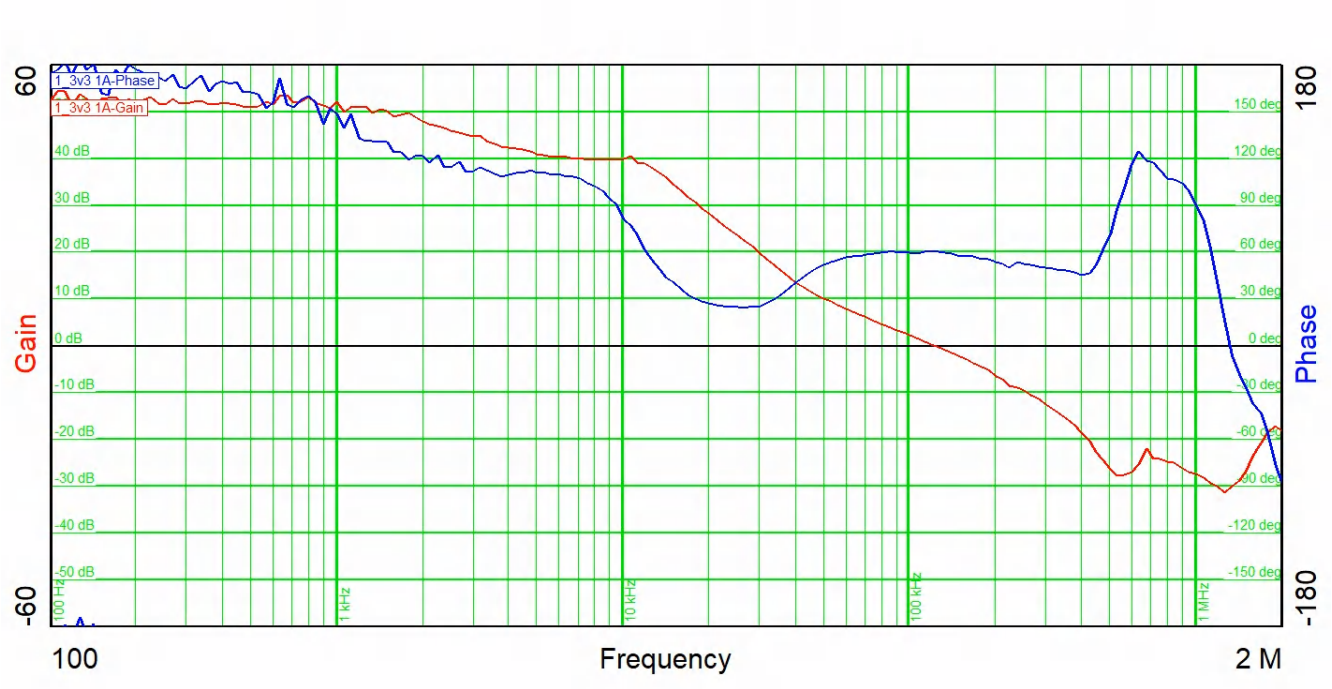

Figure 2-6. Bode Plot for Output Voltage 2

Input Voltage	5 V
Bandwidth (kHz)	123
Phase margin	60°
Slope (20 dB / decade)	–1.22
Gain margin (dB)	–30.4
Slope (20 dB / decade)	–2.9
Freq (kHz)	1320

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3 Waveforms

3.1 Switching

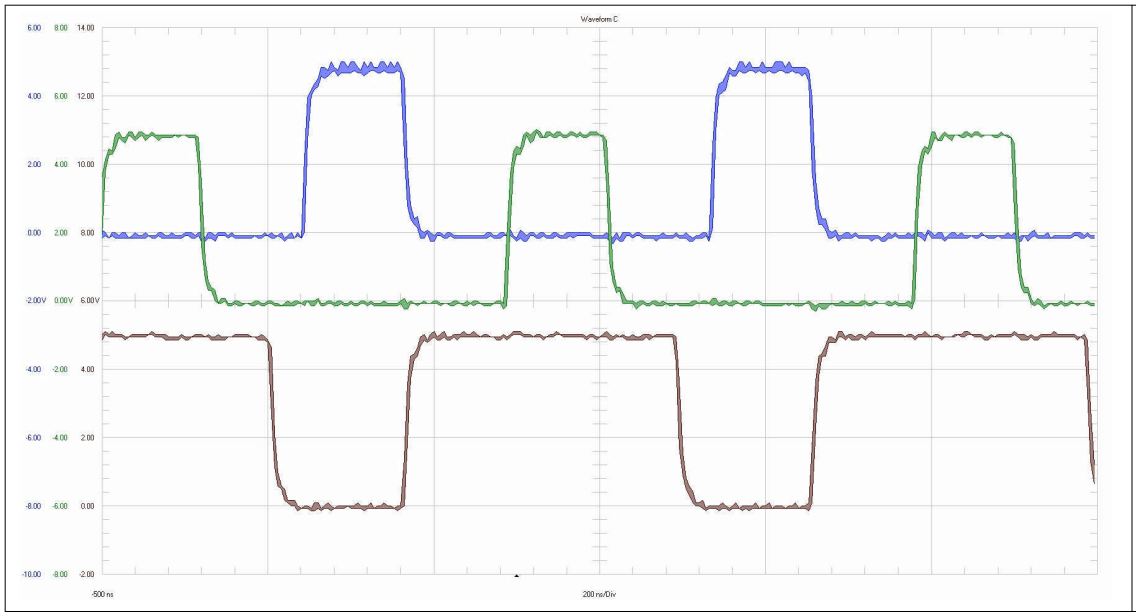

Figure 3-1. Switching Overview

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3.1.1 Output Voltage 1 (1.1 V at 6 A)

3.1.1.1 Test Point TP3 (Pin SW_B0)

Test point TP3 is shown in the *PMP30819 Schematic*.

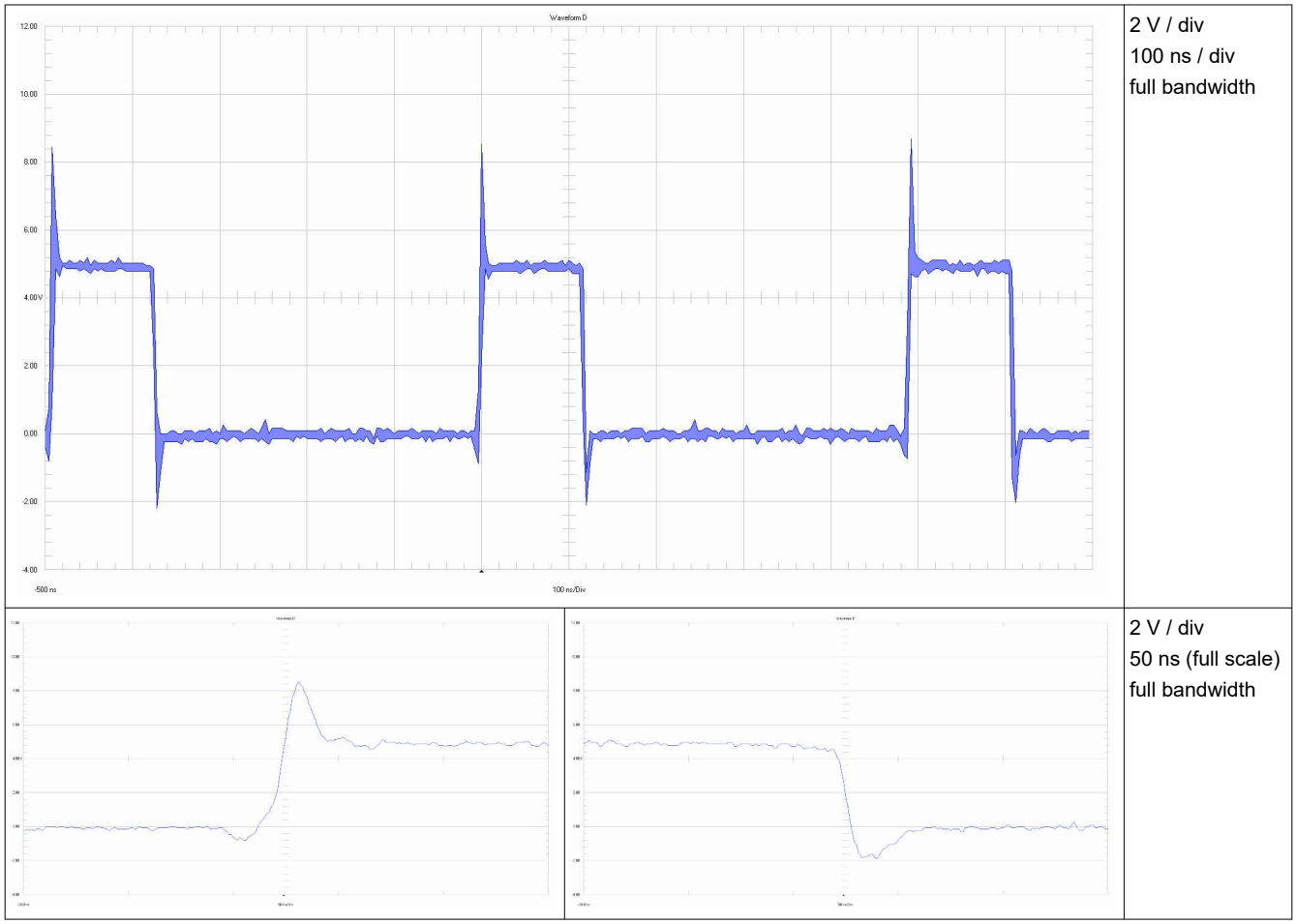

Figure 3-2. Switch Node 1.1 V_{OUT} (at 6 A) Switch Node #0 (TP3)

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3.1.1.2 Test Point TP9 (Pin SW_B1)

Test point TP9 is shown in the *PMP30819 Schematic*.

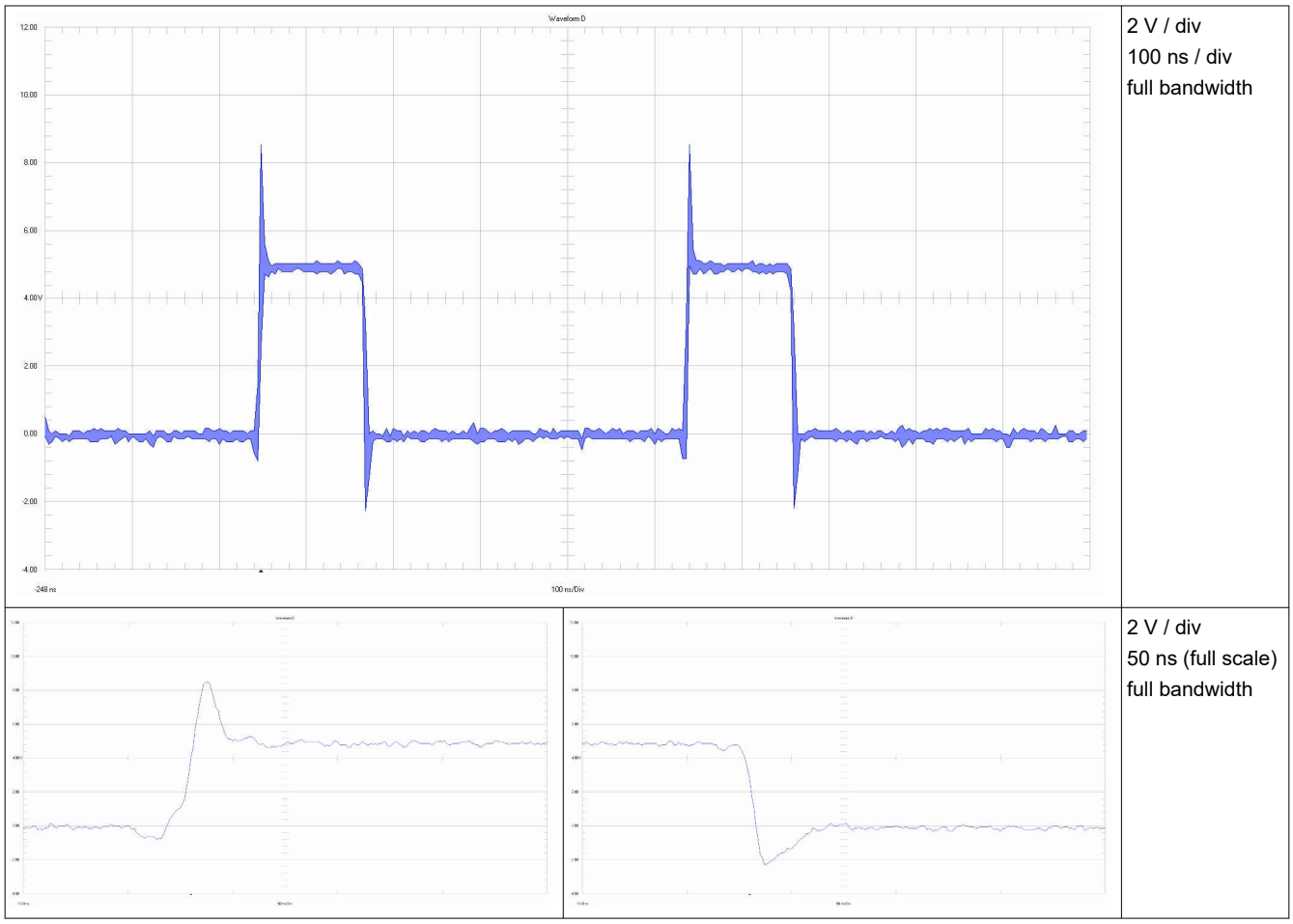

Figure 3-3. Switch Node 1.1 V (at 6 A) #1 (TP9)

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3.1.2 Output Voltage 2 (3.3 V at 1 A)

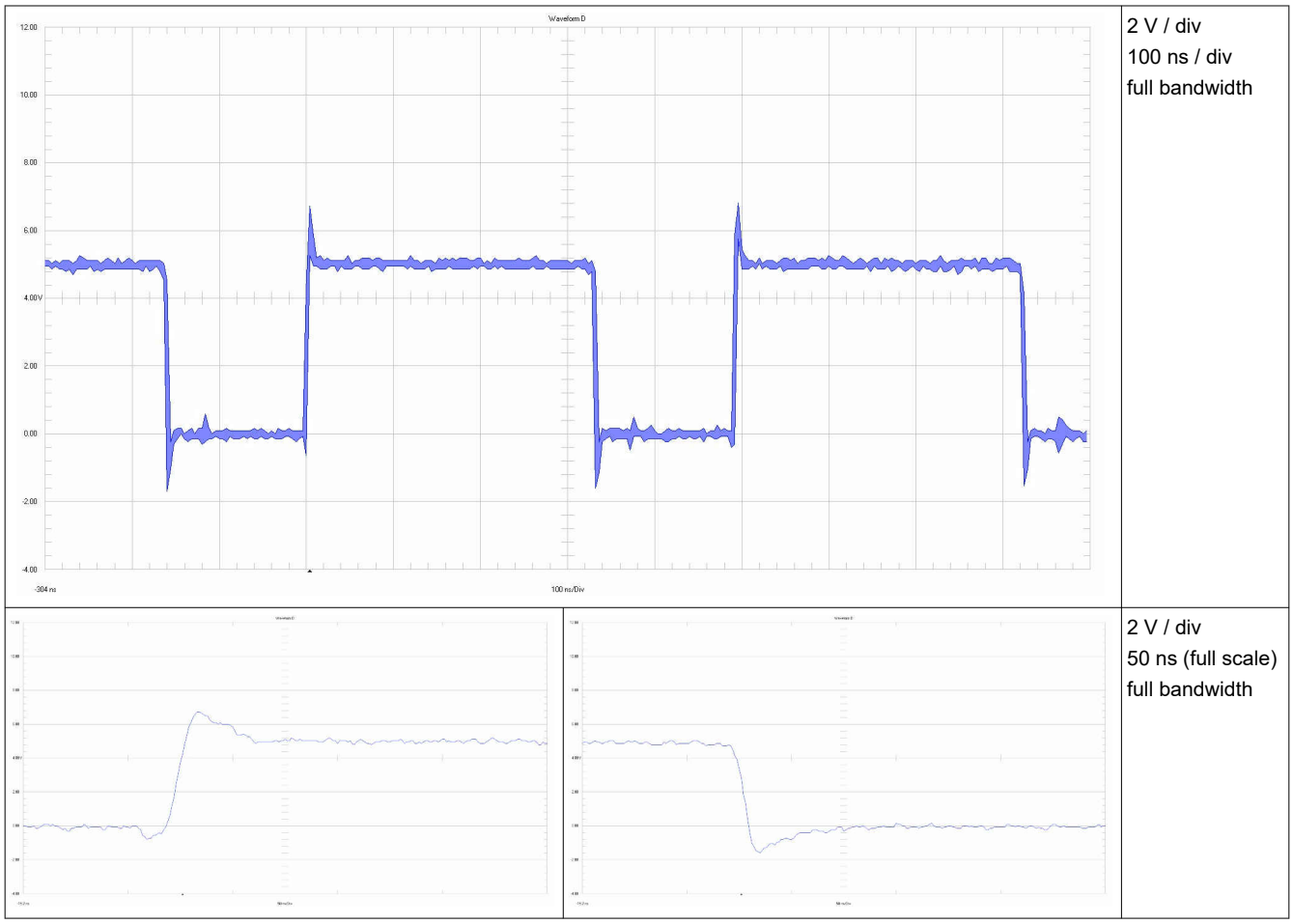

Figure 3-4. Switch Node #2 (TP11)

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3.2 Output Voltage Ripple

3.2.1 V_{OUT1} (1.1 V_D at 6 A) and V_{OUT2} (3.3 V at 1 A)

Both waveforms in Figure 3-5 were measured separately with low impedance probe.

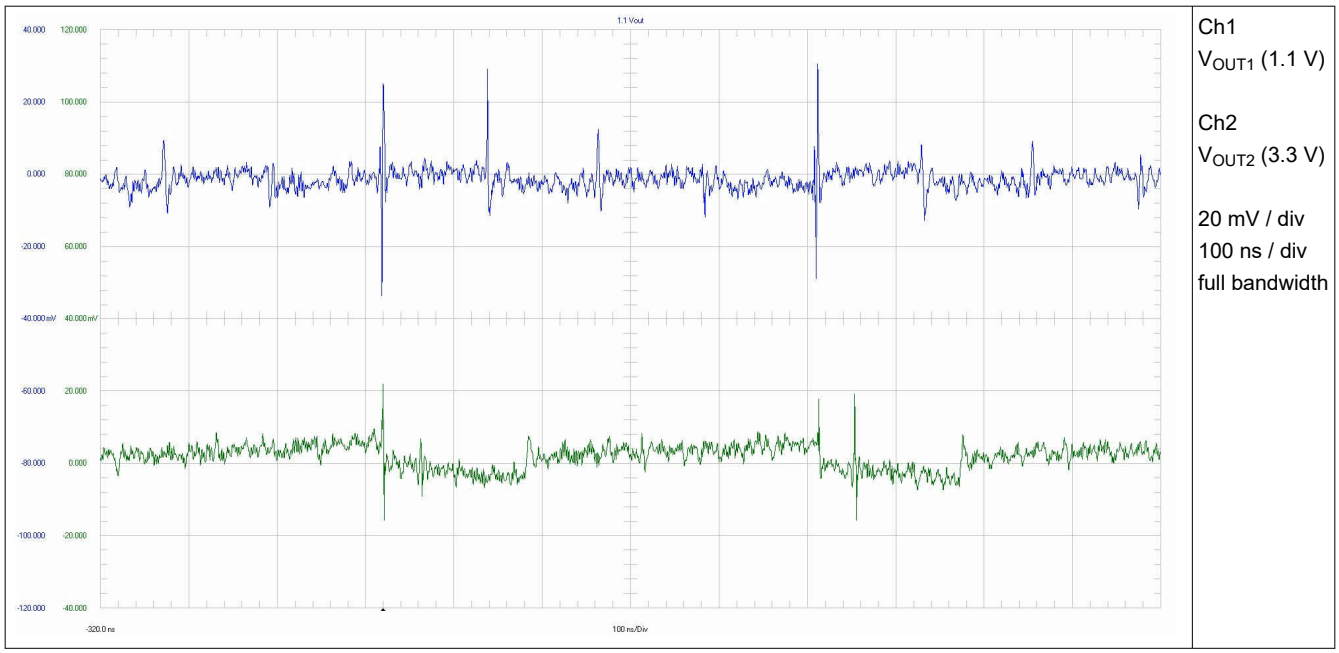

Figure 3-5. Output Voltage Ripple (V_{OUT1} and V_{OUT2})

3.2.2 V_{OUT3} (2.5 V at 0.3 A) and V_{OUT4} (1.1 V at 0.4 A)

Both waveforms in Figure 3-6 were measured separately with low impedance probe.

V_{OUT2} (3.3 V) were charged with 0.1 A during this measurement.

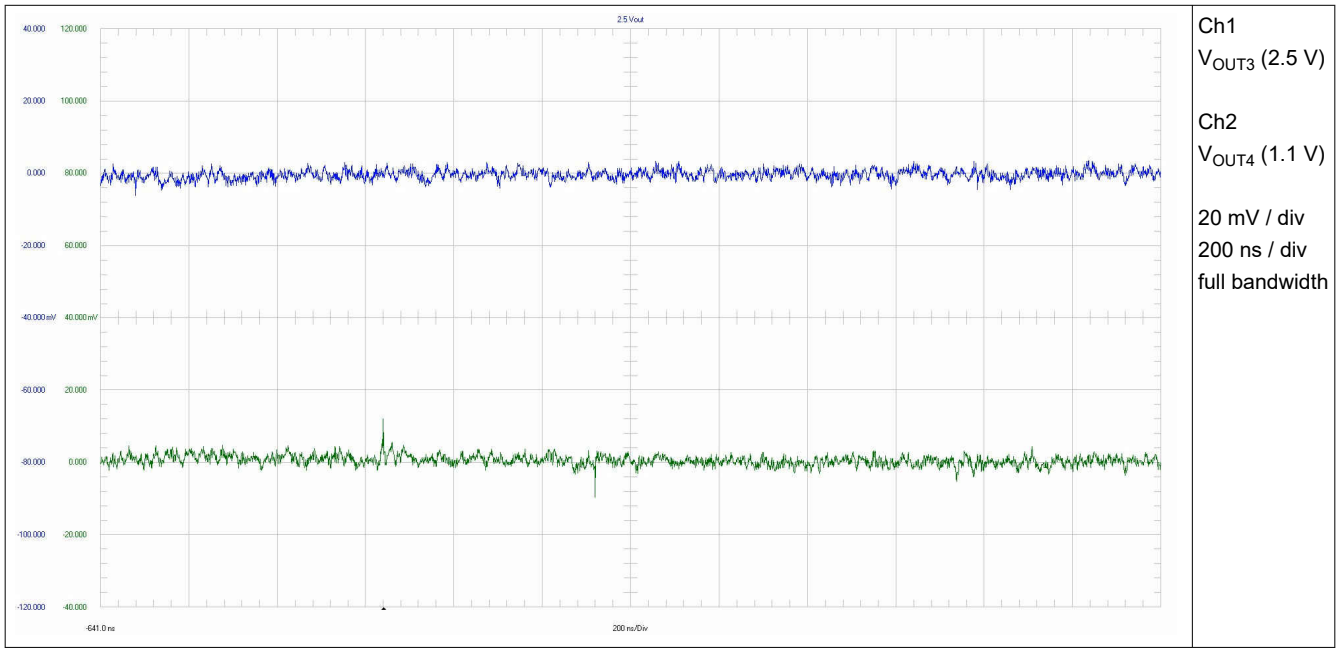

Figure 3-6. Output Voltage Ripple (V_{OUT3} and V_{OUT4})

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3.3 Input Voltage Ripple

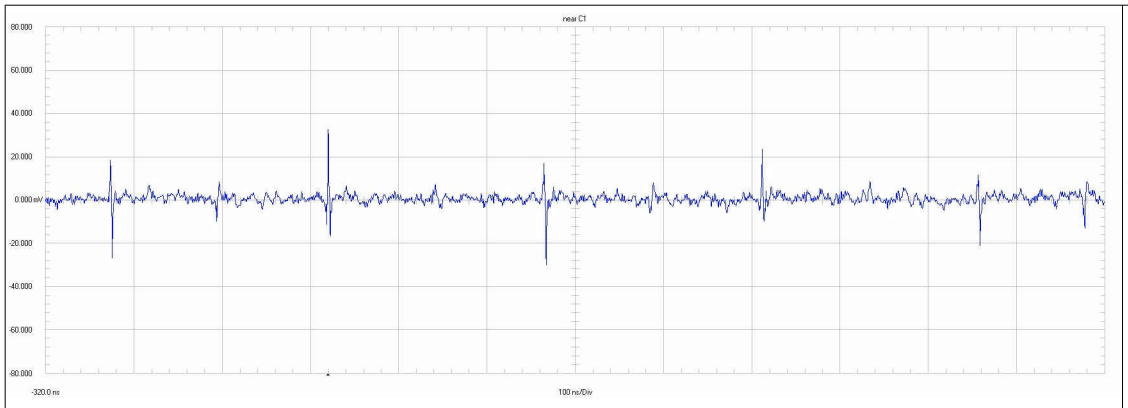
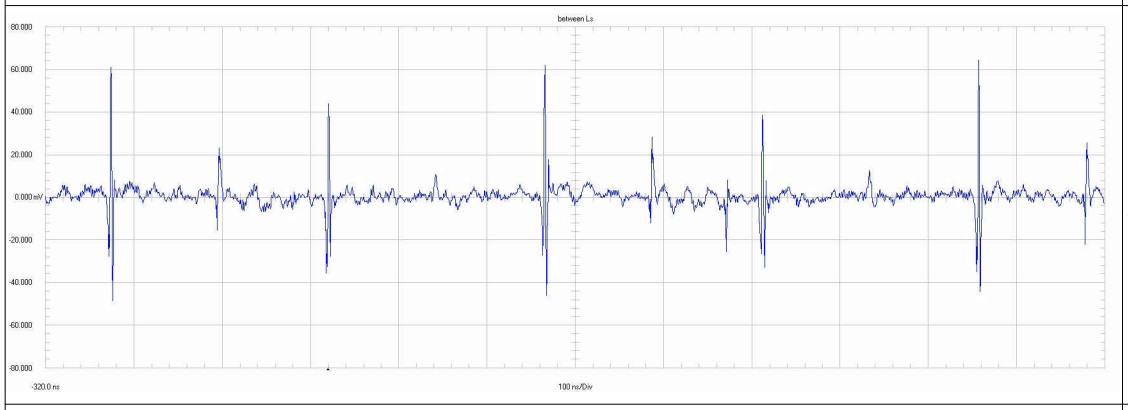
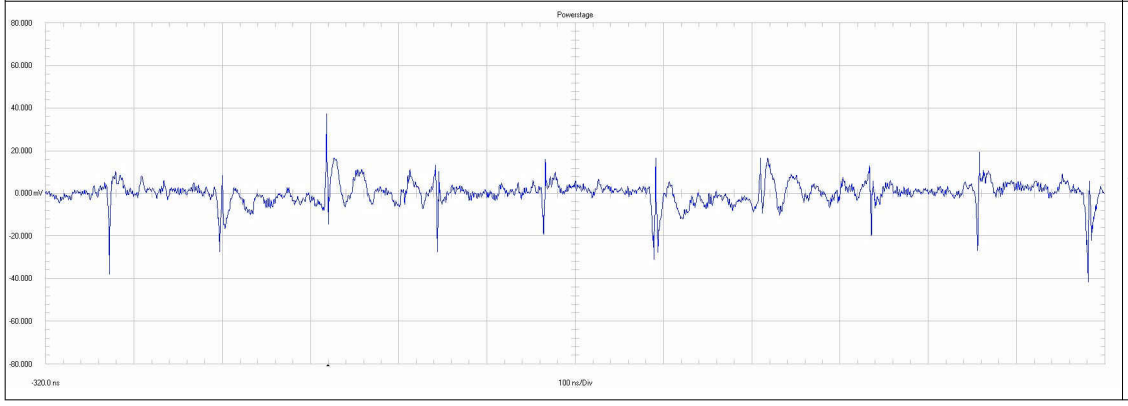
	V_{IN} measured near C1 20 mV / div 100 ns / div full bandwidth
	V_{IN} measured between L1 and L2 (to GND) 20 mV / div 100 ns / div full bandwidth
	V_{IN} measured near TP1 (to GND) 20 mV / div 100 ns / div full bandwidth

Figure 3-7. Input Voltage Ripple Measured on Different Locations

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3.4 Load Transients

3.4.1 Switching Load on Output Voltage 1 (1.1 V_D)

Load switches from 0.61 A to 6.07 A (**= 90% transient**) with a frequency of 200 Hz.

3.4.1.1 Output Voltage 1 (V_{OUT1})

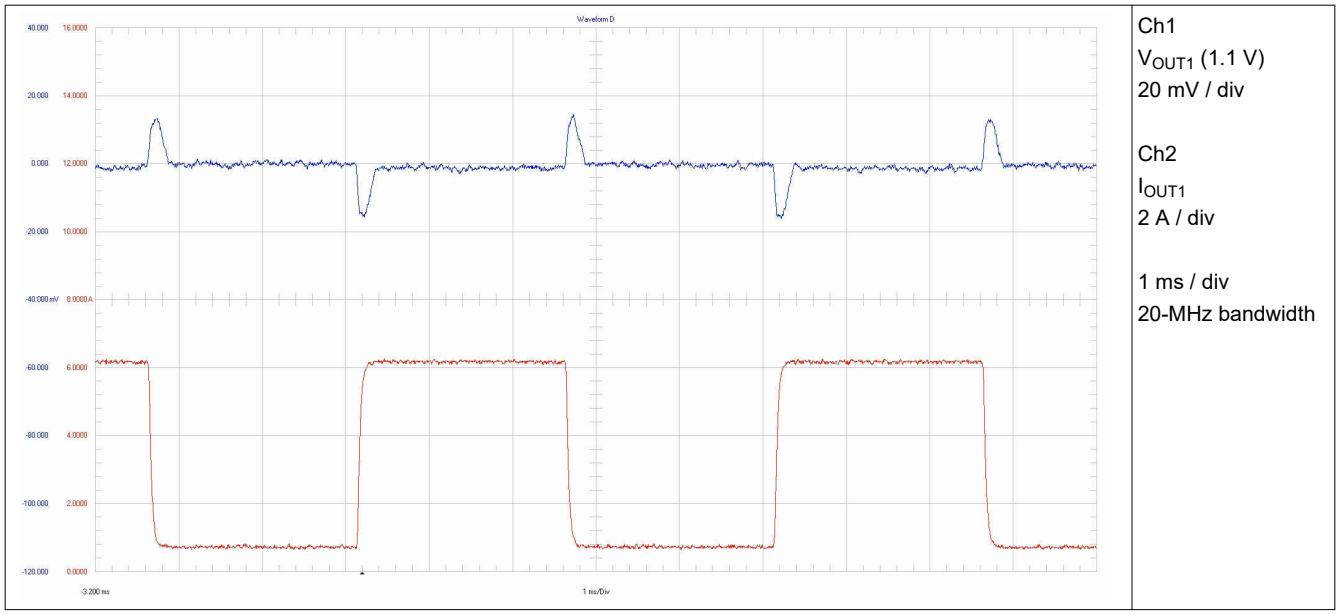

Figure 3-8. Load Transient V_{OUT1} ⇒ V_{OUT1}

3.4.1.2 Cross Talking on V_{OUT2} (3.3 V)

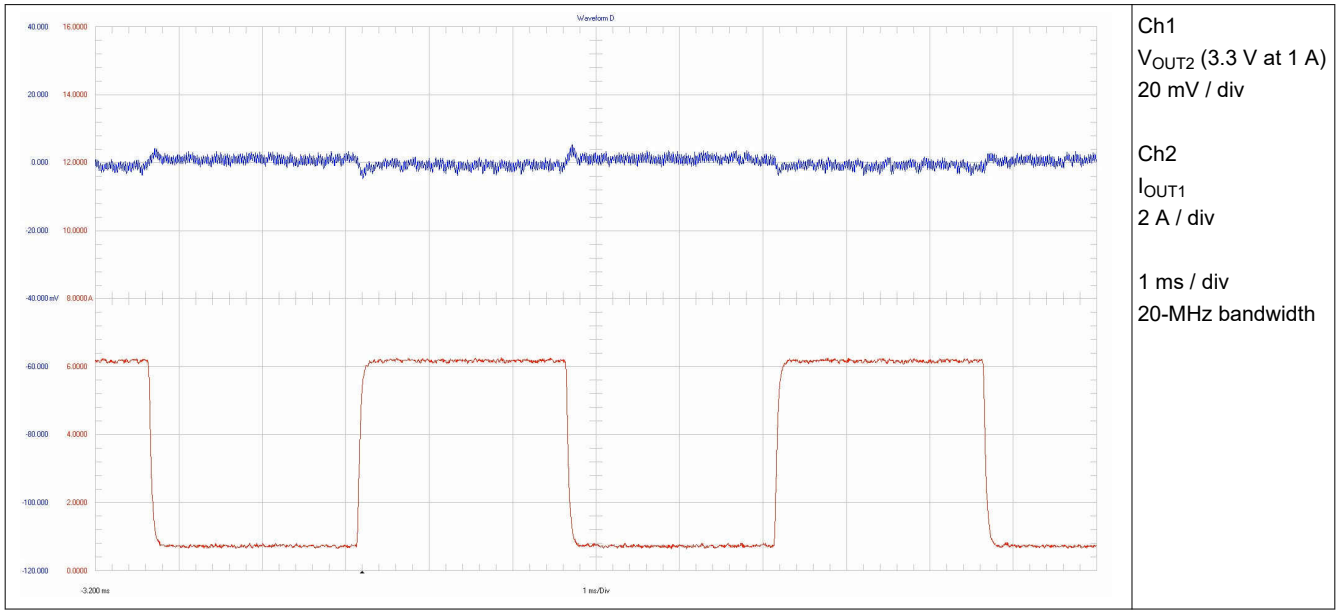

Figure 3-9. Load Transient V_{OUT1} ⇒ Cross Talking V_{OUT2}

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3.4.2 Switching Load on Output Voltage 2 (3.3 V)

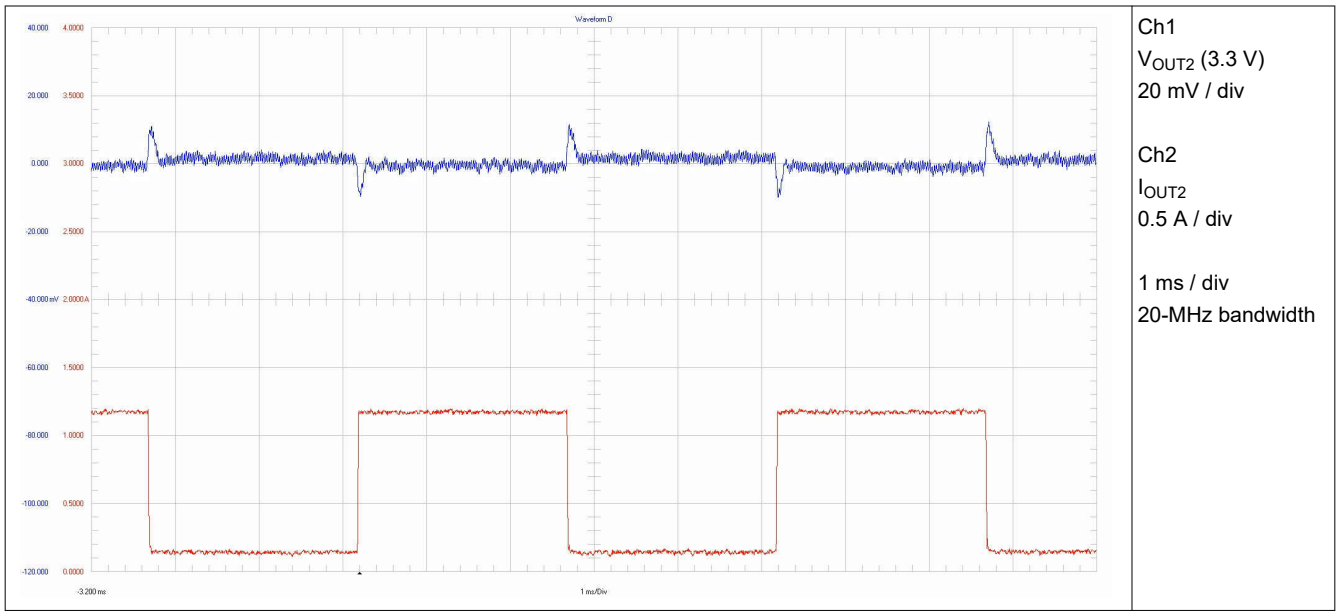

Figure 3-10. Load Transient V_{OUT2} ⇒ V_{OUT2}

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3.5 Start-Up Sequence

3.5.1 Hot Plug-In

For the waveform in Figure 3-11 for V_{OUT1} a resistor was used instead of electronic load (see Considerations).

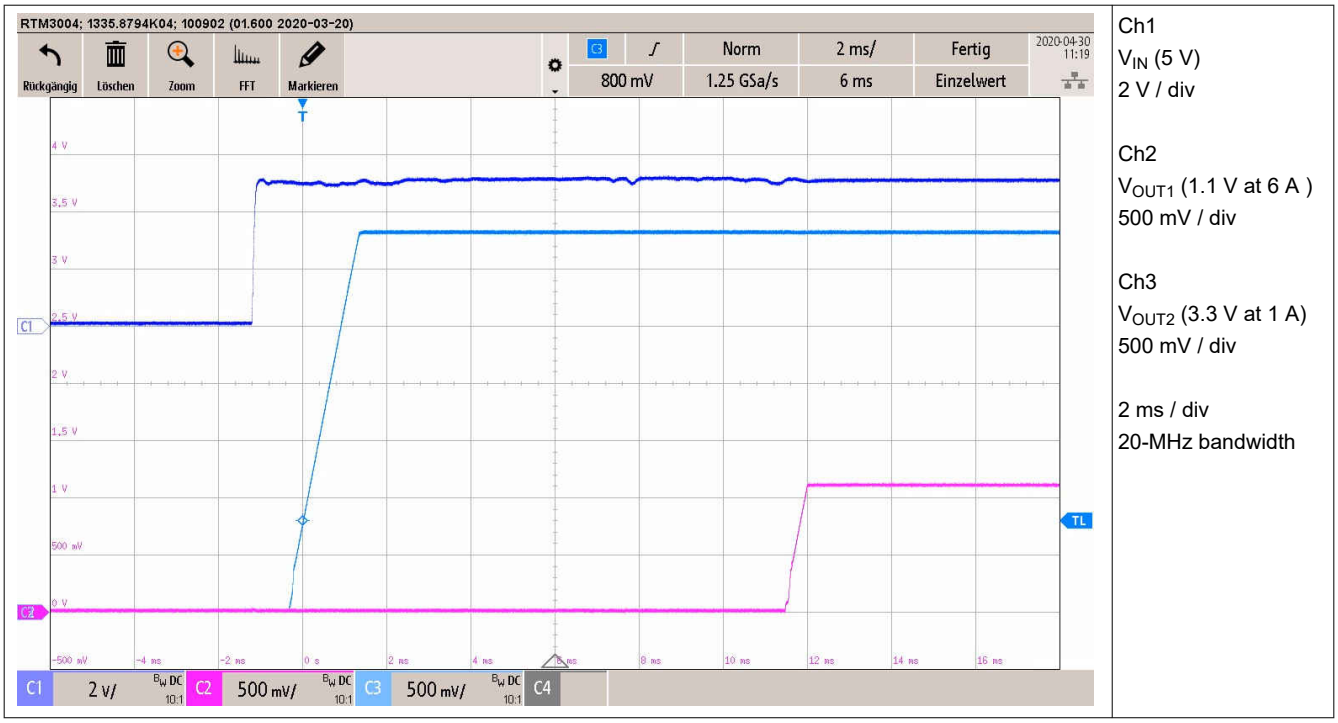

Figure 3-11. Connecting Power Supply, Hot Plug-In 5 V_{IN}; 3.3 V and 1.1 V_D

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3.5.2 Enable with Switch S1

3.5.2.1 All Traces

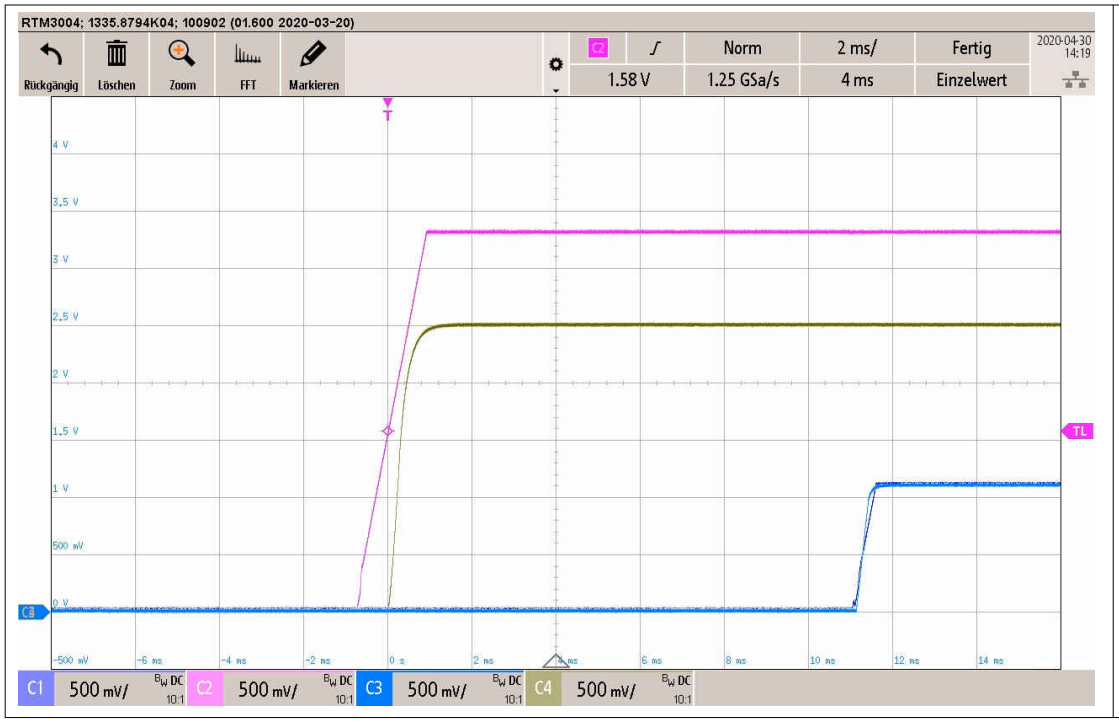

Figure 3-12. Enable With Switch S1; 3.3 V_{OUT}, 2.5 V_{OUT}, Then After 11 ms Both are 1.1 V_{OUT}

Note

Both 1.1 V_{OUT} traces have almost identical shape. In Section 3.5.2.3 and Section 3.5.2.2 these traces are displayed separately.

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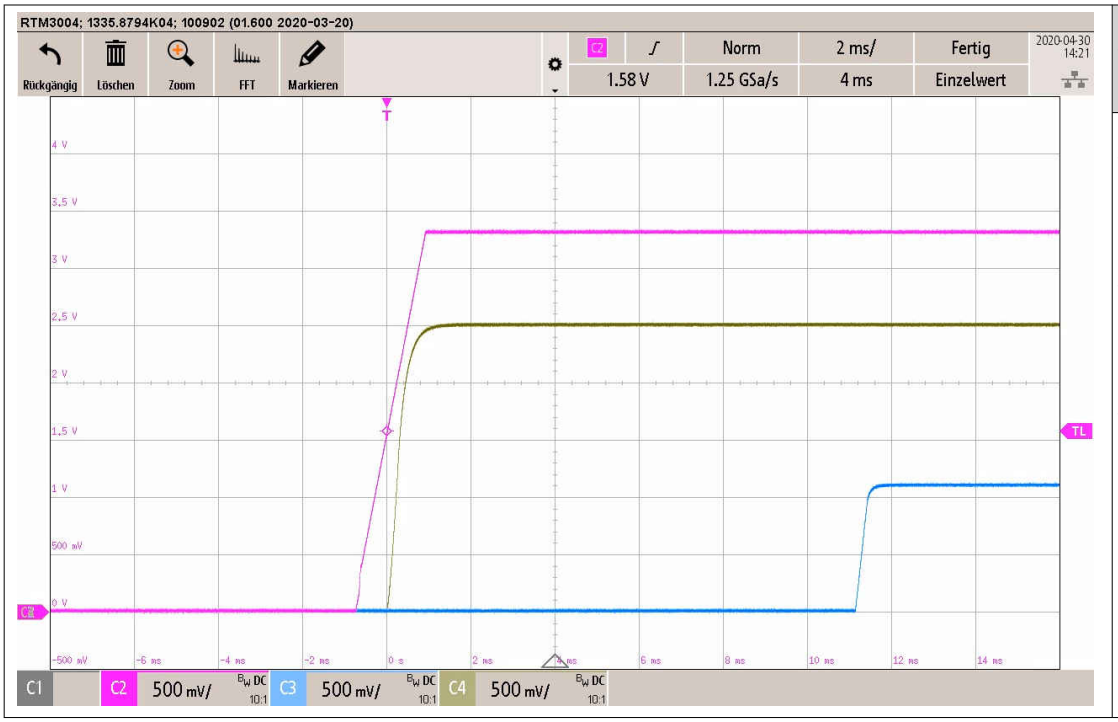
3.5.2.2 Without V_{OUT1}



Ch1
V_{OUT1} (1.1 V at 2 A)
not displayed

Ch2
V_{OUT2} (3.3 V at 0.1 A)
500 mV / div

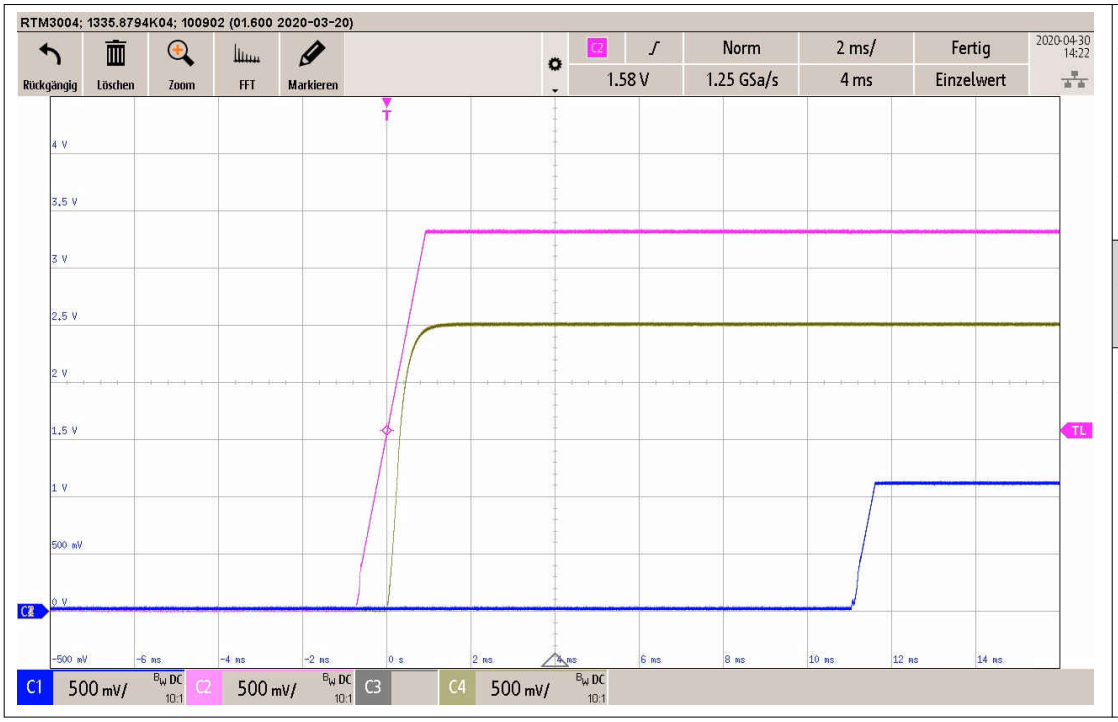
Ch3
V_{OUT4} (1.1 V at 0.4 A)
500 mV / div

Ch4
V_{OUT3} (2.5 V at 0.3 A)
500 mV / div

2 ms / div
20-MHz bandwidth

Figure 3-13. Enable With Switch S1; 3.3 V_{OUT}, 2.5 V_{OUT} and 1.1 V_{OUT} at 0.4 A

3.5.2.3 Without V_{OUT4}



Ch1
V_{OUT1} (1.1 V at 2 A)
500 mV / div

Ch2
V_{OUT2} (3.3 V at 0.1 A)
500 mV / div

Ch3
V_{OUT4} (1.1 V at 0.4 A)
not displayed

Ch4
V_{OUT3} (2.5 V at 0.3 A)
500 mV / div

2 ms / div
20-MHz bandwidth

Figure 3-14. Enable With Switch S1; 3.3 V_{OUT}, 2.5 V_{OUT}, 1.1 V_{OUT} at 2 A

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3.6 Shutdown Sequence

3.6.1 Hot Plug Off

For the waveform in Figure 3-15 for V_{OUT1}, a resistor was used instead of electronic load (see Considerations).

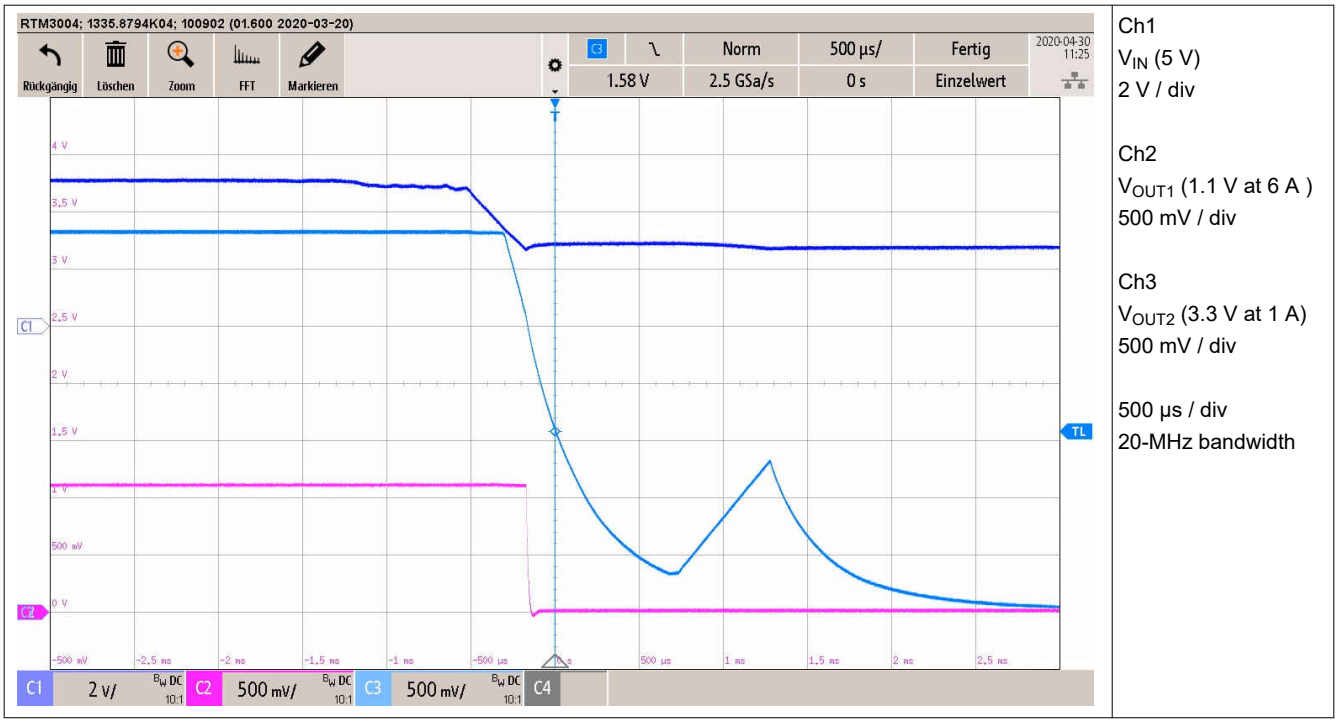

Figure 3-15. Disconnecting Power Supply, Hot Plug Off

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3.6.2 Disable With Switch S1

3.6.2.1 All Traces

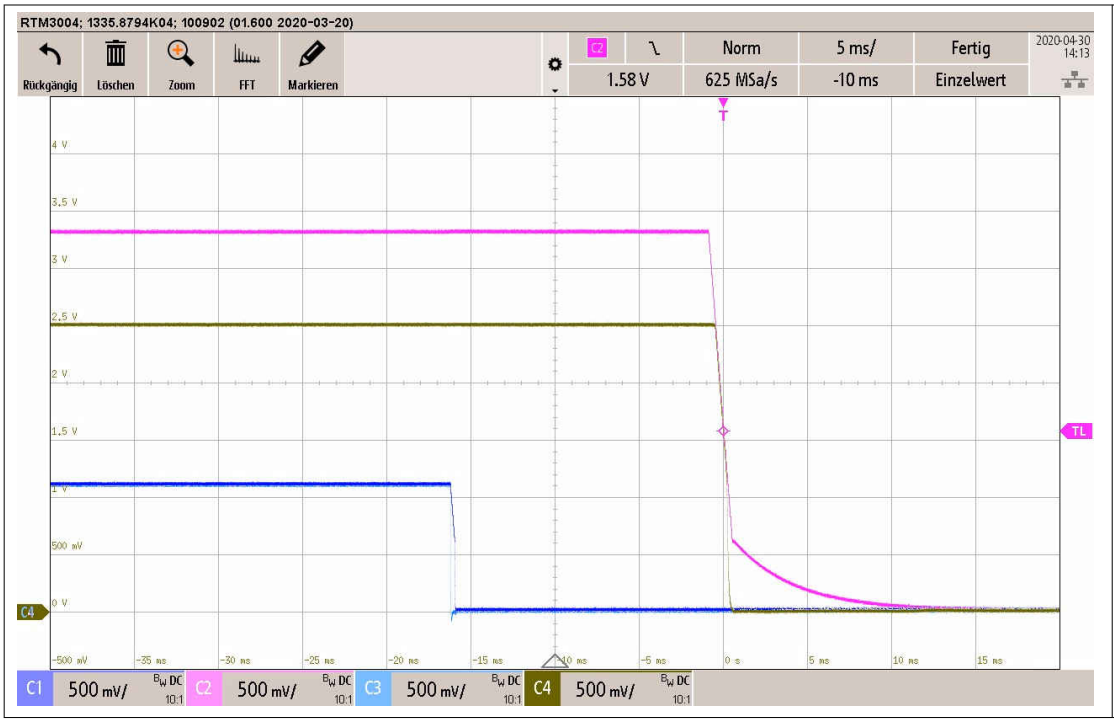

Figure 3-16. Disable With Switch S1 (all Traces)

Note

Both 1.1 V_{OUT} traces have almost identical shape. In Section 3.6.2.2 and Section 3.6.2.3 these traces are displayed separately.

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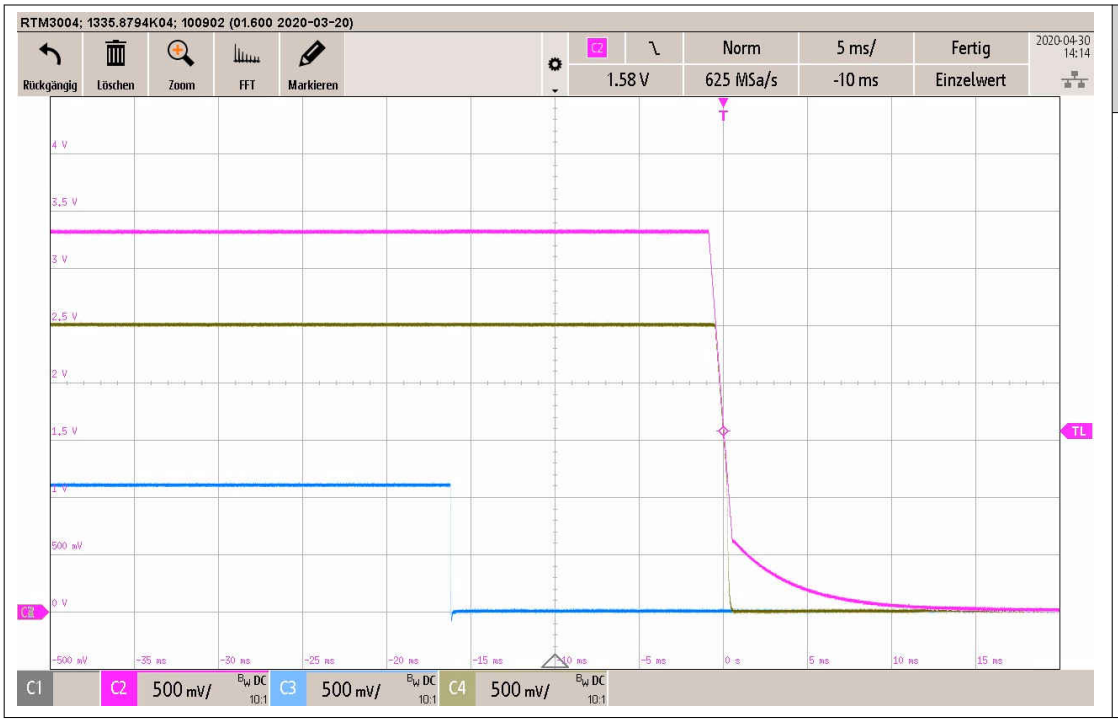
3.6.2.2 Without V_{OUT1}



Ch1
V_{OUT1} (1.1 V at 2 A)
not displayed

Ch2
V_{OUT2} (3.3 V at 0.1 A)
500 mV / div

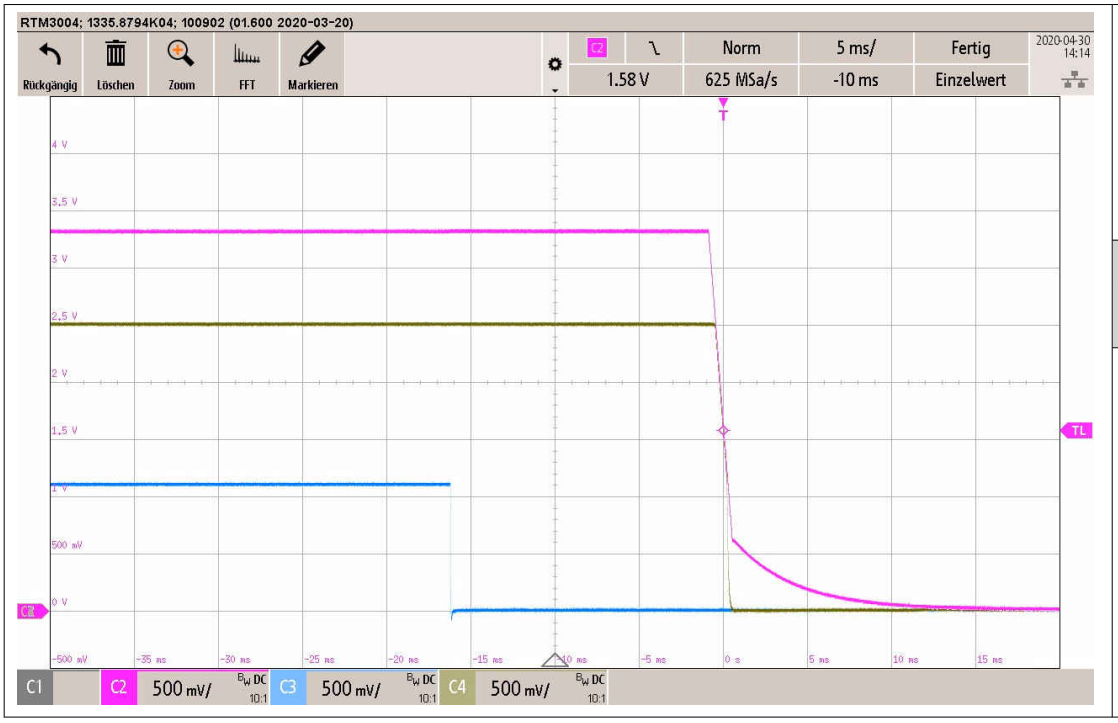
Ch3
V_{OUT4} (1.1 V at 0.4 A)
500 mV / div

Ch4
V_{OUT3} (2.5 V at 0.3 A)
500 mV / div

5 ms / div
20-MHz bandwidth

Figure 3-17. Disable With Switch S1 With V_{OUT4}

3.6.2.3 Without V_{OUT4}



Ch1
V_{OUT1} (1.1 V at 2 A)
500 mV / div

Ch2
V_{OUT2} (3.3 V at 0.1 A)
500 mV / div

Ch3
V_{OUT4} (1.1 V at 0.4 A)
not displayed

Ch4
V_{OUT3} (2.5 V at 0.3 A)
500 mV / div

5 ms / div
20-MHz bandwidth

Figure 3-18. Disable With Switch S1 With V_{OUT1}

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