Test Report: PMP23223

Smart Isolated Gate Driver With Bias Supply Reference Design

Description

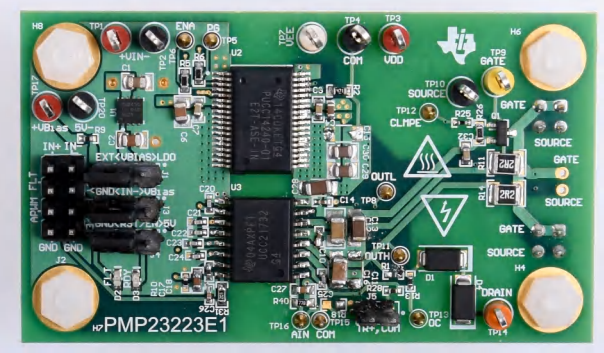
This reference design demonstrates the combination of a UCC21732 gate driver with a UCC14xxx series bias supply. This board can be used to drive a variety of power switches, including connecting directly to a Wolfspeed SiC FET module. This board can serve as either a high- or low-side driver, or it can be tested with a capacitive dummy load.

Features

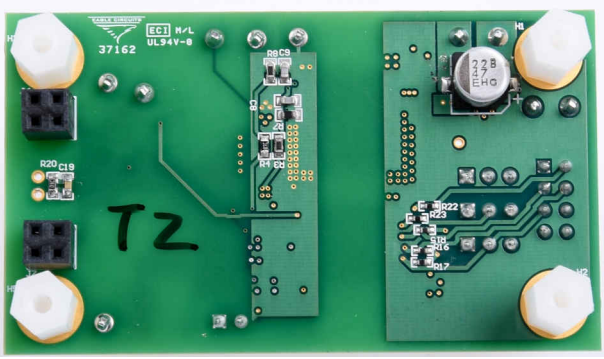
- LDO on the primary side allows the board to be tested with only one bench supply
- Analog temperature sense across the isolation barrier
- Internal two-level turn-off
- External Miller clamp
- Adjustable DESAT protection
- Resistor programmable bias supply voltage
- Suitable for automotive applications
- 10-A source and sink
- > 1.5-W bias supply power

Applications

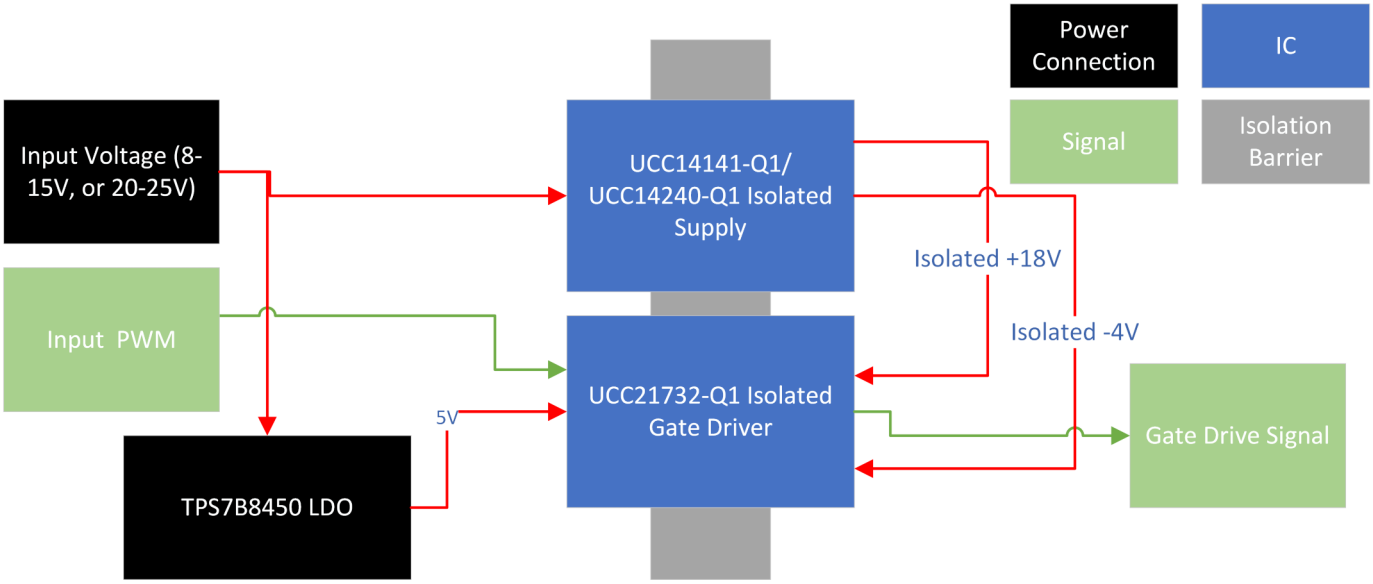
- Traction inverter-high voltage
- Traction inverter-low voltage
- Automotive HVAC compressor module
- On-board (OBC) and wireless charger
- String inverter
- Automotive interior heater module



PMP23223 Top Photo



PMP23223 Bottom Photo



Block Diagram

1 Test Prerequisites

1.1 Voltage and Current Requirements

Table 1-1. Voltage and Current Requirements

Parameter	Specifications
VIN input voltage	21 V to 27 V, 500 mA
PWM input	3.3 V to 5 V PWM input

1.2 Required Equipment

- 24-V bench supply
- Function generator
- Oscilloscope

1.3 Test Setup

Testing is performed with 24-V input on V_{IN}, and PWM applied to IN+. VEE is tied to the primary side GND, and all signals were probed relative to primary side GND. Jumper J1 is connected from pin 1-2, J3 is connected from pin 2-3, and J4 is connected from pin 1-2. All testing in this report was done with a 100-nF capacitive load populated on C19.

2 Testing and Results

2.1 UCC14240 Power-Up Sequence

Figure 2-1 shows the typical start-up of the bias supply. The input voltage (Green) drives the enable signal (Blue) through an LDO. The purple trace shows the VDD voltage, and the blue trace shows the COM voltage, both relative to VEE. The red trace shows the VDD voltage relative to COM, calculated from C2 and C3.

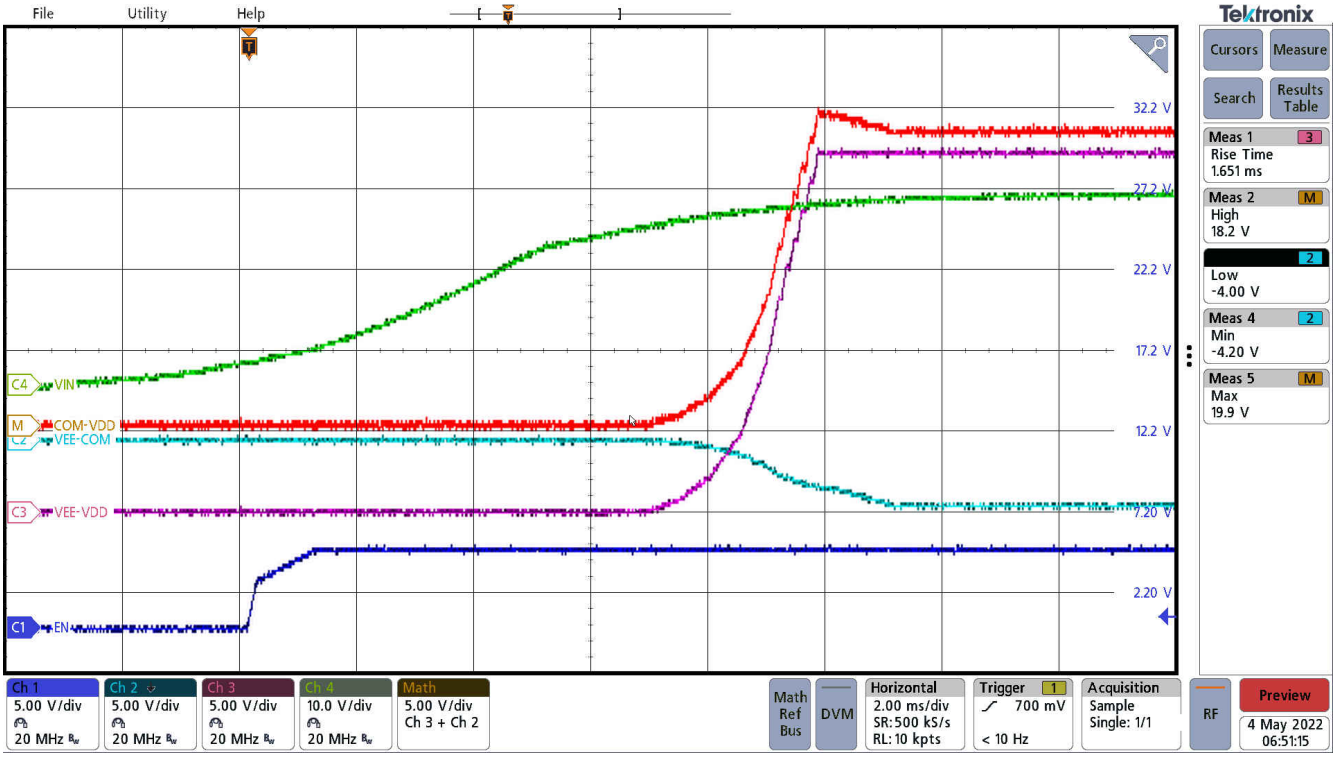


Figure 2-1. Power-Up Sequence

2.2 UCC14240 Output Ripple

Output ripple waveforms are shown in the following figures.

The green waveform in Figure 2-2 shows the VEE-COM rail ripple while the output is switching a 100-nF capacitive load at 1 kHz. The peak-to-peak ripple is 252 mV, which is 6.3%.

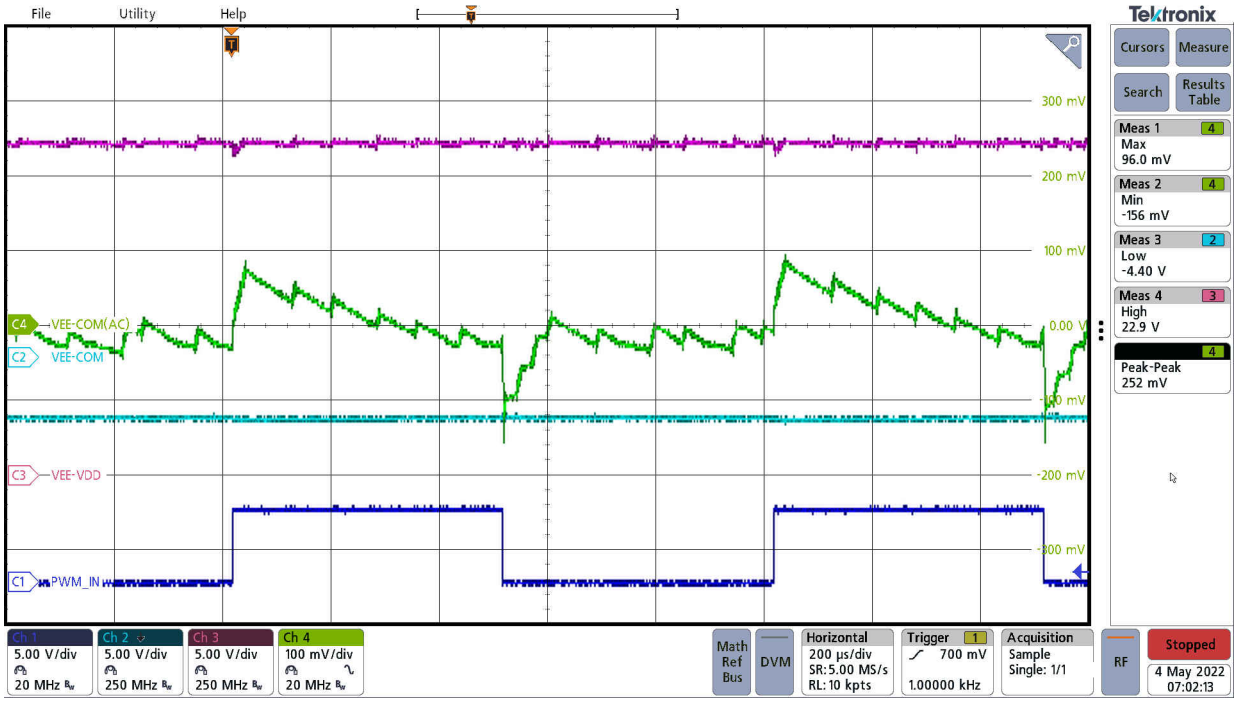


Figure 2-2. VEE-COM Switching 100-nF Load at 1 kHz

The green waveform in Figure 2-3 shows the VEE-VDD rail ripple while the output is switching a 100-nF capacitive load at 1 kHz. The peak to peak ripple is 865 mV, which is 3.9%.

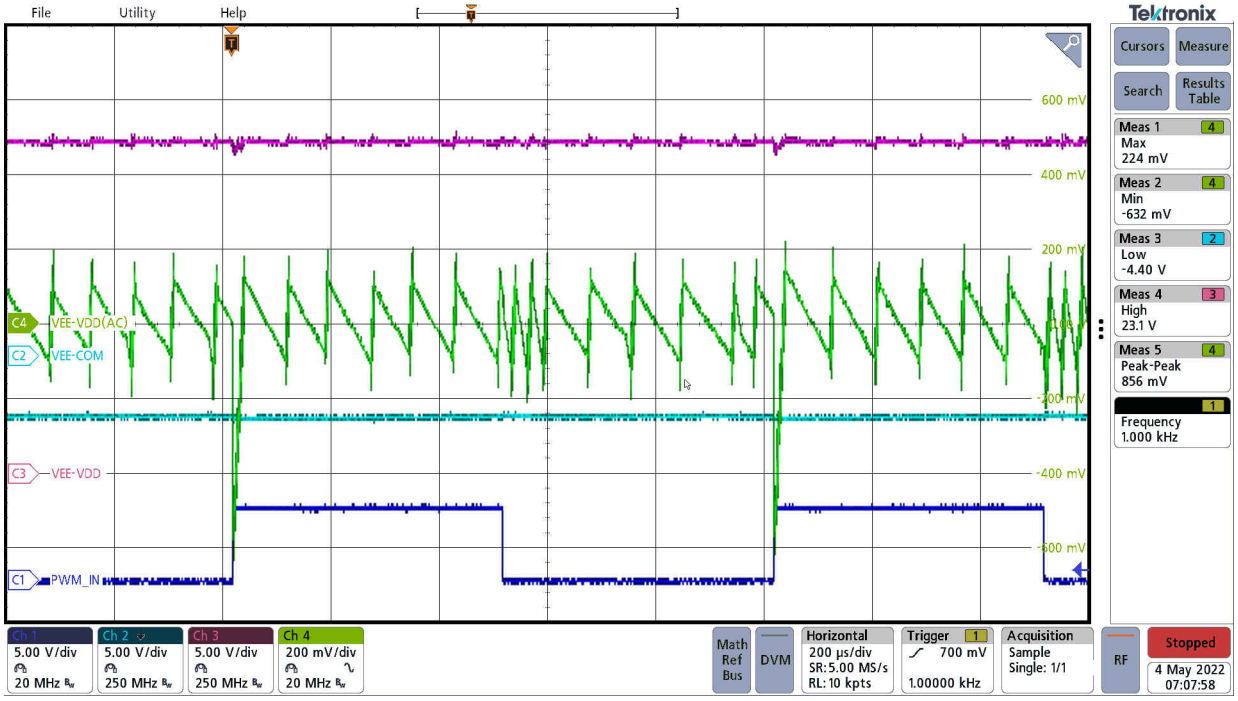


Figure 2-3. VEE-VDD Switching 100-nF Load at 1 kHz

The green waveform in Figure 2-4 shows the VEE-COM rail ripple while the output is switching a 100-nF capacitive load at 35 kHz. The peak to peak ripple is 232 mV, which is 5.8%.

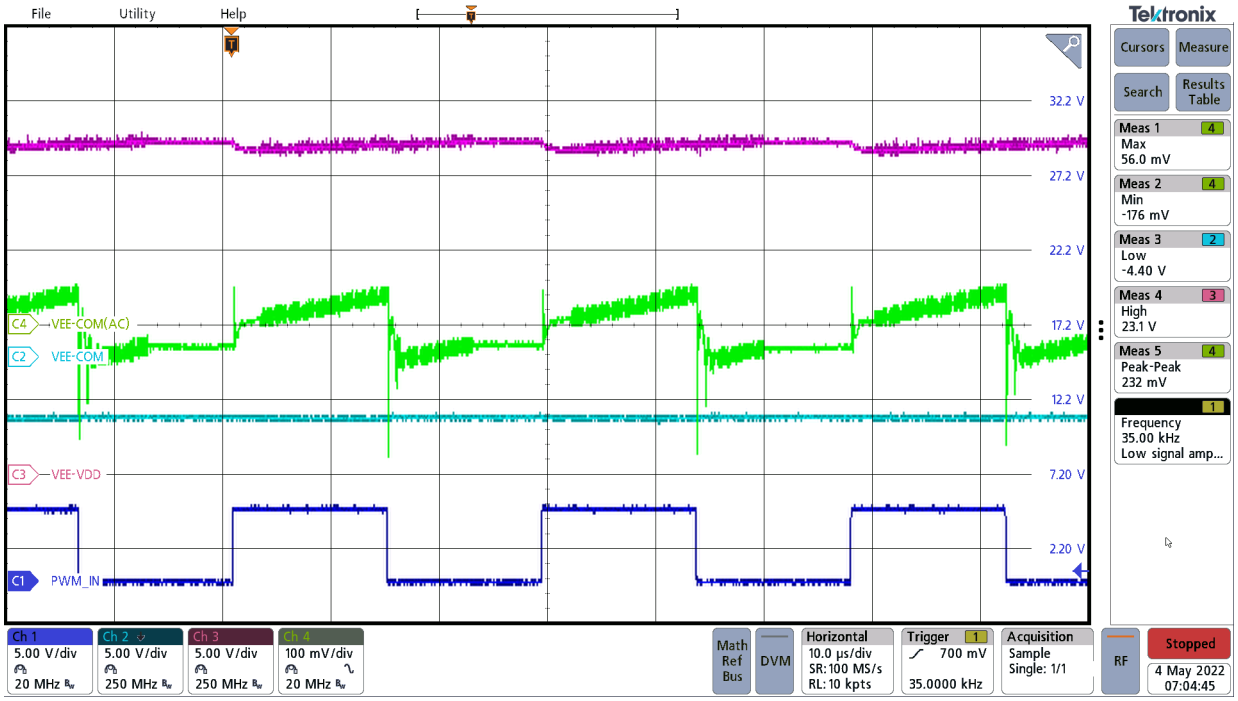


Figure 2-4. VEE-COM Switching 100-nF Load at 35 kHz

The green waveform in Figure 2-5 shows the VEE-VDD rail ripple while the output is switching a 100-nF capacitive load at 35 kHz. The peak to peak ripple is 800 mV, which is 3.6%.

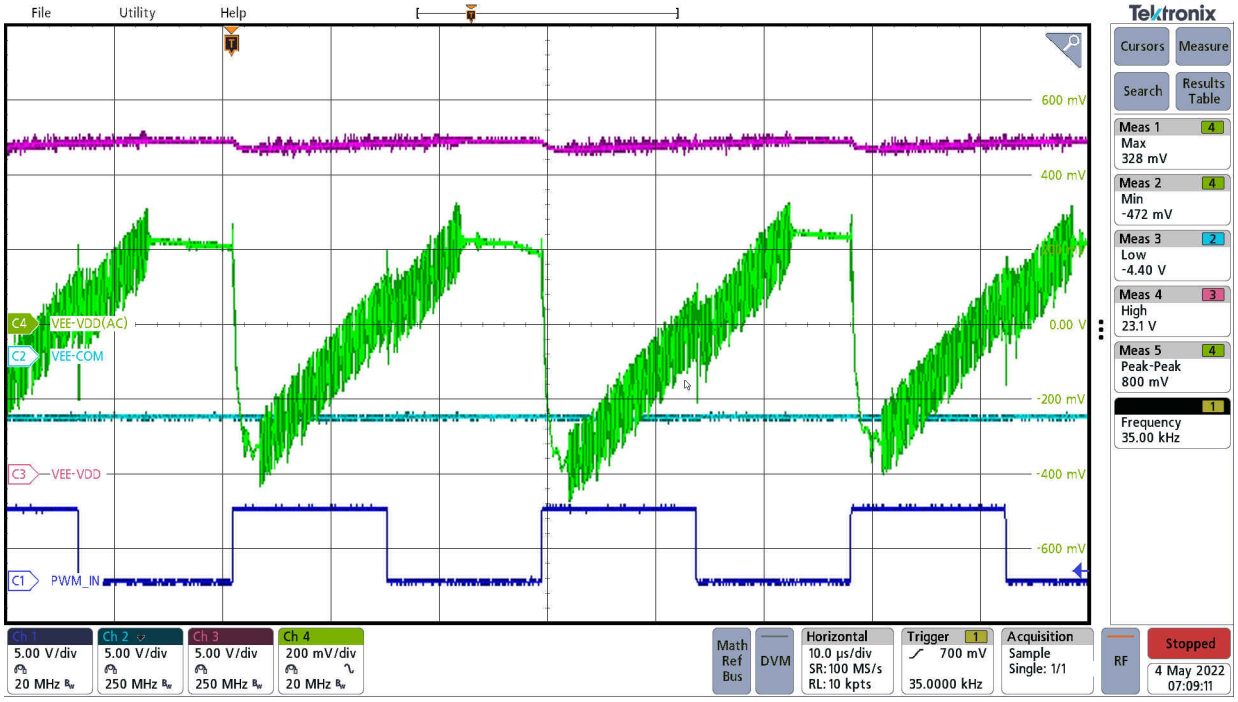


Figure 2-5. VEE-VDD Switching 100-nF Load at 35 kHz

2.3 Gate Waveforms

Gate waveforms are shown in Figure 2-6 switching at 1 kHz, and Figure 2-7 switching at 35 kHz.

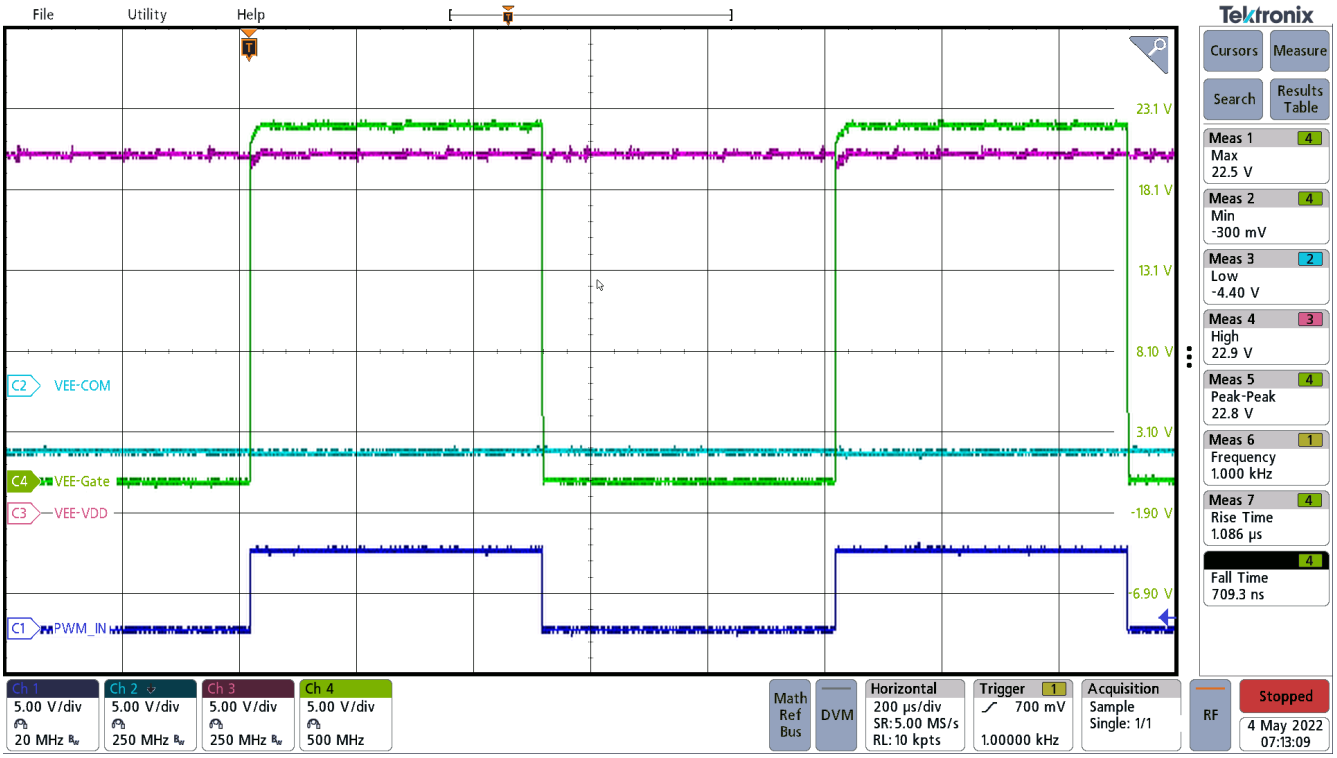


Figure 2-6. Gate Waveform Switching 100 nF at 1 kHz

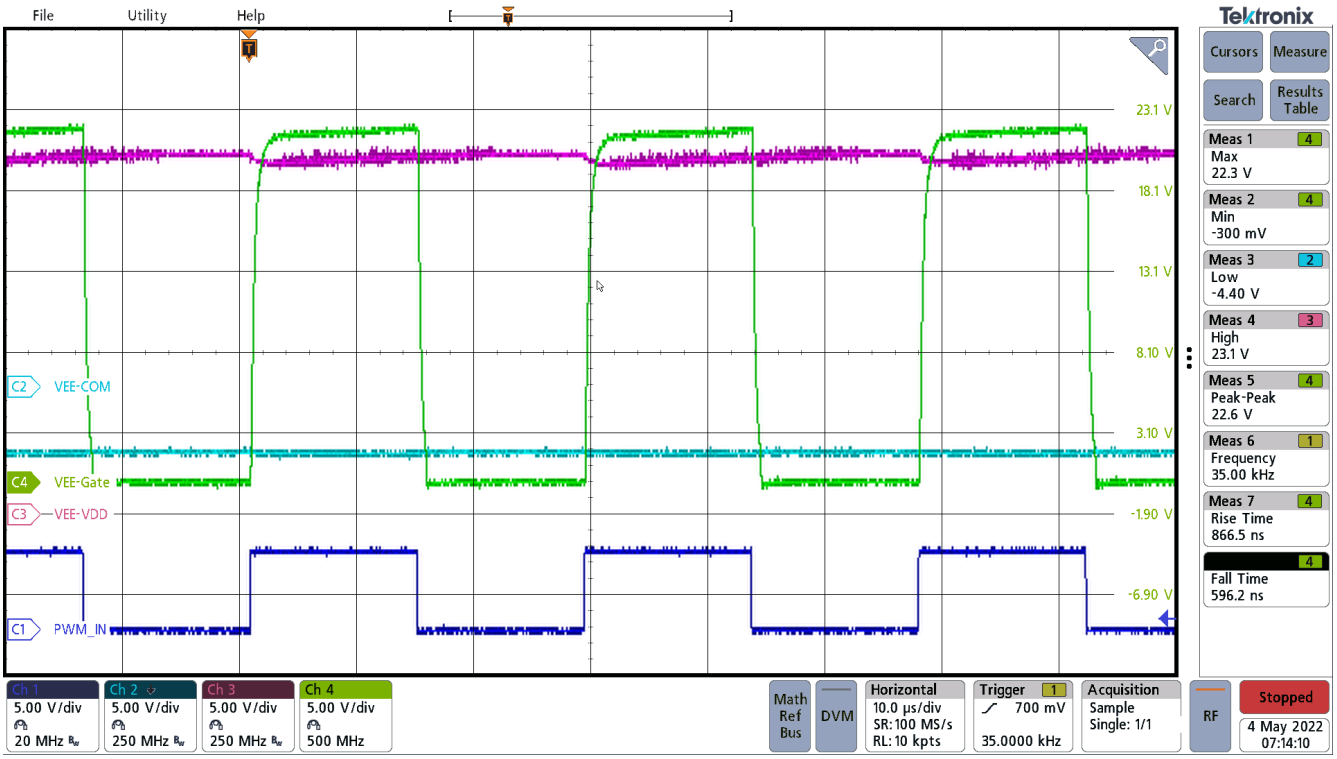


Figure 2-7. Gate Waveform Switching 100 nF at 35 kHz

2.4 Analog Sense

The analog sense feature of the UCC21732 is designed to allow easy temperature sensing across the isolation barrier, as described in the *Isolated Analog to PWM Signal Function* section of the *UCC21732-Q1 10-A Source/Sink Reinforced Isolated Single Channel Gate Driver for SiC/IGBT with Active Protection, Isolated Analog Sensing and High-CMTI* data sheet. The AIN voltage range is 0.6 V to 4.5 V, producing a PWM output on the APWM pin ranging from 88% duty cycle to 10% duty cycle. Figure 2-8 shows an AIN voltage of 4.87 V from VEE-AIN, which is 0.6 V from COM-AIN (Purple). The output PWM is 80.33% duty cycle (Green), and a filtered version of the APWM signal is 4.17 V which is an averaged version of the PWM output. Figure 2-9 shows the same waveforms, but with an input of 2.5 V to AIN, and a 40% APWM duty cycle. To use the APWM for power switch temperature sense connect a thermistor across J5. For more information, see the *UCC21732-Q1* data sheet.

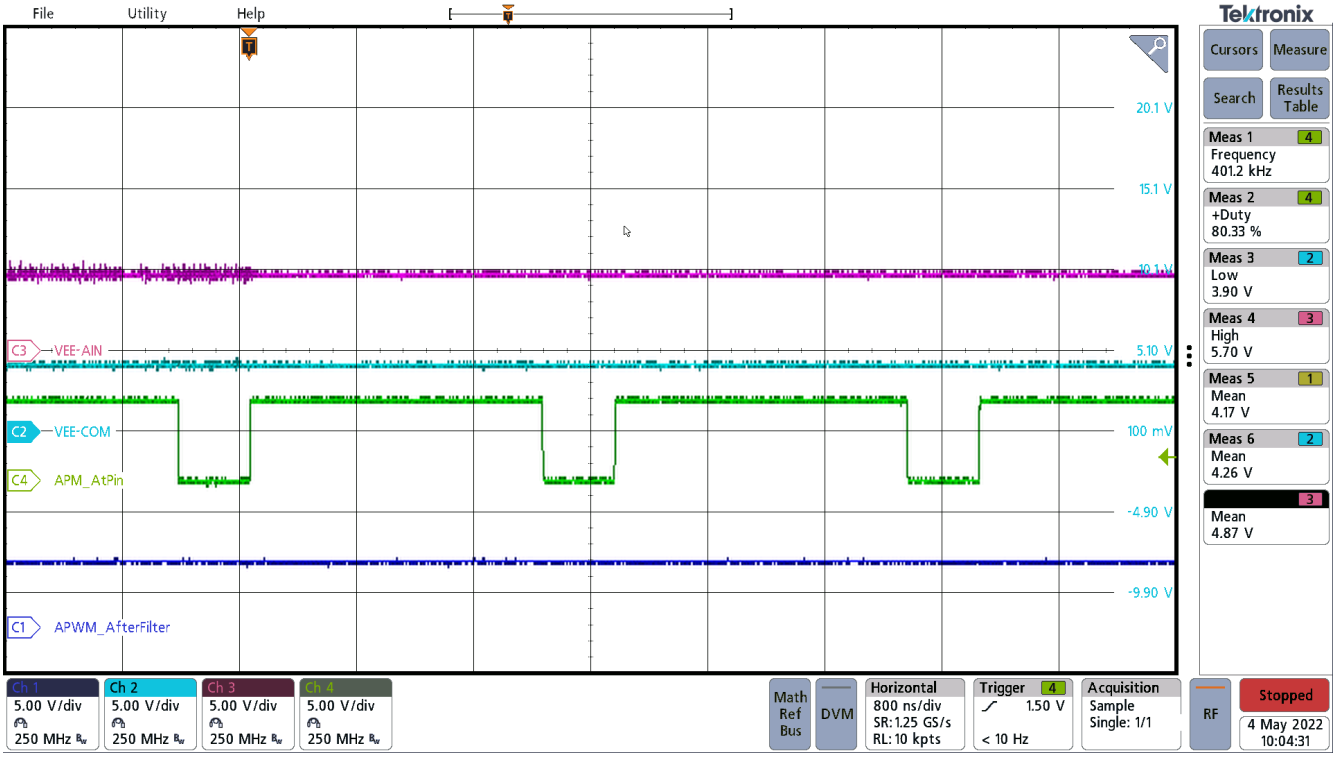


Figure 2-8. Analog Sense With 0.6-V AIN

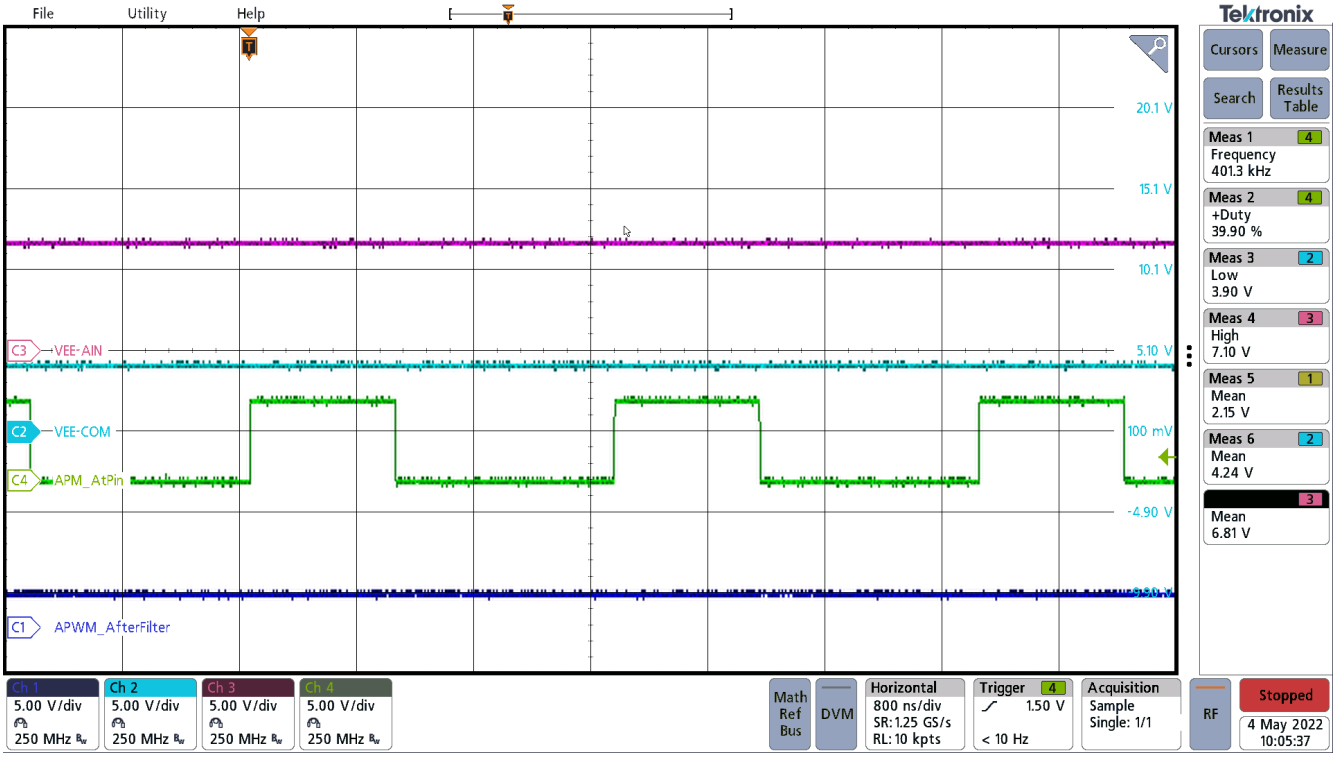


Figure 2-9. Analog Sense With 2.5-V AIN

2.5 DESAT, OC

This board implements overcurrent and short-circuit protection based on desaturation, as described in the *Protection Based on Desaturation Circuit* section of the *UCC21732-Q1* data sheet. This implementation allows the detection voltage and blanking time to be set with external passive components, as described in the UCC217xx excel calculator tool. This feature is disabled by default on the board to allow testing with a capacitive load, but can be enabled by populating R1 with a 2.2-kΩ resistor and connecting TP14 to the drain of the power switch. The default DESAT voltage is 5.4 V, and the blanking time is 130 ns.

2.6 Thermal Images

The test conditions for the thermal images are:

24-V input, VDD = 18 V, VEE= –4 V

The load is UCC21732 switching a 0.1-µF capacitive load.

Figure 2-10 shows the thermals while switching a 100-nF load at 1 kHz, which is about 0.18-W power through UCC14240. This is calculated as the sum of the power to charge the gate, and the quiescent power of the gate driver:

$$P_{gd} = F_{sw} \times C \times V_{gs} \times V_{gs} = 1\ kHz \times 100\ nF \times 22\ V \times 22\ V = 48.4\ mW \quad (1)$$

$$P_{ig} = V_{gs} \times I_q = 22\ V \times 4\ mA = 88\ mW \quad (2)$$

$$P_{gd} + P_{iq} = 48.4\ mW + 88\ mW = 136\ mW \quad (3)$$

Figure 2-11 shows the thermals while switching a 100-nF load at 35 kHz, which is about 1.5-W power through UCC14240. This is calculated as the sum of the power to charge the gate, and the quiescent power of the gate driver:

$$P_{gd} = F_{sw} \times C \times V_{gs} \times V_{gs} = 35\ kHz \times 100\ nF \times 22\ V \times 22\ V = 1.69\ W \quad (4)$$

$$P_{ig} = V_{gs} \times I_q = 22\ V \times 4\ mA = 88\ mW \quad (5)$$

$$P_{gd} + P_{iq} = 1.69\ W + 88\ mW = 1.778\ W \quad (6)$$

The soak time in both cases was 15 minutes, with no forced airflow.

At light load, the UCC14240 temperature peaks at 41.4°C, while the UCC21732 peaks at 38.1°C. The layout of this board balances thermal performance and switch node are. Thermals can be improved by increasing the thermal plane area on the secondary side.

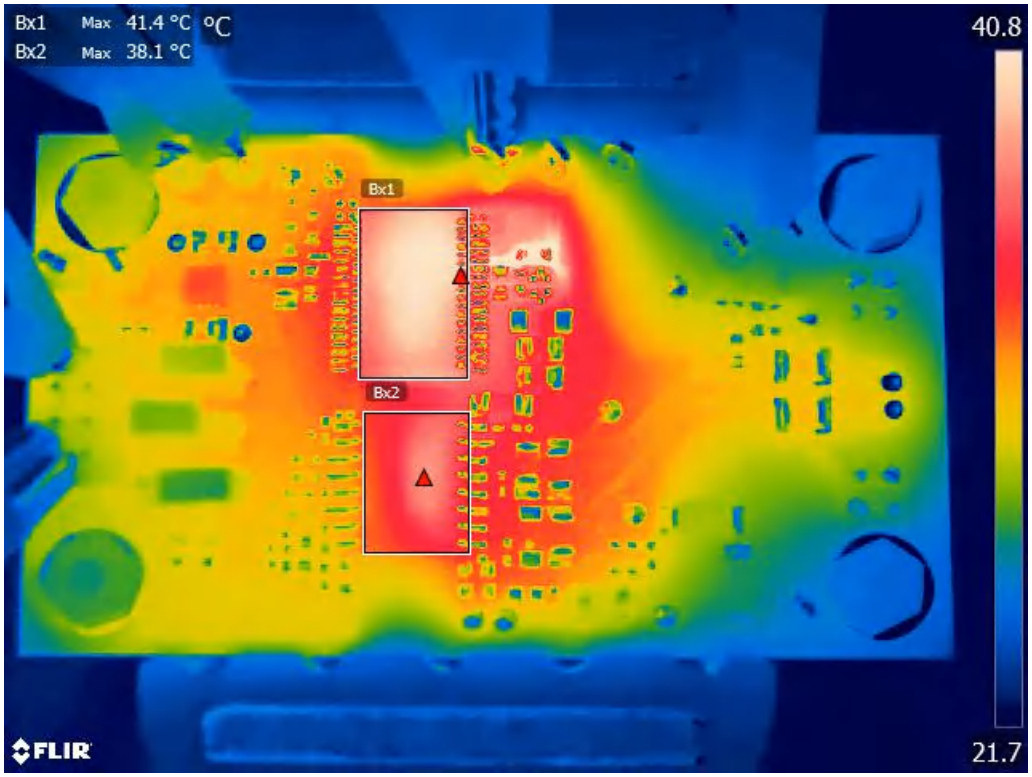


Figure 2-10. Thermal Image of 100-nF Load at 1 kHz, 0.17-W Power Draw

At peak load the UCC14240 temperature peaks at 86.9°C, while the UCC21732 peaks at 80.5°C. The highest temperature on the board is the gate resistors, which is not related to the performance of the ICs, and could be improved by paralleling multiple gate resistors or reducing the gate resistance. The layout of this board balances thermal performance and switch node are. Thermals can be improved by increasing the thermal plane area on the secondary side.

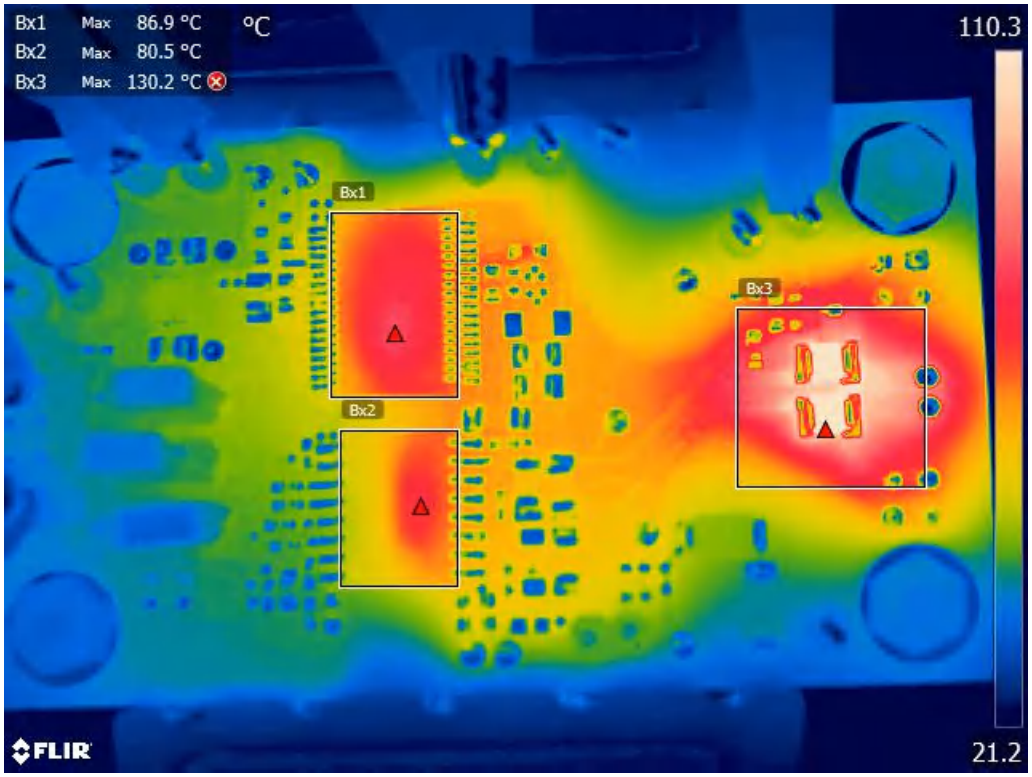


Figure 2-11. Thermal Image of 100-nF Load at 35 kHz, 1.5-W Power Draw

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265