Test Report: PMP30834

Isolated 4-W Reference Design With Integrated Switch and PSR

Description

This reference design provides 5.2-V, 4-W, isolated voltage from a 5-V DC input supply. The isolated output voltage is sampled from the primary-side flyback voltage, eliminating the need for an optocoupler, voltage reference, or third winding from the transformer for output voltage regulation. The high level of integration results in a simple, reliable, and high-density design with only one component crossing the isolation barrier.

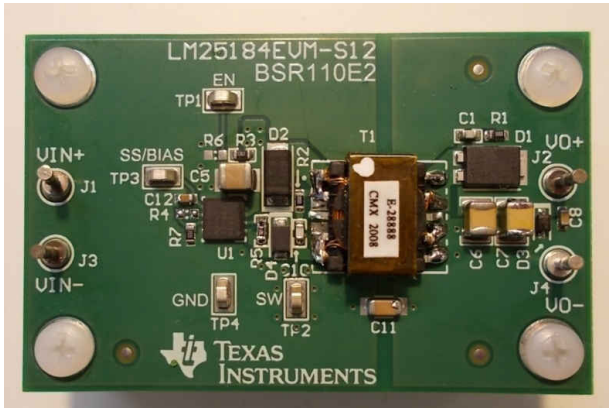
The reference design was built by modifying the LM25184EVM-S12.

Features

- 4.5-V to 6-V input voltage range
- 5.2-V output voltage primary side regulated
- Rated for 750 mA of load current
- Packaged in a miniature footprint with low component count
- Board dimensions, excluding the connectors: 56 mm × 36 mm, height = 5.5 mm

Applications

- Analog input module
- Analog output module
- Mixed module (AI,AO,DI,DO)



Top Board Photo

Bottom Board Photo

1 Test Prerequisites

1.1 Voltage and Current Requirements

Table 1-1. Voltage and Current Requirements

Parameter	Specifications
Input Voltage Range	4.5 V–6 V (DC)
Output Voltage	5.2 V, –2% to +8%
Output Current	750 mA

1.2 Required Equipment

- 0 V to 20 V, (minimum 2 A), constant voltage source (VS1)
- 0 A to 1 A, electronic load
- Oscilloscope (minimum 200-MHz bandwidth)

1.3 Considerations

Connect the source VS1 to J1 and J3.

Connect the load to J2 and J4 set to constant-current mode.

Connect an oscilloscope probe to TP2 versus primary ground.

Connect the second oscilloscope probe to the anode of D1 and secondary side ground.

1.4 Dimensions

The board dimensions, excluding the connectors, are 56 mm × 36 mm, height = 5.5 mm.

2 Testing and Results

2.1 Efficiency Graphs

Figure 2-1 shows the efficiency graph versus output current. The load current shown increases from zero to 750 mA. The voltage of the power source was set to 4.5 V and 6 V.

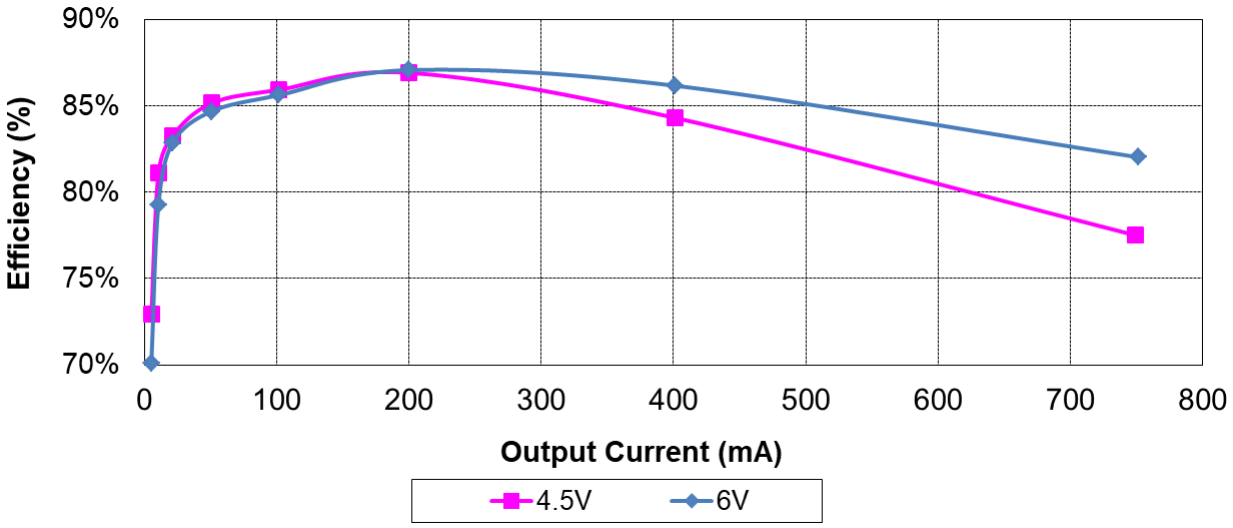


Figure 2-1. Efficiency Graph

2.2 Efficiency Data

V_{IN} (V)	I_{IN} (mA)	P_{IN} (W)	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)	Efficiency (%)
4.565	9.0	0.041	5.587	0	0	0%
4.565	9.0	0.041	5.548	5.4	0.030	72.92%
4.564	15.1	0.069	5.176	10.8	0.056	81.11%
4.561	29.3	0.134	5.176	21.5	0.111	83.27%
4.550	68.0	0.309	5.176	50.9	0.263	85.15%
4.532	135.2	0.613	5.177	101.7	0.527	85.93%
4.518	264.3	1.194	5.179	200.4	1.038	86.92%
4.514	545.9	2.464	5.181	401.0	2.078	84.31%
4.500	1092	4.914	5.085	749.0	3.809	77.51%

V_{IN} (V)	I_{IN} (mA)	P_{IN} (W)	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)	Efficiency (%)
6.036	7.1	0.043	5.600	0	0	0%
6.034	7.1	0.043	5.561	5.4	0.030	70.09%
6.037	11.6	0.070	5.187	10.7	0.056	79.25%
6.034	22.3	0.135	5.186	21.5	0.111	82.86%
6.027	51.7	0.312	5.184	50.9	0.264	84.68%
6.012	102.4	0.616	5.183	101.7	0.527	85.62%
6.032	197.8	1.193	5.184	200.4	1.039	87.07%
6.012	401.5	2.414	5.187	401.0	2.080	86.17%
6.021	790	4.755	5.189	751.6	3.900	82.02%

2.3 Output Voltage Regulation

Figure 2-2 shows the output voltage regulation graphs for each output.

Both outputs are equally loaded from zero to 130 mA.

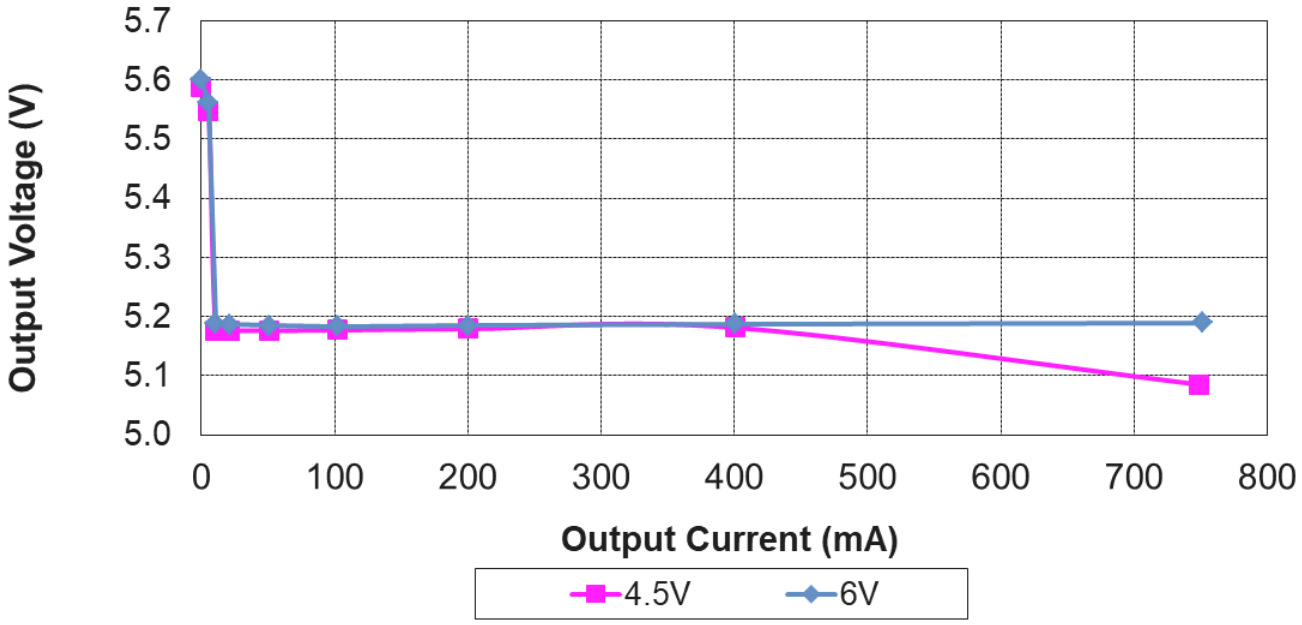
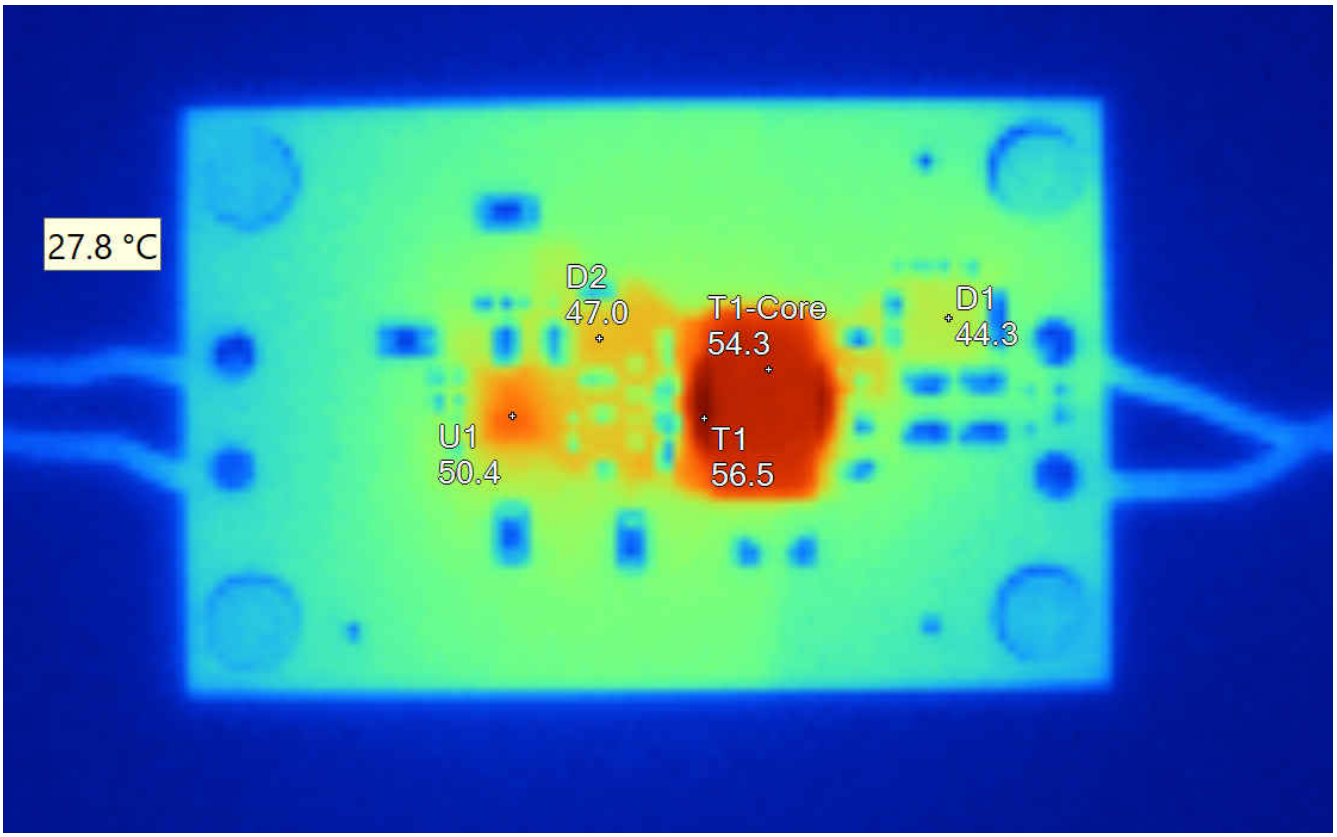


Figure 2-2. Output Voltage Regulation

2.4 Thermal

The following graph and table describe the thermal behavior of the converter placed horizontally on the bench, at full load, with ambient temperature of 25.5°C and in a still air condition.



Conditions: V_{IN} = 5 VDC, fully loaded; image taken after 60 minutes

Figure 2-3. Thermal Image

Table 2-1. Main Image Markers

Name	Temperature	Emissivity	Background
T1	56.5°C	0.96	25.5°C
T1-Core	54.3°C	0.96	25.5°C
U1	50.4°C	0.96	25.5°C
D1	44.3°C	0.96	25.5°C
D2	47.0°C	0.96	25.5°C

3 Waveforms

3.1 Switching

The switching waveforms in Figure 3-1 through Figure 3-3 were measured by supplying the converter at 5 V and 750-mA load, where the primary current reaches its highest peak, resulting into the highest spike on the SW-node.

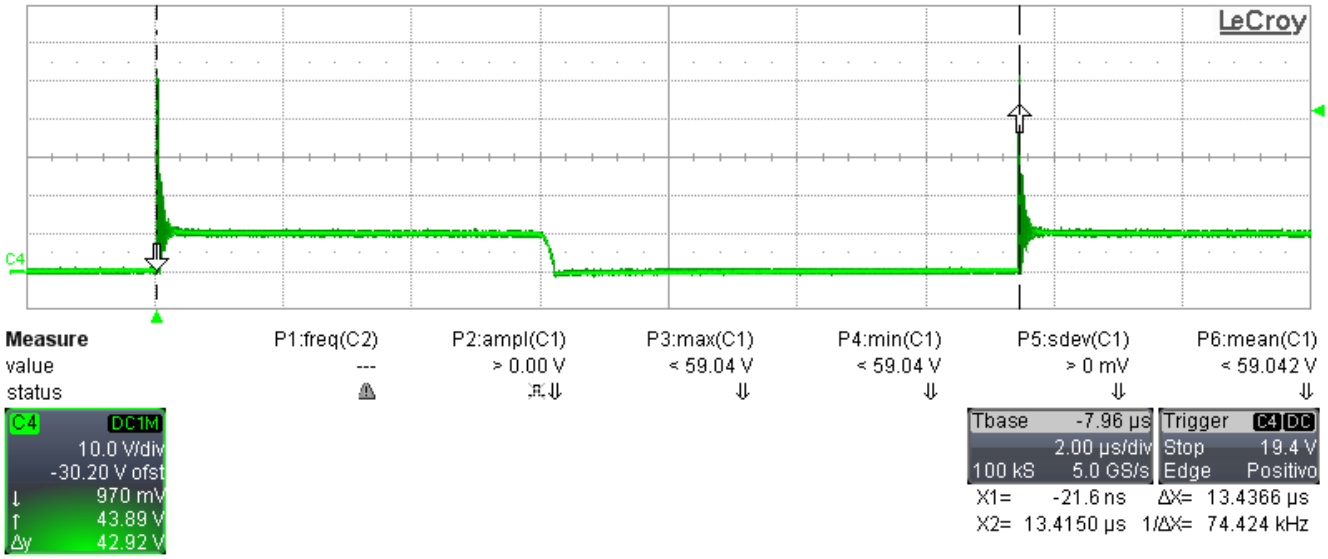


Figure 3-1. C2: Switch Node of U1 (TP2) (10 V/div, 2 µs/div, no BWL), V_{IN} = 5 V

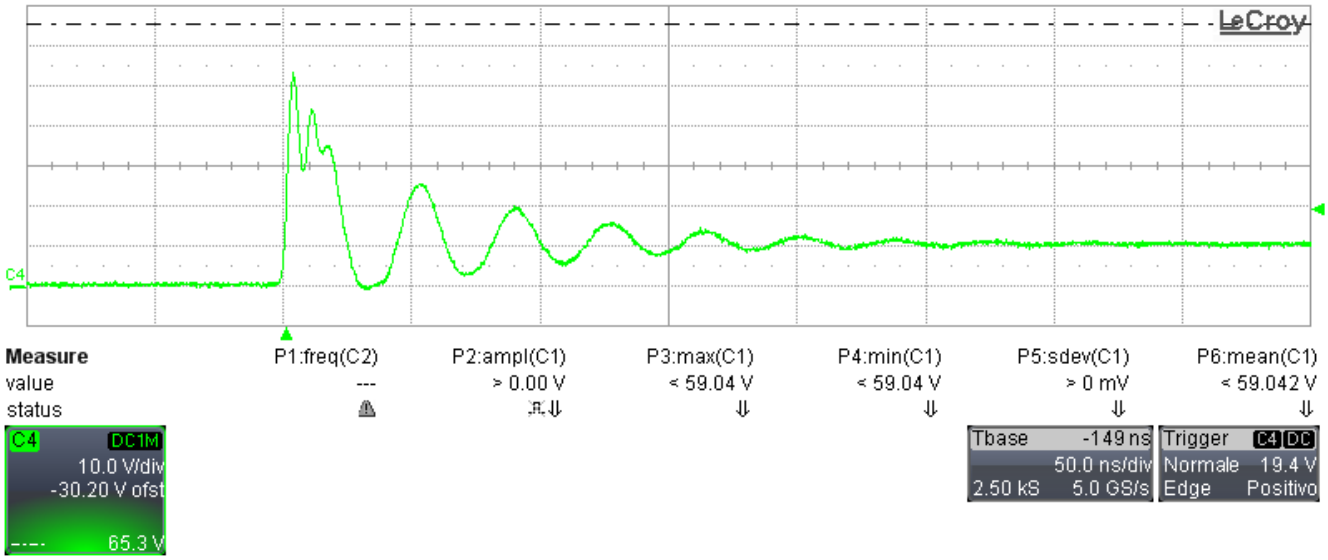


Figure 3-2. C2: Switch Node of U1 (TP2) (10 V/div, 50 ns/div, no BWL), V_{IN} = 5 V

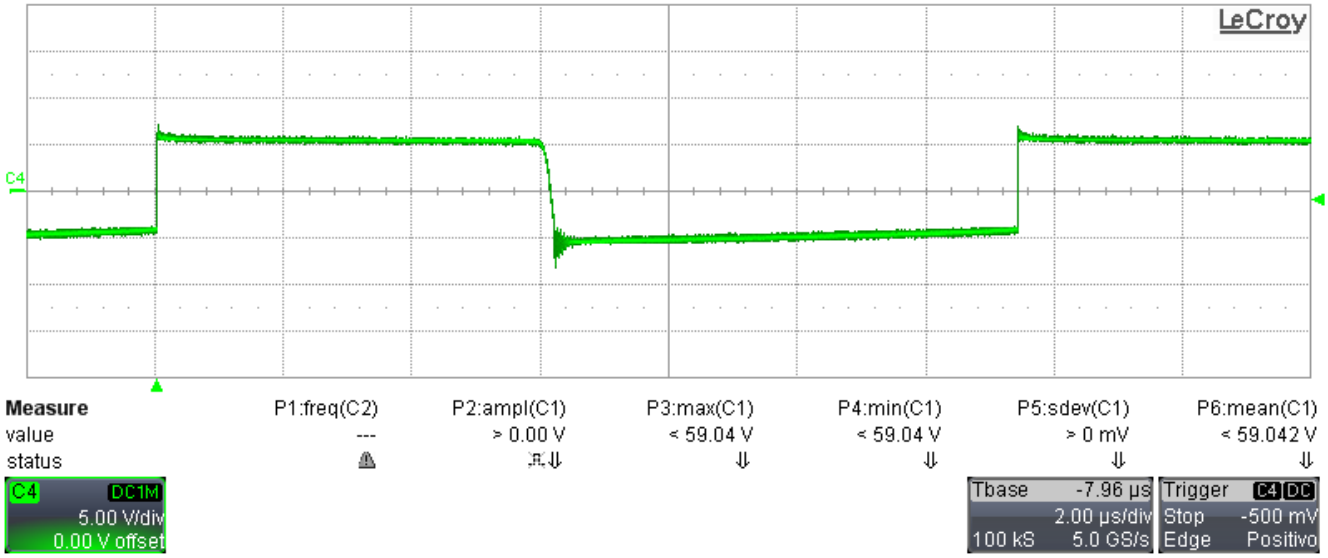


Figure 3-3. C4: Anode of D1 vs Secondary Ground (5 V/div, 2 µs/div, no BWL)

3.2 Output Voltage Ripple

The output voltage ripple was measured by supplying the converter at 5 V in full-load condition.

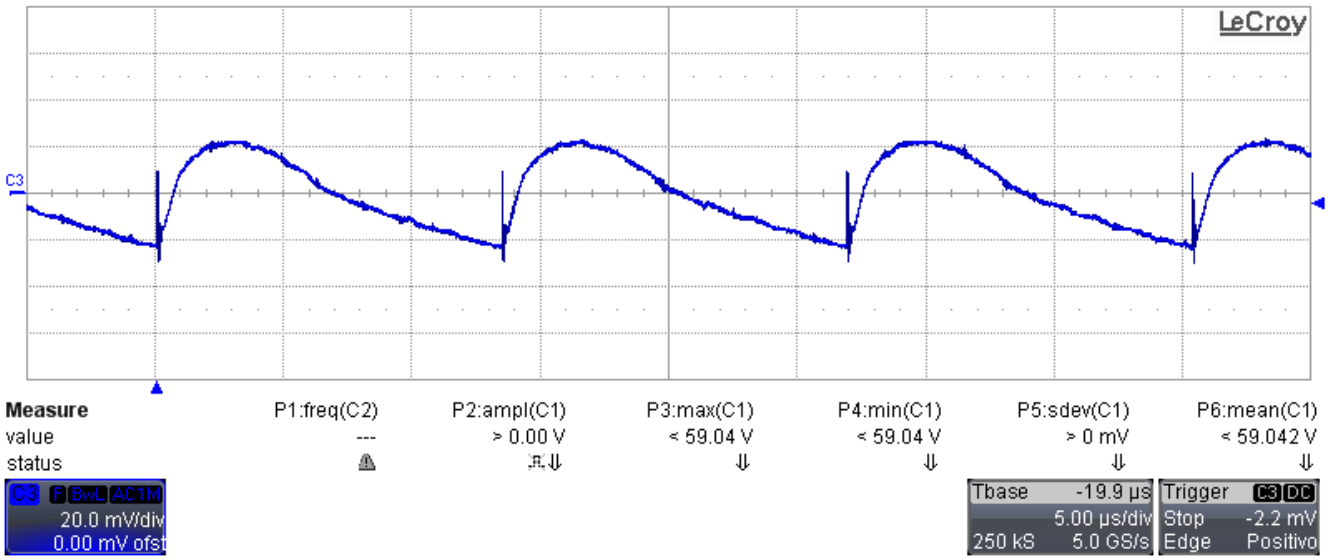
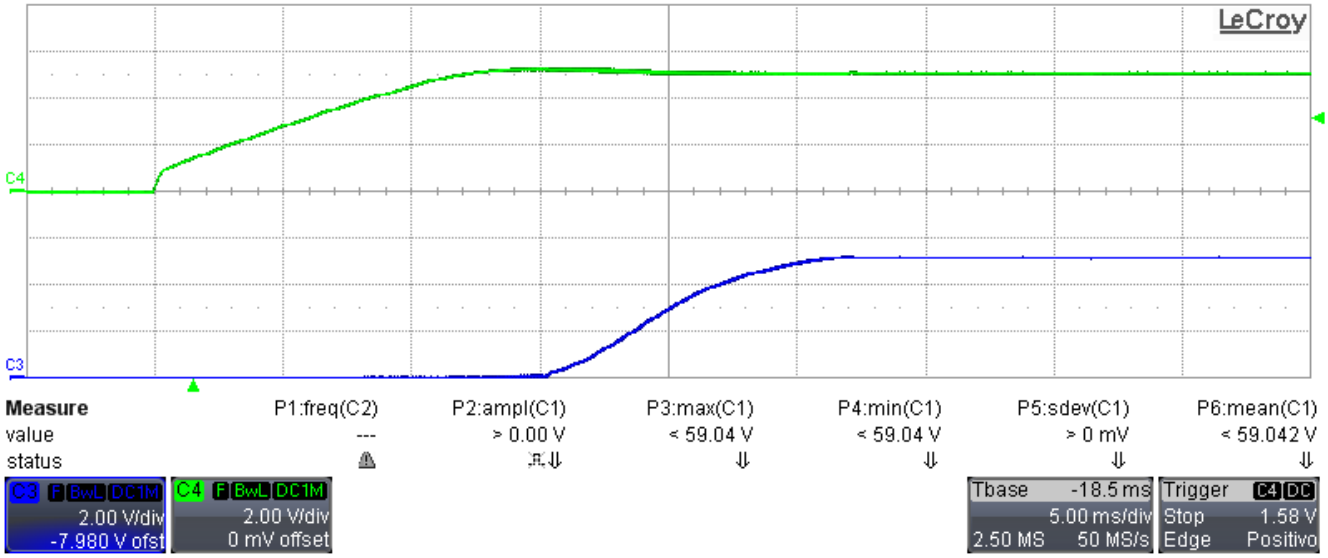


Figure 3-4. C3: Output Voltage (20 mV/div, 5 µs/div, AC coupling, 20-MHz BWL)

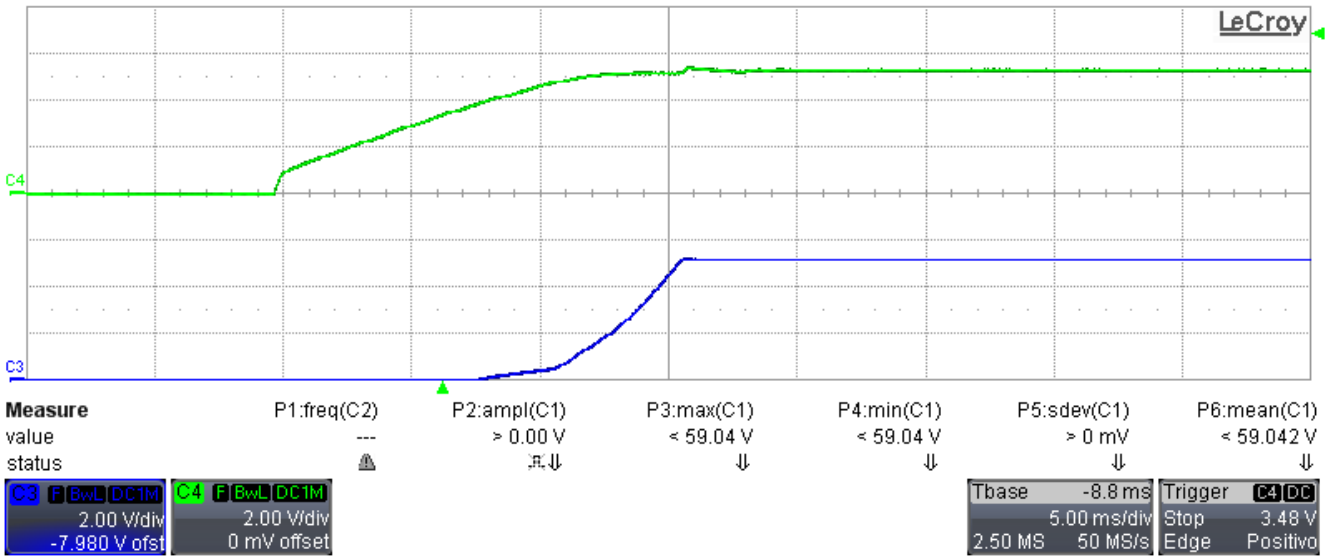
3.3 Start-Up Sequence

The behavior of the converter, showing V_{IN} and the output voltage, is shown in Figure 3-5 and Figure 3-6. The input voltage has been set to 5 V.



C3: Output Voltage (2 V/div, 5 ms/div, 20-MHz BWL)
C4: Input Voltage (2 V/div, 20-MHz BWL)
I_{OUT} = 750 mA

Figure 3-5. Start-Up With I_{OUT} = 750 mA

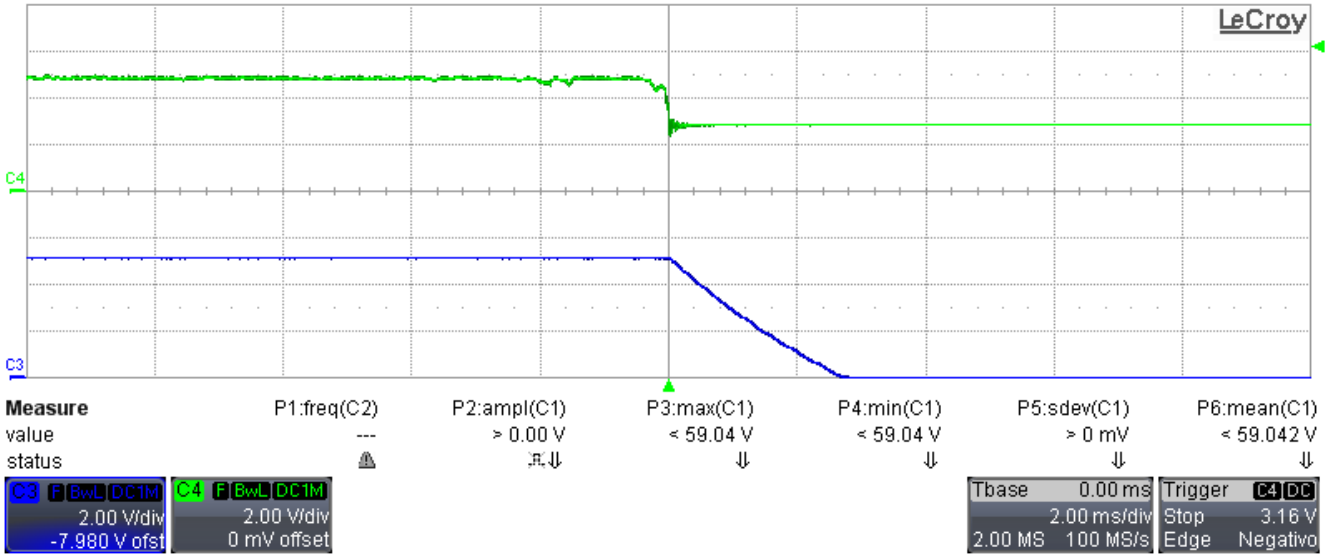


C3: Output Voltage (2 V/div, 5 ms/div, 20-MHz BWL)
C4: Input Voltage (2 V/div, 20-MHz BWL)
I_{OUT} = 0 mA

Figure 3-6. Start-Up With I_{OUT} = 0 A

3.4 Shutdown Sequence

The behavior of the converter, during shutdown by disconnecting the power source, was measured and is shown in Figure 3-7.



C3: Output Voltage (2 V/div, 2 ms/div, 20-MHz BWL)
C4: Input Voltage (2 V/div, 20-MHz BWL)
I_{OUT} = 750 mA

Figure 3-7. Shutdown

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