Test Report: PMP30833

30-W Two-Switch Buck-Boost Reference Design With 24-V or 48-V Output

Description

This two-switch buck boost controlled by the LM5118 device is stepping up and stepping down an input voltage range of 30 V to 60 V to either 24-V or 48-V output voltage. Jumper #3 at the digital-to-analog converter (DAC) is used to decide for 24 V_{OUT} or 48 V_{OUT} – with jumper 48 V_{OUT}, without 24 V_{OUT}.

For the final application, the 48-V output voltage is just needed for short term use < 1 s. For test purposes the power stage withstands this power level continuously, so the power stage itself could be shrunk for the final application.

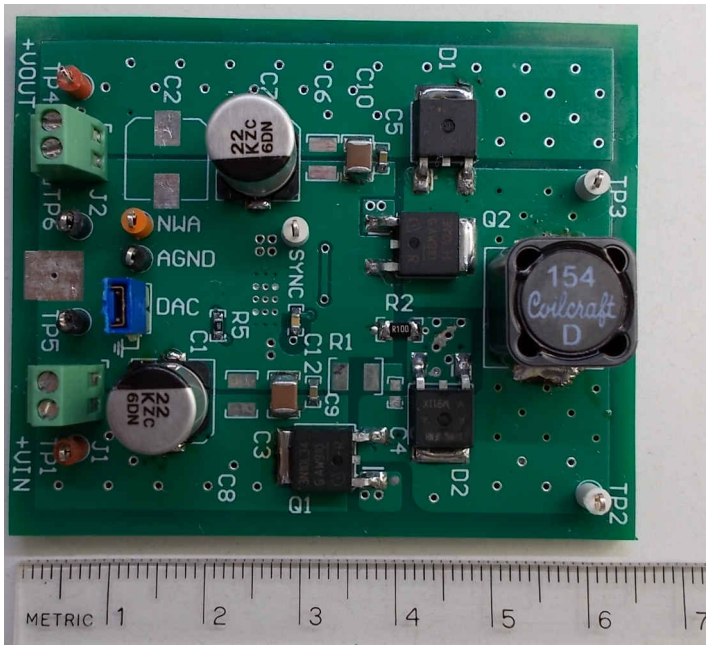
Modify the loop bandwidth from between 600 Hz, 1200 Hz, and 2400 Hz – the default is 1.2 kHz. The final application adds a reactive load to the output and needs to be adapted; this prototype supports three different tested variants.

Features

- Supports 48-V start-up output voltage and 24-V continuous output voltage
- The prototype itself supports continuous 48-V output operations at full load, 600 mA for test purposes
- Three control variants support various reactive load types
- Control scheme supports switched output voltage, load transient, and line transient

Applications

- Appliances pumps and fans



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1 Test Prerequisites

1.1 Voltage and Current Requirements

Table 1-1. Voltage and Current Requirements

Parameter	Specifications
Input Voltage Range	30 V to 60 V, 65 V_{MAX}
Output Voltage	24 V or 48 V
Maximum Output Current	0.6 A at 48 V_{OUT}
Switching Frequency	300 kHz

1.2 Considerations

Unless otherwise indicated, all measurements were done by 0.6 A adjusted by a variable resistor.

The circuit starts with switching at 28 V and stops with switching around 25.7 V.

The prototype worked at a measured switching frequency of 300 kHz and soft start set to 12 ms.

Note

By inserting the jumper J3, the output voltage can be switched from 24 V to 48 V.

1.3 Dimensions

The outline of the board PMP30520 Rev. A is 53 mm × 64 mm. This PCB is a two-layer board with 2-oz copper thickness on each layer.

2 Testing and Results

2.1 Efficiency Graphs

2.1.1 24-V Output Voltage

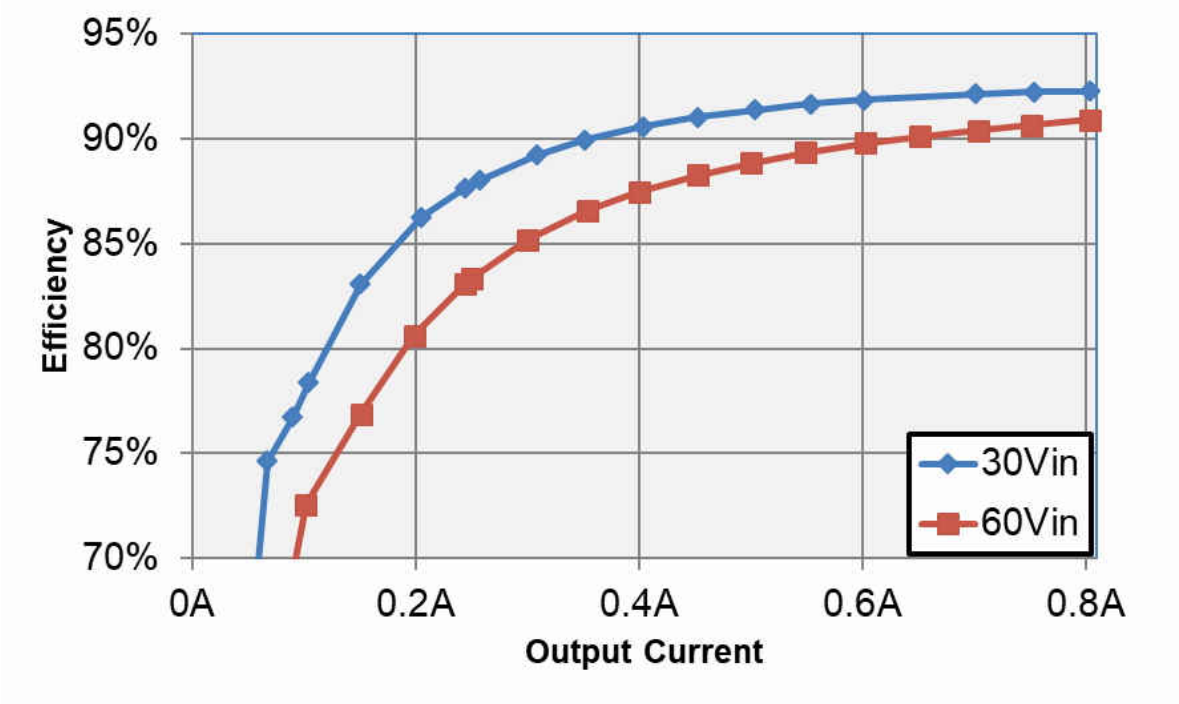


Figure 2-1. Efficiency vs Output Current

2.1.2 48-V Output Voltage

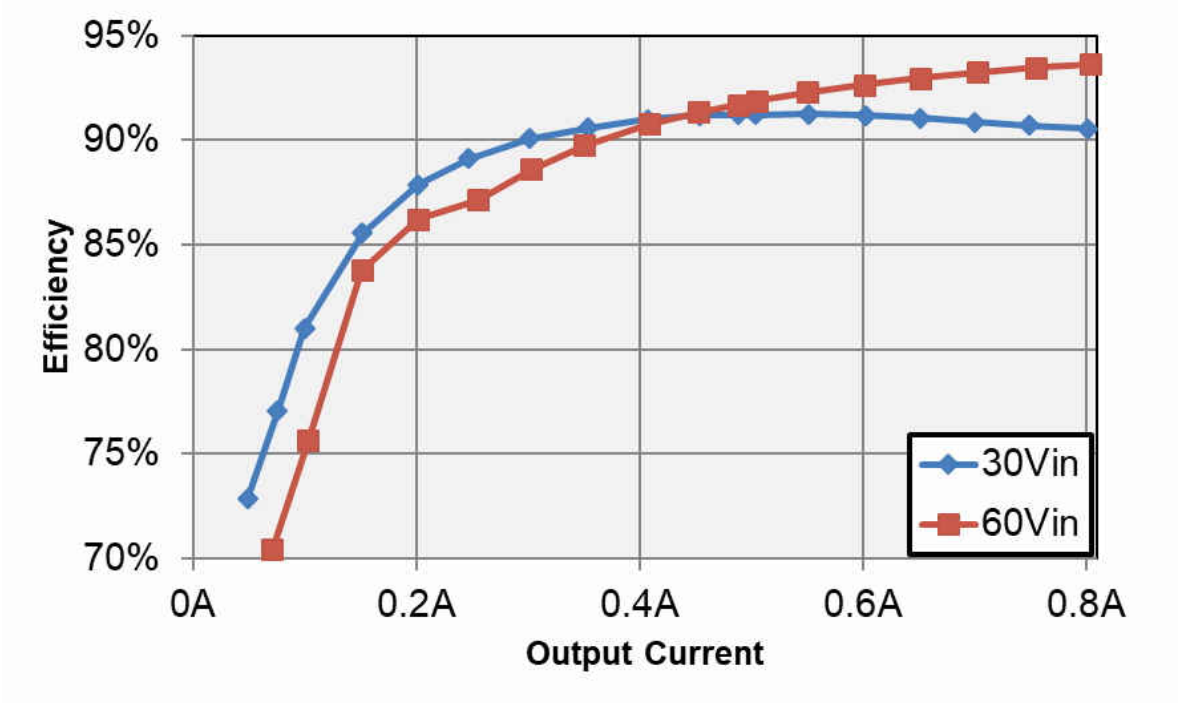


Figure 2-2. Efficiency vs Output Current

2.2 Loss Graphs

2.2.1 24-V Output Voltage

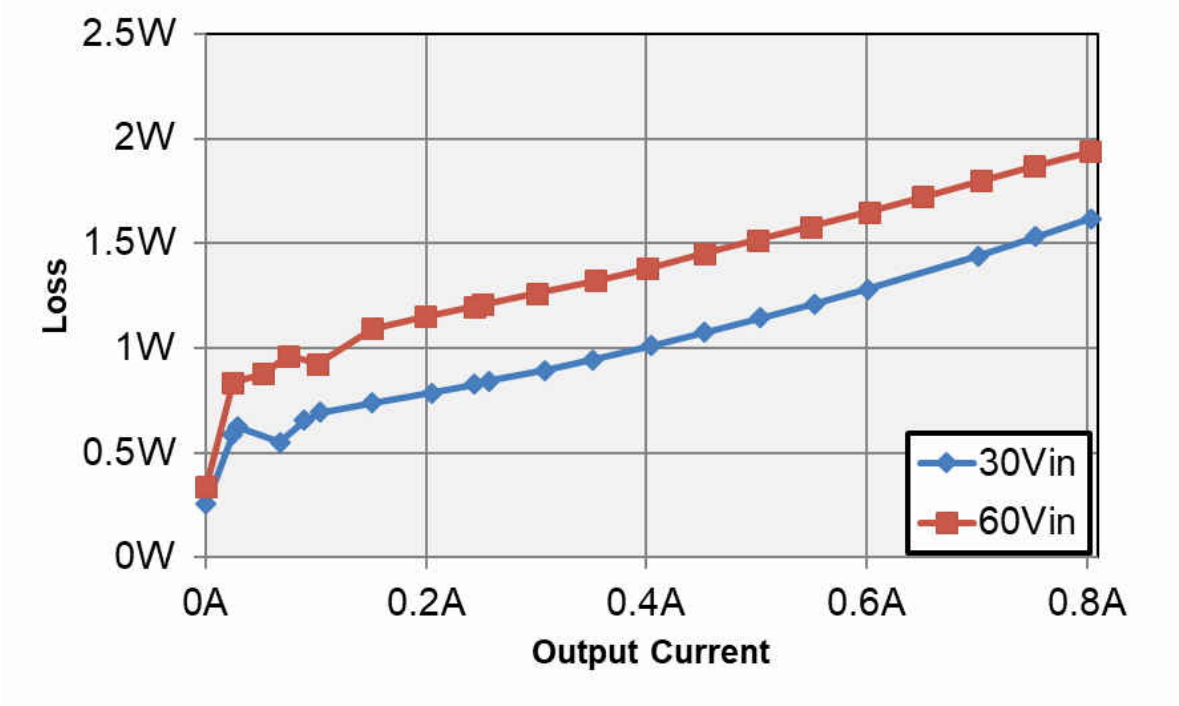


Figure 2-3. Loss vs Output Current

2.2.2 48-V Output Voltage

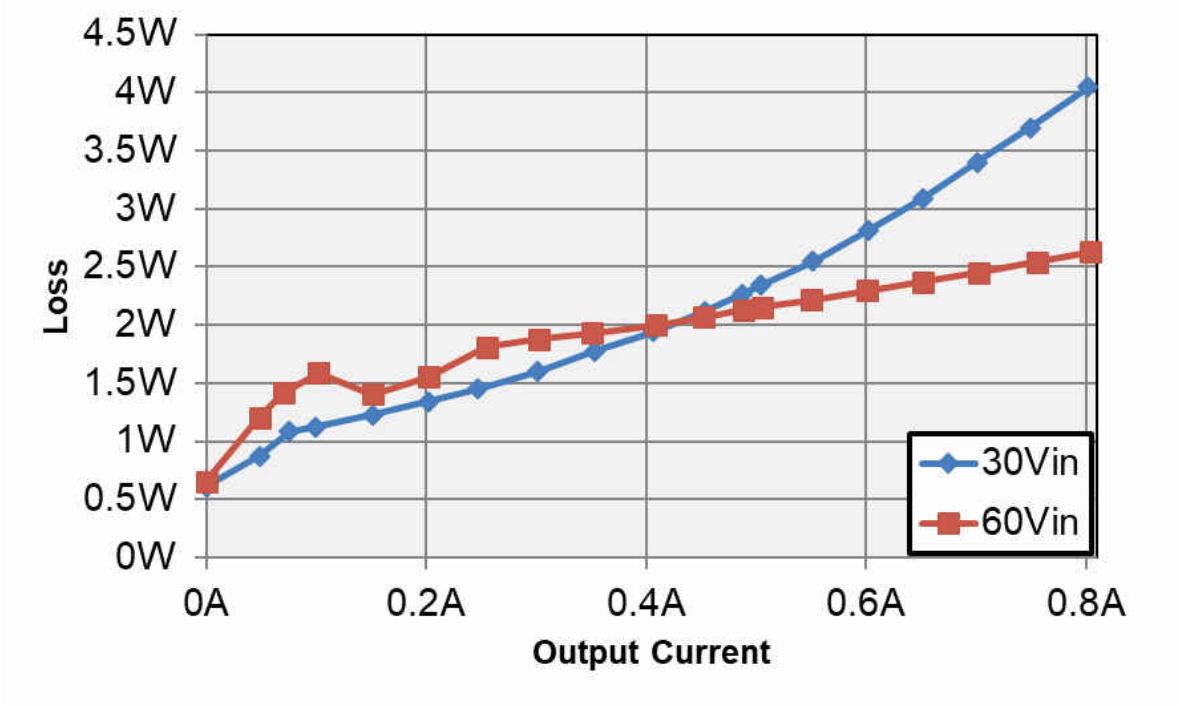


Figure 2-4. Loss vs Output Current

2.3 Load Regulation

2.3.1 24-V Output Voltage

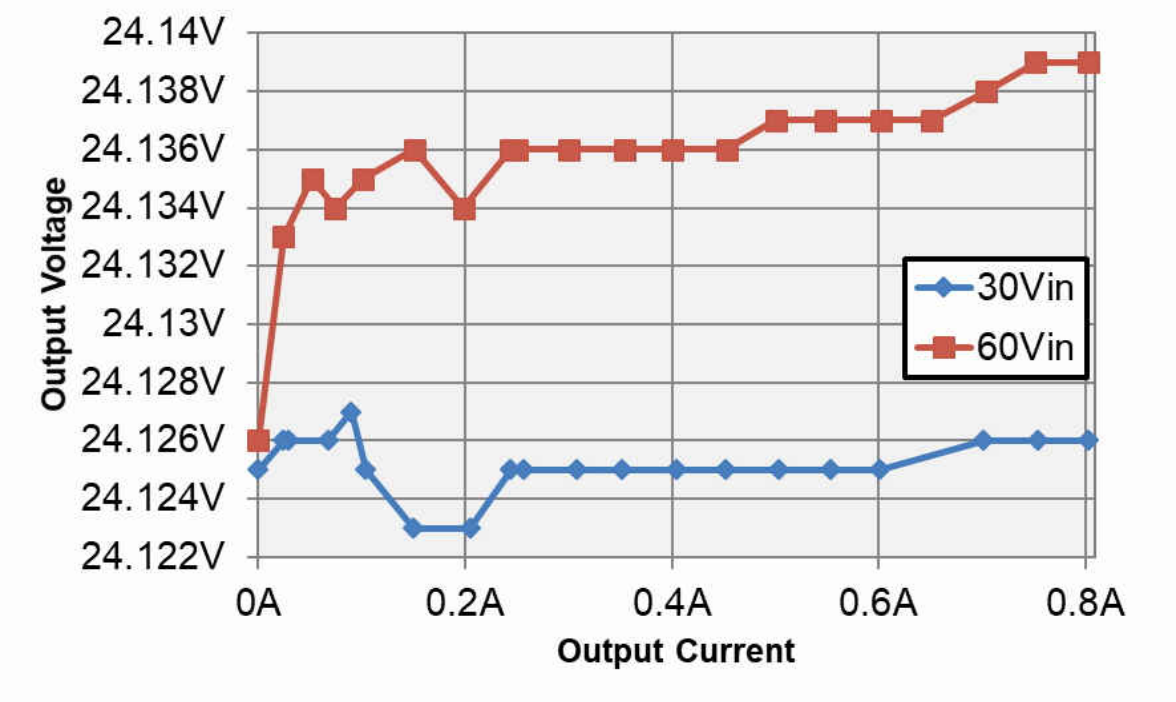


Figure 2-5. Output Voltage vs Output Current

2.3.2 48-V Output Voltage

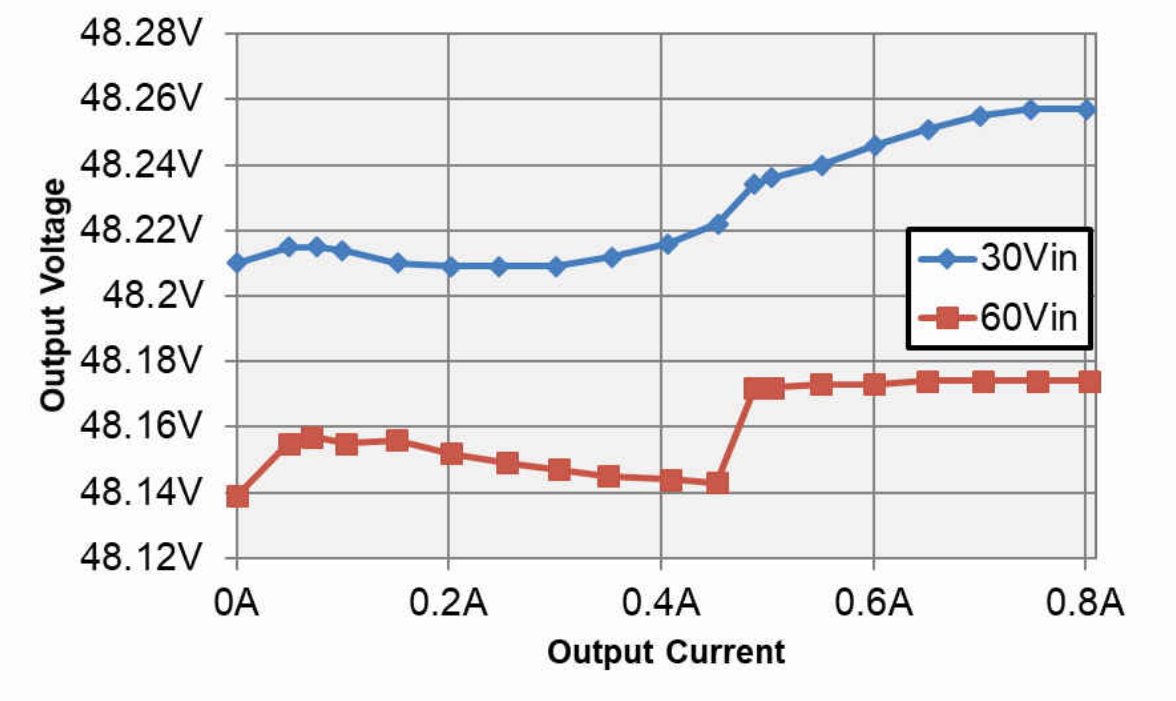


Figure 2-6. Output Voltage vs Output Current

2.4 Line Regulation

2.4.1 24-V Output Voltage

Figure 2-7 shows the output voltage depending on the input voltage.

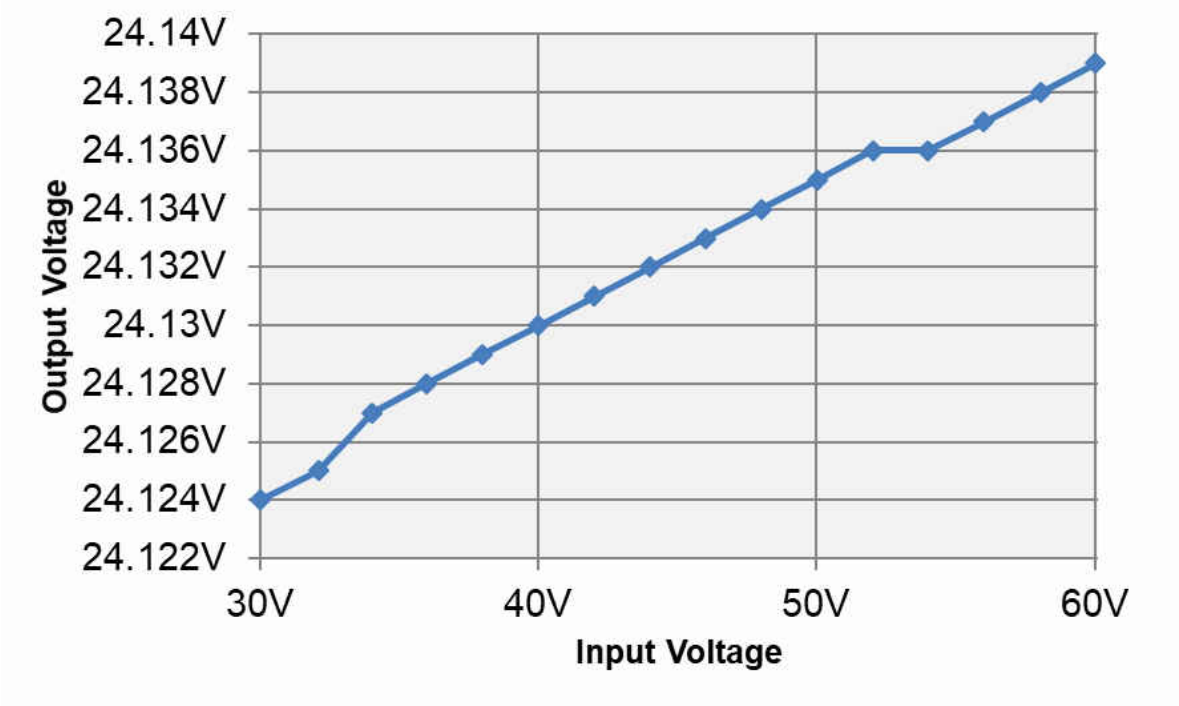


Figure 2-7. Output Voltage vs Input Voltage

Efficiency and loss were also calculated.

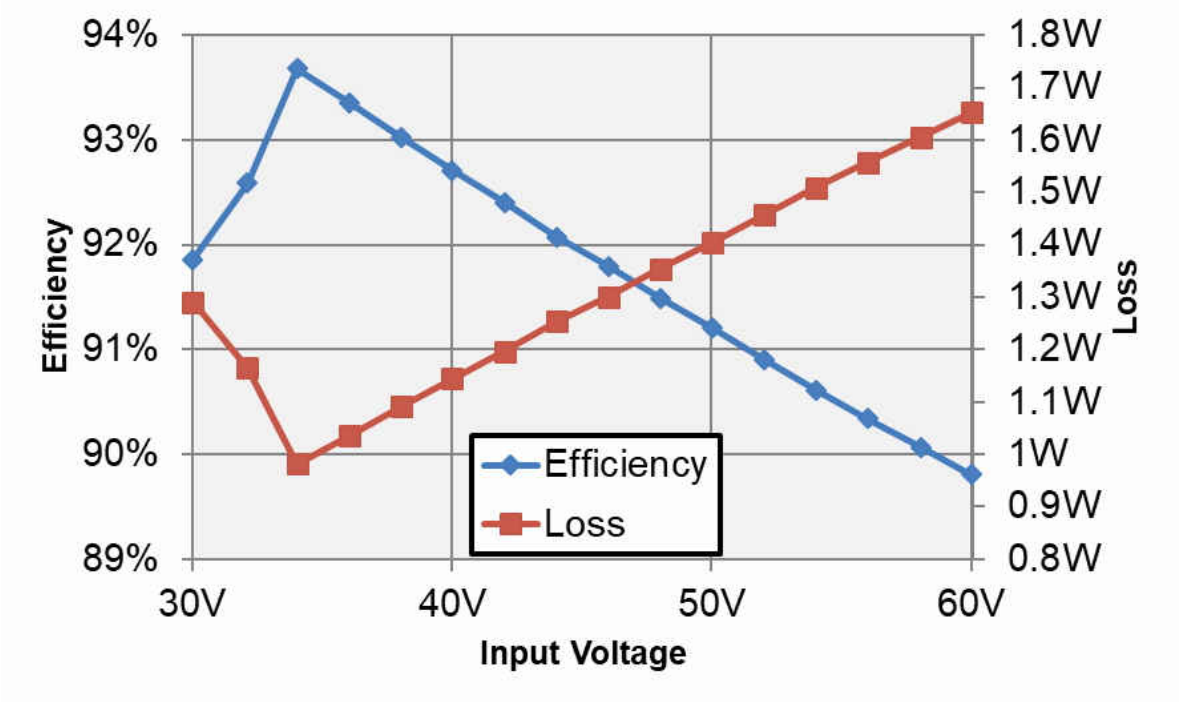


Figure 2-8. Loss and Efficiency vs Input Voltage

2.4.2 48-V Output Voltage

The dependency of output voltage to the input voltage is shown in Figure 2-9.

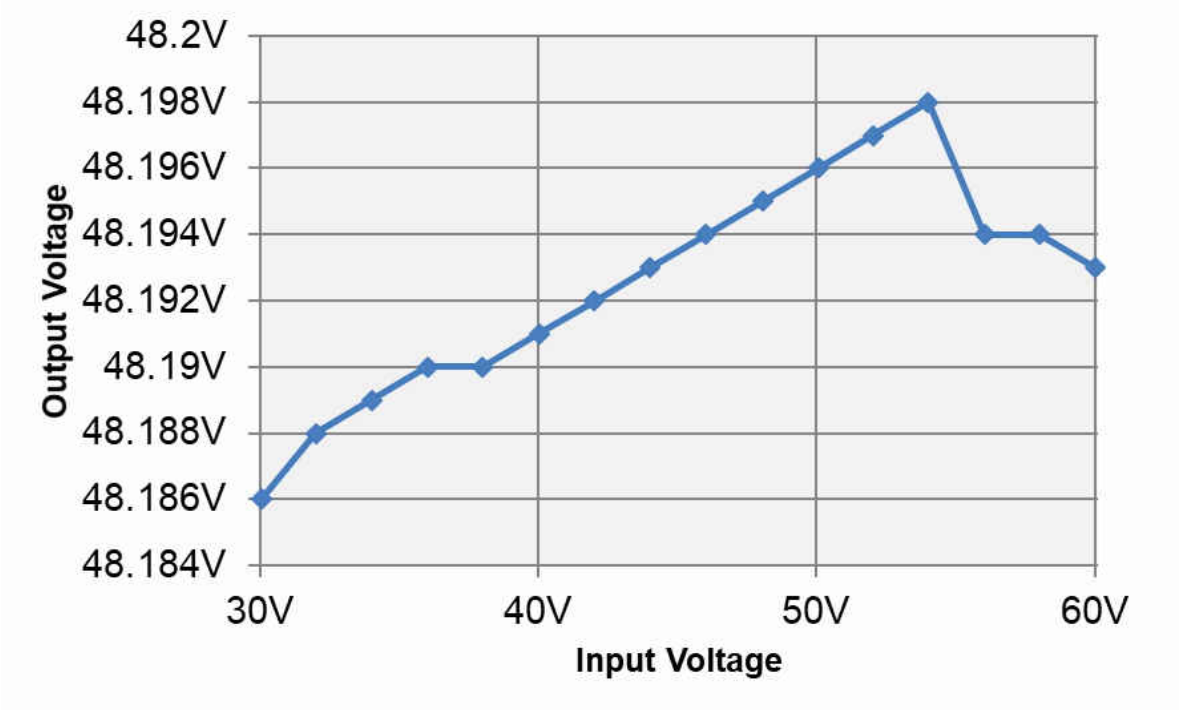


Figure 2-9. Output Voltage vs Input Voltage

Figure 2-10 shows the efficiency and loss data.

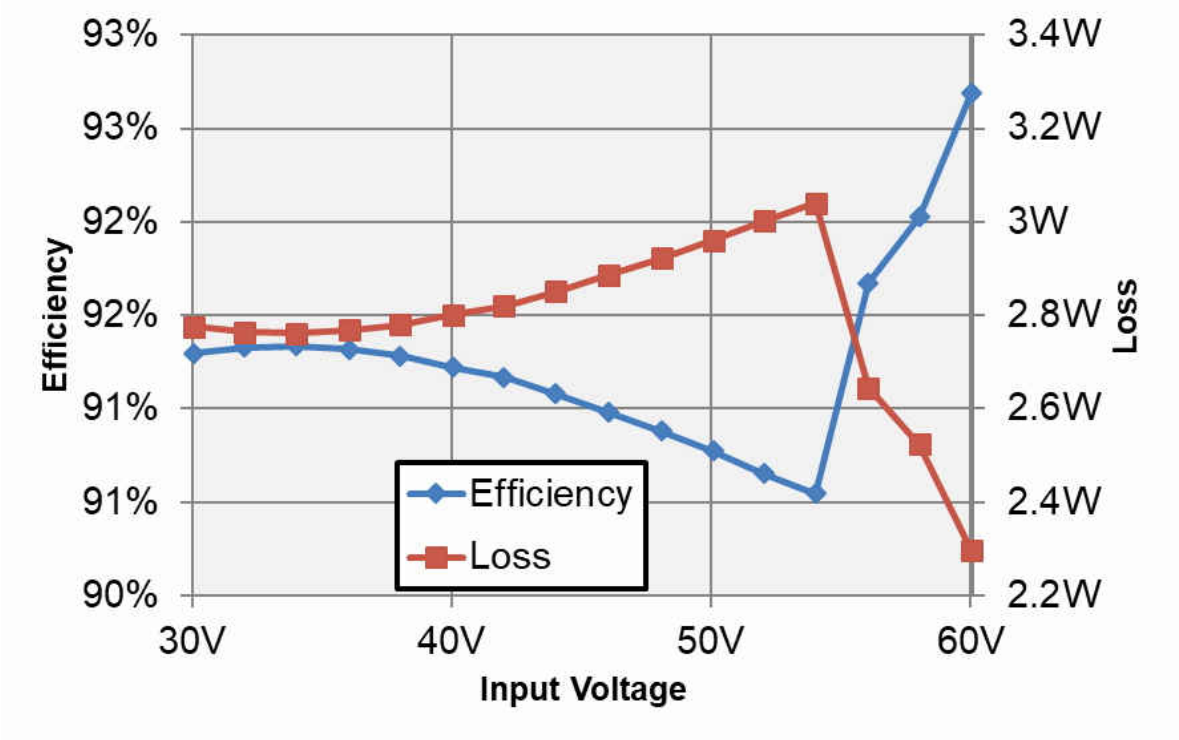


Figure 2-10. Loss and Efficiency vs Input Voltage

2.5 Thermal Images

These images have been taken after 30 minutes of operation at full load and 600 mA each.

Note

For the final application, 48-V output voltage is just needed for less than one second.

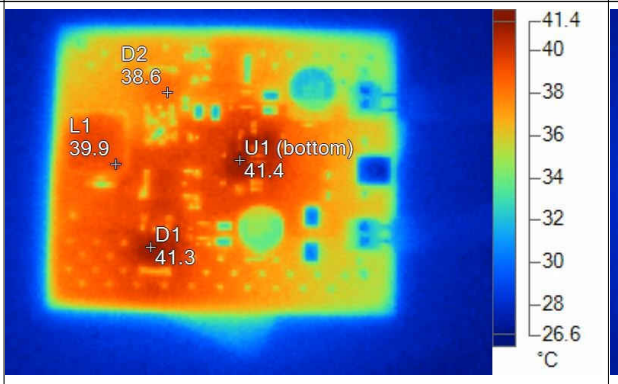
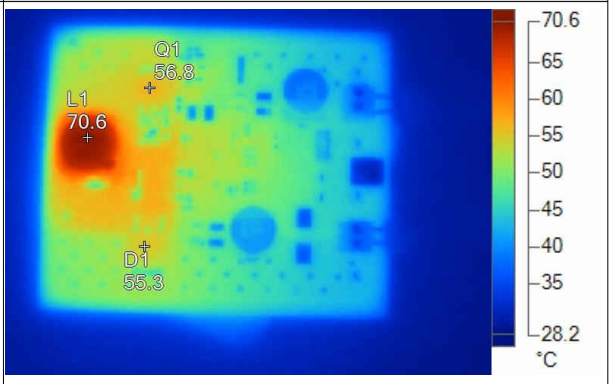
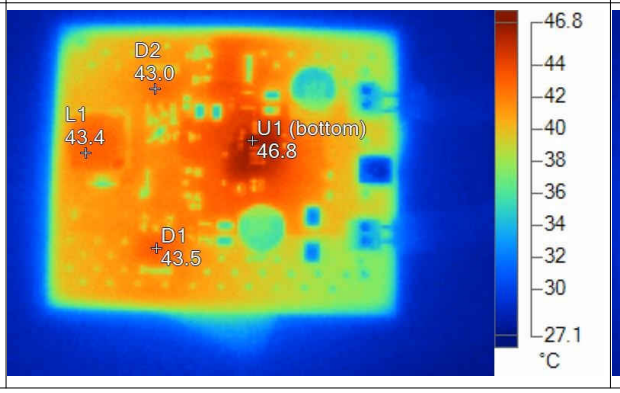
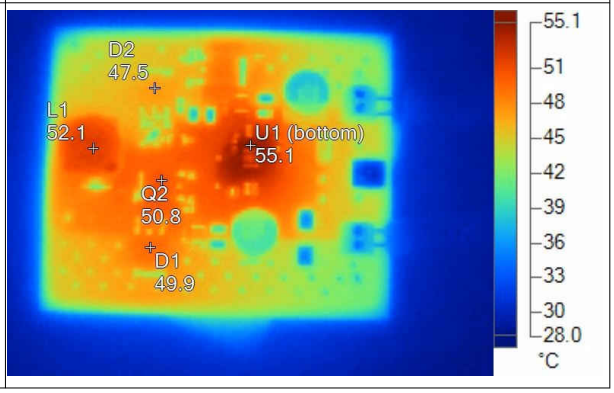
	24 V_{OUT}	48 V_{OUT}
30 V_{IN}		
60 V_{IN}		

Table 2-1. Temperature Comparison

Name	30 V_{IN} 24 V_{OUT}	60 V_{IN} 24 V_{OUT}	30 V_{IN} 48 V_{OUT}	60 V_{IN} 48 V_{OUT}
D1	41.3°C	43.5°C	55.3°C	49.9°C
D2	38.6°C	43.0°C		47.5°C
L1	39.9°C	43.4°C	70.6°C	52.1°C
Q1			56.8°C	
Q2				50.8°C
U1 (bottom)	41.4°C	46.8°C		55.1°C

2.6 Bode Plots

2.6.1 60-V Input Voltage and 24-V Output Voltage

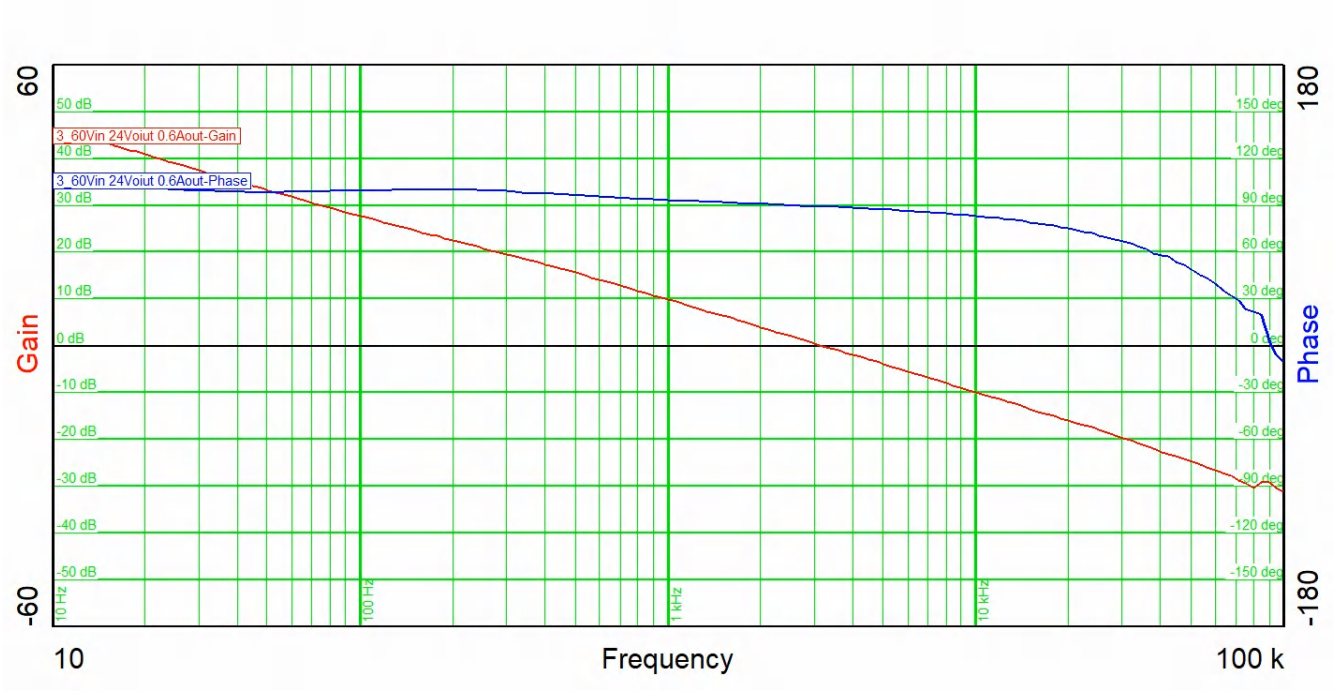


Figure 2-11. Bode Plot for 24 V_{OUT} and 60 V_{IN}, Buck mode

Parameter	Value
Bandwidth (kHz)	3.18
Phase margin	89°
Slope (20 dB / decade)	–1
Gain margin (dB)	–29.6
Slope (20 dB / decade)	–2.6
Freq (kHz)	91

2.6.2 30-V Input Voltage and 48-V Output Voltage

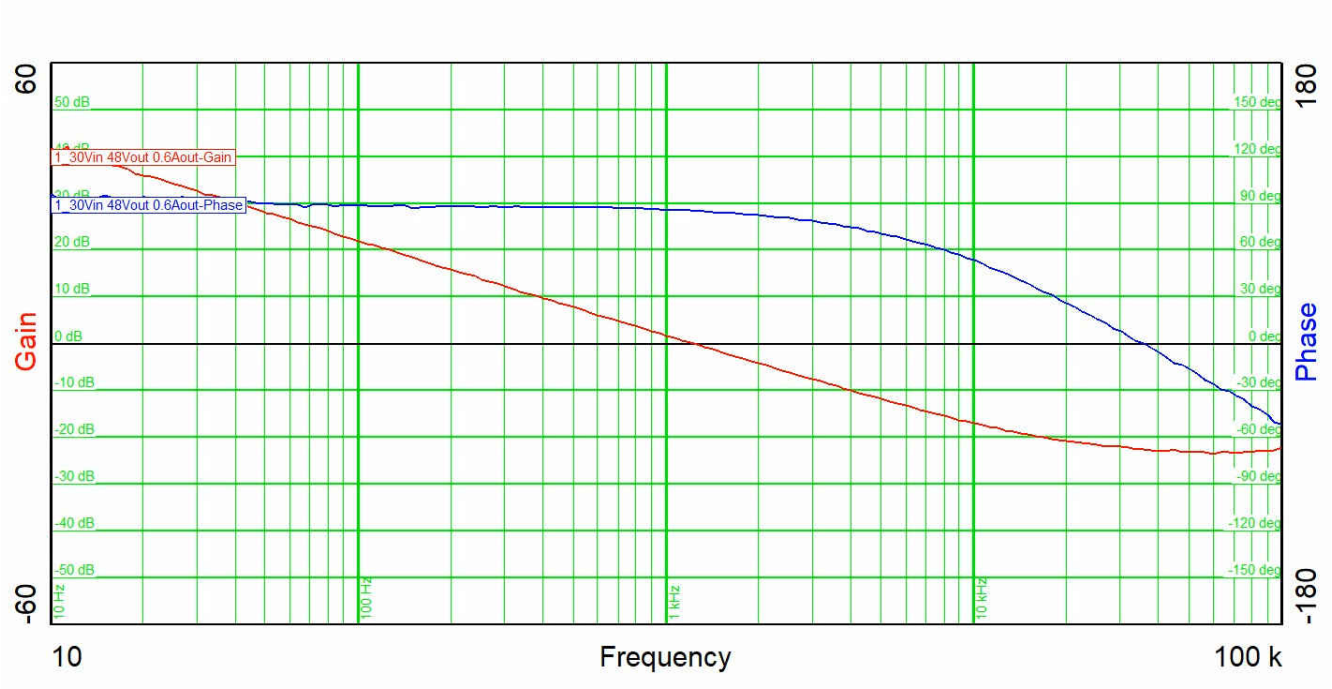


Figure 2-12. Bode Plot for 48 V_{OUT} and 30 V_{IN}, Boost mode - RHPZ at 32 kHz

Parameter	Value
Bandwidth (kHz)	1.23
Phase margin	85°
Slope (20 dB / decade)	–0.98
Gain margin (dB)	–22.6
Slope (20 dB / decade)	–0.49
Freq (kHz)	35.8

2.6.3 Loop Variants

- Rev. A (R12 = 10 kΩ , C15 = 100 nF , C16 = 100 pF) reduces to 600-Hz loop bandwidth
- Rev. B (R12 = 20 kΩ , C15 = 47 nF , C16 = 47 pF) 1200-Hz (default)
- Rev. C (R12 = 40.2 kΩ , C15 = 22 nF , C16 = 22 pF) boosts to 2400 Hz; using loop C for Fco 2.4 kHz still provides phase margin > 70 degrees and gain margin –15 dB

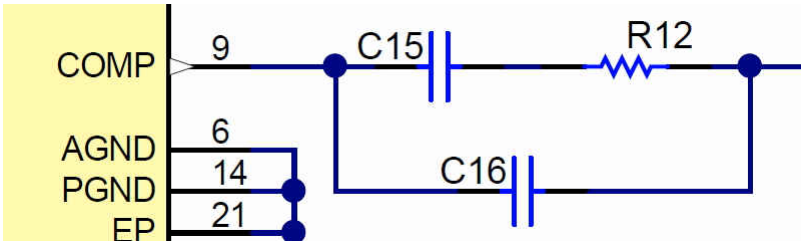


Figure 2-13. Schematic Detail

3 Waveforms

3.1 Switching

Note

With duty cycle greater than 75%, the controller steps into buck-boost mode.

3.1.1 24-V Output Voltage, 30-V Input Voltage (Duty Cycle 80%)

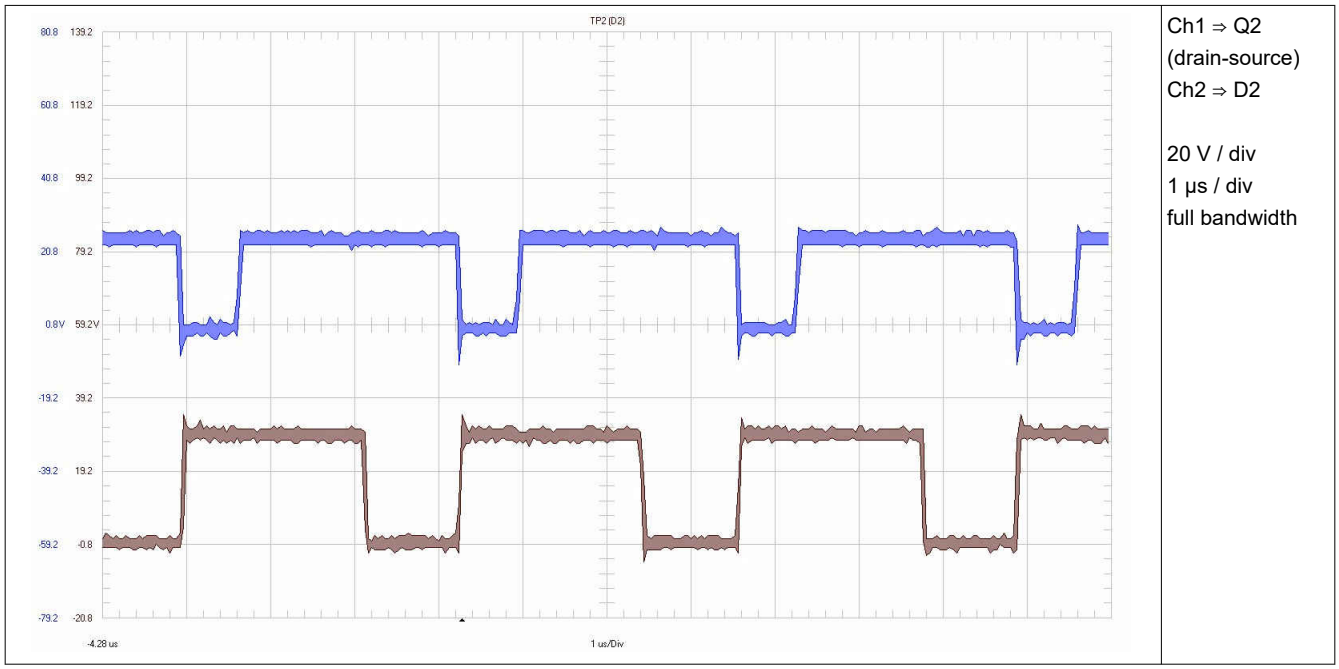


Figure 3-1. Transistor Q2 Drain (TP3) to GND; Diode D2 (TP2) to GND

3.1.1.1 Diode D1

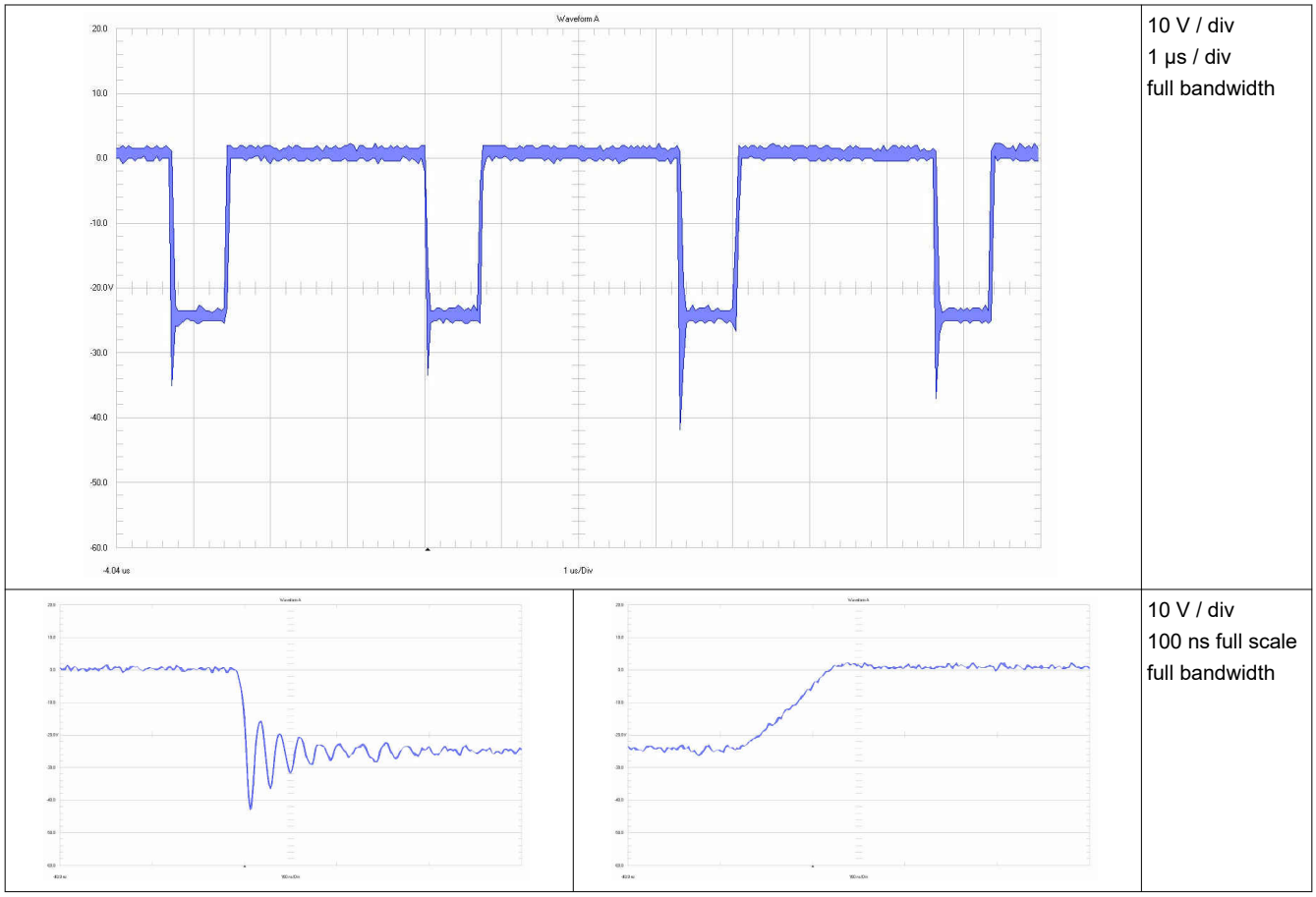


Figure 3-2. Diode D1 Referenced to V_{OUT}

3.1.1.2 Transistor Q2

3.1.1.2.1 Drain - GND

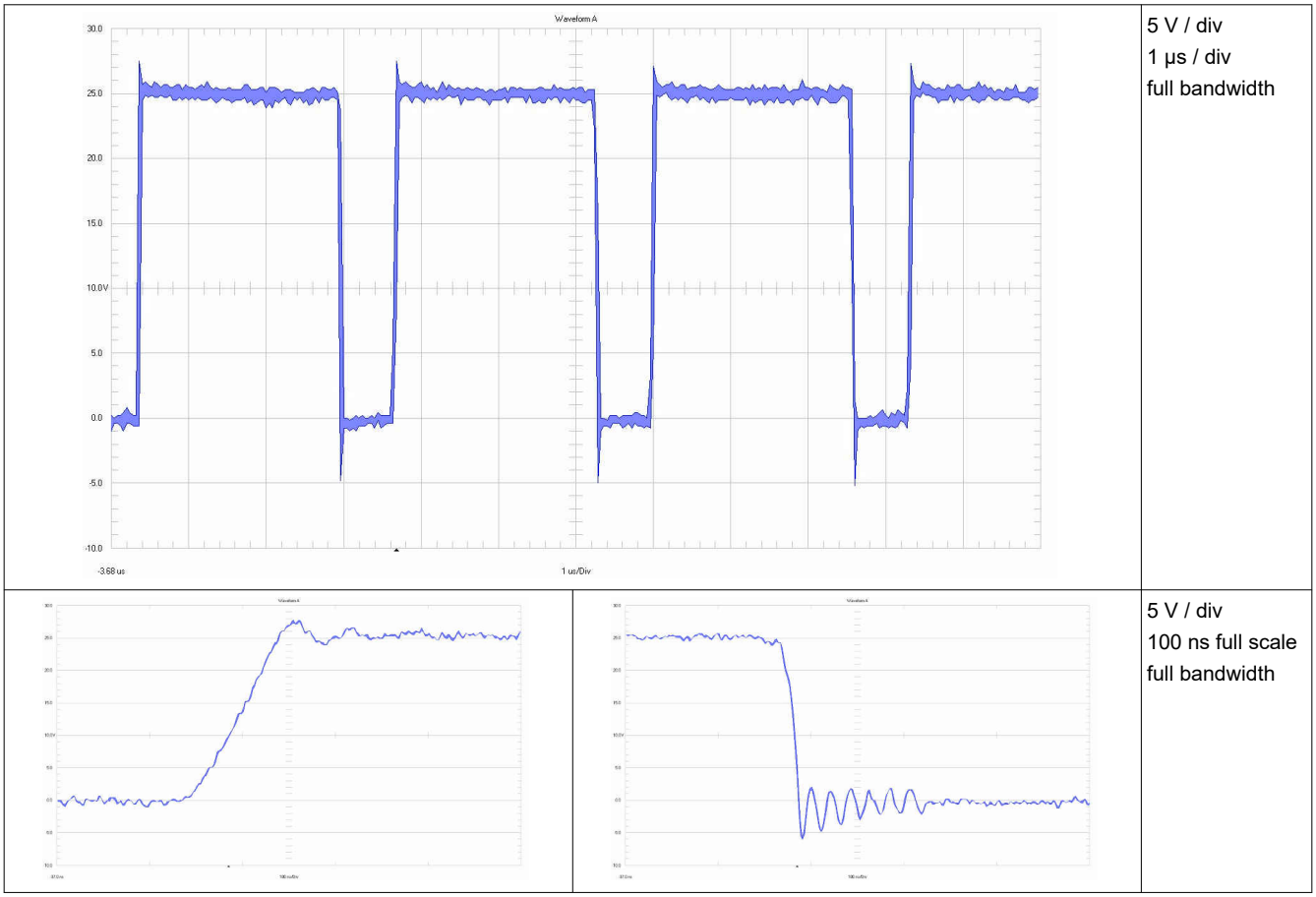


Figure 3-3. Transistor Q2 Drain - GND

3.1.1.2.2 Gate - GND

Note

The final application uses FETs with much lower gate charge QG. A gate resistor (3.3 Ω to 4.7 Ω) might reduce the ringing on the gate.

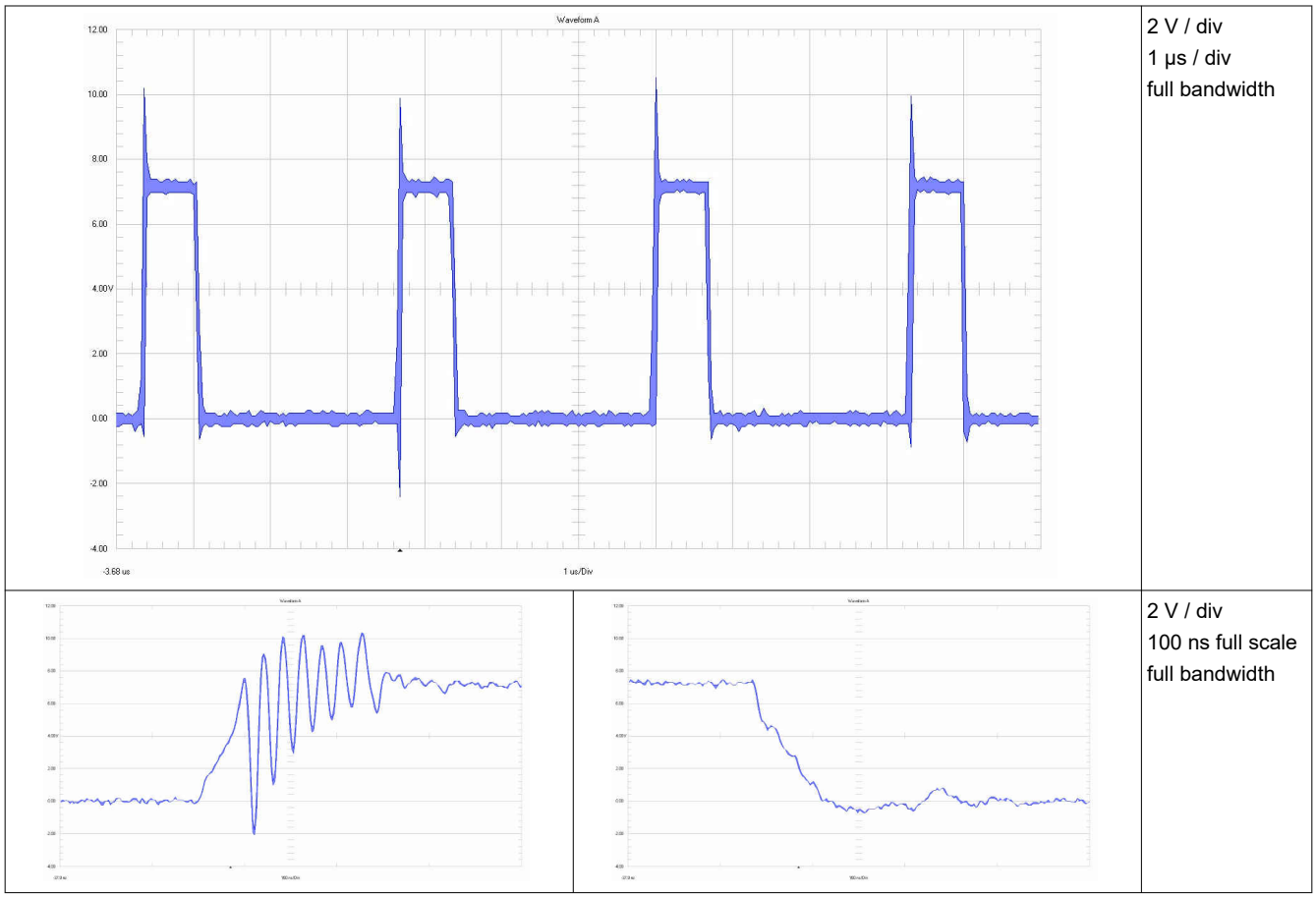


Figure 3-4. Transistor Q2 Gate - GND

3.1.1.3 Diode D2

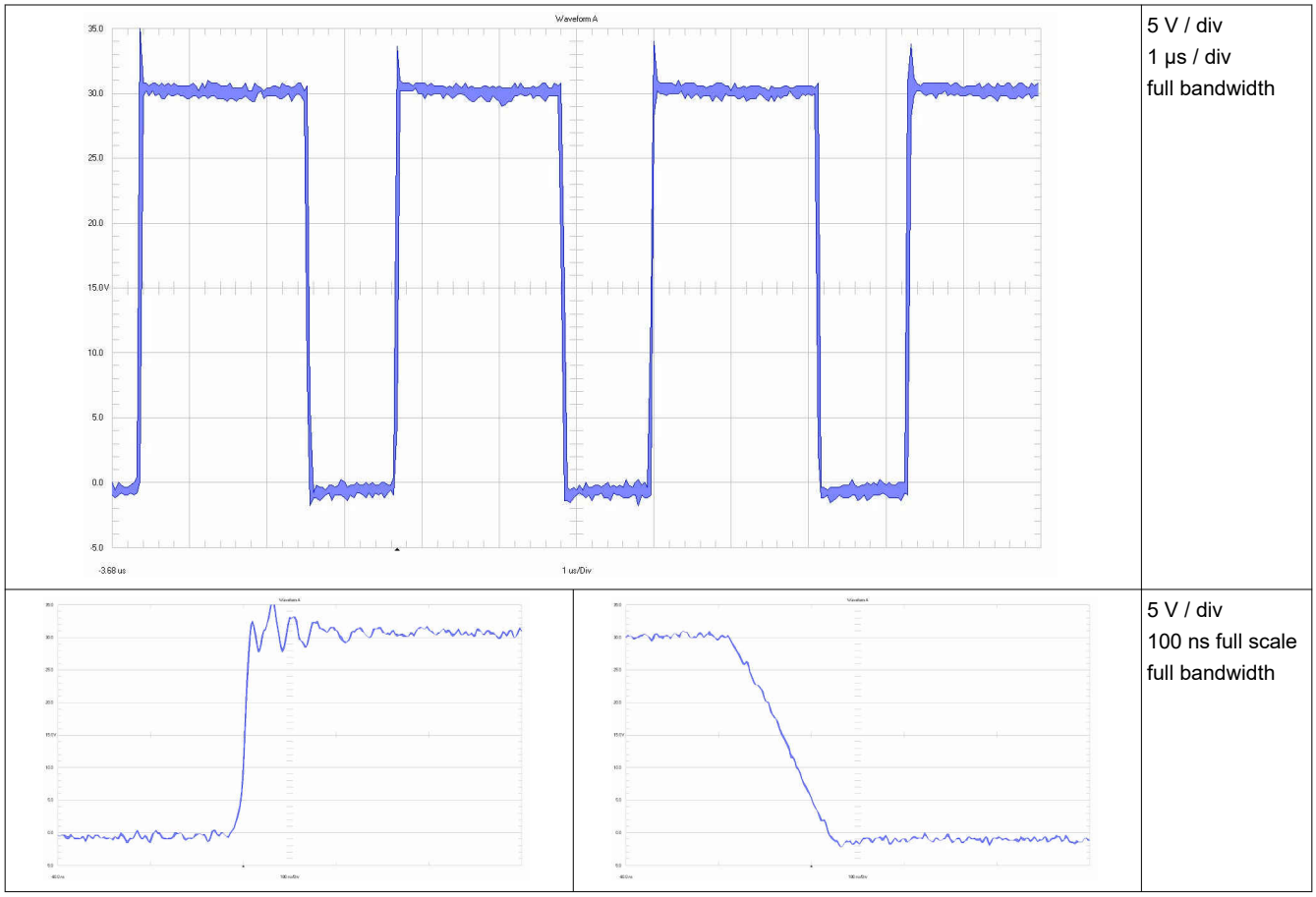
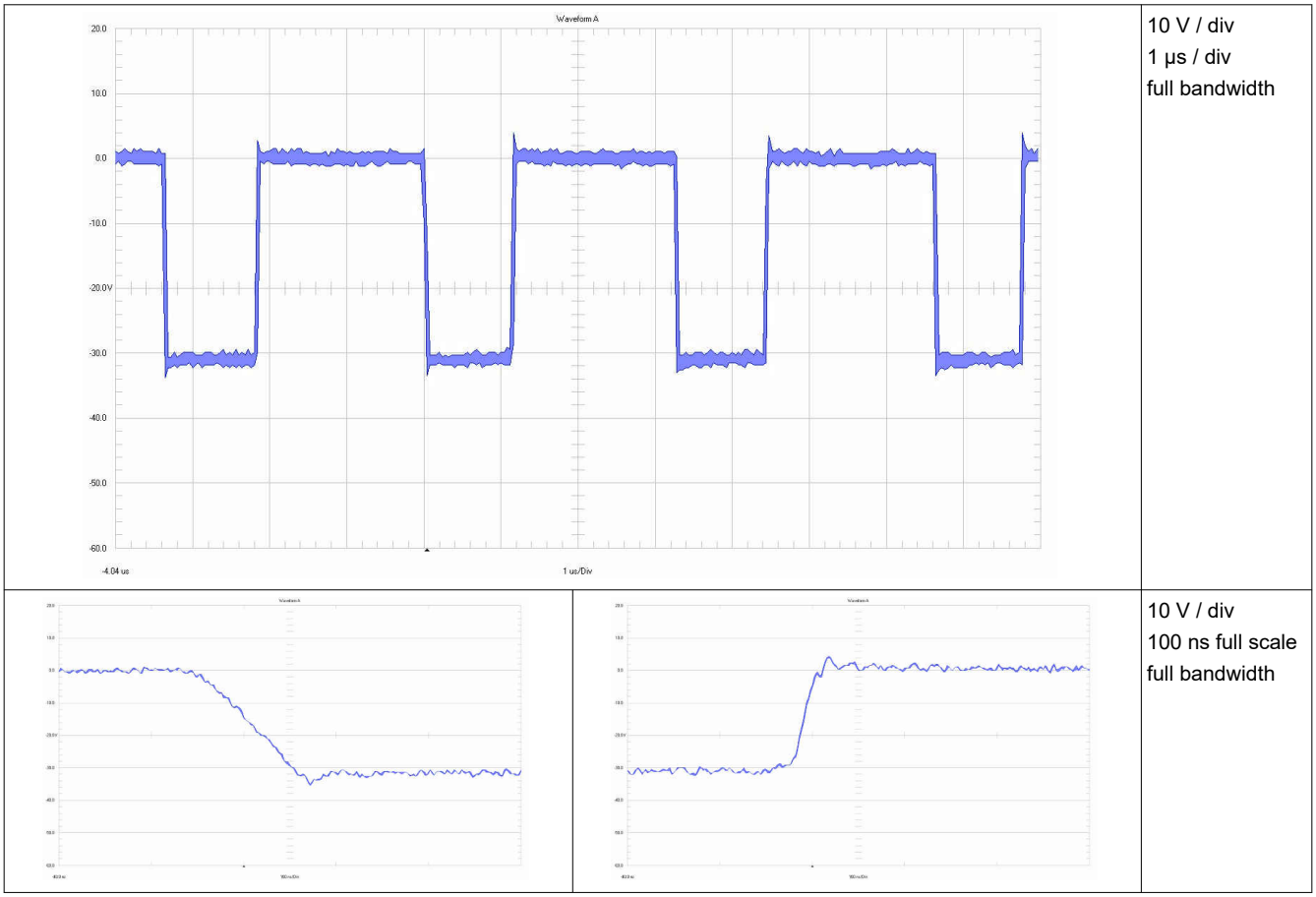


Figure 3-5. Diode D2

3.1.1.4 Transistor Q1

3.1.1.4.1 Source - V_{IN}



	10 V / div 1 µs / div full bandwidth
	10 V / div 100 ns full scale full bandwidth

Figure 3-6. Transistor Q1 Source - Drain (Referenced to V_{IN})

3.1.1.4.2 Gate - Source

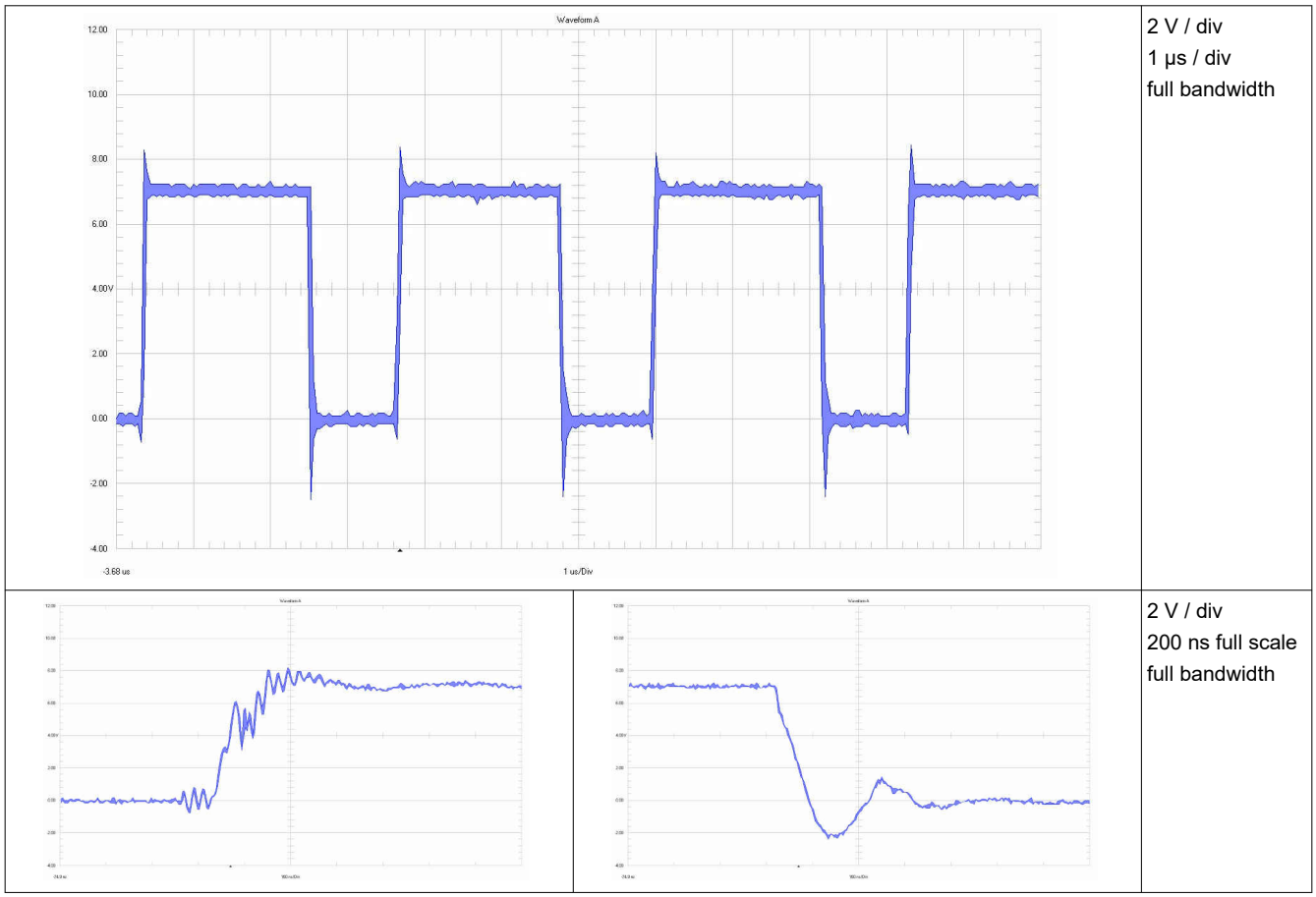
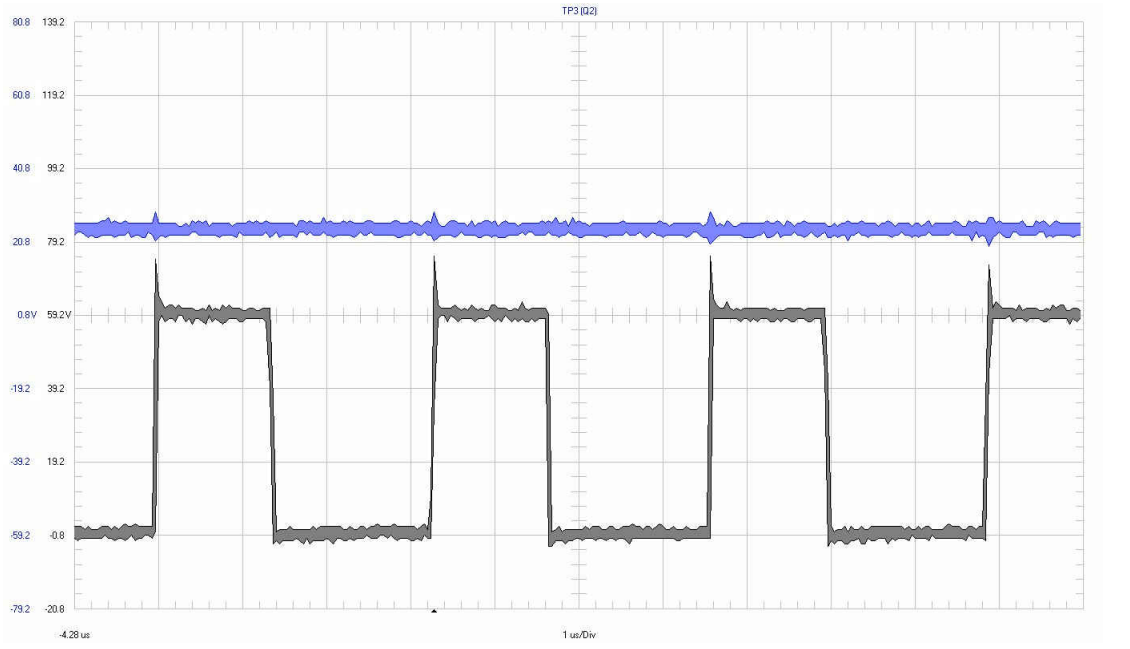


Figure 3-7. Transistor Q1 Gate - Source

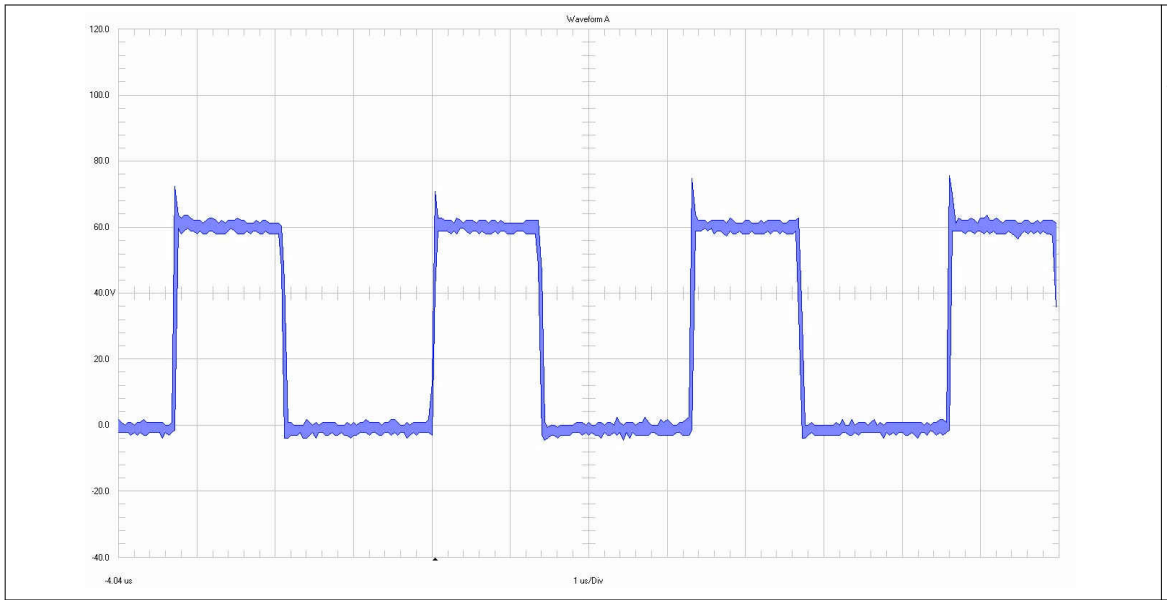
3.1.2 24-V Output Voltage; 60-V Input Voltage



The duty-cycle is 40%. The circuit works in pure buck mode.

Figure 3-8. Transistor Q2 Drain (TP3) to GND; Diode D2 (TP2) to GND

3.1.2.1 Diode D2

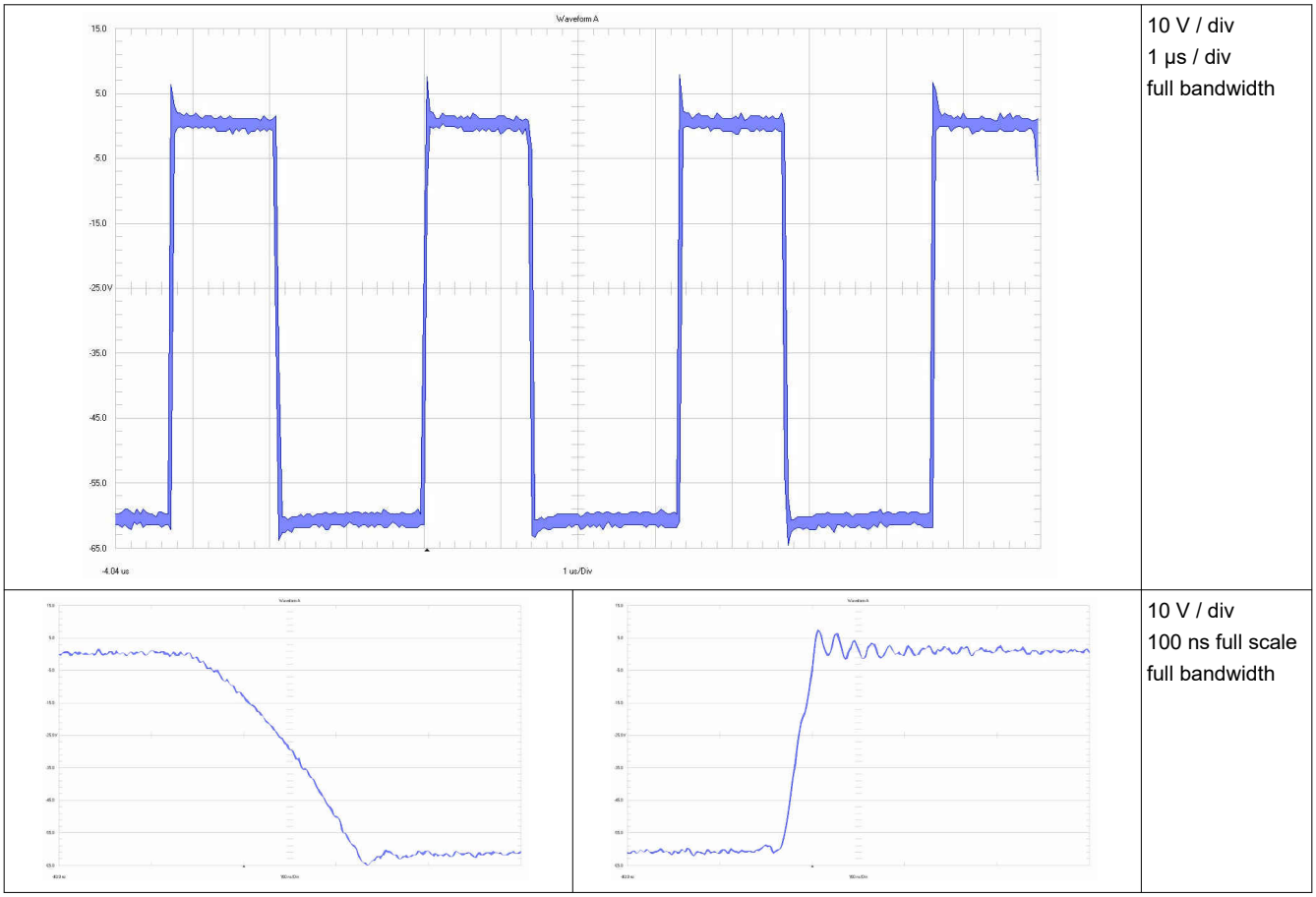


	20 V / div 1 µs / div full bandwidth
	20 V / div 100 ns full scale full bandwidth

Figure 3-9. Diode D2

3.1.2.2 Transistor Q1

3.1.2.2.1 Source - V_{IN}



	10 V / div 1 µs / div full bandwidth
	10 V / div 100 ns full scale full bandwidth

Figure 3-10. Transistor Q1 Source - Drain (Referenced to V_{IN})

3.1.2.2.2 Gate-Source

Note

The final application uses FETs with much lower gate charge QG. A gate resistor (3.3 Ω to 4.7 Ω) might reduce the ringing on the gate.

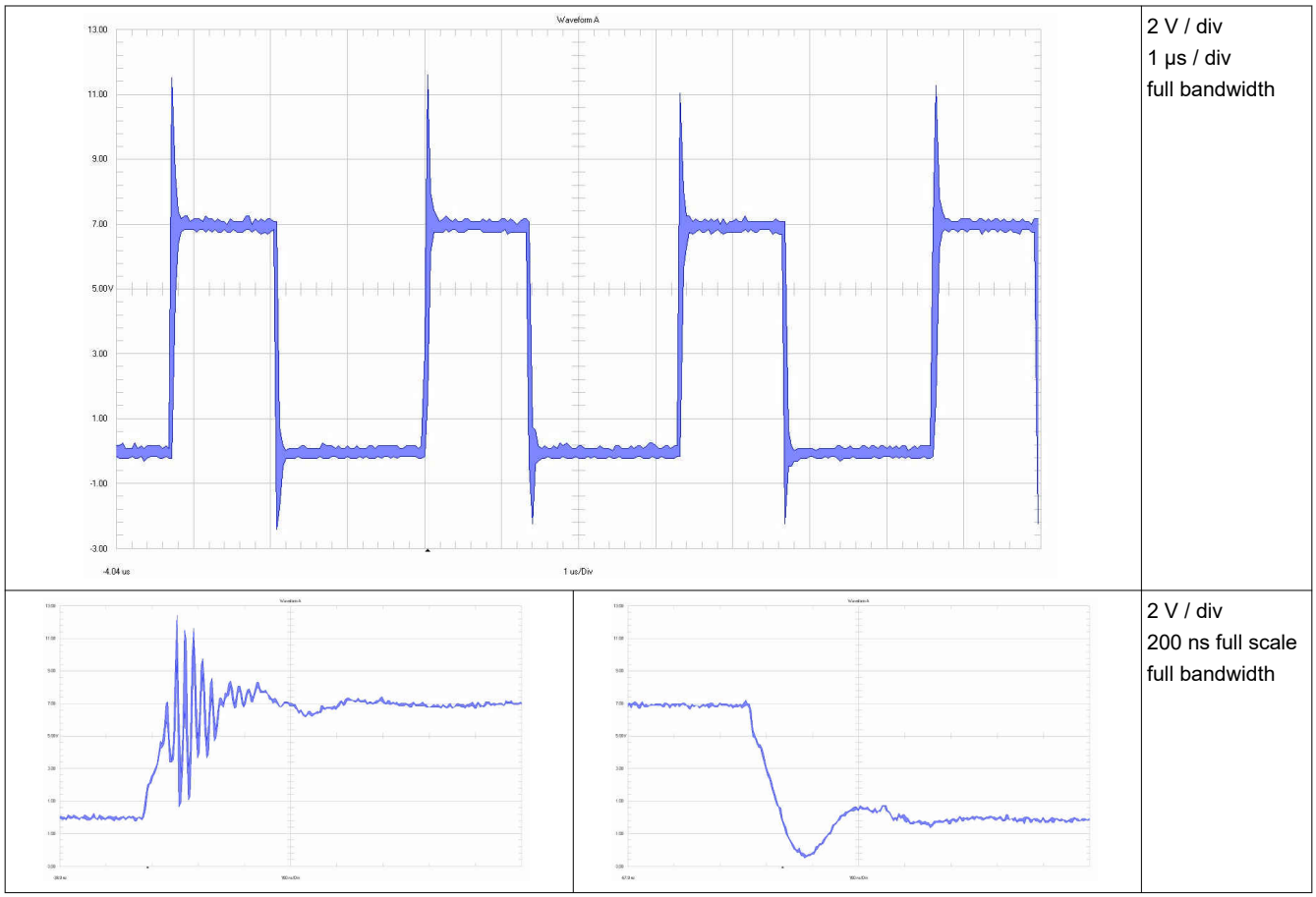


Figure 3-11. Transistor Q1 Gate - Source

3.1.3 48-V Output Voltage; 30-V Input Voltage (Maximum Stress)

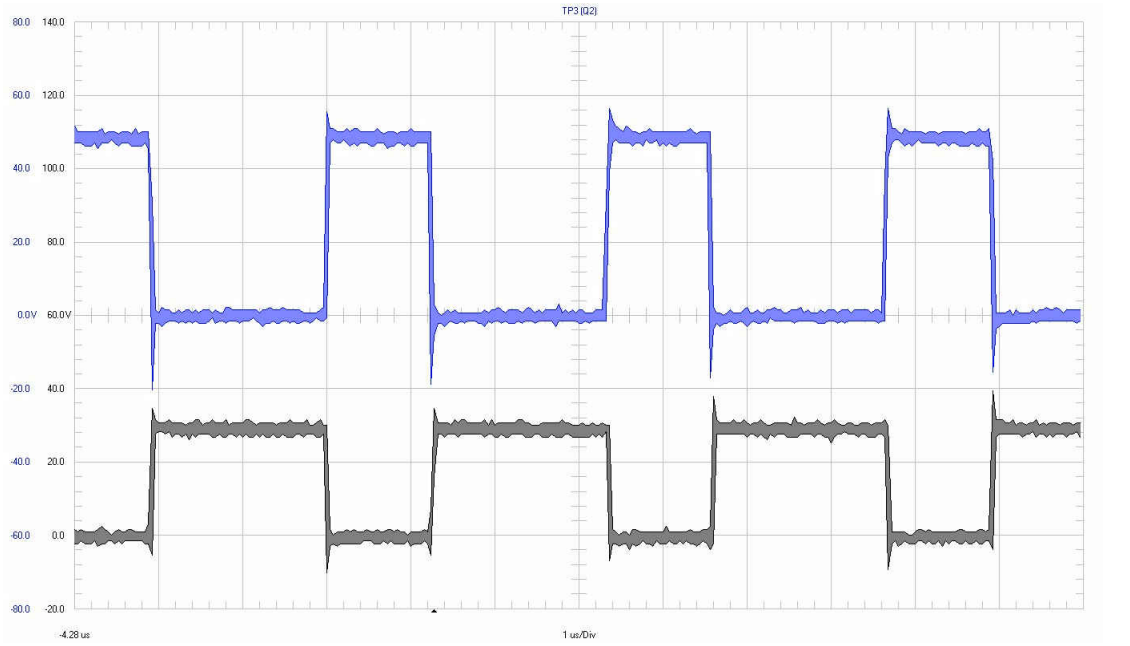
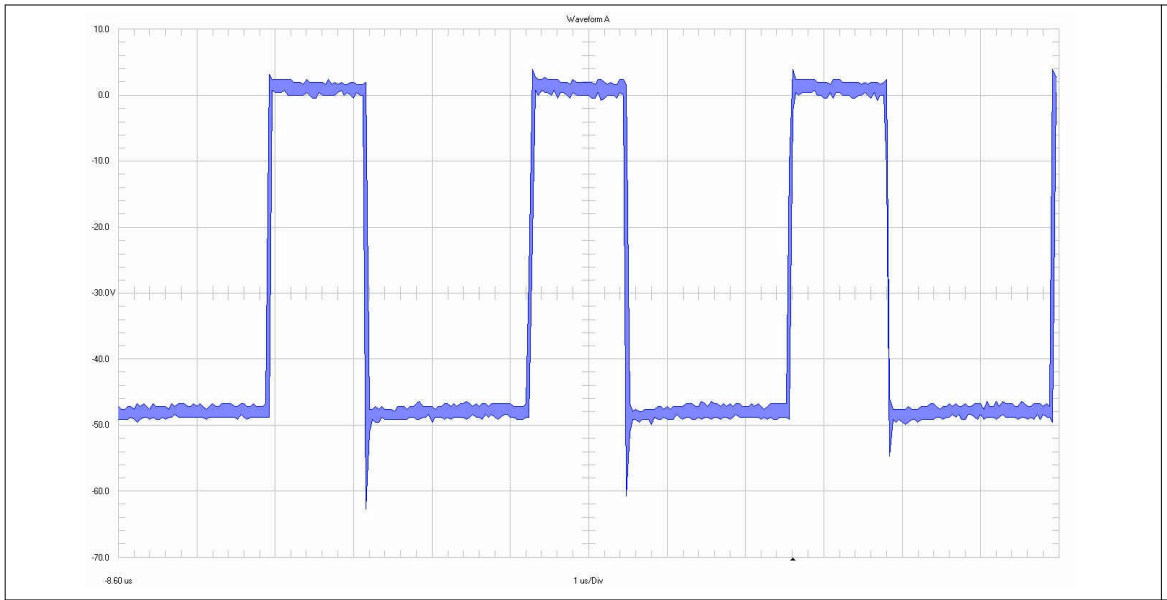


Figure 3-12. Transistor Q2 Drain (TP3) to GND; Diode D2 (TP2) to GND

3.1.3.1 Diode D1



	10 V / div 1 µs / div full bandwidth
	10 V / div 100 ns full scale full bandwidth

Figure 3-13. Diode D1

3.1.3.2 Transistor Q2

3.1.3.2.1 Drain-GND

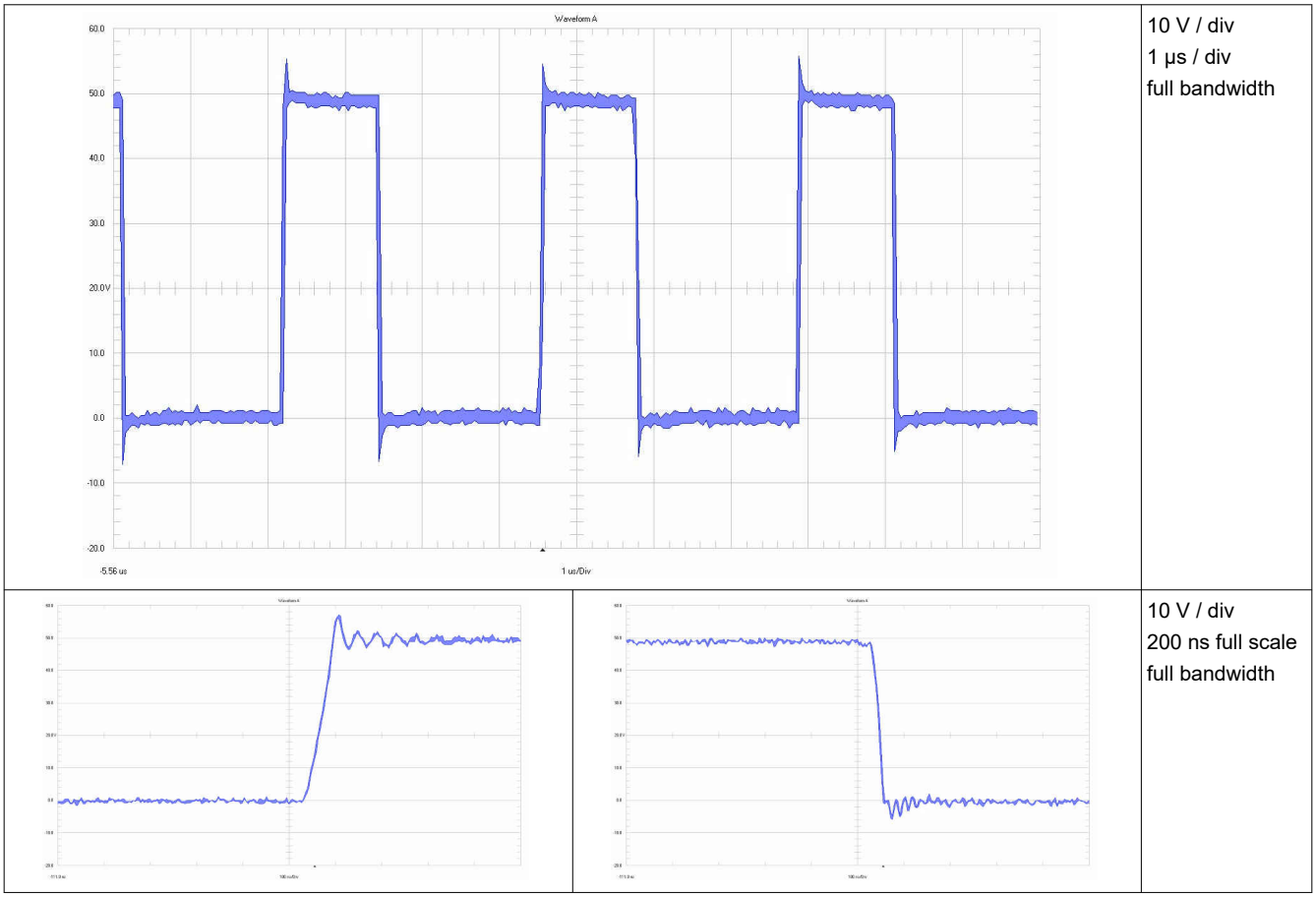


Figure 3-14. Transistor Q2 Drain - GND

3.1.3.2.2 Gate-GND

Note

The final application uses FETs with much lower gate charge QG. A gate resistor (3.3 Ω to 4.7 Ω) might reduce the ringing on the gate.

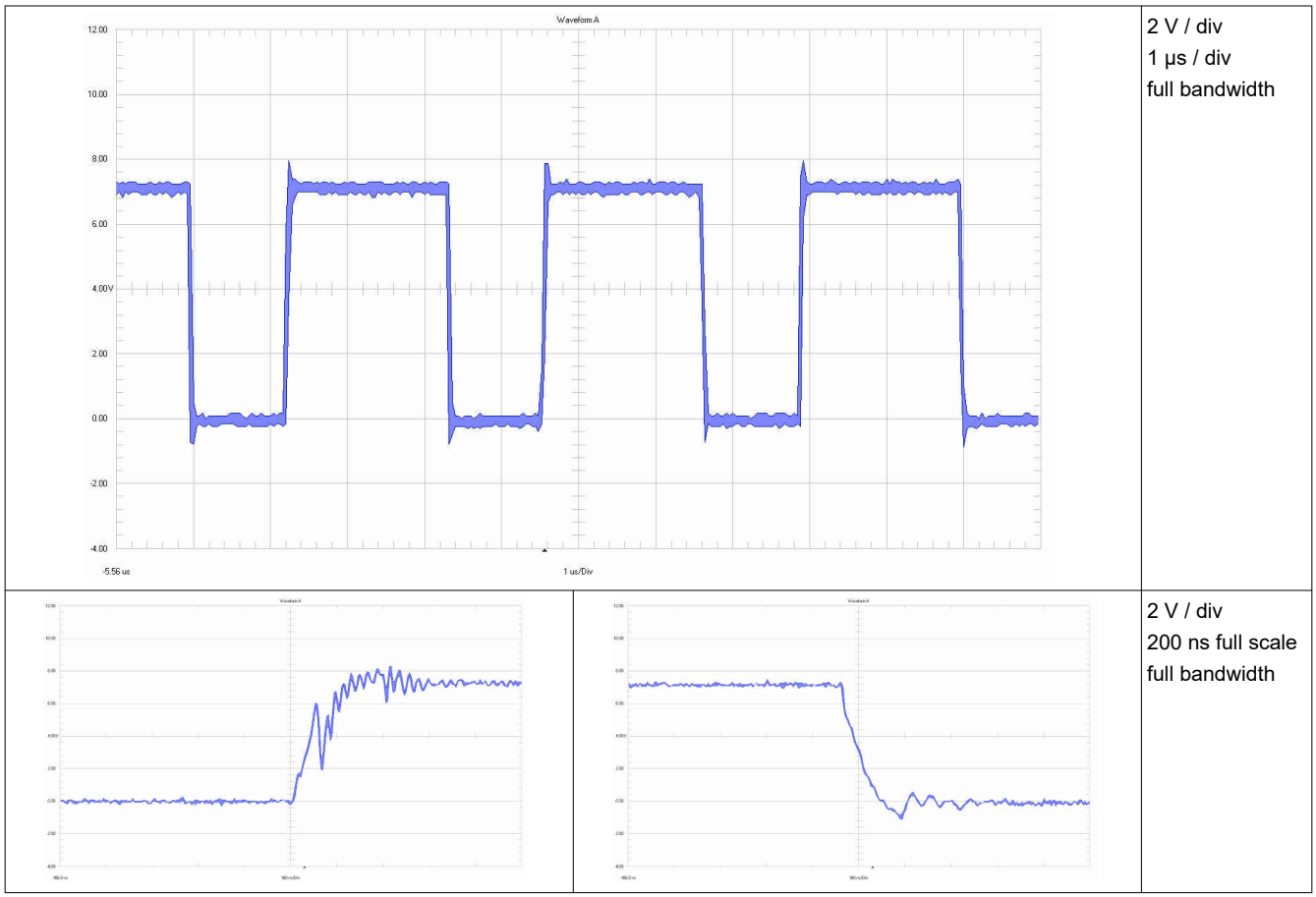


Figure 3-15. Transistor Q2 Gate - GND

3.1.3.3 Diode D2

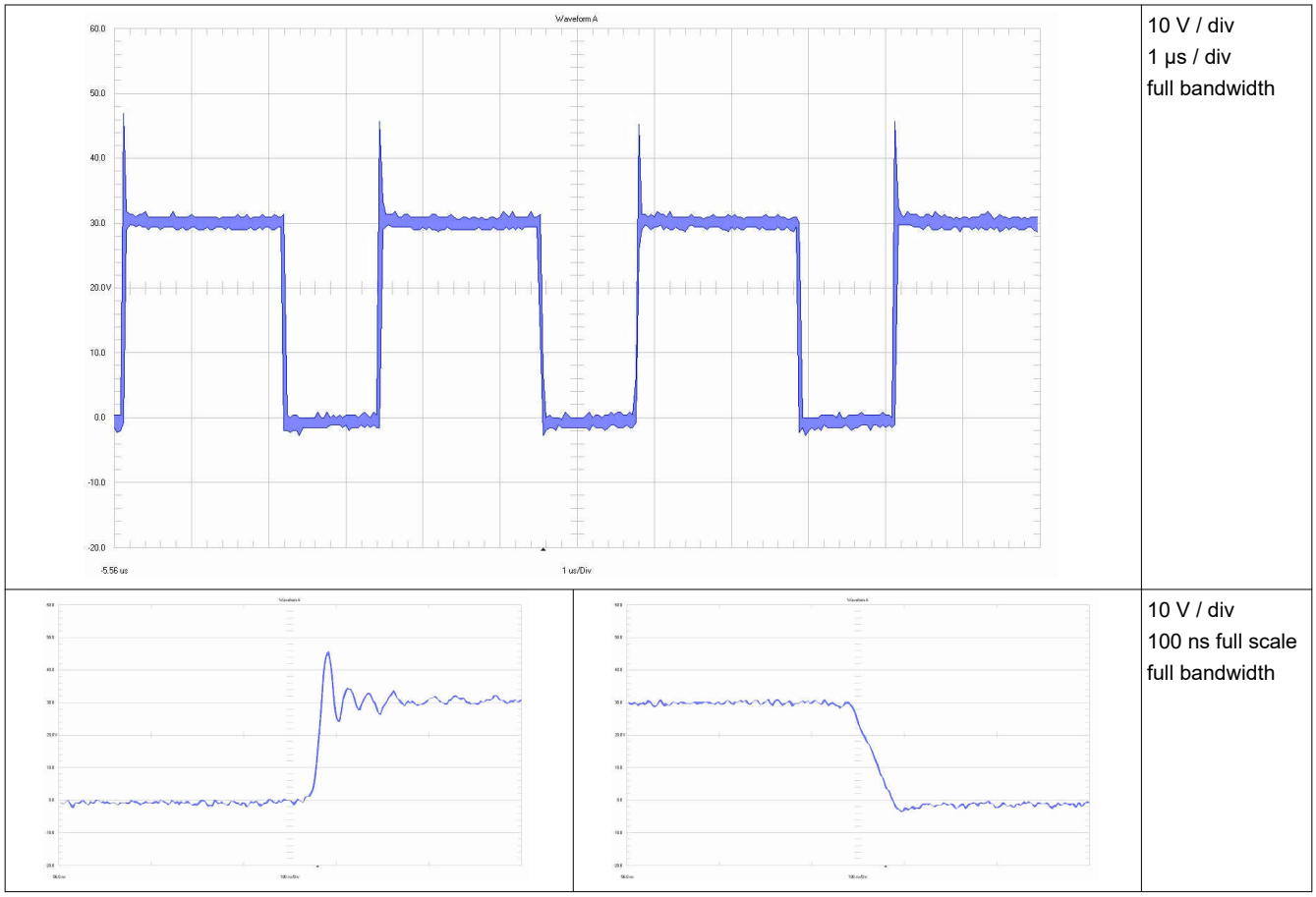
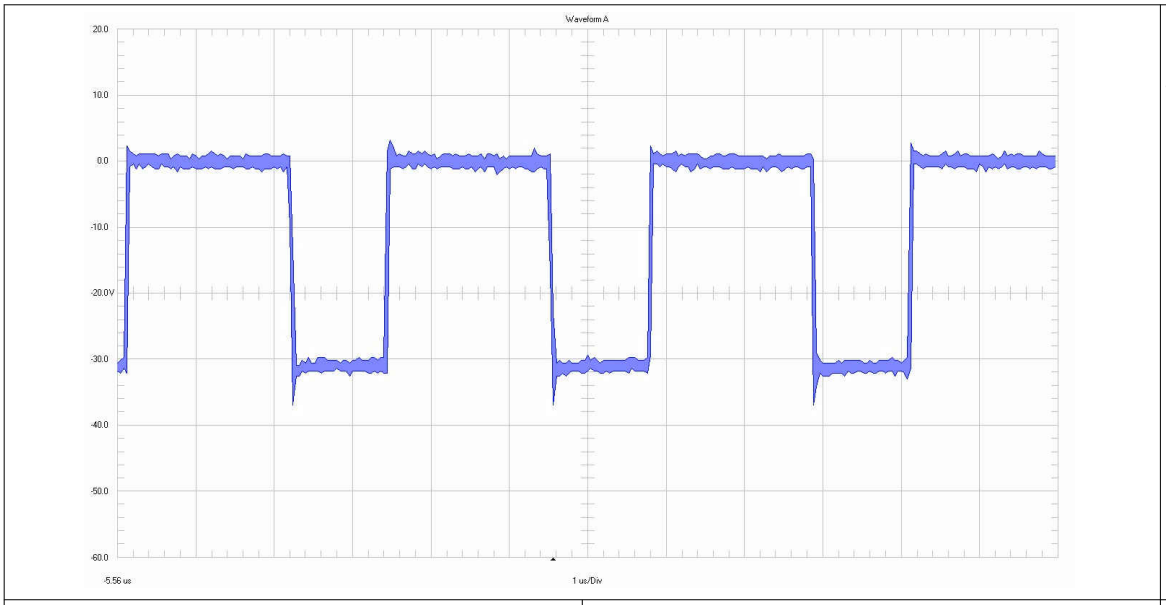


Figure 3-16. Diode D2

3.1.3.4 Transistor Q1

3.1.3.4.1 Source - V_{IN}



	10 V / div 1 µs / div full bandwidth
	10 V / div 200 ns full scale full bandwidth

Figure 3-17. Transistor Q1 Source-Drain (referenced to V_{IN})

3.1.3.4.2 Gate - Source

Note

The final application uses FETs with much lower gate charge QG. A gate resistor (3.3 Ω to 4.7 Ω) might reduce the ringing on the gate.

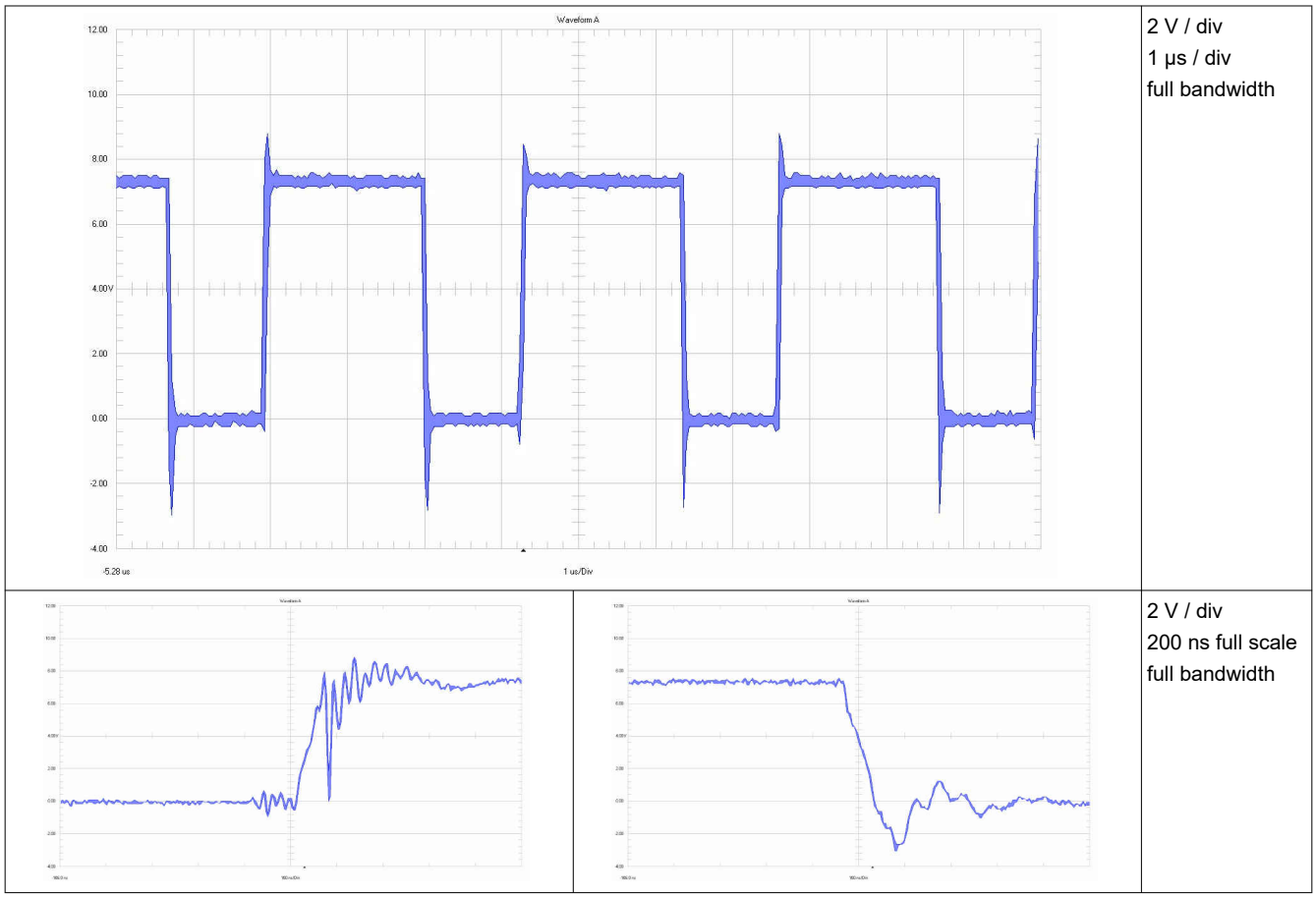


Figure 3-18. Transistor Q1 Gate - Source

3.1.4 48-V Output Voltage; 60-V Input Voltage

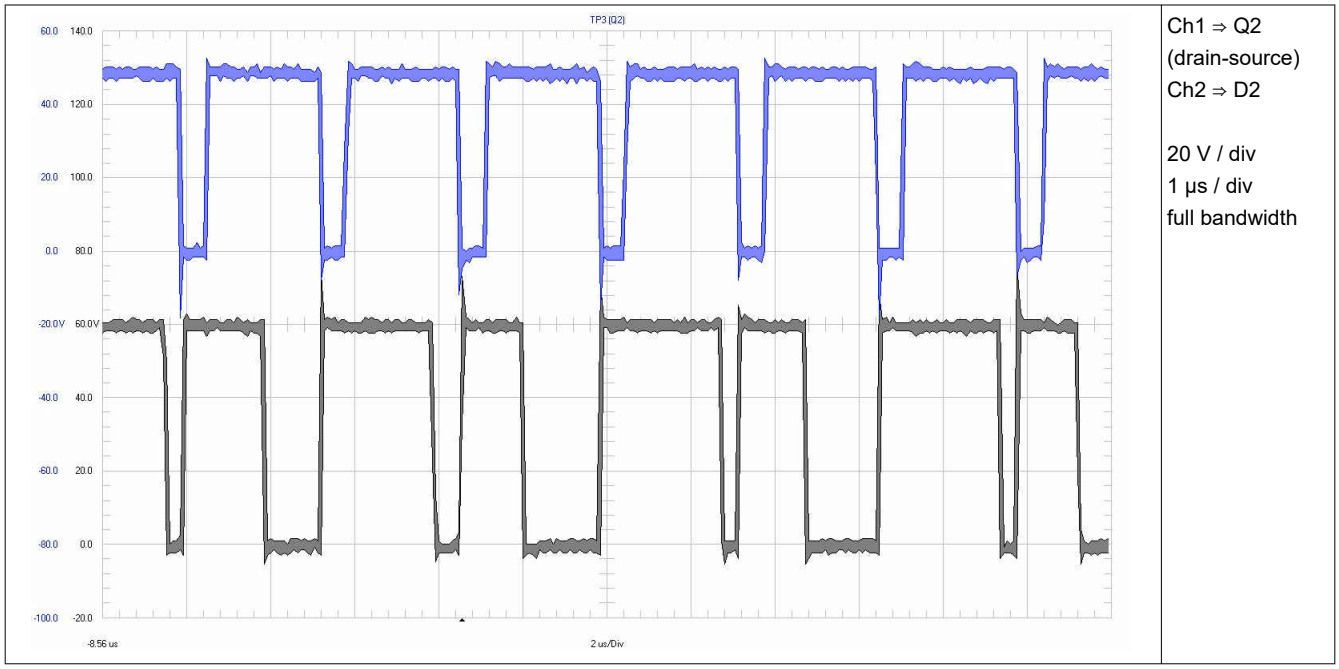


Figure 3-19. Transistor Q2 Drain (TP3) to GND; Diode D2 (TP2) to GND

3.1.4.1 Diode D1

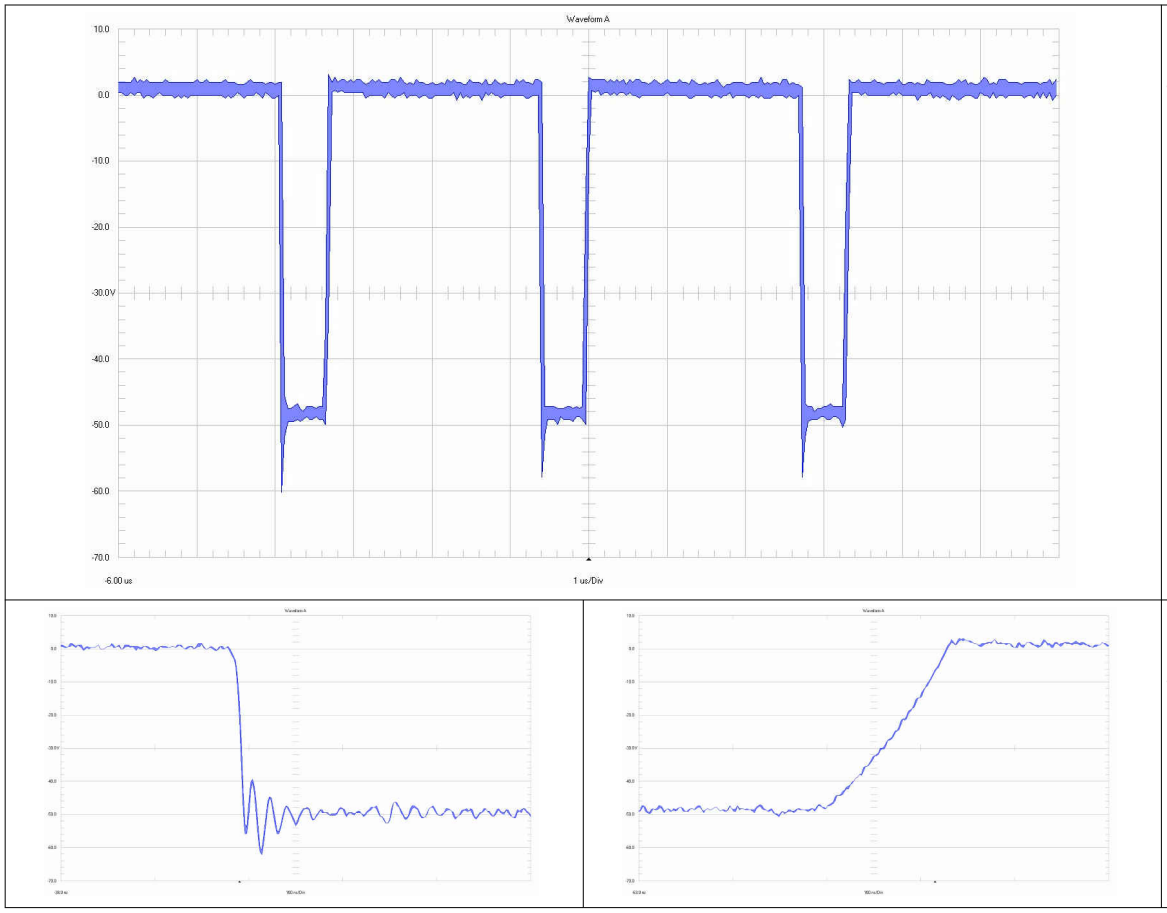


Figure 3-20. Diode D1

3.1.4.2 Transistor Q2

3.1.4.2.1 Drain - GND

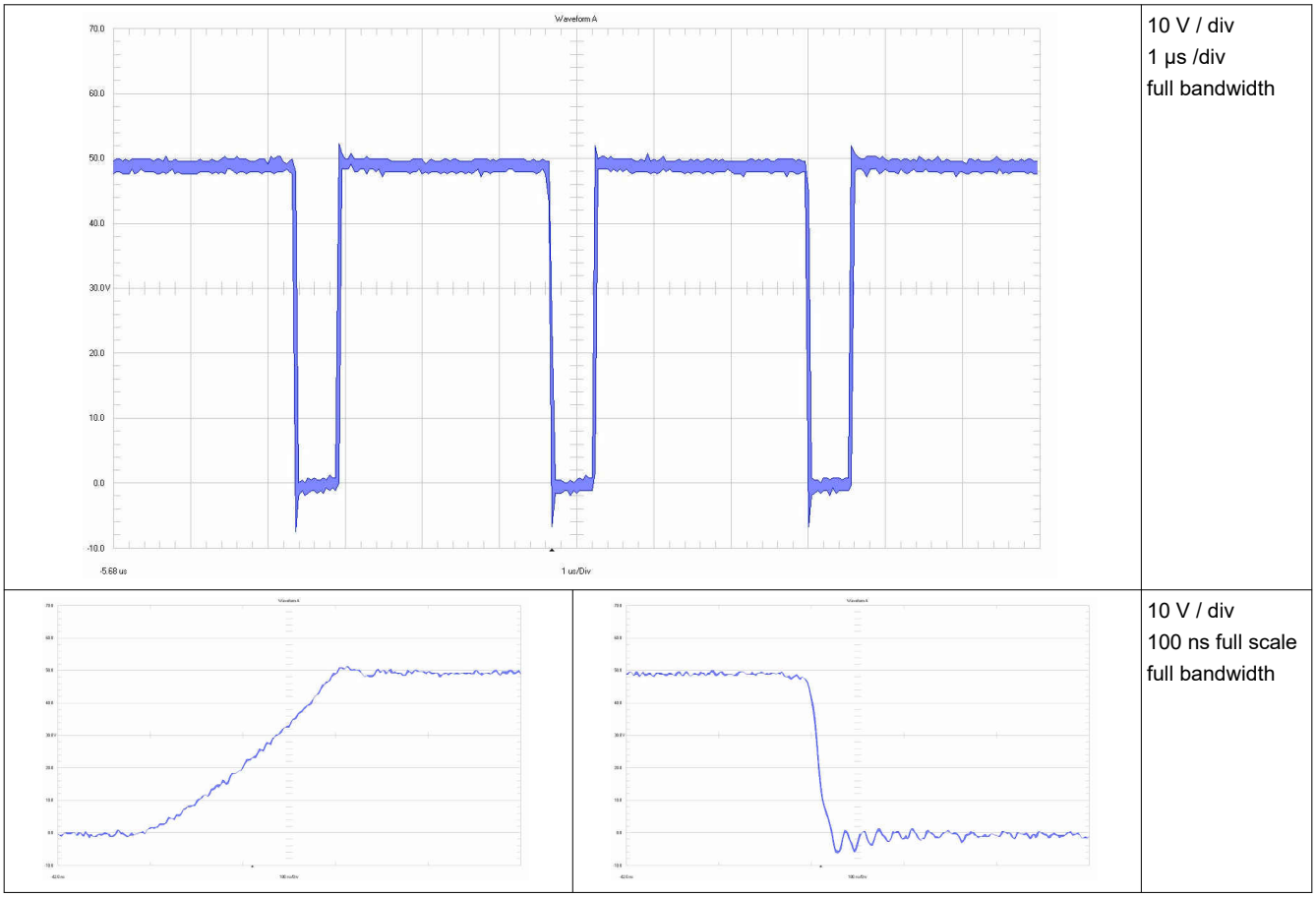


Figure 3-21. Transistor Q2 Drain - GND

3.1.4.2.2 Gate - GND

Note

The final application uses FETs with much lower gate charge QG. A gate resistor (3.3 Ω to 4.7 Ω) might reduce the ringing on the gate.

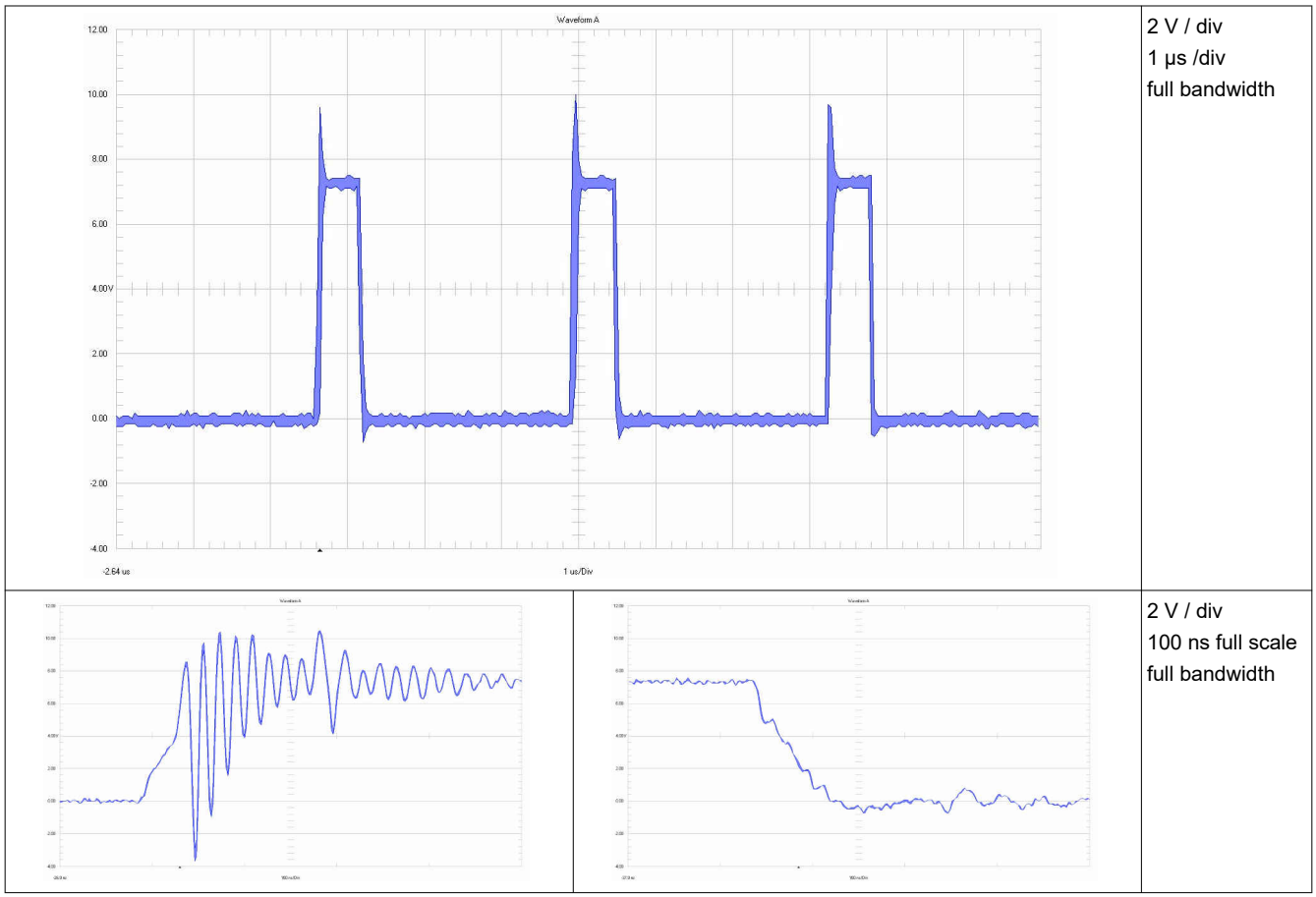
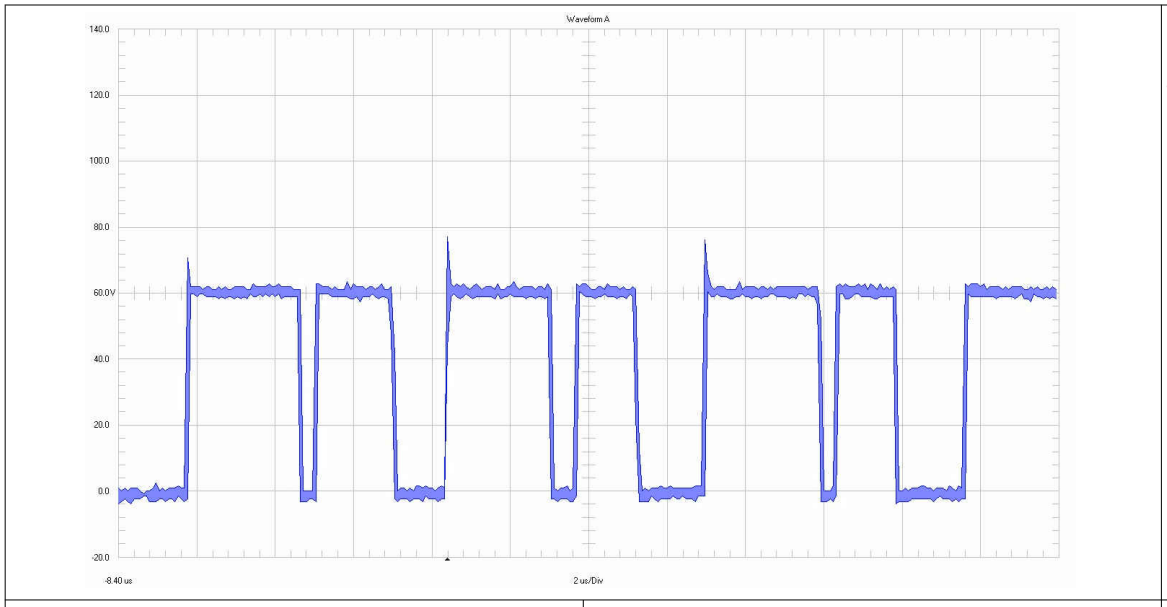


Figure 3-22. Transistor Q2 Gate - GND

3.1.4.3 Diode D2



20 V / div
1 µs / div
full bandwidth

20 V / div
100 ns full scale
full bandwidth

Figure 3-23. Diode D2

3.1.4.4 Transistor Q1

3.1.4.4.1 Source - V_{IN}

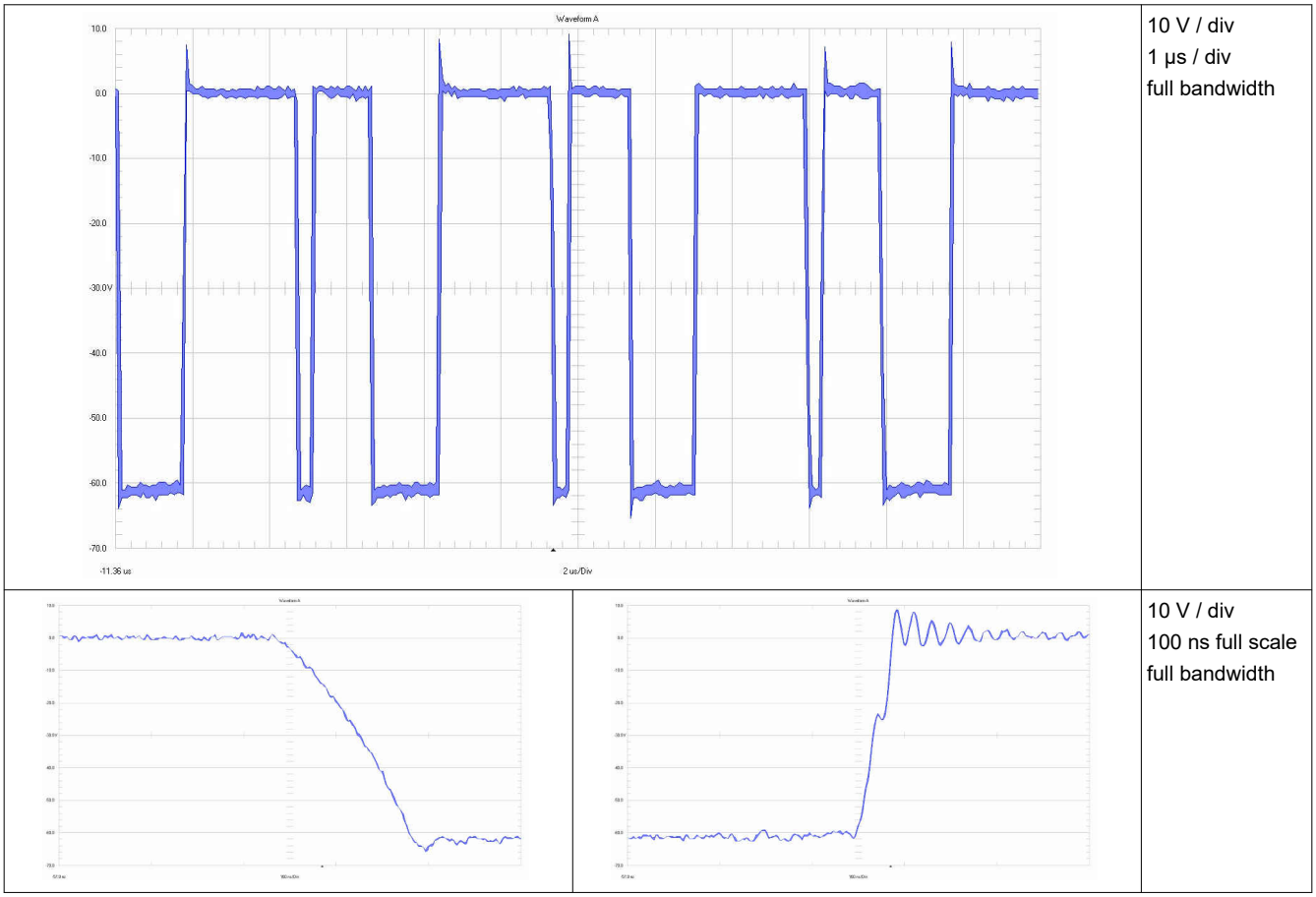


Figure 3-24. Transistor Q1 Source - Drain (Referenced to V_{IN})

3.1.4.4.2 Gate - Source

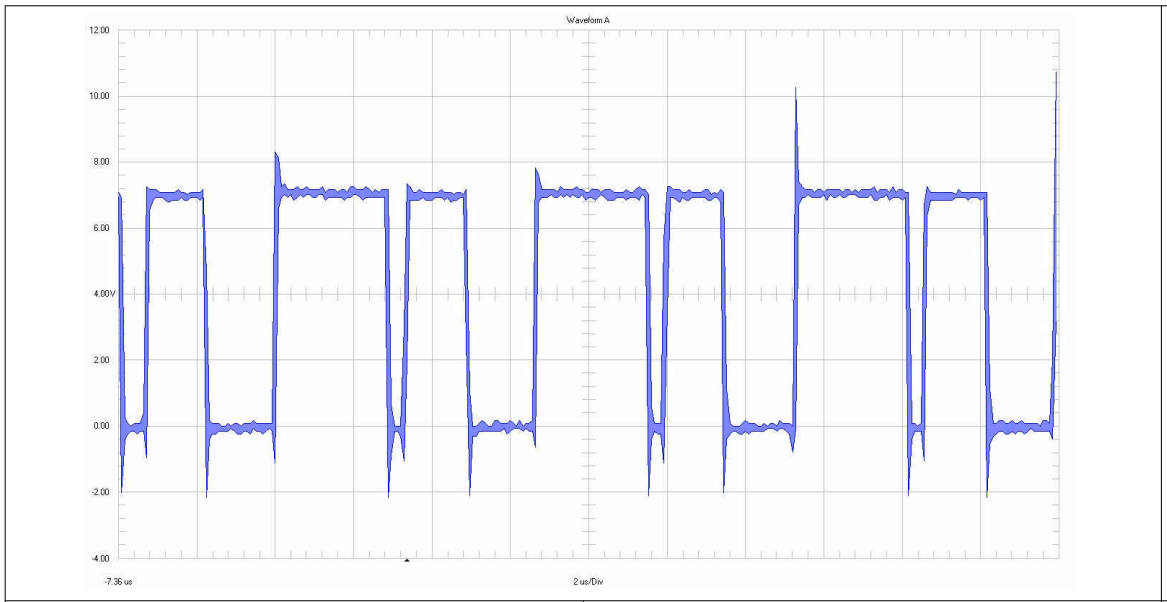


Figure 3-25. Transistor Q1 Gate - Source

3.2 Output Voltage Ripple

Note

Each trace in Figure 3-26 and Figure 3-27 was measured separately.

3.2.1 24-V Output Voltage

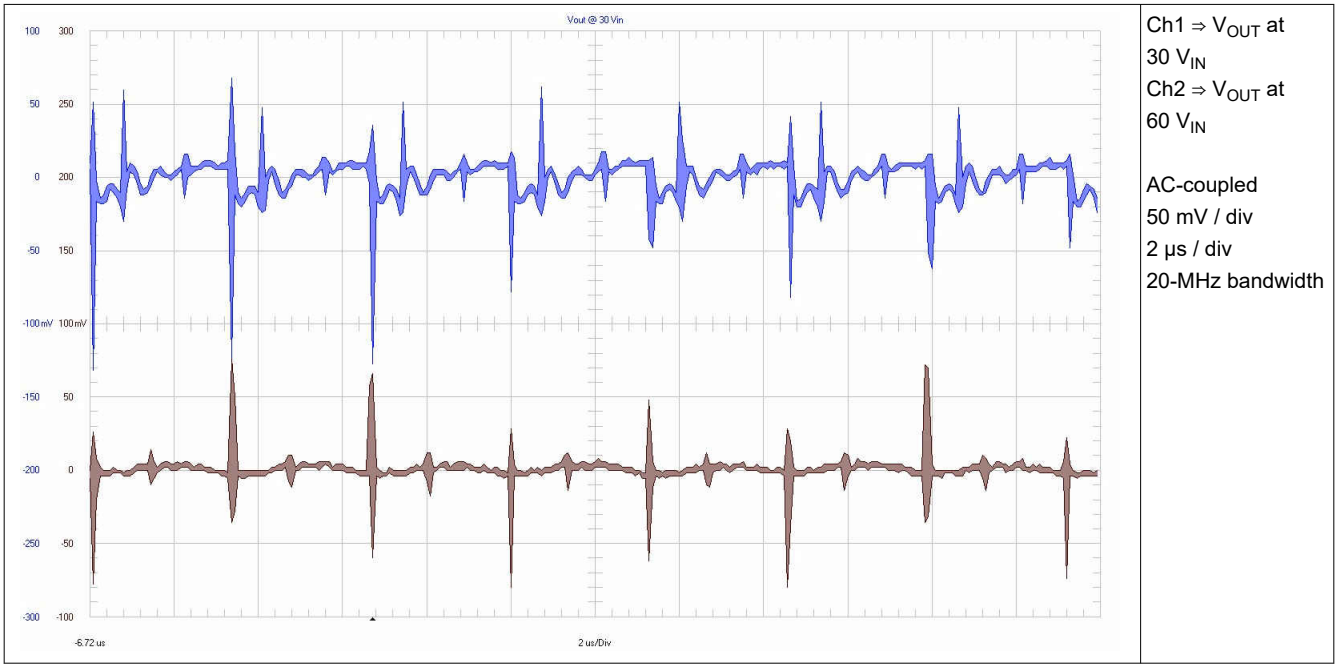


Figure 3-26. Output Voltage Ripple for 24 V_{OUT}

3.2.2 48-V Output Voltage

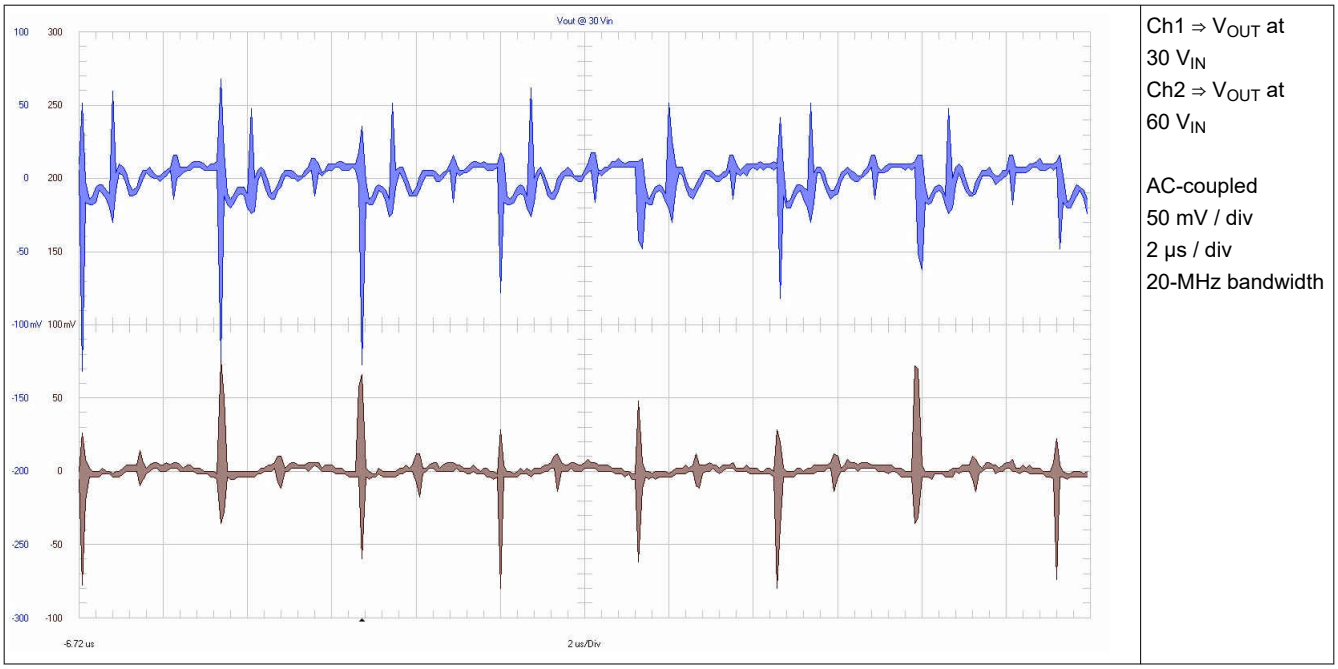


Figure 3-27. Output Voltage Ripple for 48 V_{OUT}

3.3 Input Voltage Ripple

Note

Each trace in Figure 3-28 and Figure 3-29 was measured separately.

3.3.1 24-V Output Voltage

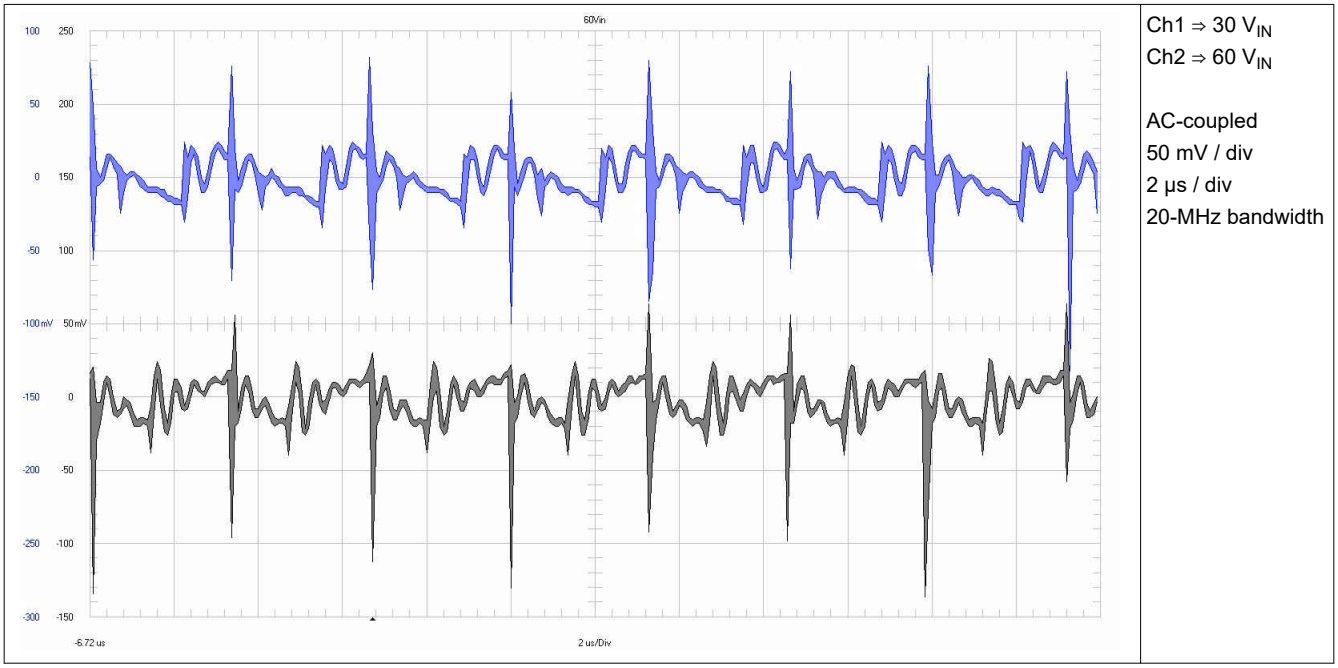


Figure 3-28. Input Voltage Ripple for 24 V_{OUT}

3.3.2 48-V Output Voltage

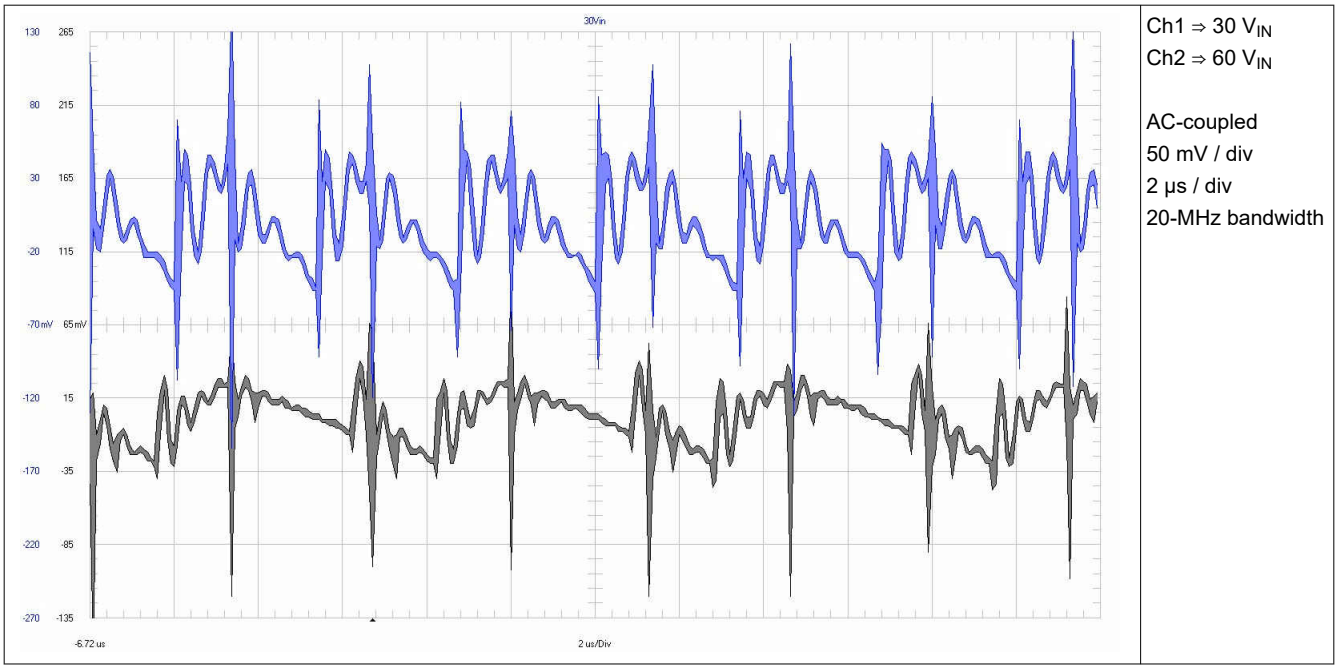


Figure 3-29. Input Voltage Ripple for 48 V_{OUT}

3.4 Load Transients

The electronic load switches between 0.3 A and 0.6 A with a frequency of 75 Hz.

3.4.1 24-V Output Voltage

3.4.1.1 30-V Input Voltage

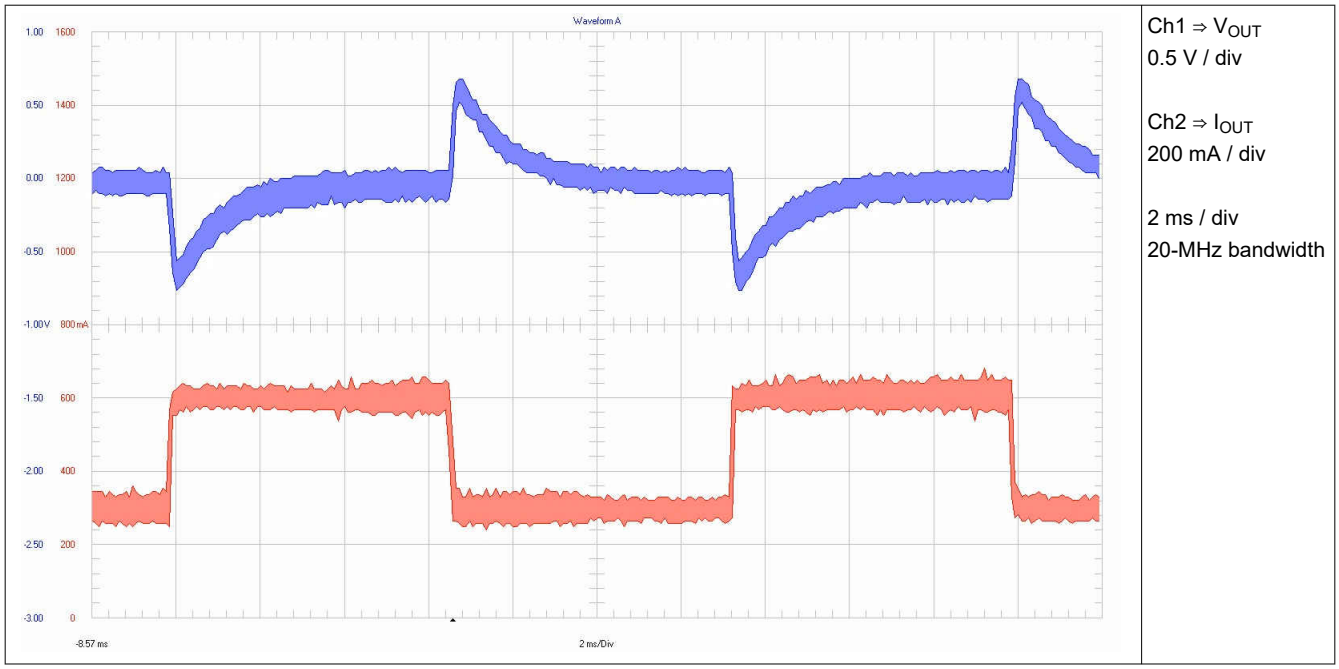


Figure 3-30. Transient at 30 V_{IN} and 24 V_{OUT}

3.4.1.2 60-V Input Voltage

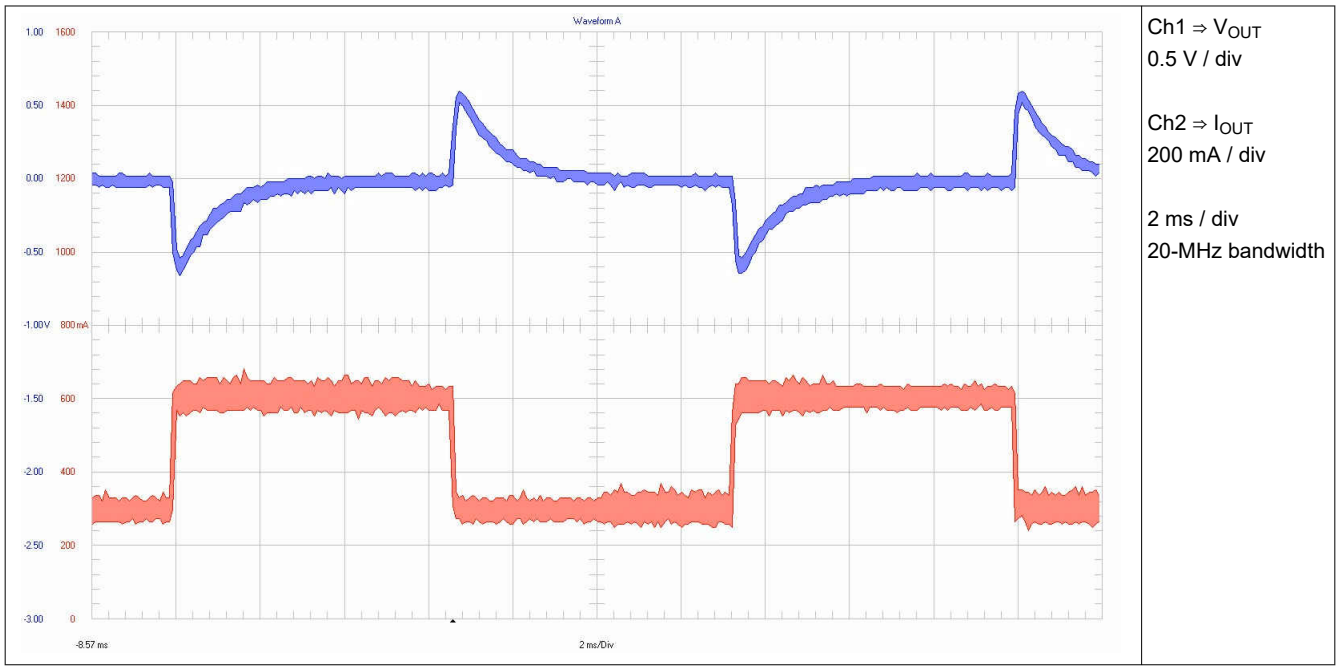


Figure 3-31. Transient at 60 V_{IN} and 24 V_{OUT}

3.4.2 48-V Output Voltage

3.4.2.1 30-V Input Voltage

Note

This voltage combination is the worst case in boost mode due to *Right Half-Plane Zero* (RHPZ).

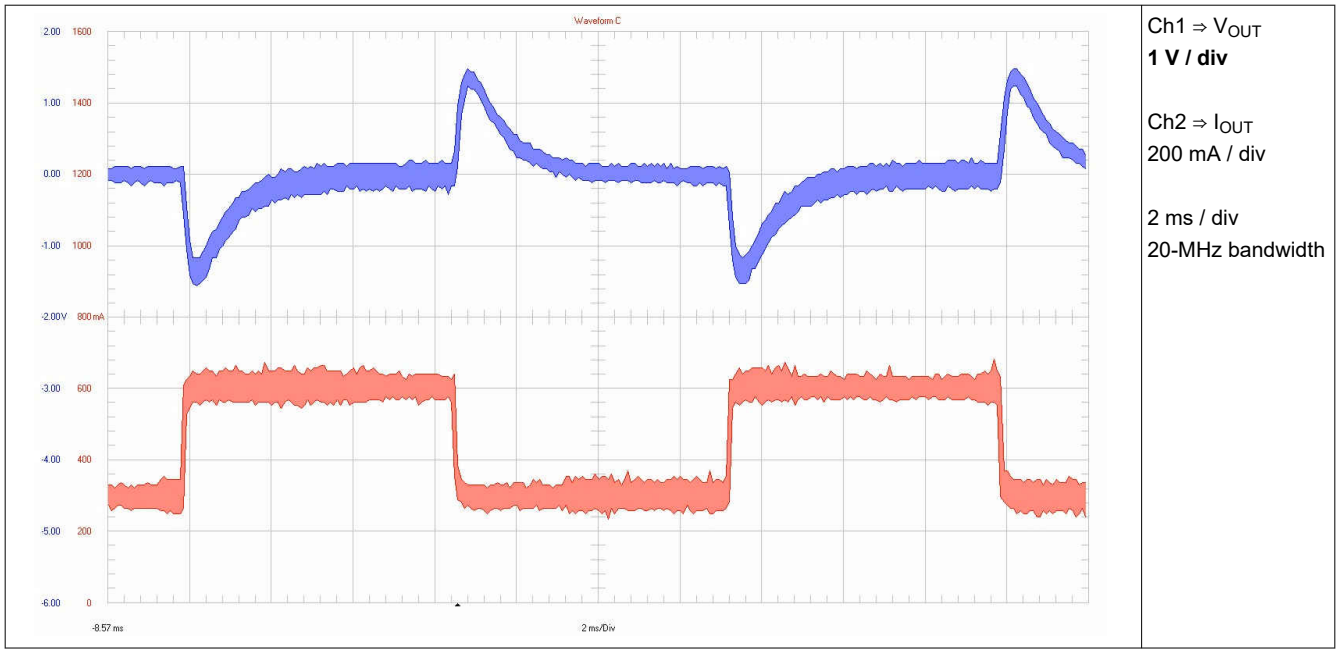
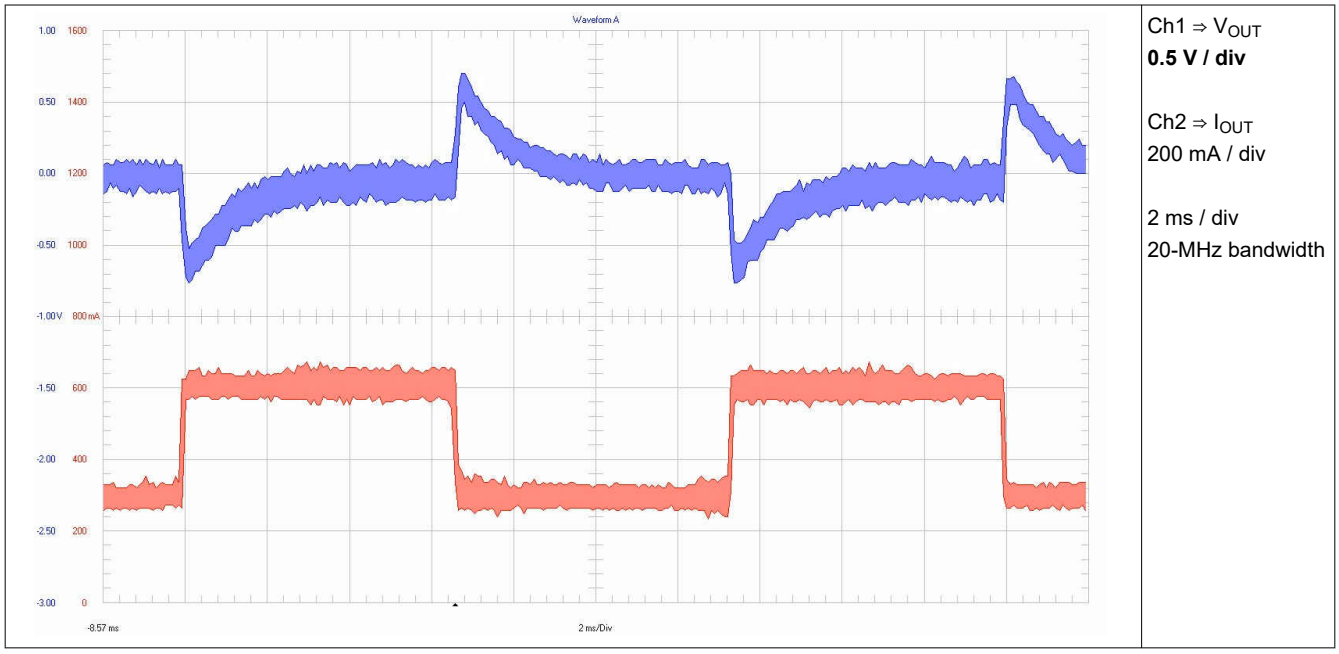


Figure 3-32. Transient at 30 V_{IN} and 48 V_{OUT}

3.4.2.2 60-V Input Voltage



Loop compensation according to Rev. B (Fco 1.2 kHz) shows transient response differential voltage (dv) < 3% for load transient 50%

Figure 3-33. Transient at 60 V_{IN} and 48 V_{OUT}

3.5 Start-Up Sequence

3.5.1 24-V Output Voltage

3.5.1.1 30-V Input Voltage

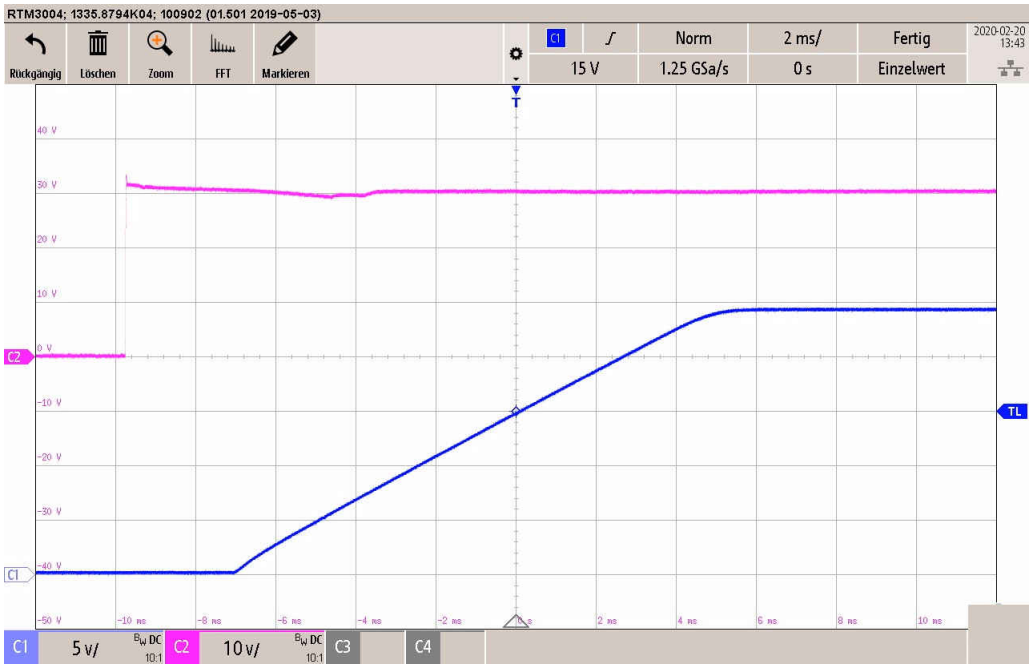


Figure 3-34. Start-up at 30 V_{IN} and 24 V_{OUT}

3.5.1.2 60-V Input Voltage

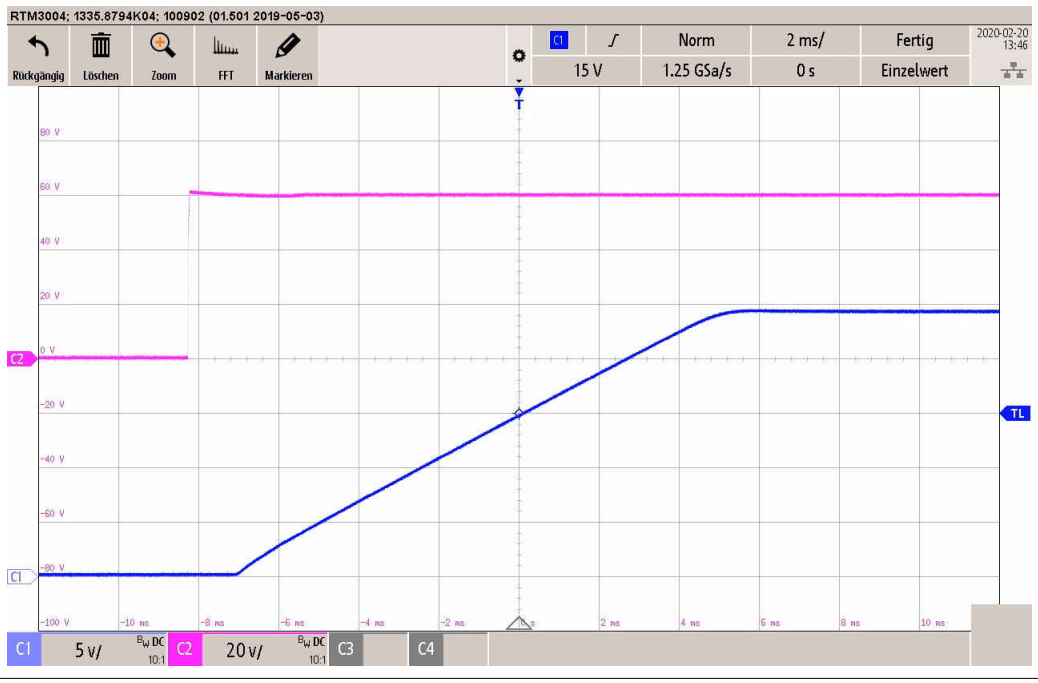
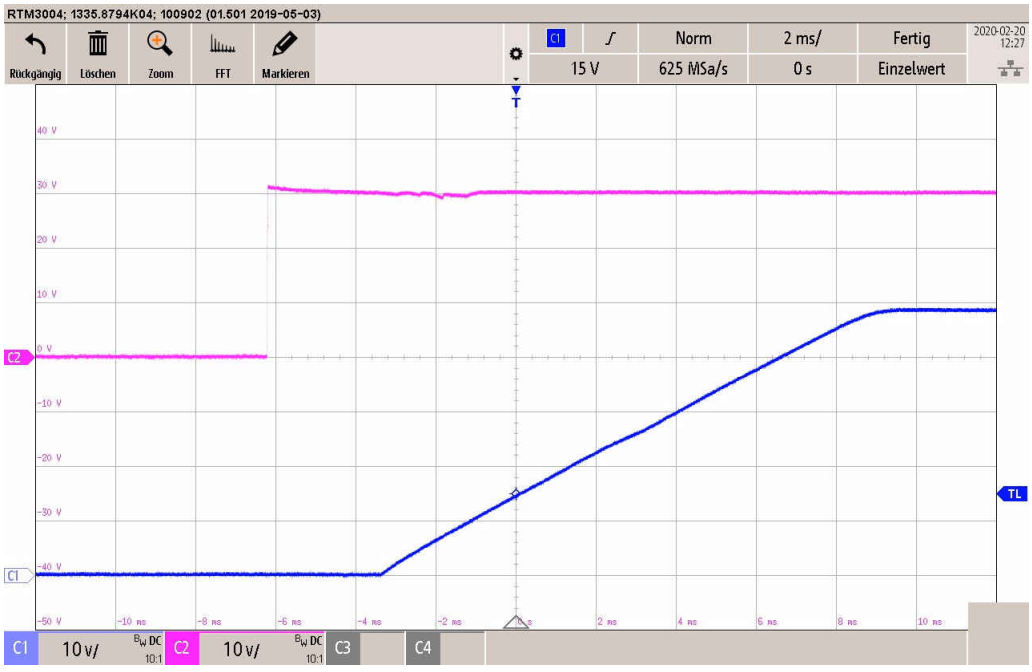


Figure 3-35. Start-up at 60 V_{IN} and 24 V_{OUT}

3.5.2 48-V Output Voltage

3.5.2.1 30-V Input Voltage



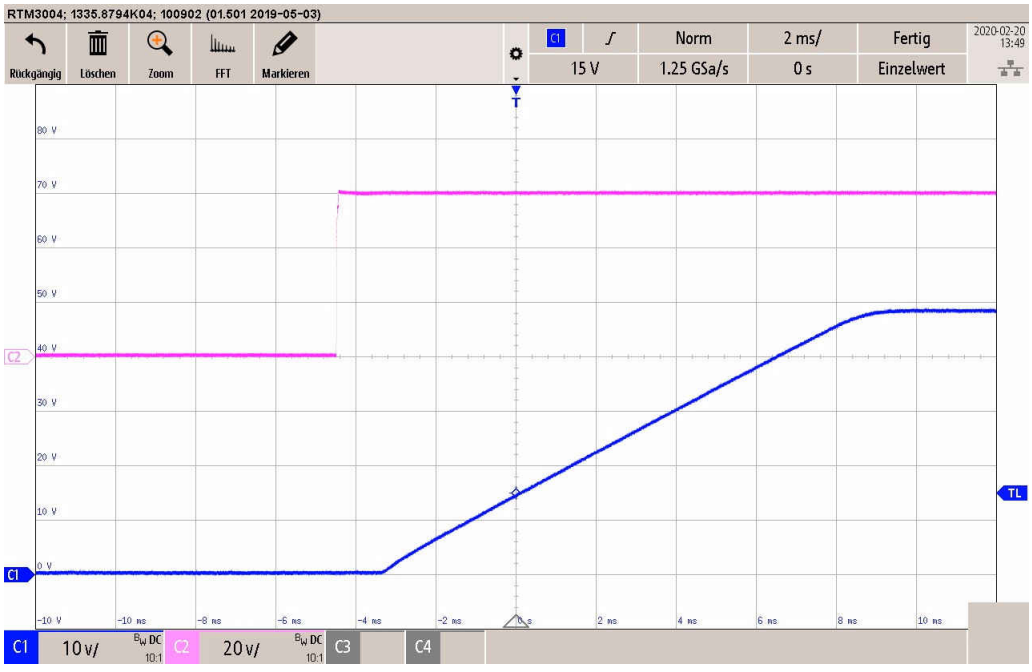
C2 ⇒ V_{IN}
10 V / div

C1 ⇒ V_{OUT}
10 V / div

2 ms / div
20-MHz bandwidth

Figure 3-36. Start-up at 30 V_{IN} and 48 V_{OUT}

3.5.2.2 60-V Input Voltage



C2 ⇒ V_{IN}
20 V / div

C1 ⇒ V_{OUT}
10 V / div

2 ms / div
20-MHz bandwidth

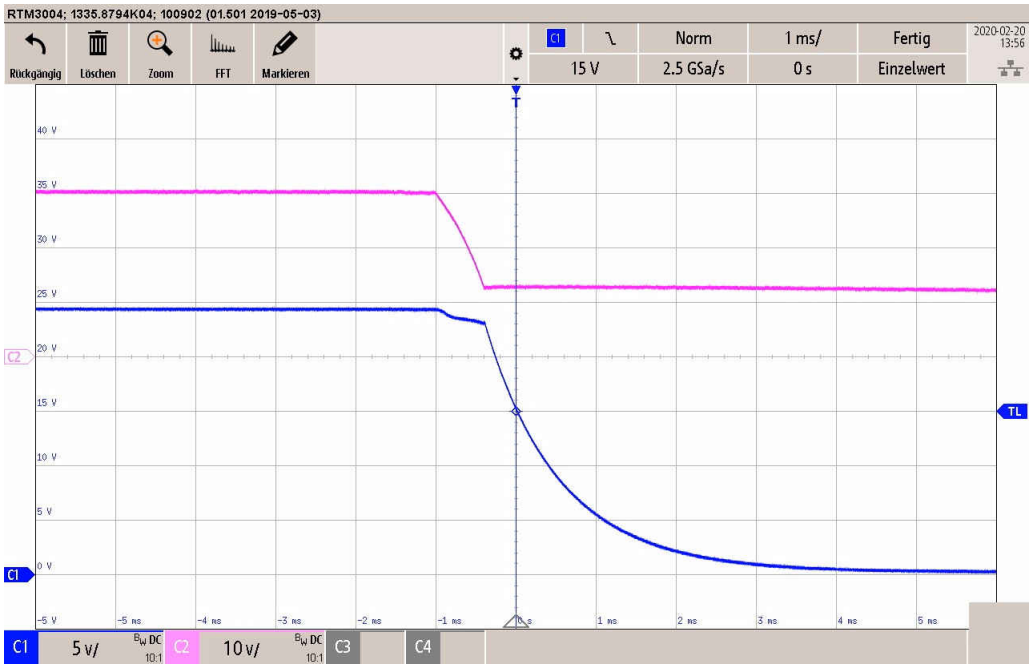
Soft-start capacitor C18, 100 nF results in soft-start time of 12 ms.

Figure 3-37. Start-up at 60 V_{IN} and 48 V_{OUT}

3.6 Shutdown Sequence

3.6.1 24-V Output Voltage

3.6.1.1 30-V Input Voltage



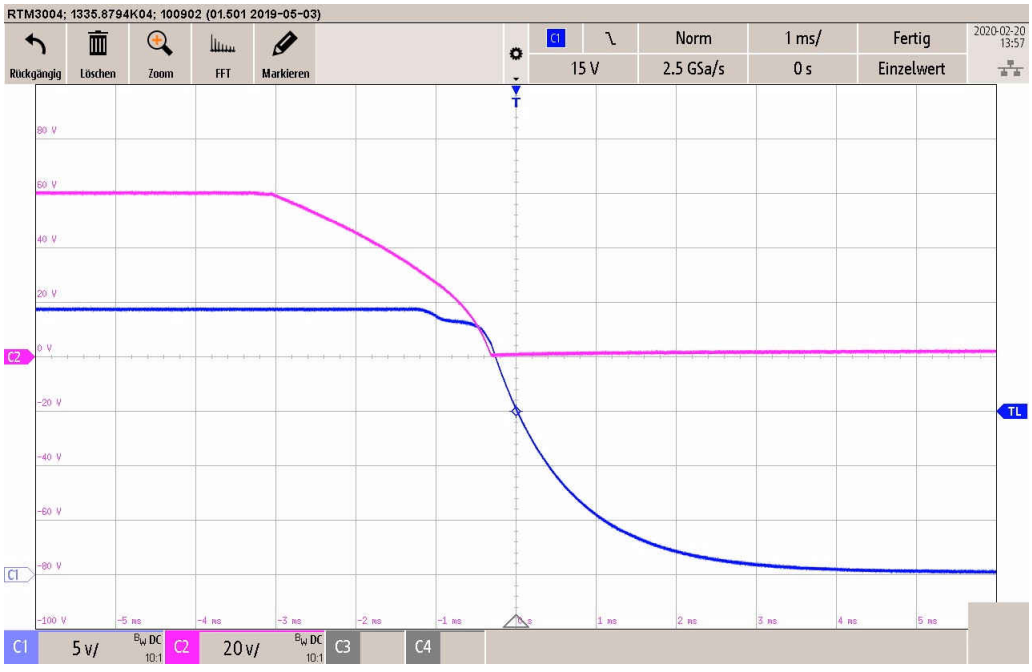
C2 ⇒ V_{IN}
10 V / div

C1 ⇒ V_{OUT}
5 V / div

1 ms / div
20-MHz bandwidth

Figure 3-38. Shutdown at 30 V_{IN} and 24 V_{OUT}

3.6.1.2 60-V Input Voltage



C2 ⇒ V_{IN}
20 V / div

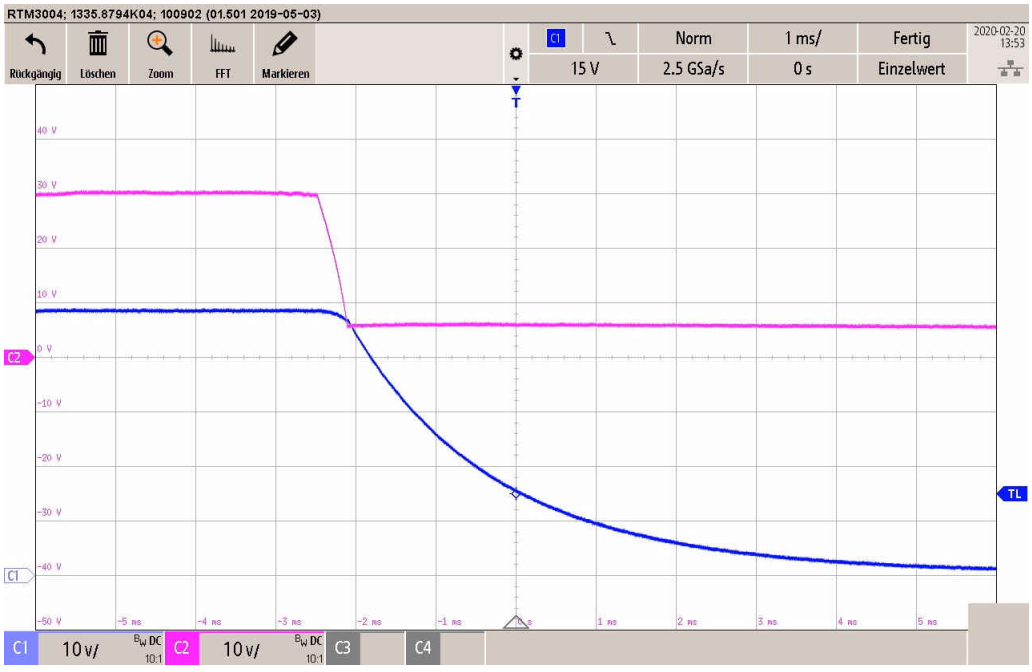
C1 ⇒ V_{OUT}
5 V / div

1 ms / div
20-MHz bandwidth

Figure 3-39. Shutdown at 60 V_{IN} and 24 V_{OUT}

3.6.2 48-V Output Voltage

3.6.2.1 30-V Input Voltage



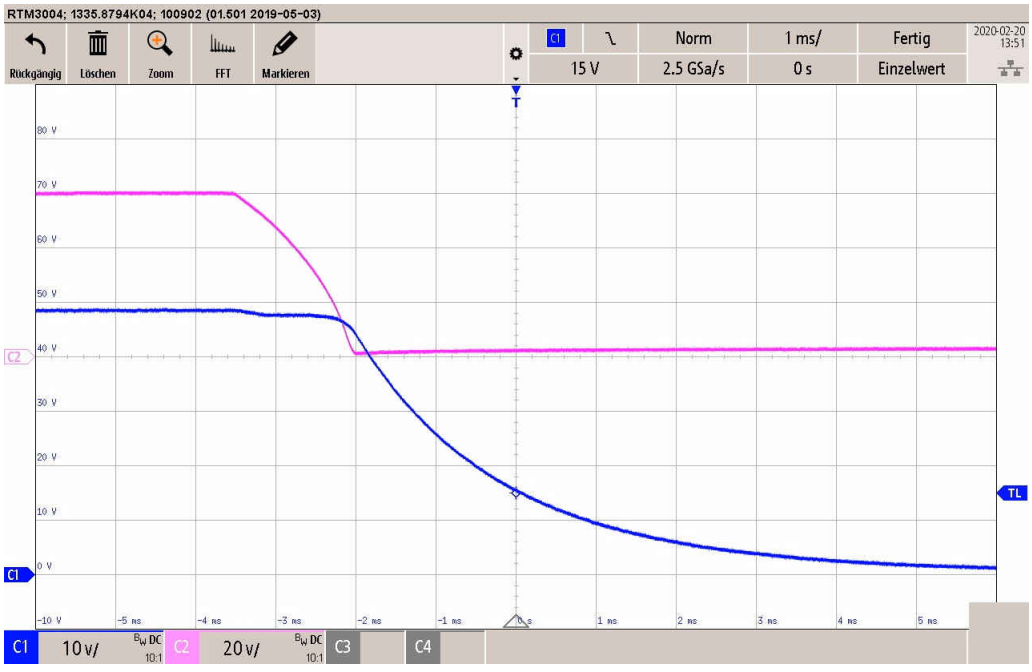
C2 ⇒ V_{IN}
10 V / div

C1 ⇒ V_{OUT}
10 V / div

1 ms / div
20-MHz bandwidth

Figure 3-40. Shutdown at 30 V_{IN} and 48 V_{OUT}

3.6.2.2 60-V Input Voltage



C2 ⇒ V_{IN}
20 V / div

C1 ⇒ V_{OUT}
10 V / div

1 ms / div
20-MHz bandwidth

Figure 3-41. Shutdown at 60 V_{IN} and 48 V_{OUT}

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