Test Report: PMP30921

4-W Discontinuous Conduction Mode Primary Side Regulated Flyback Reference Design

Description

This tiny 4-W flyback converter with additional three isolated output windings generates four outputs in total. With a windings ratio of 1:1 in between the primary and auxiliary winding, the conventional RCD snubber could be replaced by an AC flying capacitor providing better efficiency and lower EMI, but this requires the lowest leakage inductance.

The input is in the automotive range of 7 V up to 42-V surge, three outputs are post-regulated by LDO to improve line and load regulation and power supply ripple rejection (PSRR).

A differential input filter has been added to attenuate conducted emissions, and a Schottky rectifier acts as reverse-polarity protection.

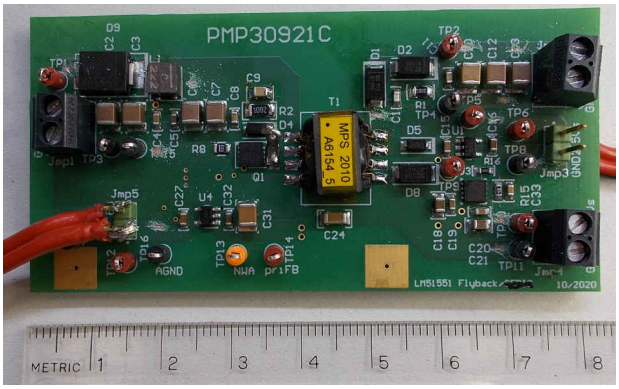
As for all multi-output primary-side regulated approaches using general purpose controllers *no load* at the auxiliary windings is a limitation for cross regulation.

Features

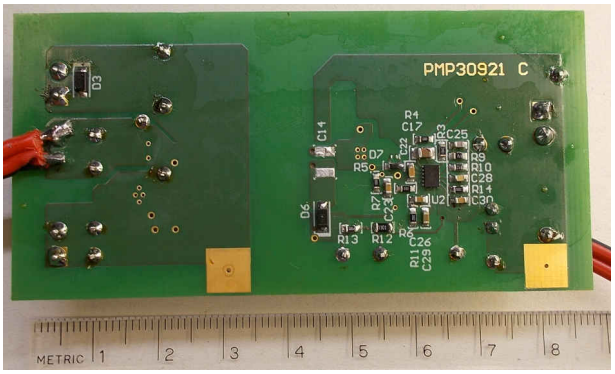
- Three isolated outputs ⇒ 12 V, 5 V, and 3.3 V and one single non-isolated output ⇒ 5 V
- Both 5-V outputs and the 3.3-V output are post-regulated for the lowest possible noise
- Differential input filter to prevent from reflected ripple
- Temperature rise less than +35 K at full load
- A table for all sixteen load combinations with light load and full load is provided

Applications

- Automotive HVAC compressor module



Board Photo (Top)



Board Photo (Bottom)

1 Test Prerequisites

1.1 Voltage and Current Requirements

Table 1-1. Voltage and Current Requirements

Parameter	Specifications
Input Voltage Range	7 V to 27 V, 42-V surge
Output Primary Side	5 V at 0.05 A_{max}
Output 1 Secondary Side	12 V_{nom}, 11 V to 14 V at 0.17 A_{max}
Output 2 Secondary Side	5 V at 0.05 A_{max}
Output 3 Secondary Side	3.3 V at 0.3 A_{max}
Switching Frequency	250 kHz

1.2 Considerations

Resistors were used as load.

Unless otherwise mentioned, the input voltage was adjusted to 12 V and the output current was determined by resistors. The resistor values were calculated for nominal output voltage for reaching the maximum output current for each single output.

1.3 Dimensions

The size of the board is 80 mm × 39.4 mm. The two-layer board was manufactured with 35-µm copper thickness on each layer.

2 Testing and Results

2.1 Efficiency Graphs

Efficiency is shown in Figure 2-1.

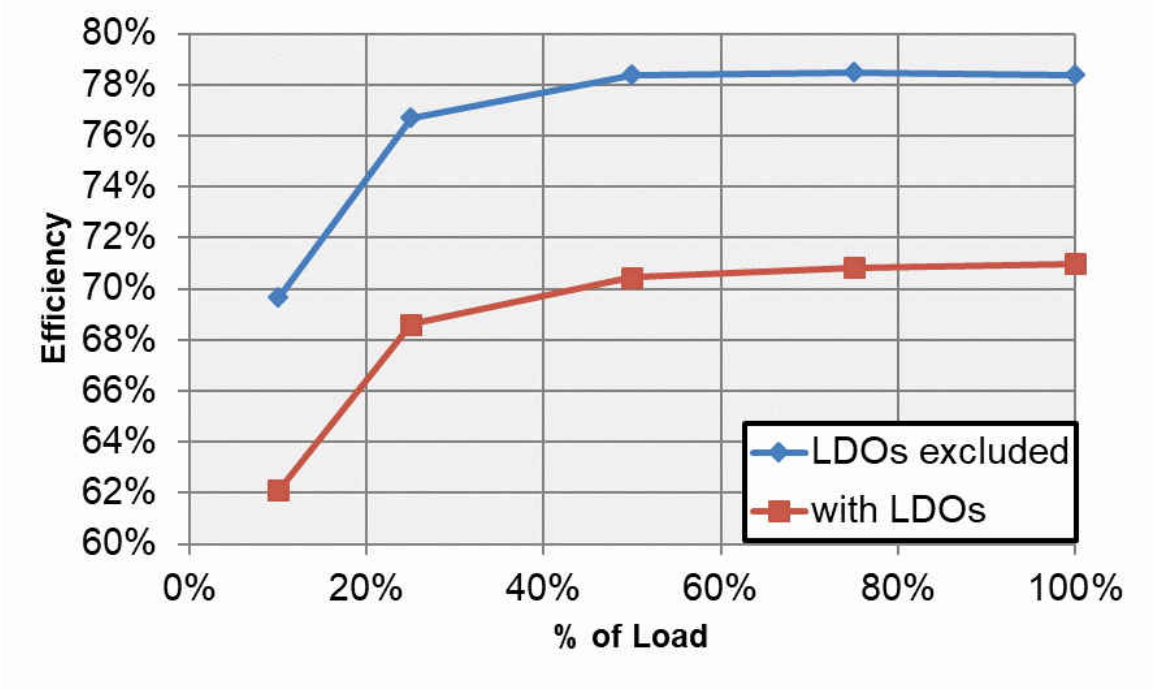


Figure 2-1. Efficiency vs Percentage of Load

2.2 Loss

Figure 2-2 shows the loss versus percentage of load graph.

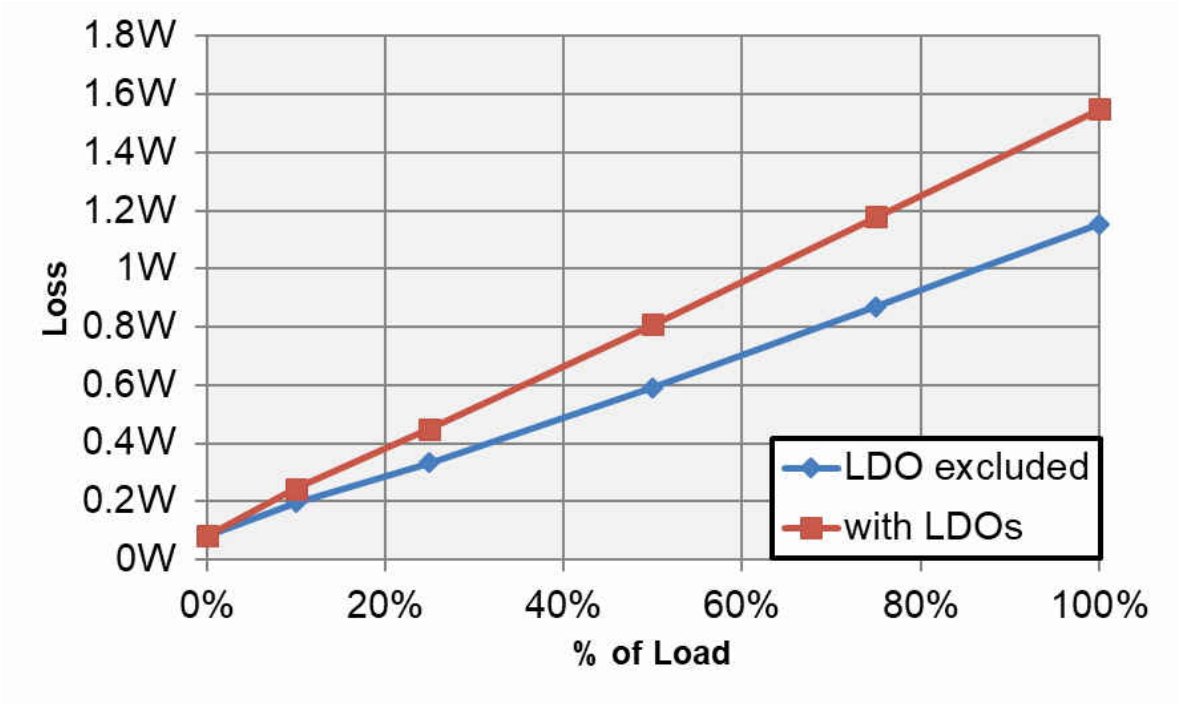


Figure 2-2. Loss vs Percentage of Load

2.3 Load Regulation

All of the outputs in Figure 2-3 through Figure 2-7 are measured at the same percentage loading.

2.3.1 5-V Output Voltage

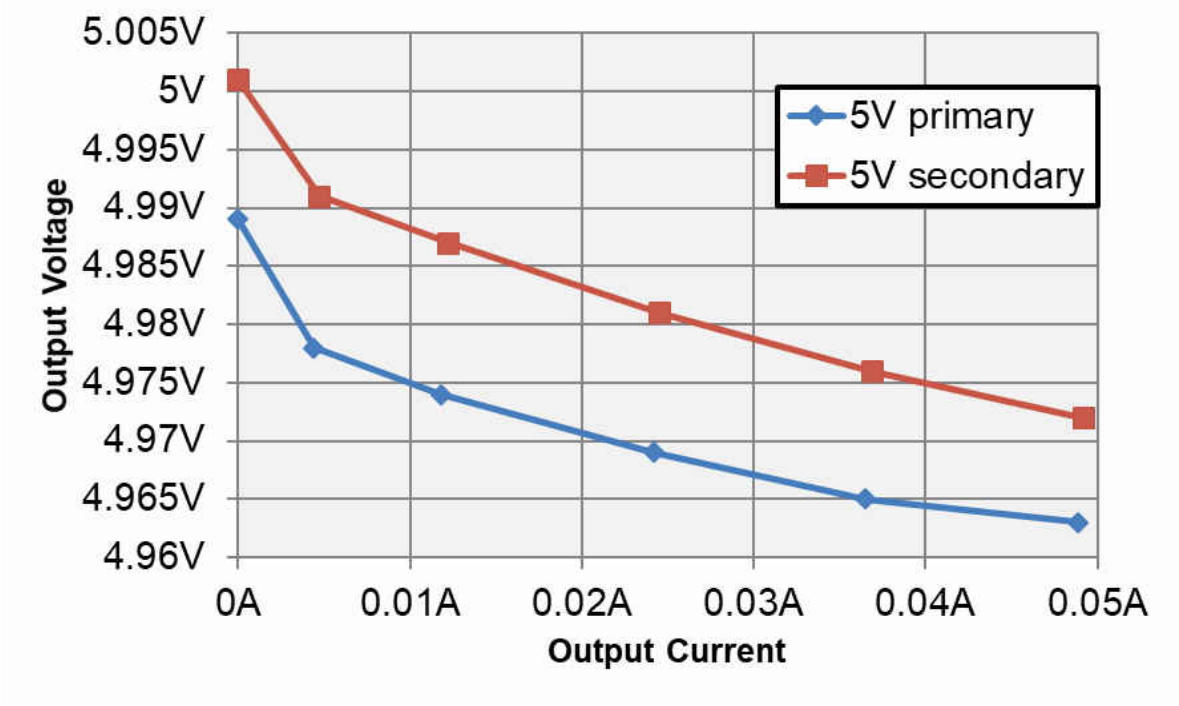


Figure 2-3. 5-V Output Voltages vs Output Current at LDO Output

Note

Figure 2-4 illustrates *LDO inputs* at 5 V.

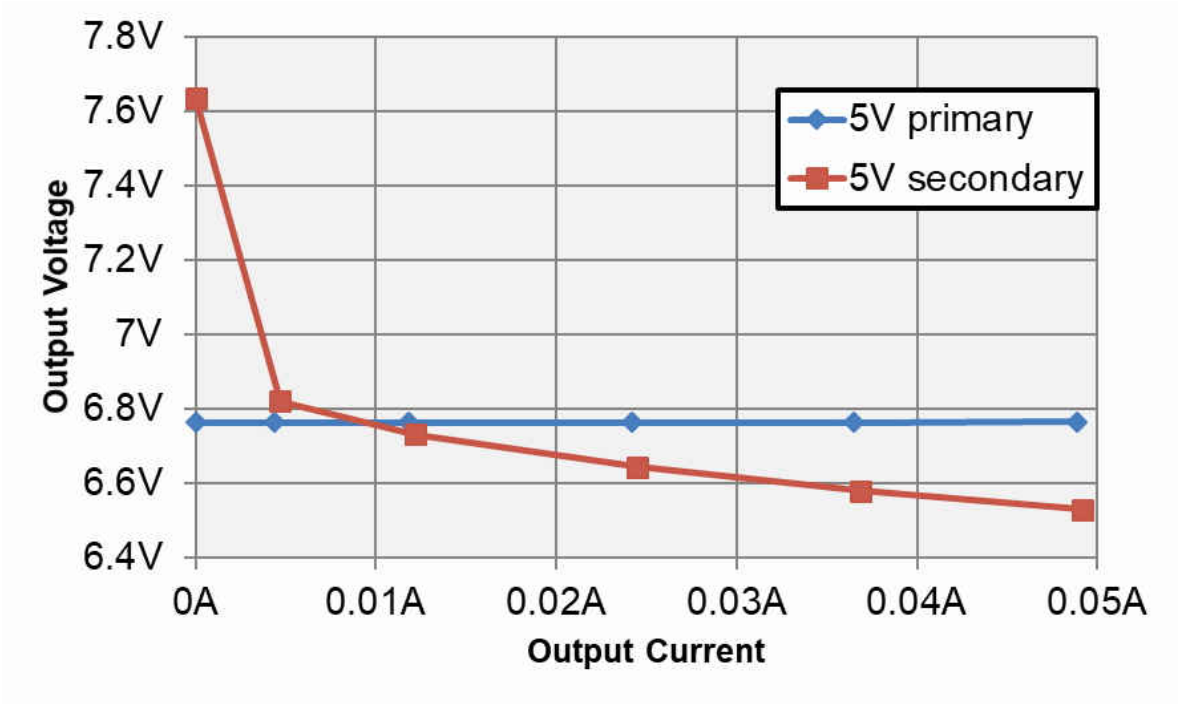


Figure 2-4. Voltages at 5-V LDO Inputs vs Output Current

2.3.2 3.3-V Output Voltage

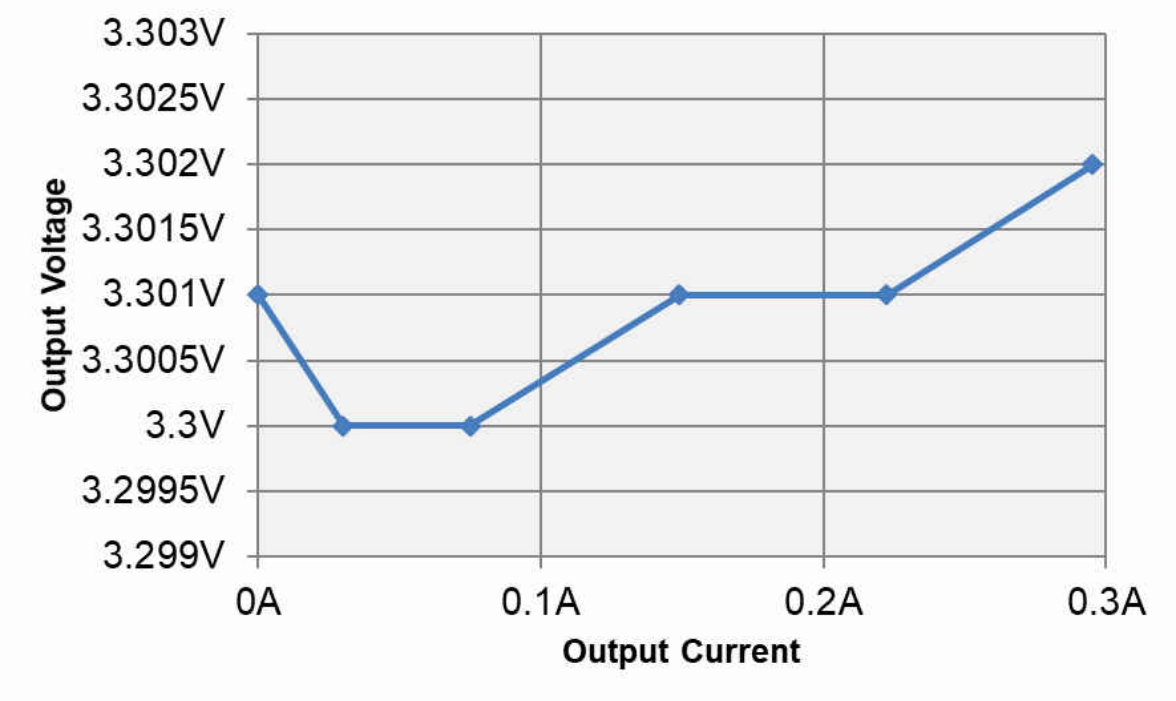


Figure 2-5. Output Voltage vs Output Current

Note

Figure 2-6 illustrates *LDO inputs* at 3.3 V.

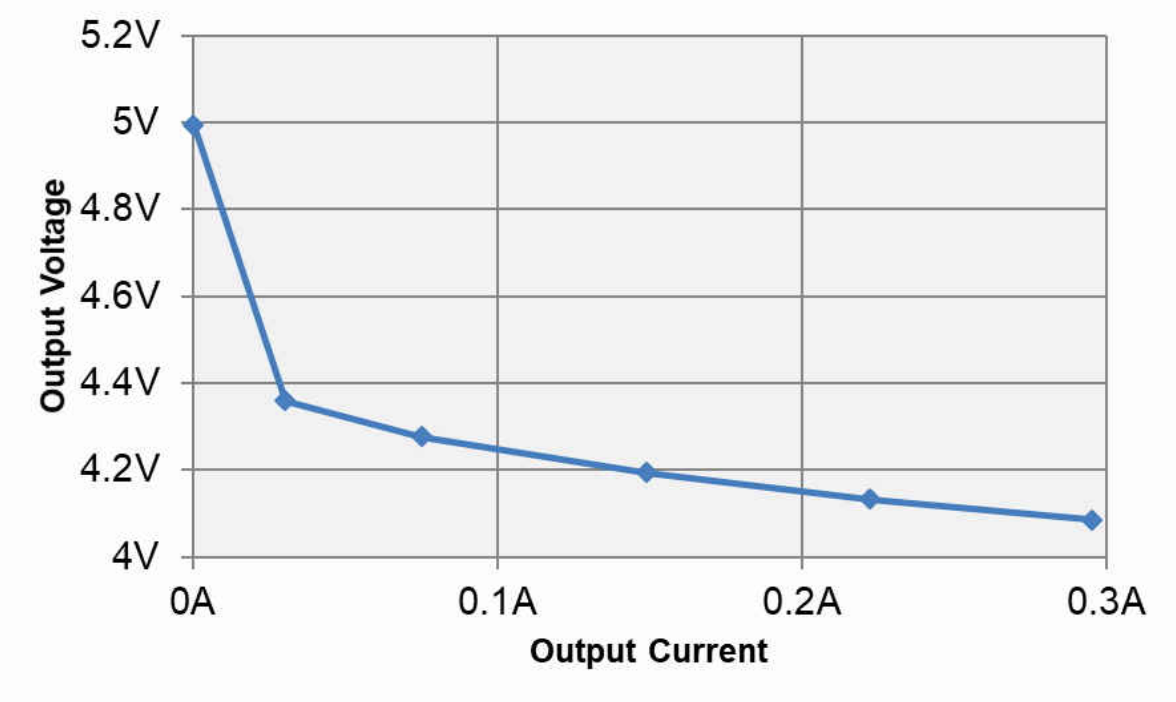
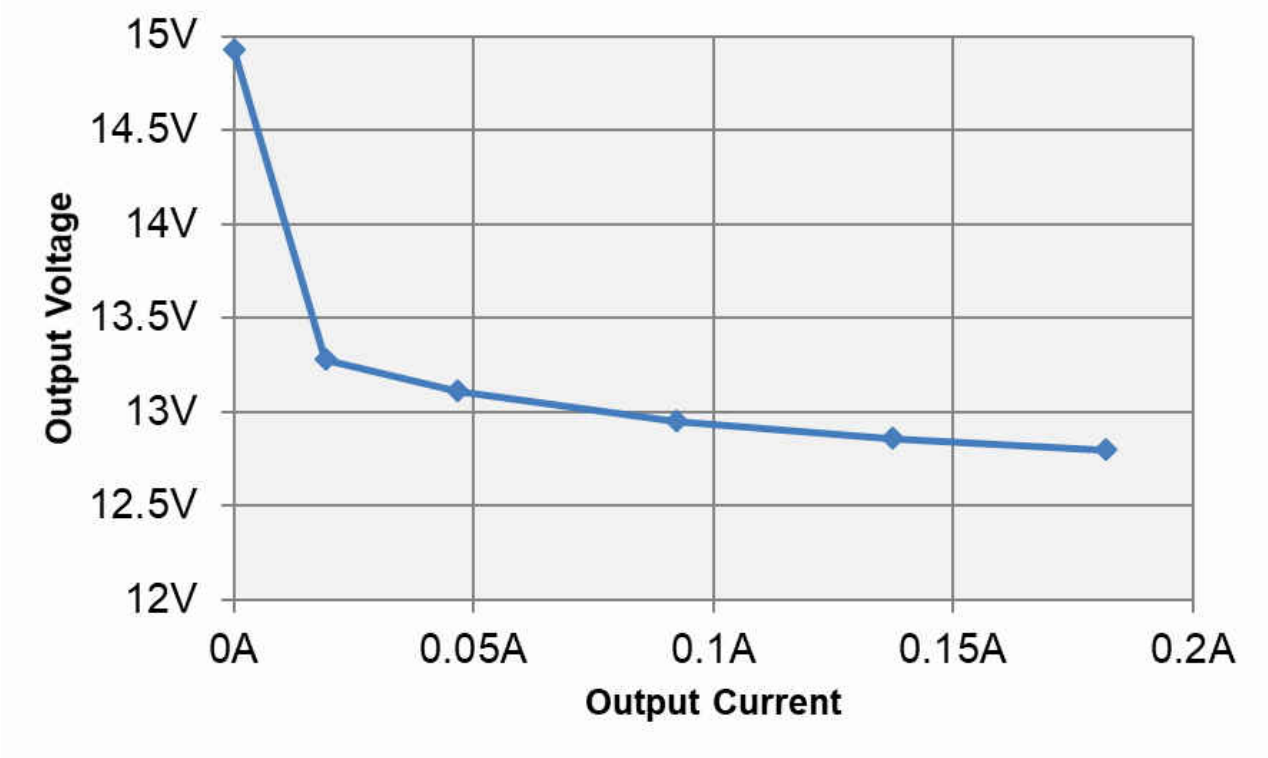


Figure 2-6. Voltage at 3.3-V LDO Input vs Output Current

2.3.3 12-V Output Voltage



Due to peak detection at ***zero*** load, this output needs to be clamped by Zener diode or minimum load.

Figure 2-7. 12-V Output Voltage vs Output Current

2.4 Line Regulation

The input voltage was varied from 7 V to 27 V.

2.4.1 5-V Outputs

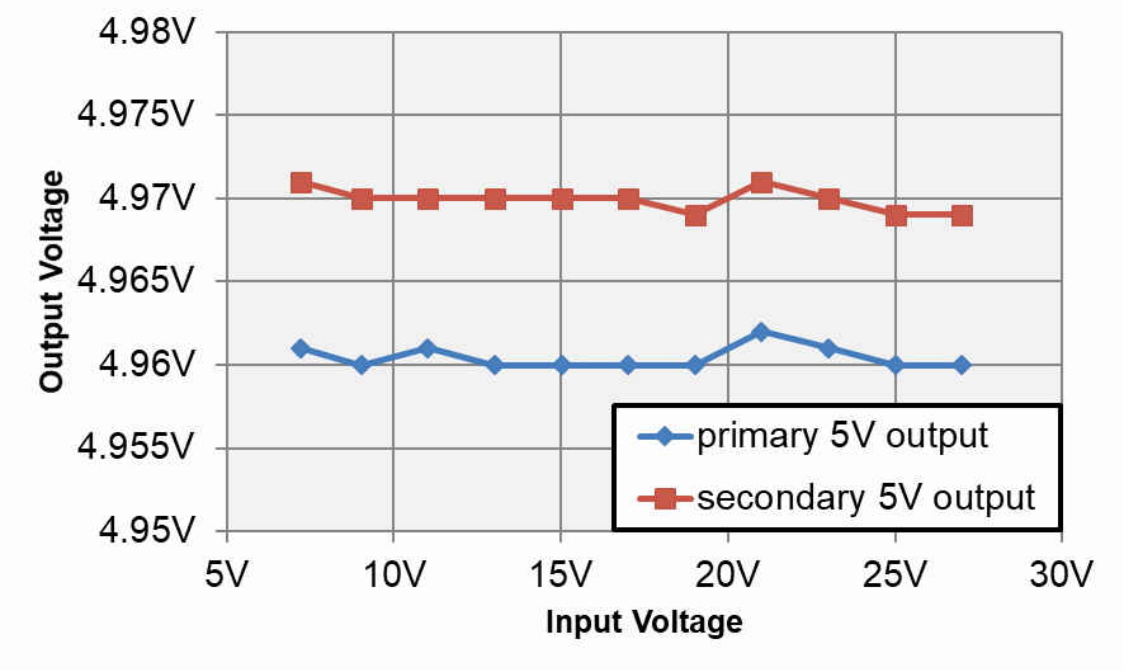


Figure 2-8. 5-V Output Voltages vs Input Voltage

Figure 2-9 shows voltages measured before the corresponding LDOs.

Note

Figure 2-9 illustrates *LDO inputs* at 5 V.

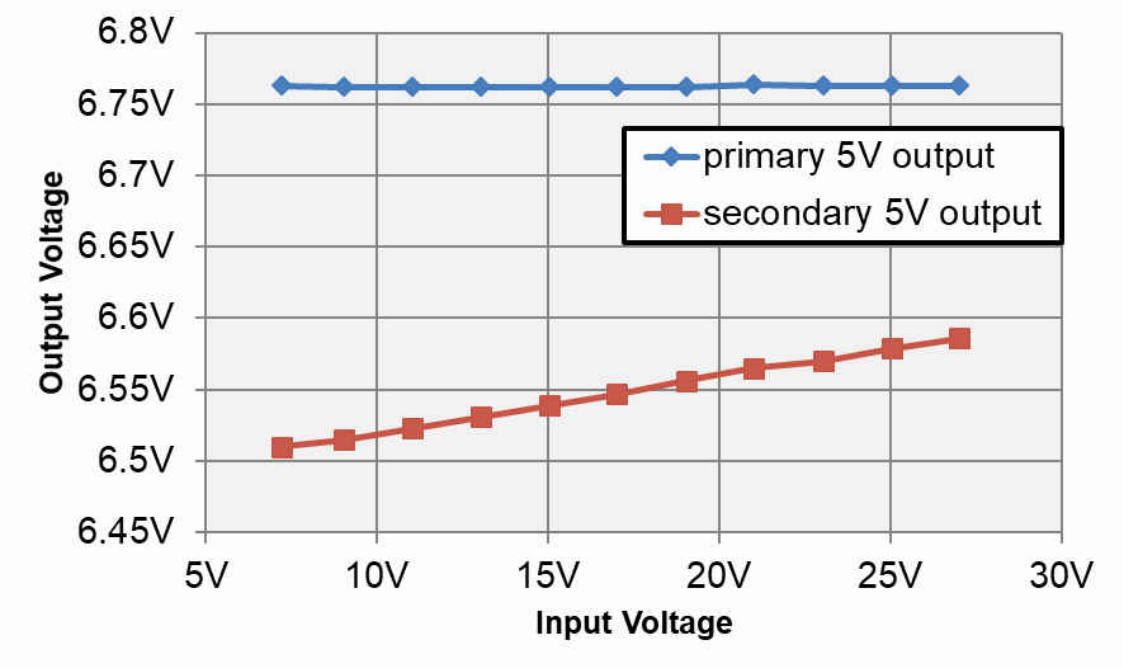


Figure 2-9. 5-V LDOs Input Voltages vs Input Voltage

2.4.2 3.3-V Output Voltage

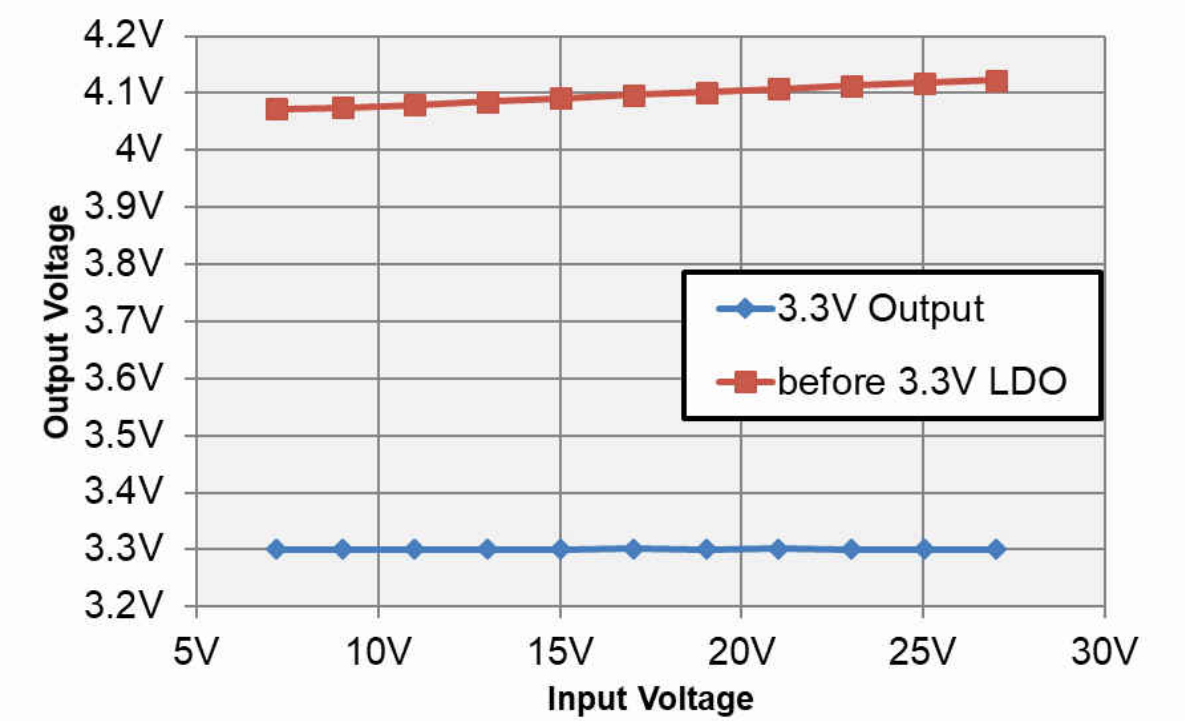
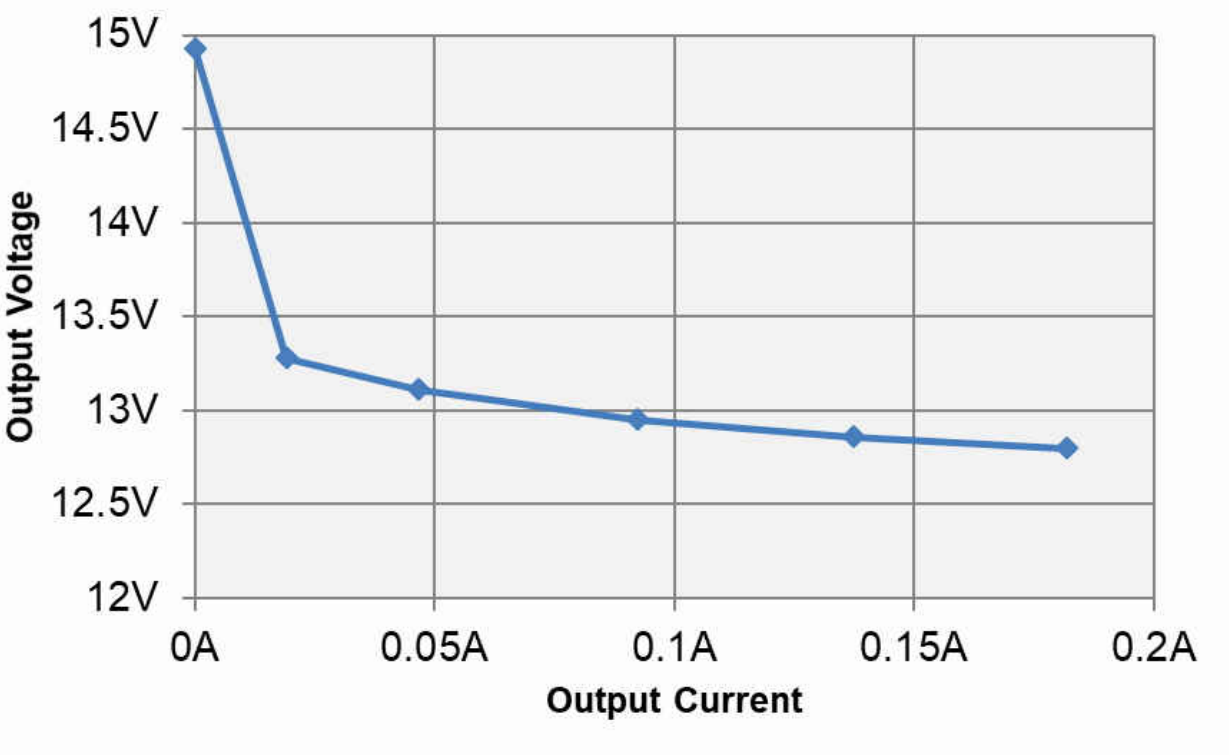


Figure 2-10. 3.3-V Output Voltage vs Input Voltage

2.4.3 12-V Output Voltage



Due to peak detection at ***zero*** load, this output needs to be clamped by Zener diode or minimum load.

Figure 2-11. 12-V Output Voltage vs Output Current

2.4.4 Efficiency and Loss in Dependance of Input Voltage

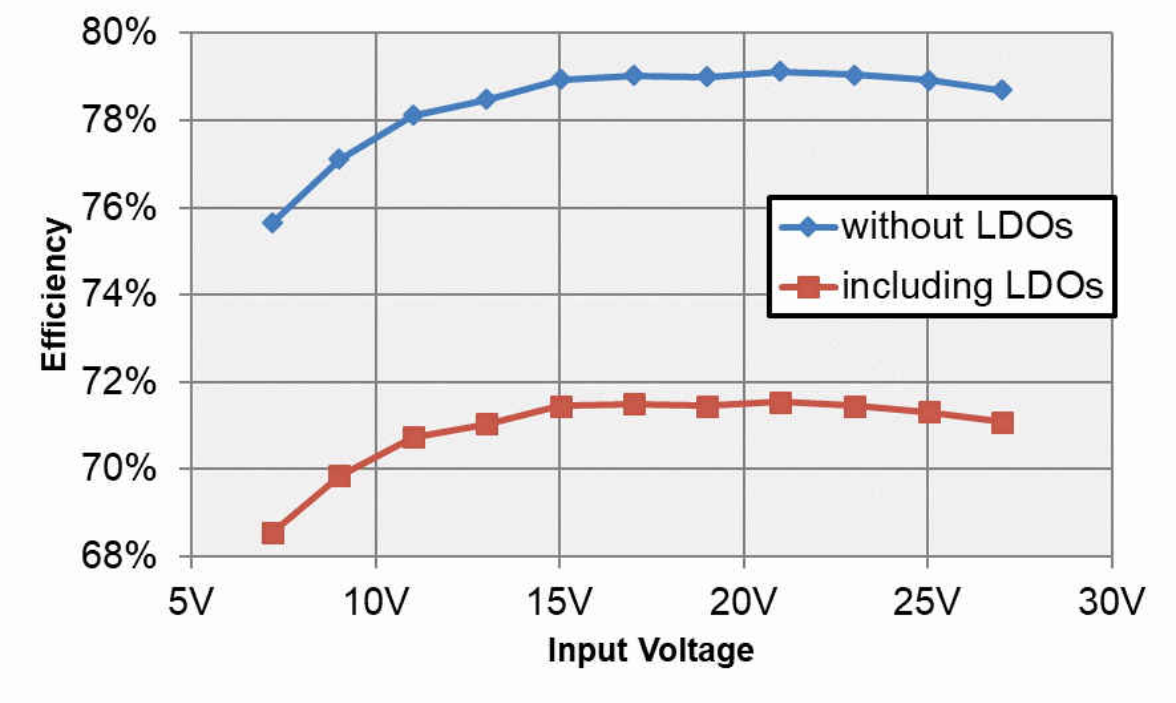


Figure 2-12. Efficiency vs Input Voltage

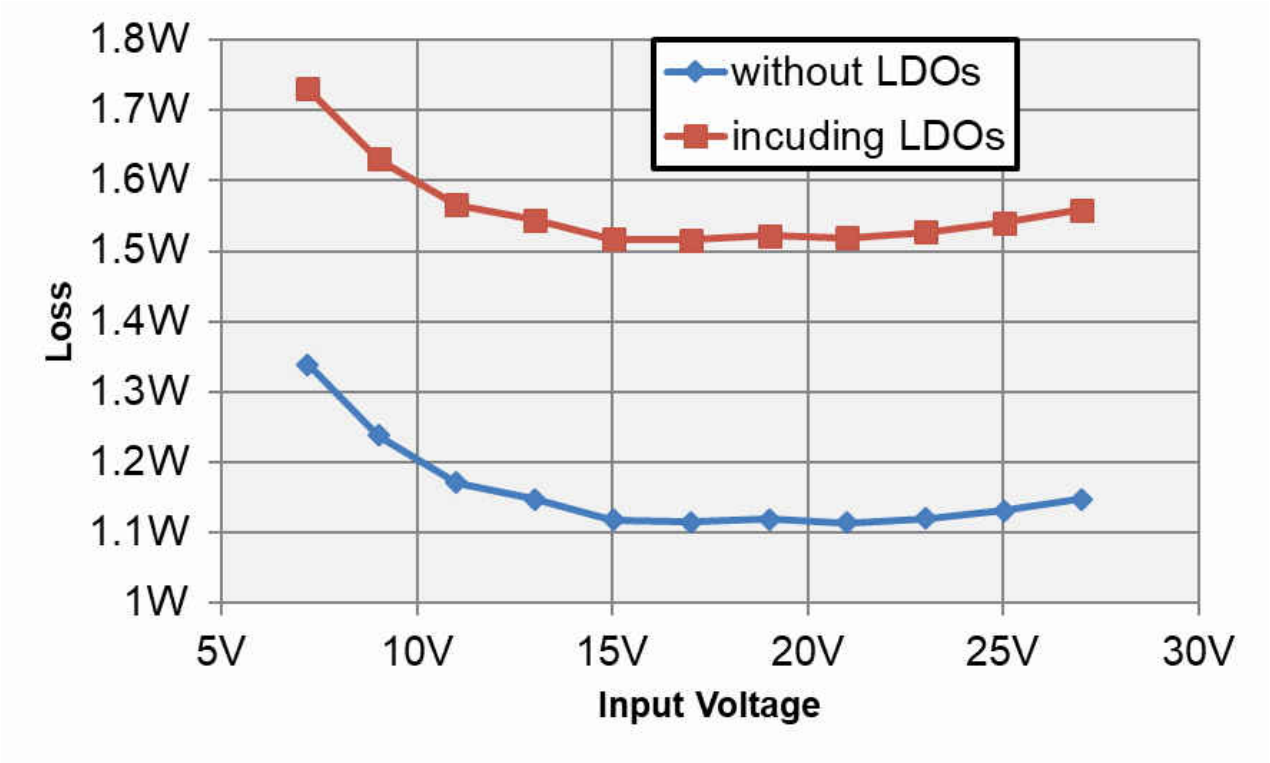


Figure 2-13. Loss vs Input Voltage

2.5 Cross Regulation Light Load and Full Load

2.5.1 Bias Current 1 mA

Table 2-1. Cross Regulation With Bias Current set to 1 mA

primary			secondary							
5 V	LDO in	LDO out	3.3 V	LDO out	LDO in	5 V	LDO out	LDO in	12 V	out
0	6.142	4.98	0	3.3	3.899	0	4.995	6.134	0	11.93
0	6.141	4.979	0	3.3	3.59	0	4.994	5.645	1	10.581
0	6.14	4.979	0	3.3	3.84	1	4.98	5.736	0	11.79
0	6.14	4.979	0	3.3	3.511	1	4.98	5.313	1	10.369
0	6.14	4.979	1	3.123	3.187	0	4.994	5.659	0	11.248
0	6.139	4.978	1	2.995	3.056	0	4.994	5.18	1	9.752
0	6.139	4.978	1	3.11	3.173	1	4.978	5.245	0	11.043
0	6.138	4.978	1	2.939	3	1	4.822	4.887	1	9.563
1	6.14	4.964	0	3.301	**4.168**	0	4.994	**6.532**	0	12.7
1	6.139	4.963	0	3.3	4.015	0	4.992	6.28	1	11.8
1	6.138	4.963	0	3.3	4.116	1	5.023	6.165	0	12.57
1	6.138	4.962	0	3.3	3.995	1	5.019	6.044	1	11.75
1	6.137	4.962	1	3.3	3.653	0	4.991	6.283	0	12.38
1	6.137	4.962	1	3.299	3.689	0	4.99	6.149	1	11.62
1	6.136	4.961	1	3.299	3.653	1	4.974	5.963	0	12.3
1	6.136	4.961	1	3.299	3.678	1	4.974	5.915	1	11.58
	max. 10V				max. 6V			max. 10V		11V..14V
RevE:					out of range					
flyback configuration										
xfmr A6154Rev3										
bias current 1mA										
bias voltage 6.14V										
2x rectifier at 12Vout										

2.5.2 Bias Current 5 mA

Table 2-2. Cross Regulation With Bias Current set to 5 mA

primary			secondary							
5 V	LDO in	LDO out	3.3 V	LDO out	LDO in	5 V	LDO out	LDO in	12 V	out
0	**6.766**	4.979	0	3.301	4.36	0	4.993	6.822	0	13.29
0	6.765	4.979	0	3.3	4.102	0	4.993	6.413	1	12.06
0	6.764	4.978	0	3.3	4.308	1	4.976	6.43	0	13.16
0	6.763	4.978	0	3.3	4.041	1	4.976	6.099	1	11.89
0	6.763	4.977	1	3.299	3.67	0	4.99	6.408	0	12.7
0	6.762	4.976	1	3.3	3.586	0	4.991	6.009	1	11.35
0	6.764	4.978	1	3.3	3.669	1	4.975	6.012	0	12.55
0	6.763	4.978	1	3.3	**3.527**	1	4.976	**5.696**	1	**11.196**
1	6.762	4.96	0	3.301	**4.603**	0	4.99	**7.184**	0	**13.99**
1	6.762	4.96	0	3.3	4.429	0	4.989	6.9	1	13.01
1	6.763	4.961	0	3.301	4.547	1	4.973	6.8	0	13.85
1	6.763	4.961	0	3.301	4.41	1	4.972	6.653	1	12.98
1	6.762	4.96	1	3.3	4.067	0	4.989	6.922	0	13.65
1	6.762	4.96	1	3.301	4.095	0	4.988	6.769	1	12.84
1	6.762	4.96	1	3.301	4.064	1	5.011	6.599	0	13.57
1	6.761	4.96	1	3.301	4.083	1	5.009	6.534	1	12.8
	max. 10V				max. 6V			max. 10V		11V..14V
RevE:					out of range					
flyback configuration					worst case					
xfmr A6154Rev3										
bias current 5mA										
bias voltage 6.76V										
2x rectifier at 12Vout										

2.6 Thermal Images

The PMP30921 thermal image is shown in the following figure.

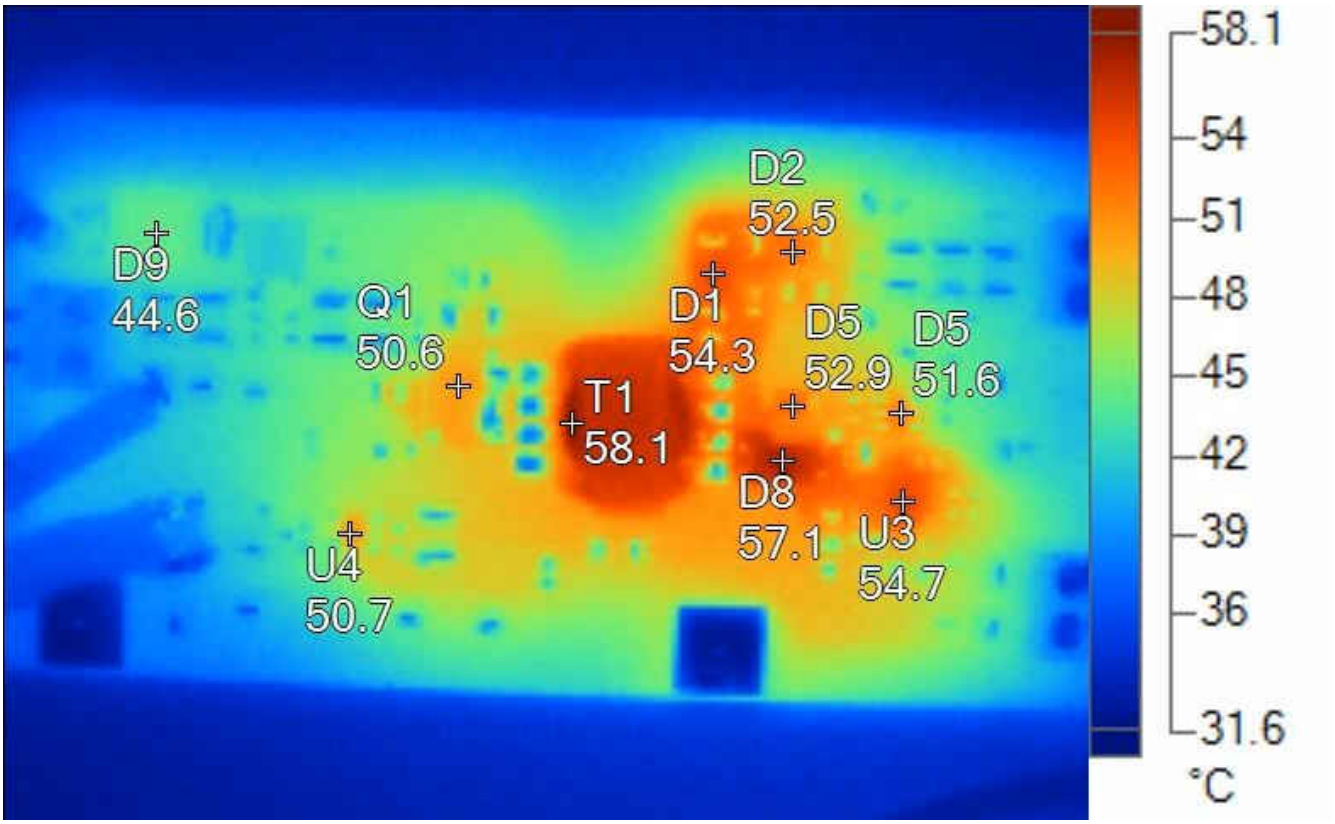


Figure 2-14. Thermal Image

Name	Temperature
D1	54.3°C
D2	52.5°C
D5	51.6°C
D5	52.9°C
D8	57.1°C
D9	44.6°C
Q1	50.6°C
T1	58.1°C
U3	54.7°C
U4	50.7°C

2.7 Bode Plots

The PMP30921 bode plot is shown in the following figure.

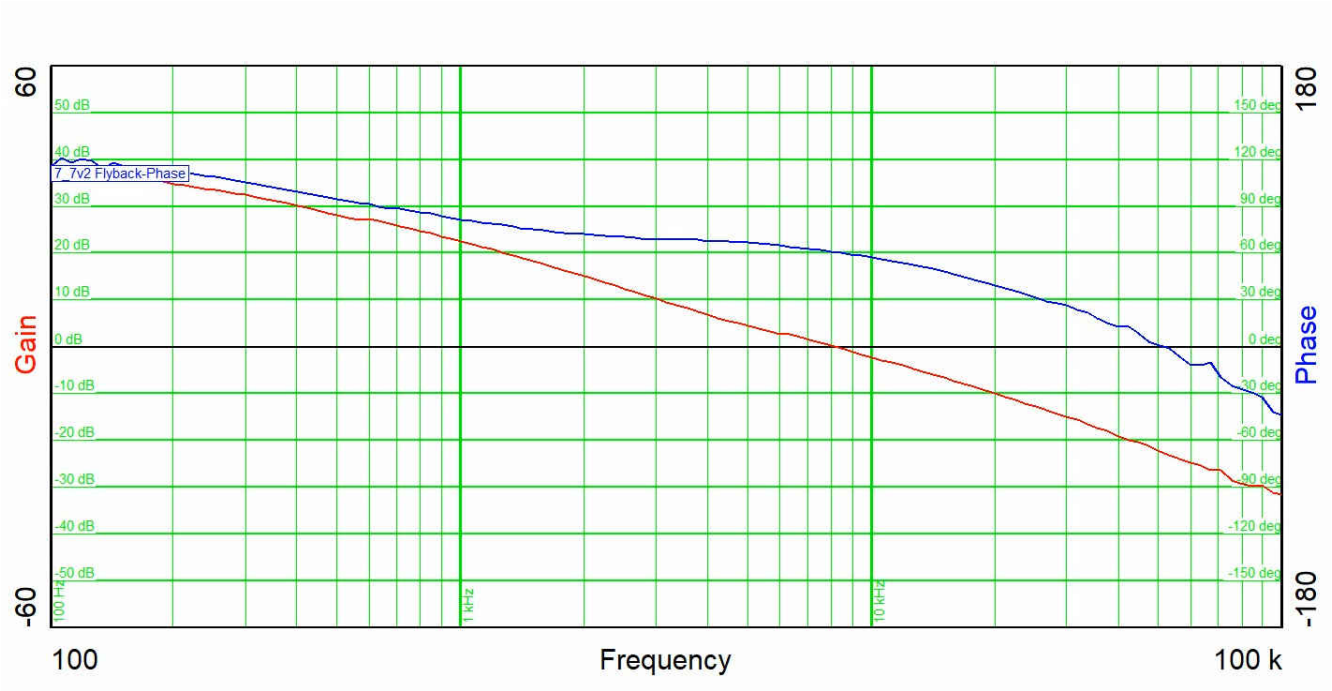


Figure 2-15. Frequency Response for 7.2-V Input Voltage

V_{IN}	7.2 V
Bandwidth (kHz)	8.16
Phase margin	61°
Slope (20 dB / decade)	–1.3
Gain margin (dB)	–22.8
Slope (20 dB / decade)	–1.9
Freq (kHz)	51.6

3 Waveforms

3.1 Switching

3.1.1 Q1 Drain to GND

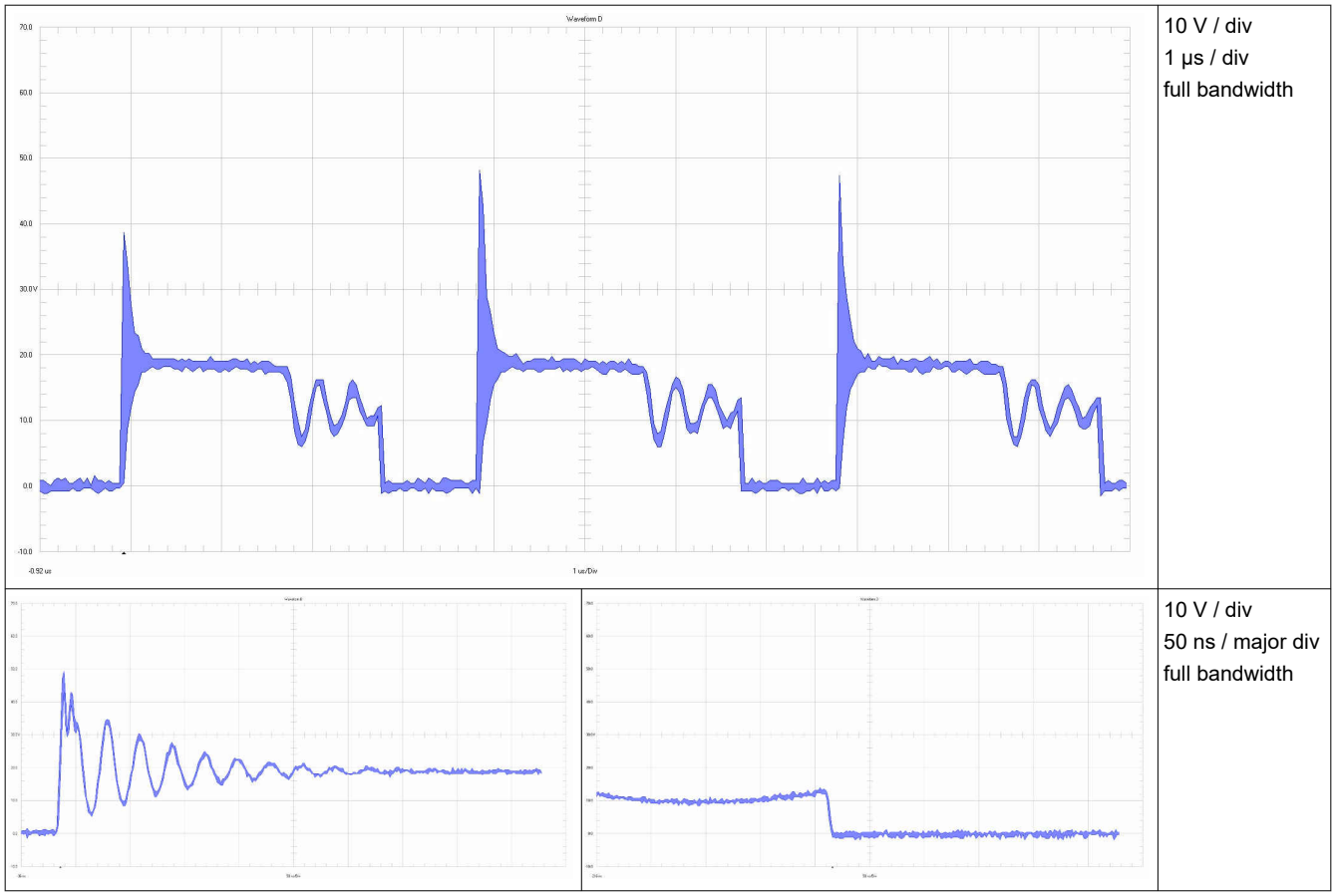


Figure 3-1. Switchnode (Q1 Drain to GND)

3.1.2 Q1 Gate to GND

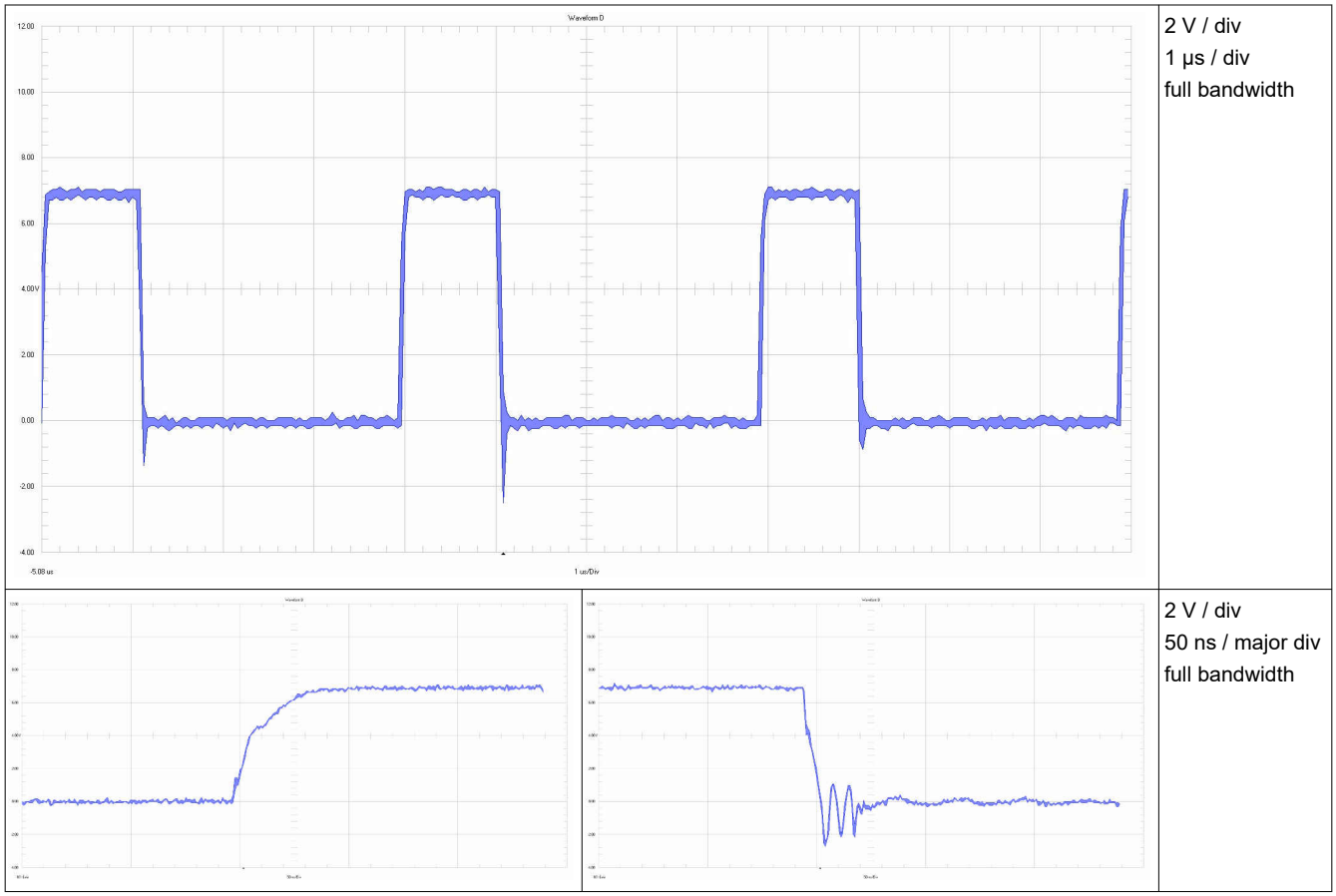


Figure 3-2. Switching (Q1 Gate to GND)

3.1.3 D1 Anode to 12 V_{OUT}

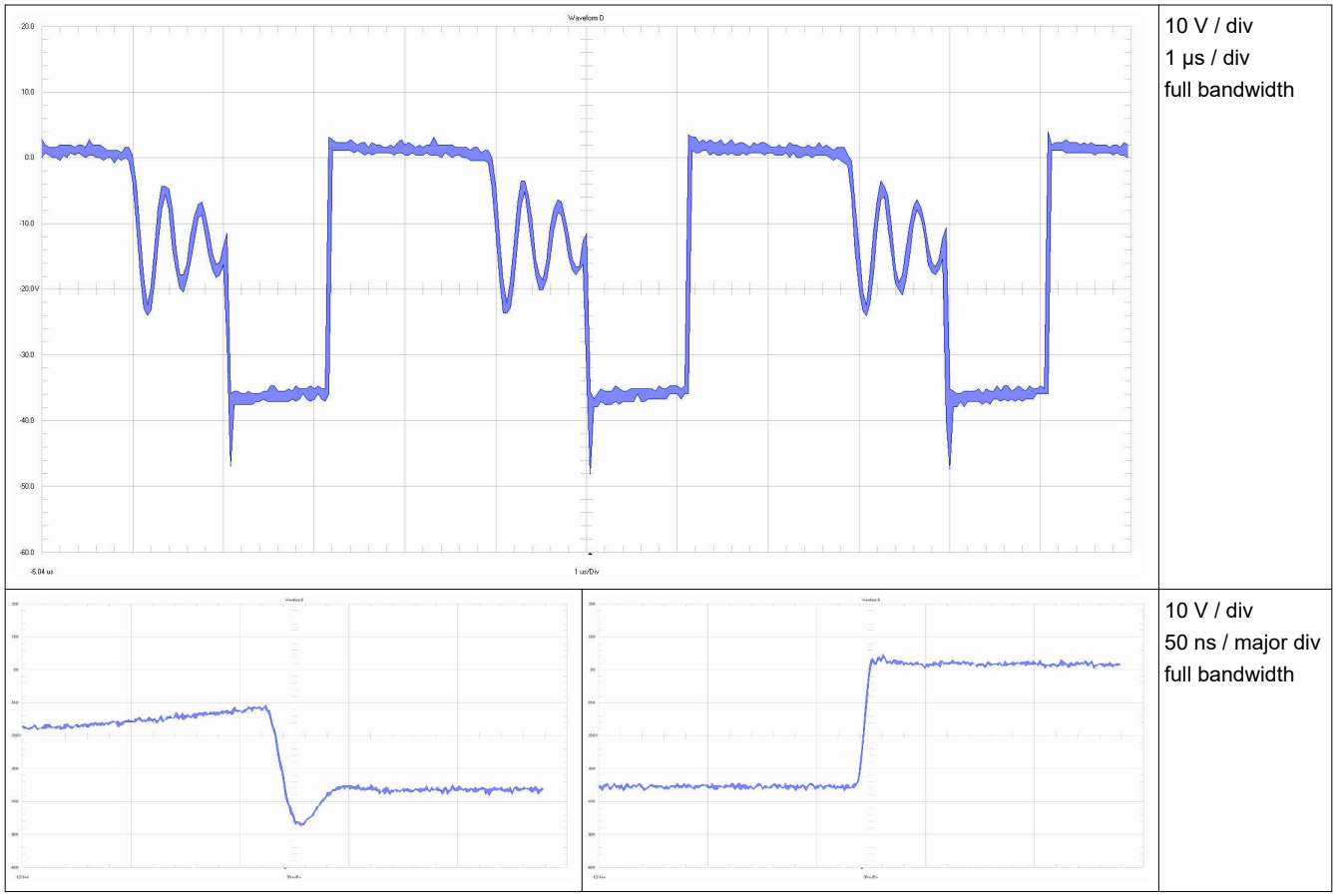


Figure 3-3. D1 (Anode to 12 V_{OUT})

3.2 Input Voltage Ripple

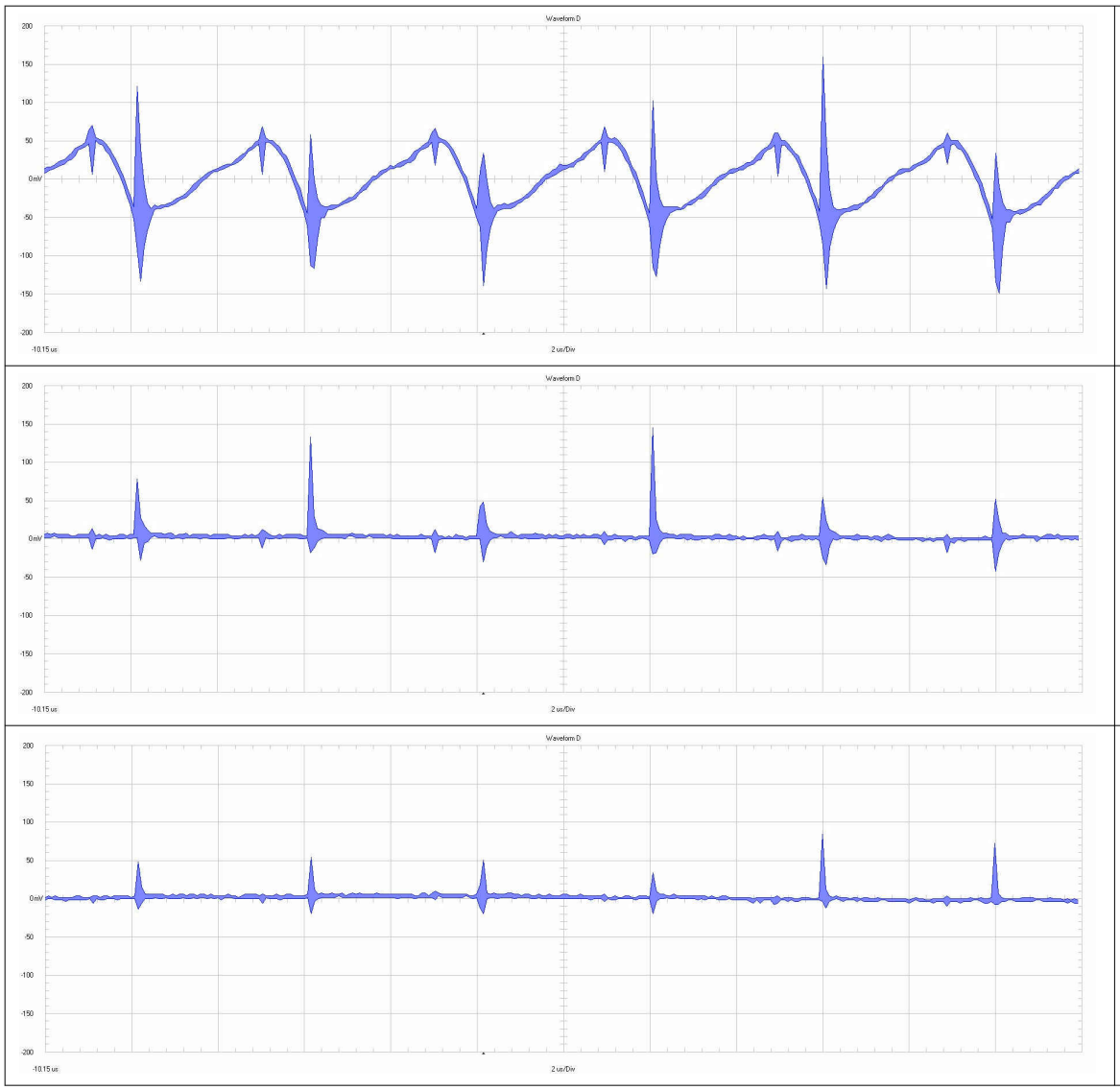


Figure 3-4. Input Voltage Ripple

The input filter is attenuating the reflected ripple (= conducted emissions).

To attenuate RF spikes further a ferrite bead (600 Ω at 100 MHz) could be added to the input.

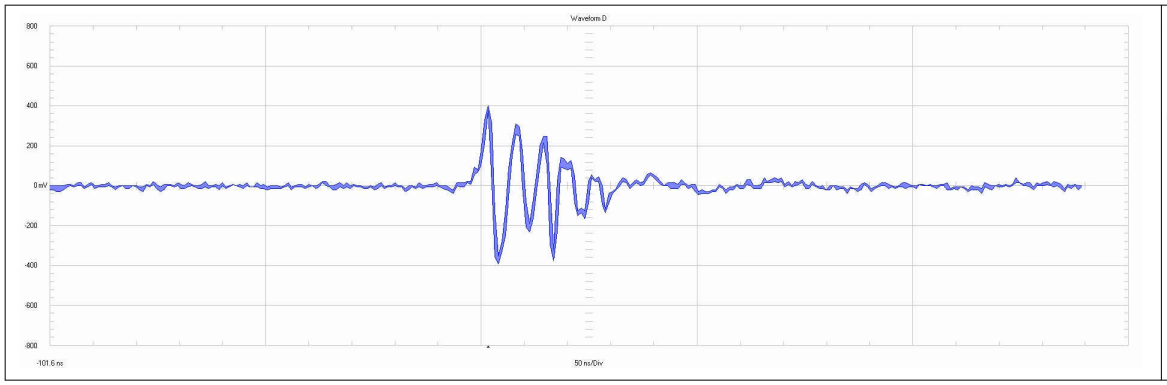
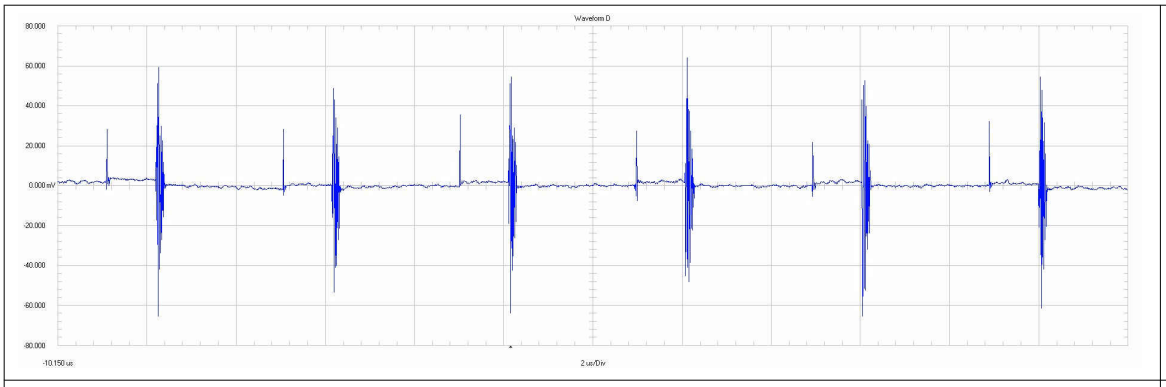


Figure 3-5. Input Ripple (Jmp1 Zoomed and Full Bandwidth)

3.3 Output Voltage Ripple

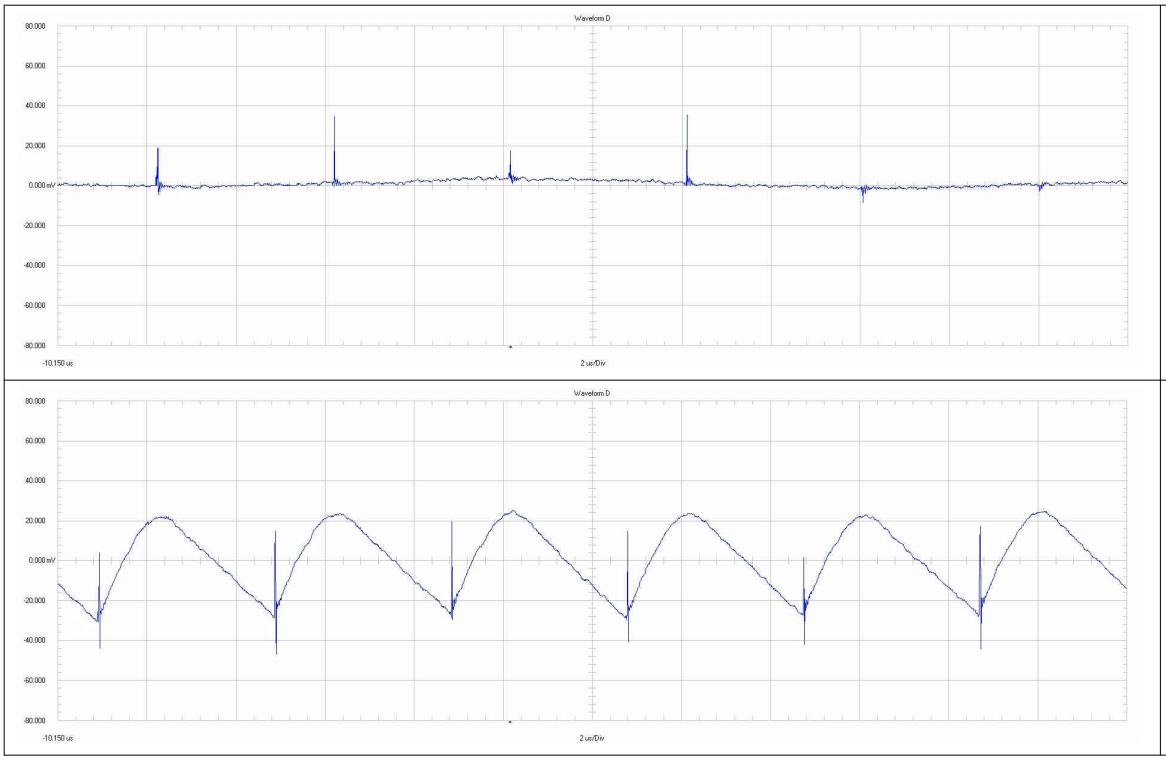
3.3.1 5-V Output Voltage (Primary)



5-V Output primary 20 mV / div 2 µs / div 20 MHz bandwidth	
	at LDO output 20 mV / div 2 µs / div 20 MHz bandwidth

Figure 3-6. Output Voltage Ripple (5 V_p)

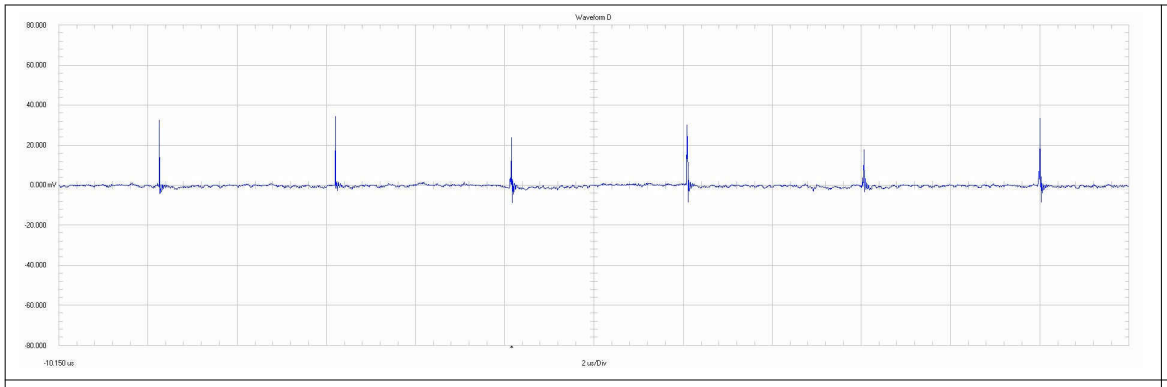
3.3.2 5-V Output Voltage (Secondary)



5 V Output secondary 20 mV / div 2 µs / div 20 MHz bandwidth	
	at LDO input 20 mV / div 2 µs / div 20 MHz bandwidth

Figure 3-7. Output Voltage Ripple (5 V_s)

3.3.3 3.3-V Output Voltage

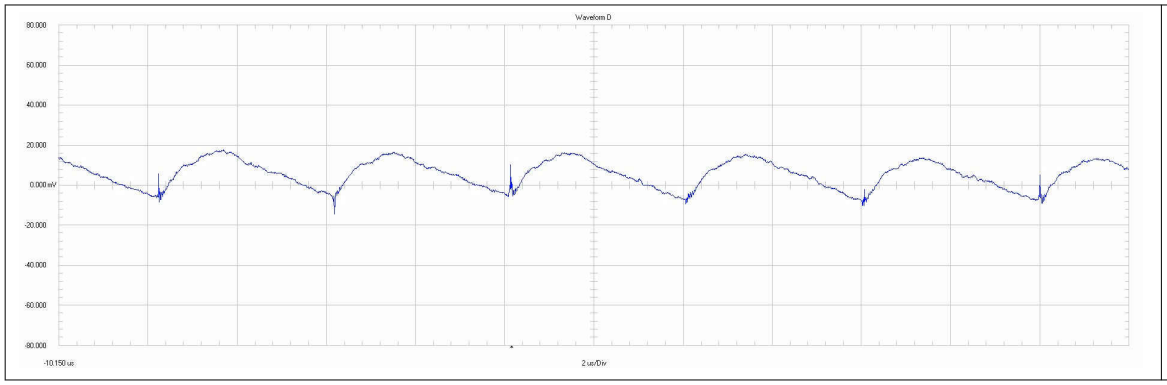


3.3-V output
20 mV / div
2 µs / div
20 MHz
bandwidth

at LDO Input
20 mV / div
2 µs / div
20 MHz
bandwidth

Figure 3-8. Output Voltage Ripple (3.3 V)

3.3.4 12-V Output Voltage



20 mV / div
2 µs / div
20 MHz
bandwidth

Figure 3-9. Output Voltage Ripple (12 V)

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