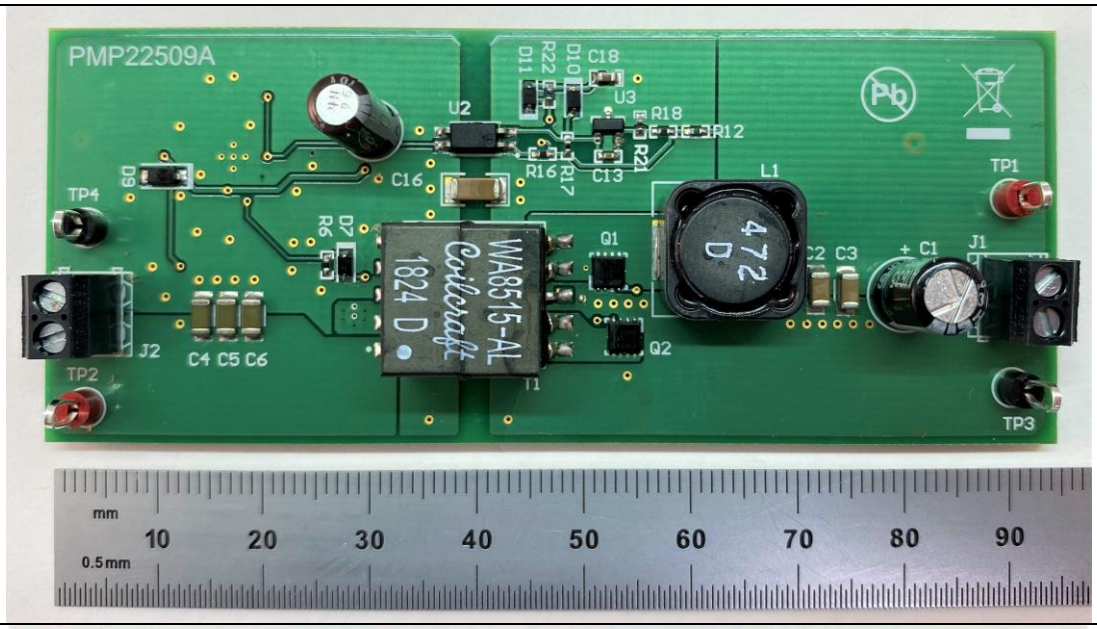
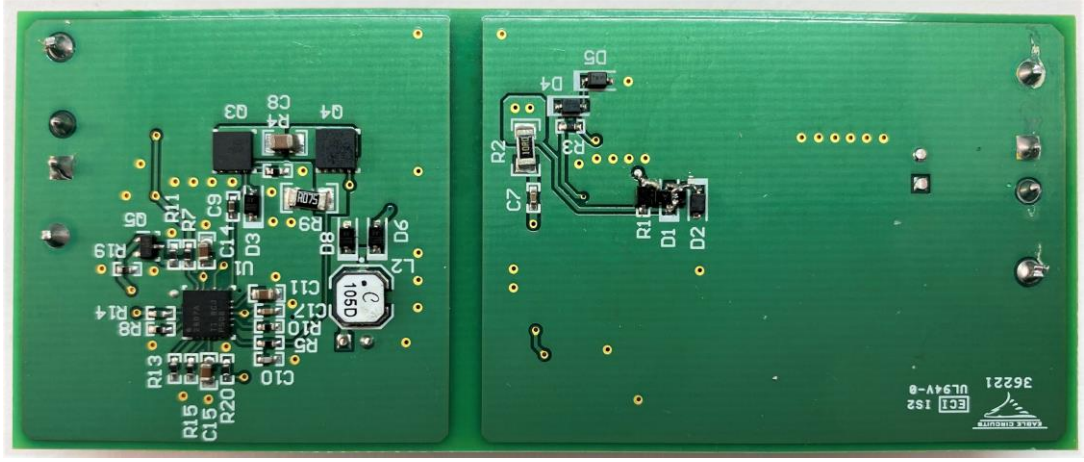
Test Report: PMP22509

18- to 36-VDC Input, 25-W DC-DC Active Clamp Forward Reference Design

Description

This active clamp forward design converts an 18-V to 36-V input to a 5-V, 25-W output. The reference design uses the UCC2897A advanced current-mode active-clamp PWM controller to simplify active clamp implementation with a P-channel auxiliary FET. The design achieves 91.7% peak efficiency at 24-V input. The active clamp topology allows for self-driving synchronous rectifier (SR) FETs, lowering cost and complexity on the secondary side. This design also uses a catalog transformer and inductor.





1 System Specification

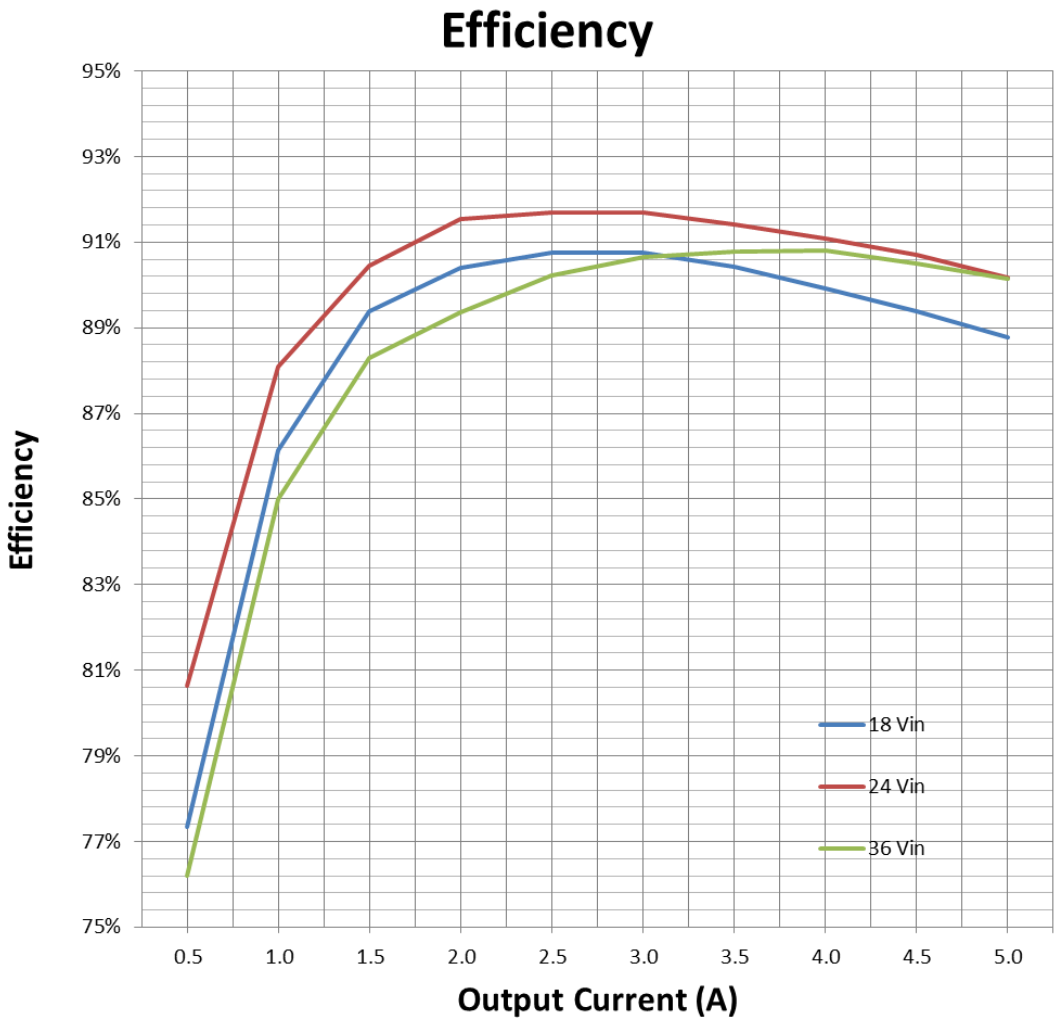
1.1 Board Dimension: 9.35cm x 3.83cm

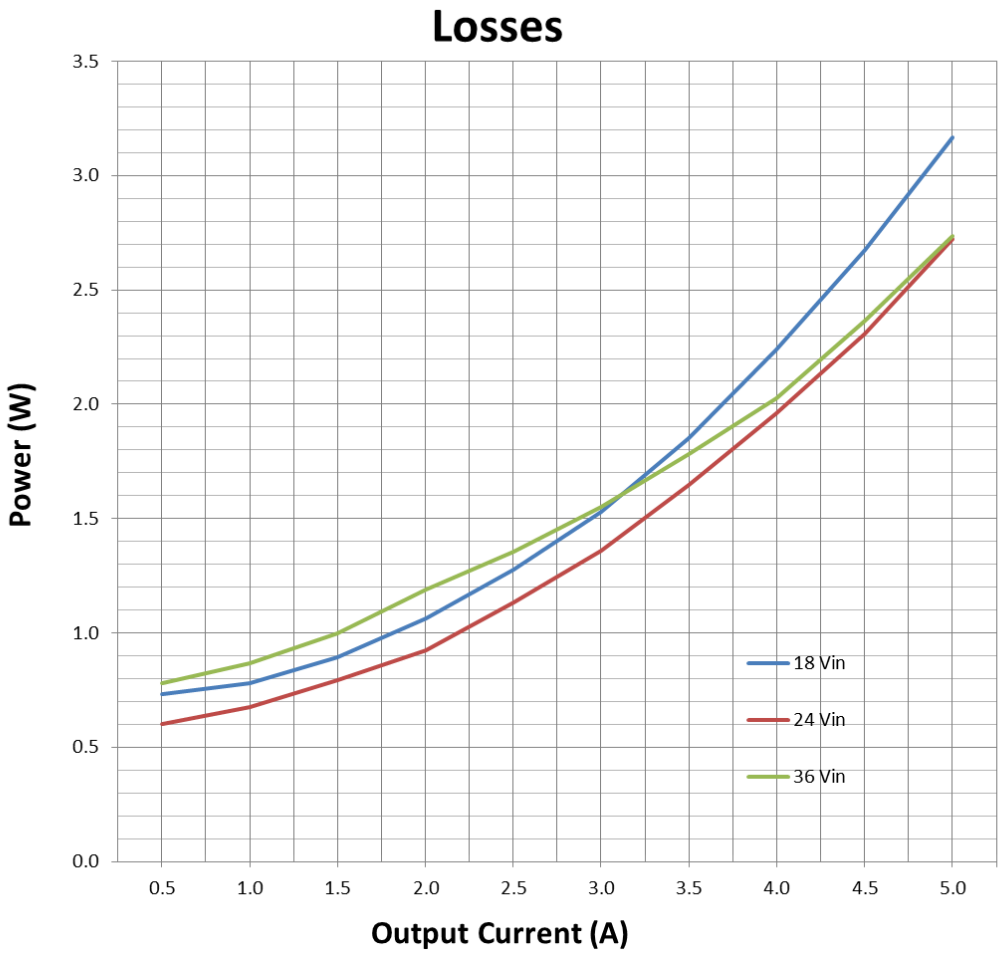
1.2 Input and Output Characteristics

PARAMETER	SPECIFICATIONS	
Input Voltage	18 – 36	Vdc
Output Voltage	5	Vdc
Output Current	5	A

2 Testing and Results

2.1 Efficiency Data





2.1.1 Raw Data

18Vin Efficiency

Vin (V)	Iin (A)	Pin (W)	Vout (V)	Iout (A)	Pout (W)	Eff (%)	Loss (W)
18.05	0.18	3.23	5.01	0.50	2.50	77.35%	0.73
18.11	0.31	5.63	5.01	0.97	4.85	86.14%	0.78
18.02	0.47	8.40	5.01	1.50	7.51	89.38%	0.89
18.00	0.62	11.07	5.01	2.00	10.01	90.40%	1.06
18.04	0.76	13.78	5.01	2.50	12.51	90.75%	1.28
18.04	0.92	16.54	5.01	3.00	15.01	90.75%	1.53
18.01	1.08	19.36	5.00	3.50	17.51	90.44%	1.85
17.99	1.23	22.20	5.00	3.99	19.96	89.92%	2.24
18.02	1.40	25.19	5.00	4.50	22.52	89.39%	2.67
18.02	1.56	28.18	5.00	5.00	25.01	88.77%	3.17

24Vin Efficiency

Vin (V)	Iin (A)	Pin (W)	Vout (V)	Iout (A)	Pout (W)	Eff (%)	Loss (W)
24.08	0.13	3.11	5.01	0.50	2.50	80.63%	0.60
24.07	0.24	5.68	5.01	1.00	5.00	88.09%	0.68
24.06	0.35	8.30	5.01	1.50	7.51	90.44%	0.79
24.04	0.46	10.94	5.01	2.00	10.01	91.55%	0.92
24.03	0.57	13.65	5.01	2.50	12.52	91.69%	1.13
24.02	0.68	16.38	5.01	3.00	15.02	91.69%	1.36
24.01	0.80	19.16	5.01	3.50	17.51	91.40%	1.65
23.99	0.92	21.97	5.00	4.00	20.02	91.09%	1.96
24.01	1.03	24.83	5.00	4.50	22.52	90.70%	2.31
23.99	1.16	27.73	5.00	5.00	25.01	90.18%	2.72

36Vin Efficiency

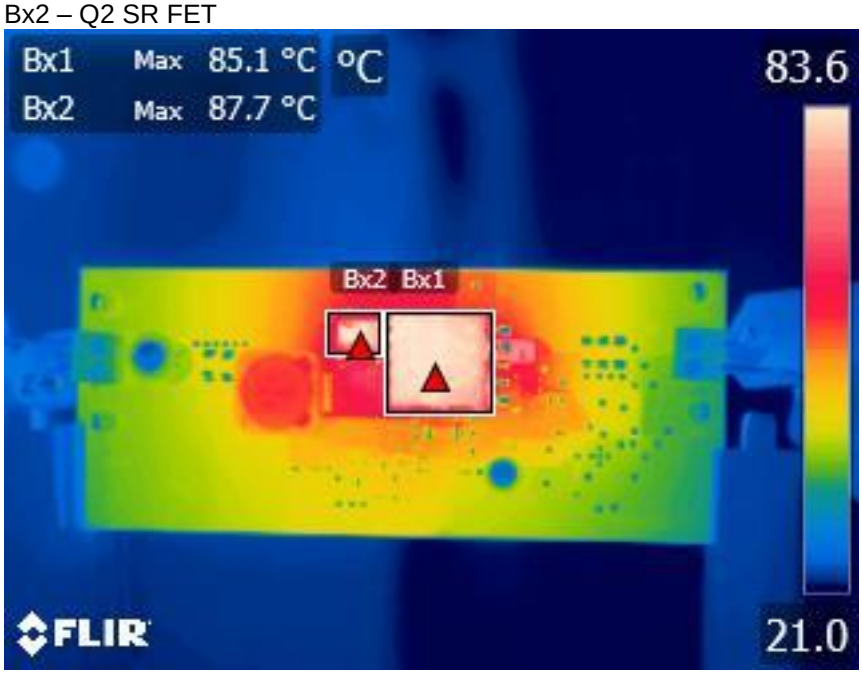
Vin (V)	Iin (A)	Pin (W)	Vout (V)	Iout (A)	Pout (W)	Eff (%)	Loss (W)
36.05	0.09	3.28	5.01	0.50	2.50	76.21%	0.78
36.07	0.16	5.77	5.01	0.98	4.90	84.99%	0.87
36.03	0.24	8.50	5.01	1.50	7.51	88.29%	1.00
36.02	0.31	11.20	5.01	2.00	10.01	89.37%	1.19
36.02	0.39	13.87	5.01	2.50	12.51	90.23%	1.36
36.04	0.46	16.58	5.01	3.00	15.03	90.65%	1.55
36.00	0.54	19.30	5.01	3.50	17.52	90.78%	1.78
35.90	0.61	22.04	5.01	4.00	20.01	90.80%	2.03
36.01	0.69	24.88	5.00	4.50	22.52	90.50%	2.36
36.00	0.77	27.76	5.00	5.00	25.02	90.14%	2.74

2.2 Thermal Images

The thermal images below show a top view and bottom view of the board. The board is placed vertically during the test. The ambient temperature was 25ºC with no air flow. The output was loaded with 5A for 15 minutes to reach thermal equilibrium.

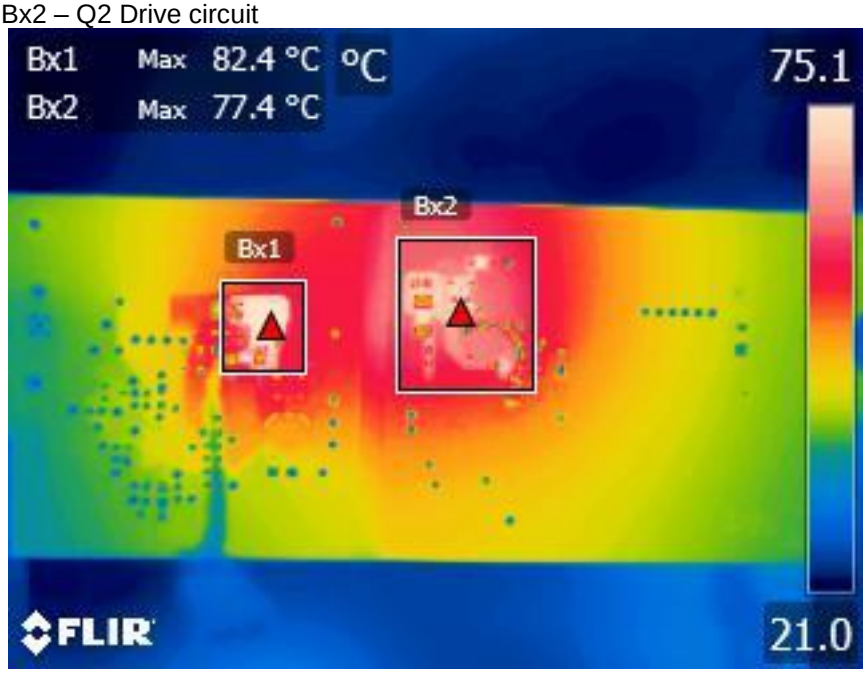
2.2.1 18V input, 5V/5A output, Top Side

Bx1 – T1
Bx2 – Q2 SR FET



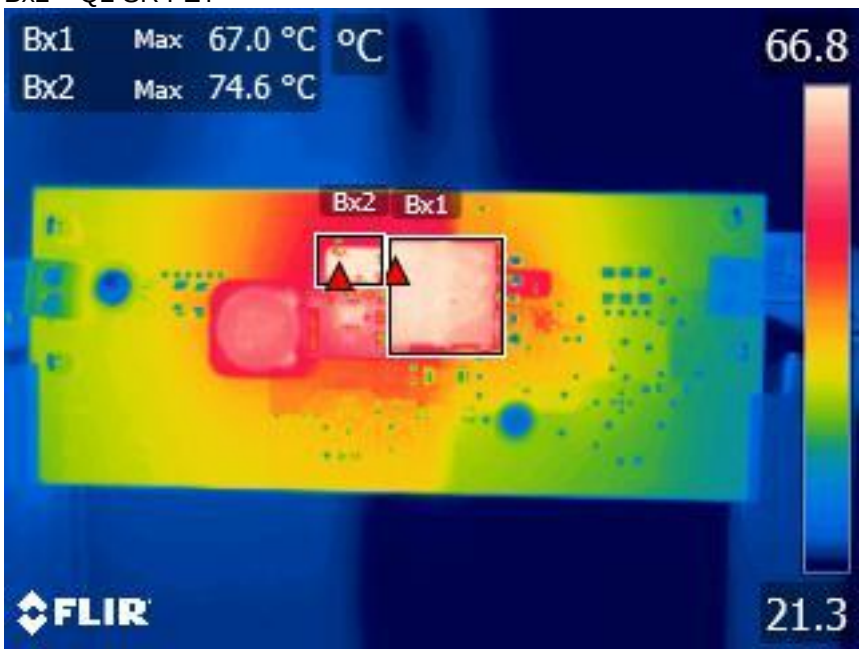
2.2.2 18V input, 5V/5A output, Bottom Side

Bx1 – Q4 Primary FET
Bx2 – Q2 Drive circuit



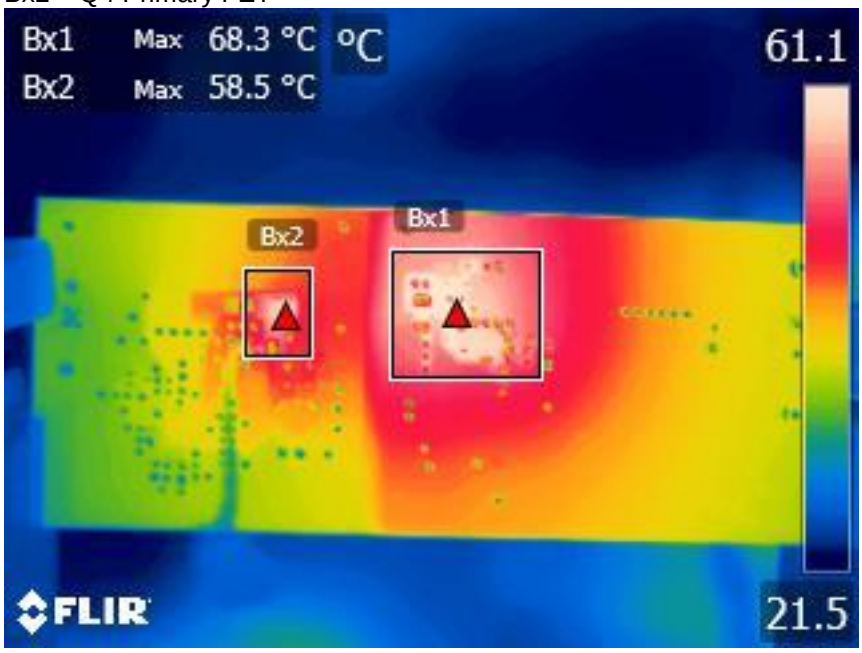
2.2.3 36V input, 5V/5A output, Top Side

Bx1 – T1
Bx2 – Q2 SR FET



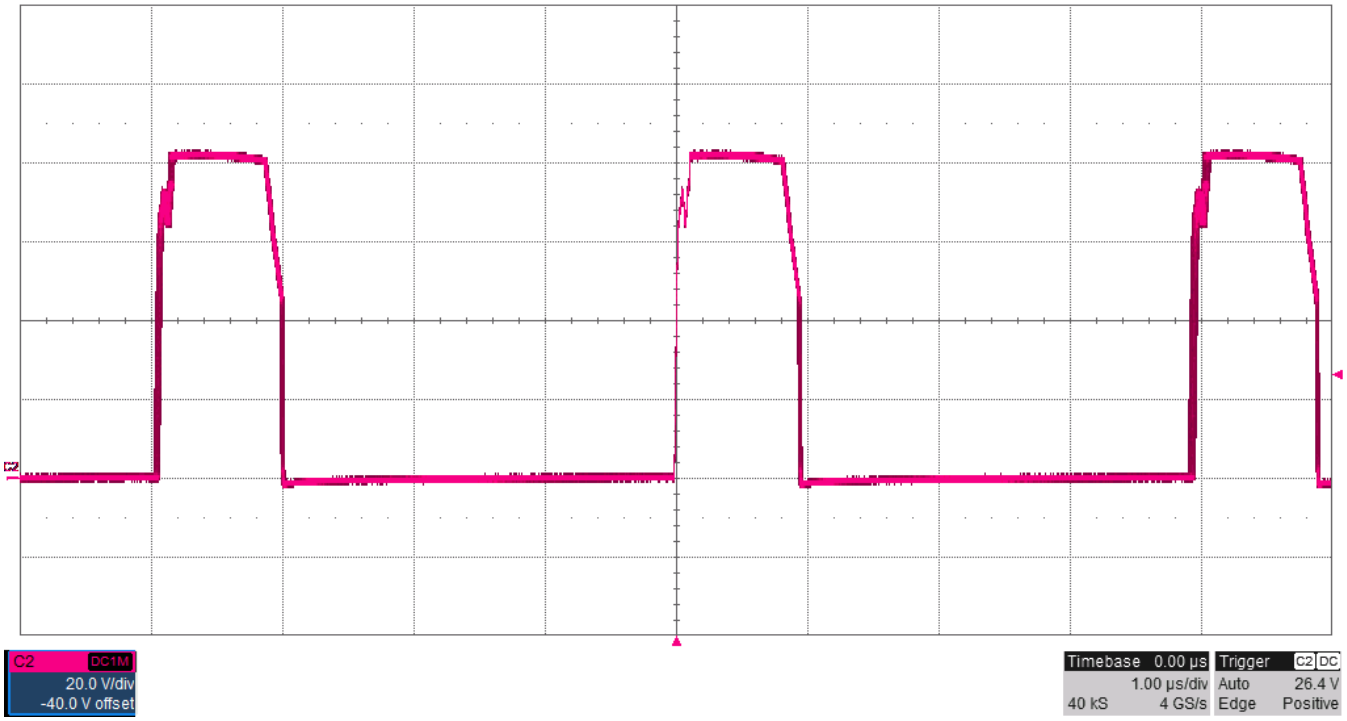
2.2.4 36V input, 5V/5A output, Bottom Side

Bx1 – Q2 Drive circuit
Bx2 – Q4 Primary FET

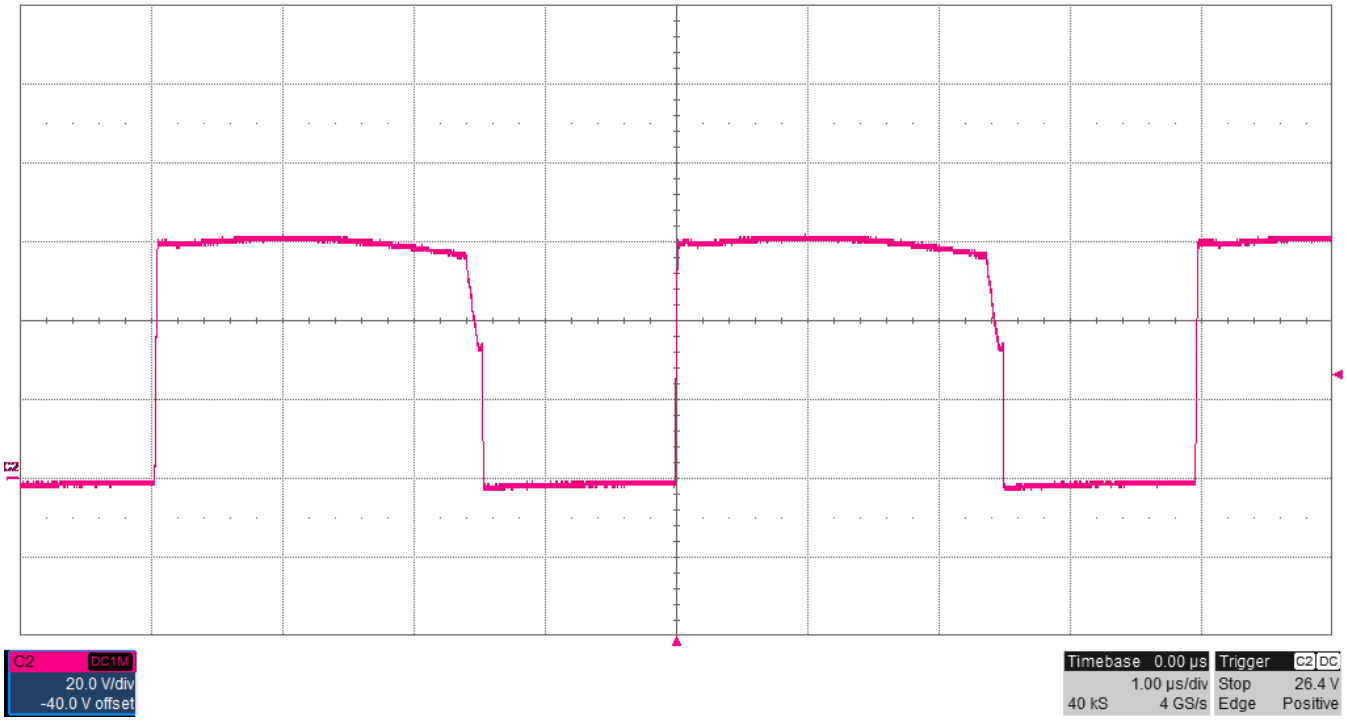


2.3 Switching Waveforms

2.3.1 Primary FET Vds (Q4) – 18Vin, 5A Load

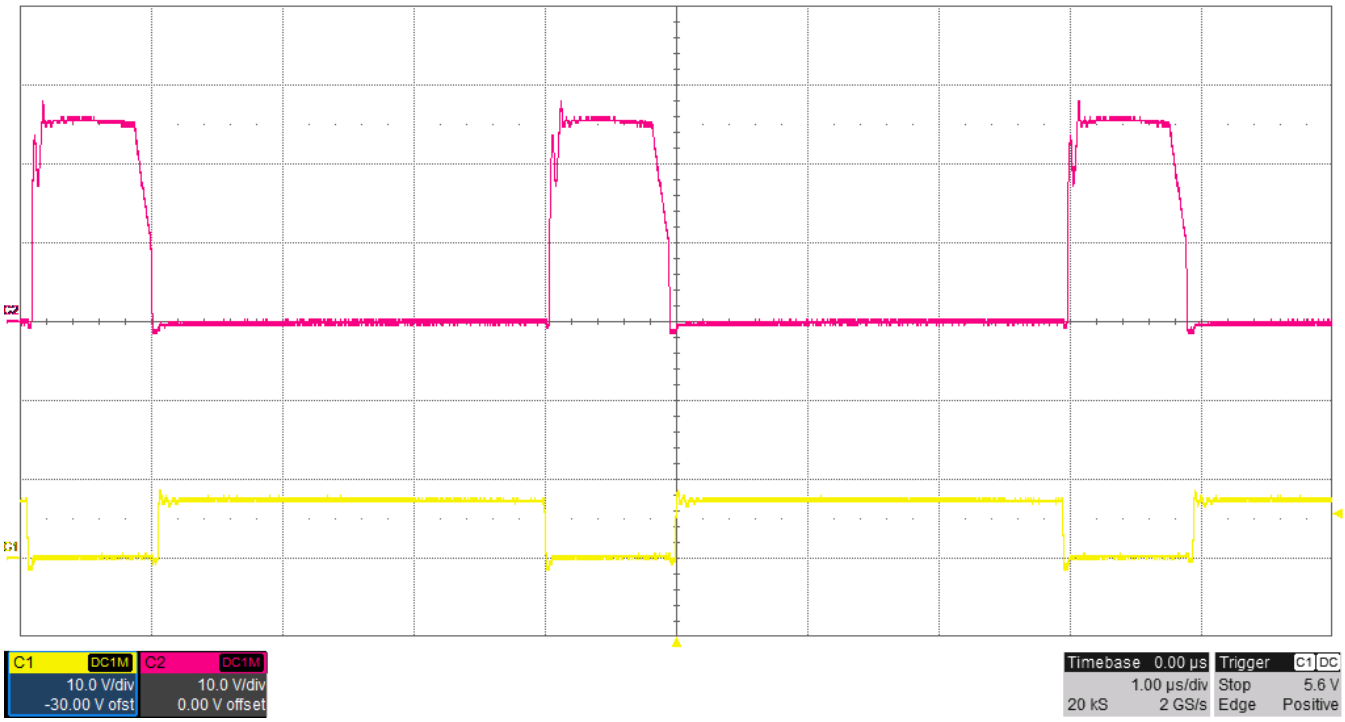


2.3.2 Primary FET Vds (Q4) – 36Vin, 5A Load



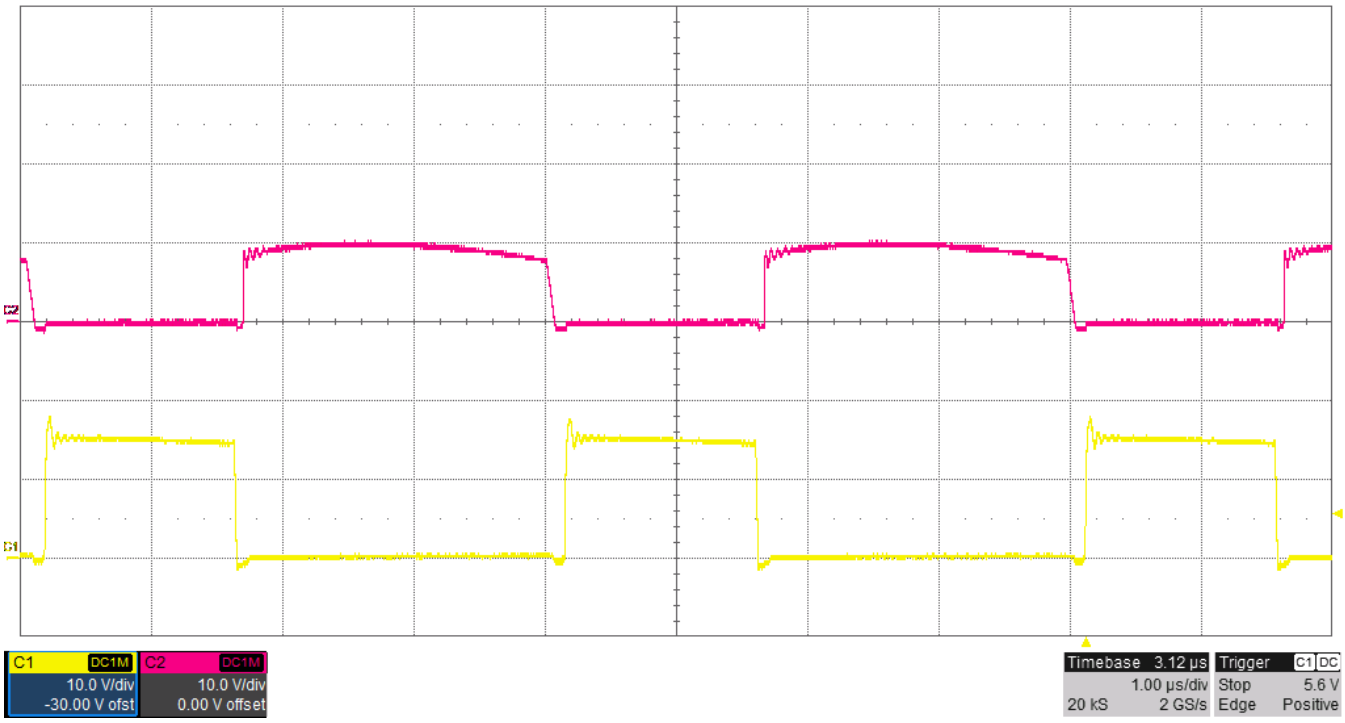
2.3.3 Sync FETs Vds (Q1, Q2) – 18Vin, 5A Load

C1 – Q1 (Pink)
C2 – Q2 (Yellow)



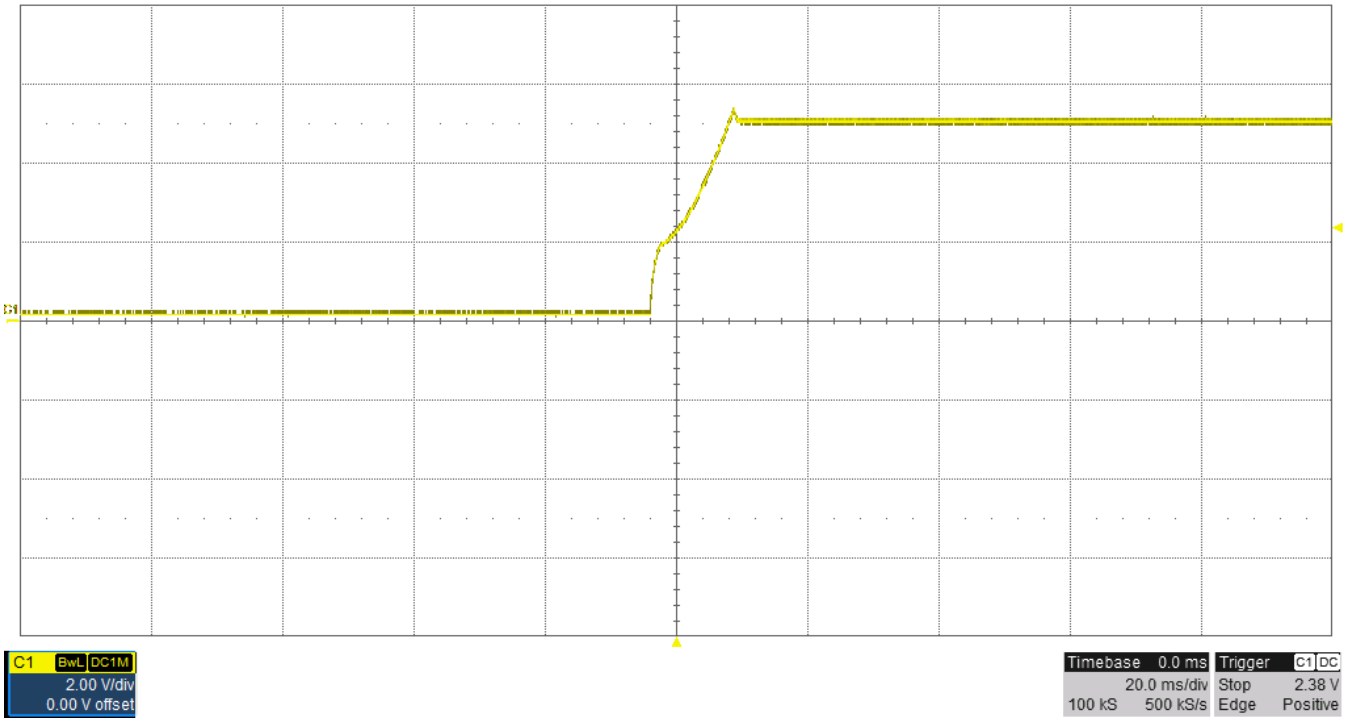
2.3.4 Sync FET Vds (Q1, Q2) – 36Vin, 5A Load

C1 – Q1 (Pink)
C2 – Q2 (Yellow)

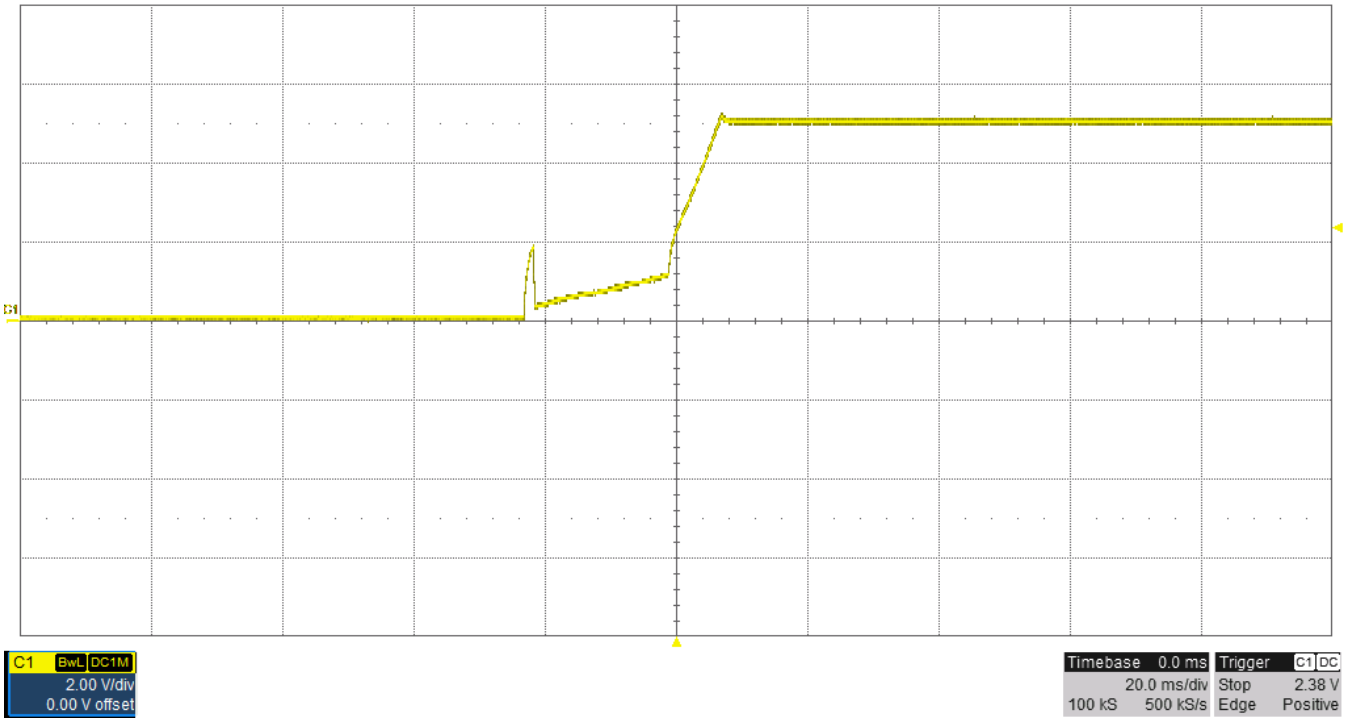


2.4 Startup

2.4.1 24V Input, No Load

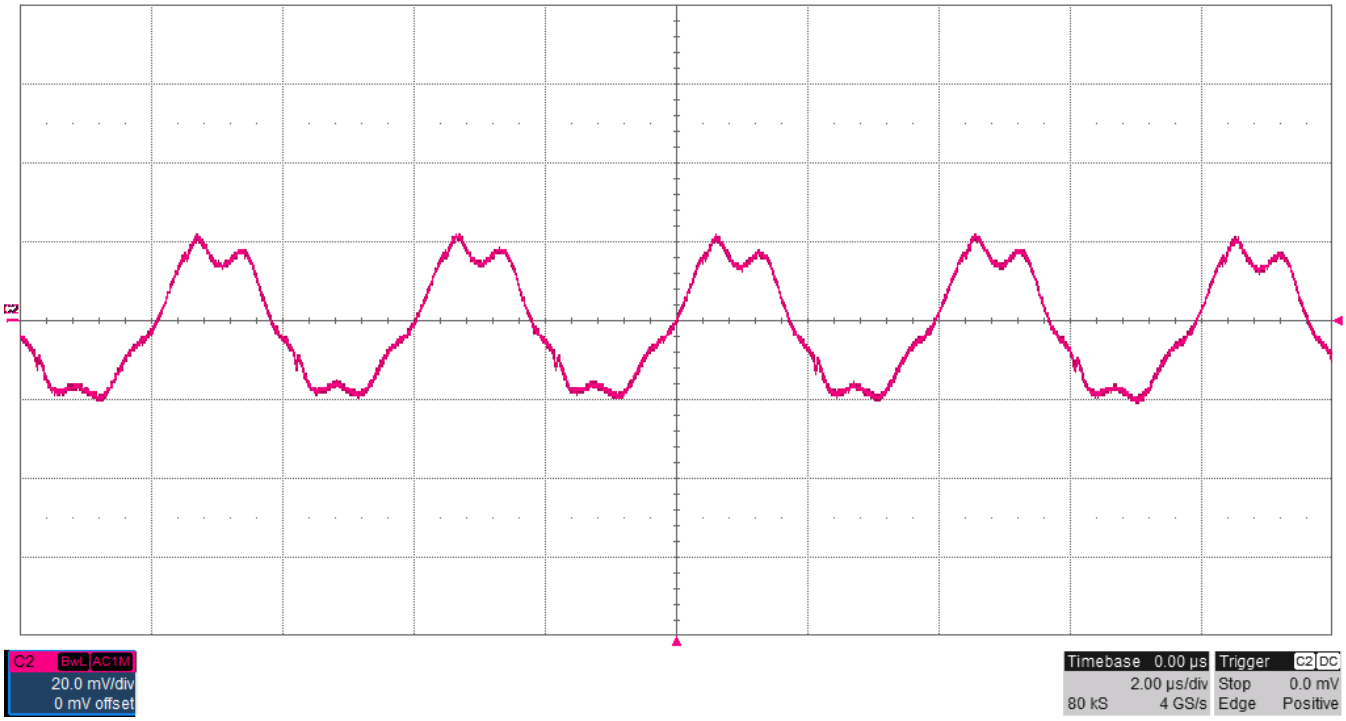


2.4.2 24V Input, 5A Load



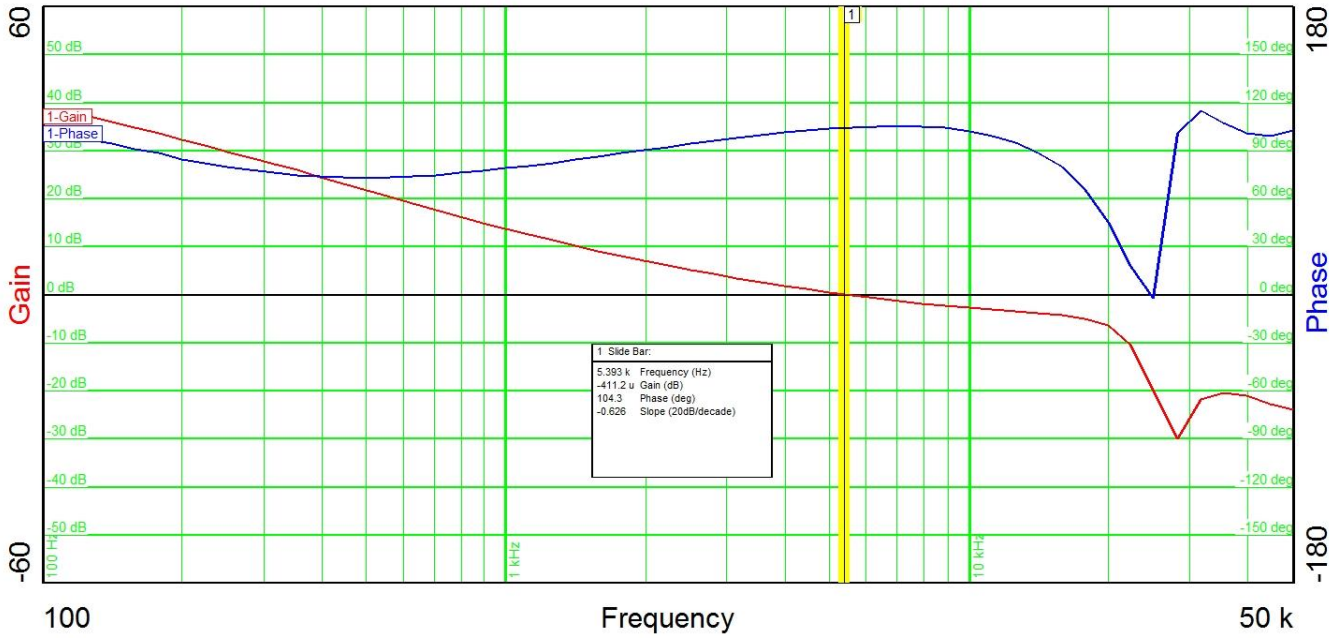
2.5 Output Ripple Voltage

2.5.1 24V Input, 5A Load



2.6 Loop Response

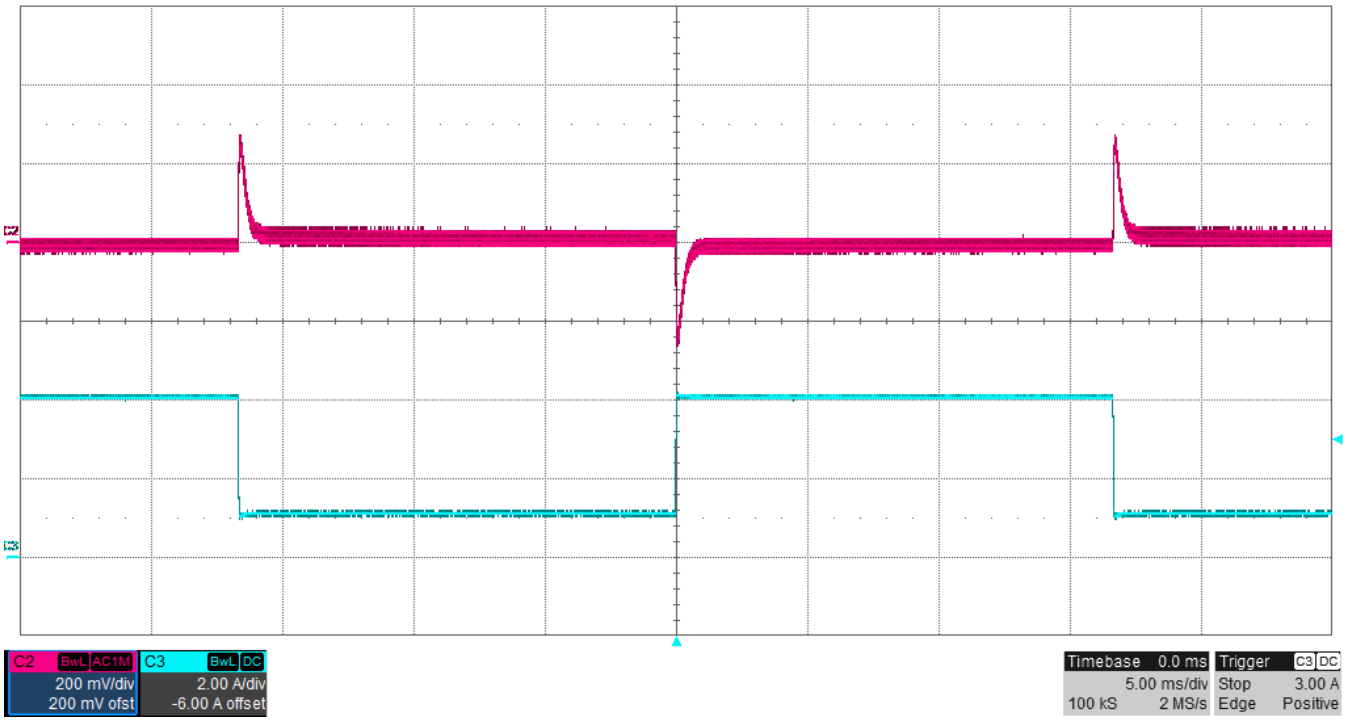
2.6.1 24V Input, 5A Load



2.7 Transient Response

2.7.1 24V Input, Load step from 1A to 4A

C2 – Output Voltage, AC Coupled (Pink)
C3 – Load Current



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