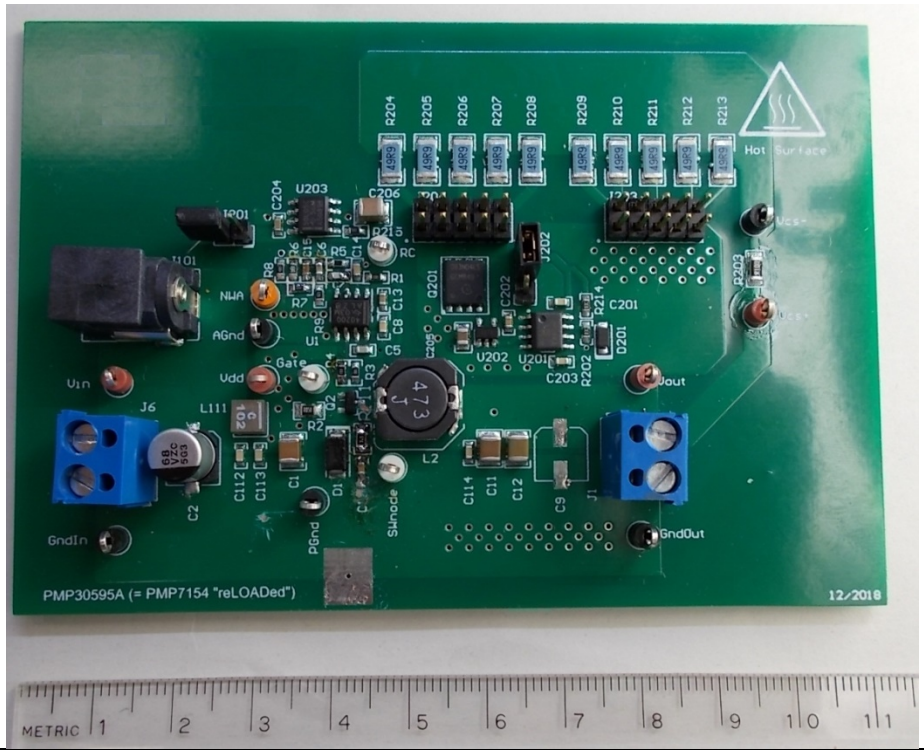
Test Report: PMP30595

Universal buck converter reference design for educational purposes

Description

This buck-converter design is mainly based on PMP7154, an easy to understand non synchronous topology for design training. At PMP30595 a tiny onboard electronics load has been added to demonstrate the relationship in between network analysis (= small signal analysis in frequency domain) and transient response (= large signal analysis in time domain). At PMP30595 the loop bandwidth has been squeezed to maximum, here cross over frequency at 20 kHz. For using this converter design in mass production it's recommended to use compensation values of PMP7154, cross over frequency 15 kHz with a safe gain margin. At this design the loop bandwidth has been exhausted to test Bode function of measurement equipment.

- Extra low input voltage <16 V for safety reasons
- 2.5mm jack to use cost effective 12 V wall adapter
- Input filter to demonstrate attenuation of reflected ripple (= conducted emissions)
- RC snubber circuit to demonstrate RF ripple reduction (= radiated emissions)
- Onboard load, load transient 500 mA<>1000 mA / 1 kHz / 50%, simply triggered by timer 555
- Load and load control could be fully disconnected from input and output for efficiency measurement
- High side shunt needs single differential probe or two probes plus using algorithm
- Numerous test points to access all voltages and waveforms



1 Test Prerequisites

1.1 Voltage and Current Requirements

Table 1. Voltage and Current Requirements

PARAMETER	SPECIFICATIONS
Input Voltage Range	8 V to 16 V
Output Voltage	5V
Output Current (max)	1A (via onboard load or external)
Onboard load	Up to 500mA static/dynamic load each

1.2 Considerations

- Resistors were use as load.
- Unless otherwise mentioned, input voltage was to 12 V and the output current was adjusted to 1A.
- Unless otherwise mentioned the jumper J201 was removed, all jumpers from J203 to J213 were removed and J202 was set to the upper position (2-3 = disable transient).
- The switching frequency of this prototype has been measured at 280kHz.

2 Testing and Results

2.1 Efficiency Graphs

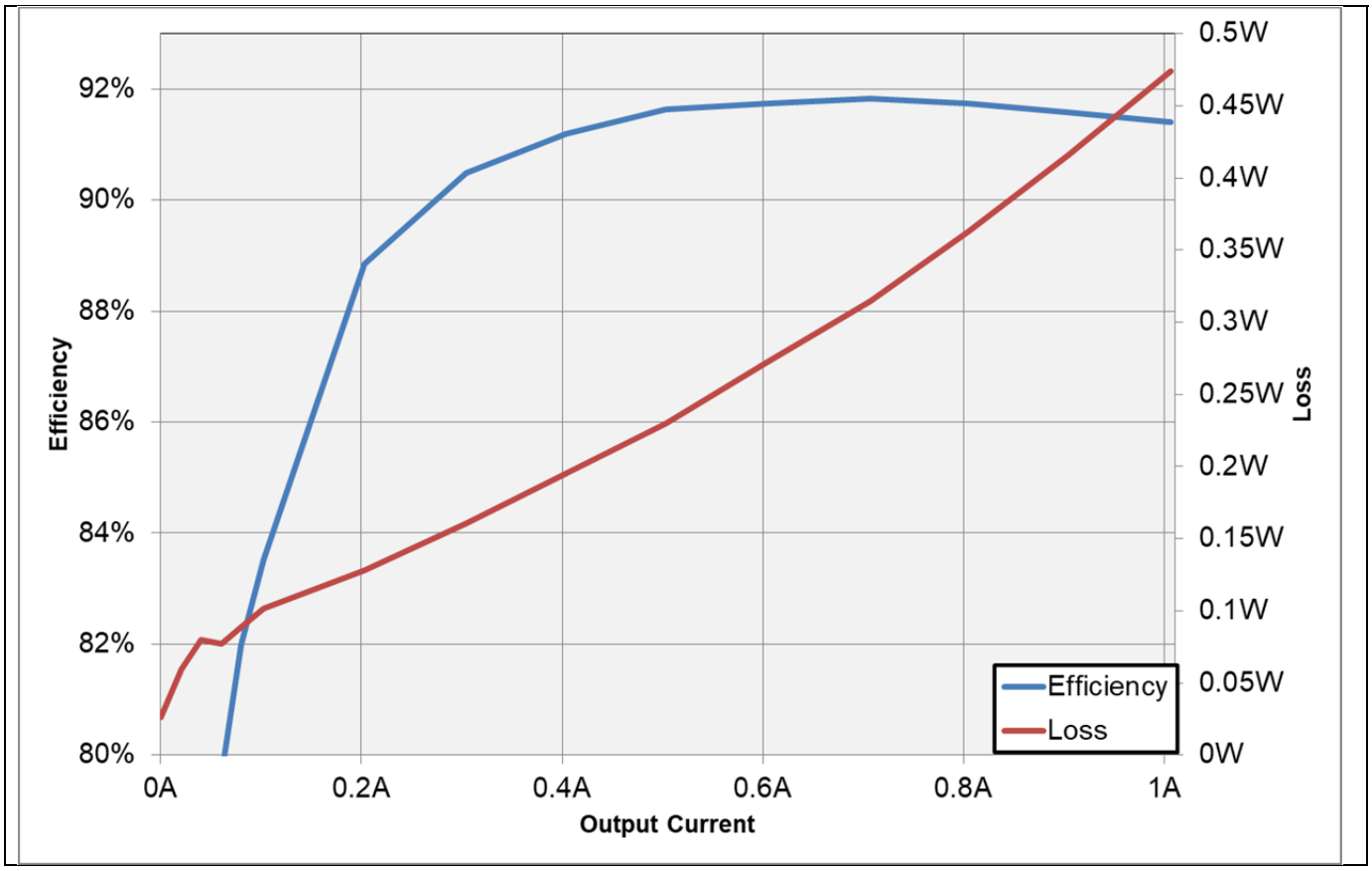


Figure 1 Efficiency and Loss vs Output Current

In general for output voltages >3.3V and currents <2A a nonsynchronous approach is a cost effective solution with acceptable power losses

2.2 Load Regulation

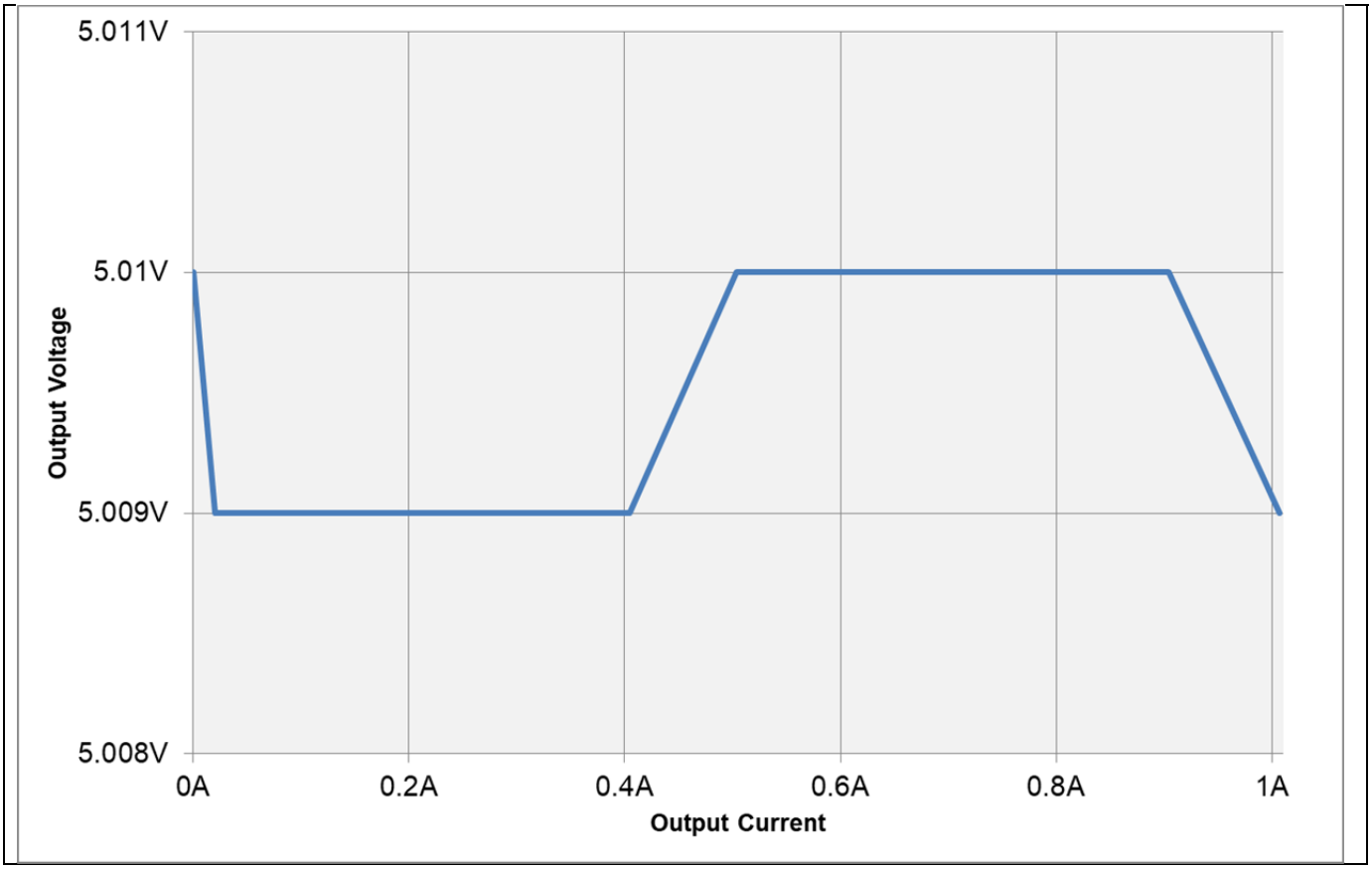


Figure 2 Output Voltage vs Output Current

By locating the test points to feedback divider it could be demonstrated that static load regulation is excellent, deviation 1mV.

2.3 Thermal Images

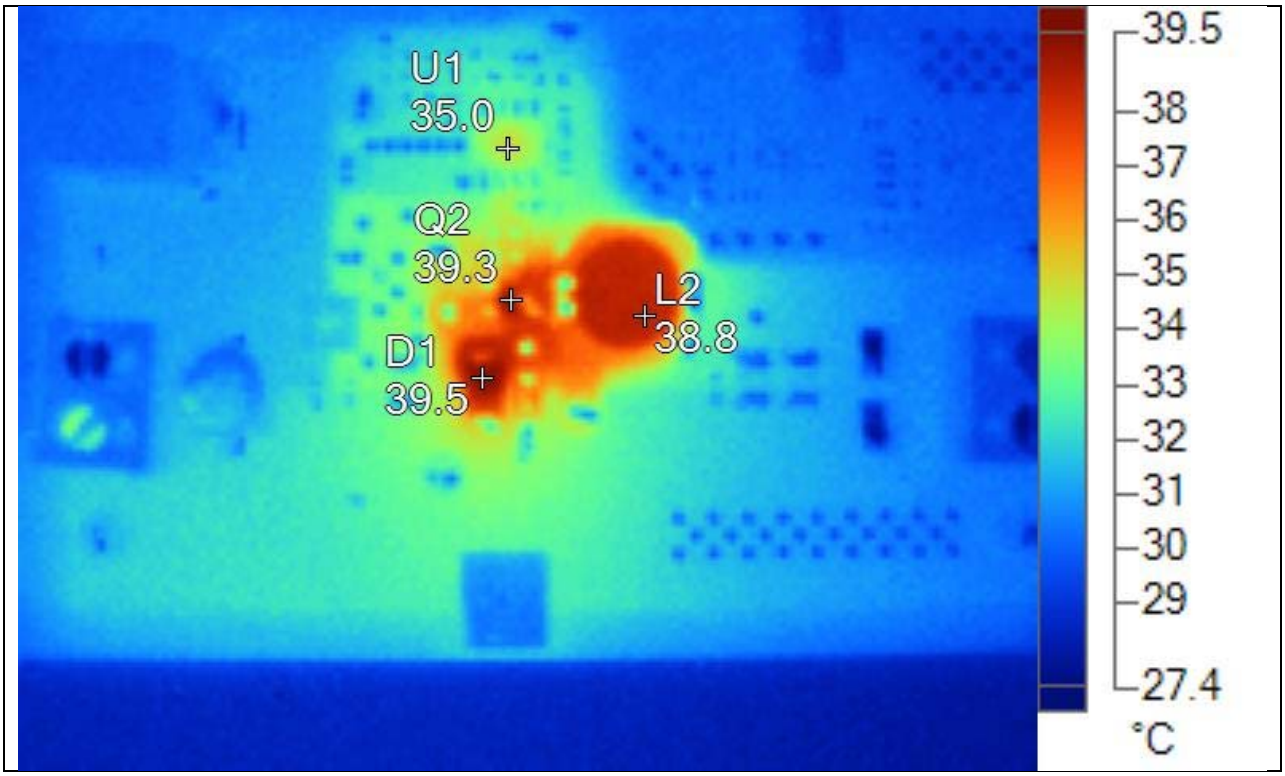


Figure 3 Thermal Image (12Vin, 1Aout)

Name	Temperature
D1	39.5°C
L2	38.8°C
Q2	39.3°C
U1	35.0°C

It could be seen that the SOT-23 geometry of P-MOS Q2 is fully sufficient to generate 5W output power with reasonable thermal performance. By smart parts selection even a nonsynchronous power stage could have a balanced thermal behavior across controller – switch – rectifier – inductor, here temperature rise <+20K.

3 Waveforms

3.1 Switching

All measurement done in this chapter are done with low impedance probe.

3.1.1 Test Point “SW node” across Diode (D1)

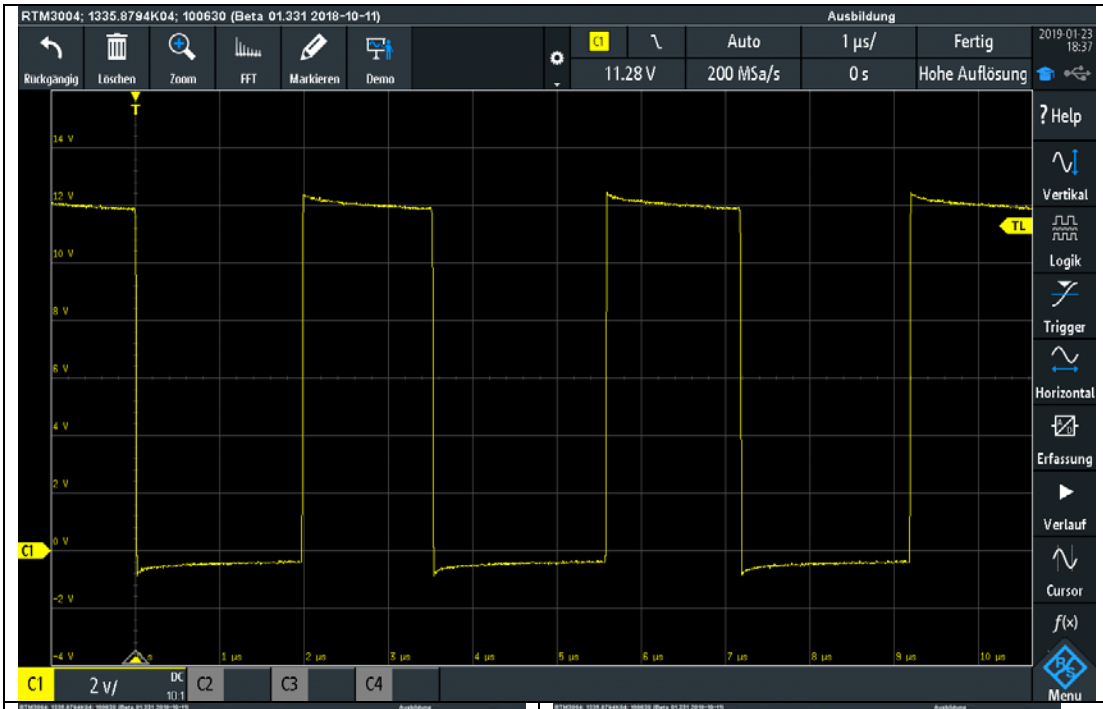
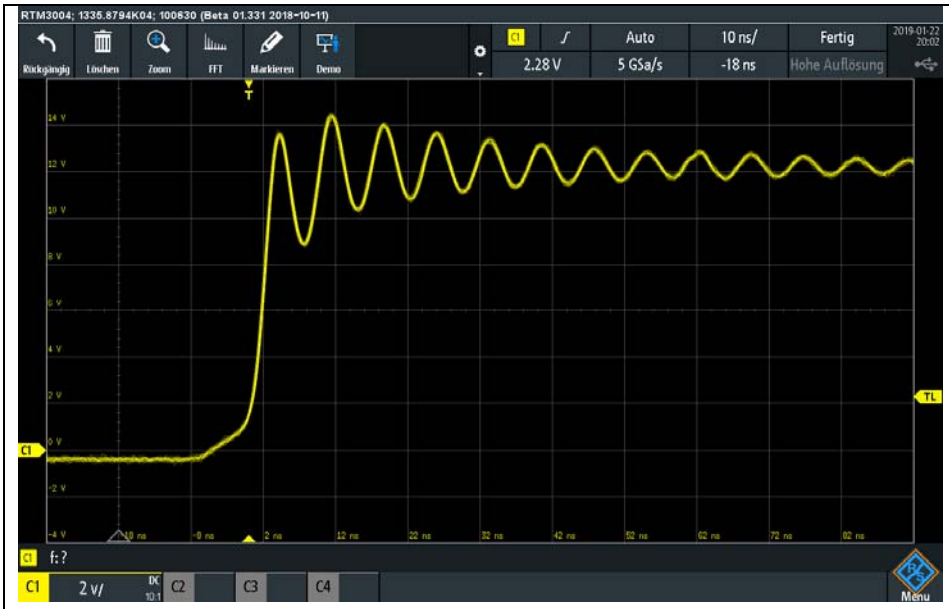
	2 V/div 1 µs/div full bandwidth
	20 ns/div full bandwidth

Figure 4 Switch Node to GND (D1)

The switch node has been measure with implemented RC snubber circuit R111/C111.

3.1.1.1 Switch Node *without* snubber.



2 V/div
10 ns/div

full bandwidth

Figure 5 Switch Node without snubber

The ringing frequency is 138 MHz (= AIR band !) with a peak voltage of 14.39 V, overshoot 2.5V.

3.1.1.2 Switch Node with 470pF (capacitor only)

2 V/div
10 ns/div

full bandwidth

Figure 6 Switch Node with 470pF

The ringing frequency is 68 MHz with a peak voltage of 13.9 V.

The ringing frequency with a 390 pF capacitor is 73. 2MHz (no figure). The decision was to use 470 pF.
The Snubber Calculator of the Power Stage Designer results a resistor value of 7.6 Ohms. Therefore a resistor of 7.5 Ohms is used.

3.1.1.3 Switchnode with 470pF and 7.5 Ohms

2 V/div
10 ns/div

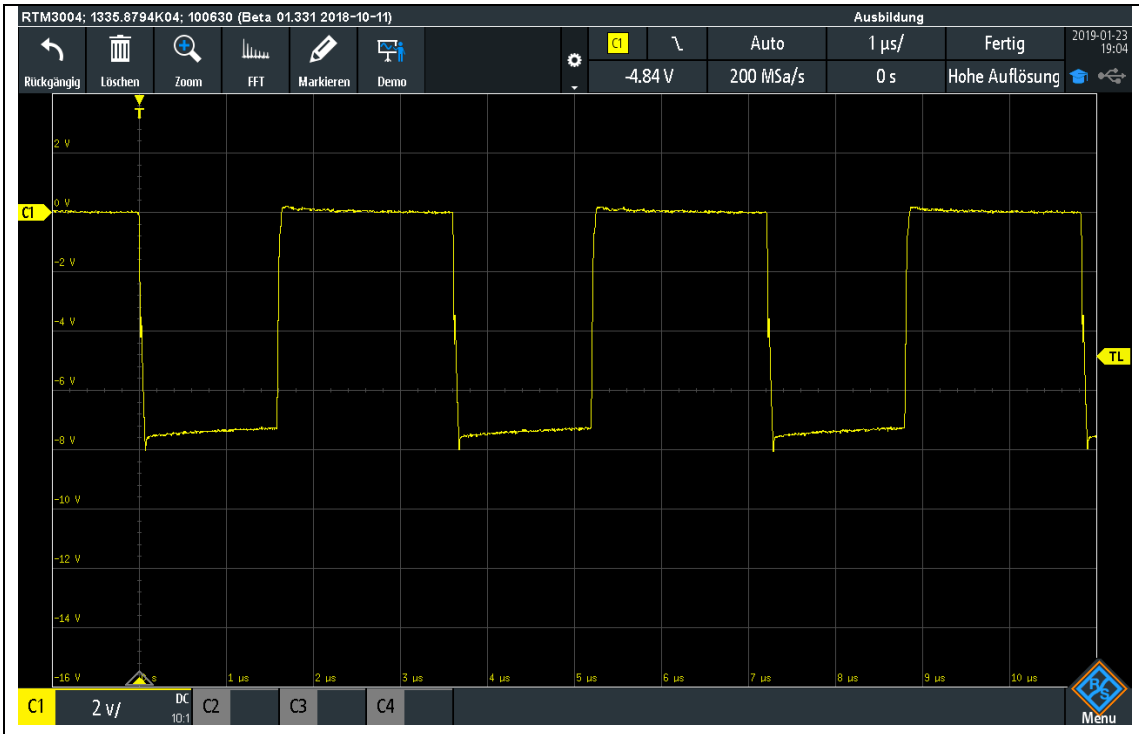
full bandwidth

Figure 7 Switch Node with C111=470pF and R111=7.5 Ohms

The peak voltage is 13.6 V – overshoot has been reduced and RF ringing removed.
Using strongest drivers, ultrafast FETs and doing a good layout such a almost ideal rectangular waveform is not possible. Overshoot could be reduced, ringing could be attenuated – but there will be in most cases some ringing.

Clamping way too hard will result in big power losses at the snubber resistor !

3.1.2 Gate to VIN, Output Gate Driver 8V



2 V/div
1 µs/div

full bandwidth

20 ns/div

full bandwidth

Figure 8 Gate to VIN

notice Miller plateau, enlarged cutout above

3.2 Output Voltage Ripple

Figure 9 Output Voltage (AC-coupled)

By using low ESR ceramic output capacitors the output ripple is fairly small <10mV;
Designator C9 allows to elaborate with electrolytics or polymer capacitors to replace MLCC.
For using electrolytics please recalculate ESR zero; if this zero is in range of cross over frequency place one of the poles on to that frequency.

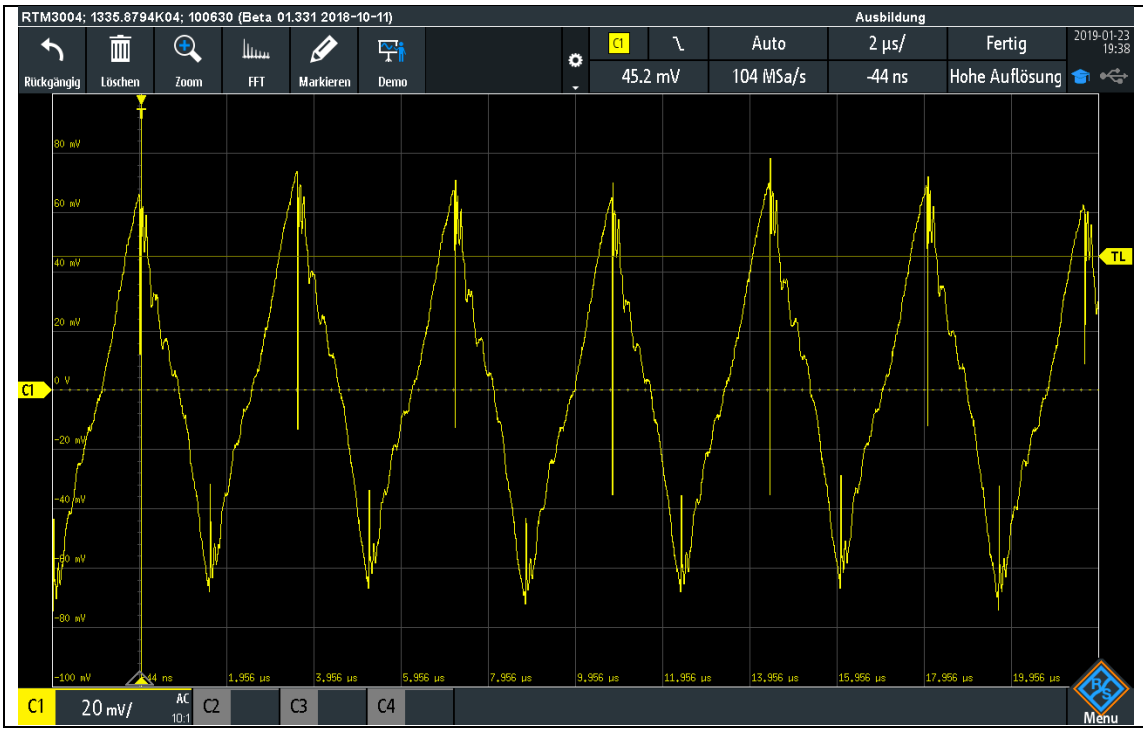
3.3 Input Voltage Ripple = reflected ripple = conducted emissions (!)

5 mV /div
2 µs / div

full bandwidth

converter input,
filtered

Figure 10 Vin (J5)



20 mV /div
2 µs / div

full bandwidth

power stage,
non-filtered

Figure 11 Power Stage Input (C1)

Input ripple depends on line and source impedance, a LISN could be used here – BUT:
The impact of a small input filter is notable. To reduce remaining RF spikes a ferrite bead is an option.
the triangular ripple voltage is attenuated from 140mVpp to less than 5mVpp, -29dB. (corner frequency 20kHz).

3.4 Bode Plot

	R&S RTM3004	Venable Mod. 3120
Bandwidth (kHz)	20.9	22.8
Phasemargin	64.3°	63.6°
slope (20dB/decade)		-1.12
gain margin (dB)	**-13.7**	**-14.4**
slope (20dB/decade)		-1.5
freq (kHz)	83	102

Table 1 Bode Plot Values

For measurement w/ R&S scope the signal generator output has been injected across isolation transformer “PICOTEST” Model J2100A, for injecting NWA signals of Venable transformer Model 200-002 has been used. The minor differences of both measurements could be neglected and might be caused by linearity of different transformers.

3.4.1 Oscilloscope Rohde & Schwarz RTM3004 plus Picotest J2100A

red curve=>phase 30° /div
blue curve=> gain 10 dB/div
X axis logarithmic frequency scale from 100 Hz to 200 kHz

Figure 12 Bode Plot generated with R&S Oszi

- For this measurement the 1:1 passive probes (RT-ZP1X) were used.
- Channel 3 was connected to the NWA test point and GND.
- Channel 2 was connected to VOUT and GND.
- The generator output of the oscilloscope was connected to the injection transformer (PICOTEST 1:1 J2100A) input.
- The injection transformer output was connected to NWA test point and VOUT
- Amplitude Profile: 100Hz to 8kHz => 0.5 V; 8kHz to 200kHz => 0.15 V
- A small gain margin could result in gate jitter, 15db+ is recommended

3.4.2 Reference: Venable Bode Analyzer Model 3120

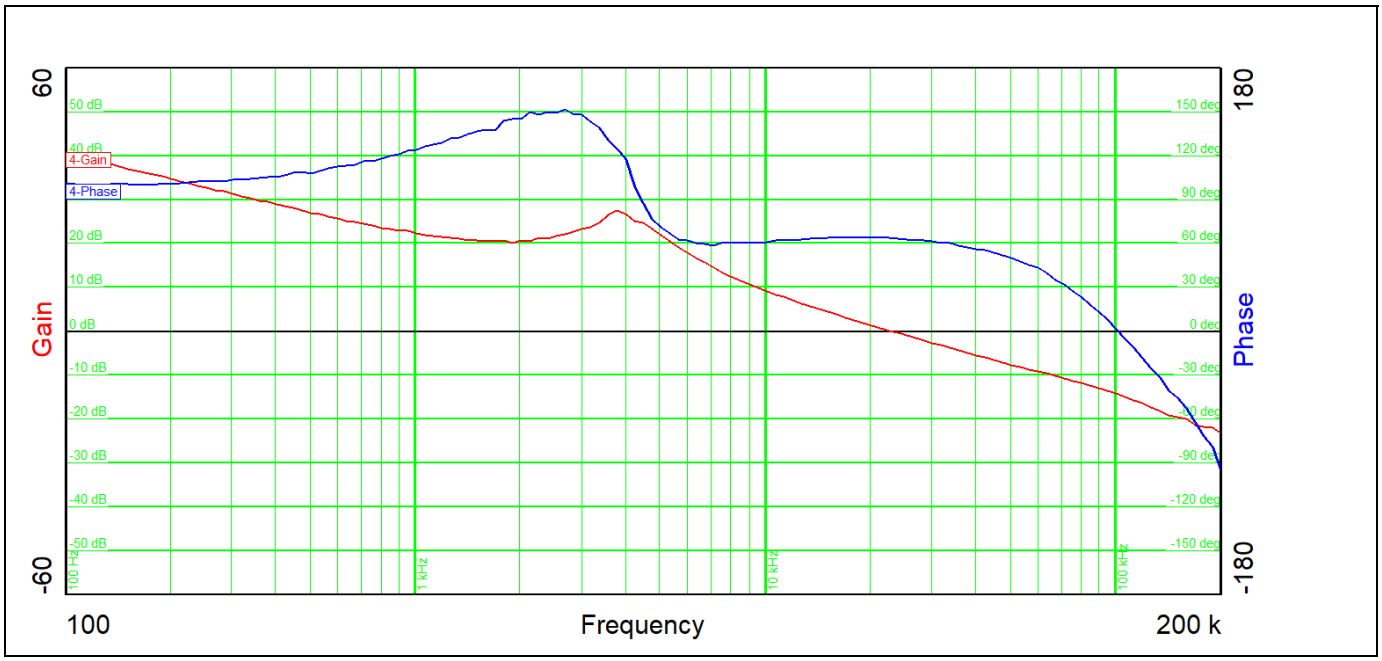


Figure 13 Bode Plot generated with Venable NWA

3.5 Load Transients 0.5A to 1A

The jumper J201 was set, all jumpers from J203 to J213 were set and J202 was set to the lower position (1:2 = enable transient).
The voltage on R203 (current sense resistor) was measured for getting the load current.
In Figure 14 the voltage on R203 was measured with a differential probe.

C1=> output voltage 50mV/div
20 MHz bandwidth

C3=> output current 0.5A/div
(50mV/div divided by 0.1 ohms [= current sense resistor])

200 µs/div

Figure 14 Load Transient

In Figure 15 voltage on the current sense resistor is calculated by subtracting the voltage measured between Vcs+ to GND with the voltage Vcs- to GND. This method allows measurement without differential probe.

C3=> output voltage (calculated)
50 mV/div
20 MHz bandwidth

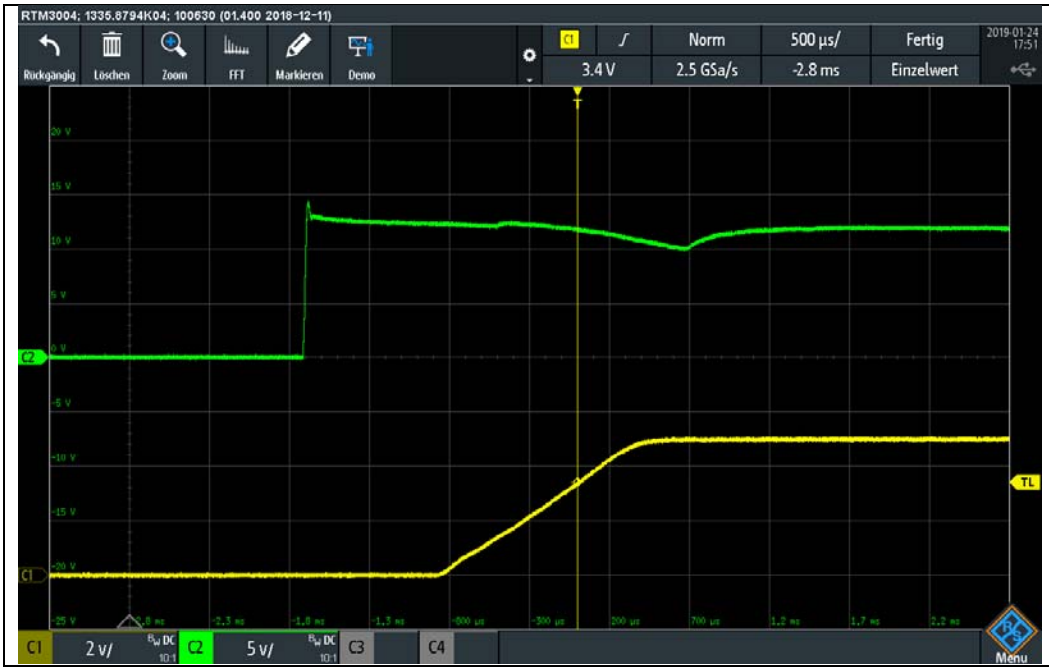
M2=> output current
0.5 A/div (50mV/div divided by 0.1 ohms [current sense resistor])
20 MHz bandwidth

C2=> Vcs-

500 µs/div

Figure 15 Load Transient

3.6 Start-up Sequence = Soft Start, here around 1ms



C2=> input voltage
5 V/ div

C1=> output voltage
2 V/ div
20 MHz bandwidth

500 µs/div

Figure 16 Start-up Sequence

3.7 Shut-Down Sequence

C2=> input voltage
5 V/ div

C1=> output voltage
2 V/ div
20 MHz bandwidth

500 µs/div

Figure 17 Shut-down Sequence

Start Up and Shutdown is measured to proof that converter is going properly into regulation without any overshoot or drop at output. Furthermore the calculated startup time could be verified.

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