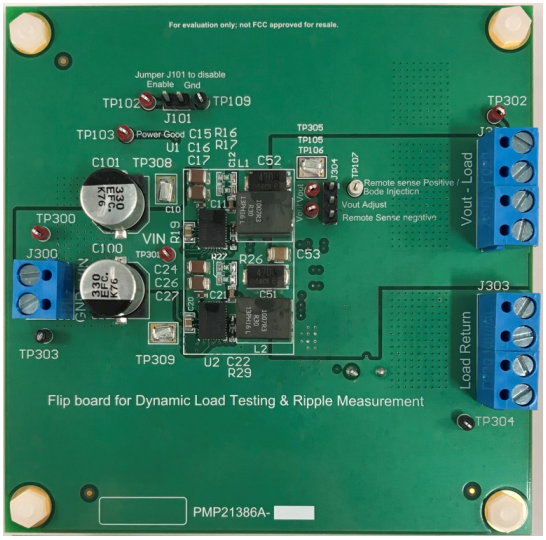
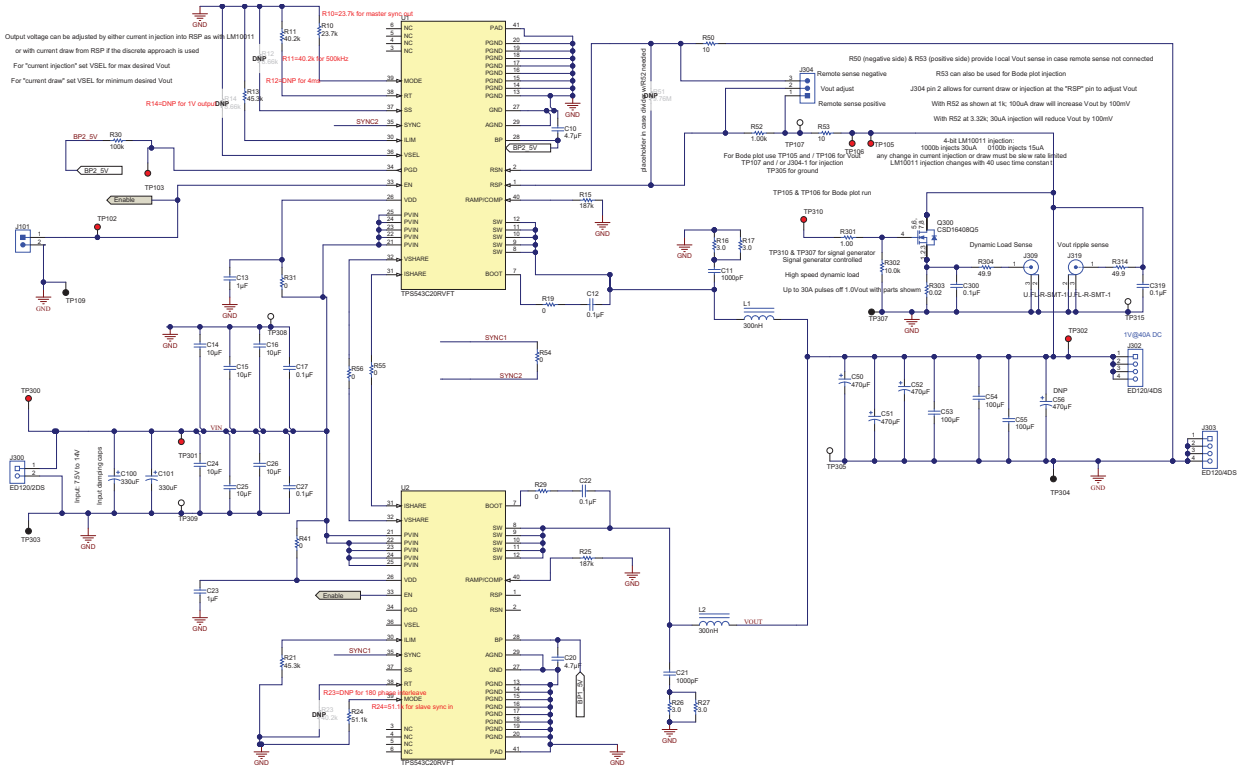
Test Report: PMP21386

Dual-Phase Stackable Buck Converter Reference Design With Full Test Capability

Description

This reference design utilizes two stackable buck converters to provide 0.85 V at 40 A in a compact (21 mm × 35 mm) form factor with low temperature rise with no airflow. The board includes an onboard high-speed dynamic load tester, output ripple probe interface, and test point for a stability analyzer, such as the Venable 2130. Internal compensation allows for design density and simplicity.





1 Test Prerequisites

1.1 Voltage and Current Requirements

Table 1. Voltage and Current Requirements

PARAMETER	SPECIFICATIONS
V_{IN}	4.5 V–16 V
V_{OUT}	1 V
I_{OUT}	40 A nominal

2 Testing and Results

2.1 Efficiency Graphs

Figure 1, Figure 2, and Figure 3 show the converter efficiency for a 4.5-, 12-, and 16-V input with a 1-V output.

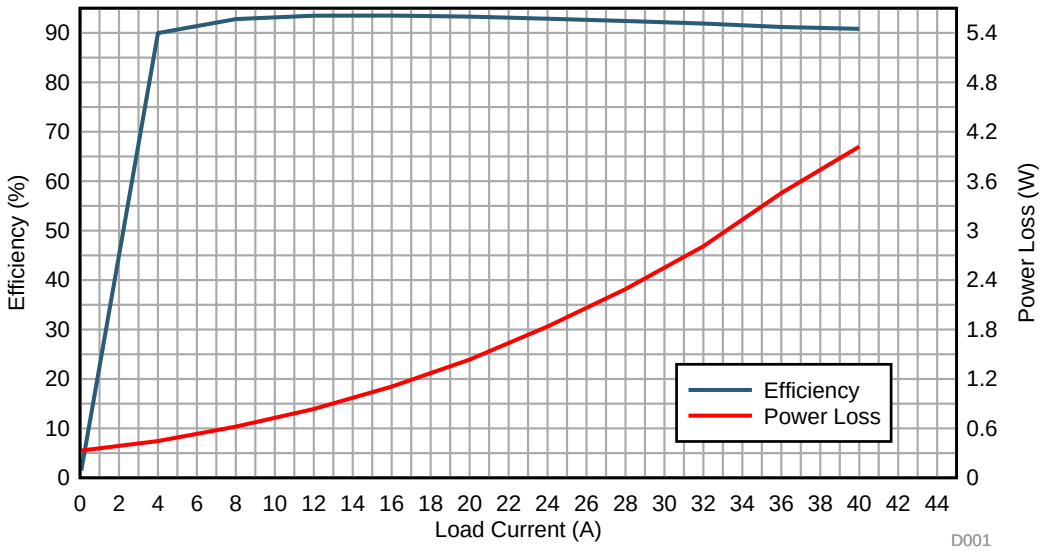


Figure 1. Converter Efficiency 4.5-V Input, 1-V Output

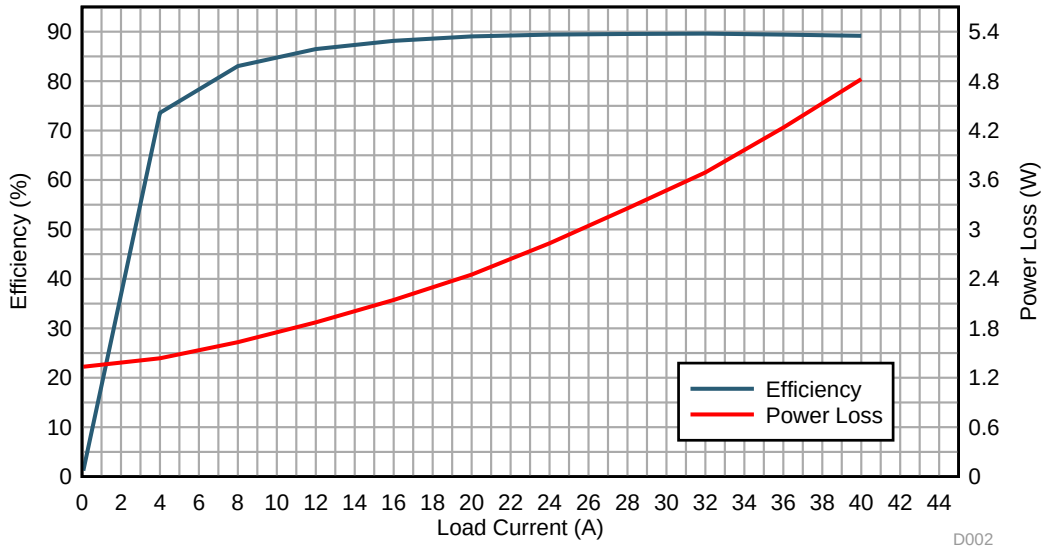


Figure 2. Converter Efficiency 12-V Input, 1-V Output

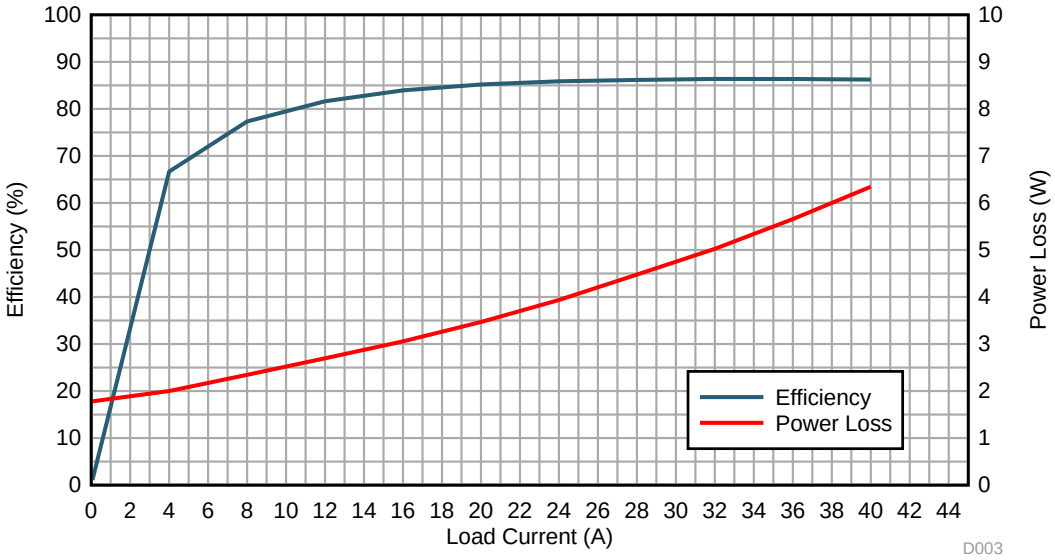


Figure 3. Converter Efficiency 16-V Input, 1-V Output

2.2 Efficiency Data

Table 2, Table 3, and Table 4 show the efficiency data for a 4.5-, 12-, and 16-V input with a 1-V output.

Table 2. Efficiency Data 4.5-V Input, 1-V Output

I_{OUT}	V_{OUT}	V_{IN}	I_{IN}	P_{IN}	P_{OUT}	Losses	Efficiency
0.000	1.000	4.5	0.07300	0.3285	0.00	0.33	0.0%
4.000	1.000	4.5	0.9880	4.4460	4.00	0.45	90.0%
8.000	0.999	4.5	1.914	8.6130	7.99	0.62	92.8%
12.000	0.998	4.5	2.847	12.8115	11.98	0.84	93.5%
16.000	0.997	4.5	3.791	17.0595	15.95	1.11	93.5%
20.000	0.997	4.5	4.750	21.3750	19.94	1.44	93.3%
24.000	0.996	4.5	5.720	25.7400	23.90	1.84	92.9%
28.000	0.995	4.5	6.700	30.1500	27.86	2.29	92.4%
32.000	0.995	4.5	7.700	34.6500	31.84	2.81	91.9%
36.000	0.994	4.5	8.720	39.2400	35.78	3.46	91.2%
40.000	0.993	4.5	9.720	43.7400	39.72	4.02	90.8%

Table 3. Efficiency Data 12-V Input, 1-V Output

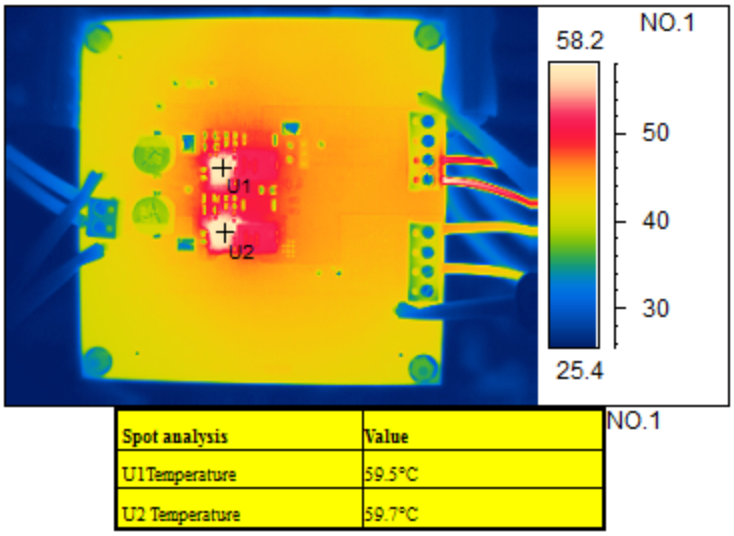
I_{OUT}	V_{OUT}	V_{IN}	I_{IN}	P_{IN}	P_{OUT}	Losses	Efficiency
0.000	1.000	12.0	0.11100	1.3320	0.00	1.33	0.0%
4.000	1.000	12.0	0.4530	5.4360	4.00	1.44	73.6%
8.000	0.999	12.0	0.802	9.6240	7.99	1.63	83.0%
12.000	0.998	12.0	1.154	13.8480	11.98	1.87	86.5%
16.000	0.997	12.0	1.508	18.0960	15.95	2.14	88.2%
20.000	0.997	12.0	1.866	22.3920	19.94	2.45	89.0%
24.000	0.996	12.0	2.228	26.7360	23.90	2.83	89.4%
28.000	0.995	12.0	2.593	31.1160	27.86	3.26	89.5%
32.000	0.995	12.0	2.961	35.5320	31.84	3.69	89.6%
36.000	0.994	12.0	3.335	40.0200	35.78	4.24	89.4%
40.000	0.993	12.0	3.712	44.5440	39.72	4.82	89.2%

Table 4. Efficiency Data 16-V Input, 1-V Output

I_{OUT}	V_{OUT}	V_{IN}	I_{IN}	P_{IN}	P_{OUT}	Losses	Efficiency
0.000	1.000	16.0	0.11100	1.7760	0.00	1.78	0.0%
4.000	1.000	16.0	0.3750	6.0000	4.00	2.00	66.7%
8.000	0.999	16.0	0.646	10.3360	7.99	2.34	77.3%
12.000	0.998	16.0	0.917	14.6720	11.98	2.70	81.6%
16.000	0.998	16.0	1.189	19.0240	15.97	3.06	83.9%
20.000	0.997	16.0	1.463	23.4080	19.94	3.47	85.2%
24.000	0.996	16.0	1.740	27.8400	23.90	3.94	85.9%
28.000	0.995	16.0	2.021	32.3360	27.86	4.48	86.2%
32.000	0.995	16.0	2.304	36.8640	31.84	5.02	86.4%
36.000	0.994	16.0	2.590	41.4400	35.78	5.66	86.4%
40.000	0.993	16.0	2.879	46.0640	39.72	6.34	86.2%

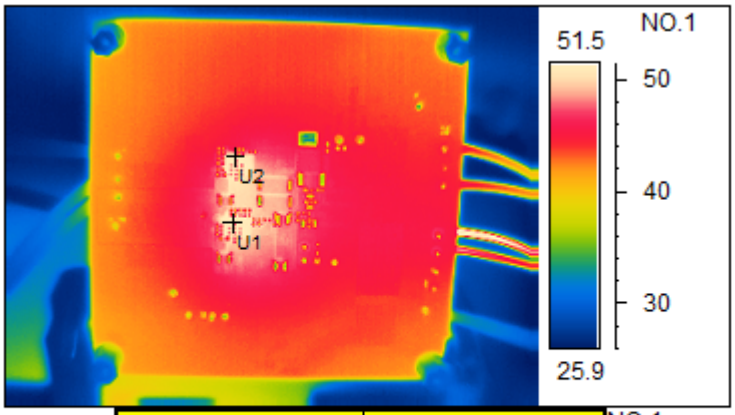
2.3 Thermal Images

The thermal images in Figure 4 and Figure 5 show operation at 12-V input and 1 V at 40-A output, with no airflow. The board ran for 20 minutes under these conditions before the images were taken.



Spot analysis	Value
U1 Temperature	59.5°C
U2 Temperature	59.7°C

Figure 4. Top Thermal



Spot analysis	Value
U1 Temperature	51.6°C
U2 Temperature	51.7°C

Figure 5. Bottom Thermal

2.4 Dimensions

Figure 6 and Figure 7 present the top and bottom photos of the PMP21386 board.

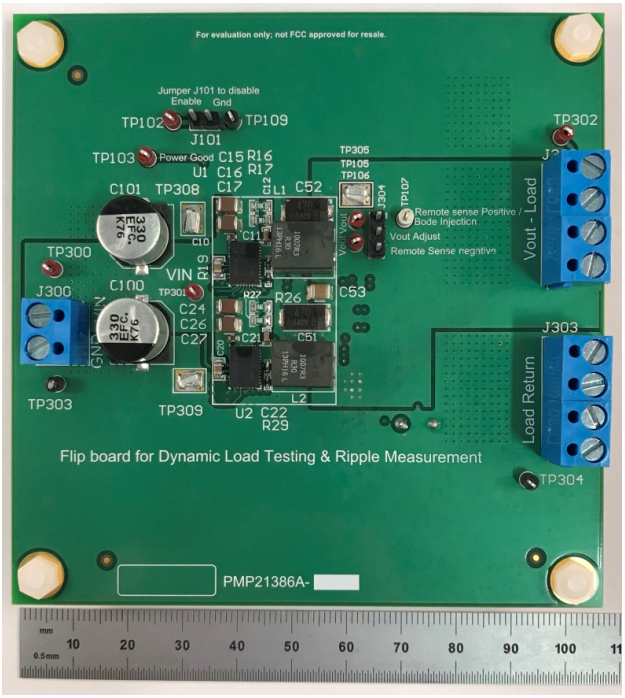


Figure 6. Top of PMP21386 Board

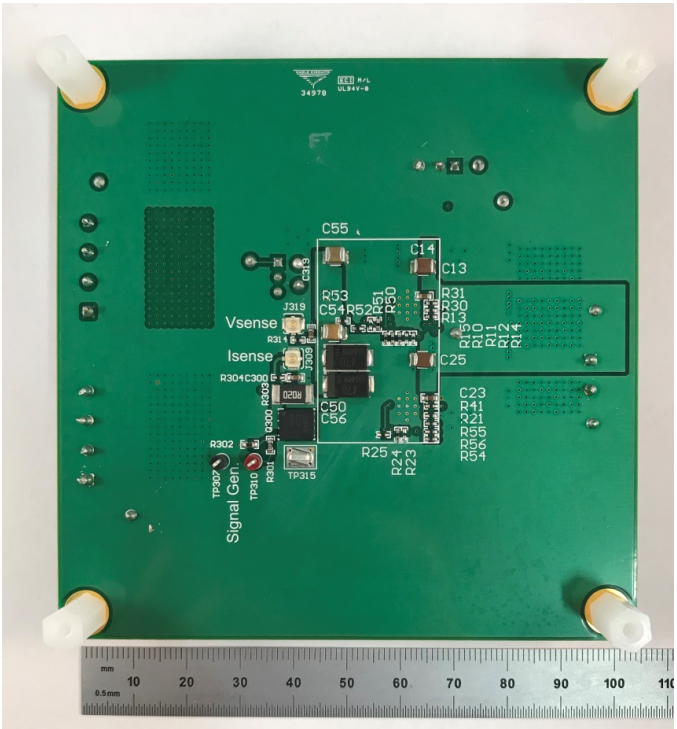


Figure 7. Bottom of PMP21386 Board

3 Waveforms

3.1 Switching

Figure 8 shows the switch node voltage of the master TPS53C20. The input voltage is 12 V and the 1-V output is loaded to 40 A. (5 V/div, 1 µs/div). Figure 9 is a view of the wavform when zoomed in.

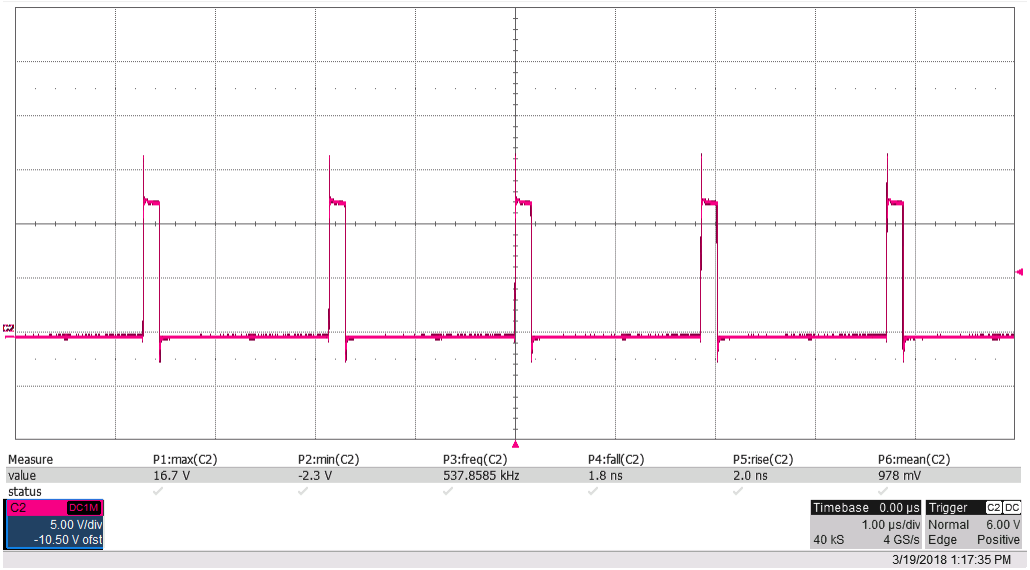


Figure 8. Switch Node Voltage, V_{IN} = 12 V, 1-V V_{OUT} = 40-A Load

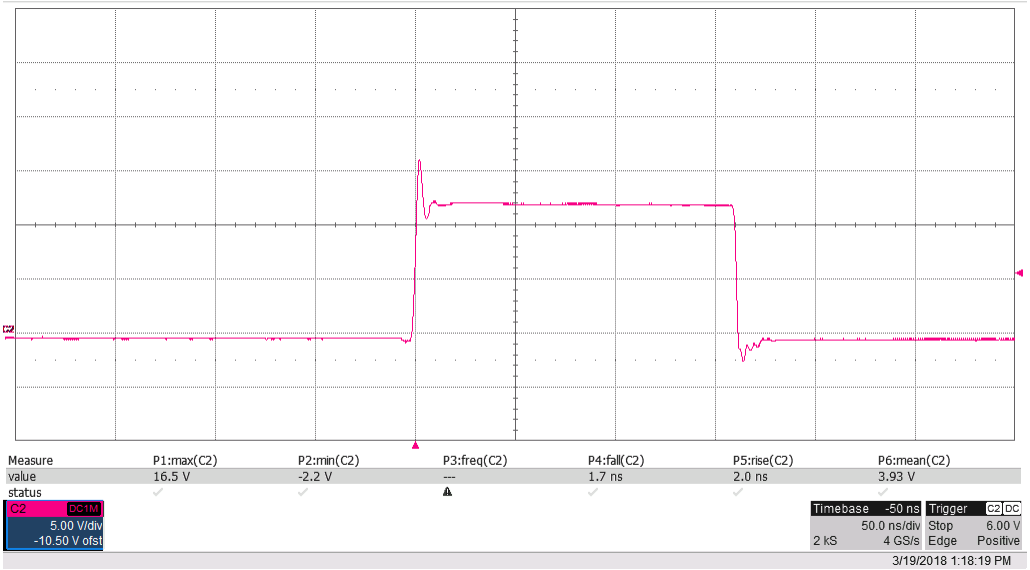


Figure 9. Switch Node Voltage Zoom, V_{IN} = 12 V, 1-V V_{OUT} = 40-A Load

3.2 Output Voltage Ripple

Figure 10 shows the output ripple voltage. The image was taken with the 1-V output loaded to 40 A and the input voltage set to 12 V.

The ripple measurement was taken using connections on the bottom side of the board. The peak-to-peak ripple is 8.3 mV (10 mV/div, 5 µs/div) .

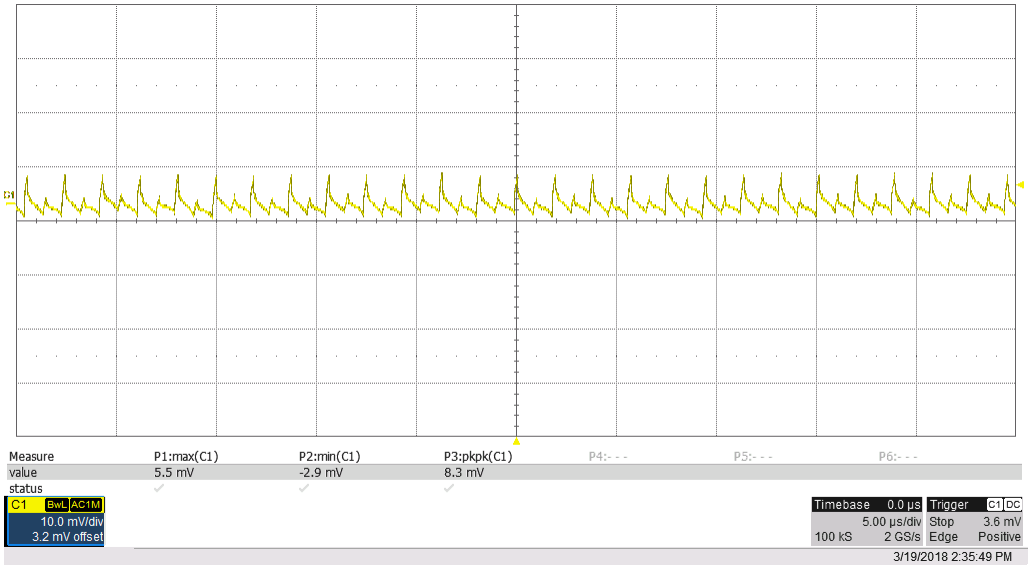


Figure 10. Output Voltage Ripple, V_{IN} = 12 V, 1-V V_{OUT} = 40-A Load

3.3 Bode Plot

The bode plot in Figure 11 shows the loop gain and phase margin of the converter when loaded to 1 V at 40 A.

V_{IN} = 12 V, bandwidth = 62.66 kHz, phase margin = 96.34 degrees.

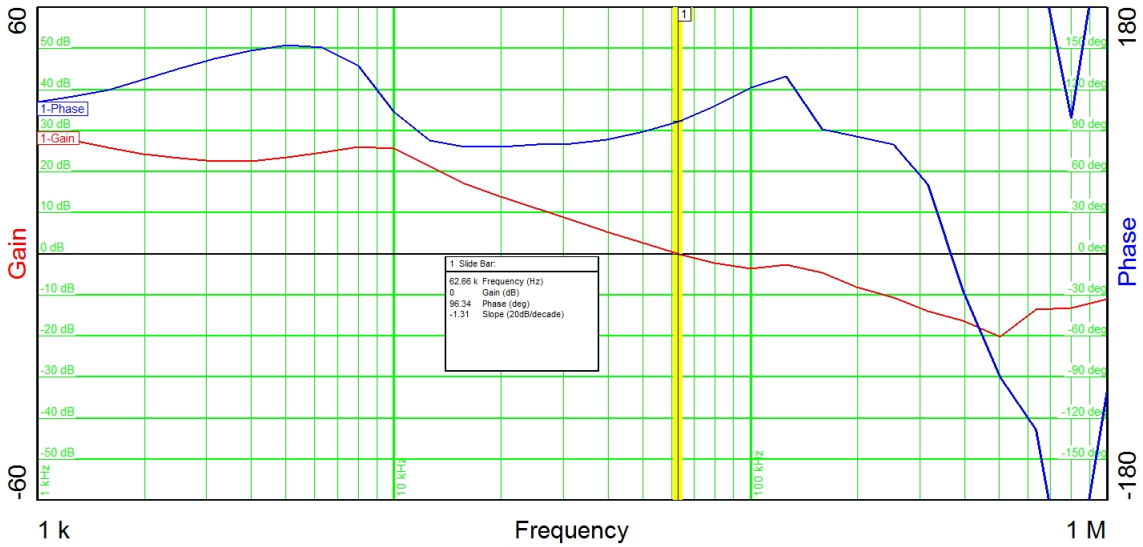


Figure 11. PMP21386 Bode Plot

3.4 Load Transients

Figure 12 shows the 1-V output voltage when the load current is stepped between 20 A and 40 A. An external static load of 20 A was used along with an onboard dynamic load for 20-A pulses.

V_{IN} = 12 V, rise 11.85 A/µs, fall 12.5 A/µs (10 mV/div, 10 A/div, 200 µs/div)

The dynamic load response measured at V_{OUT} was measured on the bottom side of the board using a coaxial connection:

- The maximum overshoot of 20.4 mV above nominal 1 V, or 2.04% above nominal
- The minimum undershoot of 23.9 mV below nominal 1 V, or 2.39% below nominal
- The waveform in Figure 12 is across a 20-mΩ resistor to ground on the dynamic load
- The *top* of this pulse of 400 mV divided by 20 mΩ corresponds to a 20-A pulse
- dI/dT of rise is 80% of this 20 A (as rise time is defined for “10% to 90%” or “80%”) divided by the rise time of 1.35 µs; or 20 A × 0.8 / 1.35 = 11.85 A /µs
- dI/dT of fall is 80% of this 20 A (as fall time is defined for “90% to 10%” or “80%”) divided by the fall time of 1.28 µs; or 20 A × 0.8 / 1.28 = –12.5 A/µs

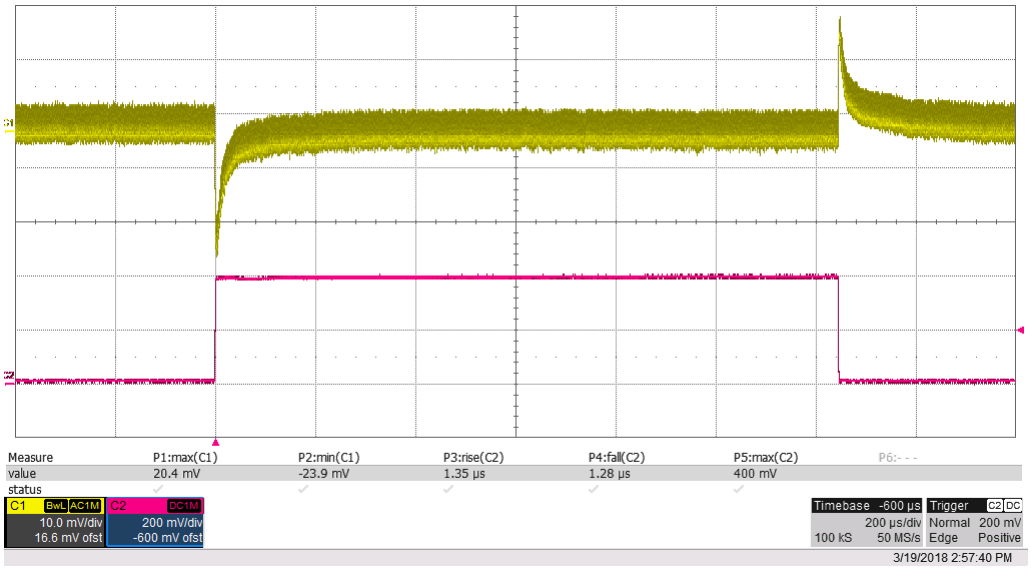


Figure 12. Output Voltage Transient, V_{IN} = 12 V, 1-V V_{OUT} From 20-mA to 40-mA Load

Figure 13 shows the 1-V output voltage when the load current is stepped between 20 A and 40 A. An external static load of 20 A was used along with an onboard dynamic load for 20-A pulses.

V_{IN} = 12 V, rise 0.342 A/µs, fall 0.337 A/µs (10 mV/div, 10 A/div, 200 µs/div)

Dynamic load response measured at V_{OUT} measured on bottom side of the board using coax connection:

- The maximum overshoot of 10.7 mV above nominal 1 V, or 1.07% above nominal
- The minimum undershoot of 10.9 mV below nominal 1 V, or 1.09% below nominal
- The waveform in Figure 13 is across a 20-mΩ resistor to ground on the dynamic load
- The *top* of this pulse of 400 mV divided by 20 mΩ corresponds to a 20-A pulse
- dI/dT of rise is 80% of this 20 A (as rise time is defined for “10% to 90%” or “80%”) divided by the rise time of 46.76 µs; or 20 A × 0.8 / 46.76 = 0.342 A /µs
- dI/dT of fall is 80% of this 20 A (as fall time is defined for “90% to 10%” or “80%”) divided by the fall time of 47.46 µs; or 20 A × 0.8 / 47.46 = –0.337 A/µs

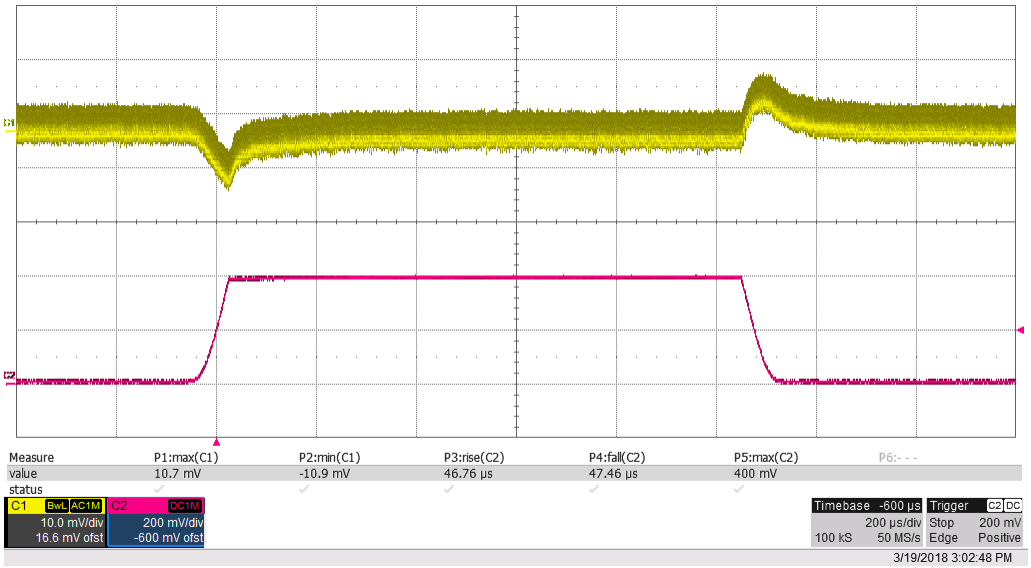


Figure 13. Output Voltage Transient, V_{IN} = 12 V, 1-V V_{OUT} From 20-mA to 40-mA Load

3.5 Start-up Sequence

Figure 14 shows the output voltage startup waveform after the application of 12 V in and the enable pin manually disconnected from GND with the 1-V output loaded to 0 A (200 mV/div, 1 ms/div).

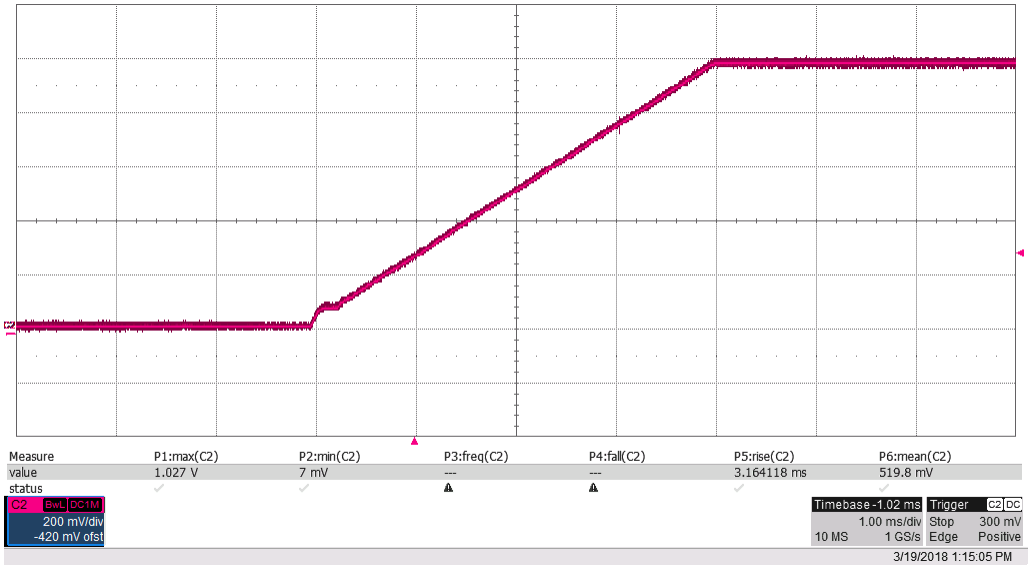


Figure 14. Output Voltage Startup Waveform, V_{IN} = 12 V, 1-V V_{OUT} = 0-mA Load

3.6 Additional Thermal Images

Figure 15 through Figure 19 show additional thermal image results.

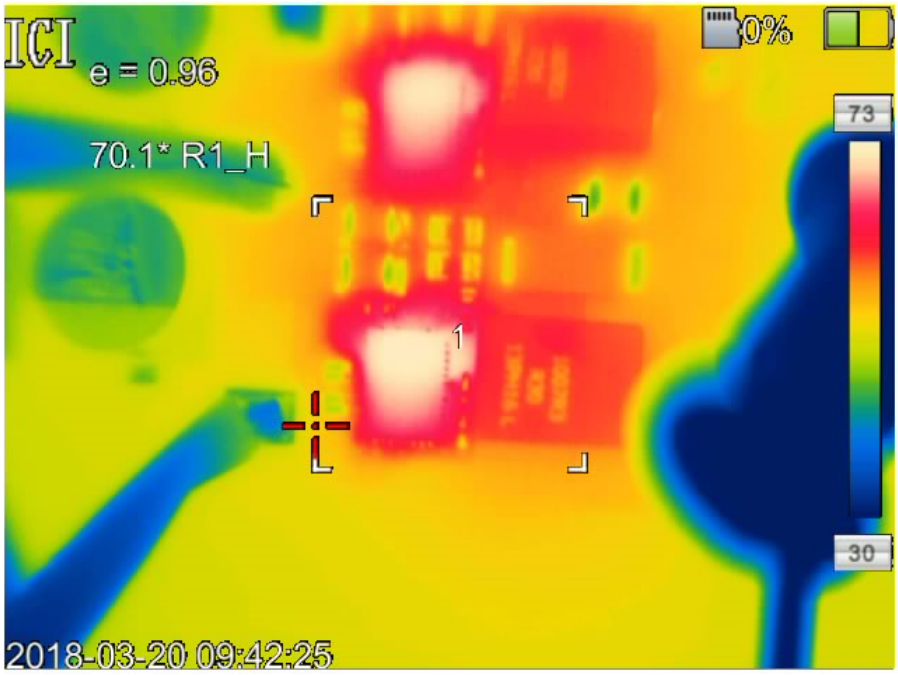


Figure 15. PMP21386 Thermal Image 1 V at 50 A, No Fan

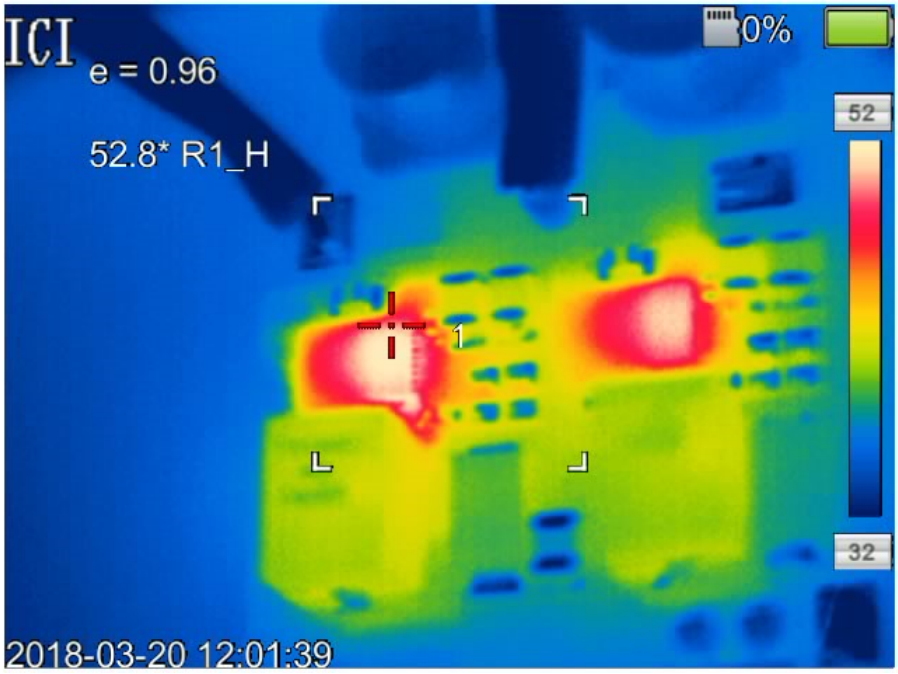


Figure 16. PMP21386 Thermal Image 1 V at 50 A, Small Fan

Figure 17. PMP21386 Thermal Image 1 V at 60 A, Small Fan

Figure 18. PMP21386 Thermal Image 1 V at 70 A, Small Fan

Figure 19. PMP21386 1 V at 75 A, Small Fan

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (https:www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265