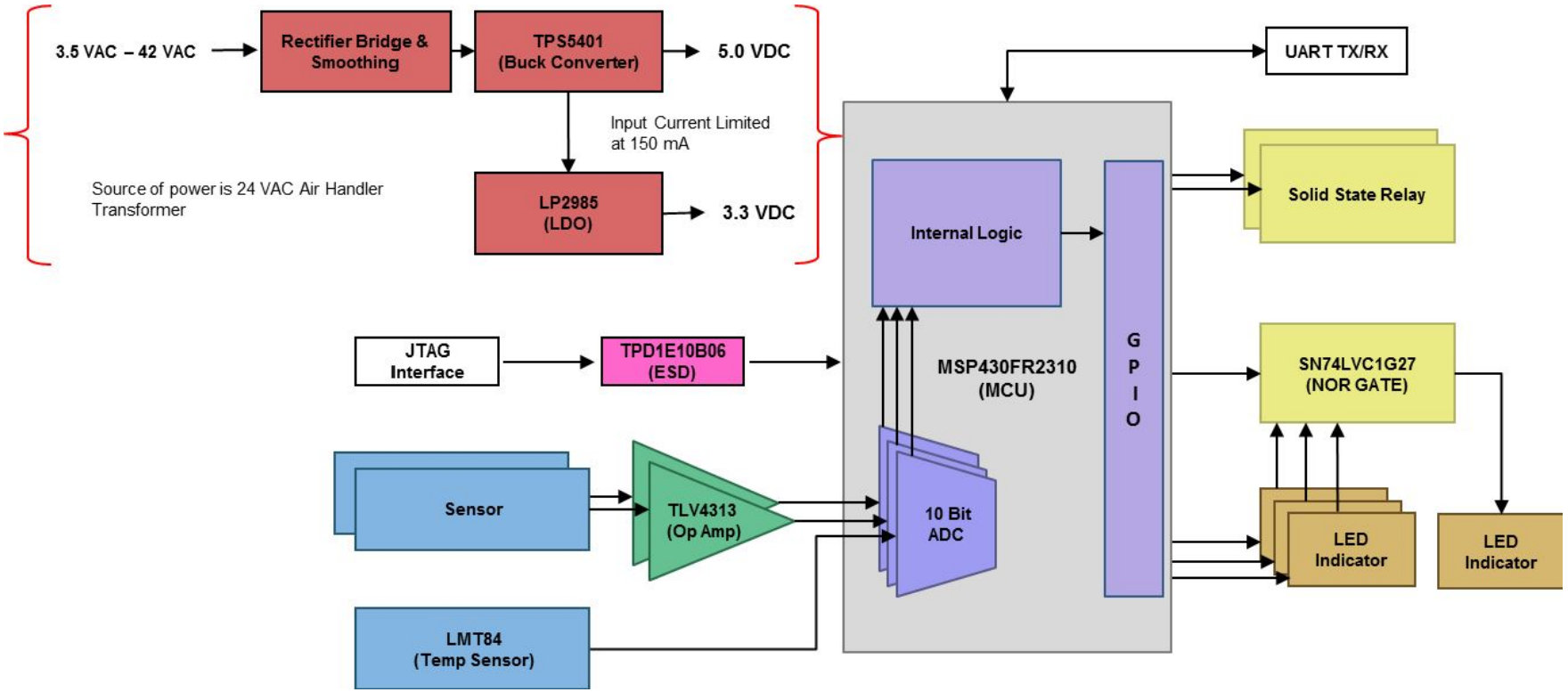

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TID #: TIDA-01070	Project Title: TIDA-01070	
Number: TIDA-01070 Rev: E1	Sheet Title:	
SVN Rev: Version control disabled	Assembly Variant: [No Variations]	Sheet: 1 of 6
Drawn By:	File: AA_System Block Diagram.SchDoc	Size: B
Engineer: Brian Dempsey	Contact: http://www.ti.com/support	

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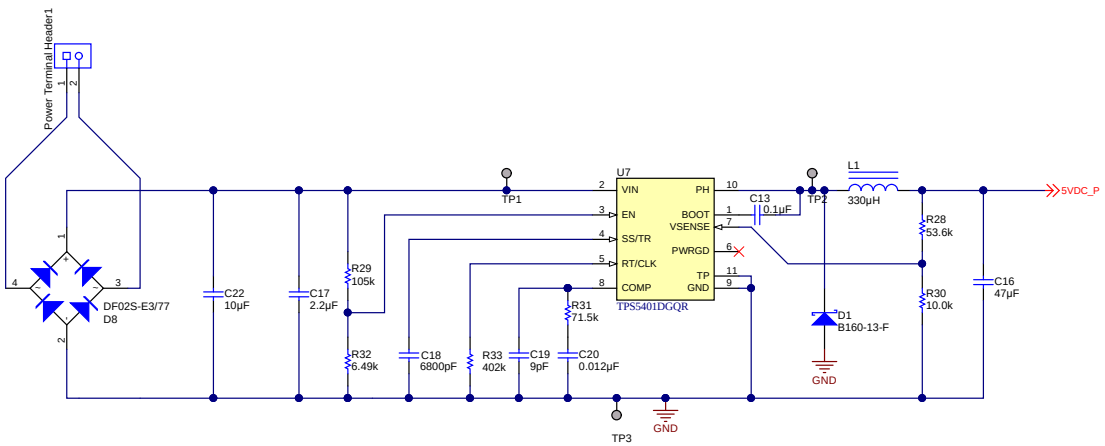

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Number: TIDA-01070 Rev: E1	Sheet Title:	
SVN Rev: Version control disabled	Assembly Variant: [No Variations]	Sheet: 2 of 6
Drawn By:	File: Ac to DC Converter.SchDoc	Size: B
Engineer: Brian Dempsey	Contact: http://www.ti.com/support	

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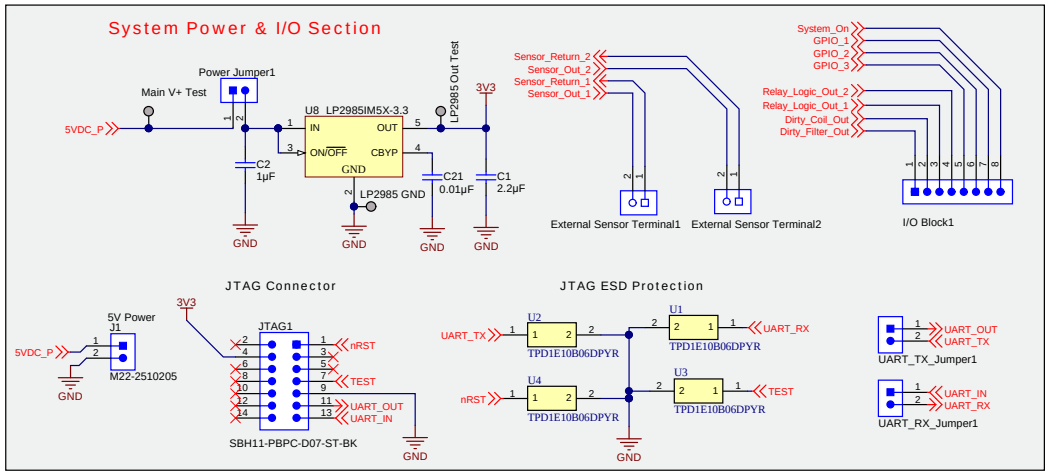
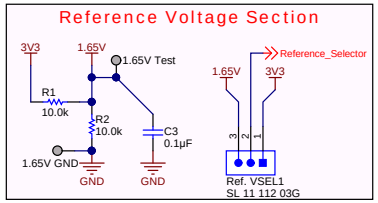
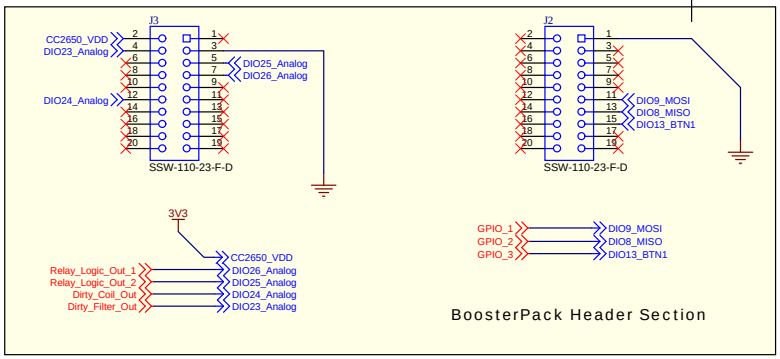




SSW-110-23-F-D's are 1700 mil. apart on centerline. Standard booster pack spacing required.



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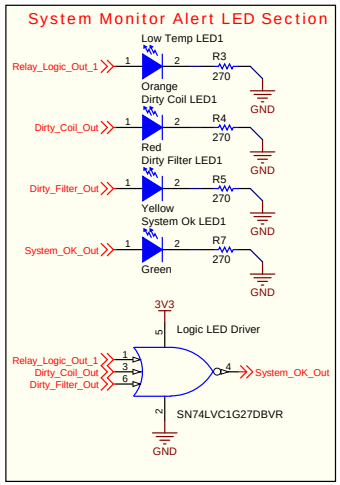
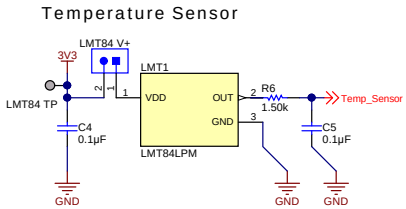
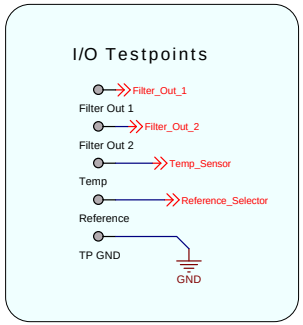
Number: TIDA-01070 Rev: E1	Sheet Title:	
SVN Rev: Version control disabled	Assembly Variant: [No Variations]	Sheet: 3 of 6
Drawn By:	File: Board_IO_Interface.SchDoc	Size: B
Engineer: Brian Dempsey	Contact: http://www.ti.com/support	







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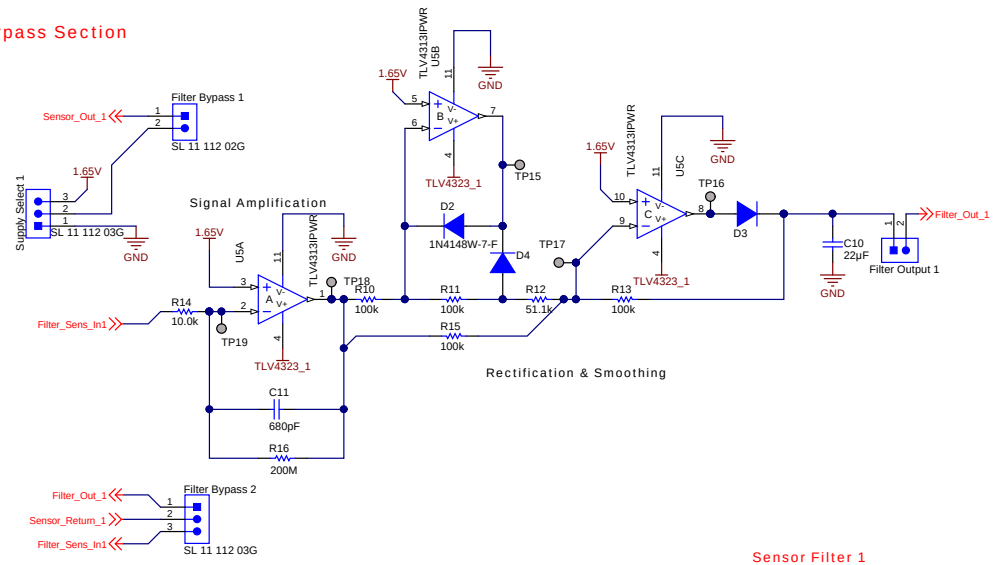
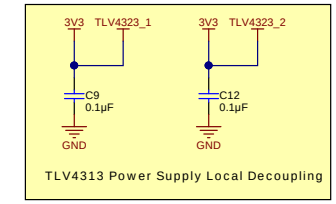
Number: TIDA-01070 Rev: E1	Sheet Title:		
SVN Rev: Version control disabled	Assembly Variant: [No Variations]	Sheet: 4 of 6	
Drawn By:	File: Internal_Processing.SchDoc	Size: B	
Engineer: Brian Dempsey	Contact: http://www.ti.com/support		

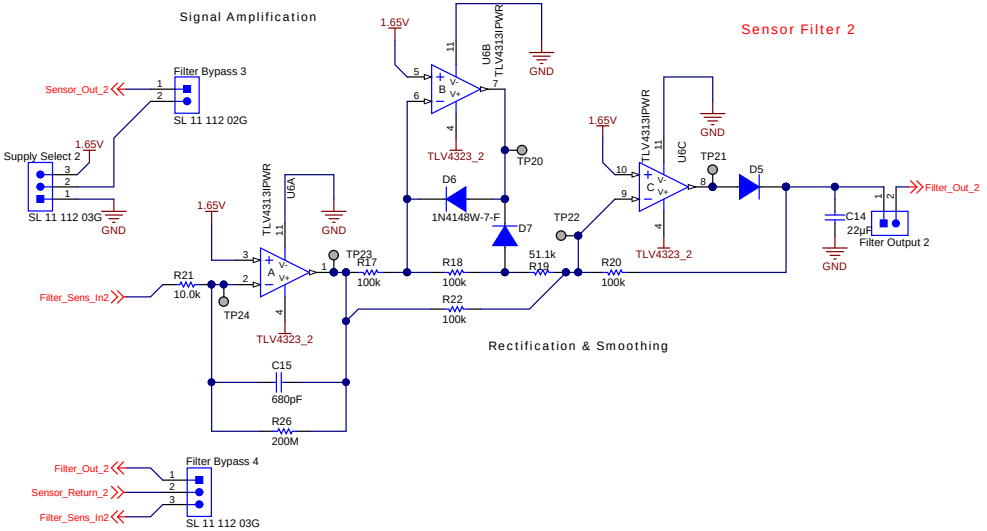
Peripheral Sensor Signal Conditioning/Bypass Section





Sensor Filter 1

Sensor Filter 2



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TID #: TIDA-01070	Project Title: TIDA-01070		
Number: TIDA-01070 Rev: E1	Sheet Title:		
SVN Rev: Version control disabled	Assembly Variant: [No Variations]	Sheet: 5 of 6	
Drawn By:	File: Sensor_Filtering.SchDoc	Size: B	
Engineer: Brian Dempsey	Contact: http://www.ti.com/support		

H1
SJ-5303 (CLEAR)

H2
SJ-5303 (CLEAR)

H3
SJ-5303 (CLEAR)

H4
SJ-5303 (CLEAR)

FID1 FID2 FID3

PCB Number: TIDA-01070
PCB Rev: E1

PCB LOGO
Texas Instruments

PCB LOGO
Pb-Free Symbol

PCB LOGO
FCC disclaimer

SH-1 SH-2 SH-3 SH-4 SH-5 SH-6 SH-7 SH-8

SH-9 SH-10 SH-11 SH-12 SH-13 SH-14

ZZ2
Assembly Note
These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ3
Assembly Note
These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ4
Assembly Note
These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

Orderable: EVM_orderable	Designed for: Public Release	Mod. Date: 9/15/2016
TID #: TIDA-01070	Project Title: TIDA-01070	
Number: TIDA-01070 Rev: E1	Sheet Title:	
SVN Rev: Version control disabled	Assembly Variant: [No Variations]	Sheet: 6 of 6
Drawn By:	File: TIDA-01070_EVM_Hardware.SchDoc	Size: B
Engineer: Brian Dempsey	Contact: http://www.ti.com/support	

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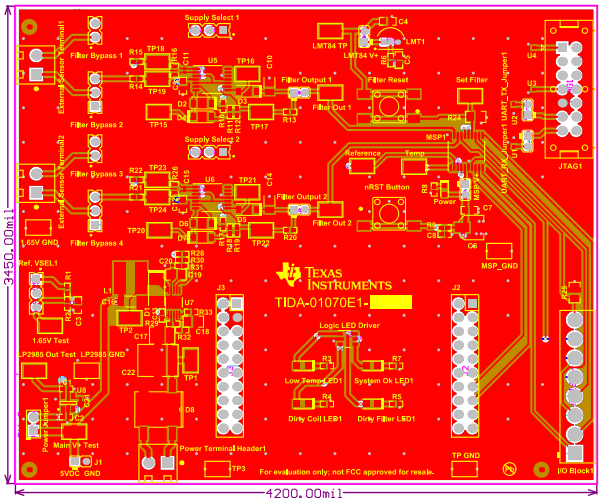
Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	Top Layer	Copper	1.42mil		
4	Dielectric1	FR-4 High TG	12.00mil	4.3	
5	Signal Layer 1	Copper	1.42mil		
6	Dielectric 2	FR-4 High TG	32.00mil	4.3	
7	Signal Layer 2	Copper	1.42mil		
8	Dielectric 3	FR-4 High TG	12.00mil	4.3	
9	Bottom Layer	Copper	1.42mil		
10	Bottom Solder	Solder Resist	0.40mil	3.5	
11	Bottom Overlay				

Z22 ■ These assemblies are ESD sensitive, ESD precautions shall be observed.
Z23 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
Z24 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.



1000.00mil

COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED
ASSEMBLY VARIANT: [No Variations]

DESIGN INFORMATION

MIN. TRACK WIDTH: 8 MIL
MIN. CLEARANCE: 8 mm
MIN. VIA PAD SIZE: 22 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[ ] FR-408 [X] FR-4 High Tg [ ] OTHER
THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [ ] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[X] MATTE [ ] SEMI-GLOSS
SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER
ARRAY/PANEL: [ ] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [X] V. SCORE
CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER
ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER

TEXAS INSTRUMENTS

PROJECT TITLE: TIDA-01070
DESIGNED FOR: Public Release
FILE NAME: TIDA-01070

ENGINEER: Brian Dempsey
LAYOUT BY: Krypton Solutions/RS
SCALE: 1.00
ALTIUM DESIGNER VERSION: 16.1.9.221

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