Designator
CSD95xxxPowerStages850mV_1-6.SchDoc

Designator
PMP21887_Control_850mV.SchDoc

Designator
CSD95xxxPowerStages850mV_7-12.SchDoc

Designator
PMP21887_Bias&Hardware.SchDoc

Designator
PMP21887_ASIC_CAPS.SchDoc

Designator
PMP21887_OutputCaps.SchDoc

Designator
InputCaps&PowerConns&DynamicLoad250A.SchDoc

Revision History

Rev	ECN #	Approved Date	Approved by	Notes
N/A	N/A	N/A	N/A	N/A

Orderable: ChangeMe in variant	Designed for:	Mod. Date: 4/3/2019
TID #: N/A	Project Title: Power for High Current ASIC with Dynamic Loads	
Number: PMP21887 Rev: A	Sheet Title:	
SVN Rev: Not in version control	Assembly Variant: 001	Sheet: 1 of 8
Drawn By:	File: PMP21887_CoverSheet.SchDoc	Size: B
Engineer: Josh Mandelcorn	Contact: http://www.ti.com/support	

TEXAS INSTRUMENTS
http://www.ti.com

POP R3 when Input current sense is not used

Margining range: 595mV to 1.105V

Set target Vcore 850mV with or without margining

If margining not used: R21 is zero ohms

In TPS536C7 pins 21-22-23-24 are Do Not Connect

TPS536C7RSL

Local & Remote main Vcore sense

Text String

Iin sense filter

pins 46 & 45 for input voltage sense and input current sense (if used)

If input current sense not used: omit caps to CSPIN and short CSPIN to VIN_CSNIN

PMBus address: 96d
12 + 0 config

PMBUS test conn

850mV boot up for main channel

External Analog Voltage for Control

With 1.5V Vcore will be 595mV (-30% margining)

With 850mV Vcore will be 850mV

With 0.2V Vcore will be 1.105V (+30% margining)

Jumper to disable main output

Orderable: ChangeMe in variant		Designed for:	Mod. Date: 4/3/2019
TID #: N/A		Project Title: Power for High Current ASIC with Dynamic Loads	
Number: PMP21887	Rev: A	Sheet Title:	
SVN Rev: Not in version control		Assembly Variant: 001	Sheet: 2 of 8
Drawn By:		File: PMP21887_Control_850mV.SchDoc	Size: B
Engineer: Josh Mandelcorn		Contact: http://www.ti.com/support	

One board to be built with the 100nH inductors running at 500kHz
One board to be built with 150mH inductors running at 350kHz

SLA40476B-150L

U110 CSD95480RWJ

VINC
C111 1210 22uF 16V
C112 1210 22uF 16V
C113 1210 22uF 16V
C114 0603 25V 2.2µF
C110 4700pF
PGND
5V-DRV is external 5V
5V-DRV
R112 2.2
C116 2.2uF
C117 2.2uF
R113 0
R114 110k
APWM1
R115 0
ACSP1
R116 0
Vref1v5
C118 0.1uF
ATAO
R117 0
C119 1000pF
R118 1.0
C101 0.1uF
VIN VIN VIN VIN VIN VIN
PVDD
VDD
EN/FCCM
LSET
PWM
IOUT
REFIN
TAO/FAULT
BOOTR
BOOT
VSW VSW VSW VSW VSW VSW VSW VSW VSW VSW VSW VSW
VOS
NC NC NC
AGND
PGND PGND PGND PGND PGND PGND PGND PGND PGND PGND PGND PGND
L110 150nH
L111 100nH 74431012010A
Vcore- Phase-1
Vcore
0603 R110 2.2
0603 R111 2.2
Only one of the 2 inductors populated
0603 C115 50V 1000pF

SLA40476B-150L

U120 CSD95480RWJ

VINC
C121 1210 22uF 16V
C122 1210 22uF 16V
C123 1210 22uF 16V
C124 0603 25V 2.2µF
C120 4700pF
PGND
5V-DRV is external 5V
5V-DRV
R122 2.2
C126 2.2uF
C127 2.2uF
R123 0
R124 110k
APWM2
R125 0
ACSP2
R126 0
Vref1v5
C128 0.1uF
ATAO
R127 0
C129 1000pF
R128 1.0
C102 0.1uF
VIN VIN VIN VIN VIN VIN
PVDD
VDD
EN/FCCM
LSET
PWM
IOUT
REFIN
TAO/FAULT
BOOTR
BOOT
VSW VSW VSW VSW VSW VSW VSW VSW VSW VSW VSW VSW
VOS
NC NC NC
AGND
PGND PGND PGND PGND PGND PGND PGND PGND PGND PGND PGND PGND
L120 150nH
L121 100nH 74431012010A
Vcore- Phase-2
Vcore
0603 R120 2.2
0603 R121 2.2
Only one of the 2 inductors populated
0603 C125 50V 1000pF

SLA40476B-150L

U130 CSD95480RWJ

VINC
C131 1210 22uF 16V
C132 1210 22uF 16V
C133 1210 22uF 16V
C134 0603 25V 2.2µF
C130 4700pF
PGND
5V-DRV is external 5V
5V-DRV
R132 2.2
C136 2.2uF
C137 2.2uF
R133 0
R134 110k
APWM3
R135 0
ACSP3
R136 0
Vref1v5
C138 0.1uF
ATAO
R137 0
C139 1000pF
R138 1.0
C103 0.1uF
VIN VIN VIN VIN VIN VIN
PVDD
VDD
EN/FCCM
LSET
PWM
IOUT
REFIN
TAO/FAULT
BOOTR
BOOT
VSW VSW VSW VSW VSW VSW VSW VSW VSW VSW VSW VSW
VOS
NC NC NC
AGND
PGND PGND PGND PGND PGND PGND PGND PGND PGND PGND PGND PGND
L130 150nH
L131 100nH 74431012010A
Vcore- Phase-3
Vcore
0603 R130 2.2
0603 R131 2.2
Only one of the 2 inductors populated
0603 C135 50V 1000pF

SLA40476B-150L

U140 CSD95480RWJ

VINC
C141 1210 22uF 16V
C142 1210 22uF 16V
C143 1210 22uF 16V
C144 0603 25V 2.2µF
C140 4700pF
PGND
5V-DRV is external 5V
5V-DRV
R142 2.2
C146 2.2uF
C147 2.2uF
R143 0
R144 110k
APWM4
R145 0
ACSP4
R146 0
Vref1v5
C148 0.1uF
ATAO
R147 0
C149 1000pF
R148 1.0
C104 0.1uF
VIN VIN VIN VIN VIN VIN
PVDD
VDD
EN/FCCM
LSET
PWM
IOUT
REFIN
TAO/FAULT
BOOTR
BOOT
VSW VSW VSW VSW VSW VSW VSW VSW VSW VSW VSW VSW
VOS
NC NC NC
AGND
PGND PGND PGND PGND PGND PGND PGND PGND PGND PGND PGND PGND
L140 150nH
L141 100nH 74431012010A
Vcore- Phase-4
Vcore
0603 R140 2.2
0603 R141 2.2
Only one of the 2 inductors populated
0603 C145 50V 1000pF

SLA40476B-150L

U150 CSD95480RWJ

VINC
C151 1210 22uF 16V
C152 1210 22uF 16V
C153 1210 22uF 16V
C154 0603 25V 2.2µF
C150 4700pF
PGND
5V-DRV is external 5V
5V-DRV
R152 2.2
C156 2.2uF
C157 2.2uF
R153 0
R154 110k
APWM5
R155 0
ACSP5
R156 0
Vref1v5
C158 0.1uF
ATAO
R157 0
C159 1000pF
R158 1.0
C105 0.1uF
VIN VIN VIN VIN VIN VIN
PVDD
VDD
EN/FCCM
LSET
PWM
IOUT
REFIN
TAO/FAULT
BOOTR
BOOT
VSW VSW VSW VSW VSW VSW VSW VSW VSW VSW VSW VSW
VOS
NC NC NC
AGND
PGND PGND PGND PGND PGND PGND PGND PGND PGND PGND PGND PGND
L150 150nH
L151 100nH 74431012010A
Vcore- Phase-5
Vcore
0603 R150 2.2
0603 R151 2.2
Only one of the 2 inductors populated
0603 C155 50V 1000pF

SLA40476B-150L

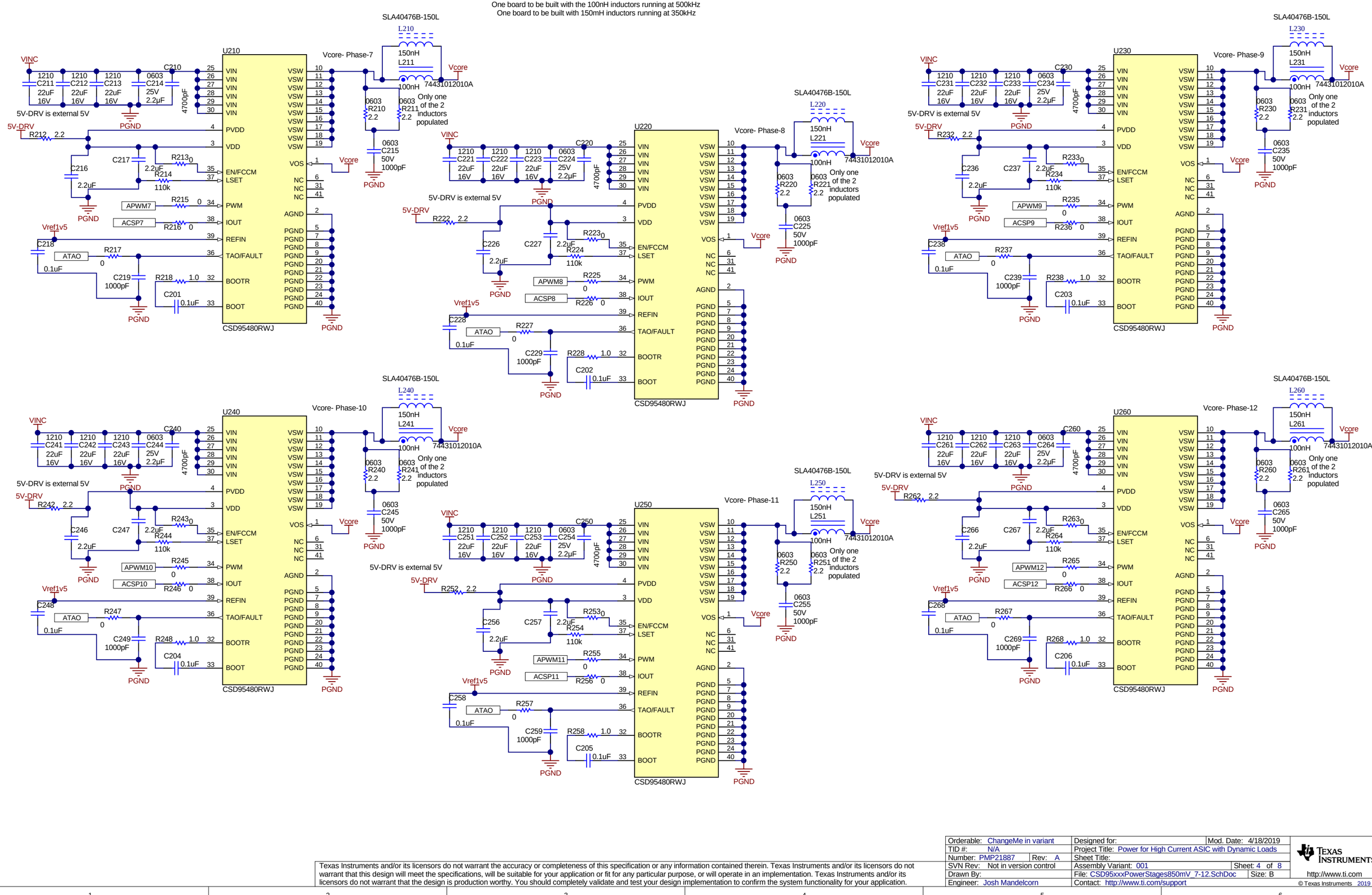
U160 CSD95480RWJ

VINC
C161 1210 22uF 16V
C162 1210 22uF 16V
C163 1210 22uF 16V
C164 0603 25V 2.2µF
C160 4700pF
PGND
5V-DRV is external 5V
5V-DRV
R162 2.2
C166 2.2uF
C167 2.2uF
R163 0
R164 110k
APWM6
R165 0
ACSP6
R166 0
Vref1v5
C168 0.1uF
ATAO
R167 0
C169 1000pF
R168 1.0
C106 0.1uF
VIN VIN VIN VIN VIN VIN
PVDD
VDD
EN/FCCM
LSET
PWM
IOUT
REFIN
TAO/FAULT
BOOTR
BOOT
VSW VSW VSW VSW VSW VSW VSW VSW VSW VSW VSW VSW
VOS
NC NC NC
AGND
PGND PGND PGND PGND PGND PGND PGND PGND PGND PGND PGND PGND
L160 150nH
L161 100nH 74431012010A
Vcore- Phase-6
Vcore
0603 R160 2.2
0603 R161 2.2
Only one of the 2 inductors populated
0603 C165 50V 1000pF

Orderable: ChangeMe in variant		Designed for:	Mod. Date: 4/18/2019
TID #: N/A		Project Title: Power for High Current ASIC with Dynamic Loads	
Number: PMP21887	Rev: A	Sheet Title:	
SVN Rev: Not in version control		Assembly Variant: 001	Sheet: 3 of 8
Drawn By:		File: CSD95xxxPowerStages850mV_1-6.SchDoc	Size: B
Engineer: Josh Mandelcorn		Contact: http://www.ti.com/support	

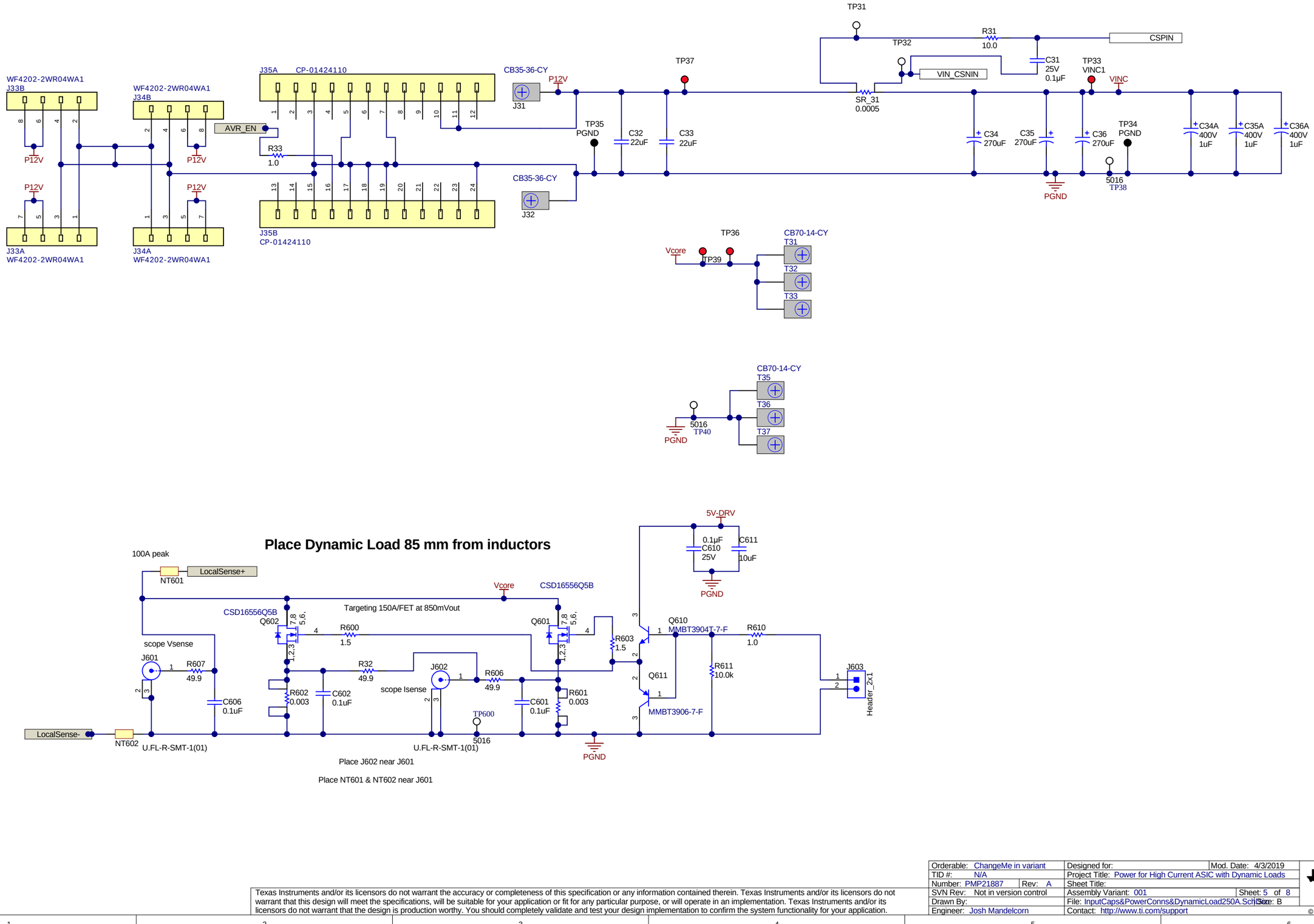
Texas Instruments
http://www.ti.com

One board to be built with the 100nH inductors running at 500kHz
One board to be built with 150mH inductors running at 350kHz



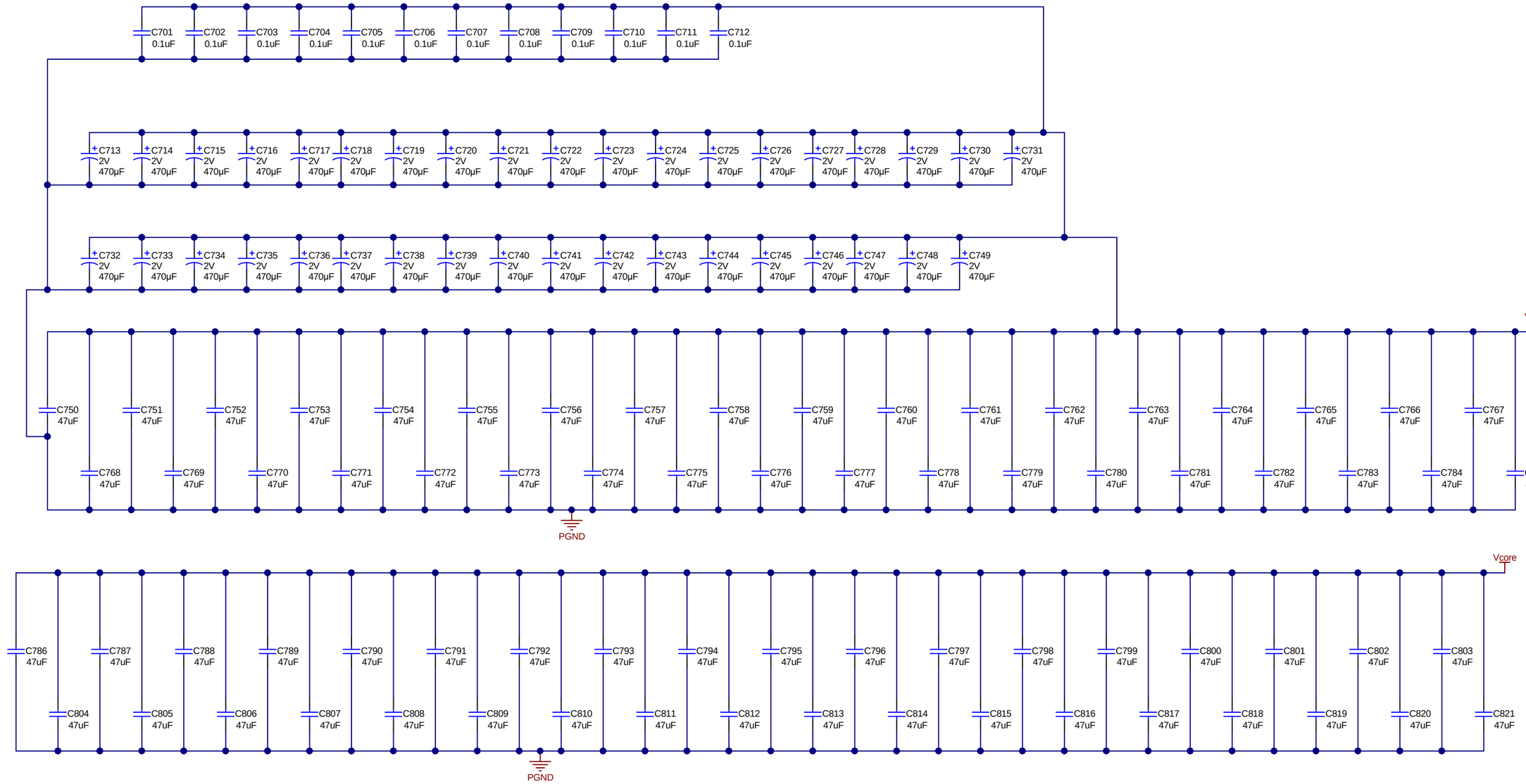
Orderable: ChangeMe in variant		Designed for:	Mod. Date: 4/18/2019
TID #: N/A		Project Title: Power for High Current ASIC with Dynamic Loads	
Number: PMP21887	Rev: A	Sheet Title:	
SVN Rev: Not in version control		Assembly Variant: 001	Sheet: 4 of 8
Drawn By:		File: CSD95xxxPowerStages850mV_7-12.SchDoc	Size: B
Engineer: Josh Mandelcorn		Contact: http://www.ti.com/support	

http://www.ti.com



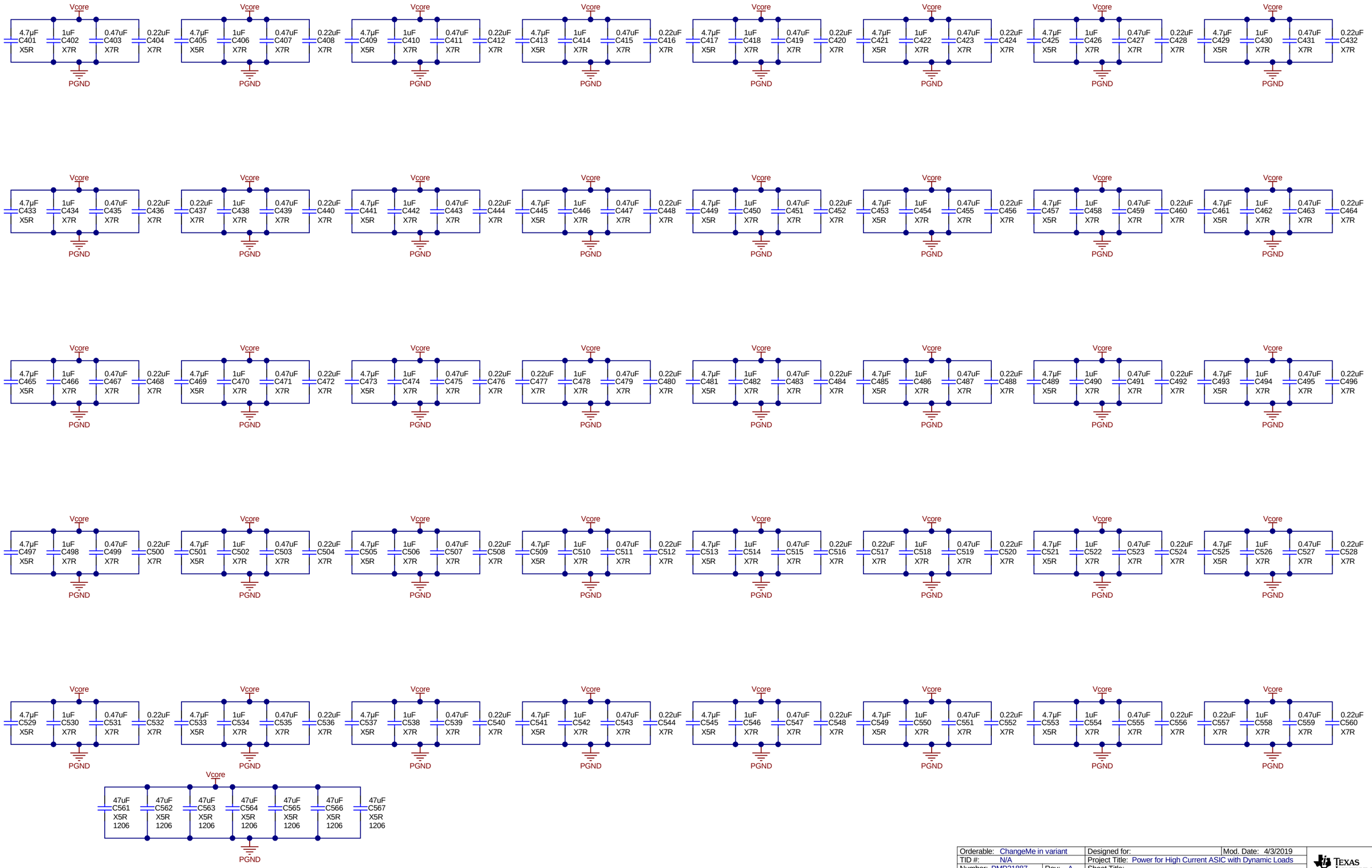
Orderable: ChangeMe in variant		Designed for:	Mod. Date: 4/3/2019
TID #: N/A		Project Title: Power for High Current ASIC with Dynamic Loads	
Number: PMP21887	Rev: A	Sheet Title:	
SVN Rev: Not in version control		Assembly Variant: 001	Sheet: 5 of 8
Drawn By:		File: InputCaps&PowerConns&DynamicLoad250A.SchDoc	Size: B
Engineer: Josh Mandelcorn		Contact: http://www.ti.com/support	

TEXAS INSTRUMENTS
http://www.ti.com



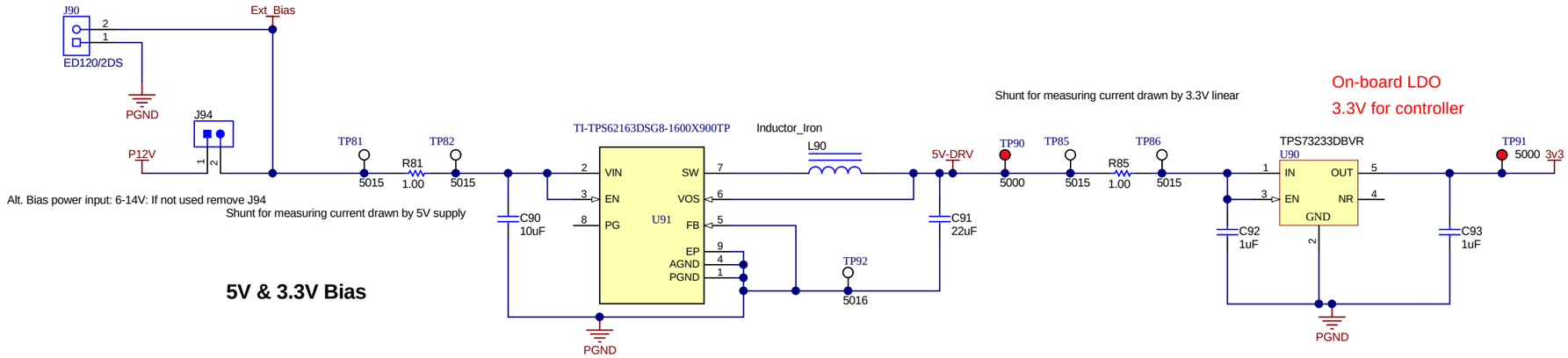
Orderable: ChangeMe in variant	Designed for:	Mod. Date: 4/3/2019
TID #: N/A	Project Title: Power for High Current ASIC with Dynamic Loads	
Number: PMP21887 Rev: A	Sheet Title:	
SVN Rev: Not in version control	Assembly Variant: 001	Sheet: 6 of 8
Drawn By:	File: PMP21887_OutputCaps.SchDoc	Size: B
Engineer: Josh Mandelcorn	Contact: http://www.ti.com/support	

Texas Instruments
http://www.ti.com



Orderable: ChangeMe in variant	Designed for:	Mod. Date: 4/3/2019
TID #: N/A	Project Title: Power for High Current ASIC with Dynamic Loads	
Number: PMP21887 Rev: A	Sheet Title:	
SVN Rev: Not in version control	Assembly Variant: 001	Sheet: 7 of 8
Drawn By:	File: PMP21887_ASIC_CAPS.SchDoc	Size: B
Engineer: Josh Mandelcorn	Contact: http://www.ti.com/support	

TEXAS INSTRUMENTS
http://www.ti.com



5V & 3.3V Bias

LBL1

PCB Label

THT-14-423-10

Size: 0.65" x 0.20 "

ZZ1

Label Assembly Note

This Assembly Note is for PCB labels only

ZZ2

Assembly Note

These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ3

Assembly Note

These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ4

Assembly Note

These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

CE Mark

PCB LOGO
FCC disclaimer

PCB LOGO
WEEE logo

DNP FID1 DNP FID2 DNP FID3 FID4 FID5 FID6

PCB Number: PMP21887
PCB Rev: A

PCB LOGO
Texas Instruments

H1 NY PMS 440 0025 PH
H2 NY PMS 440 0025 PH
H3 NY PMS 440 0025 PH
H4 NY PMS 440 0025 PH

H5 1902C
H6 1902C
H7 1902C
H8 1902C

Variant/Label Table	
Variant	Label Text
001	ChangeMe!
002	ChangeMe!

Orderable: ChangeMe in variant		Designed for:	Mod. Date: 4/3/2019
TID #: N/A		Project Title: Power for High Current ASIC with Dynamic Loads	
Number: PMP21887	Rev: A	Sheet Title:	
SVN Rev: Not in version control		Assembly Variant: 001	Sheet: 8 of 8
Drawn By:		File: PMP21887_Bias&Hardware.SchDoc	Size: B
Engineer: Josh Mandelcorn		Contact: http://www.ti.com/support	

Texas Instruments
http://www.ti.com

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265