

Simultaneous-Switching Performance of TI Logic Devices

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ABSTRACT

Simultaneous-switching noise can generate and propagate glitches in electronic systems. Therefore, system designers are faced with challenges to minimize simultaneous-switching noise, while increasing switching speed and improving signal quality. This report presents the performance of different TI logic devices under various simultaneous-switching conditions. Factors such as the number of bits switching, temperature, supply voltage, package type, and output loads play a role in the amount of noise generated at the output of a device during simultaneous switching. A discussion of the effects of these factors, along with concerns regarding simultaneous-switching noise and suggestions for improvement of simultaneous-switching performance, is provided. System designers concerned about implications of simultaneous-switching noise can use this report to choose the right Texas Instruments logic solution for their application.

Keywords: simultaneous switching, V_{OHV} , V_{OHP} , V_{OLV} , V_{OLP} , ground bounce, V_{CC} bounce, AUC

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1 Introduction

Switching multiple output drivers simultaneously on the same device is called simultaneous switching. The elements in the electrical path from the ground or power pads of the integrated circuit (IC) to the ground or power planes on the printed circuit board (PCB) behave as inductances with negligible resistive components.[1] In Figure 1, the inductive elements to the power rail are shown collectively as L_{power} , and the inductive elements to the ground rail are shown collectively as L_{GND} , while L_{input} and L_{output} represent the inductive elements at the input and output, respectively.

CMOS devices operate by charging and discharging a capacitive load (see Figure 1a). When the output changes state from high to low or low to high, a current flows in the output loop. This current determines the output edge rate (see Equation 1).

$$\frac{dV_O}{dt} = \frac{-i(t)}{C_L} \quad (1)$$

Figure 1b shows a CMOS inverter. When a high (H) signal is applied at the input, the upper p-channel transistor is off and the lower n-channel transistor is on. The output is pulled to ground (low) through the conducting n-channel. Similarly, when a low (L) signal is applied at the input, the n-channel is off and the p-channel is on, pulling the output high through the conducting p-channel. When changing states from high to low, the p-channel begins to turn off and the n-channel begins to turn on. In the threshold region ($V_{IL} < V_{\text{input}} < V_{IH}$), both these transistors are partially ON, causing a through current, I_{CC} , to flow from V_{CC} to GND. A similar situation exists when the output switches from L to H.

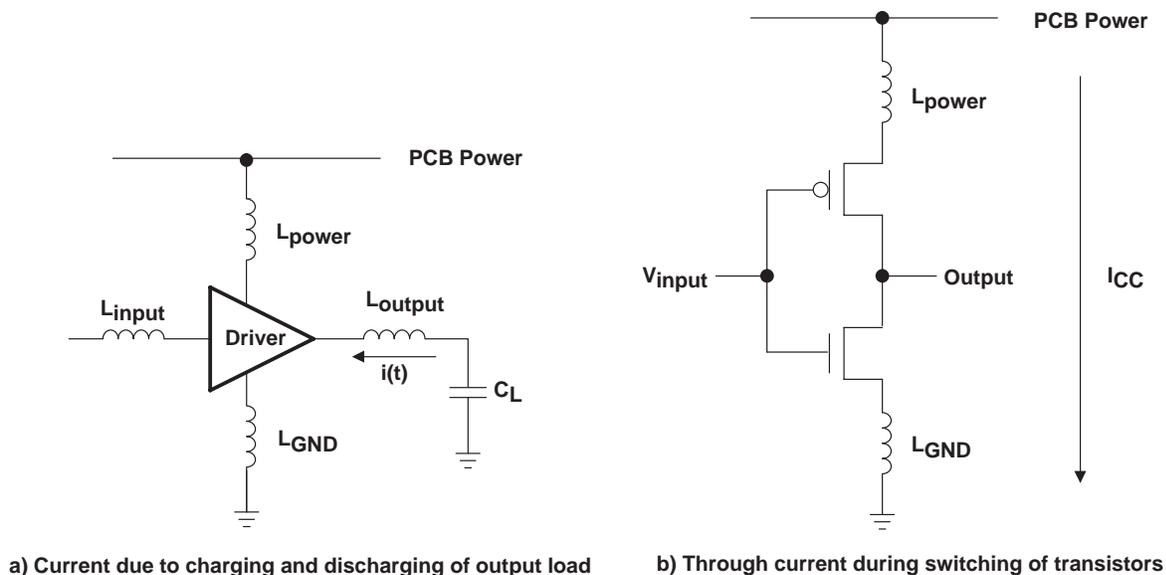


Figure 1. Currents That Lead to Simultaneous-Switching Noise

These currents interact with the inductances in their path to generate ground and V_{CC} bounce (see Figure 2). When the output changes from H to L, the output capacitor discharges to ground through the n-channel pulldown, generating a current $i(t)$ in the output loop. This current interacts with the ground inductance (L_{GND}) to generate ground bounce V_{GND} (see Equation 2). Similarly, when the output changes states from low to high, the current induces a voltage drop on the power rail (see Equation 4).

$$V_{GND} = \left(\frac{L_{GND}}{N} \right) \left(\frac{di}{dt} \right) \quad (2)$$

From Equations (1) and (2): $V_{GND} = - \left(\frac{L_{GND} \times C_L}{N} \right) \left(\frac{d^2 V_O}{dt^2} \right) \quad (3)$

$$V_{power} = \left(\frac{L_{power}}{N} \right) \left(\frac{di}{dt} \right) \quad (4)$$

From Equations (1) and (4): $V_{power} = - \left(\frac{L_{power} \times C_L}{N} \right) \left(\frac{d^2 V_O}{dt^2} \right) \quad (5)$

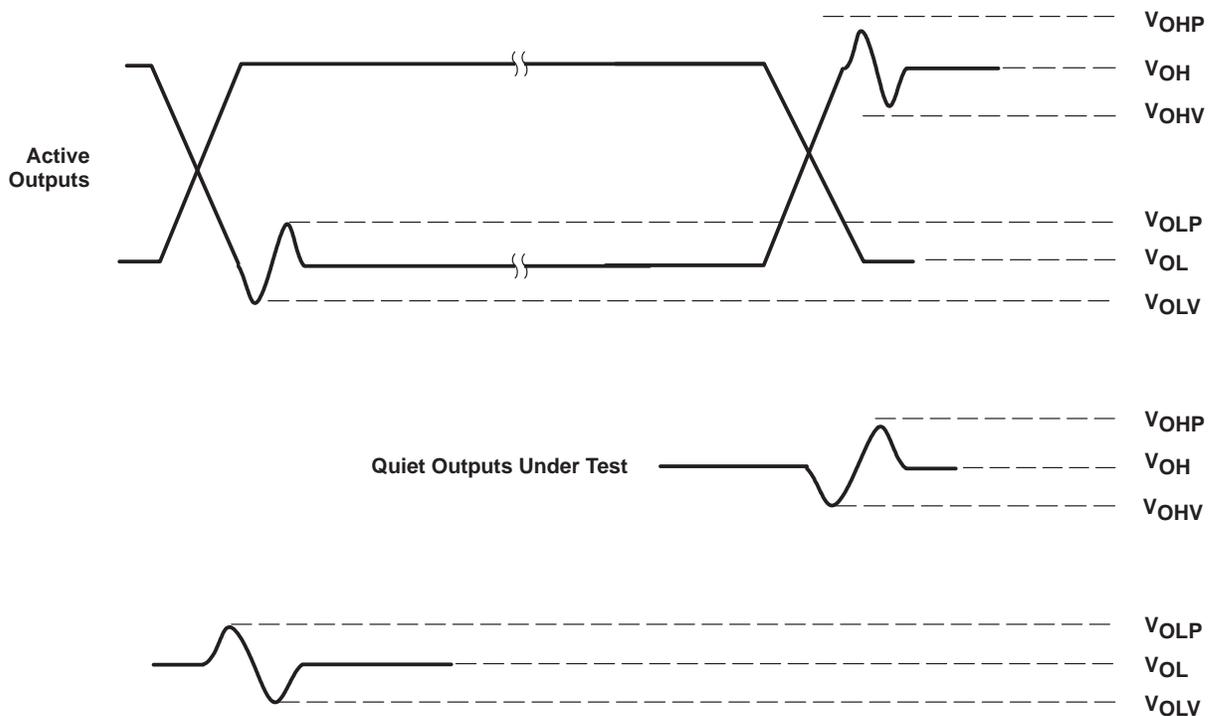


Figure 2. Generation of Simultaneous-Switching Noise

Whatever applies to ground bounce also applies to V_{CC} bounce in a similar manner. Hence, through the remainder of this application report, only the effects of ground bounce are discussed.

For the simultaneous-switching measurement procedure, one input is connected to a fixed low or high state while a specified number of other inputs are switched simultaneously. The outputs of these drivers react to the changes in the corresponding inputs after a certain delay, while the nonswitched output maintains a constant low (or high) state.

Figure 2 also sets out the parameters and definitions of significance for this measurement procedure. Points on the curves are defined as:

- V_{OHP} (voltage output high peak): V_{CC} bounce: peak output-voltage value during a static high at the nonswitched output or during a low-to-high transition at a switching output.
- V_{OHV} (voltage output high valley): V_{CC} bounce: minimum output-voltage value during a static high at the nonswitched output or during a low-to-high transition at a switching output.
- V_{OLP} (voltage output low peak): Ground bounce: peak output-voltage value during a static low at the nonswitched output or during a high-to-low transition at a switching output.
- V_{OLV} (voltage output low valley): Ground bounce: minimum output-voltage value during a static low at the nonswitched output or during a high-to-low transition at a switching output.

V_{OLV} and V_{OHP} could cause damage if the voltage spike goes well beyond the rails and/or lasts for a long period of time. V_{OLP} and V_{OHV} are critical because, in the worst case, they could exceed the switching thresholds (V_{IH} and V_{IL}) of a subsequent receiver.[2]

2 Simultaneous-Switching Considerations

From Equations 3 and 5, output load, output edge rate, and package inductance affects ground bounce. We have investigated how these and other factors affect ground bounce. In our evaluation, the '244 function (noninverting buffer/driver with 3-state outputs) is used as an example.

2.1 Effect of the Number of Bits Switching

As more bits are switched simultaneously, more current flows in the output loop. From Equations 2 and 4, ground bounce is expected to increase in proportion to the number of bits switching. This relationship holds true until the device begins to limit the transient current flow. Figure 3 shows the increase in ground bounce as the number of simultaneously switching bits increases.

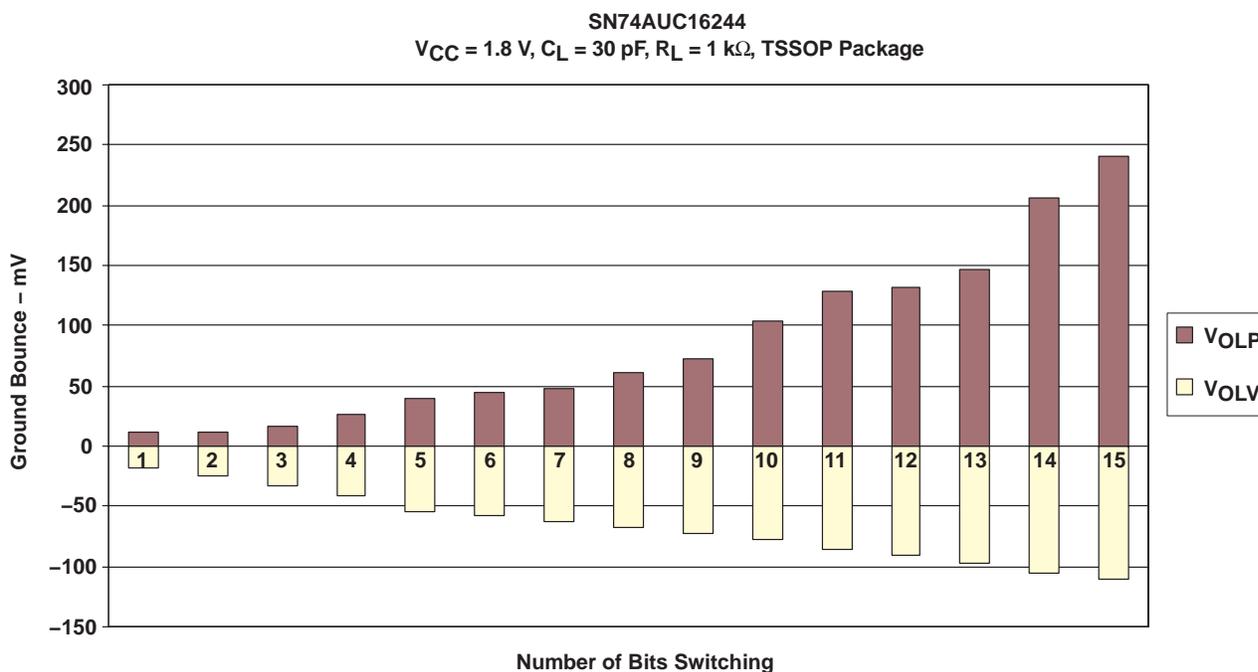


Figure 3. Ground Bounce vs Number of Bits Switching

2.2 Effect of Temperature

As CMOS devices operate at lower temperatures, they become intrinsically faster. This is because electron and hole mobility increases with decreasing temperature. This results in faster edges, causing simultaneous-switching noise to increase, with a decrease in temperature.[1] Figure 4 shows the effect of temperature on the amount of ground bounce generated on a quiet output held low when the other 15 outputs switch from H to L. Ground bounce increases as temperature decreases.

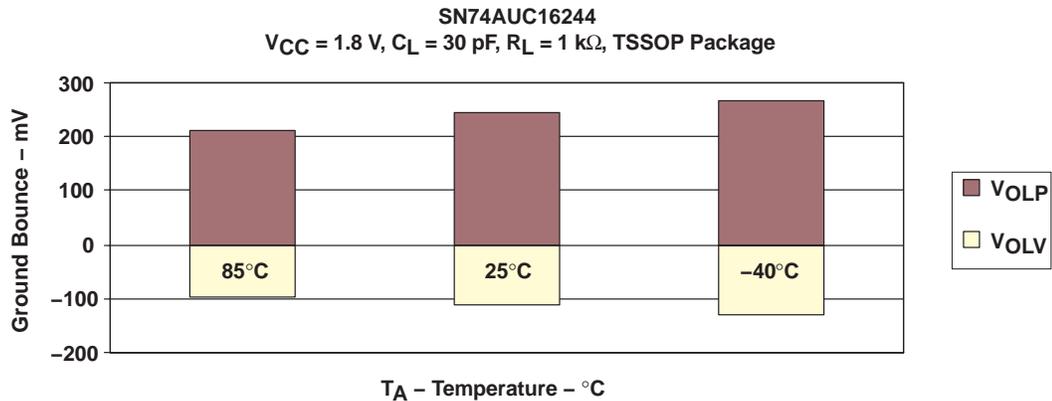


Figure 4. Ground Bounce vs Temperature

2.3 Effect of Power-Supply Voltage

Equations 3 and 5 show that the amount of noise generated is directly proportional to the output voltage swing (dV_O/dt). Hence, as the supply voltage increases, so do the output voltage swing (dV_O) and the ground bounce. The quiescent supply current also increases with a rise in the supply voltage, contributing further to greater ground bounce. Figure 5 shows the effects of supply voltage on ground bounce.

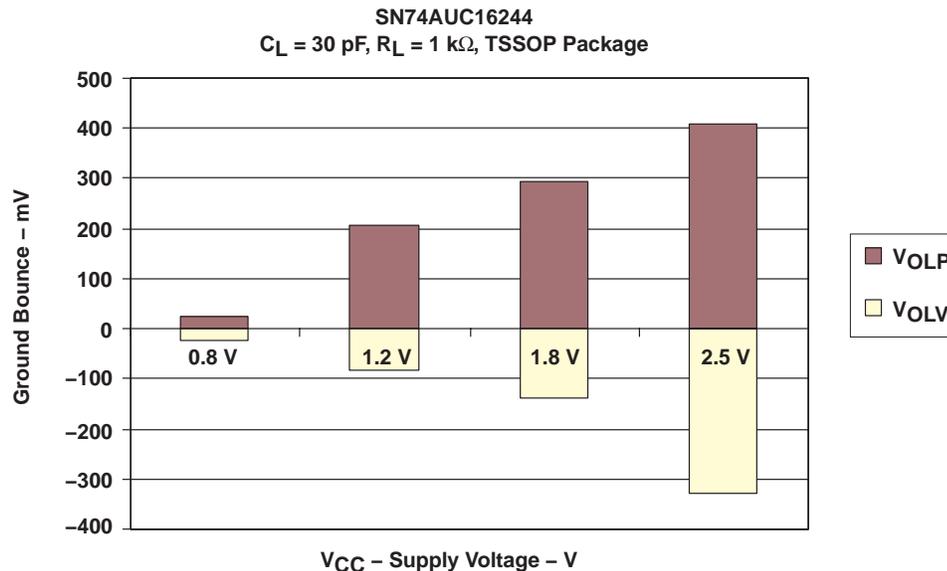


Figure 5. Ground Bounce vs Supply Voltage

CMOS outputs have a greater output voltage swing compared to TTL outputs. Because dV_O/dt is higher for CMOS devices than for TTL devices, CMOS devices generate more simultaneous-switching noise compared to similar TTL devices.

2.4 Effect of Lumped and Distributed Loading

TI logic data sheets usually specify ac (switching) parameters using a lumped capacitive load at the output. Typically, such lumped capacitances at the output in a system environment do not occur. Instead, as shown in Figure 6, a driver output sees a short transmission line as a lumped capacitance some distance away, whereas longer transmission lines appear as distributed capacitive loads.[1] Equation 6 gives a rule of thumb for short and long transmission lines.

$$l_{short} \leq \frac{t_r}{2t_{pd}}, l_{long} > \frac{t_r}{2t_{pd}} \quad (6)$$

Where:

t_r = rise time of the output signal

t_{pd} = flight time through the transmission line[3]

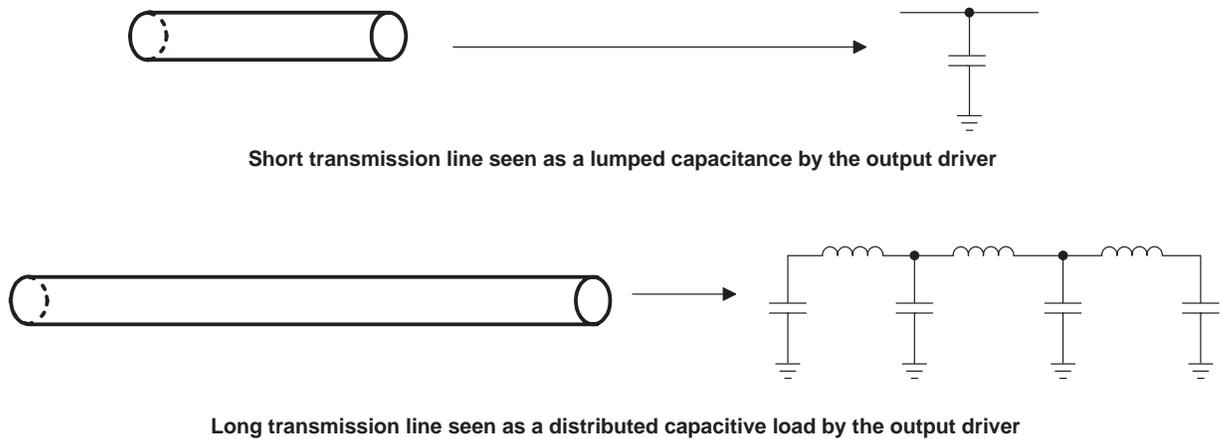
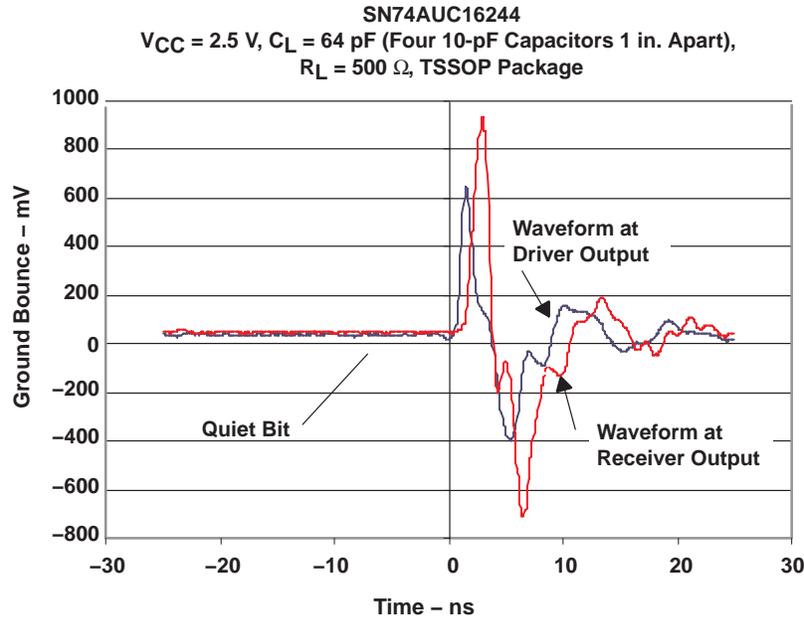


Figure 6. Short and Long Transmission Lines

To simulate the system environment, ground bounce was measured by placing lumped and distributed capacitances at a distance away from the output. The main effect of placement of these capacitances at a distance away from the driving device is reduction of ground bounce at the output of the driver. However, the magnitude of ground bounce at the input of the receiver is not reduced (see Figure 7).



**Figure 7. Ground Bounce at the Driver Output and Receiver Input
With a Distributed Capacitive Load**

Ground bounce would decrease if additional lumped capacitances were added at the device output. This would seem to invalidate Equations 3 and 5, which indicate that ground bounce is directly proportional to the output capacitive load. However, these equations also indicate that ground bounce is proportional to the output edge rate (dV_O/dt). The output edge rate is inversely proportional to the capacitive load it is charging or discharging, which explains the reduction in ground bounce with an increase in the lumped capacitance at the output.

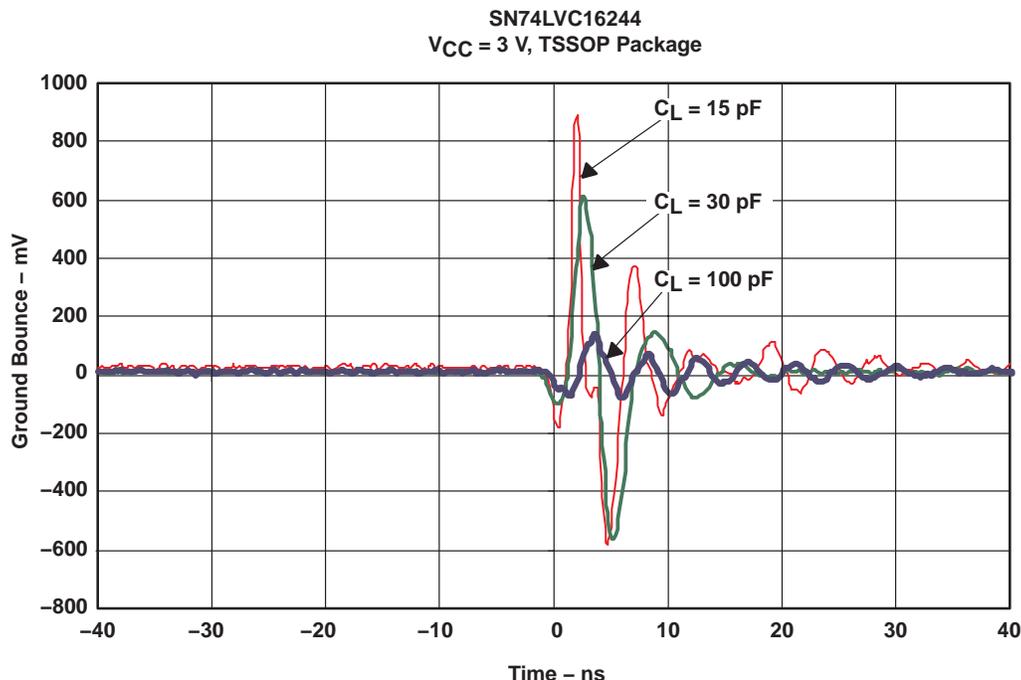


Figure 8. Effect of Output Capacitive Load on Ground Bounce

2.5 Effect of Package Options

2.5.1 Reducing Package Inductance

Ground bounce is directly proportional to the ground inductance L_{GND} (see Equation 2). To reduce simultaneous-switching noise, the value of the ground-lead inductances must be reduced. However, all pins pose an inductance, so it is vital to use better packaging with reduced lead inductance (see Table 1).

Table 1. Pin Inductance Values^[4]

PACKAGE	MAXIMUM DIE-TO-PIN INDUCTANCE (nH)
48-pin SSOP	7.970
48-pin TSSOP	3.990
48-pin TVSOP	4.310
96-ball BGA	2.866

Lead inductance is proportional to lead length. Smaller packages with shorter leads reduce simultaneous-switching noise. Figures 9–12 show ground bounce on the SN74LVCH16244 using different packages.^[4] The maximum positive ground bounce is reduced from 1 V for the SSOP package to about 300 mV for the LFBGA package – an improvement of 70%. TI also offers devices in the quad flatpack no-lead (QFN) package, which has excellent thermal and electrical characteristics. For more information on this package, please refer to TI application report, *Quad Flatpack No-Lead Logic Packages*, literature number SCBA017. Using packages such as TVSOP, QFN, and LFBGA, which demonstrate superior simultaneous-switching performance, is recommended.

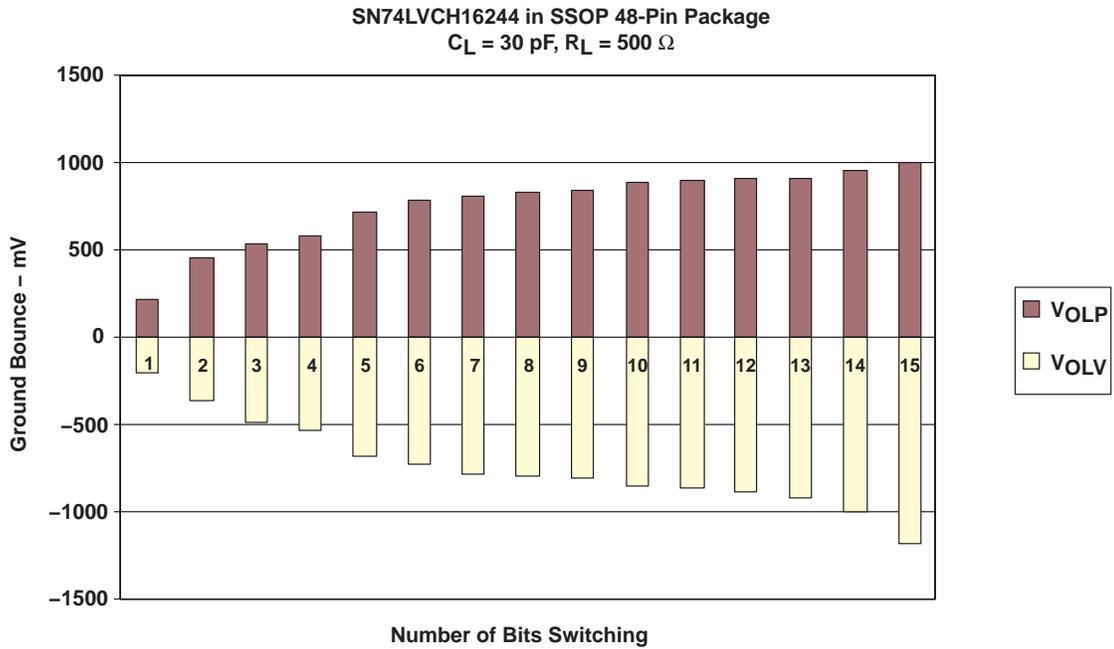


Figure 9. Ground Bounce Using SSOP 48-Pin Package

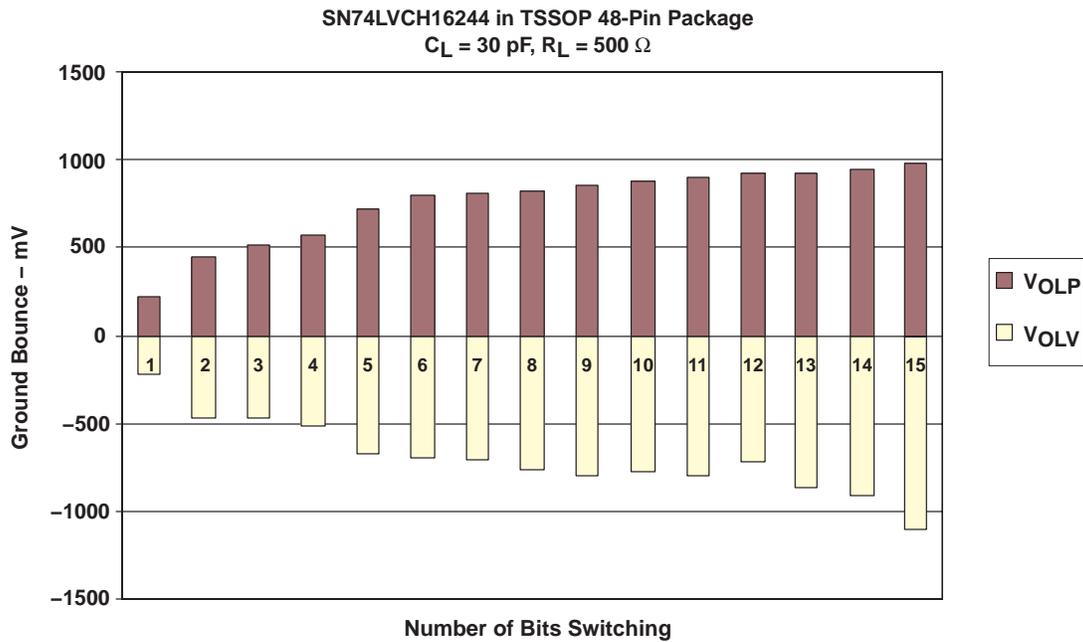


Figure 10. Ground Bounce Using TSSOP 48-Pin Package

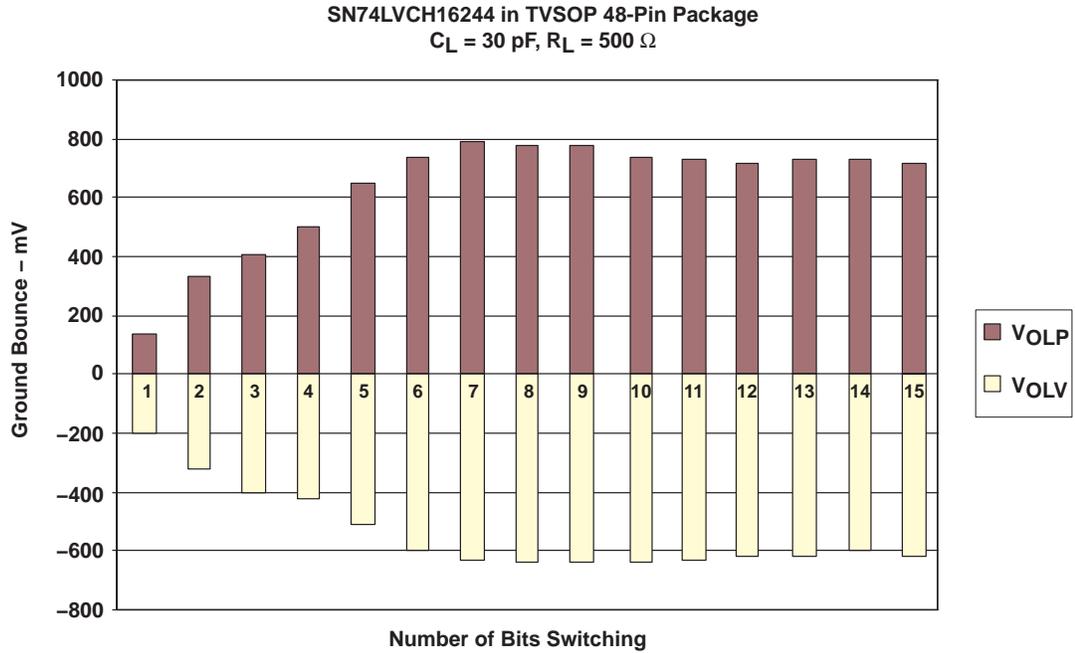


Figure 11. Ground Bounce Using TVSOP 48-Pin Package

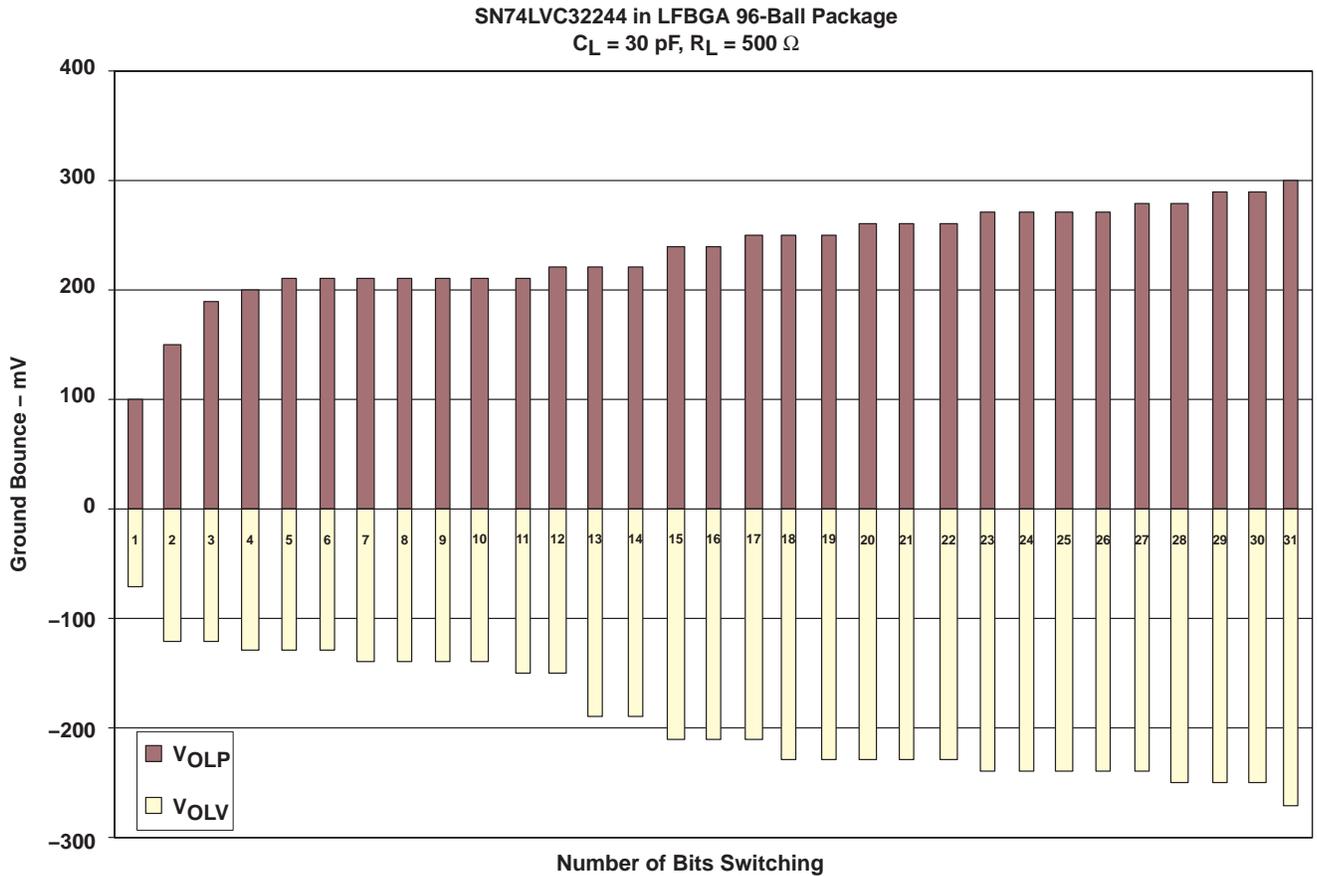


Figure 12. Ground Bounce on SN74LVC32244 Using LFBGA 96-Ball Package

2.5.2 Multiple GND and V_{CC} Pins

Multiple ground pins reduce the total ground inductance because the total inductance is a parallel combination of the ground-lead inductances. Hence, with n ground pins, the total ground inductance is approximately 1/n times that of a similar chip with only one GND pin. TI Widebus™ and 32-bit devices are available with multiple GND and V_{CC} pins to improve simultaneous-switching performance.

$$\frac{1}{L_{total}} = \frac{1}{L_1} + \frac{1}{L_2} + \dots + \frac{1}{L_N} \quad (7)$$

Devices with center GND and V_{CC} pins also show excellent simultaneous-switching performance. The center pins are closest to the die, have the shortest leads, and have smaller inductance values. Table 2 shows TI devices that are available with center pins for better simultaneous-switching performance.

Table 2. TI Logic Devices Available With Center GND and V_{CC} Pins

DEVICE	FUNCTION	DEVICE	FUNCTION
74AC1100 74ACT11000	Quad 2-Input Positive-NAND Gates	74AC11138	3-Line to 8-Line Decoder/Demultiplexer
74AC11004 74ACT11004	Hex Inverter	74ACT11139	Dual 2-Line to 4-Line Decoder/Demultiplexer
74AC11008 74ACT11008	Quad 2-Input Positive-AND Gates	74AC11175	Quad D-Type Flip-Flop with Clear
74ACT11030	8-Input Positive-NAND Gates	74AC11244 74ACT11244	Octal Buffer/Driver with 3-state Outputs
74AC11032 74ACT11032	Quad 2-Input Positive-OR Gates	74AC11257 74ACT11257	Quad 2-Line to 1-Line Data Selector/Multiplexer with 3-state Outputs
74AC11074 74ACT11074	Dual Positive-Edge-Triggered D-type Flip-Flop with Clear and Preset	74ACT11286	9-Bit Parity Generator/Checker with Bus Driver Parity I/O ports
74AC11086	Quad 2-Input XOR Gate	74ACT11374	Octal Edge-Triggered D-Type Flip-Flops with 3-state Outputs

2.6 Use of Series-Damping-Resistor Option

Several TI logic devices are offered with an output-damping-resistor option. This resistor eliminates the need for an external damping resistor, provides current limiting, and offers better signal integrity. Figure 13 shows a typical CMOS output with a series damping resistor. TI logic devices with an extra “2” or “R” in the device name have the damping-resistor option, for example, SN74LVC162244 or SN74LVCHR16245. Figure 14 shows the improvement in simultaneous-switching performance by using the internal series damping resistor.

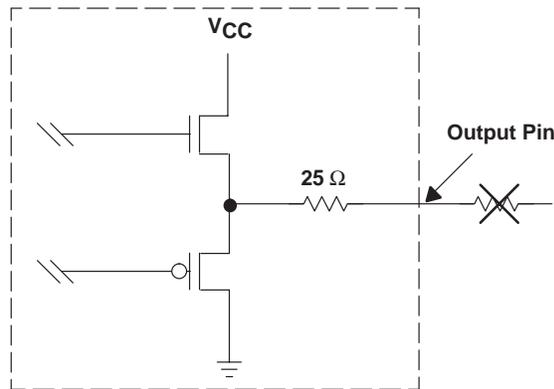


Figure 13. Damping Resistors Replace External Series Resistors

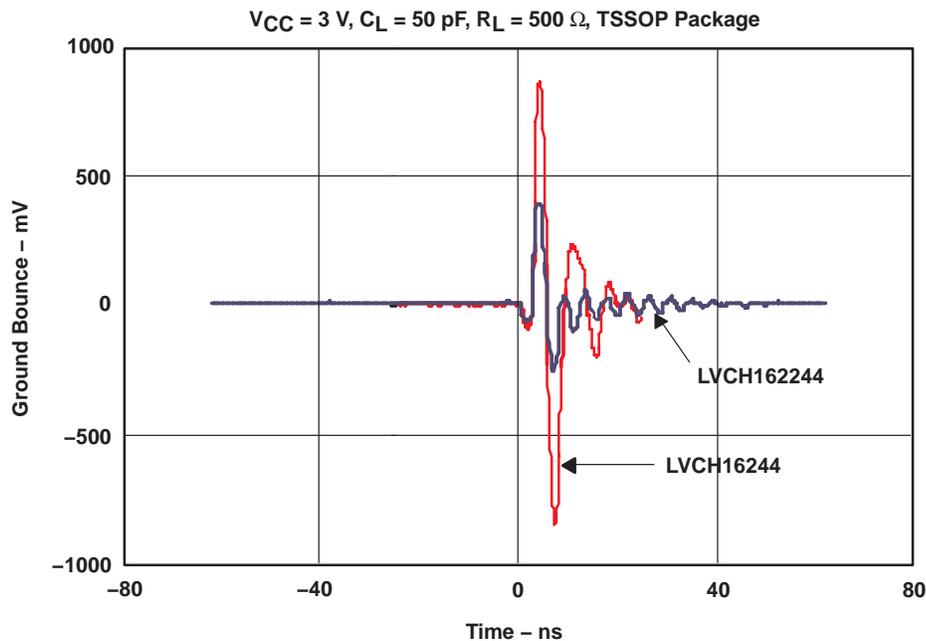


Figure 14. Improvement in Simultaneous-Switching Performance Using Device With Series-Damping-Resistor Option

3 Concerns Regarding Simultaneous-Switching Noise

3.1 Glitches or False Switching

The input threshold of CMOS devices depends on the voltage difference across the input structure. Ground bounce causes a change in this voltage across the input structure, which shifts the input threshold (see Figure 15).

For example, the input threshold for a 3.3-V LVTTTL device is approximately 1.5 V. If a positive ground bounce of 1 V is observed, the threshold shifts to 2.15 V [1 V of bounce + 50% of (3.3 – 1)]. If there were a quiet input at 2 V, the input structure falsely detects a change of state. Depending on the type of device and the input under question, this can alter the state of a device, causing corruption of data.

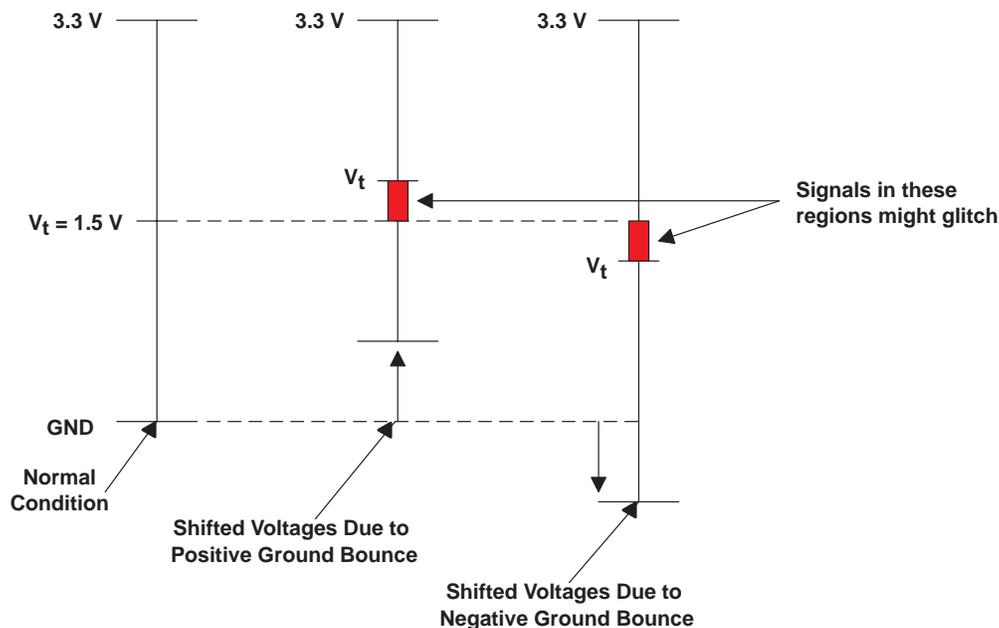


Figure 15. Change in Threshold Levels Caused by Ground Bounce

Ground bounce can cause failure in a system as well. If the ground bounce is very large and crosses the input threshold of a subsequent device, the subsequent device might falsely switch. If the subsequent device is an asynchronous device, such as an inverter, the device output might falsely change states. Or, if the subsequent input is the clock input of a synchronous device like a flip-flop, it may falsely trigger this input, latching in an incorrect value.

A slow-rising input edge, combined with ground-bounce effects, can cause the output to oscillate because of a shift in the input threshold. For further information, please see TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

3.2 Propagation-Delay Degradation

3.2.1 Causes

As ground bounce increases, the propagation delay through the device is affected adversely. To understand the cause of propagation-delay (t_{pd}) degradation, consider Figure 16, which shows a CMOS output stage modeled as an RC network. Ground bounce increases the voltage drop across R2 (reduces the voltage across R1), reducing current in the output loop. The rate of change of voltage across the capacitor (dV_O/dt) is directly proportional to the current in the loop (see Equation 1). As this current decreases, the output is slowed; hence, it takes more time to transition from rail to rail.[1] This causes the t_{pd} push-out shown in Figure 17.

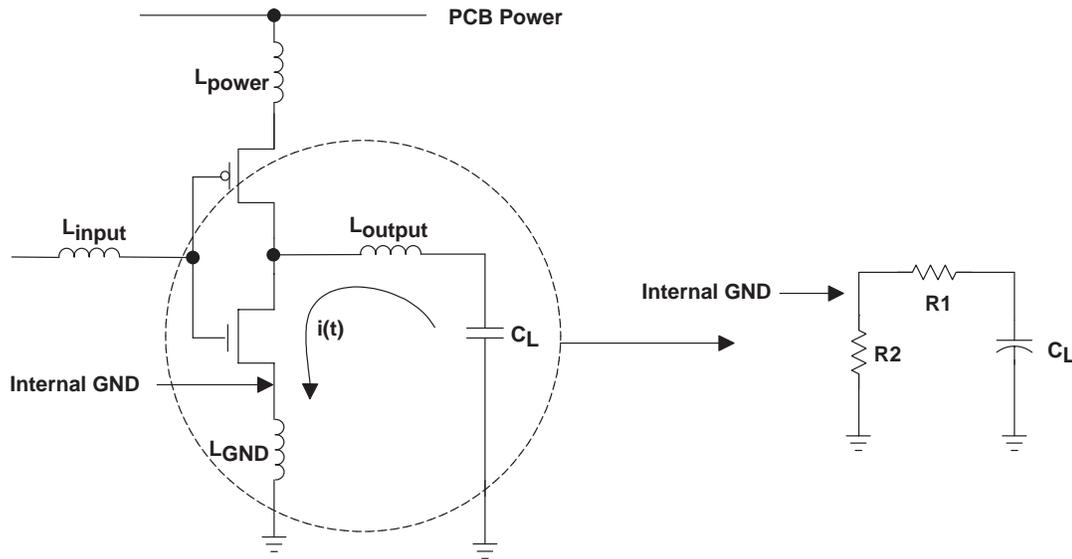


Figure 16. Output Stage Modeled as RC Network

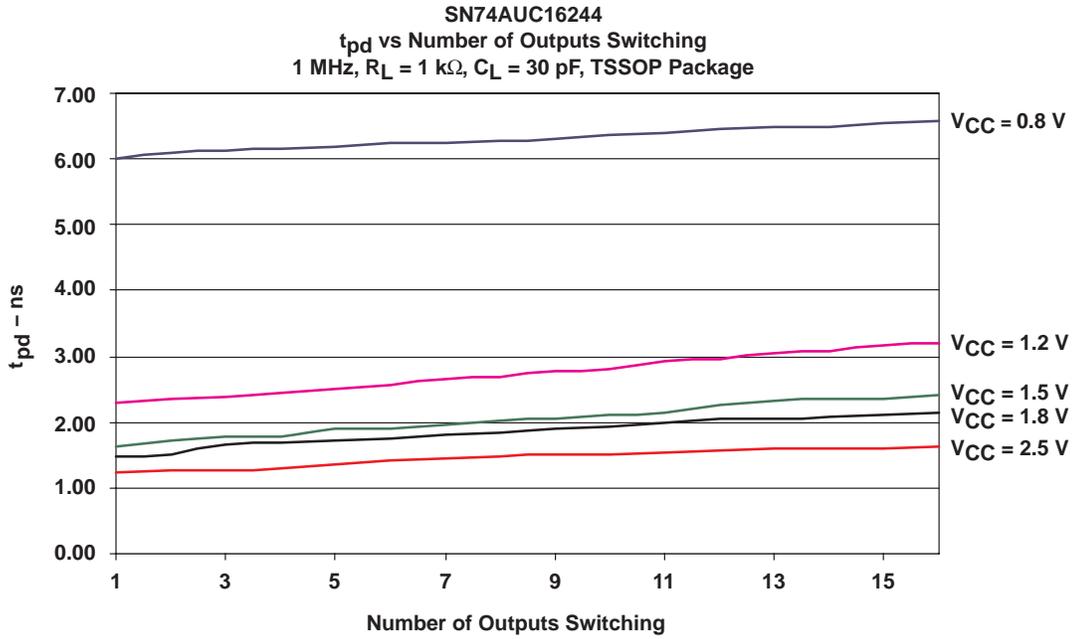


Figure 17. Propagation-Delay Degradation

3.2.2 Jitter in Clock-Distribution Applications

When clock signals with different frequencies are passed through a single logic device, simultaneous switching can lead to output jitter because of propagation-delay degradation (t_{pd} pushout).

Because of the different clock frequencies, at any given time there might be a different number of bits switching simultaneously. For example, at time t , there might be only one bit switching; at time $(t + x)$, there might be four bits switching simultaneously, whereas at time $(t + y)$, there might be three bits switching simultaneously. If the signals at time t , $(t + x)$, $(t + y)$, etc. are overlaid, it produces an eye pattern that can be used to observe jitter.

Such an eye pattern for an SN74LVTH125DB is shown in Figure 18. Using HSPICE, four signals were passed through the device model: signal 1 at 100 MHz, signal 2 at 50 MHz, signal 3 at 33 MHz, and signal 4 at 25 MHz. Figure 18 shows the jitter on signal 1 output to be 195 ps. Figure 19 shows the same signal, but modeled using three GND and three V_{CC} pins. The observed jitter is reduced to 102 ps. Hence, devices with multiple GND and V_{CC} pins can be used to reduce the incidence of jitter in such clock-distribution applications.

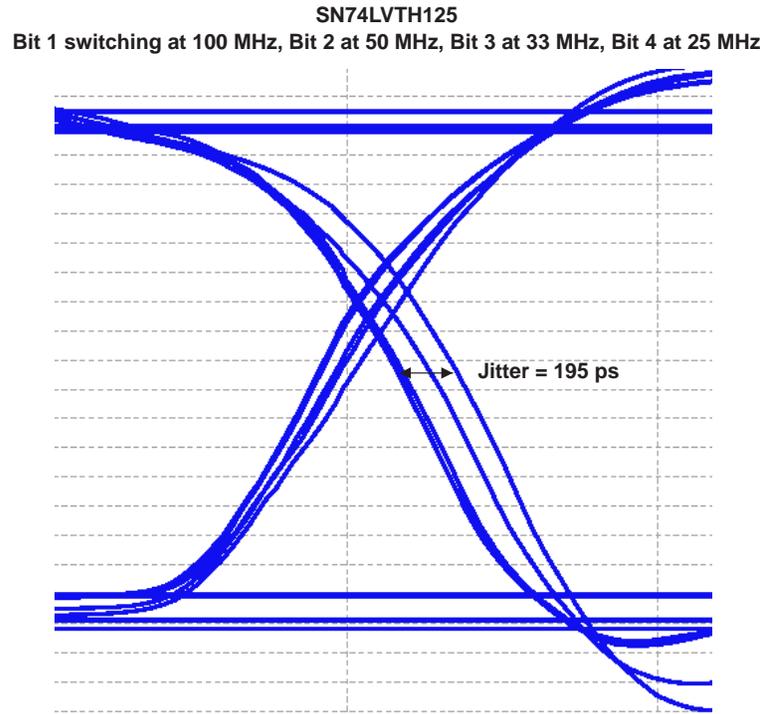


Figure 18. Eye Pattern for Signal 1 Switching at 100 MHz

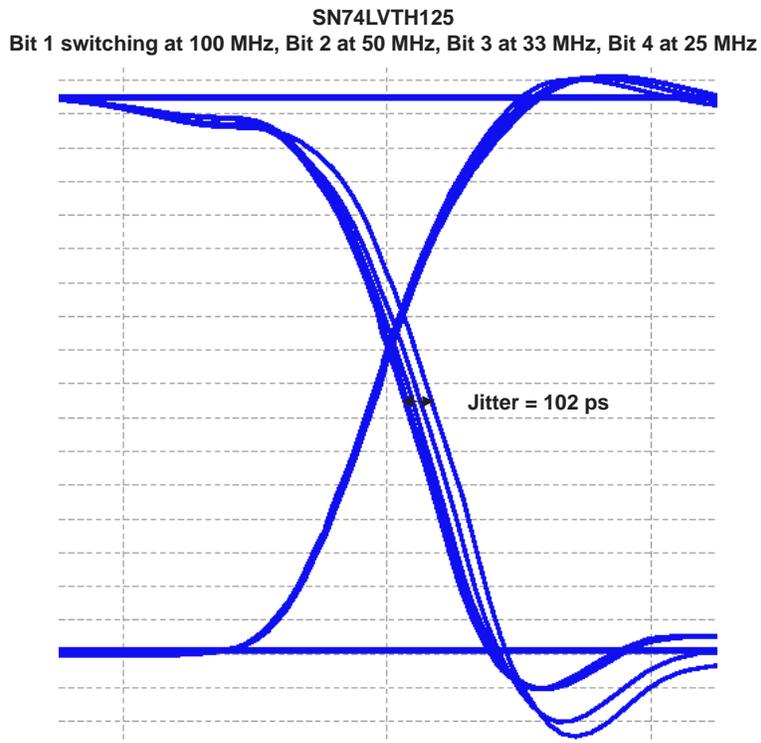


Figure 19. Eye Pattern for Signal 1 Switching at 100 MHz, Using Multiple GND and V_{CC} Pins

3.3 Increase in the Supply Current

The length of the internal paths from different inputs to their corresponding outputs might be different, even on the same device. Multiple-output drivers might not switch at exactly the same time, causing paths from V_{CC} to ground to exist during simultaneous switching. As the number of simultaneously switching outputs increases, the paths from V_{CC} to ground exist for a longer time, leading to a greater supply current. This larger supply current interacts with the ground inductance, leading to greater ground bounce (see Figure 20).

SN74AUC16244
 $R_L = 0$, $C_L = 0$, ~15-pF Board Capacitance, TSSOP Package,
 Outputs Switching at 100 MHz

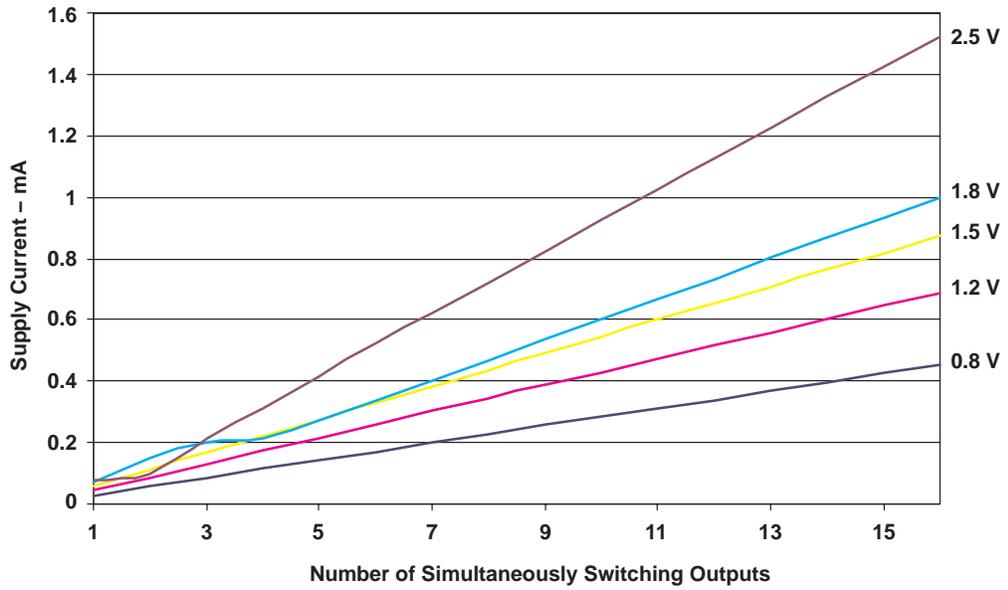


Figure 20. Increase in Supply Current With Number of Bits Switching

4 Conclusion

Several factors affect the simultaneous-switching performance of a logic device. These include temperature, supply voltage, number of bits switching, package options, and output loads. Simultaneous-switching noise can lead to device and system-level issues. There are different approaches to reducing this noise. One approach is to use devices with the damping resistor option. Another approach is to use better package options that offer reduced lead inductances, multiple GND and V_{CC} pins, and/or center GND and V_{CC} pins. TI AUC devices with advanced package techniques demonstrate excellent ground-bounce performance. By knowing how different factors affect ground bounce, systems can be optimized for better simultaneous-switching performance.

5 Acknowledgments

The authors of this report thank Tomdio Nana and Ernest Cox for their contributions.

6 References

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2. Navid Madani, *Simultaneous-Switching Noise Analysis for Texas Instruments FIFO Products*, Application Report, literature number SCAA008, 1996.
3. Mike Higgs, *Advanced Schottky Load Management*, Application Report, literature number SDYA016, 1997.
4. Johannes Huchzermeier, *Comparison of Electrical and Thermal Parameters of Widebus™ SMD, and LFBGA Packages*, Application Report, literature number SCYA007, 1999.

Appendix A

Ground bounce of devices from different TI logic families is shown on the following pages. For each device, the worst-case-condition bounce is shown (noise on one quiet output that is held low, while all other outputs are switched from H to L).

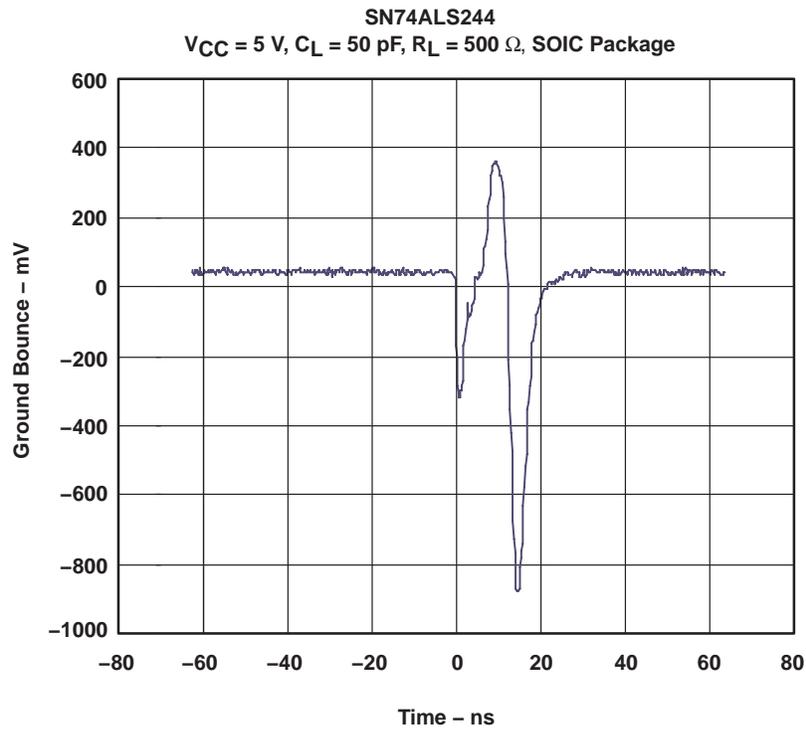


Figure A-1. Bounce on Quiet Output Held Low, While the Other Seven Outputs Are Switched From H to L, SN74ALS244

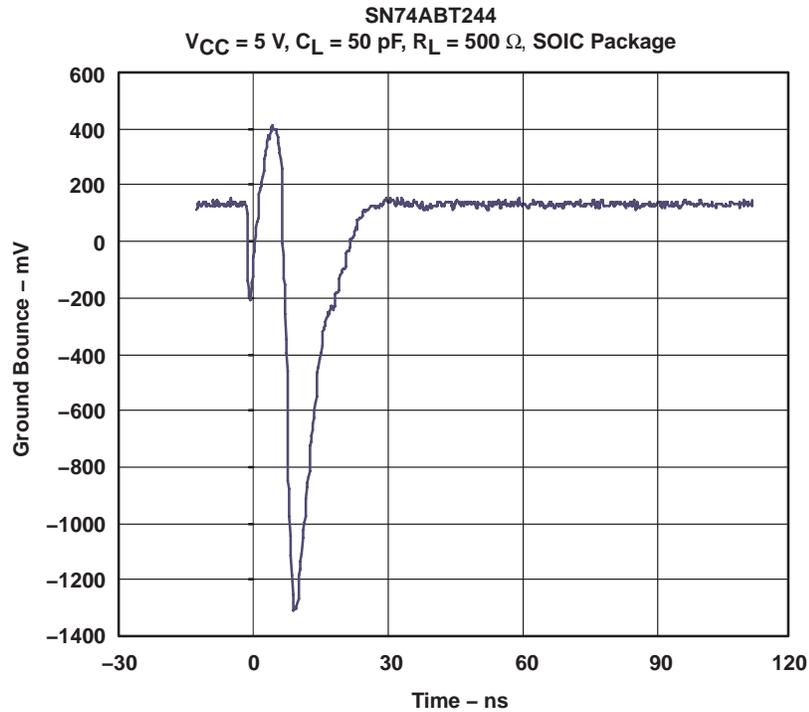


Figure A-2. Bounce on Quiet Output Held Low, While the Other Seven Outputs Are Switched From H to L, SN74ABT244

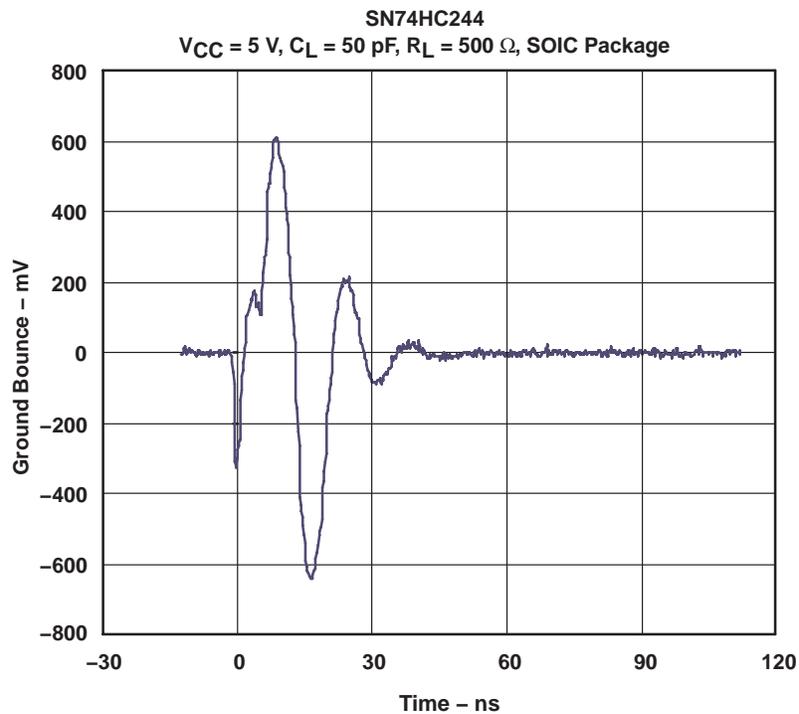


Figure A-3. Bounce on Quiet Output Held Low, While the Other Seven Outputs Are Switched From H to L, SN74HC244

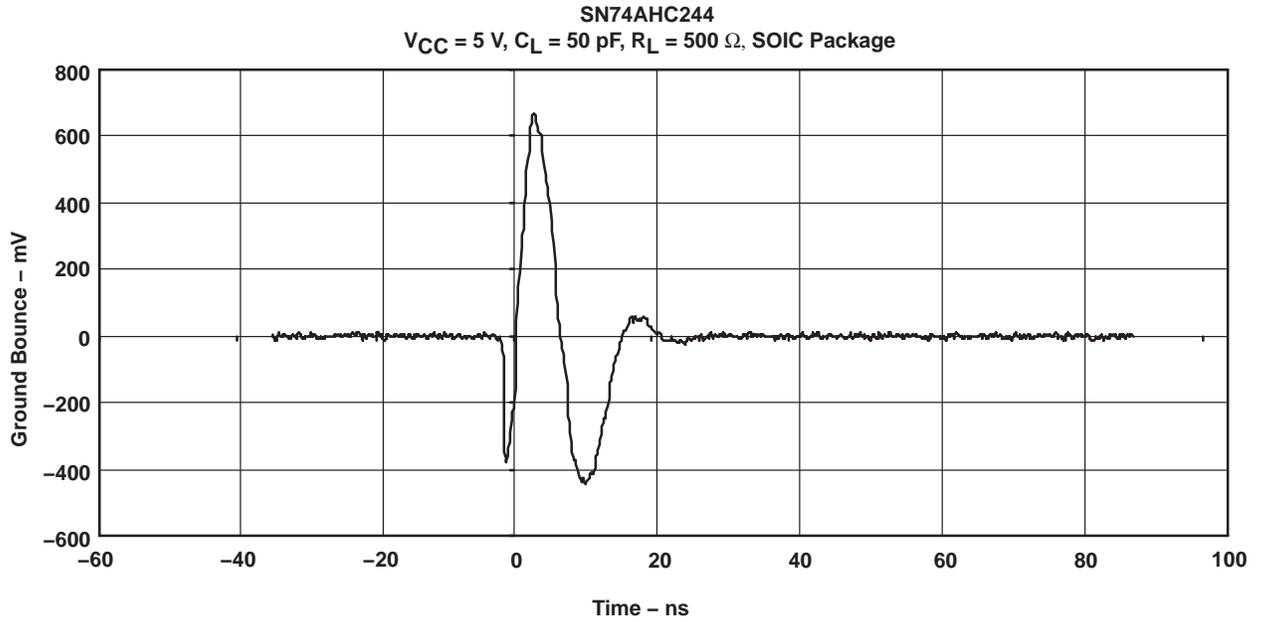


Figure A-4. Bounce on Quiet Output Held Low, While the Other Seven Outputs Are Switched From H to L, SN74AHC244

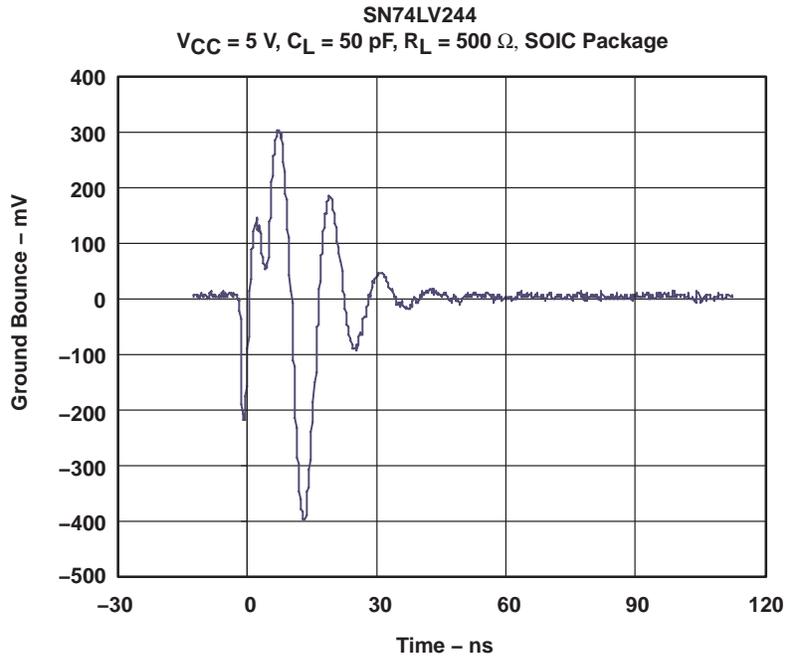


Figure A-5. Bounce on Quiet Output Held Low, While the Other Seven Outputs Are Switched From H to L, SN74LV244

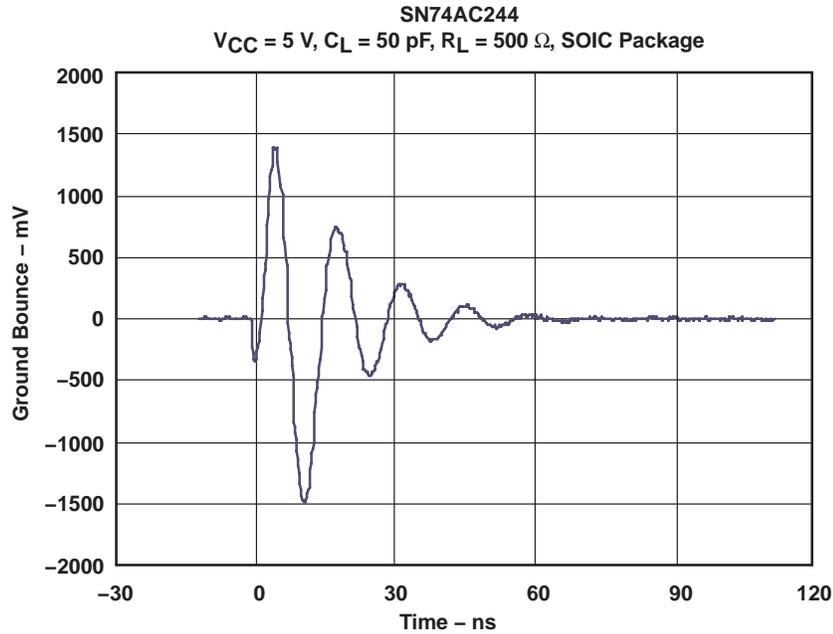


Figure A-6. Bounce on Quiet Output Held Low, While the Other Seven Outputs Are Switched From H to L, SN74AC244

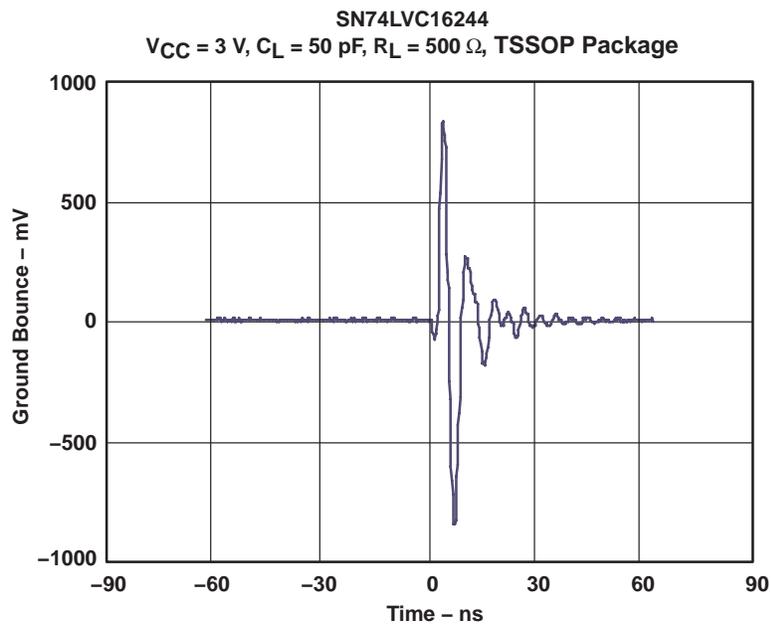


Figure A-7. Bounce on Quiet Output Held Low, While the Other 15 Outputs Are Switched From H to L, SN74LVC16244

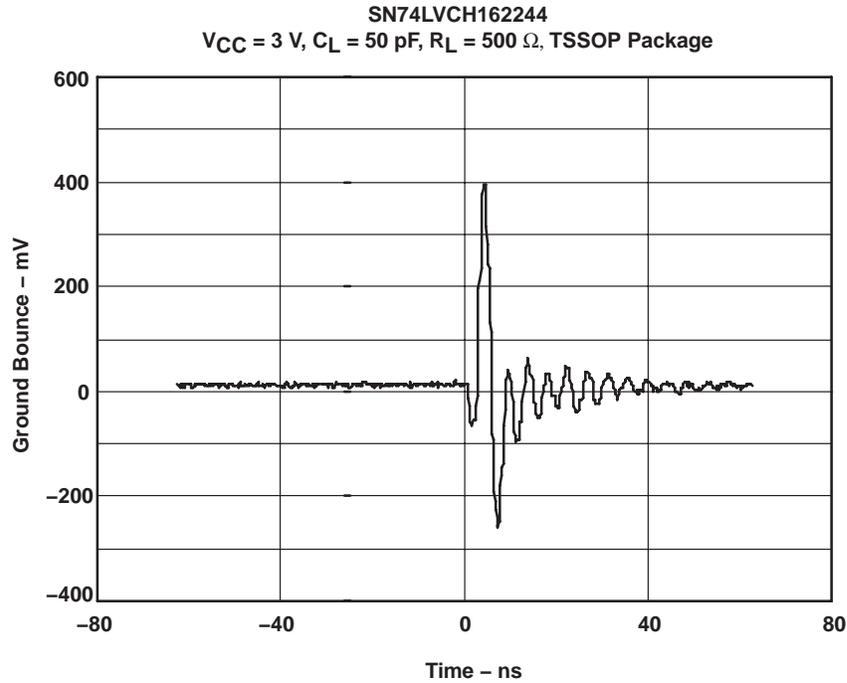


Figure A-8. Bounce on Quiet Output Held Low, While the Other Seven Outputs Are Switched From H to L, SN74LVCH162244

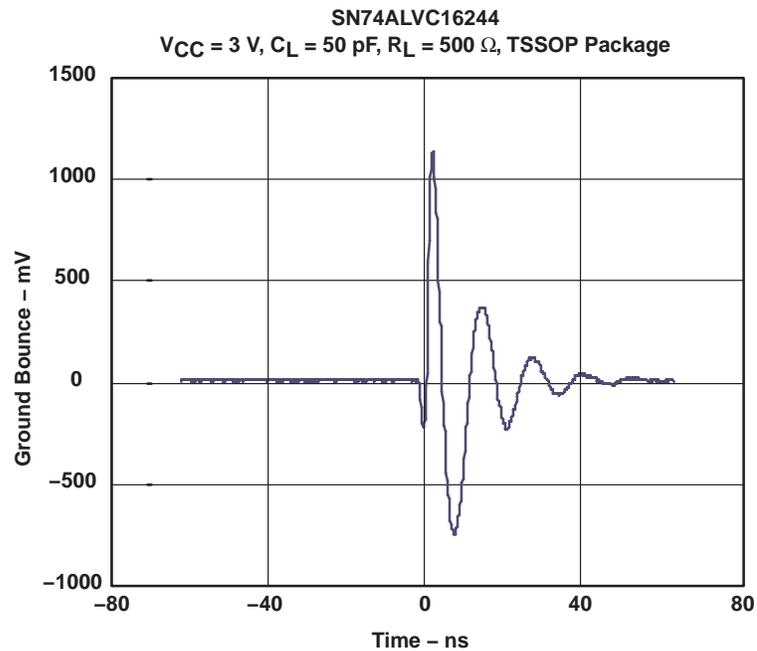


Figure A-9. Bounce on Quiet Output Held Low, While the Other 15 Outputs Are Switched From H to L, SN74ALVC16244

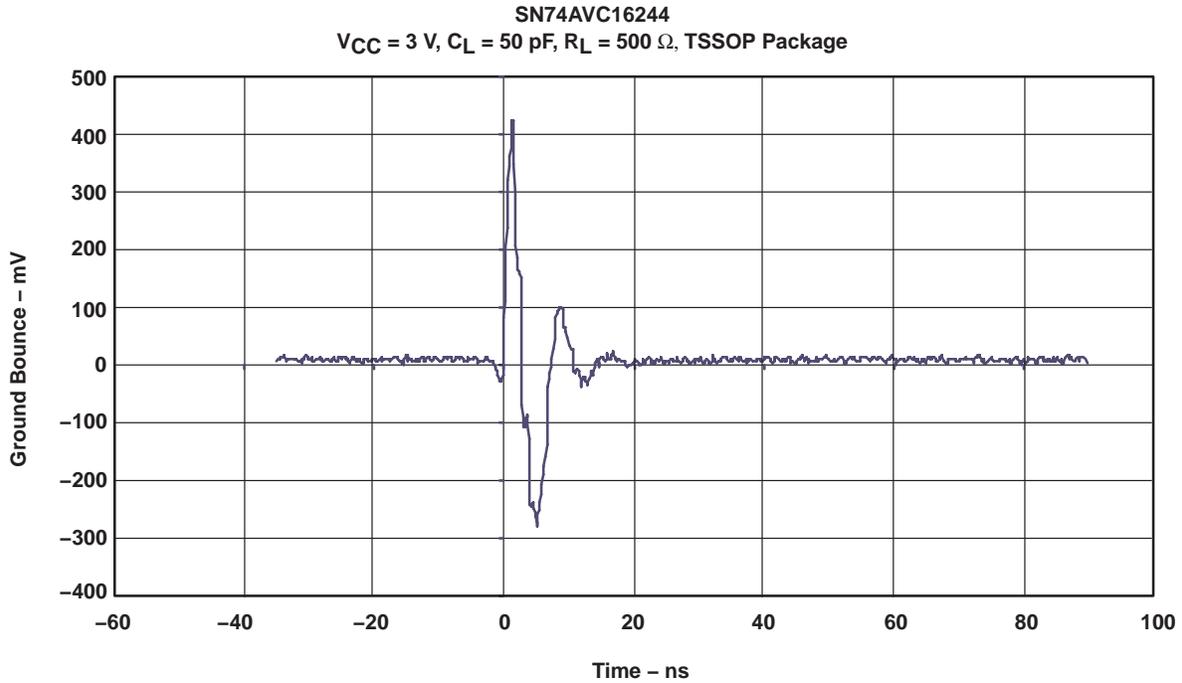


Figure A-10. Bounce on Quiet Output Held Low, While the Other 15 Outputs Are Switched From H to L, SN74AVC16244

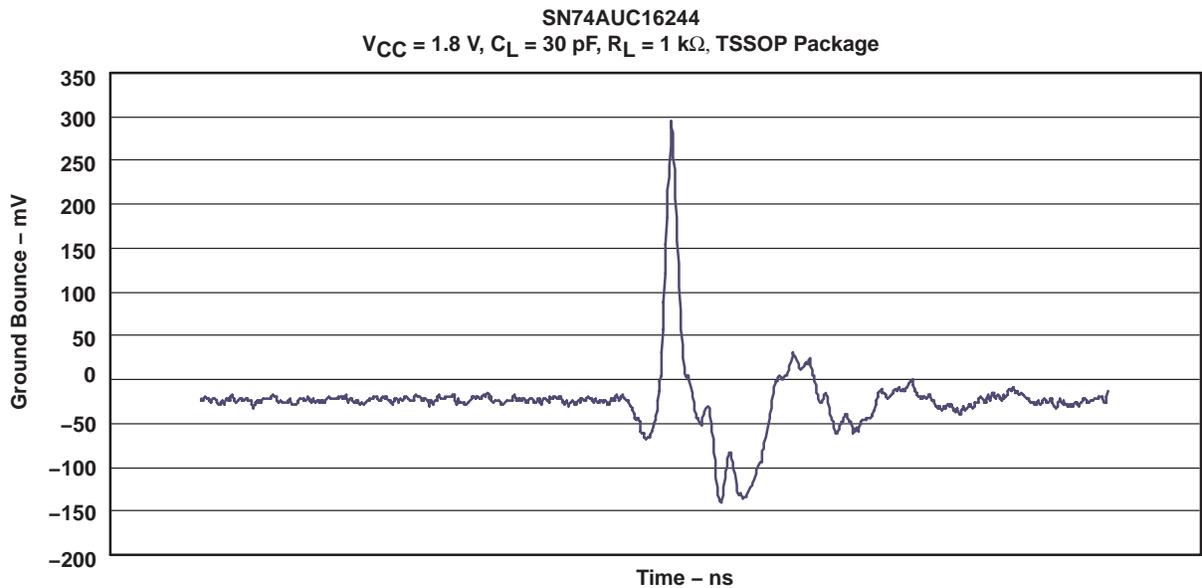


Figure A-11. Bounce on Quiet Output Held Low, While the Other 15 Outputs Are Switched From H to L, SN74AUC16244

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