Power-Up 3-State (PU3S) Circuits in TI Standard Logic Devices

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ABSTRACT

Many telecom and networking applications require that cards be inserted and extracted from a live backplane without interrupting data or damaging components. To achieve this, interface terminals of the card must be electrically isolated from the bus system during insertion or extraction from the backplane. To facilitate this, Texas Instruments provides bus-interface and logic devices with features such as I_{OFF}, power-up 3-state (PU3S), and precharge circuits. A combination of these three features, along with the output enable and disable feature, allows the customer to realize a successful live insertion. This application report discusses the concept of PU3S circuitry, its functionality, and the interpretation of data-sheet parameters related to this feature.

For an explanation of I_{OFF}, precharge circuits, and live insertion, please refer to the TI application report, *Logic in Live Insertion Applications With a Focus on GTLP*, literature number SCEA026.

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Why Power-Up 3-State (PU3S) Circuits?

In almost all of the backplanes in telecom and networking applications requiring live insertion, the power source commonly resides in the backplane chassis. Power planes or traces are routed, along with data lines, to the daughter cards in different slots. While inserting a daughter card into a live backplane, the V_{CC} plane, output, and I/O ports are connected to the power line and the live data at the same time (with special connectors, the situation may vary). The power plane of the daughter card cannot be charged instantaneously. A minimal time is required to charge all the devices and their requisite bypass capacitors before the card reaches the desired V_{CC} level. Depending on the amount of circuitry on board, this time may vary from microseconds to several hundred milliseconds. In the electronics world, this is sufficient time for any undesired surge current through the device output or I/O ports to cause permanent damage to, or degradation of, the device. The same situation can occur while extracting the card from the backplane or partially powering down a segment of the system to save energy. The situation is illustrated in Figure 1.
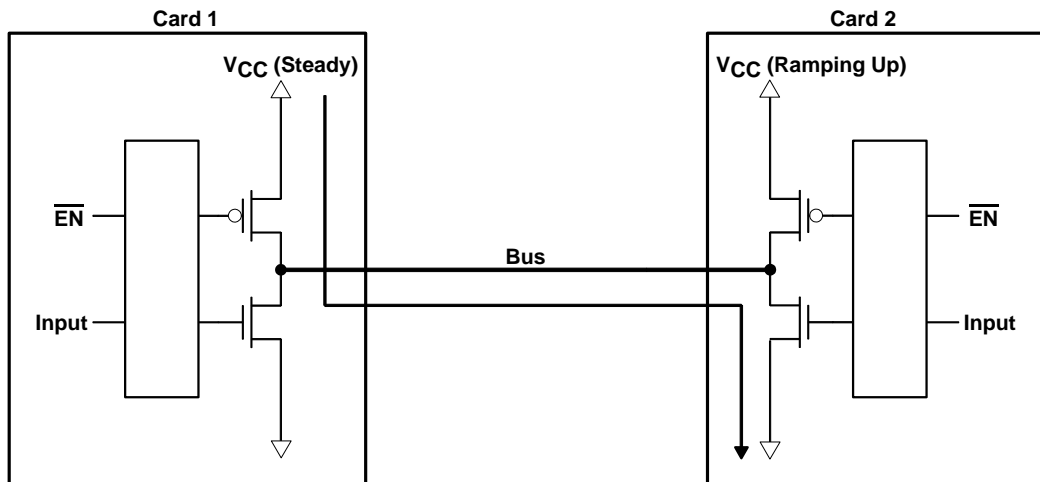
Figure 1. Bus Contention During Power Up

In Figure 1, it is assumed that the interface devices are noninverting buffers with an active-low enable input, and daughter card 1 is driving the bus high. Then, card 2 (with $\overline{EN}$ and input pulled down to GND) is inserted into the backplane slot. Because of the input and the enable-pin conditions, card 2 will turn the pulldown transistor on and actively drive the bus low. This may happen while the V_{CC} plane of card 2 is ramping up at a voltage much below the recommended operating region. The result is a momentary low-impedance current path from the steady-state full V_{CC} plane of card 1 to GND of card 2. This could easily cause damage to either device.

A second scenario can occur, even in applications not meant for live insertion. While ramping up V_{CC}, the logic device input may respond to noise below its threshold level. As a result, it may generate an undesired logic state at the output and cause erroneous data in the application. Because inputs cannot be completely isolated electrically, a suitable solution is obtained if the output does not respond to any input signal until the recommended V_{CC} is reached.

This type of application requires interface-logic devices to have protection from the outside world while the device V_{CC} rail is powering up or powering down. PU3S circuits, available on select TI logic families, isolate the output while V_{CC} is ramping up or ramping down. In the recommended V_{CC} region, this circuit should not affect device operation. Thus, TI power-up circuitry is designed to operate up to approximately one-half the recommended V_{CC} range.

Basic Operating Principle

PU3S circuits in TI logic disable the output buffer of the output or I/O ports of a logic device while V_{CC} is ramping up or ramping down. The PU3S circuit consists of a separate control block similar to the output-disable or direction-control circuitry (see Figure 2).
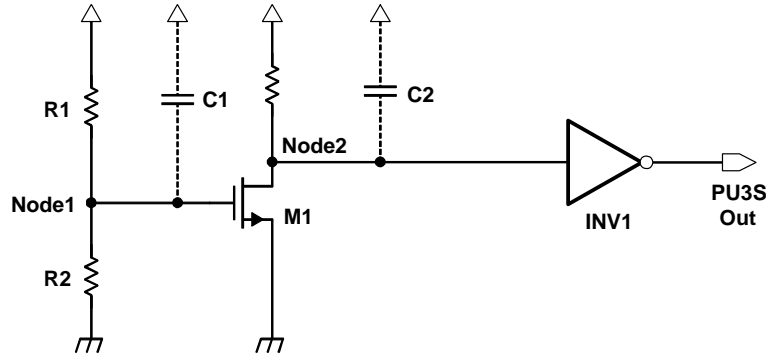

Figure 2. PU3S Circuit of TI Logic Devices

The circuit in Figure 2 works on the following principle. With a low state at the PU3S output, the device output buffer is disabled. A high state at the PU3S output releases its control of the output buffer. R1 and R2 (in practice, the implementation of R1 and R2 may differ from simple resistors) work as a voltage divider. With V_{CC} = 0 V, or below the data-sheet specified threshold limit, the voltage at node 1 is not sufficient to turn on the M1 transistor. As a result, the voltage at node 2 remains at a high logic state to generate a low output at PU3S out. At a certain V_{CC} level, (above the data-sheet specified limit, as stated in the test conditions of Table 2) the voltage at node 1 is sufficient to turn on the n-channel transistor M1. This, in turn, generates a high logic output at PU3S out. So, it does not matter whether it is a power-up or power-down situation, resistor-divider R1, R2, and transistor M1 determine the threshold voltage. Above this threshold V_{CC}, the state of the device output buffer depends on input, OE, DIR, or other control pins. Below this threshold, the PU3S circuit disables the output buffer, regardless of any other input condition.

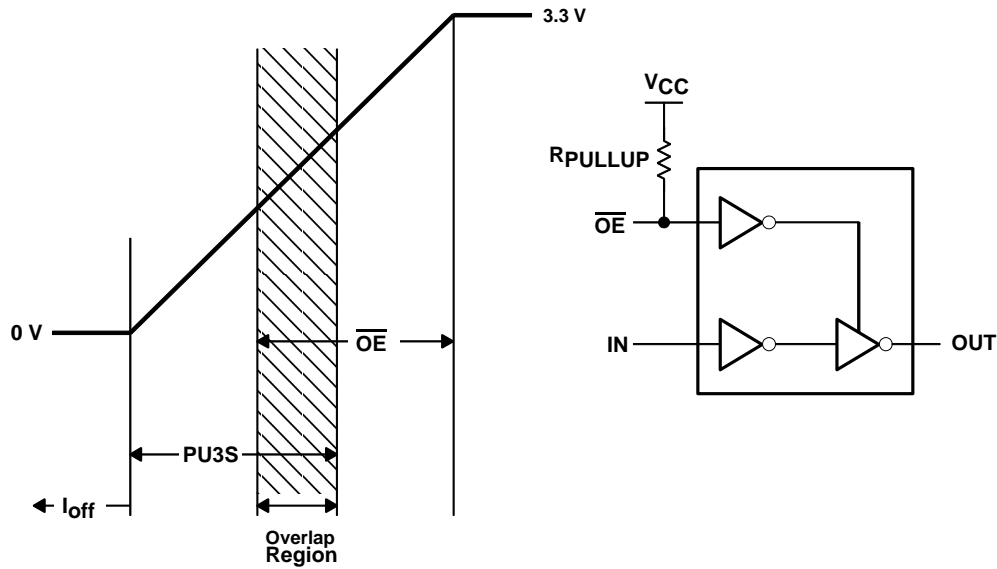# Protection for the Full Range of V_{CC} Ramping

Figure 3. Protection at Different Regions of V_{CC} Ramp

While powering up and powering down, three different circuits take part in isolating the output and I/O ports from the bus. At V_{CC} = 0 V, the I_{OFF} circuitry prevents the upper transistors of the output buffer from providing an active path for a data-sheet-specified signal at the output or I/O pin. While V_{CC} is ramping from 0 V up to a V_{CC} level equal to the process transistor threshold, all transistors in the device remain off. At that V_{CC} level, the PU3S circuit activates and forces the device output(s) into the high-impedance state. Again, after crossing the threshold V_{CC} level (V_{CC} threshold levels of individual families are specified in Table 2), the PU3S releases its control of the output(s) to the DIR, OE, or other control pins.

To maintain complete isolation throughout the ramping process, the OE pin needs to remain at the inactive level specified on the data sheet. There is an overlap region where both the PU3S and the OE circuit can take control of the output(s). This overlap region ensures that neither the pullup nor the pulldown transistors of the output is in the active state at any time during power up or power down, while the OE or control pins are held in the inactive state. The recommended practice to maintain an inactive level on the OE circuitry is to pull the OE input high or low with a weak pullup or pulldown resistor to V_{CC} or GND. The overlap region between OE and PU3S for disabling the output buffer of TI standard logic parts is not production tested. This data is obtained during characterization.

TEXAS
INSTRUMENTS

Data-Sheet Parameters for PU3S

Recommended Operating Conditions

Table 1 shows the data-sheet-recommended operating conditions for the V_{CC} ramp rate of different TI logic families with PU3S (Not all devices of a specific family have PU3S. Customers should refer to the data sheet for the device under consideration).

Table 1. Recommended V_{CC} Ramp Rate

DEVICE FAMILY	POWER-UP RAMP RATE $\Delta t/\Delta V_{CC}$	MIN/MAX
LVT	200 µs/V	Min
ALVT	200 µs/V	Min
ABT	200 µs/V	Min
GTLP	20 µs/V	Min
GTL	200 µs/V	Min
VME	20 µs/V	Min
FB†	200 µs/V	Min
LVCZ	150 µs/V	Min

† Power-up ramp rate is not specified in data sheets for FB-family devices. Nevertheless, those devices use the same PU3S circuits as the other TI logic devices, and have a minimum value of recommended $\Delta t/\Delta V_{CC}$.

A frequent source of confusion is that different logic vendors represent the V_{CC} ramp rate requirement in the data sheet in different ways. This specific parameter in the TI data sheet indicates that, with a V_{CC} ramp rate faster than specified, proper operation of the PU3S circuitry cannot be assured. To clarify the point, 20 µs/V is not recommended for an LVT power-up ramp rate because it is faster than 200 µs/V. Figure 4 shows the valid operating region for LVT, ALVT, ABT, and FB families. Similar graphical representations can be drawn for the other families with PU3S listed in Table 1.
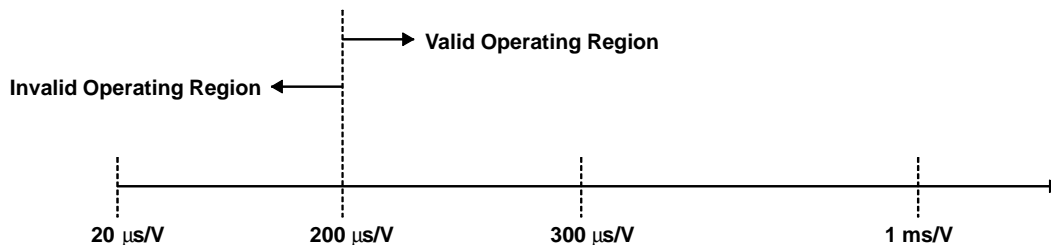

Valid Operating Region

Invalid Operating Region

20 µs/V   200 µs/V   300 µs/V   1 ms/V

Figure 4. Valid Operating Region for LVT, ALVT, ABT, and FB Families

At faster ramp rates, the device output buffer may become active due to a "race condition", when V_{CC} is lower than the threshold level. We can explain the race condition as follows: the parasitic capacitors (C1 and C2 in Figure 2) across the resistors need time to be charged or discharged. With a very fast ramp rate, the capacitors may not have sufficient time to stabilize, and the output of the power-up circuitry may turn on the device output earlier than desired. The recommended power-up ramp rate of each family is common throughout that family. This is because all of the devices from each family use the same process and circuit design for their power-up circuits.

Data-Sheet Test Parameters

Table 2 shows the data-sheet values for the PU3S-associated parameters, along with I_{OFF} and I_{OZ} specifications. From this table, it can easily be concluded how much current the device would sink or source at different stages while powering up or powering down. For accurate and updated specifications for a specific device, please see the data sheet, rather than relying on this table.

Table 2. Current Through Output(s) at Different Stages of Power Up

DEVICE FAMILY	TEST CONDITIONS (FOR POWER-UP CIRCUITS ONLY)	I_{OZPU} (μA, max)	I_{OZPD} (μA, max)	I_{OFF} (μA, max)	I_{OZ} (μA, max)
LVT	$V_{CC} \leq 1.5$ V, $V_O = 0.5$ V to 3 V, OE don't care	±100	±100	±100	±5
ALVT	$V_{CC} \leq 1.2$ V, $V_O = 0.5$ V to V_{CC}, OE don't care	±100	±100	±100	±5
ABT	$V_{CC} \leq 2.1$ V, $V_O = 0.5$ V to 2.7 V, OE don't care	±50	±50	±100	±10
GTLP	$V_{CC} \leq 1.5$ V, $V_O = 0.5$ V to 1.5 V, OE enabled, BIAS $V_{CC} = 0$	±30	±30	±10	±10
GTL1655	$V_{CC} \leq 1.5$ V, $V_O = 0.5$ V to 3 V, OE don't care	±100	±100	±100	±10
VME	$V_{CC} \leq 1.5$ V, $V_O = 0.5$ V to 3 V, OE don't care	±100	±100	±100	±10
FB (TTL side)	$V_{CC} \leq 2.1$ V, $V_O = 0.5$ V to 2.7 V, OE don't care	±50	±50	±100	±50
LVCZ	$V_{CC} \leq 1.5$ V, $V_O = 0.5$ V to 2.5 V, OE don't care	±5	±5	±5	±5

I_{OZPU} is the current into or out of the device output or I/O pin while V_{CC} is ramping up. I_{OZPD} is the current into or out of the device output or I/O pin while V_{CC} is ramping down. I_{OZPU} and I_{OZPD} are based on the test conditions in Table 2.

I_{OFF} is the current into or out of the device output, I/O, or input pin when a positive voltage is applied at that pin with V_{CC} = 0 V. The valid range of this applicable voltage at a specific pin is specified in the data sheet under the I_{OFF} test condition.

I_{OZ} is the current into or out of an output or I/O pin when the output buffer of the output or I/O pin is in the high-impedance state. Sometimes, the I_I specification covers the I_{OZ} test for an I/O pin.

Among the device families listed in Table 2, GTLP, VME, FB, and GTL (GTL1655) are fully live insertable. This implies that they have I_{OFF}, PU3S, output disable or enable feature, along with precharge circuits on the backplane port (GTLP/VME/BTL/GTL side). In FB and GTL1655 data sheets, the I_{OZPU} and I_{OZPD} for the BTL and GTL ports are not explicitly tabulated, but they are specified under the live-insertion section as I_O. The test condition of I_O for FB (at BTL port) and GTL1655 (at GTL port) is the same as that of I_{OZPU} and I_{OZPD}.

Power-Up Sequence

Depending on the application's requirement and the device's internal construction, a specific power-up sequence might be required for some devices, while others may not need one. With a clear idea of the different functionalities, such as I_{OFF}, PU3S, and BIAS V_{CC}, the validity of a power-up sequence can be understood.

Some logic device families (for example, GTLP and VME) have full live-insertion capability with I_{OFF}, PU3S, BIAS V_{CC} and output-disable features. To utilize their full live-insertion capabilities, the following power-up sequence should be used: GND, BIAS V_{CC}, disable OE, I/O or the output pin, and last, V_{CC}. The goal is to precharge the output or I/O port up to the middle of the signal swing and disable it before connecting to the live signal. Because these devices have I_{OFF} and PU3S, some other sequences (for example, GND, disable OE, V_{CC}, I/O or output pin, and BIAS V_{CC}) do not damage the device, but data at the bus might be corrupted.

For devices with I_{OFF} and PU3S (for example, LVT and ABT), I/O or output ports can be safely exposed to live signals, with OE disabled. However, this would not ensure data integrity on the bus, momentarily, at the time of card insertion. The two recommended power-up sequences are: GND, V_{CC}, disable OE, I/O or output pins and GND, disable OE, I/O or output pins, V_{CC}.

For devices with only an I_{OFF} specification or without any of the I_{OFF}, PU3S, and precharge specifications (for example, LVC and ALVC), GND and V_{CC} need to be powered up to the recommended operating level before output or I/O ports can be exposed to any live signal. A device output or I/O port can be exposed to a live signal with V_{CC} = 0 V if I_{OFF} is specified for that port. But an input port, with I_{OFF}, can handle a live signal when V_{CC} = 0 V and while V_{CC} is ramping up or ramping down. This is why an input port connection can occur any time after the GND connection in the power-up sequence, if that port has I_{OFF} specified.

TI offers some logic devices with dual power supplies for level-translation applications (for example, SN74LVC4245A). For these devices, one of the two power supplies drives the control circuitry, such as OE, DIR, etc. To avoid excessive supply current and bus contention, the following power-up sequence is recommended: GND, control-side V_{CC}, disable OE, and the other V_{CC}. If OE is to be connected to V_{CC} through a pullup resistor, it should be tied to the control-side V_{CC}.

NOTE: Please refer to the *Texas Instruments Voltage-Level-Translation Devices* application report for more information on the power-up sequence for level-translation devices.[1]

Conclusion

The main objective of this application report is to facilitate a better understanding of the PU3S features of TI logic devices. Hopefully, this will help in the design of more robust systems. While choosing the proper device for the application, careful consideration should be paid to power-up and power-down issues. Systems with multiple power planes from completely different sources add to the complexity. Sometimes, a marginal design without proper consideration for power-up issues works. However, problems can occur when small variations in process are encountered. A minute change well inside the data-sheet limit of a device may cause the system to malfunction.

Common Application Questions

Q1: What can be done if the V_{CC} ramp rate is faster than the recommended V_{CC} ramp rate in the data sheet?

A1: Typically, the ramp rate for a board is in the range of several milliseconds. It is unlikely that the ramp rate will be faster than the microsecond range specified when using the requisite bypass capacitors to stabilize the power line. An easy solution is to add bypass capacitors at the V_{CC} plane to slow down the V_{CC} ramp if it is faster than the recommended V_{CC} ramp rate in the data sheet.

Q2: How can we interpret the recommended V_{CC} ramp-rate parameter in TI logic data sheets?

A2: Please refer to Figure 4 of this application report for the proper interpretation of the ramp-rate parameter. Also, the V_{CC} ramp-rate parameter in the data sheet applies solely to the PU3S circuitry.

Q3: What is the difference between LVC and LVCZ?

A3: In TI standard logic-device nomenclature, Z stands for PU3S circuits. So, LVCZ has PU3S, LVC does not. However, a large majority of TI bus and backplane-interface logic products have PU3S, but are not designated with Z. To be certain, please consult the data sheet for the I_{OZPU} and I_{OZPD} parameters in Table 2 of this application report.

Q4: Is the OE pin sufficient to disable the output buffer of the device if there are no PU3S circuits?

A4: Output-disable circuits are not characterized or tested to operate throughout the entire V_{CC} ramp from 0 V through the operating range. Therefore, OE might not disable the output(s) at low V_{CC}.

References

1. *Texas Instruments Voltage-Level-Translation Devices* application report, literature number SCEA021
2. *Logic in Live Insertion Applications With a Focus on GTLP* application report, literature number SCEA026

Appendix A Test Results

Testing of power-up three-state (PU3S) circuits was done at nominal temperature and voltage. Devices under test were selected randomly from a single-lot trace code and, therefore, do not represent all process variations. All devices tested have a nominal V_{CC} of 3.3 V.

The test setup is shown in Figure A–1. The V_{CC} plane was ramped at various ramp rates to determine the effect of the V_{CC} ramp rate on the device output or I/O structure. I_O was not measured directly; instead, the voltage was measured at the output or I/O terminal (terminal A in Figure A–1) with a 1-MΩ oscilloscope probe.
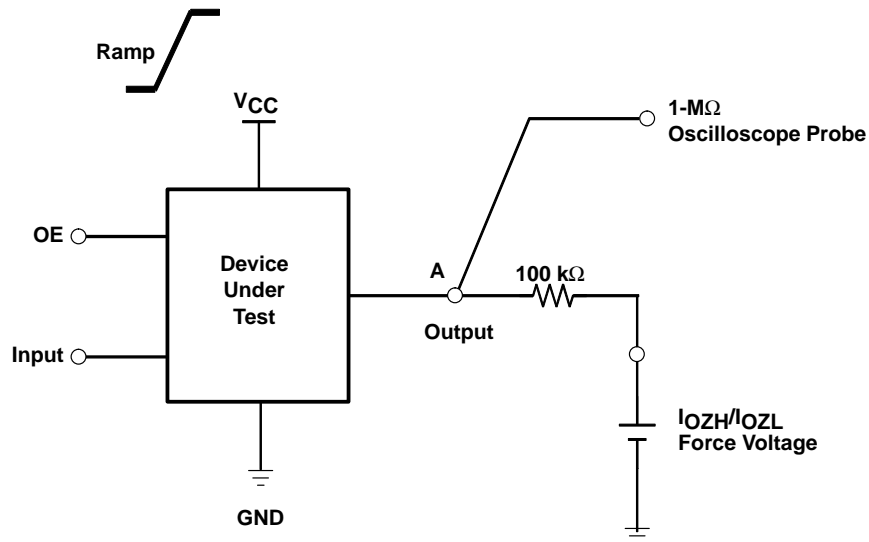

Figure A–1. Test Setup

A 100-kΩ resistor is connected between the output or I/O terminal and the force-voltage source. The objective of this test is to capture the level of V_{CC} at which the PU3S circuit releases its control over the output buffer. From this level of V_{CC} and upward, the OE, input, and DIR pin conditions set the output state. The following tests were performed on each output or I/O port:

- I_{OZL} – OE is biased to the active state. The input is set so that the output activates into the high logic state when enabled. The force voltage is set at 0.5 V (logic low). V_{CC} is ramped from 0 V to 3.3 V, then from 3.3 V to 0 V, while the voltage at terminal A is measured.

- I_{OZH} – OE is biased to the active state. The input is set so that the output activates into the low logic state when enabled. The force voltage is set at 3.0 V (logic high). V_{CC} is ramped from 0 V to 3.3 V, then from 3.3 V to 0 V, while the voltage at terminal A is measured.
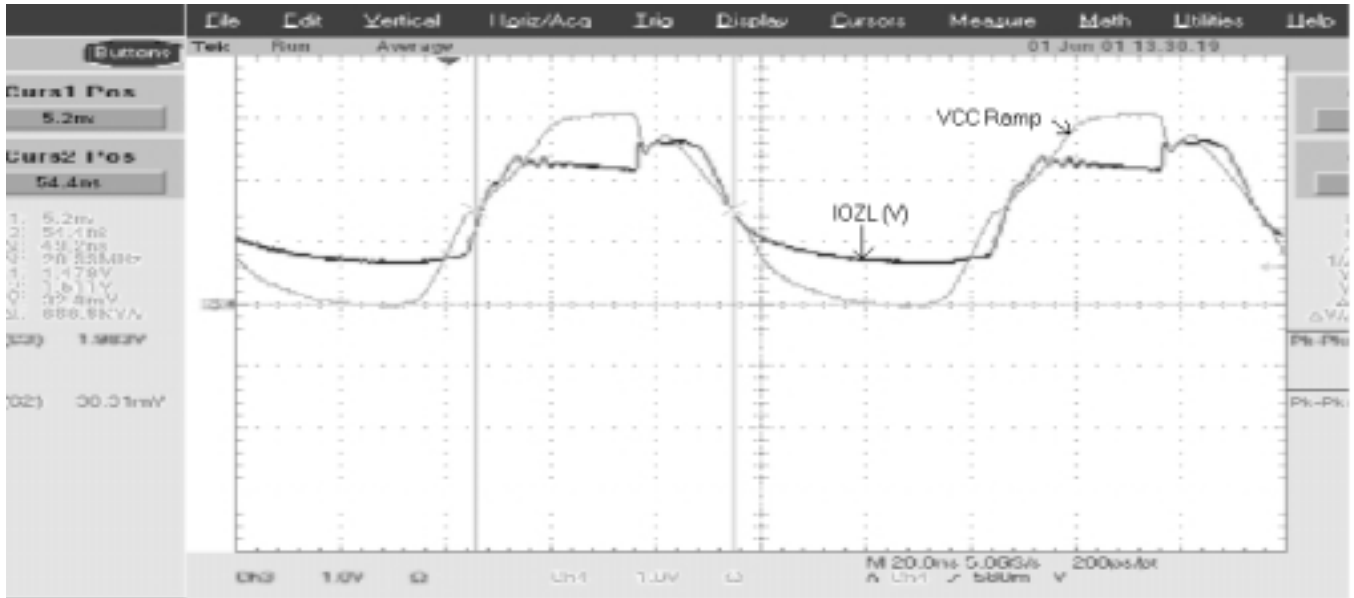
LVT245B Test Results

A series of I_{OZL} and I_{OZH} tests were performed on the LVT245B I/O port at a number of different V_{CC} ramp rates. The two cases shown in Figures A–2, A–3, and A–4 are at the extreme conditions of 150 ms/V and 15 ns/V.

Figure A–2. LVT245B I_{OZL} at 150-ms/V V_{CC} Ramp Rate

Figure A–3. LVT245B I_{OZH} at 150-ms/V V_{CC} Ramp Rate

Figure A–4. LVT245B I_{OZL} at 15-ns/V V_{CC} Ramp Rate

In Figures A–2, A–3, and A–4, the vertical bars denote the data-sheet V_{CC} threshold limit, above which the PU3S should release control of the output(s). Figures A–2 and A–3 show that, at slower ramp rates, the output is going out of high impedance at ~2.3-V V_{CC}. After this V_{CC} level, the output follows the input because OE is enabled. Figure A–4 shows that at faster V_{CC} ramp rates, the output buffer goes out of the high-impedance state much earlier. Also, note that the trip points are the same for both power up and power down.

LVC245A and LVCZ245A Test Results

The LVC245A and LVCZ245A devices were analyzed to show a comparison between the PU3S and OE circuitry. The difference between LVC245A and LVCZ245A is that the "Z" version has PU3S, while the LVC245A does not.

For the LVCZ245A, the same I_{OZL} test described previously, and also another test with the same setup for I_{OZL}, except that OE is disabled, were performed. For the LVC245A, an I_{OZL}-type setup with OE enabled was used.

Figure A–5 shows that, for the LVC245A with OE enabled, the output buffer enters an active state when V_{CC} is much below 1.5 V. However, LVCZ245A enters an active state after 1.5 V due to the PU3S circuits at the output. With OE disabled, LVCZ245A maintains the high-impedance state throughout the V_{CC} ramp. In this case, there is an overlap between the OE and PU3S in terms of disabling the output buffer.
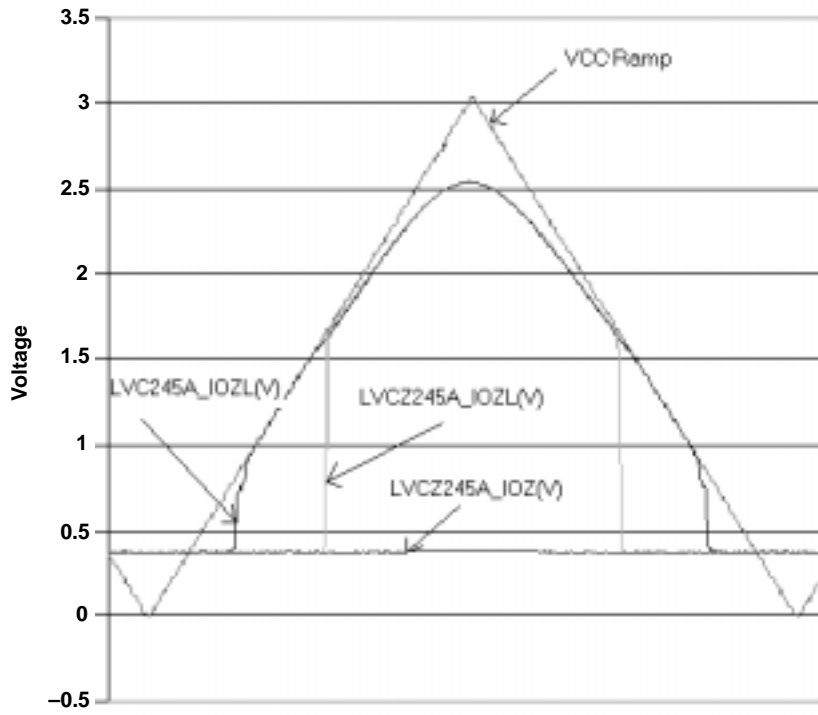
Figure A–5. LVC245A and LVCZ245A Active States vs V$_{CC}$ Ramp

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