*Errata*

# *IWR1843AOP Device Silicon Errata Silicon Revision 1.0*

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# 1 Introduction

This document describes the known exceptions to the functional and performance specifications to TI CMOS Radar Devices (AWR1843AOP).

# 2 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of Radar / mmWave sensor devices. Each of the Radar devices has one of the two prefixes: XIx or IWR1x (for example: **IWR1843A**RBGALP). These prefixes represent evolutionary stages of product development from engineering prototypes (XIx) through fully qualified production devices (IWR1x).

Device development evolutionary flow:

**XIx** — Experimental device that is not necessarily representative of the final device's electrical specifications and may not use production assembly flow.

**IWR1x** — Production version of the silicon die that is fully qualified.

X1x devices are shipped with the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

Texas Instruments recommends that these devices not to be used in any production system as their expected end –use failure rate is still undefined.

# 3 Device Markings

Figure 3-1 shows an example of the IWR1843AOP Radar Device's package symbolization.

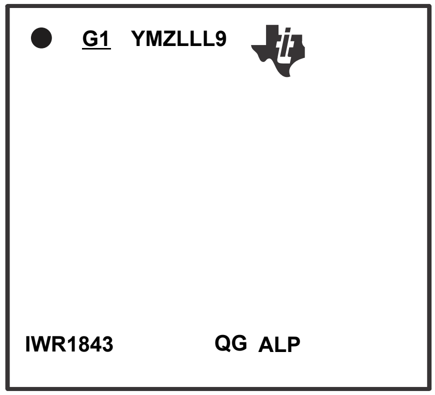



**Figure 3-1. Example of Device Part Markings**

This identifying number contains the following information:

- **Line 1:**
  - G1 = "Green" Package Build (must be underlined)
  - YM = Year/Month Code
  - Z = Assembly Site Code
  - LLL = Assembly Lot Code
  - S = Primary Site Code
  - TI Logo
- **Line 2:**
  - XIWR1843 = IWR1843AOP Device Identifier
  - BG = Safety Level and Security Grade
  - ALP = Package Identifier

# 4 Advisory to Silicon Variant / Revision Map

**Table 4-1. Advisory to Silicon Variant / Revision Map**

| Advisory Number | Advisory Title | IWR1843AOP |
|---|---|---|
| | **Main Subsystem** | |
| MSS#03 | Incorrect Handling of “Saturation” in FFT Hardware Accelerator’s Input / Output Formatter and Statistics Block | X |
| MSS#04A | Number of Samples (SRCACNT) Should be >3 for Correct Operation of FFT Hardware Accelerator | X |
| MSS#05A | Incorrect FFT Intermediate Stage Clip Status Indication | X |
| MSS#13 | Incorrect Read from FFT Hardware Accelerator After Complex Multiplication Operation | X |
| MSS#17 | Invalid Pre-fetch from MSS CR4 Processor (due to Speculative Read Operation from Tightly Coupled Memory Instance) Leads to Generation of MSS_ESM Group 3 Channel 7: MSS_TCMA_FATAL_ERR | X |
| MSS#18 | Core Compare Module (CCM-R4F) may Cause nERROR Toggle After First Reset De-assertion Subsequent to Power Application | X |
| MSS#19 | DMA Read from Unimplemented Address Space may Result in DMA Hang Scenario | X |
| MSS#20 | Radar Frame Stuck due to Missing Synchronizer Logic in Hardware | X |
| MSS#21A | Issue with HWA Input Formatter 16 bit Real Signed Format | X |
| MSS#22 | CAN-FD: Message Transmitted With Wrong Arbitration and Control Fields | X |
| MSS#23 | HWA Read Registers Cannot be Read Reliably When the HWA is Executing a ParamSet Instruction | X |
| MSS#24 | Limitation With Peak Grouping Feature in Hardware Accelerator | X |
| MSS#25 | Debugger May Display Unpredictable Data in the Memory Browser Window if a System Reset Occurs | X |
| MSS#26 | DMA Requests Lost During Suspend Mode | X |
| MSS#27 | MibSPI in Peripheral Mode in 3- or 4-Pin Communication Transmits Data Incorrectly for Slow SPICLK Frequencies and for Clock Phase = 1 | X |
| MSS#28 | A Data Length Error is Generated Repeatedly in Peripheral Mode When IO Loopback is Enabled | X |
| MSS#29 | Spurious RX DMA REQ From a Peripheral Mode MibSPI | X |
| MSS#30 | MibSPI RX RAM RXEMPTY Bit Does Not Get Cleared After Reading | X |
| MSS#31 | CPU Abort Generated on a Write to Implemented CRC Space After a Write to Unimplemented CRC Space | X |
| MSS#32 | DMMGLBCTRL BUSY Flag Not Set When DMM Starts Receiving A Packet | X |
| MSS#33 | MibSPI RAM ECC is Not Read Correctly in DIAG Mode | X |
| MSS#34 | HS Device Does Not Reboot Successfully on Warm Reset Getting Triggered by Watchdog Expiry | X |
| MSS#35 | EDMA TPTC Generates an Incorrect Address on the Read Interface, Causing one or More Data Integrity Failures, Hangs, or Extra Reads | X |
| MSS#37B | DCC Module Frequency Comparison can Report Erroneous Results | X |
| MSS#38A | GPIO Glitch During Power-Up | X |
| MSS#39 | The state of the MSS DMA is left pending and uncleared on any DMA MPU fault | X |
| MSS#40 | Any EDMA Transfer That Spans ACCEL_MEM1 +ACCEL_MEM2 Memories of Hardware Accelerator May Result In Data Corruption Without Any Notification Of Error From The SoC | X |
| MSS#42 | DSP L2 memory initialisation can reoccur on execution DSP self test (STC) OR DSP Power cycling execution by application. | X |
| MSS#43A | Read-data from internal registers of PCR is not reliable. Shared PCS region protection is also not supported | X |
| MSS#44 | SYNC IN input pulse wider than 4usec can cause a FRC lockstep error | X |
| MSS#45 | Bootup failure during the serial flash busy state | X |
| | **Analog / Millimeter Wave** | |
| ANA#08A | Doppler Spur Observed at Certain RF Frequencies | X |
| ANA#09A | Synthesizer Frequency Nonlinearity around 76.8 GHz when Synthesizer (Chirp) Frequency Monitor Enabled | X |
| ANA#10 | Unreliable Readings from Synthesizer Supply Voltage Monitor | X |
| ANA#11A | TX, RX Gain Calibrations Sensitive to Large External Interference | X |

**Table 4-1. Advisory to Silicon Variant / Revision Map (continued)**

| Advisory Number | Advisory Title | IWR1843AOP |
|---|---|---|
| ANA#12A | Second Harmonic (HD2) Present in the Receiver | X |
| ANA#13B | TX1 to TX3 Phase Mismatch Variation over Temperature is Double that of TX2/TX1 and TX3/TX2 Combinations | X |
| ANA#15 | Excessive TX-RX Coupling or Reflection can Lead to Saturated RX Output | X |
| ANA#16 | LVDS Coupling to Clock System | X |
| ANA#17A | On-Board Supply Ringing Induced Spur | X |
| ANA#18B | Spurs Caused due to Digital Activity Coupling to XTAL | X |
| ANA#20 | Occasional Failures Observed During Calibration of the Radar Subsystem | X |
| ANA#21B | Out of Band Radiated Spectral Emission | X |
| ANA#22A | Overshoot and Undershoot During Inter-Chirp Idle Time | X |
| ANA#24A | 40-MHz OSC CLKOUT Causing Spurs in 2D-FFT Spectrum | X |
| ANA#27 | Digital Temperature Sensor Having Higher Error | X |
| | **Package** | |
| PACKAGE#02A | Surface Wave Artifact from PCB | X |

# 5 Known Design Exceptions to Functional Specifications

**MSS#03** ***Incorrect Handling of “Saturation” in FFT Hardware Accelerator’s Statistics Block***

**Revision(s) Affected:**

**Description:**

- Input formatter block performs saturation based on signed or unsigned samples. However, the compute engine module always saturates the input as a 24 bit signed number.
- Output formatter block saturates the 16 bits unsigned number as signed number. This causes magnitude outputs to have a smaller max range.
- Statistics block always assumes that input is signed when checking for saturation, but the input can be unsigned in some cases.

**Workaround(s):** None.

**MSS#04A** ***Number of Samples (SRCACNT) Should be >3 for Correct Operation of FFT Hardware Accelerator***

**Revision(s) Affected:**

**Description:** Logic which subtracts the compute engine pipelined delay from FFT counter wraps around incorrectly when the number of samples is less (specifically, when it is 3).

**Workaround(s):** FFT engine should not be used with FFT counter value < 4.

**MSS#05A** ***Incorrect FFT Intermediate Stage Clip Status Indication***

**Revision(s) Affected:**

**Description:** FFT clip status register incorrectly uses all butterfly stages, even if only a few of the stages are enabled.

**Workaround(s):** Do not use the HWA FFT Intermediate Stage Clip status indication

**MSS#13** ***Incorrect Read from FFT Hardware Accelerator After Complex Multiplication Operation***

**Revision(s) Affected:**

**Description:** Read-back from FFT hardware accelerator peripheral, static configuration registers, Window RAM, Param RAM, and First stage RAM gives incorrect data if the last operation performed by the accelerator was a complex multiplication.

**Workaround(s):** None.

### MSS#17 — *Invalid Pre-fetch from MSS CR4 Processor (due to Speculative Read Operation from Tightly Coupled Memory Instance) Leads to Generation of MSS_ESM Group 3 Channel 7: MSS_TCMA_FATAL_ERR*

**Revision(s) Affected:**

**Description:** The CR4 processor may perform an invalid pre-fetch access due to speculative TCM read leading to an invalid address access. This can result in a TCERROR and also a 2-bit ECC fatal error. The TCERROR is ignored by the processor since these correspond to instructions that are pre-fetched but never executed. However, the invalid MSS_TCMA_FATAL_ERR is generated on the ESM group3 channel-7.

*Implication: In case of a genuine TCMA ECC fatal error, nERROR will not be generated directly through ESM.*

**Workaround(s):** Mask Group 3 channel 7: MSS_TCMA_FATAL_ERR to ESM can be masked by writing into MSS_RCM:ESMGATE0 register. CR4F abort handler should handle the nERROR generation

OR

Disable branch prediction for MSS-CR4F

### MSS#18 — *Core Compare Module (CCM-R4F) may Cause nERROR Toggle After First Reset De-assertion Subsequent to Power Application*

**Revision(s) Affected:**

**Description:** The CCM-R4F module compares the outputs of the two Cortex-R4F CPU cores and generates an error on any mis-compare. This ensures the lock-step operation of the two Cortex-R4F CPUs. The nERROR signal should only be set by the CCM-R4 module by a valid core mismatch. At power-on, some uninitialized circuits may cause the CCMR4-F to falsely detect a mis-compare.

**Workaround(s):** The anomalous nERROR toggle would need to be ignored by the external monitoring circuit (if deployed).

### MSS#19 — *DMA Read from Unimplemented Address Space may Result in DMA Hang Scenario*

**Revision(s) Affected:**

**Description:** The MSS DMA generates a BER (Bus Error) interrupt when the DMA detects a bus error due to a read from unimplemented address space. This interrupt is available on VIM Interrupt Channel-70 for DMA1 and VIM Interrupt Channel-51 for DMA2 .This read from unimplemented address space results in a hang condition in the DMA infrastructure bridge that connects it to the main interconnect.

*Implication: A DMA read from an unimplemented address can result in a DMA hang condition. In the resulting state the DMA will not respond to any further DMA requests.*

**Workaround(s):** The MSS CR4F processor will have to invoke a warm reset or generate an nERROR if it receives a DMA BER error.

### MSS#20 — *Radar Frame Stuck due to Missing Synchronizer Logic in Hardware*

**Revision(s) Affected:**

**MSS#20** (continued) ***Radar Frame Stuck due to Missing Synchronizer Logic in Hardware***

**Description:** Radar Sub System Internal Frame Clock is triggered by rlSensorStart API which starts the Radar Frame. Occasionally the rlSensorStart API does not trigger the clock due to missing synchronizer logic in hardware.

*Implication: A DMA read from an unimplemented address can result in a DMA hang condition. In the resulting state the DMA will not respond to any further DMA requests.*

**Workaround(s):** The issue is frequent if FRC clock source is changed. Ensure that FRC Clock source is not changed.

**MSS#21A** ***Issue with HWA Input Formatter 16 bit Real Signed Format***

**Revision(s) Affected:**

**Description:** Wrong sign extension is implemented for 16 bit signed format in real only mode operation. Hence, signed 16-bit real format cannot be supported for input formatter.

**Workaround(s):** Don’t use the 16 bit signed format in real only mode with HWA

## MSS#22 *CAN-FD: Message Transmitted With Wrong Arbitration and Control Fields*

**Revision(s) Affected:**

**Description:**

Under the following conditions a message with wrong ID, format, and DLC is transmitted:

- M_CAN is in state "Receiver" (PSR.ACT = "10"), no pending transmission
- A new transmission is requested before the 3rd bit of Intermission is reached
- The CAN bus is sampled dominant at the third bit of Intermission which is treated as SoF (see ISO11898-1:2015 Section 10.4.2.2)

Under the conditions listed above it may happen, that:

- The shift register is not loaded with ID, format, and DLC of the requested message
- The M_CAN will start arbitration with wrong ID, format, and DLC on the next bit
- In case the ID wins arbitration, a CAN message with valid CRC is transmitted
- In case this message is acknowledged, the ID stored in the Tx Event FIFO is the ID of the requested Tx message and not the ID of the message transmitted on the CAN bus, no error is detected by the transmitting M_CAN

The erratum is limited to the case when M_CAN is in state "Receiver" (PSR.ACT = "10") with no pending transmission and a new transmission is requested before the 3rd bit of Intermission is reached and this 3rd bit of intermission is seen dominant.

When a transmission is requested by the CPU, the Tx Message Handler performs an internal arbitration and loads the pending transmit message with the highest priority into its output buffer and then sets the transmission request for the CAN Protocol Controller. The problem occurs only when the transmission request for the CAN Protocol Controller is activated between the sample points of the 2nd and 3rd bit of Intermission and if that 3rd bit of intermission is seen dominant.

This dominant level at the 3rd bit of Intermission may result from an external disturbance or may be transmitted by another node with a significantly faster clock.

In the described case it may happen that the shift register is not loaded with arbitration and control field of the message to be transmitted. The frame is transmitted with wrong ID, format, and DLC but with the data field of the requested message. The message is transmitted in correct CAN (FD) frame format with a valid CRC.

If the message loses arbitration or is disturbed by an error, it is retransmitted with correct arbitration and control fields.

**Workaround(s):**

Request a new transmission only if another transmission is already pending or when the M_CAN is not in state "Receiver" (when PSR.ACT ≠ "10").

Another option would be to add a checksum to the data field covering arbitration and control fields of the message to be transmitted.

### MSS#23 — *HWA Read Registers Cannot be Read Reliably When the HWA is Executing a ParamSet Instruction*

**Revision(s) Affected:**

**Description:** Any read from the HWA configuration or status registers can be corrupted, if the read access is performed when the HWA is active. Reads from the HWA registers can be performed correctly, only after the execution of the entire ParamSet (i.e., after the ACC_DONE_INTR interrupt) or when the HWA is in IDLE mode waiting for the trigger to the start the execution of the next ParamSet instruction.

**Workaround(s):** Perform the following:

- Read-back of signature registers: Software needs to maintain a soft copy of the one-hot encoded signature registers and use that copy location for the EDMA programming.
- Read-back of static registers on the HWA ParamSet interrupt. There is no reliable way to read the HWA static registers, if the HWA is active.
- Read-back of Debug/status registers: The User can only read these registers when the HWA is ***not*** active.

**MSS#24** ***Limitation With Peak Grouping Feature in Hardware Accelerator***

**Revision(s) Affected:**

**Description:** Peak is declared only if the cell under test is greater than its most immediate neighboring cells to its left and right. In the case where CFAR qualified peaks in the two adjacent cells happen to be equal in magnitude, enabling peak grouping can lead to the peak being lost.

**Workaround(s):** Do not enable the peak grouping feature in the hardware accelerator.

**MSS#25** ***Debugger May Display Unpredictable Data in the Memory Browser Window if a System Reset Occurs***

**Revision(s) Affected:**

**Description:** If a system reset (nRST goes low) occurs while the debugger is performing an access on the system resource using system view, a peripheral error should be replied to the debugger. If the access was a read, instead the response might indicate that the access completed successfully and return unpredictable data.

This issue occurs under this condition: when a system reset is asserted (nRST low) on a specific cycle, while the debugger is completing an access on the system, using the system view. An example would be, when a debugger, like the CCS-IDE memory browser window, is refreshing content using the system view. This is not an issue for a CPU only reset and, this is not an issue during a power-on-reset (nPORRST) either.

**Workaround(s):** Avoid performing debug reads and writes while the device might be in reset.

**MSS#26** ***DMA Requests Lost During Suspend Mode***

**Revision(s) Affected:**

**Description:** While the device is halted in suspend mode by the debugger, the DMA is expected to complete the remaining transfers of a block, if the DEBUG MODE bit field of the GCTRL register is configured to '01'. Instead, the DMA does not complete the remaining transfers of a block but, rather stops after two more frames of data are transferred. Subsequent DMA requests from a peripheral to trigger the remaining frames of a block can be lost.

This issue occurs only in the following conditions:
- The device is suspended by a debugger
- A peripheral continues to generate requests while the device is suspended
- The DMA is setup to continue the current block transfer during suspend mode with the DEBUG MODE bit field of the GCTRL register set to '01'
- The request transfer type TTYPE bit in the CHCTRL registers is set to frame trigger ('0')

**Workaround(s):** **Workaround #1:**

Use TTYPE = block transfer ('1'), when the DEBUG MODE bit field is '01' (*finish current block transfer*)

***or***

**Workaround #2:**

Use the DMA DEBUG MODE = '00' (ignore suspend), when using TTYPE = frame transfer ('0') to complete the block transfer, even after suspend/halt is asserted.

### MSS#27 — *MibSPI in Peripheral Mode in 3- or 4-Pin Communication Transmits Data Incorrectly for Slow SPICLK Frequencies and for Clock Phase = 1*

**Revision(s) Affected:**

**Description:** The MibSPI module, when configured in multibuffered peripheral mode with 3-functional pins (CLK, SIMO, SOMI) or 4-functional pins (CLK, SIMO, SOMI, nENA), could transmit incorrect data when all the following conditions are met:

- MibSPI module is configured in multibuffered mode,
- Module is configured to be a peripheral in the SPI communication,
- SPI communication is configured to be in 3-pin mode or 4-pin mode with nENA,
- Clock phase for SPICLK is 1, and
- SPICLK frequency is MSS_VCLK frequency / 12 or slower

**Workaround(s):** The issue can be avoided by setting the CSHOLD bit in the control field of the TX RAM (Multi-Buffer RAM Transmit Data Register). The nCS is not used as a functional signal in this communication; hence, setting the CSHOLD bit does not cause any other effect on the SPI communication.

## MSS#28 *A Data Length Error is Generated Repeatedly in Peripheral Mode When IO Loopback is Enabled*

**Revision(s) Affected:**

**Description:** When a DLEN error is created in Peripheral mode of the SPI using nSCS pins in IO Loopback Test mode, the SPI module re-transmits the data with the DLEN error instead of aborting the ongoing transfer and stopping. This is only an issue for an IOLPBK mode Peripheral in Analog Loopback configuration, when the intentional error generation feature is triggered using CTRLDLENERR (IOLPBKTSTCR.16).

**Workaround(s):** After the DLEN_ERR interrupt is detected in IOLPBK mode, disable the transfers by clearing the SPIEN (bit 24) in the SPIGCR1 register and then, re-enable the transfers by resetting the SPIEN bit.

**MSS#29** ***Spurious RX DMA REQ From a Peripheral Mode MibSPI***

**Revision(s) Affected:**

**Description:** A spurious DMA request could be generated even when the SPI peripheral is not transferring data in the following condition sequence:

- The MIBSPI is configured in standard (non-multibuffered) SPI mode, as a peripheral
- The DMAREQEN bit (SPIINT0.16) is set to enable DMA requests
- The Chip Select (nSCS) pin is in an active state, but no transfers are active
- The SPI is disabled by clearing the SPIEN (SPIGCR1.24) bit from '1' to '0'

The above sequence triggers a false request pulse on the Receive DMA Request as soon as the SPIEN bit is cleared from '1' to '0'.

**Workaround(s):** Whenever disabling the SPI, by clearing the SPIEN bit (SPIGCR1.24), first clear the DMAREQEN bit (SPIINT0.16) to '0', and then, clear the SPIEN bit.

### MSS#30 — *MibSPI RX RAM RXEMPTY bit Does Not Get Cleared After Reading*

**Revision(s) Affected:**

**Description:** The RXEMPTY flag may not be auto-cleared after a CPU or DMA read when the following conditions are met:

- The TXFULL flag of the latest buffer that the sequencer read out of transmit RAM for the currently active transfer group is 0,
- A higher-priority transfer group interrupts the current transfer group and the sequencer starts to read the first buffer of the new transfer group from the transmit RAM, and
- Simultaneously, the Host (CPU/DMA) is reading out a receive RAM location that contains valid received data from the previous transfers.

**Workaround(s):** If at all possible, avoid transfer groups interrupting one another.

If dummy buffers are used in lower-priority transfer groups, select the appropriate "BUFMODE" for them (like, SKIP/DISABLED) unless, there is a specific need to use the "SUSPEND" mode.

**MSS#31** ***CPU Abort Generated on a Write to Implemented CRC Space After a Write to Unimplemented CRC Space***

**Revision(s) Affected:**

**Description:** An abort could be generated on a write to a legal address in the address offset region (0x0000–0x01FF) of the CRC register space when a normal mode write to an unimplemented address region (0x0200–0xFFFF) of the CRC register space is followed by a write to a legal address region (0x0000–0x01FF) of the CRC register space.

**Workaround(s):** None.

## MSS#32 — *DMMGLBCTRL BUSY Flag Not Set When DMM Starts Receiving A Packet*

**Revision(s) Affected:**

**Description:** The BUSY flag in the DMMGLBCTRL register should be set when the DMM starts receiving a packet or has data in its internal buffers. However, the BUSY flag (DMMGLBCTRL.24) may not get set when the DMM starts receiving a packet under the following condition:

- The BUSY bit is set only after the packet has been received, de-serialized, and written to the internal buffers. It stays active while data is still in the DMM internal buffers. If the internal buffers are empty (meaning that no data needs to be written to the destination memory) then, the BUSY bit will be cleared.

**Workaround(s):** Wait for a number of DMMCLK cycles (for example, 95 DMMCLK cycles) beyond the longest reception and deserialization time needed for a given packet size and DMM port configuration, before checking the status of the BUSY flag, and after the DMM ON/OFF bit field (DMMGLBCTRL.[3:0]) has been programmed to OFF.

**MSS#33** ***MibSPI RAM ECC is Not Read Correctly in DIAG Mode***

**Revision(s) Affected:**

**Description:** A Read operation to the ECC address space of the MibSPI RAM in DIAG mode, does not return the correct ECC value for the first 128 buffers, if the Extended Buffer support is implemented but, the Extended Mode is disabled for the particular MibSPI instance.

**Workaround(s):** None.

**MSS#34** ***HS Device Does Not Reboot Successfully on Warm Reset Getting Triggered or With Internal Software Reset***

**Revision(s) Affected:**

**Description:** A warm reset triggered by a watchdog expiry (MSS Wdog) , a software register write (SOFTSYSRST), or an external warm reset pin does not ensure a successful reboot of the device in a secure device (HS device).

**Workaround(s):** A warm reset should not be triggered externally or internally by a watchdog expiry, a software write, or other trigger mechanisms.

To initiate a reset cycle, external circuitry should be used on the sensor design. The external circuitry uses the watchdog, nERROR OUT monitoring, or other kinds of GPIO signaling to trigger a reset using the nRST pin of the device.

## MSS#35 *EDMA TPTC Generates an Incorrect Address on the Read Interface, Causing one or More Data Integrity Failures, Hangs, or Extra Reads*

**Revision(s) Affected:**

**Description:** Certain scenarios could lead to an incorrect read, hang, or data integrity issues in the EDMA TPTC block. Table 5-1 shows the various scenarios and the resulting effects of each scenario.

A scenario happens, if *ALL* conditions listed for that scenario are satisfied (true); that is, "AND" of all conditions.

A “hang” outcome means that one or more attempts of the hang causing scenarios can progressively lead to not receiving a "transfer completion" indication from the TPTC. The last transfer attempt which does not receive the completion indication can be any transfer – any scenario transfer within this advisory or even outside of this advisory.

**Table 5-1. EDMA TPTC Scenario IDs and Condition Results**

| SCENARIO ID | CONDITIONS | DATA INTEGRITY FAILURES | HANGS | EXTRA READS |
|---|---|---|---|---|
| 1 | AB-sync<br>BCNT > 1<br>ACNT not in [2,4,8,16,32]<br>(ACNT < 64) OR ((ACNT = 64) AND (SRCBIDX != ACNT))<br>Source Addressing crossing 4-KB boundary for any of the BCNT number of ACNT transfers. | Yes (see Figure 5-4) | Possible | Possible |
| 2 | AB-sync with BCNT=1 or A-sync<br>ACNT not in [2..24, 32]<br>ACNT <= 64<br>Source Addressing crossing 4-KB boundary for any of the BCNT number of ACNT transfers. | No | Possible | Yes |
| 3 | AB-sync with BCNT=1 or A-sync<br>ACNT in [2..24, 32]<br>Source Addressing crossing 4-KB boundary for any of the BCNT number of ACNT transfers. | No | No | Yes (see Figure 5-1) |
| 4 | AB-sync<br>BCNT > 1<br>ACNT in [2,4,8,16,32]<br>SRCBIDX = ACNT<br>ACNT * BCNT <=64<br>Source Addressing crossing 4-KB boundary for any of the BCNT number of ACNT transfers. | No | No | Yes (see Figure 5-2) |
| 5 | AB-sync<br>BCNT > 1<br>ACNT in [2,4,8,16,32]<br>SRCBIDX = ACNT<br>ACNT * BCNT <=64<br>Source Addressing *does NOT* cross 4-KB boundary for any of the BCNT number of ACNT transfers; that is, NOT of<br>Source Addressing crosses 4-KB boundary for merged source array of size ACNT * BCNT. | No | No | Yes (see Figure 5-3) |

Source Addressing crossing 4-KB boundary cross **condition [1]** in Table 5-1 is defined as follows:
[X(i) = LSB_12bits(SRC_ADDR + i * SRC_BIDX)] + ACNT > 0x1000
where 0 <= i < BCNT

Source Addressing crossing 4-KB boundary cross **condition [2]** in Table 5-1 is defined as follows:
LSB_12bits(SRC_ADDR) + (ACNT * BCNT) > 0x1000

## MSS#35 (continued) *EDMA TPTC Generates an Incorrect Address on the Read Interface, Causing one or More Data Integrity Failures, Hangs, or Extra Reads*

For the and expressions above, note that the SRC_ADDR is candidate source address considering the C-dimension. If CCNT > 1, then, the SRC_ADDR would be every candidate source address for all CCNTs depending on the type of transfer and the SRCCIDX.

For each extra read in **Scenario ID #3** for which Condition [1] is applicable, each index i above that satisfies the condition results in extra read from starting address SRC_ADDR + (i + 1) * SRCBIDX and of length equal to the distance from the start address to the boundary [that is, 0x1000 – X(i)]. Note: length < ACNT.

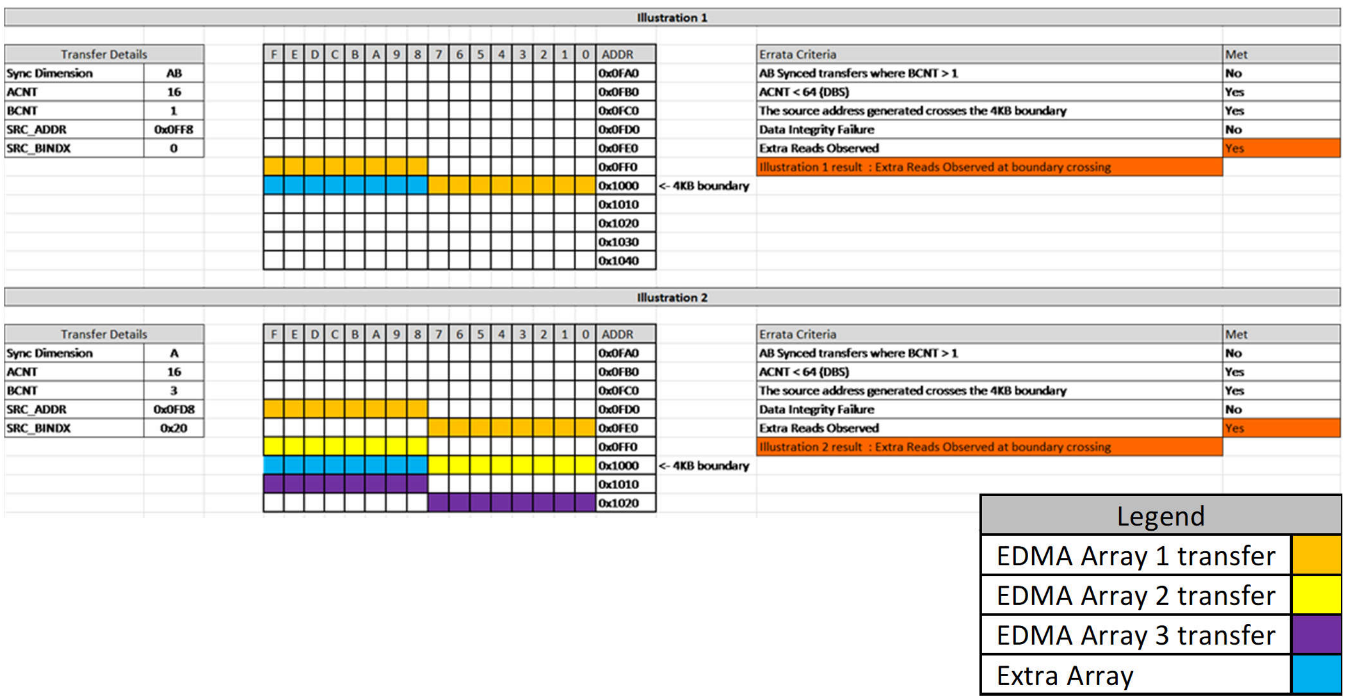



**Figure 5-1. Scenario ID #3 – Extra Reads**

**MSS#35** (continued) ***EDMA TPTC Generates an Incorrect Address on the Read Interface, Causing one or More Data Integrity Failures, Hangs, or Extra Reads***

For each extra read **Scenario ID #4** in for which Condition [1] is applicable, there is an extra read from starting address SRC + BCNT * ACNT (=SRCBIDX) of length equal to the distance of the start address to the boundary [that is, length is 0x1000 – X(i)], where i is the index of one and only 4-KB boundary crossing condition. Note: length < ACNT.

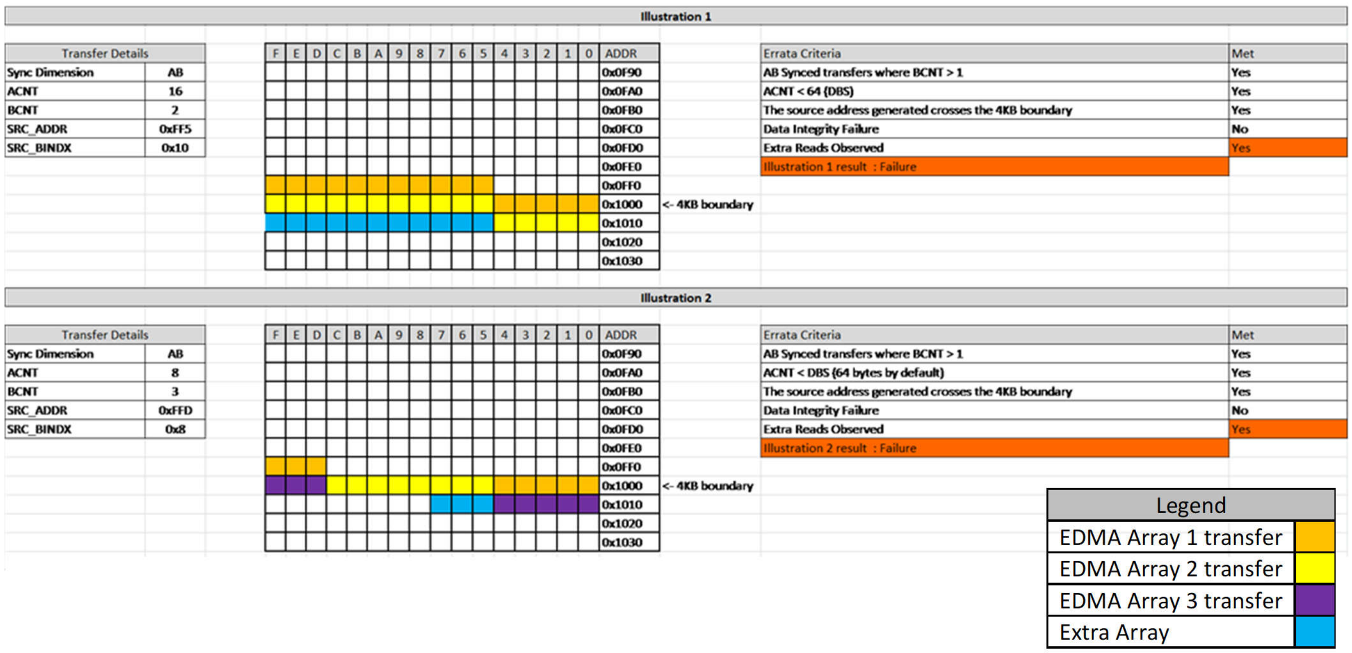



**Figure 5-2. Scenario ID #4 – Extra Reads**

**MSS#35** (continued) ***EDMA TPTC Generates an Incorrect Address on the Read Interface, Causing one or More Data Integrity Failures, Hangs, or Extra Reads***

For the extra read **Scenario ID #5** in for which Condition [2] is applicable, there is an extra read from starting address SRC + BCNT * ACNT (=SRCBIDX) of length equal to the distance of the start address and is of length ACNT.

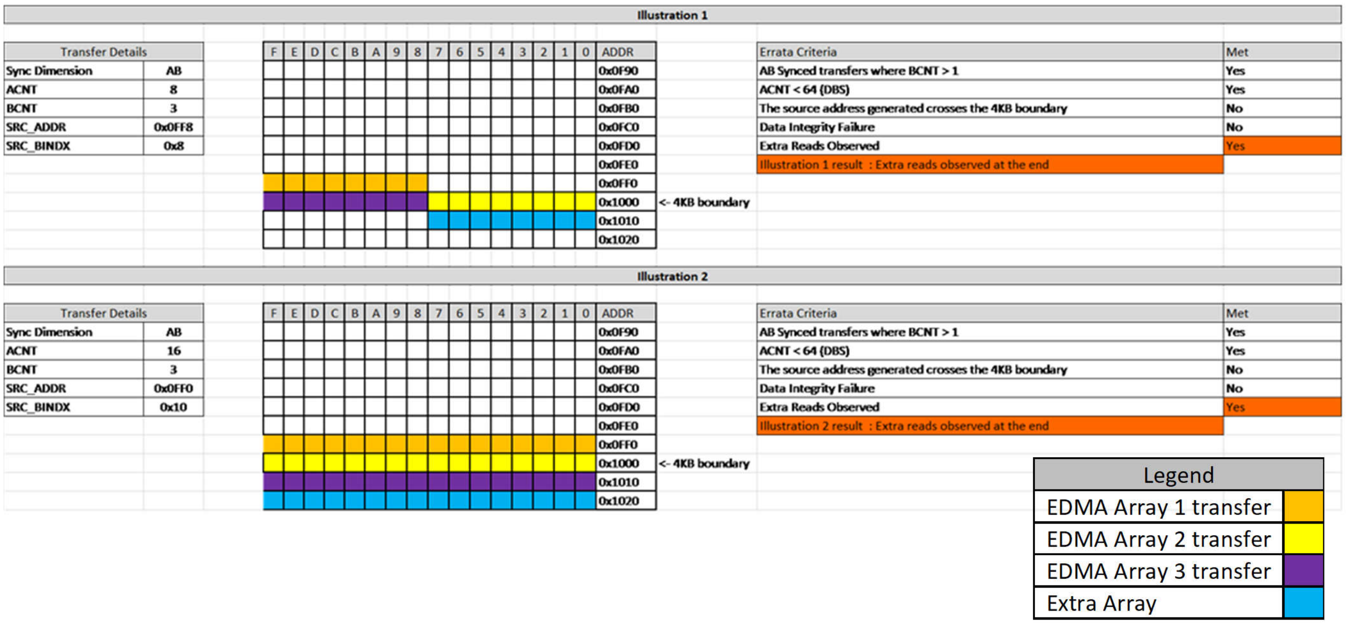



**Figure 5-3. Scenario ID #5 – Extra Reads**

## MSS#35 (continued) *EDMA TPTC Generates an Incorrect Address on the Read Interface, Causing one or More Data Integrity Failures, Hangs, or Extra Reads*

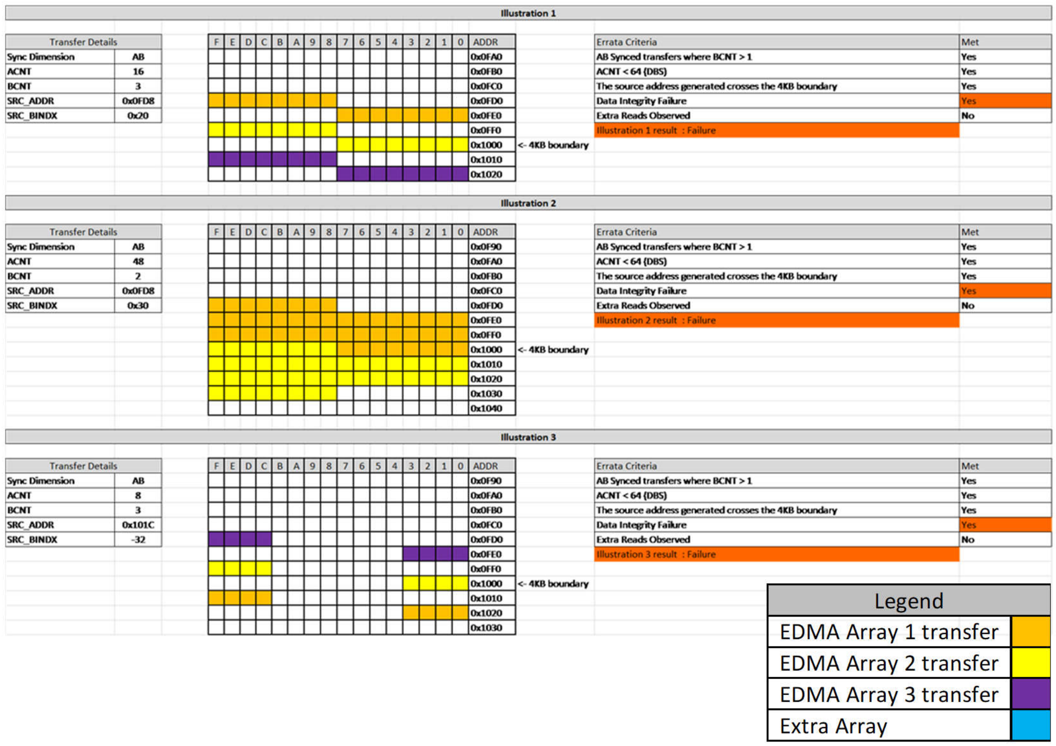



**Figure 5-4. Scenario ID #1 – Data Integrity Failure**

**Workaround(s):**

**Workaround #1 - ALL SCENARIO IDs (see Table 5-1)**

Prevent one or more of the conditions necessary for the problematic scenarios to happen.

**Workaround #2 - Scenario ID #3, Scenario ID #4, and Scenario ID #5 (see Table 5-1)**– EXTRA READS

For **Scenario ID #3, Scenario ID #4, and Scenario ID #5**– EXTRA READS, another workaround besides avoiding the 4-KB boundary cross conditions, is to ensure that buffers involved in this kind of transfer are positioned so that extra reads stay within the physical memory boundaries. If the extra reads go to Reserved space *or* space blocked by the Memory Protection Unit (MPU), the TPTC generates a bus error interrupt to the processor.

**MSS#37B** ***DCC Module Frequency Comparison can Report Erroneous Results***

**Revision(s) Affected:**

**Description:** The Dual-clock Comparator module, which is used to monitor a clock frequency while comparing with a known clock reference, could stop earlier than expected, and, thus, indicating the measured clock frequency to be lower. This is due to a clock domain crossing issue causing a preset to the error detection logic to get triggered.

**Workaround(s):** Multiple measurements can be taken for the same clock pairs and abnormal frequencies reported can be ignored

Application code, where possible, could compare the clocks using an alternate clock comparator module (CCC).

### MSS#38A *GPIO Glitch During Power-Up*

**Revision(s) Affected:**

**Description:** During the 3.3-V supply ramp, the GPIO outputs could possibly see a short glitch (*rising above the 0 V for a short duration*), if the 3.3V supply powers up before the 1.8V supply. This GPIO glitch cannot be avoided by just a pulldown resistor. If the GPIO glitch during boot-up is high enough, it could be falsely detected as a “high”.

**Workaround(s):** Powering up the 1.8V supply before the 3.3V supply resolved the issue. Incase that is not feasible, AND the GPIO is used for critical controls where glitch cannot be tolerated, the GPIO output should be gated by the nRESET signal of the xWR device.

Using a tri-state buffer (for example: SN74LVC1G126-Q1) externally to isolate the GPIO output from the system until the nRESET of xWR device is released. At this point, all the supplies are expected to be stable.

## MSS#39 *The state of the MSS DMA is left pending and uncleared on any DMA MPU fault*

**Revision(s) Affected:**

**Description:** The state of the MSS DMA is left pending and uncleared on any DMA MPU fault. The transfer that caused this MPU fault is left pending inside the DMA IP.

Any trigger on DMA REQ lines (could be caused by any module/IP that is hooked up to DMA in h/w) can re-trigger DMA to start executing the above pending transfer irrespective of whether that trigger is actually valid/enabled in DMA or that module/IP

**Workaround(s):** For devices where the Boot ROM is executing the MSS DMA MPU Self tests. As part of application initialization, if the MSS DMA will be used, the following register field should be used to reset the MSS DMA IP so that the uncleared transfer is reset

1. Write MSS_RCM:SOFTRST1[31:24] 0xAD
2. Write MSS_RCM:SOFTRST1[31:24] 0x0

It is not recommended to use this configuration at any another instance other than that recommended here in this Errata.

On an actual Real time MPU Error, this error should be treated as a non-recoverable error and a warm reset should be issued to recover.

**MSS#40** ***Any EDMA Transfer That Spans ACCEL_MEM1 +ACCEL_MEM2 Memories of Hardware Accelerator May Result In Data Corruption Without Any Notification Of Error From The SoC***

**Revision(s) Affected:**

**Description:** As per TPTC IP Spec, a Transfer request (TR) is supposed to access a single peripheral end point. ACCEL_MEM0/ACCEL_MEM1 memory banks of HWA are available via single peripheral point and ACCEL_MEM2/ ACCEL_MEM3 memory banks of HWA are available as another peripheral point (different from that of ACCEL_MEM0/ ACCEL_MEM1). Hence if a single TR is used to access a buffer spanning ACCEL_MEM1 and ACCEL_MEM2 memories of the HWA (i.e. a single buffer spanning 2 different peripheral points), the spec is not being adhered to. This errata is explicitly highlighting this spec requirement

**Workaround(s):** Split the access into 2 TRs so that a single TR does not span ACCEL_MEM1 +ACCEL_MEM2. The 2 TRs can be chained.

**MSS#42** ***DSP L2 memory initialisation can reoccur on execution DSP self test (STC) OR DSP Power cycling execution by application.***

**Revision(s) Affected:**

**Description:** MSS Boot ROM Powers on DSP, Performs a Memory Initialisation of DSP L2 and downloads the program code to L2 memory. If the user application executes the STC or DSP power cycle, memory init is triggered again, hence erasing the L2 memory contents.

**Workaround(s):** The workaround for Mem init would be to perform a Dummy mem init to reset a latch within the IP while keeping the destination domain in reset. This can be done by the application using the below sequence before running STC or DSP power cycling:

1. Set the GEM_CLK_EN_BYPASS_CTRL bit in the TOPRCM-> GEMPWRSMCFG2 register Bit 7 as ‘1’.
2. Set the GEM_GRSTN_GATE_BYPASS_CTRL bit in the TOPRCM-> GEMPWRSMCFG1 Bit 9 register as ‘1’.
3. Write a value of 0xFFFF in , DSS_REG ->L2MEMINITCFG1 register.
4. Write a value of 0xF in , DSS_REG ->L2MEMINITCFG2 register
5. Write a value of 0x0 in TOPRCM-> GEMPWRSMCFG1-> PWRSMOUTBYPCTRL register.

**MSS#43A** ***Read-data from internal registers of PCR is not reliable. Shared PCS region protection is also not supported***

**Revision(s) Affected:**

**Description:** The main subsystem has PCR interconnect that manages the accesses to the peripheral registers and peripheral memories, and provides a global reset for all peripherals. The read-data from PCR is getting corrupted before handing it of to VBUSP interconnect. So any partial write to PCR-registers is not reliable. Peripheral access is blocked by writing to internal registers which is not feasible.

Shared PCS region protection is also not supported

**Workaround(s):** None.

## MSS#44 — *SYNC IN input pulse wider than 4usec can cause a FRC lockstep error*

**Revision(s) Affected:**

**Description:** In hardware based frame triggered mode of operation, external SYNC IN pulse is provided to the radar device. If the width of the pulse if > 4usec, it could cause MSS ESM group 1 fault with FRC lockstep error.

**Workaround(s):** The pulse width of the external SYNC IN signal should be >25nsec and < 5usec

**MSS#45** ***Bootup failure during the serial flash busy state***

| | |
|---|---|
| **Revision(s) Affected:** | |
| **Description:** | If the radar device is rebooted internally or externally while the serial flash is busy completing a previous operation, like erase, format etc, the radar device might fail to bootup since the serial flash would not respond to the commands from the bootloader during the bootup process. |
| **Workaround(s):** | The user application should make sure if its triggering an internal reset due to watch dog expiry or other reasons, it should reset the serial flash to bring it to a known state or wait for completion of any pending issued commands to serial flash before it resets the IWR device. |

### ANA#08A — *Doppler Spur Observed at Certain RF Frequencies*

**Revision(s) Affected:**

**Description:** When the instantaneous FMCW Ramp frequency nears certain specific RF frequencies, there can be coupling between the synthesizer's reference and its output, and manifest as frequency glitches or spurs in TX output spectrum.

Implication: In FMCW radar 2D signal processing, this can lead to spurs in a fixed Doppler bin at all range bins. This situation can occur with narrow band chirps, if the FMCW ramp includes or nears 76.8-, 77.4-, 78-, 79.2-, 80.4-, 81-GHz RF frequencies. The affected Doppler bin is a function of chirp timing and RF frequency properties.

**Workaround(s):** Use the device's dithering features to vary idle time, RF frequency and ramp end times to spread the spurs significantly in Doppler dimension so that it does not get detected as spurious targets. Using larger chirp band widths also reduces the spur level.

### ANA#09A — *Synthesizer Frequency Nonlinearity around 76.8 GHz when Synthesizer (Chirp) Frequency Monitor Enabled*

**Revision(s) Affected:**

**Description:** When the synthesizer (chirp) frequency monitor is enabled and the synthesizer chirp is around 76.8 GHz, the frequency error can be as high as 500 kHz due to coupling between the monitor and the synthesizer. The RF frequencies impacted are 500Mhz around 76.8Ghz (76.8 ± 0.5 GHz).

*Implication: Increased nonlinearity in the chirp can lead to up to 20 dB degradation in the noise floor surrounding large objects. This leads to potential loss of dynamic range when large and small objects are present simultaneously.*

**Workaround(s):**

1. Disable the synthesizer frequency monitor during profiles where the LO crosses 76.8 ± 0.5 GHz.
2. Use non-functional chirps to detect nonlinearities (instead of high instantaneous frequency errors) in the synthesizer by inserting dummy chirps (where RX data is not used) after functional chirps (where RX data is consumed).

### ANA#10 — *Unreliable Readings from Synthesizer Supply Voltage Monitor*

**Revision(s) Affected:**

**Description:** During monitoring, the thresholds used to determine if the synthesizer supply voltage is within limits are much stricter than necessary for proper circuit operation. This can lead to occasional, erroneous reporting of supply failures even when there is no adverse impact on circuit or system behavior.

*Implication: The user cannot rely on supply failure indication from the supply monitors of PM, Clock and LO subsystems. The affected field is STATUS_SUPPLY_PMCLKLO in the monitoring report message: IWR_MONITOR_PMCLKLO_INTERNAL_ANALOG_SIGNALS_REPORT_AE_SB.*

**Workaround(s):** Ignore the field STATUS_SUPPLY_PMCLKLO in the monitoring report message: IWR_MONITOR_PMCLKLO_INTERNAL_ANALOG_SIGNALS_REPORT_AE_SB.

### ANA#11A — *TX, RX Calibrations Sensitive to Large External Interference*

**Revision(s) Affected:**

**Description:** External interference present on the RX or TX pins, during the period of the device calibration at RfInit, can lead to degraded accuracy or errors in the calibration results. If the interference changes its level while these calibrations are actively running, the calibration algorithm may interpret this as a change in signal power, leading to incorrect convergence. This applies to boot-time PD, Rx IQ mismatch calibration, Rx gain calibration, Tx power calibration, and phase-shifter calibration. It also impacts run-time Tx output power calibration in CLPC mode.

**Workaround(s):**

**Workaround #1:**

The incident power detector in the TX output power detector, along with the absolute level of the PA loopback used during the PA loopback monitors, are insensitive to this, and they can be used to check that the calibrations converged correctly. Calibration can be re-run if large interference was observed.

**Workaround #2:**

Another workaround is to save the boot time calibrations at production (done in a clean environment without interference) and during operation, the calibrations can be restored. For the runtime Tx output power calibrations, OLPC mode can be used instead of the CLPC mode.

### ANA#12A Second Harmonic (HD2) Present in the Receiver

**Revision(s) Affected:**

**Description:** There is a finite isolation between the RF pins/package and the FMCW synthesizer. This can create spurious tones at the synthesizer output and lead to appearance of 2nd order harmonics and inter-modulations of expected IF frequencies at RX ADC output. The amplitude of the 2nd harmonic could as high as -55 dBc , referenced to the power level of the intended tone at the LNA input.

**Workaround(s):** No workaround available at this time. However, in many typical radar usecases the HD2 does not affect the system performance due to two reasons:

1. Since the HD2 comes from a coupling to the LO signal, there is an inherent suppression of the HD2 level due to the self-mixing effect (that is, phase noise and phase spur suppression effect at the mixer).
2. In real-life scenarios there is often a double-bounce effect of the radar signal reflected from the target, which leads to a ghost object at twice the distance of the actual object. This effect is often indistinguishable from the effect of HD2 itself.

### ANA#13B TX1 to TX3 Phase Mismatch Variation over Temperature is Double that of TX2/TX1 and TX3/TX2 Combinations

**Revision(s) Affected:**

**Description:** TX3/TX1 combination exhibits a phase mismatch variation of ±6° from –40°C to 140°C whereas, TX2/TX1 and TX3/TX2 combinations exhibit a lower variation of ±3°C over the same temperature range.

**Workaround(s):** In applications requiring high phase accuracy across TX channels, a background angle calibration or a 2-point calibration can be used to control phase variation over temperature.

### ANA#15 — *Excessive TX-RX Coupling or Reflection can Lead to Saturated RX Output*

**Revision(s) Affected:**

**Description:** If there is excessing TX-RX coupling or chassis reflection, it can lead to a saturated RX output. This situation can occur if the RX input is stronger than -10dBm.

**Workaround(s):** Improve TX-to-RX antenna isolation on PCB. Radome/chassis should give low reflection amplitude and should be as close as possible to the sensor, to reduce the IF frequency.

**ANA#16** ***LVDS Coupling to Clock System***

**Revision(s) Affected:**

**Description:** The digital activity in the High-Speed Serial Interfaces (HSI) state machine can couple to the clock system/FMCW synthesizer and can cause spurs in its clock output. The spur frequency is HSI rate dependent (for example, for a 600-MHz HSI clock rate, 6.25-MHz and 12.5-MHz spurs can be observed on TX/RX output, and for a 900-MHz HSI clock rate, 7-MHz and 14-MHz spurs can be observed on the TX/RX output). The spur levels are low (*near or below -65 dBc*).

**Workaround(s):** The spur will not be present, when the LVDS is not used.

**ANA#17A** ***On-Board Supply Ringing Induced Spur***

**Revision(s) Affected:**

**Description:** Turning OFF and ON front-end modules can cause on-board supply ringing and slow the settling of the power supply. This supply ringing can manifest as a spur (~130KHz) in the FMCW synthesizer output spectrum.

**Workaround(s):** **Workaround #1:**

Disable inter-chirp duty cycling of the RX.

***or***

**Workaround #2:**

Design the power supply to damp out the ringing on the rails to the device.

**ANA#18B** ***Spurs Caused due to Digital Activity Coupling to XTAL***

**Revision(s) Affected:**

**Description:** Digital filtering activity can potentially couple to XTAL pins and lead to spurs in the LO, which would also be seen in the Rx data. The spur in the Rx data would be seen at the spur frequency offset around a strong object. For example if the spur frequency is 500Khz and there is a strong object at 2Mhz , the Rx ADC spectrum could have a spike at 1.5Mhz or 2.5Mhz. Note that the Tx – Rx antenna coupling would also form a strong object close to DC. The spur frequency depends on the sampling rate (Fs). The strongest of these spurs have been observed when Fs is close to 10, 12.5, 18, 18.75,20, 25, Msps. In these ranges, an IF spur can appear at Fs-10 Mhz, 2Fs-40MHz, 4Fs-40 MHz, 4Fs-100 MHz, 8Fs-100 MHz , 2Fs-37.5 MHz, 2Fs-36 MHz. The spur is observable when the spur frequency falls within 1.5 MHz, beyond that it gets heavily filtered out. Please refer the device datasheet for max usable sampling rate.

**Workaround(s):** **Workaround #1:**

Avoid sampling rates close to these numbers (10, 12.5, 18, 18.75, 20, 25 Msps) or use exactly these numbers (spur is at 0 Hz in the latter case).

**Workaround #2:**

Using external TCXO, instead of XTAL, with voltage swing between 1.4-1.8 Vpp can avoid these spurs.

### ANA#20 *Occasional Failures Observed During Calibration of the Radar Subsystem*

**Revision(s) Affected:**

**Description:** Rare occurrences of failures have been observed in the Dual-Clock Comparator (DCC) module, as a result the APLL or Synthesizer may report a failure.

**Workaround(s):** **Workaround #1:**

Any APLL calibration failure needs to be responded with a reset cycle.

***or***

**Workaround #2:**

Any SYNTH calibration failure reported by the BSS will require an RFinit.

### ANA#21B *Out of Band Radiated Spectral Emission*

**Revision(s) Affected:**

**Description:** Out-of-band radiated spectral emissions are observed at 14.4-GHz and 28.8-GHz.

**Workaround(s):** A grounded metallic shield around the device (excluding the antenna region) can be used to reduce the emission levels. Microwave absorber materials could also be placed around the device to reduce the emissions.

### ANA#22A *Overshoot and Undershoot During Inter-Chirp Idle Time*

**Revision(s) Affected:**

**Description:** At the end of the chirp , when the synthesizer starts to go back to the start frequency of the next chirp, there is some overshoot and undershoot. The undershoot/overshoot is proportional to the chirp bandwidth. Negative slope chirps have a worse undershoot than positive slope chirps.

**Workaround(s):** To ensure the TX power amplifier is OFF during chirp idle time and not causing "on-air" emissions during the undershoot/overshoot period, keep the inter-chirp power savings ON.

## ANA#24A 40-MHz OSC CLKOUT Causing Spurs in 2D-FFT Spectrum

**Revision(s) Affected:**

**Description:** Harmonics of 40 MHz from osc-clkout can be coupled onto the synthesizer and can cause low amplitude spurs in the 2D-FFT spectrum. These spurs are at fixed doppler bin, across all range bins.

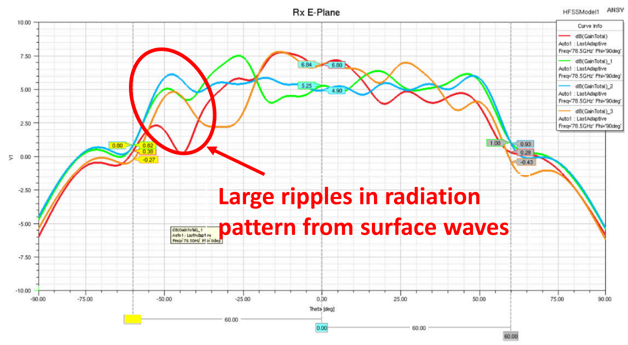
**Workaround(s):** For single chip usecases, where OSC CLKOUT is not used , OSC CLKOUT output can be disabled.

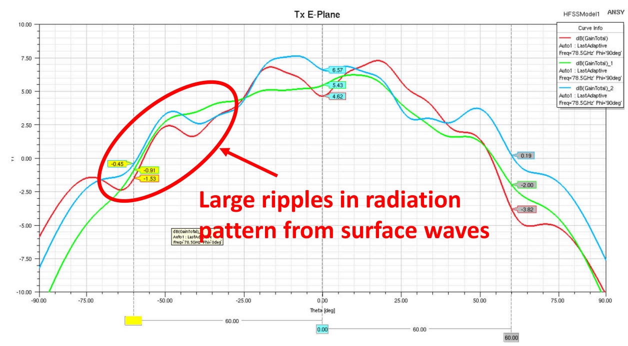
| | |
|---|---|
| **ANA#27** | ***Digital Temperature Sensor Having Higher Error*** |
| **Revision(s) Affected:** | |
| **Description:** | Due to the single-ended nature of the digital temperature sensors, as compared to the differential design of analog temperature sensors (that is, TX, RX, and PM), it is vulnerable to noise and can have higher error than the analog temperature sensors. |
| **Workaround(s):** | Use only the analog temperature sensor values (TX and RX) in the algorithm. The digital temperature sensor value can be ignored. |

## PACKAGE#02A *Surface Wave Artifact from PCB*

**Revision(s) Affected:**

**Description:** Large PCBs area around the E-plane causes surface waves that create large ripples in the elevation direction of the AoP antenna radiation pattern.




**Workaround(s):**

**Workaround #1:**

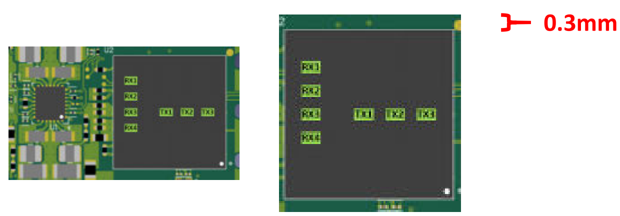



**Figure 5-5. Small form factor board with PCB edge less than 0.3mm**

Keep the Edge of PCB close to the edge of the AoP device in the E-plane to minimize the surface wave ripples.

***or***

**Workaround #2:**

If a larger board is needed for the solution, a trapezoid cutout with the PCB edge less than <0.3mm from the edge of the AoP should be implemented to minimize the ripples caused by surface waves.

**PACKAGE#02A**
(continued)

***Surface Wave Artifact from PCB***

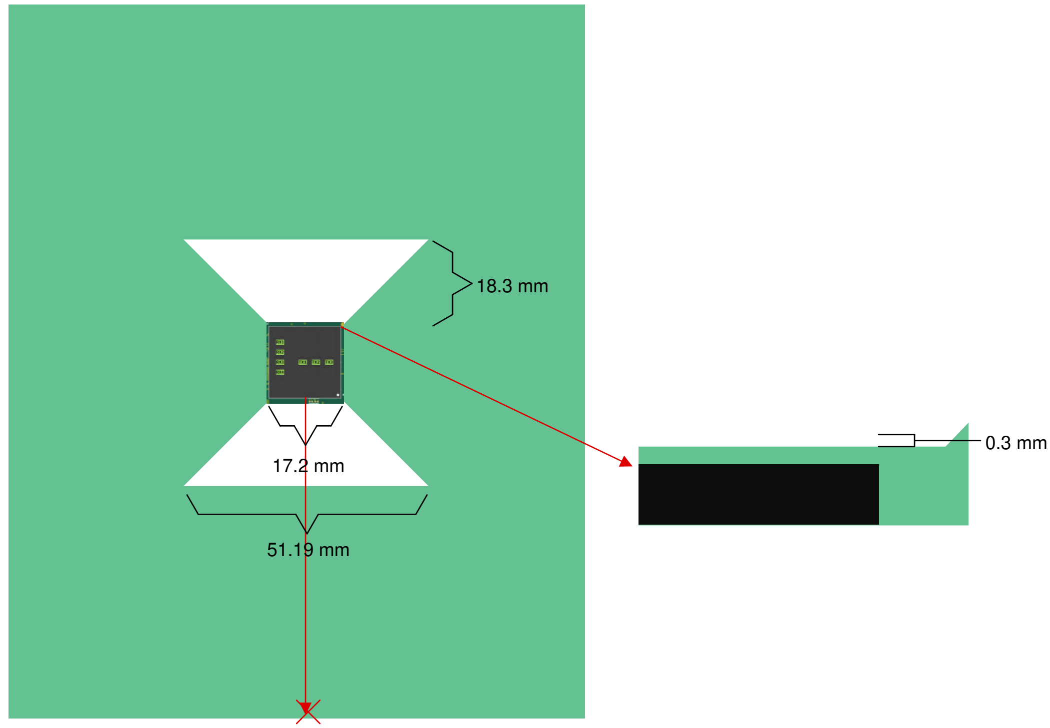



**Figure 5-6. Large form factor board with trapezoidal cutout and PCB edge less than 0.3mm**

## 6 Trademarks

All trademarks are the property of their respective owners.

## 7 Revision History

| DATE | REVISION | NOTES |
| --- | --- | --- |
| August 2023 | * | Initial Release |

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