

Errata

# **IWR6243 Device Errata**

## **Silicon Revisions 1.0 and 1.1**

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## 1 Introduction

This document describes the known exceptions to the functional and performance specifications to TI CMOS Radar Devices (IWR6243).

## 2 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of Radar / milli-meter Wave sensor devices. Each of the Radar devices has one of the two prefixes: X1x or IWR6x (for example: X16243BGABL). These prefixes represent evolutionary stages of product development from engineering prototypes (X1x) through fully qualified production devices (IWR6x).

Device development evolutionary flow:

- X1x**— Experimental device that is not necessarily representative of the final device's electrical specifications and may not use production assembly flow.
- IWR6x**— Production version of the silicon die that is fully qualified.

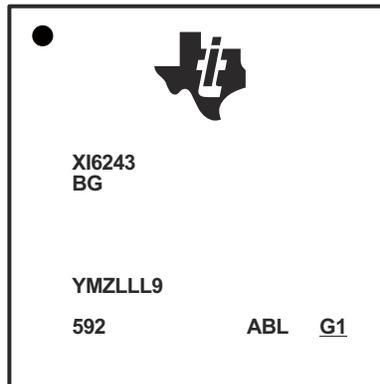
X1x devices are shipped with the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

Texas Instruments recommends that these devices not to be used in any production system as their expected end –use failure rate is still undefined.

### 3 Device Markings

Figure 3-1 shows an example of the IWR6243 Radar Device's package symbolization.



**Figure 3-1. Example of Device Part Markings**

This identifying number contains the following information:

- **Line 1:** Device Number
- **Line 2:** Safety Level and Security Grade
- **Line 3:** Lot Trace Code
  - YM = Year/Month Date Code
  - Z = Secondary Site Code
  - LLL = Assembly Lot
  - 9 = Primary Site Code
- **Line 4:**
  - 592 = IWR6243 Identifier
  - BLANK = ES1.0, A = ES1.1
  - ABL = Package Identifier
  - G1 = "Green" Package Build (must be underlined)

## 4 Advisory to Silicon Variant / Revision Map

**Table 4-1. Advisory to Silicon Variant / Revision Map**

ADVISORY NUMBER	ADVISORY TITLE	IWR6243	
		ES1.0	ES1.1
<b>MAIN SUBSYSTEM</b>			
<a href="#">MSS#37B</a>	DCC Module Frequency Comparison can Report Erroneous Results	X	X
<a href="#">MSS#44A</a>	SYNC IN input pulse wider than 4usec can cause a FRC lockstep error	X	X
<a href="#">MSS#50</a>	Occasional EDMA self-test failure	X	X
<a href="#">MSS#51</a>	Spurious toggle on nERROR OUT signal during powerup due to undefined state in ESM block	X	X
<b>ANALOG / MILLIMETER WAVE</b>			
<a href="#">ANA#11B</a>	TX, RX Calibrations Sensitive to Large External Interference	X	X
<a href="#">ANA#12A</a>	Second Harmonic (HD2) is Present in the Receiver	X	X
<a href="#">ANA#13B</a>	Phase Mismatch Variation Across Temperature in TX3/TX1 and TX3/TX2 Combinations are higher than that of TX2/TX1 Combination	X	X
<a href="#">ANA#21A</a>	Out of Band Radiated Spectral Emission	X	X
<a href="#">ANA#22A</a>	Overshoot and Undershoot During Inter-Chirp Idle Time	X	X
<a href="#">ANA#23</a>	MIPI CSI2 HS Data TX Differential Voltage Mismatch (Pulse) Marginality	X	X
<a href="#">ANA#24</a>	40-MHz OSC CLKOUT Causing Spurs in 2D FFT Spectrum	X	X
<a href="#">ANA#25</a>	High-Speed Data System Coupling to the Clock System	X	X
<a href="#">ANA#27</a>	Digital Temperature Sensor Having Higher Error	X	X
<a href="#">ANA#28A</a>	20GHz FM_CW_SYNCOUT/CLKOUT to FM_CW_SYNCIN Coupling in Cascade Use Case	X	X
<a href="#">ANA#40A</a>	Fixed spur at 20MHz IF frequency	X	X
<a href="#">ANA#41</a>	Spurs Caused due to Digital Activity Coupling to XTAL	X	X
<a href="#">ANA#42</a>	Doppler Spur Observed at Certain RF Frequencies in 57 GHz to 64 GHz band	X	X

## 5 Known Design Exceptions to Functional Specifications

### **MSS#37B** *DCC Module Frequency Comparison can Report Erroneous Results*

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**Revision(s)  
Affected:** IWR6243 ES1.0 and ES1.1

**Description:** The Dual-clock Comparator module, which is used to monitor a clock frequency while comparing with a known clock reference, could stop earlier than expected, and, thus, indicating the measured clock frequency to be lower. This is due to a clock domain crossing issue causing the error detection logic to get triggered. This incorrect reporting, can cause a rare failure in the DCC monitor used to monitor internal clock frequencies.

**Workaround(s):** Multiple measurements can be taken for the same clock pairs, and the median of the frequencies reported can be used for detecting failure.

### **MSS#44A** *SYNC IN input pulse wider than 4usec can cause a FRC lockstep error*

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**Revision(s)  
Affected:** IWR6243 ES1.0 and ES1.1

**Description:** In hardware based frame triggered mode of operation, external SYNC IN pulse is provided to the radar device. If the width of the pulse is  $> 4\mu\text{sec}$ , it could cause MSS ESM group 1 fault with FRC lockstep error.

**Workaround(s):** The pulse width of the external SYNC IN signal should be  $>25\text{nsec}$  and  $< 5\mu\text{sec}$

**MSS#50** *Occasional EDMA self-test failures*

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**Revisions Affected** IWR6243 ES1.0 and ES1.1**Details**

During the first powerup, there could be occasional failures in the EDMA self-test. It is reported as part of the "AWR\_AE\_MSS\_BOOTERRORSTATUS\_SB" flag during bootup. This is due to the undefined states of certain flops during first powerup. This blocks the EDMA channel and eventually fails any subsequent EDMA transfers as well.

EDMA is also used to transfer out ADC/CP/CQ data on the CSI or LVDS interface as well, so this data transfer would also fail in that case.

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**Note**

This failure is not seen with subsequent nReset cycles after powerup.

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**Workaround**

The host application needs to monitor the BOOTERRORSTATUS flag. If the EDMA\_Self Test flag is set to '1', indicating failure, it should issue an nReset to the mmWave device. This should be done without power cycling the device, i.e. disabling the power supplies to the mmWave device.

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**MSS#51** *Spurious toggle on nERROR OUT signal during powerup due to undefined state in ESM block.*

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**Revisions Affected** IWR6243 ES1.0 and ES1.1**Details**

When the mmWave device powers up (nReset is released), the internal state machine starts on internal RC oscillator clock before the 40MHz clock is available.

Inside the ESM module (Error Signaling Module), at least 3 cycles of RCOSC CLK cycles are needed to clear the internal states because the Flip Flops (FFs) are non-resettable.

In silicon, the ESM reset might get released before these three RCOSC CLK cycles and at that moment an undefined state of nError out flip flop could get latched. This could be either 0 or 1 since its undefined at that point. Once an error value gets latched, it would be retained until the software clears it. The bootloader then boots up and initializes the ESM block, which then clears the error. Hence, the nError out goes low for about 13msec after the power up, until it is initialized by the bootloader.

**Workaround**

1. The Host processor can ignore the nERROR OUT status until the device has fully booted up i.e. until the Host IRQ is raised and the mmWave device is ready to receive the command from the host processor over the SPI interface.
2. The Host processor could also put a timer from the nRESET release to ensure the nERROR OUT does not remain low beyond a certain time after nRESET release. For example, a 25 msec timer after the nReset release. By this time, the bootloader should have ideally cleared the ESM block and nERROR OUT should go high. If the nERROR OUT still remains low post the timer, then it could indicate a real fault.

<b>ANA#11B</b>	<b><i>TX, RX Calibrations Sensitive to Large External Interference</i></b>
<b>Revision(s) Affected:</b>	IWR6243 ES1.0 and ES1.1
<b>Description:</b>	External interference present on the RX or TX pins, during the period of the device calibration at Rflnit, can lead to degraded accuracy or errors in the calibration results. If the interference changes its level while these calibrations are actively running, the calibration algorithm may interpret this as a change in signal power, leading to incorrect convergence. This applies to boot-time PD, Rx IQ mismatch calibration, Rx gain calibration, Tx power calibration, and phase-shifter calibration.
<b>Workaround(s):</b>	Workaround is to save the boot time calibrations at production (done in a clean environment without interference) and during operation, the calibrations can be restored.

**ANA#12A**

***Second Harmonic (HD2) Present in the Receiver***

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**Revision(s)  
Affected:**

IWR6243 ES1.0 and ES1.1

**Description:**

There is a finite isolation between the RF pins/package and the FMCW synthesizer. This can create spurious tones at the synthesizer output and lead to appearance of 2nd order harmonics and inter-modulations of expected IF frequencies at RX ADC output. The amplitude of the 2nd harmonic could be as high as -55 dBc, referenced to the power level of the intended tone at the LNA input.

**Workaround(s):**

No workaround available at this time. However, in many typical radar usecases the HD2 does not affect the system performance due to two reasons:

1. Since the HD2 comes from a coupling to the LO signal, there is an inherent suppression of the HD2 level due to the self-mixing effect (that is, phase noise and phase spur suppression effect at the mixer).
2. In real-life scenarios there is often a double-bounce effect of the radar signal reflected from the target, which leads to a ghost object at twice the distance of the actual object. This effect is often indistinguishable from the effect of HD2 itself.

<b>ANA#13B</b>	<b><i>Phase Mismatch Variation Across Temperature in TX3/TX1 and TX3/TX2 Combinations are higher than that of TX2/TX1 Combination</i></b>
<b>Revision(s) Affected:</b>	IWR6243 ES1.0 and ES1.1
<b>Description:</b>	TX3/TX1 and TX3/TX2 combinations exhibit a higher phase mismatch variation across the complete recommended operating temperature range per the data manual as compared to TX2/TX1 combination over the same temperature range.
<b>Workaround(s):</b>	In applications requiring high phase accuracy across TX channels, a background angle calibration can be used to control phase variation over temperature

<b>ANA#21A</b>	<b><i>Out of Band Radiated Spectral Emission</i></b>
<b>Revision(s) Affected:</b>	IWR6243 ES1.0 and ES1.1
<b>Description:</b>	Out-of-band radiated spectral emissions are observed at 14.4-GHz and 28.8-GHz.
<b>Workaround(s):</b>	A grounded metallic shield around the device (excluding the antenna region) can be used to reduce the emission levels. Microwave absorber materials could also be placed on the device to reduce the emissions.
<b>ANA#22A</b>	<b><i>Overshoot and Undershoot During Inter-Chirp Idle Time</i></b>
<b>Revision(s) Affected:</b>	IWR6243 ES1.0 and ES1.1
<b>Description:</b>	At the end of the chirp , when the synthesizer starts to go back to the start frequency of the next chirp, there is some overshoot and undershoot. The undershoot/overshoot is proportional to the chirp bandwidth. Negative slope chirps have a worse undershoot than positive slope chirps.
<b>Workaround(s):</b>	To ensure the TX power amplifier is OFF during chirp idle time and not causing "on-air" emissions during the undershoot/overshoot period, keep the inter-chirp power savings ON.
<b>ANA#23</b>	<b><i>MIPI CSI2 HS Data TX Differential Voltage Mismatch (Pulse) Marginality</i></b>
<b>Revision(s) Affected:</b>	IWR6243 ES1.0 and ES1.1
<b>Description:</b>	Some devices could fail the MIPI CSI2 HS TX Differential Voltage Mismatch spec [ $\Delta VOD = VOD1 -  VOD0 $ ] by a few mV on the CSI data lanes at higher temperatures. The MIPI spec for this parameter is 14 mV.
<b>Workaround(s):</b>	None. This failure should typically not impact the data integrity/reception.

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<b>ANA#24</b>	<b><i>40-MHz OSC CLKOUT Causing Spurs in 2D-FFT Spectrum</i></b>
<b>Revision(s) Affected:</b>	IWR6243 ES1.0 and ES1.1
<b>Description:</b>	Harmonics of 40 MHz from osc-clkout can be coupled onto the synthesizer and can cause low amplitude spurs in the 2D-FFT spectrum. These spurs are at fixed doppler bin, across all range bins.
<b>Workaround(s):</b>	<ol style="list-style-type: none"><li>1. For single chip usecases, where OSC CLKOUT is not used , OSC CLKOUT output can be disabled.</li><li>2. For cascade usecase or where OSC clkout is needed in the system, use the chirp dithering capability (idle time, RF start frequency, ADC start time) across the frame to spread the spur across all the Doppler bins and hence avoid false detection.</li></ol>
<b>ANA#25</b>	<b><i>High-Speed Data System Coupling to the Clock System</i></b>
<b>Revision(s) Affected:</b>	IWR6243 ES1.0 and ES1.1
<b>Description:</b>	Data transfer over LVDS and CSI interface with repeatable patterns could interfere with the clock system and cause low-level spurs in the Rx spectrum and show up in the 2D-FFT. In case of CSI interface, the mode transitions (LP-to-HS or HS-to-LP) could also cause interference in the clock system.
<b>Workaround(s):</b>	The firmware allows applying random dither to the CSI data transfer start time. This can be controlled using the "AWR_DEV_CSI2_DELAY_DUMMY_CFG_SET_SB" API. With the dithering the glitch on the synthesizer frequency error gets spread out in time, across the chirps of a frame, reducing the impact in the 2D-FFT.

**ANA#27**

***Digital Temperature Sensor Having Higher Error***

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**Revision(s)  
Affected:**

IWR6243 ES1.0 and ES1.1

**Description:**

Due to the single-ended nature of the digital temperature sensors, as compared to the differential design of analog temperature sensors (that is, TX, RX, and PM), it is vulnerable to noise and can have higher error than the analog temperature sensors.

**Workaround(s):**

Use only the analog temperature sensor values (TX and RX) in the algorithm. The digital temperature sensor value can be ignored.

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<b>ANA#28A</b>	<b>20GHz FM_CW_SYNCOUT/CLKOUT to FM_CW_SYNCIN Coupling in Cascade Use Case</b>
<b>Revision(s) Affected:</b>	IWR6243 ES1.0 and ES1.1
<b>Description:</b>	<p>There is ~18dB on-chip isolation between the 20GHz FM_CW_SYNCOUT/CLKOUT and FM_CW_SYNCIN signals of the primary device in cascade configuration. Apart from the stronger FM_CW_SYNCIN signal that is looped back to the primary device in cascade, there is also a weaker signal coupled from SYNCOUT/CLKOUT directly to SYNCIN. Between the two signals, there is a delay due to PCB routing. This signal delay, caused by PCB routing, could lead to slight smearing of the object peak in the range dimension. The extent of smearing depends on the PCB routing delays of the 20GHz signals.</p>
<b>Workaround(s):</b>	Keep the PCB routing delay of the 20GHz sync signals lower, to reduce the extent of smearing of the peak.

**ANA#40** *Fixed spur at 20MHz IF frequency.*

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**Revisions Affected:** IWR6243 ES1.0 and ES1.1

**Description:** Receiver output shows a spur at 20MHz due to parasitic coupling from digital activity  
The spur will be seen for Sampling rates > 20Msps in Complex 1x and >40Msps in other modes (Complex 2x, Real and pseudo real). The spur is not a concern in lower Sampling rates as it is filtered out by the receiver chain.

**Workaround** Due to the fixed spur at 20Mhz, the maximum usable IF bandwidth is reduced to slightly below 20MHz (for example, 19.9MHz assuming 256 samples per chirp)

**ANA#41**
***Spurs Caused due to Digital Activity Coupling to XTAL***


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**Revision(s)  
Affected:**

IWR6243 ES1.0 and ES1.1

**Description:**

Digital filtering activity can potentially couple to XTAL pins and lead to spurs in the LO, which would also be seen in the Rx data. The spur in the Rx data would be seen at the spur frequency offset around a strong object. For example if the spur frequency is 500Khz and there is a strong object at 2Mhz , the Rx ADC spectrum could have a spike at 1.5Mhz or 2.5Mhz. Note that the Tx – Rx antenna coupling would also form a strong object close to DC. The spur frequency depends on the sampling rate (Fs). The strongest of these spurs have been observed when Fs is close to 10, 12.5, 18, 18.75,20, 25, 30, 35 and 40 Msps. In these ranges, an IF spur can appear at Fs-10 MHz, 2Fs-10 MHz, 2Fs-15 MHz, 2Fs-40 MHz, 4Fs-40 MHz, 4Fs- 60 MHz, 4Fs-100 MHz, 8Fs-100 MHz , 2Fs-37.5 MHz, 2Fs-36 MHz, 2Fs-60 MHz, 4Fs-140 MHz, Fs-40 MHz. The spur is observable when the spur frequency falls within 1.5 MHz, beyond that it gets heavily filtered out. Please refer the device datasheet for max usable sampling rate.

**Workaround(s):**
**Workaround #1:**

Avoid sampling rates close to these numbers (5, 7.5, 10, 12.5, 15, 18, 18.75, 20, 25, 30, 35 and 40 Msps) or use exactly these numbers (spur is at 0 Hz in the latter case).

**Workaround #2:**

Using external TCXO, instead of XTAL, with voltage swing between 1.4-1.8 Vpp can avoid these spurs.

**ANA#42** ***Doppler Spur Observed at Certain RF Frequencies in 57 GHz to 64 GHz band***

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**Revision(s)  
Affected:** IWR6243 ES1.0 and ES1.1

**Description:** There is a non-linearity of the synthesizer when crossing certain frequencies: 57.6-, 57.93-, 58.05-, 58.17-, 58.5-, 59.28-, 59.4-, 59.52-, 60.3-, 60.75-, 61.2-, 61.56-, 62.1-, 62.64-, 63-, and 63.45-GHz.

Implication: There will be a spur in the non-zero Doppler bin when the synthesizer crosses any of these frequencies during a chirp. The exact Doppler bin depends on the slope and ramp timings. The spur will be spread across multiple range bins.

**Workaround(s):** Use the device's dithering features to vary idle time, RF frequency and ADC start times to spread the spurs significantly in Doppler dimension so that it does not get detected as spurious targets. Using larger chirp band widths also reduces the spur level.

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