Application Note

Wide-Band DSSS Mode for FCC Digital Transmission Systems Using CC13x2

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ABSTRACT

This application report describes a wide-band modulation scheme to comply with the requirements of FCC section 15.247 for non-frequency hopping digital modulation systems. The scheme is implemented with an MCE patch, which is a standalone program that implements the various options of the WB-DSSS scheme. The patch is included in the SDK and a working example code can be setup using example programs and Sysconfig [4]. The SDK can be downloaded from: https://www.ti.com/tool/SIMPLELINK-CC13X2-26X2-SDK.

The implementations and summary of performance measured on CC1352PEM-XD7793-XD24-PA9093 are provided in this document.

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1 Introduction

WB-DSSS uses a well-known method to obtain sensitivity gains by means of coding and spreading the information bits into a series of transmitted symbols.

The transmit spectrum requirements of FCC Section 15.247 for digital transmission systems operating in the 902 MHz - 928 MHz band are as follows:

- The minimum 6 dB emission bandwidth of the signal shall be at least 500 kHz.
- The maximum peak conducted output power for transmitter is +30 dBm (1 Watt).
- The maximum power spectral density is limited to 8 dBm in any 3 kHz band segment within the emission bandwidth during any interval of continuous transmission.

1.1 Acronyms Used in This Document

Table 1-1. Acronyms and Descriptions

Acronym	Description
AWGN	Additive White Gaussian Noise
BER	Bit Error Rate
BW	Bandwidth
CRC	Cyclic Redundancy Check
DSSS	Direct Sequence Spread Spectrum
FEC	Forward Error Correction
(G)FSK	(Gaussian) Frequency shift keying
MCE	Modem Control Engine
PER	Packet Error Rate
SNR	Signal to Noise Ratio
XOR	Exclusive OR

2 DSSS Encoding Scheme

The DSSS scheme is depicted in Figure 2-1. A convolutional encoder of rate ½ is followed by a direct sequence spreader with variable spreading length. The output of the module is fed into the 2-GFSK modulator to produce the modulated GFSK signal.

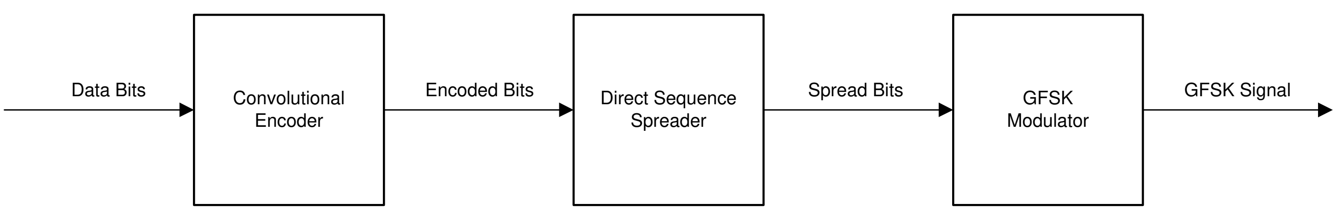

Figure 2-1. WB-DSSS Coding Scheme (the modulator is 2-GFSK)

The following subsections briefly discuss the workings of the first two main blocks shown in Figure 2-1.

2.1 Convolutional Encoder

Figure 2-2 shows the coder implemented in the DSSS modulation. A convolutional encoder is defined by its rate, its constraint-length K (number of stages in the encoding shift register) and the connections between its internal states. The convolutional encoder used in this case has K = 4 and only supports ½ rate, that is, for every input bit, the encoder produces two output bits.

The connections between internal states are a fundamental way of defining the code. The implemented encoder is based on non-systematic, non-recursive convolutional code.

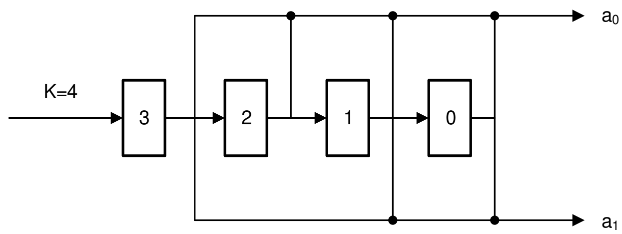

Figure 2-2. K=4, Rate = ½, Convolutional Encoder for WB-DSSS Modes

The black dots in Figure 2-2 represent logic XOR operations. The two output bits (a_0, a_1) from the encoder are serialized in a way that a_0 is transmitted first and a_1 is transmitted last.

2.2 Direct Sequence Spreader

The Direct Sequence Spreader assigns a known bit pattern to each of the incoming bits to the module. It can be considered a form of repetition code where a bit of duration t is replaced by *M* bits each of duration T_b. As a consequence, the rate at which information is transmitted is reduced by 1/M. If you want to keep information rate constant, then the bit duration must be reduced by T_b/M, which subsequently increases the bandwidth by factor M. As a consequence the information bits are "chipped" into smaller duration symbols and are transmitted over the air. The ratio of symbol rate to the bit rate is called processing gain of a spread spectrum system.

The processing gain is the figure of merit that is considered when comparing narrow-band system to spread spectrum application. To appreciate intuitively how this improves the error performance we consider the slicer in a correlation receiver followed by a maximum likelihood (ML) decision block. In a DSSS system the block will make decisions on each symbol and then integrate the result over one information bit period. The probability of making a bit error therefore reduces when the bit is divided into many short duration symbols.

In the CC1352 DSSS modes, the spreader length can be configured to be 1, 2, 4, and 8. Table 2-1 illustrates the bit mapping for each of the options.

The WB-DSSS scheme is implemented as 2-GFSK PHY with over the air symbol rate of 480 kbps.

Table 2-1. DSSS Spreading Codes

DSSS	'0'	'1'
1	'0'	'1'
2	'00'	'11'
4	'1100'	'0011'
8	'11001100'	'00110011'

3 Packet Format

A 5 byte preamble is used for testing and this is programmable. The payload in DSSS mode is byte oriented. Definition of packet lengths, headers, CRC, whitening follow the same rules as in the standard CC13x2 Generic FSK modes. The entire packet structure is illustrated in Figure 3-1.

Preamble	Sync Word	Payload	Termination
Variable	32 bits or 64 bits	N*8*2*DSSS bits	4*2*DSSS bits

Figure 3-1. WB-DSSS Packet Structure

The payload is encoded first by FEC and then spread through the DSSS block, as described in Section 2. In order to terminate the sequence, the modem automatically inserts four termination bits at the end of the payload with each termination bit resulting in 2*DSSS transmitted over-the-air symbols.

The relationship between data rate (the actual amount of information bits available to the higher protocol layers) and the symbol rate (the actual modulation rate used in the radio) can be expressed as:

$$\text{Data Rate} = \frac{\text{Symbol Rate}}{2 * \text{DSSS}} \tag{1}$$

4 Setting Up WB-DSSS in SmartRF™ Studio

The SmartRF studio contains the settings for the optimized WB-DSSS cases that can be tested from within the GUI. By launching the GUI and connecting CC13x2 launchpads with USB cable, the devices will show up in the GUI's console. From there, by clicking each one from the list of connected devices, the LaunchPads can be independently configured for TX and RX and a RF link test can be conducted.

Note

Choose Proprietary Mode when prompted to select CC13x2 modes.

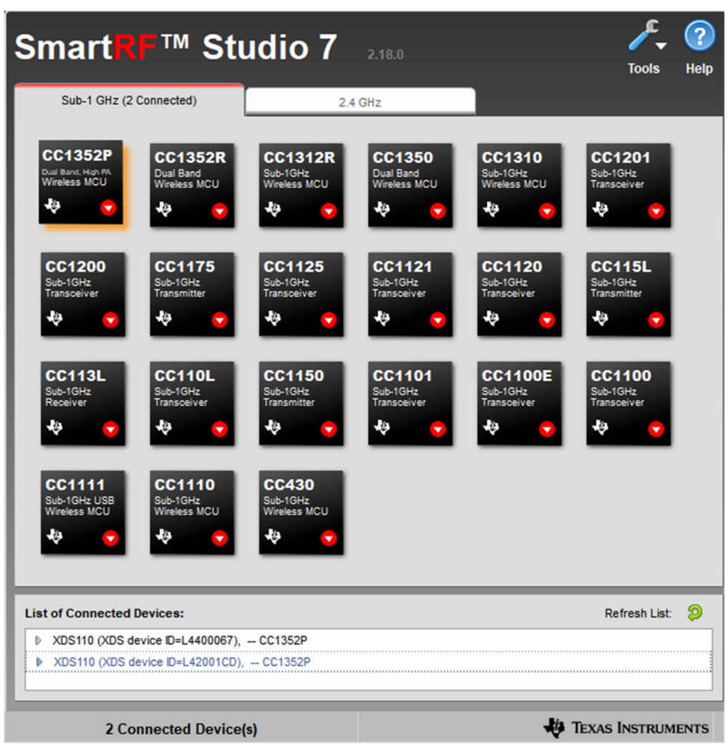

Figure 4-1. SmartRF GUI Showing Two CC1352P in List of Connected Devices

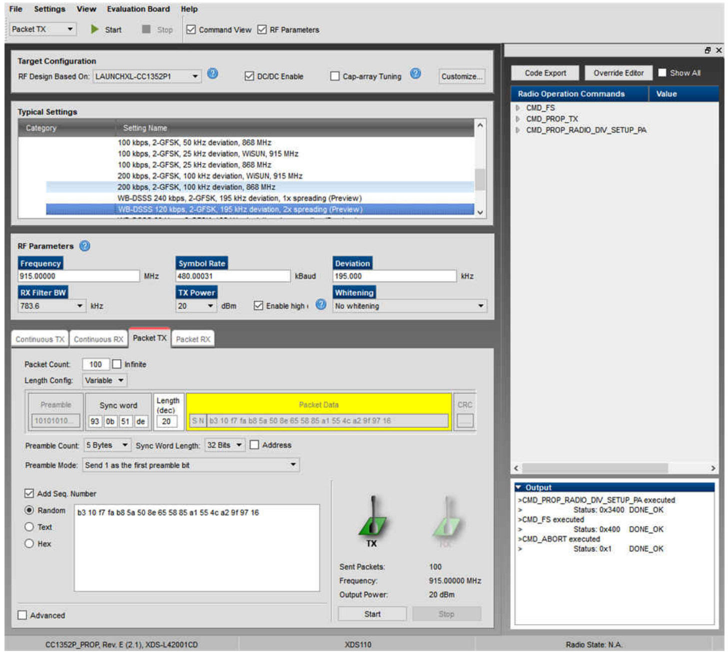

Figure 4-2. SmartRF Studio Showing WB-DSSS Setup in Transmit Mode

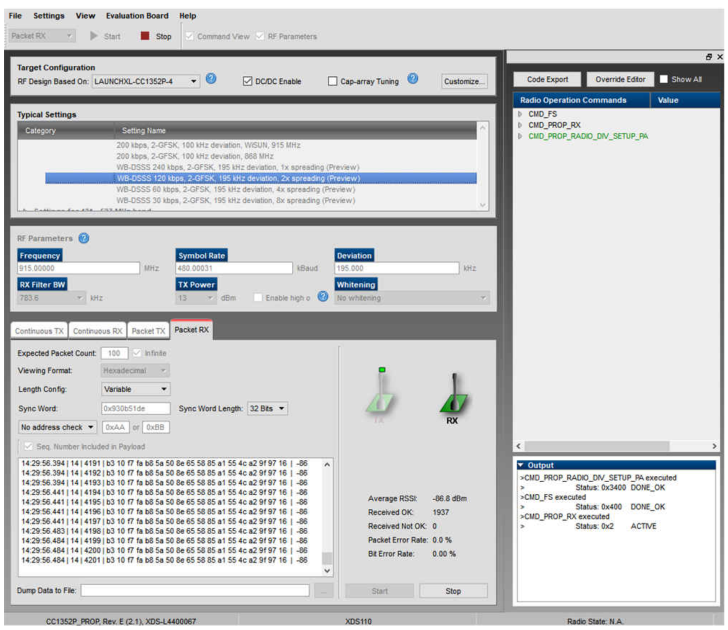

Figure 4-3. SmartRF Studio Showing WB-DSSS Setup in Receive Mode

Per default, the WB-DSSS settings in the SmartRF use **formatConf.fecMode = 0x0**. With this setting, the user can define the first 32-bits of the sync word. The patch will then append this to the remaining 32-bits of the sync word. For example, if syncWord = 0x12345678, the overall sync word will become 0x12345678_3CC3CCCC. The SmartRF studio setup for testing this scenario is shown in Figure 4-2 and Figure 4-3.

Alternatively, the WB-DSSS settings in SmartRF Studio can be changed by setting **formatConf.fecMode = 0x8** and **formatConf.whitenMode = 0x1**. In this mode, the MCE patch overrides any user defined sync word and replaces it with 0x333C_3C33_3CC3_CCCC. This is also compatible with default modes for CC13x0 devices. Note the settings in Figure 4-4.

Note

Changing sync word can affect the BER performance and must be chosen with care.

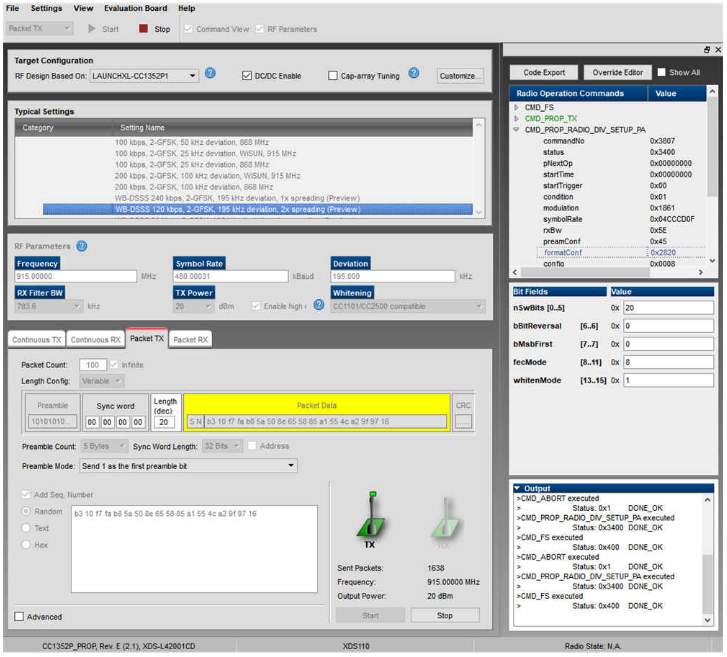

Figure 4-4. SmartRF Studio Showing WB-DSSS Setup in Transmit Mode (note the setup of sync word when testing in SmartRF Studio)

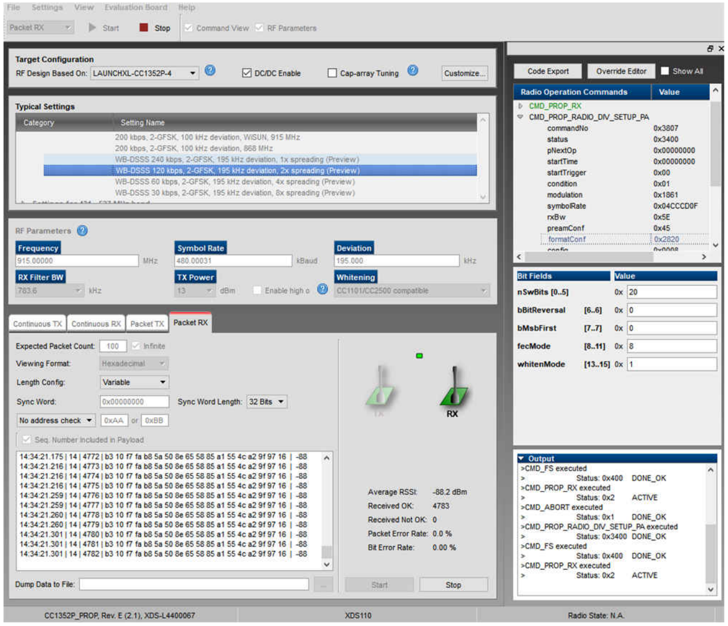

Figure 4-5. SmartRF Studio Showing WB-DSSS Setup in Receive Mode (note the setup of sync word when testing in SmartRF Studio)

5 Setting Up WB-DSSS in Code Composer Studio™

In the Simplelink SDK, there are working examples for setting up CC13x2 for evaluation. Testing the WB-DSSS scheme can easily be done by importing the rfPacketTx and rfPacketRx examples (see Figure 5-1) from the SDK, and changing the default settings (50 kbps) to the various WB-DSSS options using SysConfig.

For details on how to configure the radio via Sysconfig, see the Sysconfig documentation [4] provided in the SDK for Proprietary RF examples.

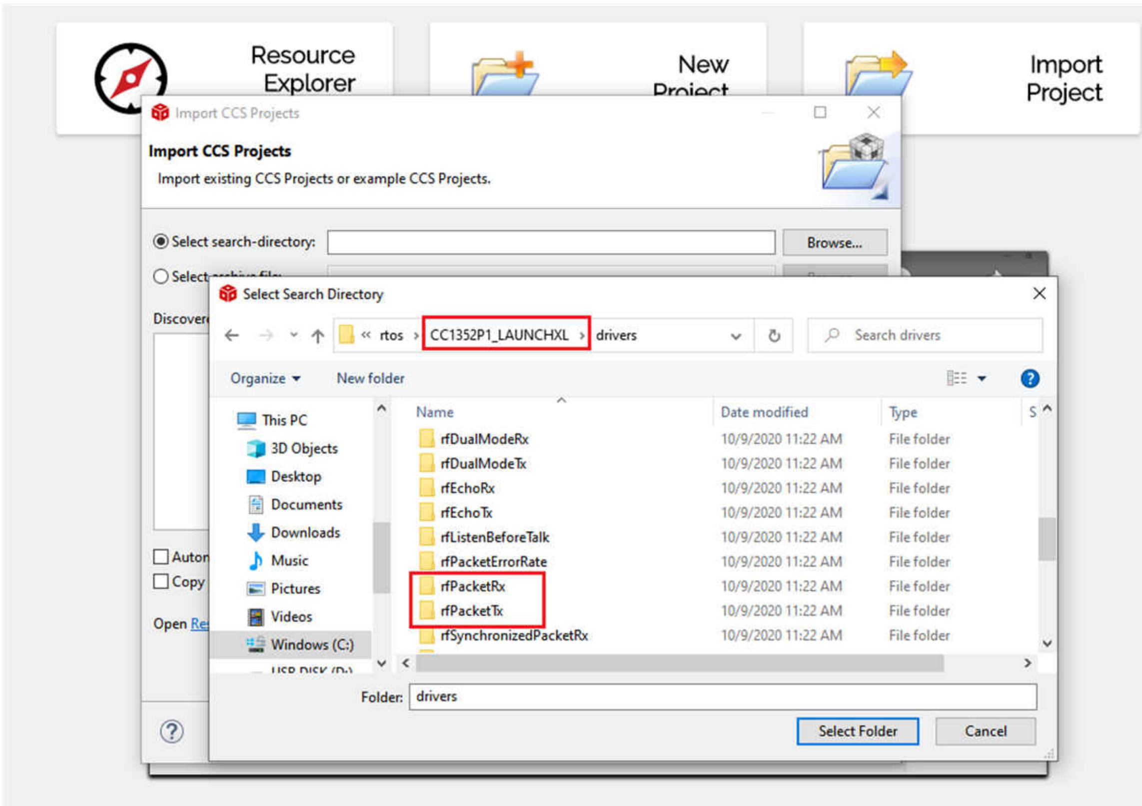

Figure 5-1. CCS Project Import Showing rfPacketRx and rfPacketTX Examples

6 Measured Results

The results shown in the following sections are measured at 25°C and 3 V on CC1352PEM-XD7793-XD24-PA9093 boards. The sensitivity is given at BER = 10^{-2} which is close to 80% PER for a 20 byte packet.

A protocol that normally uses short packets would have an acceptable packet error rate when BER is 1% where as a longer packet (200-2000 byte) would require a BER of around 10^{-5} to operate properly.

6.1 Receiver Performance

In receiver tests, the packet length was 20 bytes. Sensitivity is defined at the BER=10^{-2} point, which is close to 80% PER for that packet length.

6.1.1 DSSS = 1, 240 kbps, 2-GFSK, 195 kHz Deviation, 1x Spreading

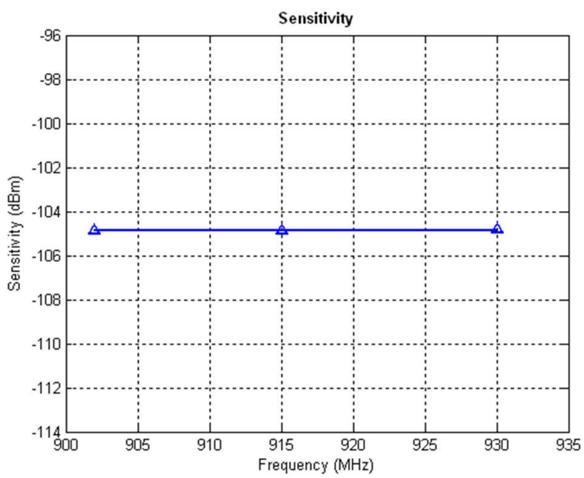

Figure 6-1. Sensitivity K = 4, DSSS = 1, 240 kbps

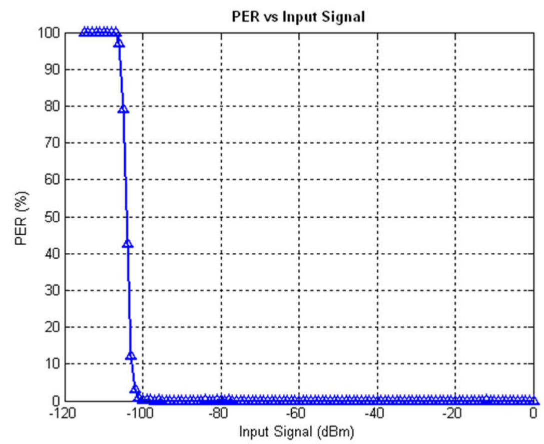

Figure 6-2. PER vs. Input Signal Level K = 4, DSSS = 1, 240 kbps

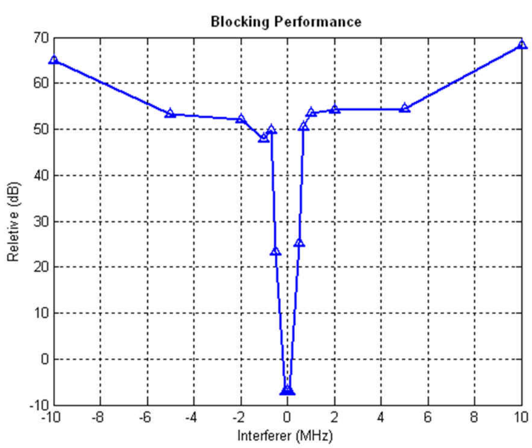

Figure 6-3. Blocking Performance K = 4, DSSS = 1, 240 kbps

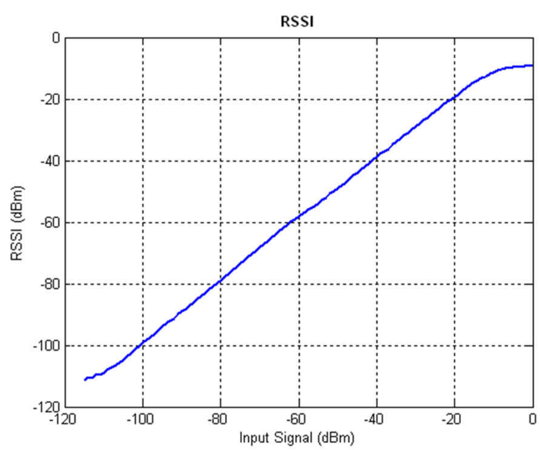

Figure 6-4. RSSI K = 4, DSSS = 1, 240 kbps

6.1.2 WB-DSSS 120 kbps, 2-GFSK, 195 kHz Deviation, 2x Spreading

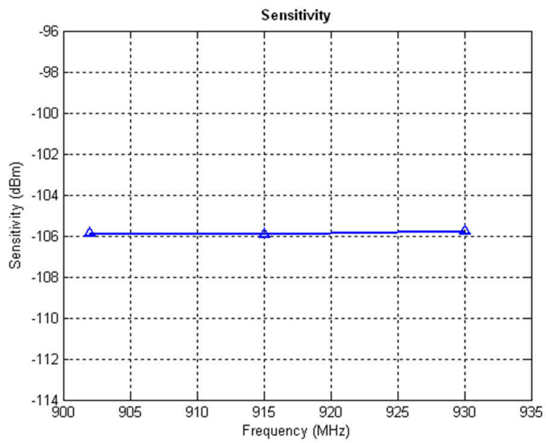

Figure 6-5. Sensitivity K = 4, DSSS = 2, 120 kbps

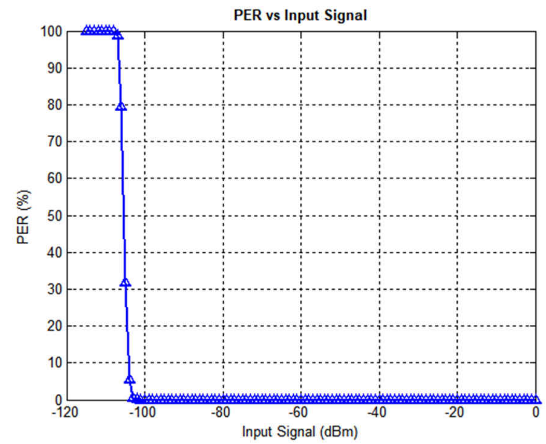

Figure 6-6. PER vs. Input Signal Level K = 4, DSSS = 2, 120 kbps

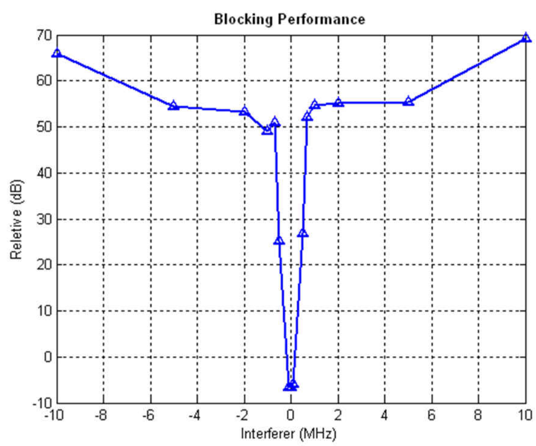

Figure 6-7. Blocking Performance K = 4, DSSS = 2, 120 kbps

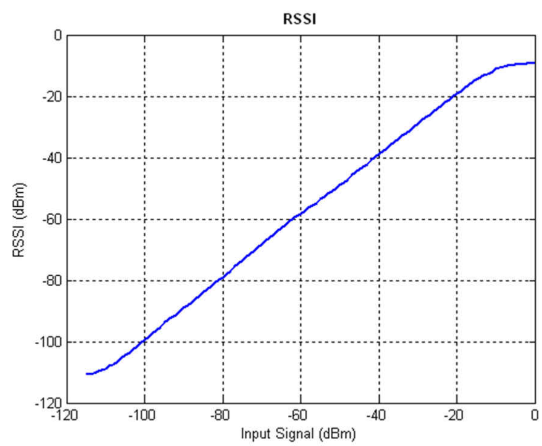

Figure 6-8. RSSI K = 4, DSSS = 2, 120 kbps

6.1.3 WB-DSSS 60 kbps, 2-GFSK, 195 kHz Deviation, 4x Spreading

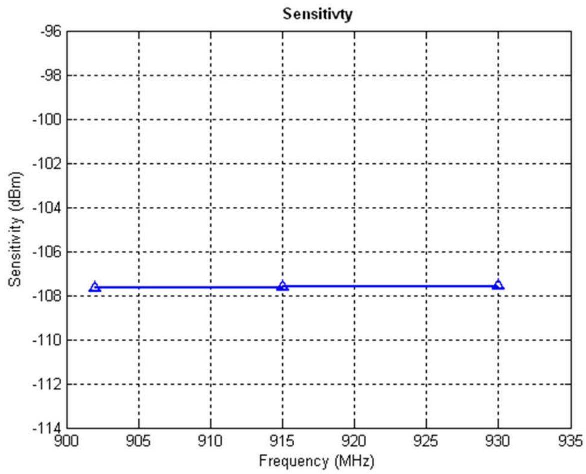

Figure 6-9. Sensitivity K = 4, DSSS = 4, 60 kbps

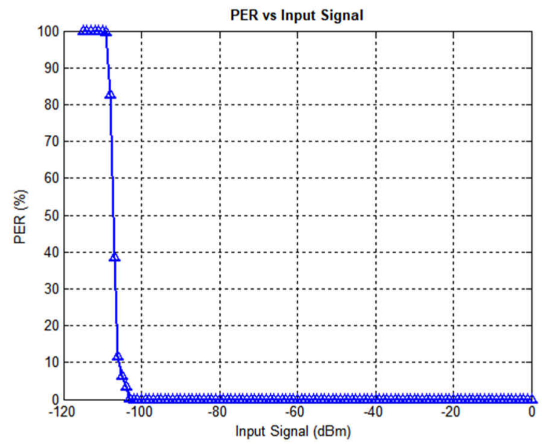

Figure 6-10. PER vs. Input Signal Level K = 4, DSSS = 4, 60 kbps

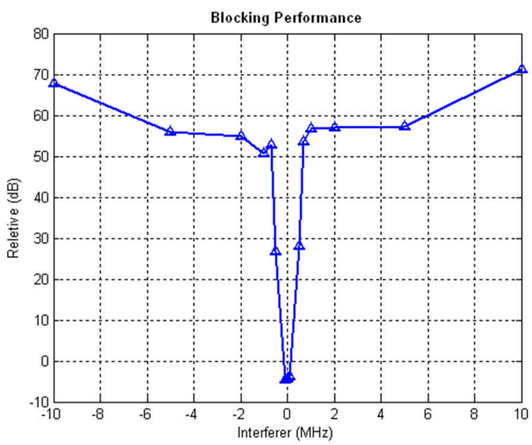

Figure 6-11. Blocking Performance K = DSSS = 4, 60 kbps

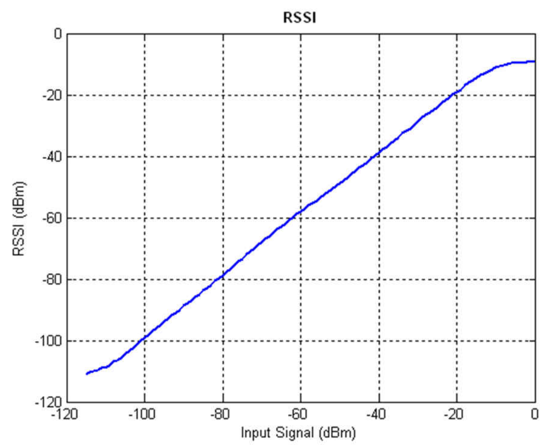

Figure 6-12. RSSI K = 4, DSSS = 4, 60 kbps

6.1.4 WB-DSSS 30 kbps, 2-GFSK, 195 kHz Deviation, 8x Spreading

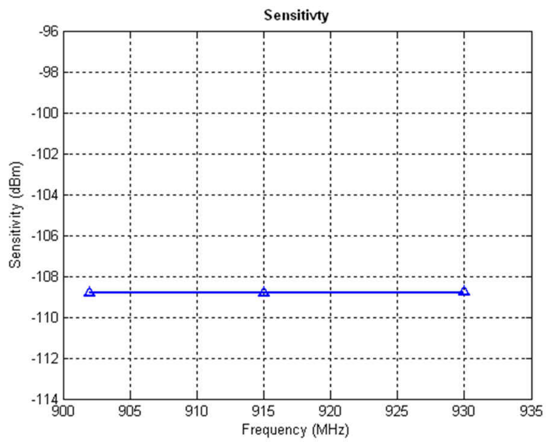

Figure 6-13. Sensitivity K = 4, DSSS = 8, 30 kbps

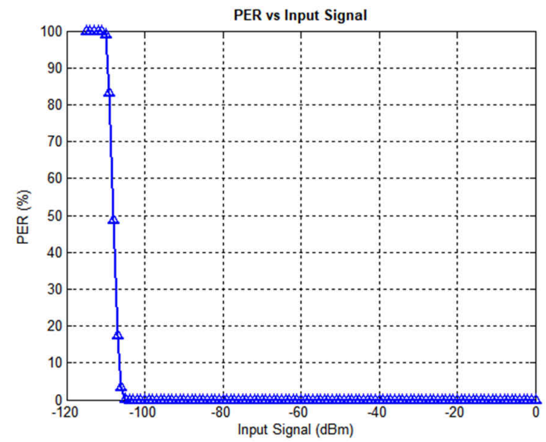

Figure 6-14. PER vs. Input Signal Level K = 4, DSSS = 8, 30 kbps

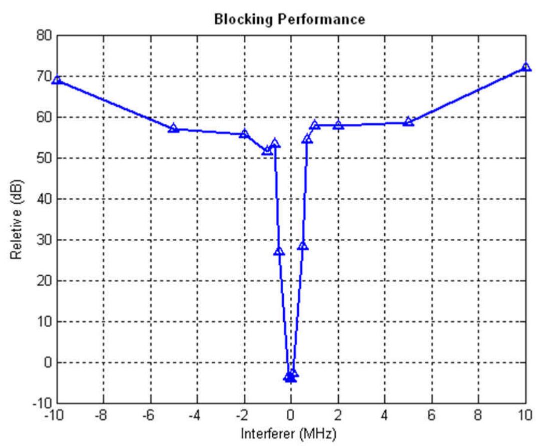

Figure 6-15. Blocking Performance K = 4, DSSS = 8, 30 kbps

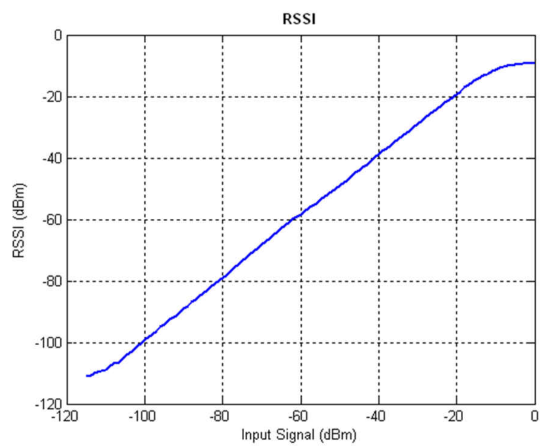

Figure 6-16. RSSI K = 4, DSSS = 8, 30 kbps

6.1.5 WB-DSSS Frequency Offset Tolerance

Figure 6-17 and Figure 6-18 show the frequency offset performance of the WB-DSSS scheme. In contrast to narrowband low data rate systems, the crystal accuracy is not critical in this case as the RX bandwidth is relatively large.

From the results, it can be seen that sensitivity remains unchanged for considerable amount of crystal drift (±70 ppm).

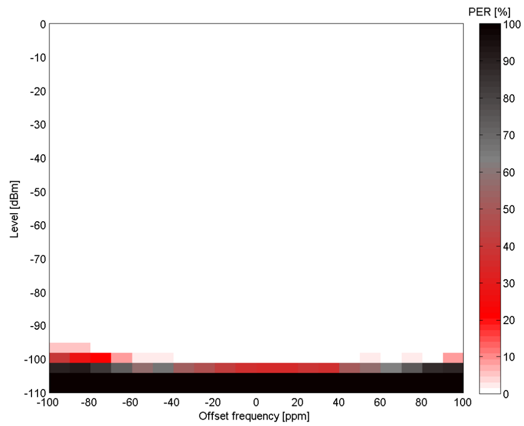

Figure 6-17. Frequency Offset Performance (915 MHz, K = 4, DSSS = 1, 240 kbps)

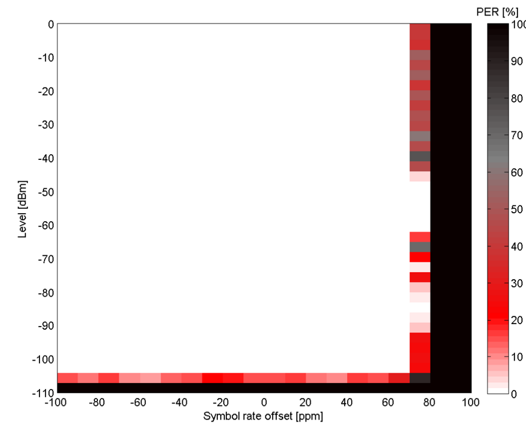

Figure 6-18. Frequency Offset Performance (915 MHz, K = 4, DSSS = 8, 30kbps)

6.2 Transmitter Performance and FCC 15.247 Measurements

Table 6-1 gives the FCC 15.247 digital modulation requirements that were tested.

Table 6-1. FCC 15.247 Digital Modulation Requirements [3]

Section	Requirements
15.247a2	The 6 dB bandwidth shall be at least 500 kHz
15.247b3	The maximum conducted power shall not exceed 1 W (+30 dBm)
15.247e	The power spectral density (PSD) shall not be greater than 8 dBm in any 3 kHz band during any time interval during continuous transmission

Most spectrum analyzers have a measurement option that automatically measures a fixed dB bandwidth. If this is not available, the 6 dB bandwidth must be measured manually by setting up markers.

Measurement setup consisted of the following:

- Six devices were tested
- Test results in Table 6-2 are average numbers of six devices
- SmartRF Studio was used to test the WB-DSSS cases

Table 6-2. FCC 15.247 Digital Modulation Results

DSSS	6 dB BW (15.247 a2)	Power (15.247 b)	PSD (15.247 d)
1	>500 kHz	19.5 dBm	9.2 dBm
2	>500 kHz	19.5 dBm	9.2 dBm
4	>500 kHz	19.5 dBm	9.5 dBm
8	>500 kHz	19.5 dBm	9.5 dBm

Note

To comply with the 8dBm/3kHz limit, the output TX power must be dropped until the limit is met.

For an explanation of marker lines for 6 dB bandwidth measurements, see Figure 6-19.

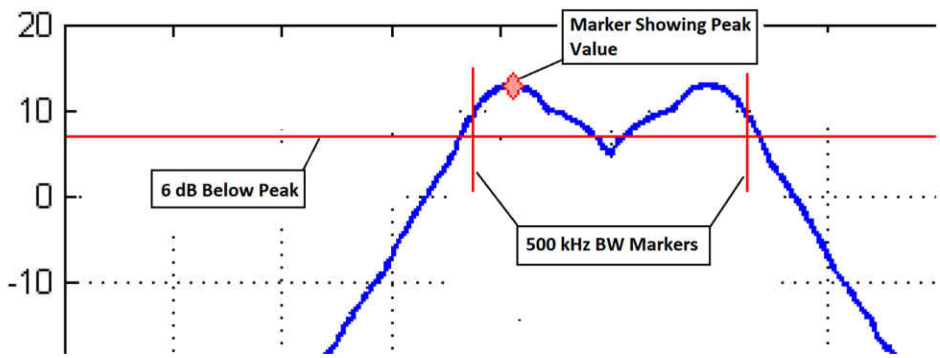

Figure 6-19. Explanation of 6 dB Bandwidth Figures

6.2.1 WB-DSSS 240 kbps, 2-GFSK, 195 kHz Deviation, 1x Spreading

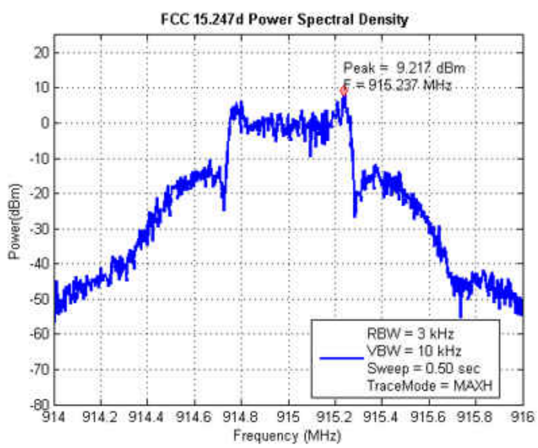

Figure 6-20. Transmit Spectrum PSD 8 dBm in any 3 kHz Bandwidth

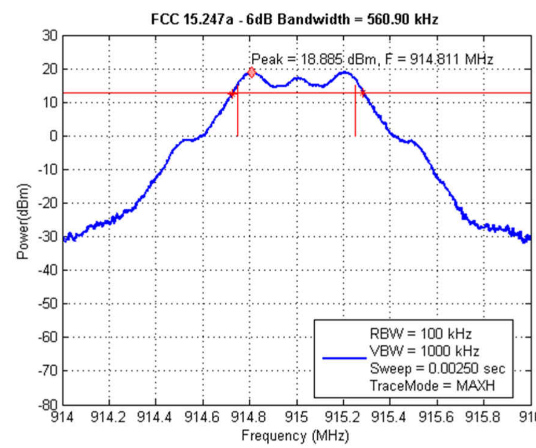

Figure 6-21. Transmit Spectrum 6 dB Occupied Bandwidth

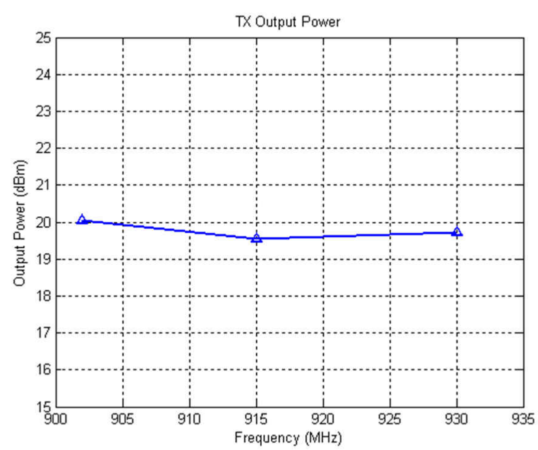

Figure 6-22. Max Output Power

6.2.2 WB-DSSS 120 kbps, 2-GFSK, 195 kHz Deviation, 2x Spreading

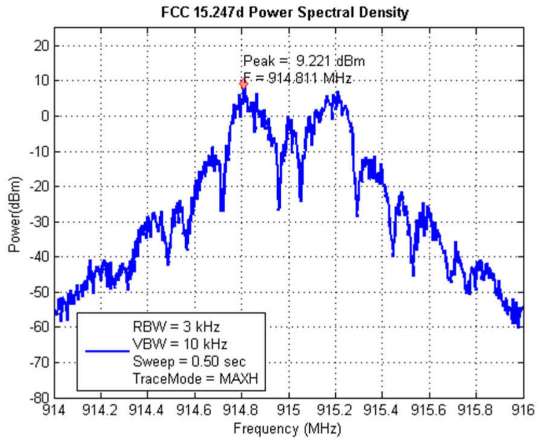

Figure 6-23. Transmit Spectrum PSD 8 dBm in any 3 kHz Bandwidth

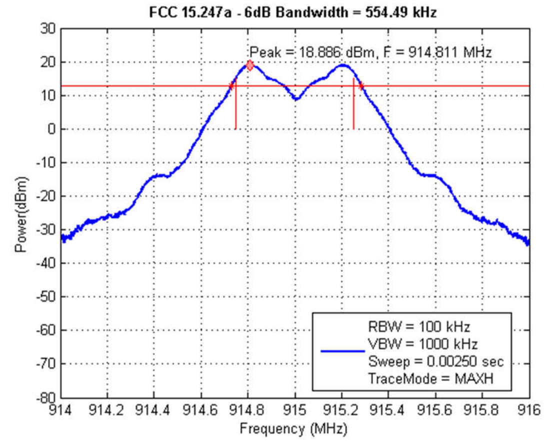

Figure 6-24. Transmit Spectrum 6 dB Occupied Bandwidth

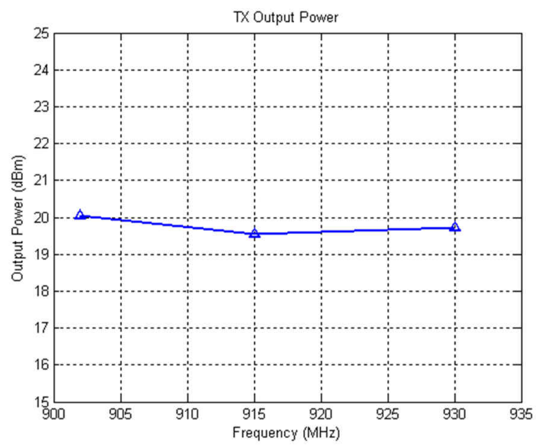

Figure 6-25. Max Output Power

6.2.3 WB-DSSS 60kbps, 2-GFSK, 195 kHz Deviation, 4x Spreading

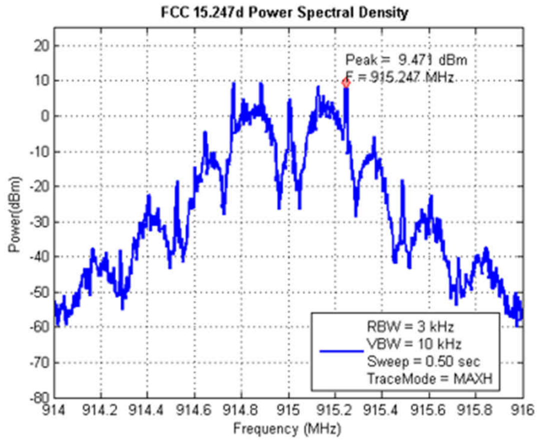

Figure 6-26. Transmit Spectrum PSD 8 dBm in any 3 kHz Bandwidth

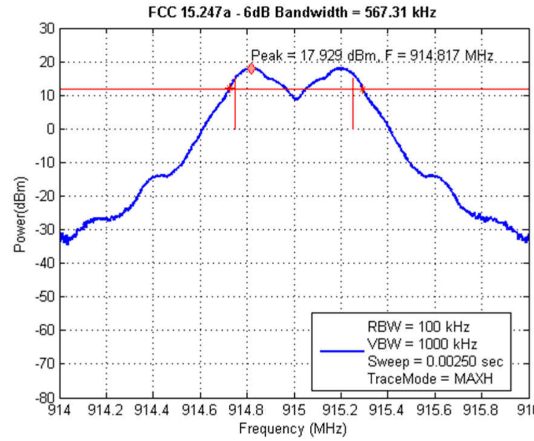

Figure 6-27. Transmit Spectrum 6dB Occupied Bandwidth

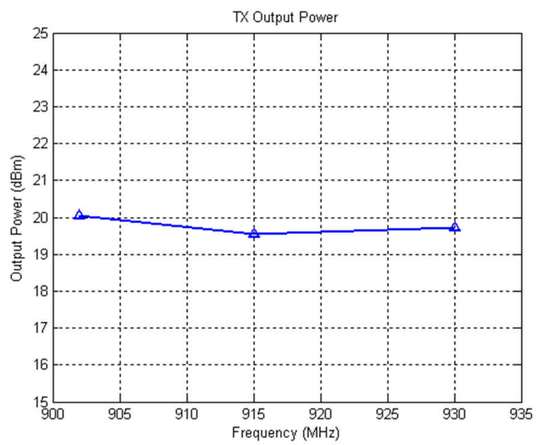

Figure 6-28. Max Output Power

6.2.4 WB-DSSS 30 kbps, 2-GFSK, 195 kHz Deviation, 8x Spreading

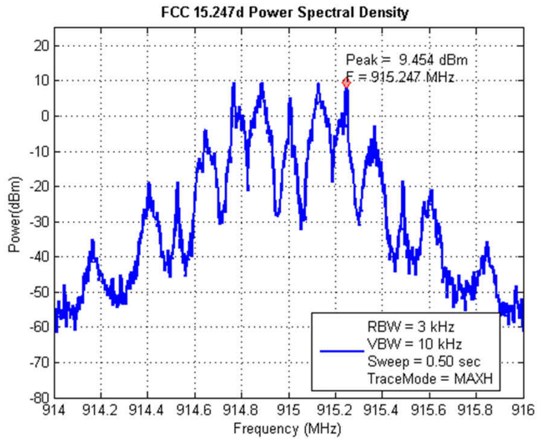

Figure 6-29. Transmit Spectrum PSD 8 dBm in any 3 kHz Bandwidth

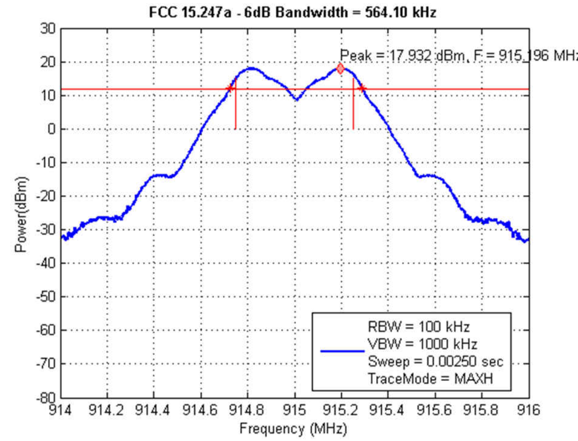

Figure 6-30. Transmit Spectrum 6 dB Occupied Bandwidth

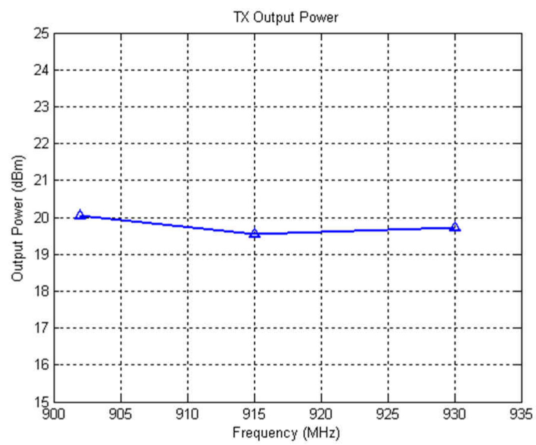

Figure 6-31. Max Output Power

7 References

1. Texas Instruments: *CC13x2, CC26x2 SimpleLink™ Wireless MCU Technical Reference Manual*
2. FCC 15.247
3. SmartRFTM Studio
4. Sysconfig Tool
5. Bernard Sklar. “Digital Communications – Fundamentals and Applications”. 2nd Edition.

8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (April 2021) to Revision A (November 2021)	Page
• Update was made in the Abstract of this document.	1
• Updated the numbering format for tables, figures and cross-references throughout the document.	3
• Update was made in Section 2.2	4
• Updates were made in Section 3	5
• Updates were made in Section 4	5

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