TEXAS INSTRUMENTS

TPS65910 Silicon Errata
ES1.1

This document describes the TPS65910 bugs, limitations, and enhancements with suggested workarounds. As this information is dated, updates will be provided.

Contents

1   Glitch on SDA-SCL not managed correctly by the I²C IP

Impact:

The standard specifies that the I²C transfer should restart on a start event in all cases. The current design does not support two consecutive Start conditions. This can cause the first real access after such a glitch to be corrupted.

Description:

An unexpected glitch on SDA and SCL can generate a wrong start event. In the current design, the SCL line must toggle two times to detect a new start event and completely restart the I²C access; hence the real start event is not detected in the case of a single SCL toggle.

Workaround:

Repeat I²C access.

2 DCDC o/p voltage can go higher than programmed value

Impact:

VDDI, VDD2, and VIO output programmed voltage level can go higher than expected or crash, when coming out of PFM to PWM mode or using DVFS.

Description:

When DCDC CLK SYNC bits are 11/01:

- VIO 3-MHz oscillator is the source clock of the digital core and input clock of VDD1 and VDD2
- Turn-on of VDD1 and VDD2 HSD PFET is synchronized or at a constant phase shift
- Current pulled though VCC1+VCC2 is I_{load}(VDD1)+ I_{load}(VDD2)
- The 3 HSD PFET will be turned-on at the same time, causing the highest possible switching noise on the application. This noise level depends on the layout, the VBAT level, and the load current. The noise level increases with improper layout.

When DCDC CLK SYNC bits are 00:

- VIO 3-MHz oscillator is the source clock of digital core
- VDD1 and VDD2 are running on their own 3-MHz oscillator
- Current pulled though VCC1+VCC2 average of I_{load}(VDD1)+I_{load}(VDD2)
- The switching noise of the 3 SMPS will be randomly spread over time, causing lower overall switching noise.

Workaround:

Set DCDCCTRL_REG [1:0] = 00.

3   Revision History

Version	Date	Notes
A	January 2014	Added Section 2

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