TPS65930/TPS65920 Layout Guide

User's Guide

Literature Number: SWCU058
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Contents

List of Figures

List of Tables

TPS65930/TPS65920 Layout Guide

1 Introduction

The TPS65930 device is an integrated power-management and audio codec and the TPS65920 device is a power-management device for use in mobile and portable applications. These devices meet the power and peripheral requirements of the Texas Instruments OMAP™ family.

This document describes constraints and special guidelines for designing with the TPS65930 or TPS65920. The TPS65930/20 are high-end analog companion devices that contain several blocks with different layout constraints. This guide explains these constraints and explains good layout practice through examples.

2 Signal Routing

The TPS65930 and TPS65920 ball grid arrays (BGAs) are designed with a technology called Via Channel™ array, which makes possible significant cost savings for the printed circuit board (PCB).

Via Channel technology depopulates the balls on the BGA chip package in a shape that lets the vias be concentrated in channels. This yields several advantages:

- Because the vias are in channels, the via outside diameter (the annular ring) can be larger than it would be if it were between the balls. This makes PCB manufacturing less expensive because larger vias are possible.
- Unlike normal BGA array PCB routing, vias are grouped in a radial pattern instead of a series of concentric rings around the middle of the chip. Traces are more easily routed out of the inner parts of the chip because they are not restricted to narrow paths among many rows of vias.

2.1 Outer Row Routing

For the first two rows (from the outside in) of the BGA, the balls are arranged to allow wider traces than would otherwise be possible. The first (outside) row supports any size trace, because the trace comes from the PCB ball and goes out on the PCB. Normally, the second row traces must be routed between the first row of the PCB ball lands. On this package, the second row traces are routed through an open channel where the BGA ball has been removed to allow wider traces. If routed correctly, the TPS65930/20 parts allow a 5 mil (0.125 mm) trace in all areas.

2.2 Via Channel Inner Routing

Starting at the third row, as with any BGA package, vias are necessary. These vias are standard 18 mil (0.45 mm) diameter vias with 8 mil (0.2 mm) – 10 mil (0.25 mm) finished hole sizes. The hole size is not important as long as the board can be built by the board shop with good yield. Because the majority of the vias are in via channels, only some vias must be placed between balls. Generally, these are in areas where all the surrounding balls share the same net. Because the via ring is larger than one that would normally fit between these balls with the required clearance, the layout tool may flag a design rule check (DRC) error; however, this is a false warning because there is no risk of shorting to a nearby pad because the balls are all on the same net.

2.3 Results

PCB layout rules are:

- 5 mil (0.125 mm) maximum trace

- 18 mil (0.45 mm) maximum via diameter
- No blind, stacked, buried, or micro vias
- Only two signal layers required

These rules are the results of the BGA escape. This results in a PCB design that must be even more cost-effective than a 0.8-mm pitch BGA part of equal pin count.

3 Signal Grouping

This section provides an overview of the main signal groups on the device.

3.1 Power Lines

Table 1 lists signals that require an enlarged net width because of high current.

Table 1. Signals That Require an Enlarged Net Width

Group	BGA Pin	Pin Name	Function
Power inputs	H13	VINT.IN	Power
	H14	VPLLA3R.IN	Power
	L1	VAUX12S.IN	Power
	K1	VDAC.IN	Power
	C1	VMMC1.IN	Power
	B7	IO.1P8	Power
	N9	VBAT.USB	Power
	N5	VBAT	Power
	A10	VBAT.RIGHT	Power
	H9	BKBAT	Power
	P7	CP.IN	Power
Power outputs	P8	VBUS	Power
	N2	VAUX2.OUT	Power
	B1	VMMC1.OUT	Power
	L2	VDAC.OUT	Power
	G14	VPLL1.OUT	Power

3.2 Dc/dc Signals

For information about the signals listed in Table 2, see Section 4.1 *Dc/dc Converters*.

Table 2. Dc/dc Signals

Group	BGA Pin	Pin Name	Function
Dc/dc	D13	VDD1.IN	Power
	D12	VDD1.IN	Power
	D14	VDD1.IN	Power
	C11	VDD1.SW	Power
	C12	VDD1.SW	Power
	C13	VDD1.SW	Power
	E14	VDD1.FB	Power
	M13	VDD2.IN	Power
	M12	VDD2.IN	Power
	N11	VDD2.SW	Power
	P11	VDD2.SW	Power

Table 2. Dc/dc Signals (continued)

Group	BGA Pin	Pin Name	Function
	N13	VDD2.FB	Power
	M2	VIO.IN	Power
	M3	VIO.IN	Power
	N4	VIO.SW	Power
	P4	VIO.SW	Power
	M4	VIO.FB	Power

3.3 Grounds

Sensitive grounds must be routed in a separate restricted plane area to avoid power grounds and other sensitive grounds. Impedance on all grounds must be minimized (see Table 3).

Table 3. Grounds

Group	BGA Pin	Pin Name	Function
Sensitive GND	D2	MICBIAS.GND	Audio
	K13	AGND	Reference
Digital GND	H10	DGND	Digital
Power GND	C7	AVSS4	Power
	N14	AVSS3	Power
	L7	AVSS2	Power
	G2	AVSS1	Power
Dc/dc GND	N3	VIO.GND	Power
	P3	VIO.GND	Power
	A12	VDD1.GND	Power
	B11	VDD1.GND	Power
	B12	VDD1.GND	Power
	N12	VDD2.GND	Power
	P12	VDD2.GND	Power

3.4 Decoupling for Internal Functions

Table 4 lists decoupling for internal functions. Decoupling capacitors for these signals must be placed close to the relevant pin.

Table 4. Decoupling for Internal Functions

Group	BGA Pin	Pin Name	Function
Internal power decoupling	H1	VINTANA1.OUT	Power
	J2	VINTANA2.OUT	Power
	A5	VINTANA2.OUT	Power
	K12	VRTC	Power
	J13	VINTDIG	Power

3.5 Power for USB

Table 5 lists power for USB.

Table 5. Power for USB

Group	BGA Pin	Pin Name	Function
USB	M8	VUSB.3P1	Power
	M7	VINTUSB1P5	Power
	N8	VINTUSB1P8	Power

3.6 Critical Signals

Critical signals must be shielded to avoid noise sources (see Table 6).

Table 6. Critical Signals

Group	BGA Pin	Pin Name	Function
ADC	H2	ADCIN0	Input
	F2	ADCIN2	Input
32-kHz clock	M10	32KCLKOUT	Output
	L14	32KXIN	Input
	K14	32KXOUT	Output
Reference	L13	VREF	Power
Audio	E2	MICBIAS1.OUT	Output
	D1	MIC.MAIN.P	Input
	E1	MIC.MAIN.M	Input
	D2	MICBIAS2/VMIC2	Output
	G1	AUXR	Input
	A7	AUXR PreDrive.LEFT	Output
	A8	PreDrive.RIGHT	Output
USB	n10	DP(1)	
	P10	DN(1)	

(1) DP/DN are 90 Ω differential signal adapted. For more information about these signals, see Section 4.2, *USB Transceiver*.

3.7 Clocks and Buses

All clocks and higher-frequency digital interface signals must have spacing of 3W. Buses must be routed together to provide similar timing on all the signals in the bus (see Table 7).

Table 7. Clocks and Buses(1)

Group	BGA Pin	Pin Name	Frequency
UTMI+ low pin interface (ULPI) bus	K11	UCLK	60 MHz
	H12	STP	
	J8	NXT	
	H11	DIR	
	E11, G12, G9, E12, G10, G11, K10, L10	DATA[7:0]	
Inter-IC sound (I2S™) audio	H3	I2S.CLK	6.14 MHz
	K2	I2S.SYNC	
	K4	I2S.DIN	
	K3	I2S.DOUT	
Inter-integrated circuit (I^2C™) control bus	B4	I2C.CNTL.SCL	3.4 MHz
	C3	I2C.CNTL.SDA	

(1) All clock signals and buses are 50 Ω adapted.

Table 7. Clocks and Buses (continued)

Group	BGA Pin	Pin Name	Frequency
I2C SmartReflex™ bus	C5	I2C.SR.SCL	3.4 MHz
	B3	I2C.SR.SDA	
Clocks	M11	HFCLKOUT	12 – 38.4 MHz
	A8	HFCLKIN	

4 Layout Guidelines

4.1 Dc/dc Converters

The dc/dc board layout is critical for the correct function and reliability of the device. Wide and short traces must be used for the main current paths as indicated in bold red lines in Figure 1.

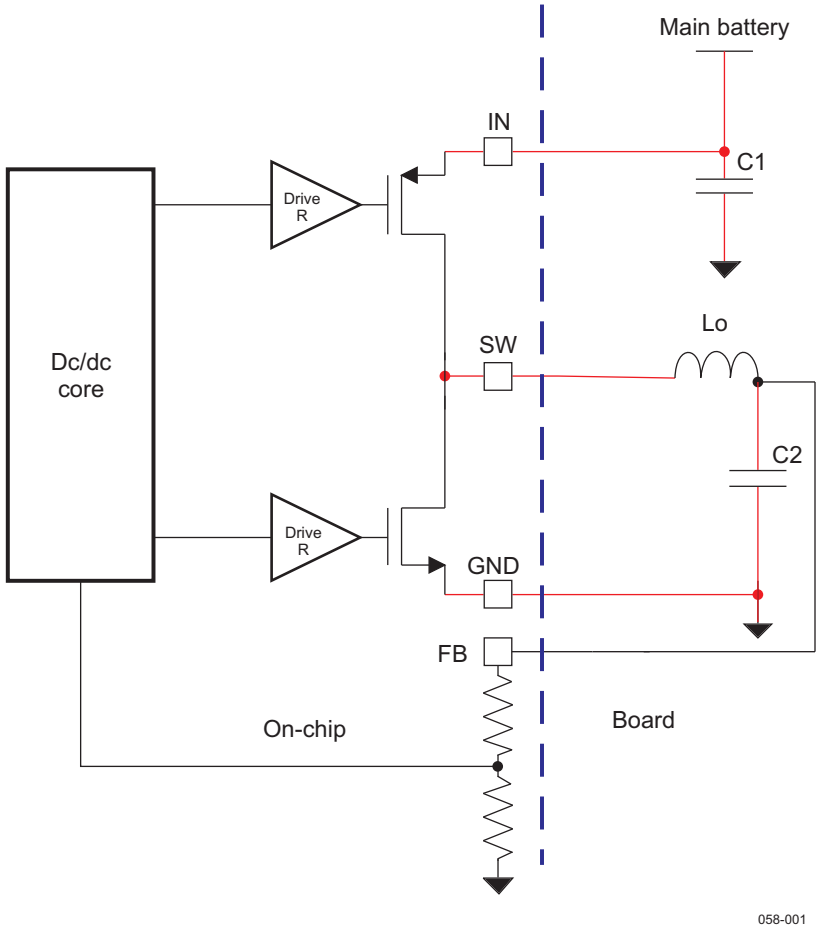

Figure 1. Dc/dc Converters

The connection between C1 and the IN ball must be less than 5 mΩ and the connection between the inductor and the software ball must be less than 8 mΩ.

WARNING

Failure to meet these parameters can severely affect the performance and reliability of the device.

The input capacitor must be placed as close as possible to the integrated circuit (IC) pins and the inductor and output capacitor. Grounds must be separated between the control and the power devices to minimize the effects of ground noise. Connect these ground nodes (star point) underneath the IC and make sure that small signal components returning to the GND pin do not share the high current path of C1 and C2.

The output voltage sense line FB must be connected directly to the output capacitor and routed away from noisy components and traces (such as the software line). Its trace must be minimized and placed where no signals can affect the voltage level, ideally, shielded by a dedicated ground.

4.2 USB Transceiver

Lay out the universal serial bus (USB) transceiver according to the following guidelines:

- With minimum trace lengths, route high-speed (HS) clock and HS USB differential pairs first.
- Place the USB connector close to the board edge. Place the OMAP processor and the TPS69530/20 close together to minimize the ULPI bus trace lengths.
- Place the low-capacitance ESD protections as close as possible to the USB connector, with no external devices between them. TPD3E001 is very convenient here because of its small size.
- Because common mode chokes degrade signal quality, use them only if EMI performance enhancement is absolutely necessary.
  Place the common mode choke (if required) as close as possible to the USB connector but after the ESD devices.
- Maintain the maximum possible distance between HS clocks/periodic signals to HS USB DP/DN differential pairs and any connector leaving the PCB (such as I/O connectors, control and signal headers, or power connectors). Consider routing the signals in a tunnel.
- DP and DN routing considerations:
  - Route the DP/DN trace pair together from the device to the USB connector with an optimal trace length of 5 cm and a maximum trace length 1-way delay of 0.5 ns.
  - Match DP/DN trace lengths. The maximum allowable mismatch allowable is 150 mils (~0.4cm).
  - Route DP/DN signals with 90 Ω differential impedance and 22.5~30 Ω common-mode impedance.
  - Use an impedance calculator to determine the trace width and spacing required for the specific board stackup being used.
  - Keep the maximum possible distance between DP and DN signals from the other platform clocks, power sources, and digital and analog signals.
  - Use 20-mil minimum spacing between DP/DN and other signal traces for optimal signal quality.
  - Do not route DP/DN over/under crystals, oscillators, clock synthesizers, magnetic devices, or ICs that use clocks.
  - Avoid changing the routing layer for DP/DN traces. If this is unavoidable, use multiple vias.
  - Minimize bends and corners on DP/DN traces: Route the DP/DN using minimum vias and corners. This reduces signal reflections and impedance changes. When it is necessary to turn 90 degrees, use two 45-degree turns or an arc instead of making a single 90-degree turn. This reduces reflections on the signal by minimizing impedance discontinuities.
  - Avoid stubs on DP/DN, because stubs cause signal reflections and affect signal quality. If a stub is unavoidable in the design, no stub must be greater than 200 mills (~0.5 cm).
  - Route DP/DN over continuous planes (VCC or GND) with no interruptions. Avoid crossing over anti-etch (plane splits), because this increases inductance and radiation levels by forcing a greater loop area. Likewise, avoid changing layers with HS traces. It is preferable to change layers to avoid crossing a plane split. If crossing a plane split is completely unavoidable, the correct placement of stitching caps can minimize the adverse effects on EMI and signal quality performance caused by crossing the split.
  - Avoid anti-etch on the ground plane.

  - Route DP/DN signals with at least 25 mils (~0.65 mm) away from any plane splits.
- Follow the 20 × h thumb rule by keeping traces at least 20 × (height above the plane) away from the edge of the plane (VCC or GND, depending on the plane the trace is over).
- Minimize the length of the HS clock and periodic signal traces that run parallel to DP/DN to minimize crosstalk. Based on EMI testing experience, the minimum suggested spacing to clock signals is 50 mils.
- The impedance from wire to wire must be from 80 to 100 Ω and from track to ground 50 Ω. For more information, see the USB specification.
- Route the USB connector ground pin to the analog ground plane of the device with multiple vias connections.

Figure 2 shows sample trace characteristics.

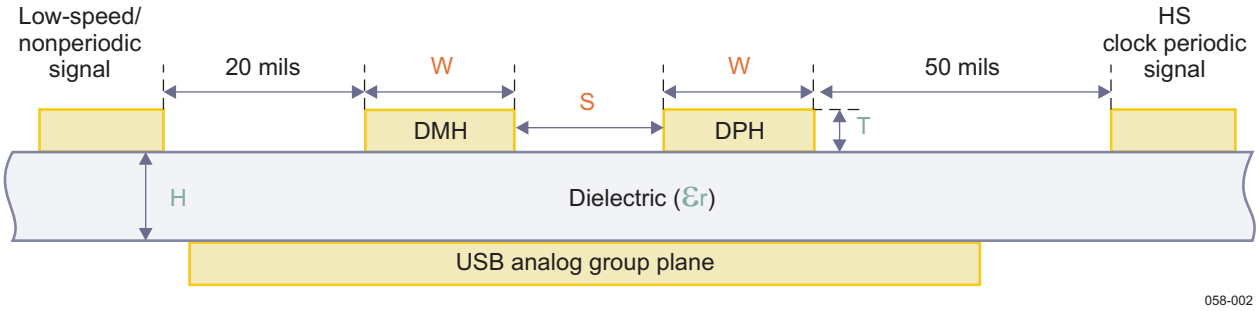

Figure 2. Sample Trace Characteristics

Table 8 lists sample trace characteristics.

Table 8. Sample Trace Characteristics

PCB Characteristics			Trace Characteristics	
ξr	H(mils)	T(mils)	W(mils)	S(mils)
4.6	4.5	1.4	7.5	7.5
3.9	5.5	1.7	10	10

4.2.1 ULPI Interface

The ULPI signals for USB between OMAP and TPS65930/20 must be considered because the speed is approximately 60 – 70 MHz. Signals are digital and therefore can introduce noise to other signals if the capacitive coupling is not considered.

Lay out the USB transceiver according to the following guidelines:

- Route the ULPI 12-pin bus as a 90 Ω single-ended adapted bus. Trace impedance from track to ground must be from 80 to 100 Ω.
- Route the ULPI 12-pin bus with minimum trace lengths and a strict maximum of 50 mm, to ensure timing.
- Keep the lengths of signals in the ULPI bus as equal as possible and route signals in parallel.
- Route the ULPI 12-pin bus as clock signals and set a minimum spacing of three times the trace width (S<3W).
- If the 3W minimum spacing is not respected, the minimum spacing for clock signals based on EMI testing experience is 50 mils (1.27 mm).
- Route the ULPI 12-pin bus with a dedicated ground plane.
- Keep the maximum possible distance between the UCLK and the other platform clocks, power sources, and digital and analog signals.

4.2.2 USB Power Supplies

Lay out the USB power supplies according to the following guidelines:

- VBUS must be a power plane from the device VBUS ball to the USB connector. If a power plane is not possible, VBUS must be as large as possible.
- The VBUS bypass capacitance required by the USB 2.0 specification must be split into two equal component capacitors of 2.2 uF, one as close as possible to the device VBUS pin, the other as close as possible to the USB connector.
- Place charge-pump fly and tank capacitors as close as possible to CP.CAPP and CP.CPAM. Target 10 mΩ or less trace resistance.
- Route a dedicated ground for the charge pump CP.GND connected to the analog ground.
- The trace width from the VBUS source to the bypass capacitor, over the current protection device, and the USB connector power and ground pins, must be at least 0.050 inches wide to ensure adequate current carrying capability.
- The trace width for the same VBUS current path must be at least 1.5- to 2-oz. copper on the outer layer.
- Wider trace widths are preferred. However, if the routing channels are restricted, it is important to achieve the same cross-sectional area by routing two or more power traces using different routes.

4.3 32-kHz Oscillator

The 32-kHz clock circuit is sensitive. Special considerations must be taken to prevent any influence on the circuit.

To protect the circuit from disturbance in the ground plane, a special restricted area can be defined. A plane can be placed in the layer directly under the components, to be shared only with the AGND ball K13 on the TPS65930/20.

Figure 3 shows the ground layer in this suggested layout; Figure 4 shows the component layer.

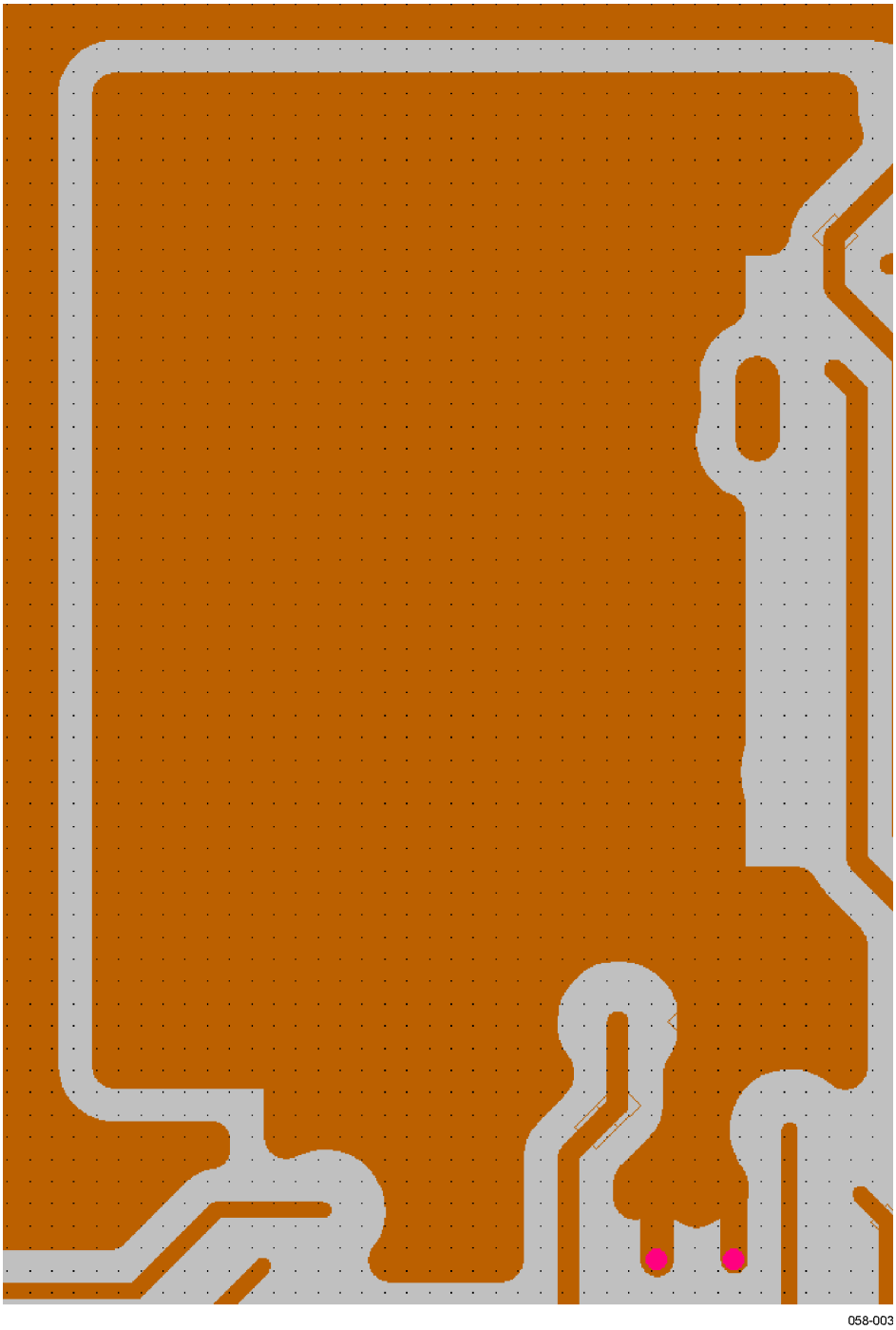

Figure 3. Ground Layer

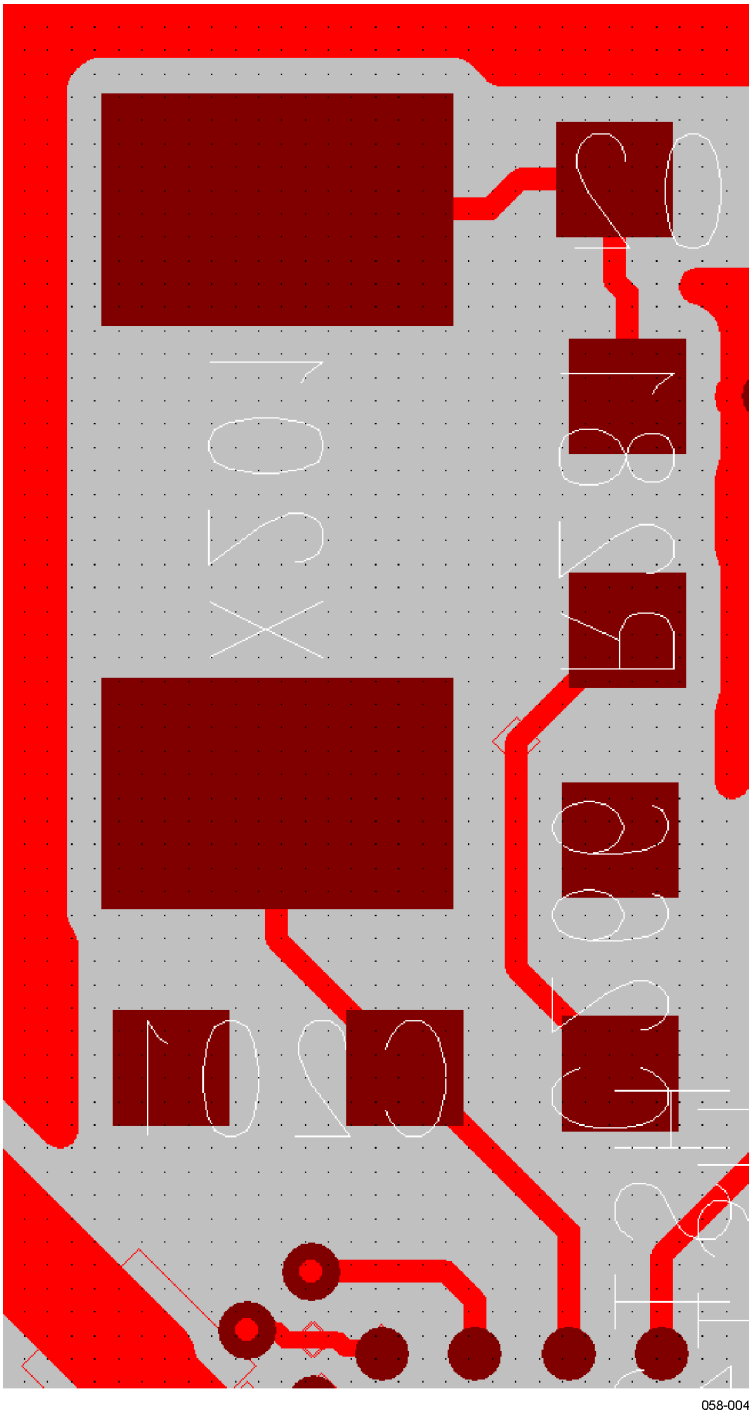

Figure 4. Component Layer

4.3.1 Use of 32-kHz Output

If the 32KCLKOUT signal must be distributed to more than one device, use star topology to avoid timing differences. Tunneling must also be used to prevent noise on this clock line from other signals.

4.4 Audio Codec (TPS65930 Only)

4.4.1 Microphone Input

The microphone differential signals (MIC.MAIN.P and MIC.MAIN.N) are very low-level and must be balanced and routed in parallel, the same distance from start to end, the same impedance for both signals.

Figure 5 and Figure 6 show typical schematics for microphone input. The microphone filtering capacitor must be as close as possible to the microphone. The other components must be as close as possible to the device.

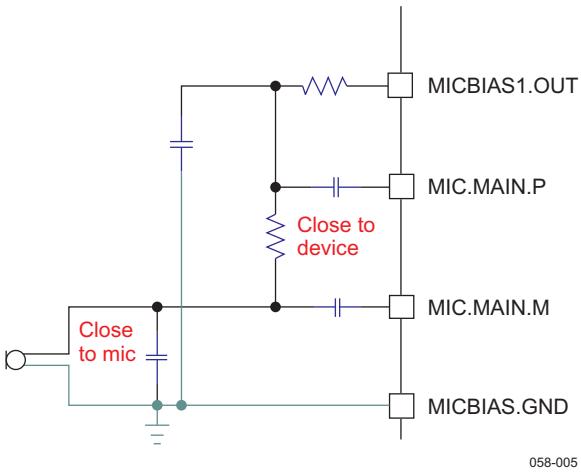

Figure 5. Microphone Pseudodifferential

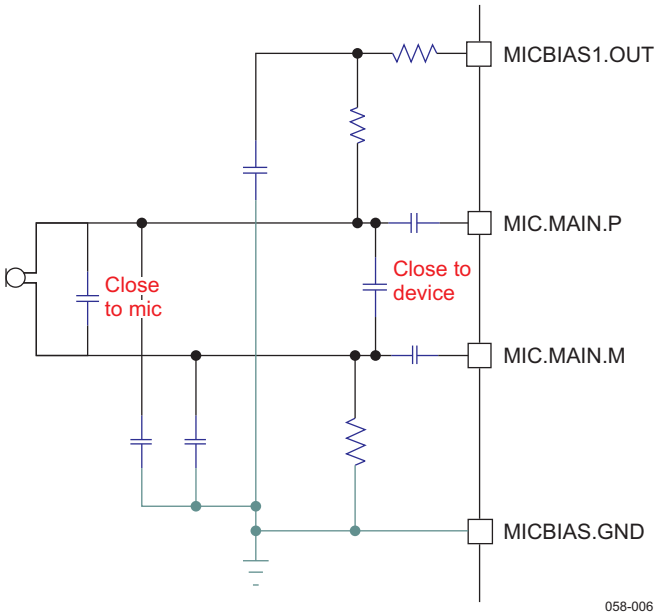

Figure 6. Microphone Differential

Because the microphone bias (MICBIAS1) uses MICBIAS.GND as a reference ground, this ground is very

sensitive, and special considerations must be taken. To prevent noise on the microphone from disturbance in the ground plane, a special restricted area can be defined. A plane can be defined in which the microphone ground and MICBIAS.GND are connected. This plane can be shared with the AGND ball K13 on TPS65930, but must not be shared with the AVSS4 ground. This plane cannot have coupling with other ground planes, and restricted areas in neighboring layers are required.

4.4.2 Line Input

The AUXR signal is a single-ended audio line input. The main layout guideline for this input is to place capacitor C1 close to the device (see Figure 7).

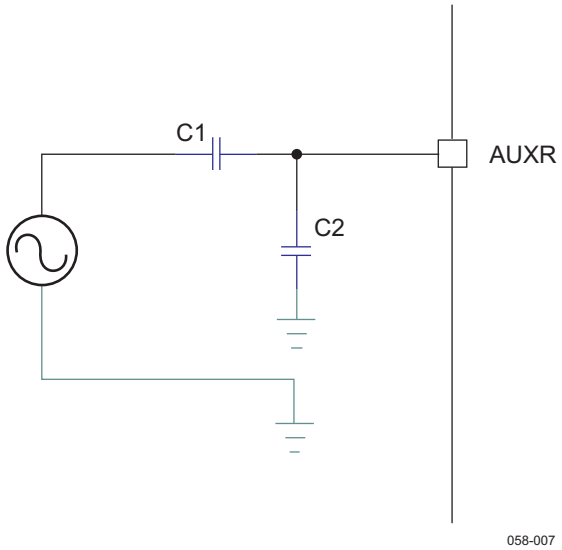

Figure 7. Line Input

4.4.3 Line Output

The PreDriv.LEFT and PreDriv.RIGHT signals are the stereo audio output lines. To prevent audio degradation, these signals must be shielded and routed to avoid noise sources, especially those that generate noise in the audio range.

Typically, these signals drive external class-D amplifiers, as shown in Figure 8. Resistors Ri and capacitors Ci must be as close as possible to the external class-D chip.

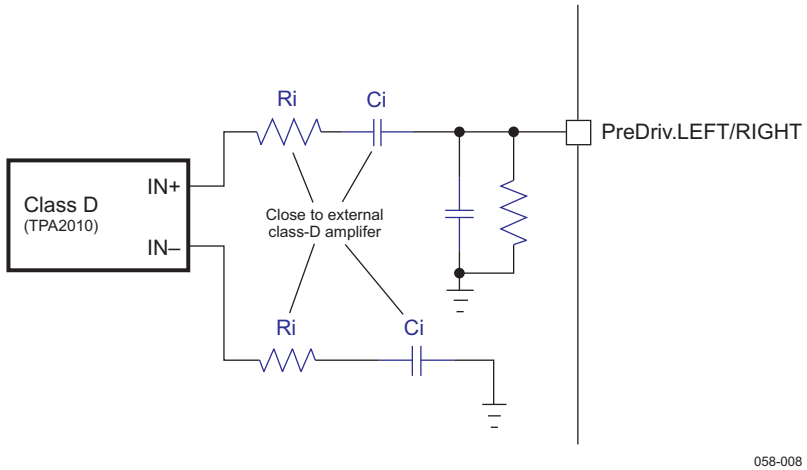

Figure 8. Line Output

Use individual audio grounds for each output. These grounds must be connected to AGND.

4.5 LED/Vibrator Drivers

To minimize the risk of EMI emission from the open-drain output, place external components as close as possible to the device pad/pin. To minimize degradation of the function, make the connecting PCB traces as wide as possible to reduce impedances.

5 Routing of Parallel Balls

Routing of parallel balls can be divided into three scenarios:

- High-power supply outputs
- High-power supply inputs
- Multiple power inputs

5.1 Signals That May Not be Directly Connected to High-Power Nets

VPLL3R.IN is the supply for the internal phase-locked loop (PLL). Because it is sensitive to noise on the supply line, it requires a battery connection separate from the other supply balls. This must be considered during layout. A small filter can be extremely useful in this case.

5.2 High-Power Outputs

When routing high-power supply outputs, ensure low impedance in the tracks to ensure low IR drop. It is crucial that the routing of the parallel balls distributes power evenly between the balls. This can be done by connecting the parallel balls to a power plane. Current distribution and hence the distribution of power can be controlled by deliberately connecting to the plane with a well-planned distribution of via connections.

5.3 High-Power Inputs

To meet requirements for IR drop, high-power supply inputs must be routed with low-impedance tracks. Decoupling capacitors are recommended: one per supply connection; these must be as close as possible to the inputs. To ensure good decoupling, power must first pass the footprint of the decoupling capacitor and then continue to the power input. Even the smallest stub from the power track to the capacitor significantly degrades the effect of the capacitor. To ensure the best possible performance from the capacitor, ground the capacitor with a solid connection to the same ground as the high-power device.

5.4 Multiple Power Inputs

Multiple power inputs means the same power source distributed to a number of devices or multiple power connections on a single device. In this case, select a distribution point from which to branch out the power supply to various devices or to various locations on the same device.

5.4.1 Distribution Point

A good distribution point can be the decoupling capacitor of the device that generates the power or a similar point in the PCB where there is good decoupling of the power and low impedance tracks from the power supply. From this point, power is distributed to where it is needed. Use the distribution point as a star point.

CAUTION

Do not distribute power in a daisy-chain manner. This causes the quality of the power to deteriorate as the chain moves from one power consumer to the next.

5.4.2 Connecting Multiple Pins on a Single Device

When connecting multiple pins on a device, assess the amount of decoupling. If in doubt, provide one capacitor per pin, if possible. Group pins that can share decoupling, route the power from the point of distribution to the decoupling capacitor, and route from the pins to the decoupling capacitor to create a common star connection at the decoupling capacitor. This prevents balls from affecting each other by injecting ripple/noise. Do not make interconnections between parallel balls in places other than at the decoupling capacitor.

6 Signals That Require Tunneling or Shielding

Tunneling and shielding in the PCB ensure the integrity of sensitive signals. Tunneling works best on a dedicated layer in the PCB on which the signals are routed. The signals are routed with unbroken ground on both sides, and the shield is formed by having ground on the PCB layers above and below the signals. The surrounding ground planes must be firmly connected with vias to ensure connection between the ground layers and to the main ground in the PCB. When using tunneling on signals, ensure that the signals are not accidentally exposed to other signals, especially HS digital signals.

Table 9 lists the characteristics of signals that require tunneling or shielding.

Table 9. Signals That Require Tunneling or Shielding

Signal	Description
MICP	Positive signal on the differential microphone input. Signal level is in mV range.
MICN	Negative signal on the differential microphone input. Signal level is in mV range.
PreDriv.LEFT	Audio left output signal. Shield to prevent coupling of noise and degradation of audio performance.
PreDriv.RIGHT	Audio right output signal. Shield to prevent coupling of noise and degradation of audio performance.
DP/DN	USB interface signals that operate at 480 MHz. These lines must be protected to prevent coupling to and from other signals
XTAL	Connection to the 32-kHz crystal. Because the 32-kHz oscillator is a very low-power circuit, this signal must be protected.
26-MHz	Clock signal. Although this signal is active only when the system is in active mode, it is a higher-frequency clock that can degrade other signals or cause system clocking issues if the clock signal is not clean. Thus, it must be routed in a tunnel.

Appendix A Incorrect Dc/dc Converter Layout

A.1 Incorrect Dc/dc Converter Layout

This section contains examples of incorrect PCB design that required a redesign.

A.1.1 Example 1

In Figure A-1, the designer has connected VBAT for VDD1 input with a connection that is too small, and does not respect the 5 mΩ requirement specified in Section 4.1, *Dc/dc Converters*. The second problem is that the design connects balls VINT.IN and VPLLA3R.IN to the same line. These balls supply sensitive circuits in the TPS65930 that are affected by the current drawn by VDD1. The inrush current for VDD1 causes a ripple in the supply line that must minimized before it is propagated to other circuits.

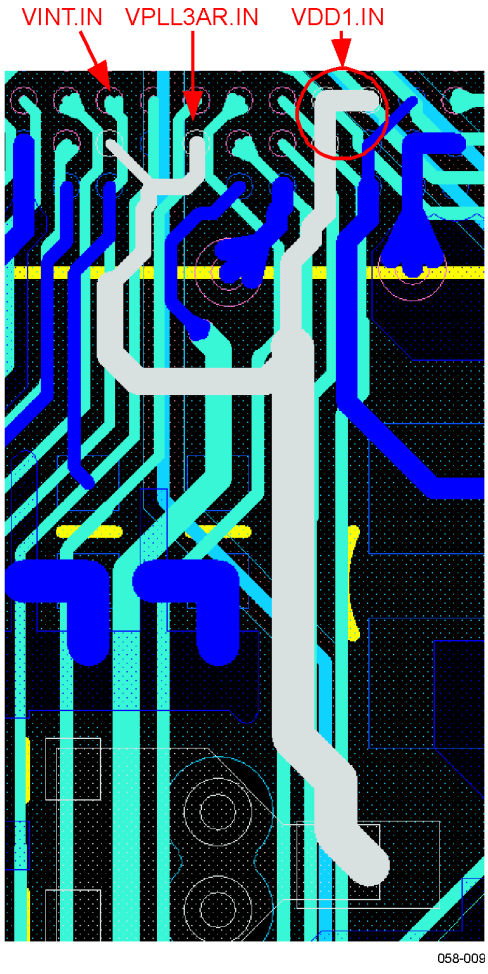

Figure A-1. Example 1

Solution

Use the small impedances in the PCB and the decoupling capacitors to minimize impedance for the VDD1.IN connection. Make a connection directly from the tank capacitor to supply VINT.IN and VPLL3AR.IN. This is called star topology.

A.1.2 Example 2

In Figure A-2, the outputs of the VDD1 DCDC are connected to three balls (C11, C12, and C13) to support the high current in the connection. A board is made with a very thin connection from VDD1.OUT to the coil. This connection is made only on the top layer.

The impedance in this connection does not respect the 8 mΩ routing requirement and will affect the efficiency and reliability of the device.

After the coil, a plane is defined, and this is acceptable. However, it is unusual that the design uses a plane from the coil to the consumer but not from the DC/DC converter to the coil. This will become a bottleneck.

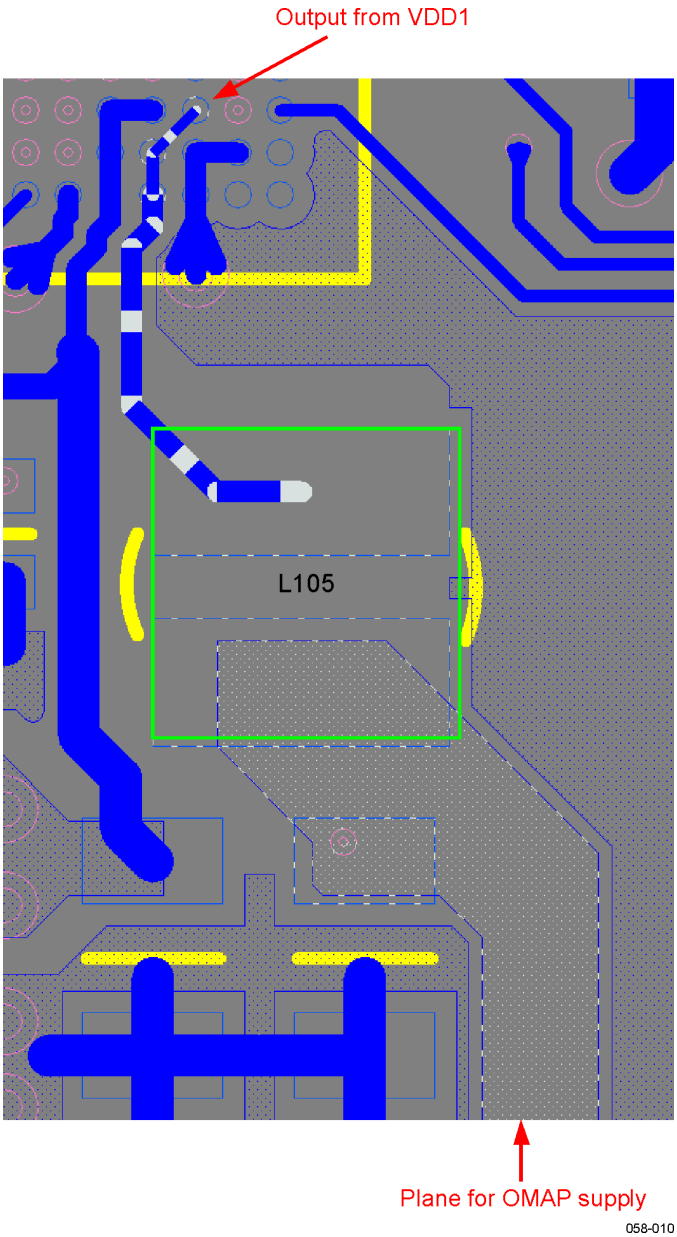

Figure A-2. Example 2

Solution

Improve the connection from the output balls and make parallel tracks in layers 2 and 3 when possible.

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