Application Report
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POR Generation in TPS65903x, TPS65917-Q1, TPS65919-Q1, and TPS65916 Devices

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ABSTRACT

Three different methods are available to make sure the TPS659038-Q1, TPS659039-Q1, TPS659037, TPS65917-Q1, TPS65919-Q1, and TPS65916 devices generate a power-on reset (POR) at each power cycle. These methods are limiting the falling VCC slew rate, limiting the rising VCC slew rate, and discharging LDOVRTC when power is off. This application note describes the POR generation behavior and a detailed description of each of these three methods.

NOTE: This document only applies to silicon versions 1.3 or earlier for the TPS65903x devices. Newer versions of silicon do not have the VCC slew rate or LDOVRTC discharge requirements to generate a POR. This document applies to all silicon versions of the TPS65917-Q1, TPS65919-Q1, and TPS65916 devices.

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Trademarks

1 Introduction

The TPS659038-Q1, TPS659039-Q1, TPS659037, TPS65917-Q1, TPS65919-Q1, and TPS65916 devices generate a power-on reset (POR) when the VCC1 supply voltage is less than the POR threshold defined in the device data sheet. These devices use VCC1 sampling to generate a POR event, which means a fast-decreasing VCC1 voltage can have the VCC1 supply powered off without generating a POR event. If the VCC1 supply is powered off without a POR event, the device may not power up correctly at the next power-on condition, therefore generating a POR event at every power cycle is important. This application note describes different application conditions which will make sure a POR event is generated.

2 POR Generation Details

To generate a POR event, the device uses VCC1 sampling to detect if the VCC1 supply voltage is less than the POR threshold. The device measures the VCC1 value every 1 ms with 10% variation, so the time between samples is from 0.9 ms to 1.1 ms. If any one of these samples detects that the VCC1 supply voltage is less than the POR threshold, a POR event is generated and the device is reset.

If a POR event is not generated from the VCC1 samples, a POR event can still be generated by discharging the voltage on the LDOVRTC_OUT pin because the LDOVRTC regulator is the supply to the POR generation circuit. When the voltage on the LDOVRTC_OUT pin is fully discharged, a POR event is generated the next time the VCC1 voltage is supplied to the PMIC.

Three conditions make sure a POR event is generated in the device. These conditions are as follows:

- The VCC1 supply has a falling slew rate less than 90 mV/ms between 1.9 V and 1.8 V.
- The VCC1 supply has a rising slew rate less than 90 mV/ms between 1.8 V and 1.9 V.
- The LDOVRTC_OUT pin voltage is discharged to less than 100 mV, with an off time of at least 300 ms.

The following sections describe each of these conditions in more detail.

2.1 VCC1 Falling Slew Rate

The POR comparator can accurately detect a POR event with a minimum VCC1 voltage of 1.8 V. Because the minimum POR threshold value in the device data sheet is 1.9 V, this means there is a 100-mV voltage range in which the device can always detect a POR event. As long as one POR sample occurs within this voltage range, a POR event is generated. Because the maximum time between two samples is 1.1 ms, the maximum slew rate to generate a POR event is calculated in Equation 1. Therefore, if the falling slew rate is less than 90 mV/ms, a POR event is generated when the VCC1 pin is discharged below the POR threshold, as shown in Figure 1.

$$(1.9\ V - 1.8\ V) / 1.1\ ms = 90.9\ mV/ms \quad (1)$$

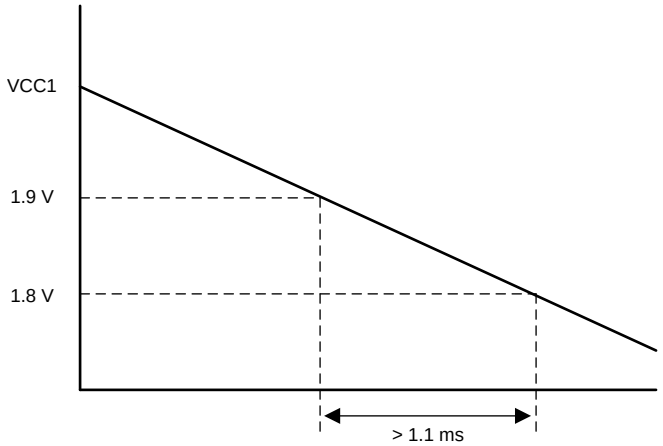

Figure 1. VCC Falling Profile

2.2 VCC1 Rising Slew Rate

If a POR event is not generated when the VCC1 voltage decreases below the POR threshold, then the POR circuit is not reset. In this case, the comparator used to detect a POR event on the falling edge of the VCC1 voltage is still active, even when the VCC1 voltage is rising at the next power-up event. When the VCC1 voltage is between 1.8 V and 1.9 V and the POR comparator samples the VCC1 voltage, the POR comparator detects that the VCC1 voltage is less than the POR threshold and generates a POR event. These samples will also be at most 1.1 ms apart, so a rising VCC1 slew rate less than 90 mV/ms will also generate a POR event as shown in Figure 2.

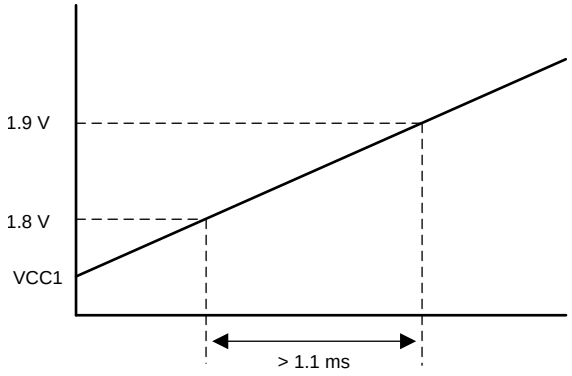

Figure 2. VCC Rising Profile

2.3 Discharging LDOVRTC_OUT

The LDOVRTC regulator is the power supply for the internal logic of the device, including the POR logic. Even if the POR comparator does not detect that the VCC1 voltage is less than the POR threshold, resetting the internal POR logic also generates a POR event. The POR event is generated by discharging the LDOVRTC voltage so that the device resets its internal active-low POR signal. The LDOVRTC_OUT pin requires a 2.2-uF capacitor to ground. In addition, a 3.9-kΩ resistor can be connected from the LDOVRTC_OUT pin to ground as described in the device data sheet. When no resistor is connected and the VCC1 voltage is discharged, the LDOVRTC regulator is turned off and the voltage on the LDOVRTC_OUT pin discharges very slowly with an off time, t_{off1}, greater than 1 s. In this case, the LDOVRTC_OUT pin should be discharged to less than 100 mV to generate POR event as shown in Figure 3.

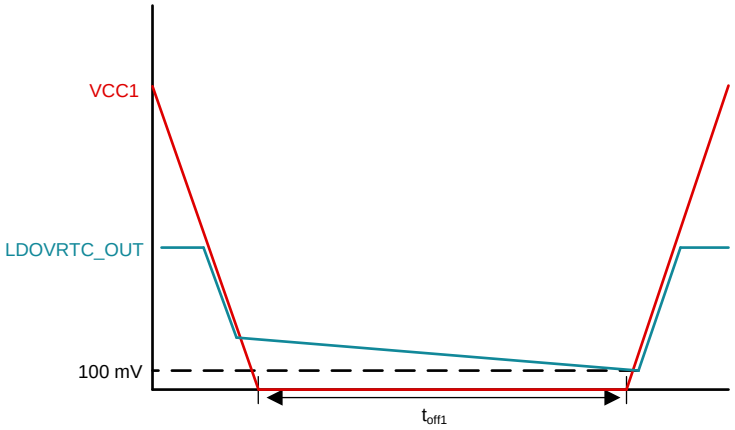

Figure 3. LDOVRTC Discharge With No Resistor

When a resistor is connected from the LDOVRTC_OUT pin to ground, then the LDOVRTC_OUT pin should be discharged to less than 100 mV for at least 300 ms to generate a POR event with an off time, t_{off2}, greater than 300 ms as shown in Figure 4. After the VCC1 voltage is discharged and the LDOVRTC_OUT pin voltage decreases to less than 500 mV, the internal transistors are all in the high-impedance state, and residual voltage on the internal logic nodes is possible. Having the t_{off2} time greater than 300 ms allows the internal nodes to discharge enough to generate a POR event.

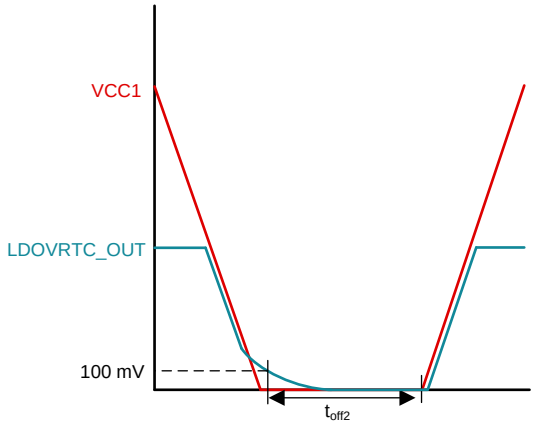

Figure 4. LDOVRTC Discharge With Resistor

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