Technical Article

Overview of a planar transformer used in a 1kW high-density LLC power module

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Growing data center power demands are driving server equipment manufacturers to reach higher power-conversion efficiencies in order to reduce the thermal footprint of their systems. The transition from a 12V power distribution bus to a 48V bus creates the need for a high-efficiency, small-footprint step-down converter (48V to 12V).

The inductor-inductor-capacitor (LLC) converter is the accepted topology of choice for bus converters because of its ability to maintain zero voltage switching over a wide load range at high switching frequencies. In this Power Tip, I'll present an overview of the transformer used in a high-density, 1MHz 1kW one-eighth-brick LLC converter with an efficiency over 98%.

LLC converter design

Any practical LLC converter design starts with the design of the resonant tank. In an effort to make the LLC converter as efficient as possible, the converter will run with open-loop control at a fixed frequency near resonance. Using the transformer leakage inductance as the resonant inductor will minimize the size of the overall converter. This design will operate at 1MHz to keep the size of the transformer and associated passive components as small as possible. Figure 1 shows the tank parameters chosen for this design. For details on how to select these parameters, see references [1] and [2].

Turns ratio	4-to-1
L_r	7 nH
L_m	2 µH
C_r	3.52 µF

Figure 1. LLC tank parameters for a design that will operate at 1MHz.

To maximize efficiency, it will be necessary to use multiple parallel field-effect transistors (FETs) for the synchronous rectifiers. The matrix transformer structure shown in Figure 2 will force sharing between multiple FETs. Functionally, each transformer has two turns on its primary and one turn for each center-tapped secondary. Putting the primary windings in series forces the same current to flow in each primary, and therefore forces the secondaries to share the current.

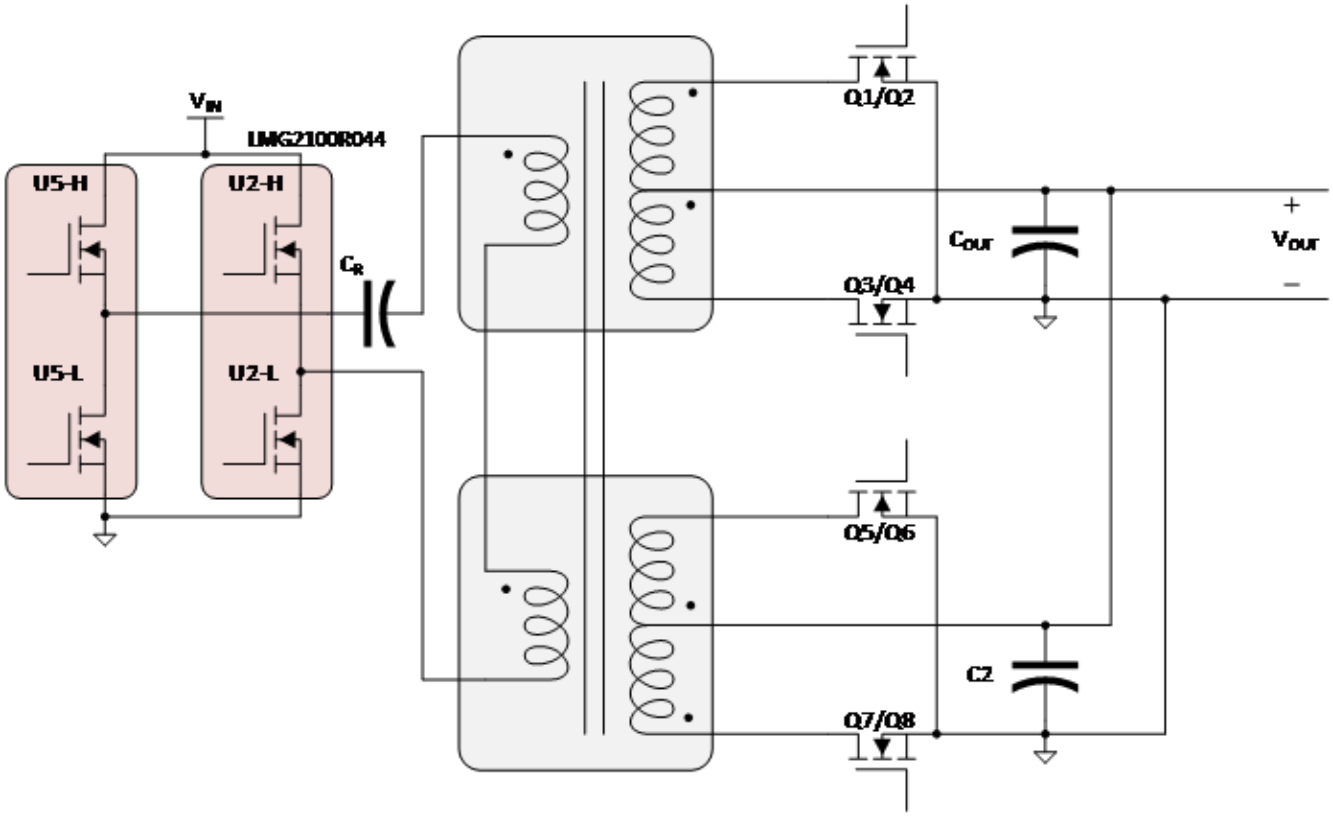

Figure 2. LLC converter with a matrix transformer that will force sharing between multiple FETs. Source: Texas Instruments

Figure 3 shows the flux paths in the two transformers shown in Figure 2. The first image shows the case for two discrete cores. Notice that the flux in the adjacent legs in the middle is equal but in opposite directions. As illustrated in the middle drawing of Figure 3, combining those legs into a single leg results in a net flux flow of 0. Since there is no flux in this leg of the core, you can eliminate the leg, as shown in the image on the far right.

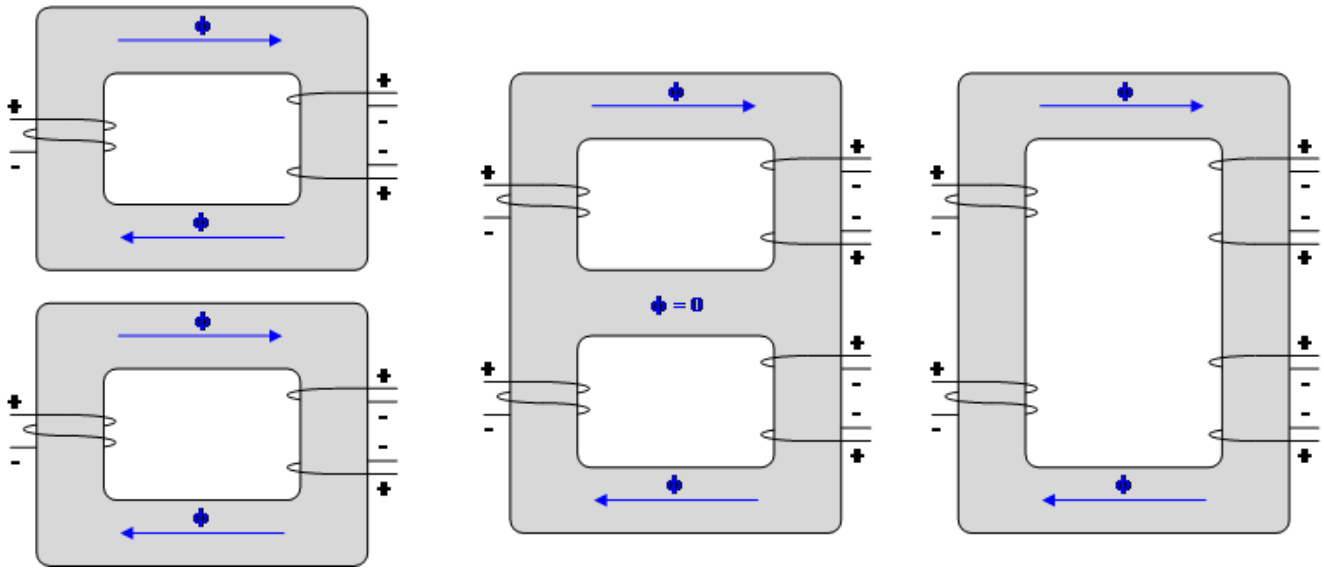

Figure 3. Flux paths of the matrix transformer integration shown in Figure 2 . Source: Texas Instruments

Thus, it is possible to integrate both matrix transformer elements shown in Figure 2 into a single transformer core. Figure 4 is a schematic representation of the LLC converter with the final integrated matrix transformer on a single ferrite core [3].

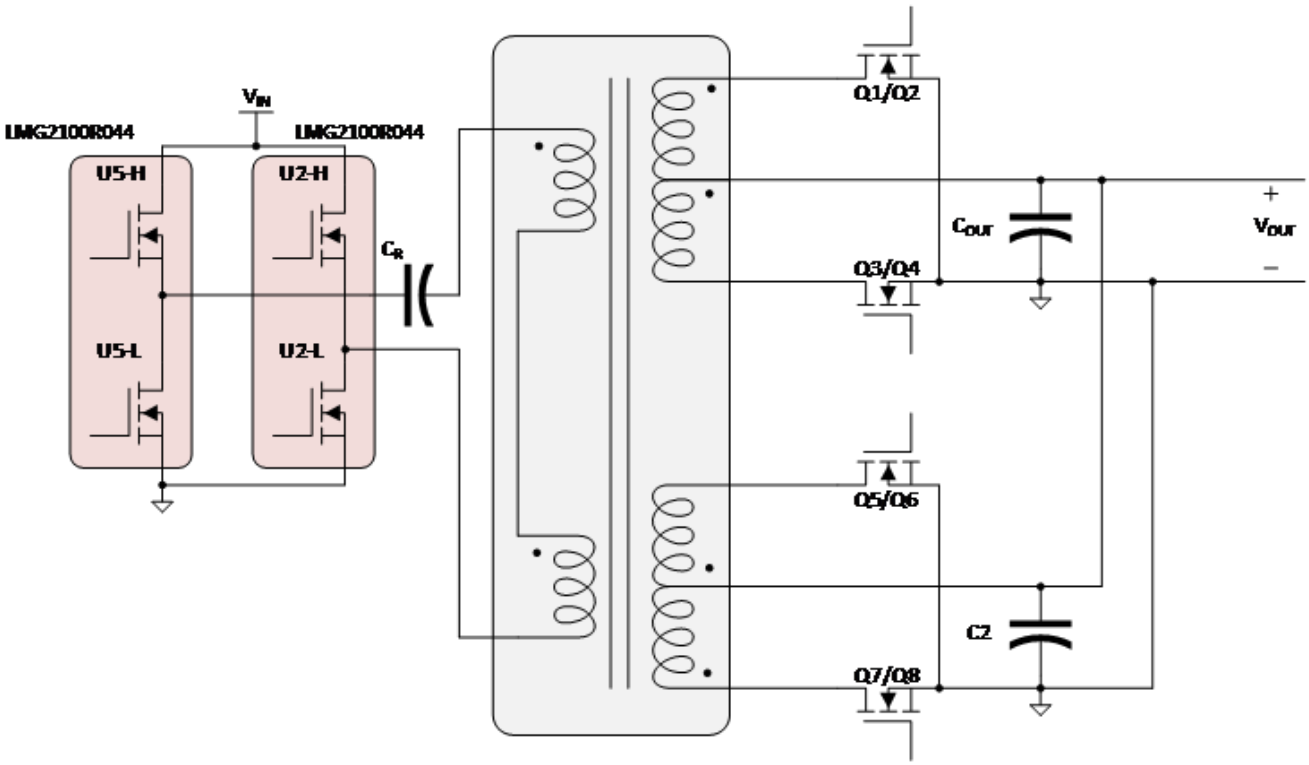

Figure 4. LLC converter with an integrated matrix transformer on a single ferrite core. Source: Texas Instruments

RMS current estimation

The majority of losses in the converter come from the root-mean-square (RMS) currents, thus requiring an accurate method to estimate the RMS currents in the transformer windings. The method presented in [4] does this by assuming that when the converter is operating at a switching frequency slightly below that of the resonant tank, the magnetizing current stays constant. With this assumption, it is possible to create a piecewise linear approximation of the LLC converter key waveforms, and from these piecewise linear definitions of the current, you can derive the closed-form expressions of the RMS current for the transformer primary current and transformer secondary current as shown in Equations 1 and 2:

$$I_{\mathrm{lr,rms}} = \frac{V_{\mathrm{out}}}{4nf_r^{3/2}L_M}\sqrt{\frac{f_s\left(4\pi^2 f_r^2 L_M^2 (2t_{\mathrm{dead}} f_r + 1)^2 + n^4 R_{\mathrm{load}}^2\right)}{2R_{\mathrm{load}}^2} + n^4 f_r - n^4 f_s} \quad (1)$$

$$I_{\mathrm{sec,rms}} = \frac{1}{4\sqrt{6}}\sqrt{\frac{f_s V_{\mathrm{out}}^2}{f_r^3 L_M^2}\left(\frac{3\left(4\pi^2 f_r^2 L_M^2 (2t_{\mathrm{dead}} f_r + 1)^2 + n^4 R_{\mathrm{load}}^2\right)}{R_{\mathrm{load}}^2} - \frac{48n^4}{\pi^2} + 2n^4\right)} \quad (2)$$

Transformer winding design

The winding interleaving strategy presented in [2] is designed to minimize high-frequency-related losses. Figure 5 illustrates the printed wiring board (PWB) stackup.

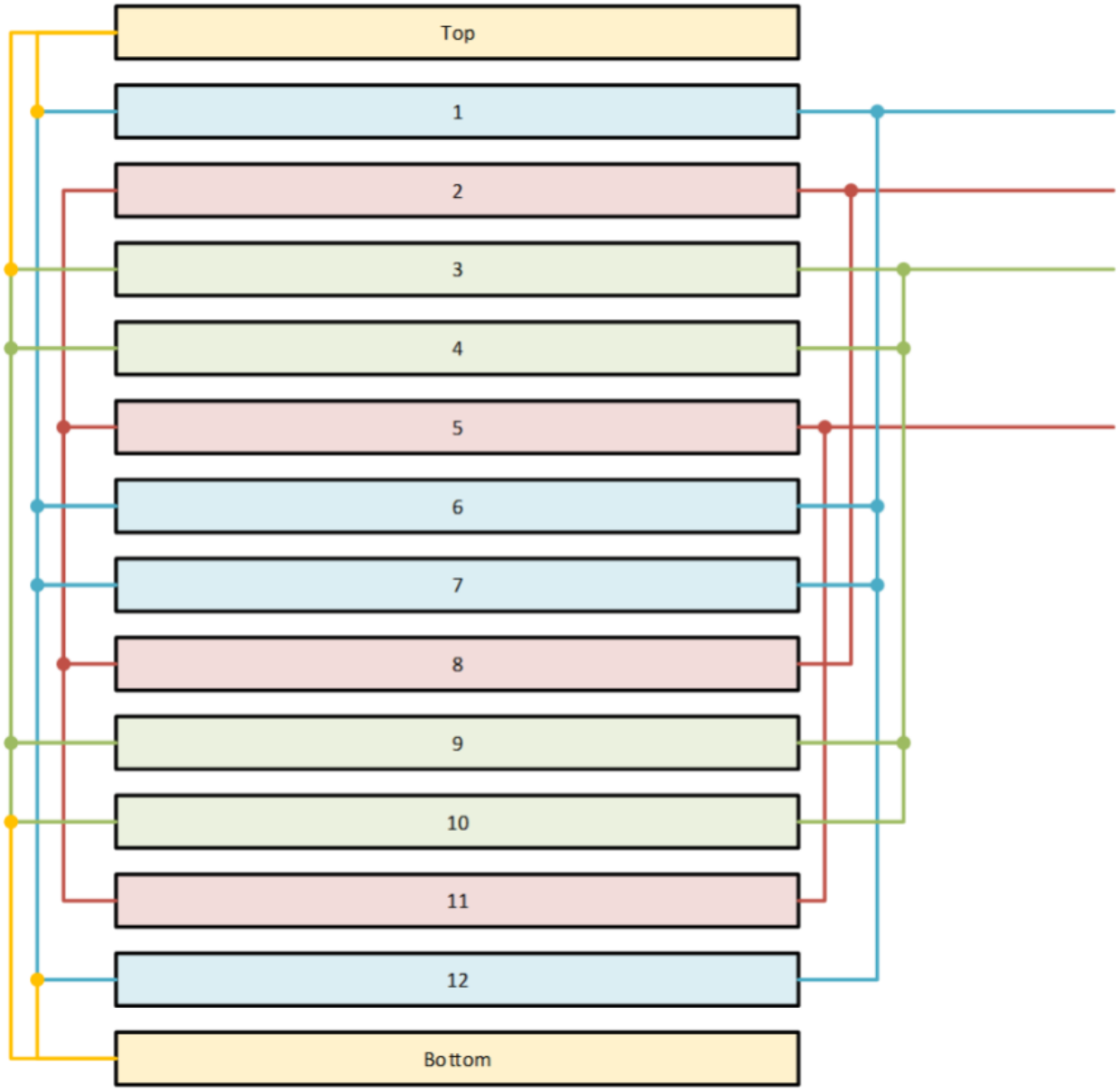

Figure 5. The transformer PWB stackup. Source: Texas Instruments

The red winding in Figure 5 comprises four PWB layers. Each layer has two turns. Layers two and five are in series, as are layers eight and 11. Furthermore, layers two and five are in parallel with layers eight and 11. Figure 6 shows the actual PWB layers. The copper shapes in red and orange are the transformer primary. Figure 6 also shows current flow direction with a yellow line during the positive half of the switching period.

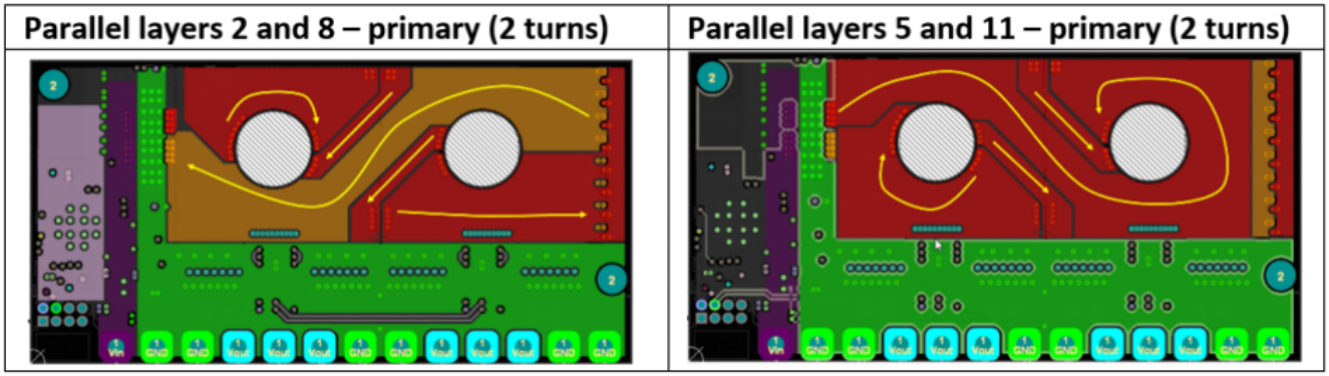

Figure 6. Actual PWB layers where the transformer primary copper layers are in red and orange. Source: Texas Instruments

The blue layers in Figure 5 are all in parallel and form one of the transformer secondaries. The green layers in Figure 5 are the same as the blue but for the other transformer secondary. Figure 7 shows the actual PWB layers. The copper shapes colored in cyan are the transformer secondaries. The positive half of the center tap is shown on the left and the negative half is shown on the right. Figure 7 also shows current flow direction with a yellow line during the positive half of the switching period.

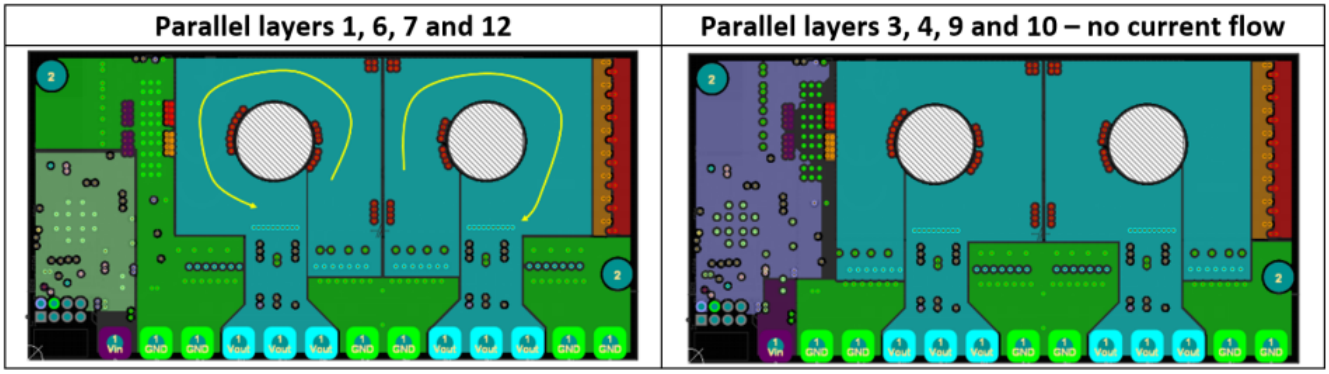

Figure 7. Actual PWB layers with the transformer secondary copper layers in cyan and where the positive half of the center tap (left) and negative half (right). Source: Texas Instruments

While this winding structure is effective at minimizing AC losses, it does not reduce winding losses to zero. In order to better approximate these losses, it is essential to first have a better estimate of the DC resistance of the winding. This is done by calculating the difference between an exact planar winding arc and a dc finite element analysis (FEA) model for the actual winding geometry. The resistance formula for an exact planar arc is shown in Equation 3:

$$R_{ca} = \frac{2 \times \pi}{\sigma \cdot h_{cu} \times \ln\left(\frac{r_2}{r_1}\right)} \quad (3)$$

where σ is the conductivity of copper, is the copper layer thickness, r_1 is the inner radius of the arc, and r_2 is the outer radius of the arc.

Figure 8 is a comparison between the DC FEA model for a circular arc and the exact winding geometry. Using only one-fourth of the model reduces the computational complexity. R_+ and R_- are two independent calculations of the winding resistances from the FEA model results; R_{ca} is the output of Equation 3. The left plot calibrates the FEA model against Equation 3. The right plot determines the error between Equation 3 and the actual geometry. Using this error as a scale factor enables an adjustment of the model to correlate more closely to the real geometry.

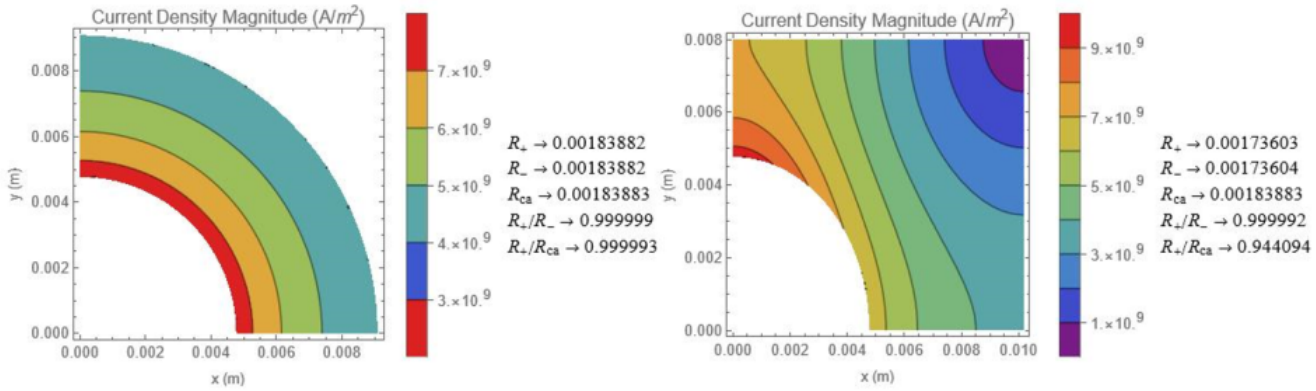

Figure 8. Finite element winding DC resistance estimate where the left plot calibrates the FEA model against Equation 3 and right plot determines the error between Equation 3 and actual geometry. Source: Texas Instruments

Equation 4 is the final winding loss equation with the calibration and AC loss influences from [5]:

$$R_{ac} = \frac{R_{+}}{R_{ca}} \frac{2 \times \pi}{\sigma \times h_{cu} \times \ln\left(\frac{r2}{r1}\right)} \times \mathrm{Re}\left(\sqrt{j \times 2 \times \pi \times f_s \times \mu_0 \times \sigma} \times h_{cu} \times \coth\left(\sqrt{j \times 2 \times \pi \times f_s \times \mu_0 \times \sigma} \times h_{cu}\right)\right) \quad (4)$$

where f_s is the switching frequency and μ_0 is 4 x π x 10^{-7}.

You can use Ansys FEA software to check the transformer winding losses under transient excitation from the simulated LLC converter waveforms. Equation 4 matched the Ansys transient FEA model to within 1%.

Test results

Figure 9 is an image of the hardware.

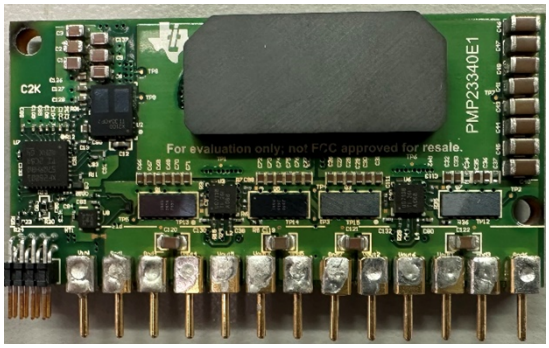

Figure 9. The One-eighth-brick LLC converter prototype hardware. Source: Texas Instruments

Figure 10 illustrates the measured losses and efficiency from the hardware. This data was collected with a 48V input constant-current load and forced air. Figure 10 also shows the module efficiency and compares the predicted and measured losses.

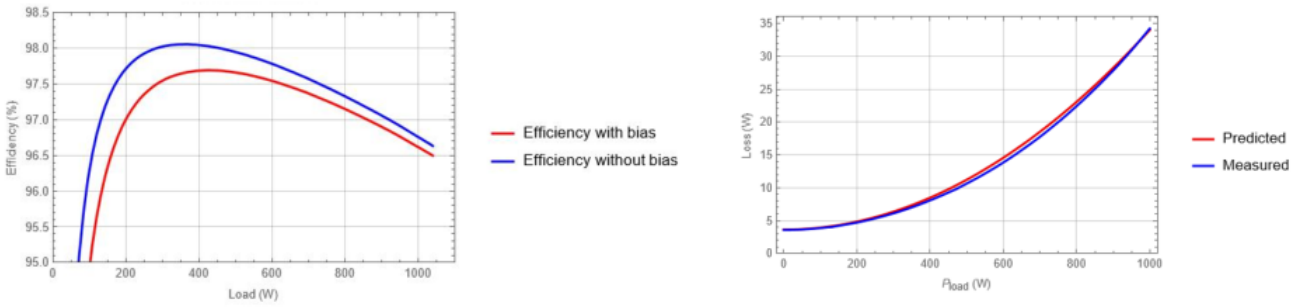

Figure 10. Measured efficiency, loss and regulation for the prototype hardware. Source: Texas Instruments

Transformer for LLC converter overview

This Power Tip presented an analytically sound transformer structure and winding loss estimation method for a high-efficiency LLC converter. This methodology in concert with high performance GaN switches like the LMG2100 [6] enable datacenter power supply designers to design smaller and higher efficiency bus converters.

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References

1. Huang, Hong. “Designing an LLC Resonant Half-Bridge Power Converter.” Texas Instruments Power Supply Design Seminar SEM1900, literature No. SLUP263, 2010-2011.
2. Bing Lu, Wenduo Liu, Yan Liang, F.C. Lee, and J.D. van Wyk. “Optimal Design Methodology for LLC Resonant Converter.” Published in 21st Annual IEEE Applied Power Electronics Conference and Exposition (APEC), March 19-23, 2006, 6 pp. doi: 10.1109/APEC.2006.1620590.
3. Ahmed, Mohamed. 2019. “Power Architectures and Design for Next Generation Microprocessors.” Ph.D. dissertation, Virginia Polytechnic Institute and State University.
4. Liu, Ya. 2007. “High Efficiency Optimization of LLC Resonant Converter for Wide Load Range.” Master’s thesis, Virginia Polytechnic Institute and State University.
5. Dowell, P.L. “Effects of Eddy Currents in Transformer Windings.” Published in Proceedings IEE (UK) 113, no. 8 (August 1966): pp. 1387-1394.

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