Technical Article
Simplifying Loop Compensation and Poles and Zeros Calculations

![Texas Instruments logo]

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Do you ever find yourself frustrated while designing the power supply for your end application? Designing for power-supply loop compensation and calculating the poles and zeros can be difficult, especially for inexperienced power-supply designers. Loop-compensation design can also be very time-consuming, thus adding more pressure if you only have a short amount of time to complete your designs.

Despite complicated calculations and deadline stresses, you still have to maintain high power density and efficiency. Yet programming soft-start times and undervoltage lockout (UVLO) and setting current limits can be another painful task. Luckily, there are several point-of-load (POL) DC/DC solutions to make your power-supply design process easier and faster.

TI's direct connect to the output capacitor (D-CAP™) is an adaptive on-time control technology that requires no phase compensation. Compared to voltage and current mode, D-CAP solutions deliver faster load-transient responses, resulting in fewer output capacitors, lower bill-of-materials (BOM) costs and higher power density. Many of our D-CAP solutions include a power management bus, or PMBus. Through TI's PMBus power solutions, you can easily program and adjust soft start, UVLO, current limit and other parameter values with a few simple clicks using TI's Fusion Digital Power Designer graphical user interface (GUI). Programming and customizing a PMBus power supply does not require software knowledge; you'll program via straightforward PMBus commands and their values, which occupy a dedicated set of registers on the I^2C bus. Along with D-CAP control mode, PMBus enables ease of use, reduced design time and component count.

The TI Designs Complete PMBus Power System for Enterprise Ethernet Switches Reference Design is a PMBus power system for application-specific integrated circuit (ASIC)/field-programmable gate array (FPGA) cores; DDR4 core memory; and auxiliary voltages found in high-performance power supplies such as Ethernet switches, storage, servers, and test and measurement applications. TI will be demonstrating this buck power supply at the 2016 Applied Power Electronics Conference (APEC).

The reference design features:

- As shown in the block diagram in Figure 1, there are eight voltage regulators, including a D-CAP+™ regulator, PMBus high-current multiphase power supply and DDR4 termination.
- PMBus sequencing, control, monitoring/margining and telemetry of analog POL power supplies, along with black-box fault logging.
- Adaptive voltage scaling (AVS) via the PMBus and AVS bus to reduce power usage.
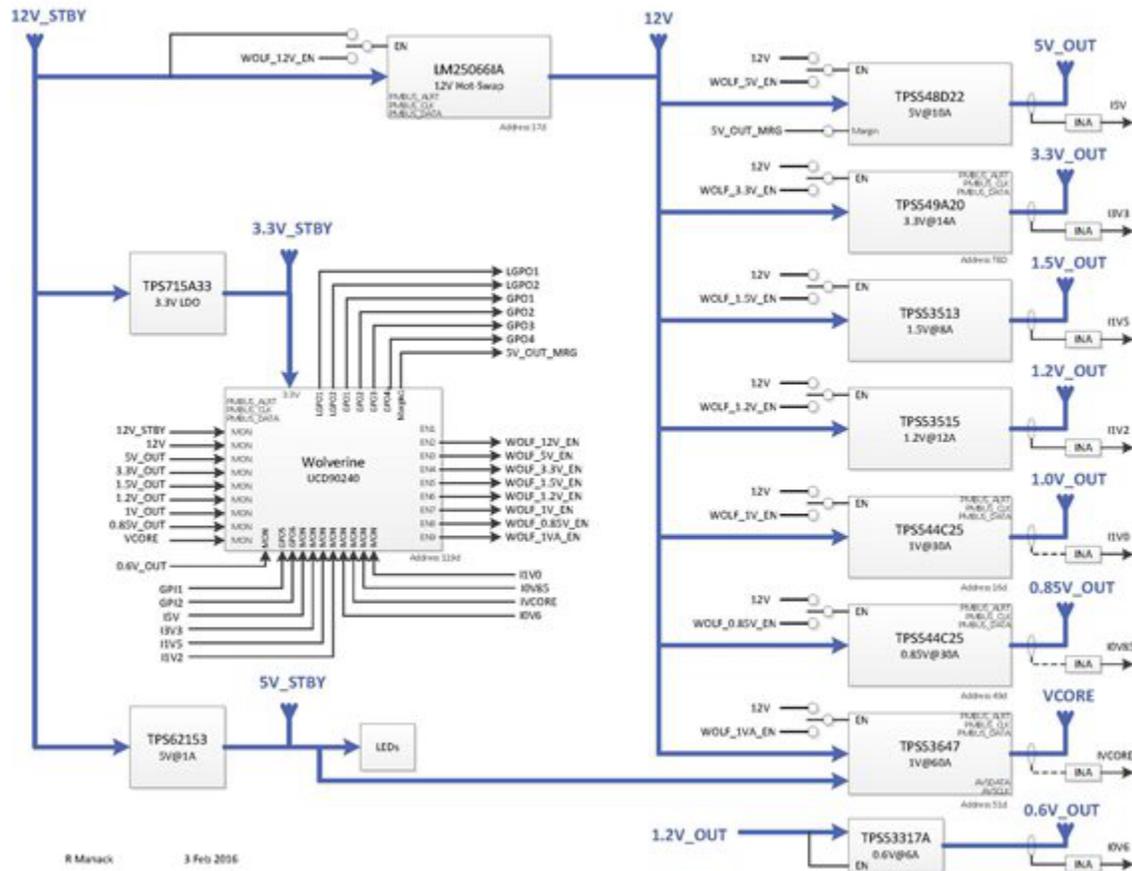
Figure 1. Complete PMBus Power System for Enterprise Ethernet Switches Reference Design Block Diagram

The reference design includes:

- TI's first DDR4/LPDDR4 termination voltage (VTT) switching regulator. The TPS53317A is a 6A, DCAP+ mode, SWIFT™ synchronous step-down converter with external rail tracking for AVS. It is suitable in split-rail operations where the input voltage (V_{IN}) powers the internal FETs, while the lower-voltage VDDQ (memory core rail) acts as REFIN to generate the VTT rail. In addition, the DCAP+ control mode enables fast load-transient response with no need for complex switch-loop compensation.
- The UCD90240 is a 24-channel PMBus power sequencer cascadable to 96 channels. The UCD90240 acts as the system manager in this reference design. It can log 100 faults and its black-box fault-logging capability takes a complete system snapshot upon the first fault detection.
- The TPS53467 is a general-purpose four-phase driverless pulse-width modulation (PWM) buck controller for ASICs and digital signal processors (DSPs). This DCAP+ mode controller offers extensive pin-strapping and PMBus programming functions. Through PMBus, the TPS53647 can monitor input/output voltage, current, temperature and power.
- The TPS549A20 is TI's newest PMBus 15A, D-CAP3™ control mode SWIFT buck converter. In a 3.5mm-by-4.5mm PowerStack™ package, this is one of the world's smallest 15A synchronous buck converters. The TPS549A20 can power an ASIC/FPGA rail up to 15A output current with high efficiency and power density while adding PMBus programming and fault status for ease of use and system diagnostics.

The reference design offers multiple benefits:

- Cut-and-paste design for high performance, high power applications.
- Complete system management, easy failure analysis and reduced time to market.
- Quick diagnostics and enhanced reliability.

Don't sweat over how to design your buck power supply. With TI's D-CAP technology and PMBus solutions, you will have your buck power supply up and running in no time.

See a live demonstration of the PMBus power system in TI's booth (No. 1617) at the Applied Power Electronics Conference (APEC), March 21-23 in Long Beach, California. Follow TI at www.ti.com/apec2016. Attend the "Next Gen PMBus Point-of-Load Solution" presentation, presented by TI in the Wurth booth (No. 1933) on Monday, March 21 at 7p.m. and Wednesday, March 23 at 1p.m.

Additional Resources

- Start designing and optimizing your complete POL DC/DC solution with WEBENCH® Power Architect.
- Access the schematic, test data and design files of the reference design tool folder.
- To learn more about D-CAP technology, read the blog post, "D-CAP3 – A sequel better than the original."
- For more information about PMBus, watch Section 2 of the TI training series, "Powering FPGA, ASIC and DDR Rails": "ASIC, FPGA and DDR rail power design through PMBus power supplies."

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