Technical Article

How to Correctly Layout a 40A Power Supply: Copper, Vias and Loop Path

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The demand for energy has gone up significantly but overall solution size continues to shrink. To adapt, you can decrease the size of a buck converter but it must still be able to handle the increasing power consumption in the electronic system. Optimizing the layout to increase the efficiency of the buck converter will result in less electricity needed to power the system.

Many electronic systems require several buck converters to supply power to different rails. Some systems may need two converters or more to power a single rail with a high current demand. The challenge of designing a smaller buck converter to satisfy this demand becomes a daunting task, but it is possible.

New technologies and processes are now in place that enable integrated circuit (IC) designers to design buck converters that can handle up to 40A for a single output. However, this capability introduces other issues. One is the printed circuit board (PCB) layout. You can design the best buck converter and power stage with space constraints in mind, but if you fail to lay out the PCB correctly, all will be lost.

With the current at 40A per output, PCB layout is crucial in regards to heat dissipation and efficiency. If you don't optimize the board design, the DC loss at 40A can increase greatly due to the higher resistance of the copper-poured area. So in this post, I'll explain the importance of the copper-poured area, via size and quantity, and current loop path on a multi-layer circuit board.

Copper Poured Area

If you know the cross-sectional area of the copper (thickness × width), length and resistivity, you can calculate the resistance of the copper trace, copper plane or copper pour. With this data, you can size the copper to optimize the PCB's thermal, efficiency and signal-integrity performance. A multi-layer board with multiple buried cooper planes connected with vias to the top layer or bottom layer can also help disperse the heat away from the IC. Figure 1 shows the difference in efficiency between switch-node areas. The modified switch-node area is larger than the original, which decreases the DC loss.

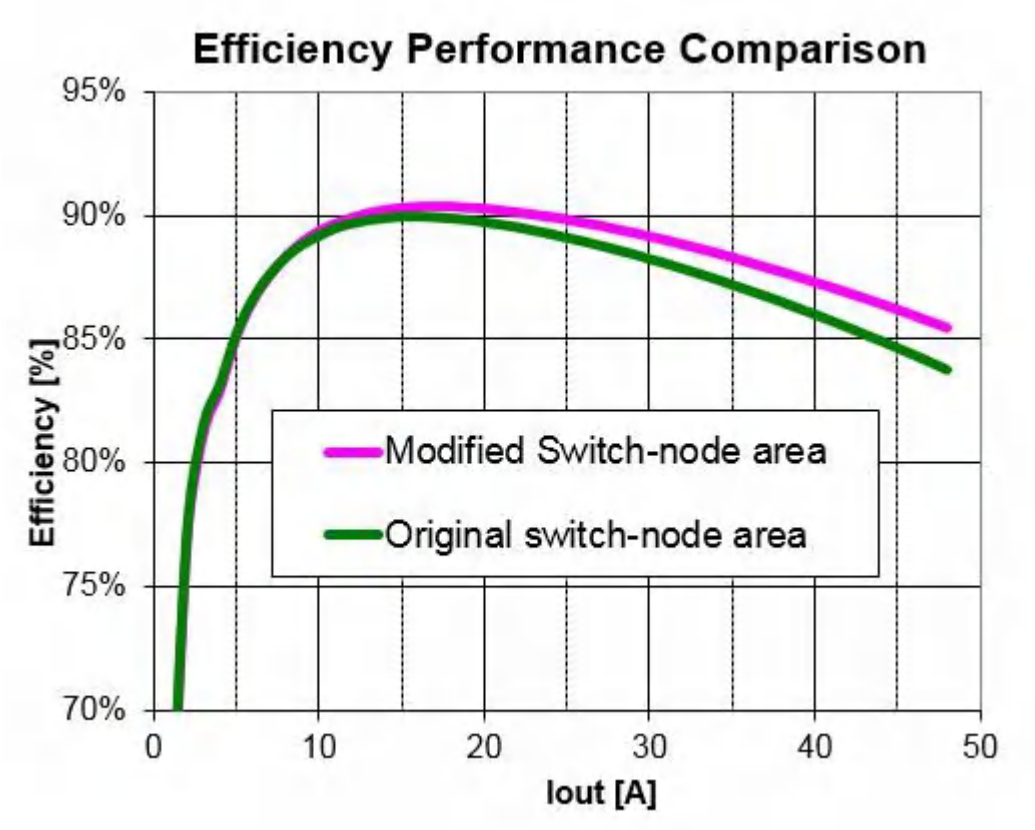

Figure 1. Modified Switch Node Area Showing a Size Increase vs. Original Switch Node Area

Via Size and Quantity

Vias make up series-resistance elements when they connect two traces or plane together. Generally, multiple vias in parallel will reduce the effective resistance. Just like the flat copper area and thickness, vias have a finite resistance. So you must optimize the vias' quantity and size to optimize the thermal performance and efficiency of a converter design.

Figure 2 and Figure 3 represent two PCBs with identical set-ups and layouts. The only difference is the amount of vias on the thermal pad of the IC.

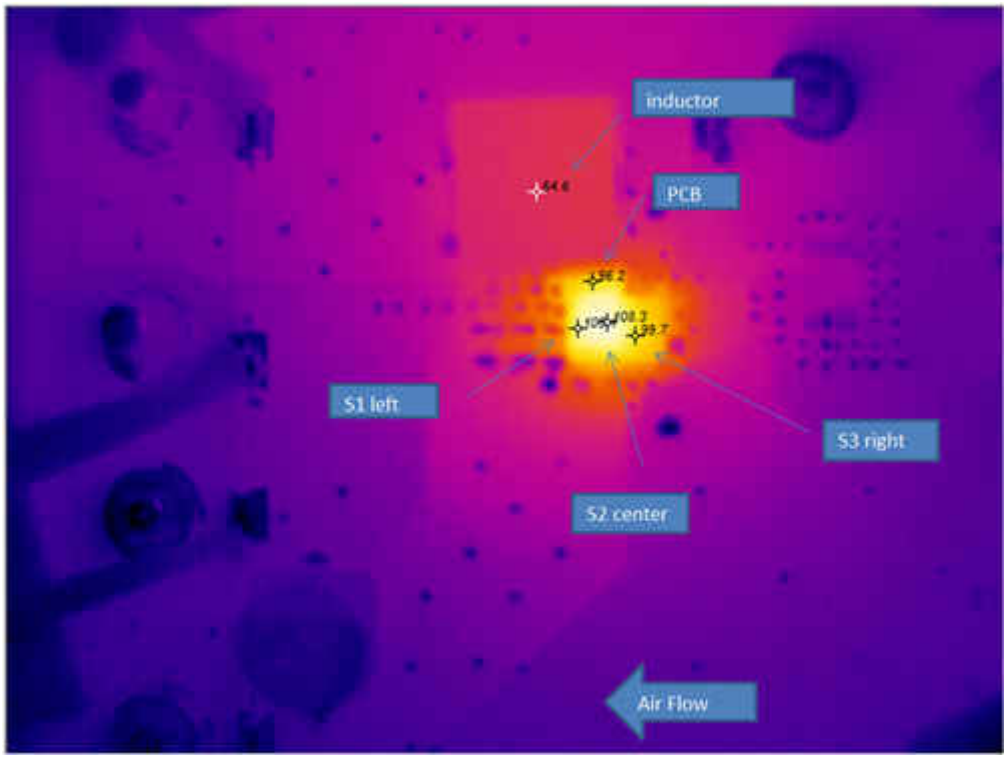

Figure 2. PCB with 11 Vias under the Thermal Pad

***S2 (Site 2): Location of the Integrate FET on the IC**

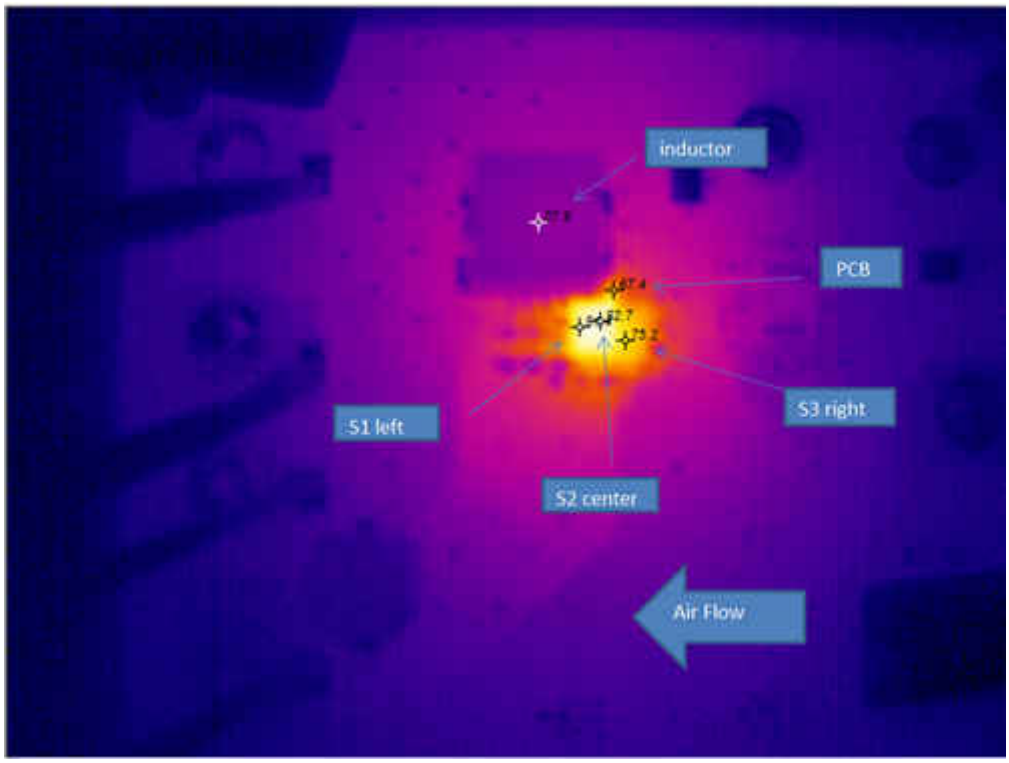

Figure 3. PCB with 35 Vias under the Thermal Pad

Current Loop Path

You also need to optimize the path of the current loop between each alternate state of operation of the high-side field-effect transistor (FET) and the low-side FET in the buck converter. Your optimization should include the distance and current-carrying capability of the loop. Properly planned designs of the IC pin-outs also become a factor in the PCB layout process. You should minimize the current-loop area as much as possible.

As semiconductor technologies and processes continue to evolve, we are packing more silicon into the same package to enable higher current rated converter designs. Consider for example, the new 40A SWIFT™ TPS543C20 synchronous step-down converter with adaptive internal compensation and integrated NexFET™ MOSFETs. However, the fundamental question remains of how to optimize the design so that we don't compromise thermal performance and efficiency. Hopefully this blog helps you correctly create a smaller-sized, true 40A power supply design.

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