

Managing Thermals: 3 Ways to Break through Power-density Barriers

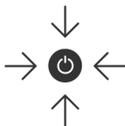


Robert Taylor

The number of semiconductors in nearly every application is multiplying, and many of the design challenges facing electronics engineers all tie back to the need for greater power density. A few example applications come to mind:

- **Hyperscale data centers:** Rack servers are using an incredible amount of power, challenging utility companies and power engineers to keep up with increasing demands.
- **Electric vehicles:** The transition from internal combustion engines to 800-V battery packs comes with an exponential increase in semiconductor content for the powertrain.
- **Commercial and home security applications:** As video doorbells and Internet Protocol cameras become more prevalent, their shrinking sizes put constraints on the necessary thermal solution.

Understanding the Trade-offs and Technologies to Increase Power Density



Thermal efficiency is paramount to improving power density. Read the [white paper](#) to learn how to overcome common barriers.

What stands in the way of achieving higher power density? Well, thermal performance is an electrical byproduct of power-management integrated circuits (ICs), which you can't ignore or "optimize out" with filtering components at the system level. The mitigation of thermals requires critical microadjustments throughout every step in the development process so that the design can achieve its system requirements for a given size constraint. Following are three key areas TI focuses on to optimize thermal performance and break through power-density barriers at the chip level.

Process Technology Innovations

Many global semiconductor manufacturers are racing to offer power-management products that leverage process technology nodes to achieve higher performance capabilities in industry-standard packages. For example, at TI we continue investing in 45- and 65-nm process technologies that leverage our internal technology development, along with 300-mm manufacturing efficiencies to offer products optimized for cost, performance, power, precision and voltage levels. Our process technology advancements also help us create products that maintain high performance under various thermal conditions. For instance, reducing the specific on-state resistance (R_{SP}) or drain-to-source on-state resistance ($R_{DS(on)}$) of integrated metal-oxide semiconductor field-effect transistors (MOSFETs) minimizes die size while enhancing thermal performance. The same is true for other semiconductor switches such as gallium nitride (GaN) or silicon carbide.

Take the [TPS566242](#) buck converter, shown in [Figure 1](#). New process nodes optimize the pin layout by integrating features and providing an extra ground connection that helps deliver 6 A of output current from a 1.6-mm-by-1.6-mm small outline transistor (SOT)-563 package. If you asked me five years ago if tiny, simple leaded packages would be capable of that type of performance, I'd have been skeptical. But that's the beauty of process technology!

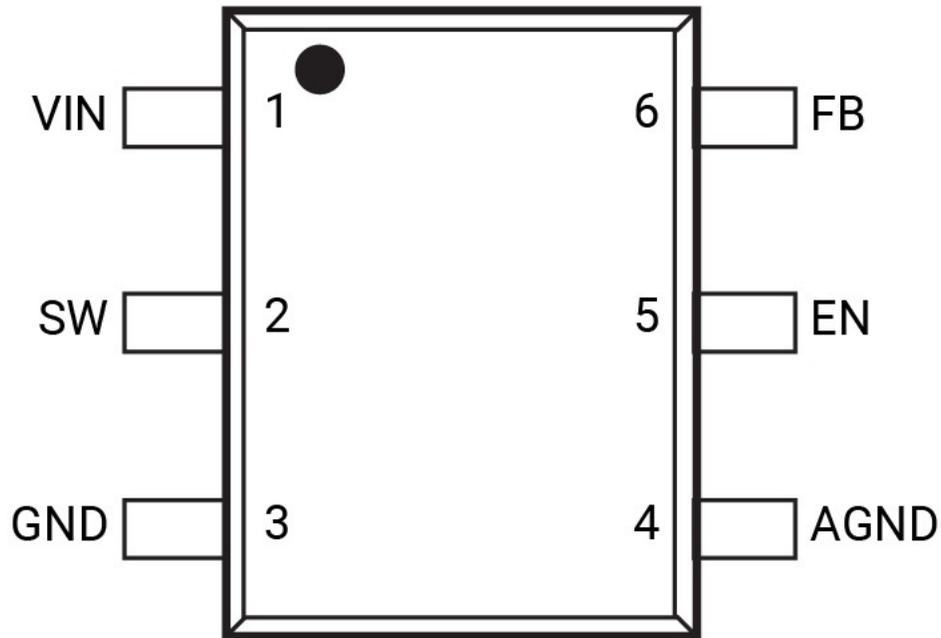


Figure 1. The TPS566242 Synchronous Buck Converter Delivers up to 6 a of Continuous Current

Circuit-design Techniques

In addition to more efficiency at the process technology level, creative circuit design also plays an important role in improving power density. Designers have historically used discrete hot-swap controllers to protect high-current enterprise applications. As a protection function, they are reliable, but with end-equipment manufacturers (and consumers) requiring more current capability, discrete power designs can grow far too large, especially for applications such as server power-supply units (PSUs) that often require 300 A of current or more.

The [TPS25985](#) eFuse pairs an integrated 0.59-mΩ FET with a current-sense amplifier. This amplifier, plus a new active current sharing approach, provides an easy way to allow for temperature monitoring. By pairing efficient switches with creative integration approaches, the TPS25985 can deliver up to 80 A of peak current, and you can easily stack multiple eFuses for higher power.

Thermally Optimized Packaging R&D

Although reducing the amount of heat dissipated into the printed circuit board (PCB) or system is a basic requirement, the reality is that undesirable heat still lingers, especially as the power requirements or your system's ambient temperature increase. TI has recently enhanced the performance of its HotRod™ quad-flat-no lead (QFN) packages, including larger die-attach pads (DAPs) to facilitate greater heat dissipation. [Figure 2](#) shows the total DAP area and pin accessibility of the 6-A, 36-V [TLVM13660](#) step-down power module.

Conclusion

Maintaining performance while reducing the impact of thermals can only happen with a multifaceted approach to process and packaging technology and power design expertise. At TI, it's a challenge that our product designers, systems engineers, packaging R&D and manufacturing teams are all hyperfocused on – to achieve greater power density without thermal pitfalls.

Additional Resources

- Find devices and technical resources to solve your density challenges at ti.com/powerdensity.
- Watch our training series, "[Understanding the Fundamental Technologies of Power Density](#)."
- Create a custom power-supply circuit with [WEBENCH® Power Designer](#).

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