TMS320C6205

Digital Signal Processor

Silicon Errata

Silicon Revisions 1.0, 1.1, 1.2, 1.3, 1.4

SPRZ181J
September 2000
Revised February 2006

REVISION HISTORY

This revision history highlights the technical changes made to SPRZ181I to generate SPRZ181J.

Scope: Clarified device numbers for Silicon Revisions.

PAGE(S) NO.	ADDITIONS/CHANGES/DELETIONS
5	Table 1: Lot Trace Code Names: Updated by clarifying device numbers for Silicon Revisions 1.4 and 1.3

Contents

1 Introduction

This document describes the silicon updates to the functional specifications for the TMS320C6205, silicon release 1.4 or earlier. [See the *TMS320C6205 Fixed-Point Digital Signal Processor* data sheet (literature number SPRS106).]

For additional information, see the latest version of *TMS320C6000 DSP Peripherals Overview Reference Guide* (literature number SPRU190).

1.1 Quality and Reliability Conditions

TMX Definition

Texas Instruments (TI) does not warranty either (1) electrical performance to specification, or (2) product reliability for products classified as “TMX.” By definition, the product has not completed data sheet verification or reliability performance qualification according to TI Quality Systems Specifications.

The mere fact that a “TMX” device was tested over a particular temperature and voltage ranges should not, in any way, be construed as a warranty of performance.

TMP Definition

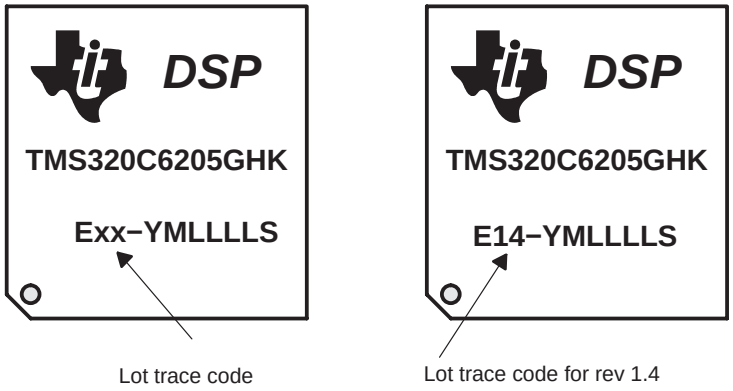
TI does not warranty product reliability for products classified as “TMP.” By definition, the product has not completed reliability performance qualification according to TI Quality Systems Specifications; however, products are tested to a published electrical and mechanical specification.

TMS Definition

Fully-qualified production device

1.2 Revision Identification

The device revision can be determined by the lot trace code marked on the top of the package. The location for the lot trace codes for the GHK package are shown in Figure 1 and Table 1.



NOTE: Qualified devices are marked with the letters “TMS” at the beginning of the device name, while nonqualified devices are marked with the letters “TMX” at the beginning of the device name.

Figure 1. Example, Lot Trace Code for TMS320C6205

Table 1. Lot Trace Code Names

Lot Trace Code	Silicon Revision	Comments
14	1.4	Revision 1.4 (C6205D) supports 5-V signaling PCI environment.
13	1.3	Revision 1.3 (C6205) has fixed the problem described in Advisory 1.2.3 of this errata.
12	1.2	This revision is functionally the same as 1.1.
11	1.1	
10	1.0	

2 Silicon Revision 1.4 Known Design Exceptions to Functional Specifications and Usage Notes

2.1 Usage Notes for Silicon Revision 1.4

Usage Notes highlight and describe particular situations where the device's behavior may not match presumed or documented behavior. This may include behaviors that affect device performance or functional correctness. These notes will be incorporated into future documentation updates for the device (such as the device-specific data sheet), and the behaviors they describe will not be altered in future silicon revisions.

PCI: PCI Burst Lengths Limited to a Maximum of 8 Words

On silicon revision 1.4 and earlier, due to the buffering between the PCI port and the internal DMA hardware servicing the port, the PCI port is only able to support bursts of 5 to 8 words. If observed PCI burst lengths are at the lower end of this range, a DMA transfer that conflicts with the PCI port will improve PCI burst lengths up to the maximum of 8 words. This conflicting DMA transfer can be periodic (i.e., timer-based) or set to trigger on PCI activity (through externally fed-back signals). The DMA transfer should be a frame-synched transfer from internal DMEM to internal DMEM. The timing and duration of the transfer should be tailored to suit system needs and performance goals.

2.2 Silicon Revision 1.4 Known Design Exceptions to Functional Specifications

Advisory 1.4.1	*PCI Cache Line Size Must Be > 4*

Revision(s) Affected: 1.4 and earlier

Details: If the cache line size (set in cache line size PCI configuration register) is set to less than 4 and a memory read line is addressed to the PCI Module of the TMS320C6205 from an external master, the PCI Module of the DSP will continually disconnect the transfer.

Workaround: Cache line size should be greater than 4.

Advisory 1.4.2	*Memory Read Line PCI Command Can Lock up DMA*

Revision(s) Affected: 1.4 and earlier

Details: The Memory Read Line PCI command can potentially lock up the DMA if the PCI master attempts to read less than one cache line of data from the DSP (cache line size is specified in PCI configuration space).

Workaround: Use the Memory Read command or Memory Read Multiple command instead of the Memory Read Line command when reading less than one line of cache. Do not use the Memory Read Line PCI command unless the whole cache line is read from the DSP.

Advisory 1.4.3	*PCI: Slave Writes With Null Data Phases Can Lock up PCI*

Revision(s) Affected: 1.4 and earlier

Details: When performing slave writes to the DSP, the PCI port is susceptable to lockup if a word is written without any byte enables asserted. The PCI port will always disconnect a transfer when it detects a null data phase. If this null data phase coincides with a particular internal FIFO state, then the PCI port will also disconnect all future accesses.

Workaround: When transferring data using slave writes to the DSP, ensure at least one byte is enabled in every data phase.

Advisory 1.4.4	*PCI: Slave Writes Can Corrupt Data*

Revision(s) Affected: 1.4 and earlier

Details: When performing slave writes to the DSP through the PCI port, it is possible for the data to be corrupted. If the end of the PCI frame coincides with a particular internal FIFO state, then the last word of the burst will overwrite the first word of the burst. The location in memory where the last word should have gone is left unmodified. Only slave writes that burst longer than 4 words are affected.

Workaround: There are several things that can be done to work around this issue. Any one of the following proven workarounds will always prevent the corruption:

- Limit slave-write burst sizes to no more than 4 words
- Alter the system to use master reads instead of slave writes to bring data into the DSP
- Implement an end-to-end data verification scheme to verify and correct any data that was corrupted

If these are not possible or desired, there is an alternate workaround that mitigates the risk, but does not eliminate the possibility, of data corruption. Since the alignment of the end of the PCI frame and the problematic FIFO state will likely only happen for certain burst sizes for a given PCI-to-CPU clock ratio. If the data corruption problem is observed, then altering the CPU speed while keeping the PCI speed constant can alter the timing of the two events (end of PCI frame and FIFO state) such that the problem no longer occurs. DMA traffic can also alter the alignment of these signals; if the problem is not observed in a system, slightly different DMA traffic can cause the problem to appear. It is therefore crucial to ensure that PCI and DMA traffic are representative of actual system usage conditions when using this workaround.

Advisory 1.4.5	*PCI: Slave Reads Without Any Byte Enables Issue Target Abort*

Revision(s) Affected: 1.4 and earlier

Details: A slave read transaction that does not assert any byte enables during a data phase will cause the PCI port to respond with a target abort. If a simple master attempts to repeat this transaction until successful, the system will be deadlocked.

Workaround: When doing PCI Slave Reads to the DSP, ensure that at least one byte lane is enabled during every data phase.

Advisory 1.4.6	*PCI: Master Transaction Following an Abort Can Erroneously Set MASTEROK*

Revision(s) Affected: 1.4 and earlier

Details: If an abort of any kind is received (Master abort, Target abort, or writing “0” to the START bits) and is followed by a master transaction, then the master transaction can set the MASTEROK interrupt bit (PCIIS.6) before the transfer has actually completed.

Workaround: When processing a MASTEROK interrupt, check the START bits to ensure the transaction has actually completed.

Advisory 1.4.7 — *PCI: Abort During Master Read Can Lock Up PCI*

Revision(s) Affected: 1.4 and earlier

Details: If an abort of any kind is received (Master abort, Target abort, or writing “0” to the START bits) while performing a master read, then the PCI port can be put into a state where no further transactions are possible. This lockup may involve the master and/or slave interface on the DSP, but does not affect other devices on the bus. PCI transactions that are neither to nor from the DSP proceed normally.

Workaround: If this PCI lock-up occurs, reset and reconfigure the PCI port.

Advisory 1.4.8 — *PCI: PCI EEPROM Size of 2K Does Not Function Properly*

Revision(s) Affected: 1.4 and earlier

Details: 2K Serial EEPROMs require 27 clock cycles to complete an access. These clock cycles consist of the following bits:

Bit 1	Start Bit
Bits 2:3	Operation Bits
Bits 4:11	Address Bits, where the fourth bit is a dummy bit
Bits 12:27	16 Data Bits

Details: The 2K EEPROM size setting does not output the dummy bit (fourth bit), causing *only* 26 cycles to be placed on the Serial EEPROM bus.

Workaround: If a 2K Serial EEPROM is required, select the 4K EEPROM size during boot configuration. Accesses beyond the 2K boundary should not be made with this configuation. If an access is made above the 2K boundary, the lower 2K will be aliased.

3 Silicon Revision 1.3 Known Design Exceptions to Functional Specifications and Usage Notes

3.1 Usage Notes for Silicon Revision 1.3

3.2 Silicon Revision 1.3 Known Design Exceptions to Functional Specifications

Advisory 1.3.8	*PCI: 5-V Signaling on PCI Bus Can Corrupt DSP PCI Transactions*

Revision(s) Affected: 1.3 and earlier

Details: If 5-V signaling is used on the PCI bus, the DSP I/O buffers may be left in a state where they are unable to drive the PCI bus to the correct logical state. Any time a signal (address, data, or control) is driven to a voltage level above 3.3 V, the DSP's I/O buffers may not be able to turn "on" for a relatively long period of time (hundreds of nanoseconds). If the DSP is expected to drive a signal during this time and is unable to, the bit may become corrupted. This can cause data corruption, address corruption, parity errors, and/or protocol violations.

Workaround: Do *not* use the DSP in 5-V signaling PCI environments. Voltage-translating bus transceivers may be used to convert 5-V signals to safe 3.3-V signals.

Revision 1.4 (part number TMS320C6205DGHK200) supports 5-V signaling PCI environment.

4 Silicon Revision 1.2 Known Design Exceptions to Functional Specifications

Advisory 1.2.3 *Internal Data RAM: Corruption After STB*

Revision(s) Affected: 1.2, 1.1, and 1.0

Details: When an STB accesses byte 0 from any memory bank (address 8000 xxxy, where y = 0,4,8,C, etc.), data can get corrupted. This occurs when on the very next cycle any load or store access to the memory bank is made as shown in Table 2. The next cycle access must be one that accesses byte 1 within the same bank of RAM.

Table 2. Fail Instruction Sequence Examples

Example Number	Possible Sequence†	
	First	Second
1	STB Reg, dst1[0]	LDB dst2[1], Reg
2	STB Reg, dst1[0]	LDH dst2[0], Reg
3	STB Reg, dst1[0]	LDW dst2[0], Reg
4	STB Reg, dst1[0]	STB Reg, dst2[1]
5	STB Reg, dst1[0]	STH Reg, dst2[0]
6	STB Reg, dst1[0]	STW Reg, dst2[0]

Reg = any general-purpose register
dst = Any data memory address (80000000−8000FFFF)
† General Fail conditions:
1. The accesses must be within the same bank.
2. The first cycle must be a STB Reg, dst1[0] instruction.
3. The second cycle can be any instruction that accesses byte 1 of the same bank as the previous STB instruction.

Workaround: Use half-word and word stores (STH, STW rather than STB). This can be done from C by using long, int, and short rather than char.
In Assembly, add a NOP after an STB instruction or move any following accesses to byte 1 of the same bank one cycle away.

This has been fixed on Revison 1.3.

5 Silicon Revision 1.0 Known Design Exceptions to Functional Specifications

Advisory 1.0.1	*Data Corruption of STB on 0−1 or 2−3 Byte-Boundary*

Revision(s) Affected: 1.0

Details: Data corruption occurs when a write to data memory is followed by an instruction that modifies the byte-enables on a 0−1 or a 2−3 byte boundary, as shown in Figure 2. Essentially, an STB instruction acts as an STH instruction. Data corruption occurs at the address referenced by the first instruction. Reads from data memory, as well as both read and write accesses to program memory and external memories do not exhibit this issue.

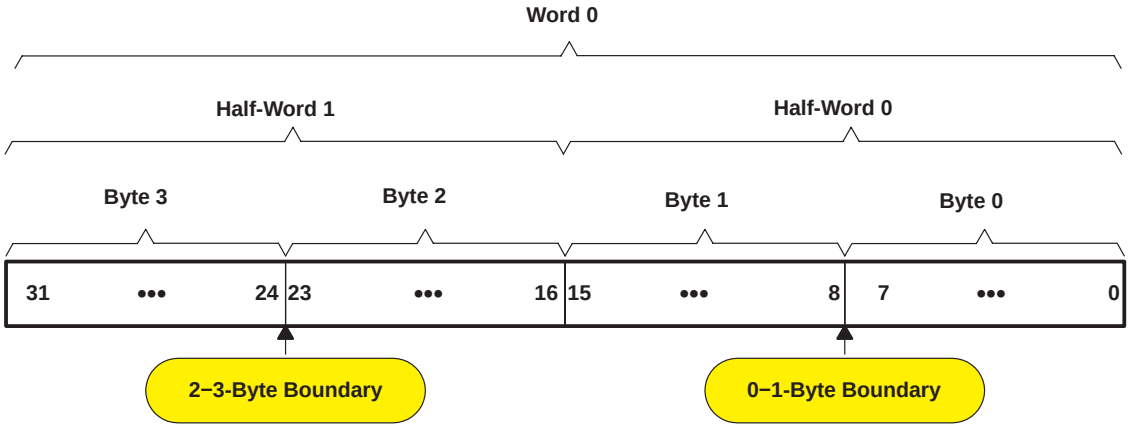


Figure 2. Diagram Showing the 0−1 and 2−3 Byte-Boundary From a Word in Data Memory

Data Corruption of STB on 0−1 or 2−3 Byte-Boundary (Continued)

Examples: The examples listed in Table 3 show some general coding where the bug occurs.

Table 3. Example Execute Packets

Example Number	Execute Packet	Possible Instructions
1	First	STB reg, byte0, or STH reg, half_word0, or STW reg, word0
	Second	STB reg, byte1, or LDB reg, byte1
2	First	STB reg, byte1, or STH reg, half_word0, or STW reg, word0
	Second	STB reg, byte0, or LDB reg, byte0
3	First	STB reg, byte3, or STH reg, half_word1, or STW reg, word0
	Second	STB reg, byte2, or LDB reg, byte2

In these examples, the second execute packet contains an instruction that modifies a byte on either a 0−1 byte-boundary (Examples 1 and 2) or a 2−3 byte-boundary (Example 3).

Workaround: Utilize half-word and word accesses instead of byte-wide accesses.

Avoid use of the char type from C.

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