Jump Start Upgrading Your Digital Cluster Design with Jacinto™ 6 Platform

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Instrument panels are a critical part of the automotive industry's ongoing digital cockpit revolution. The new digital solutions will enable more complex content, larger displays and new ergonomics, including the addition of augmented reality head-up displays (HUDs).

With display prices coming down, a digital cluster solution becomes cost competitive with analog/hybrid clusters, while providing a number of key advantages over traditional instrument clusters, including delivering more relevant content to the driver, including media, larger maps, etc., and enabling customized display content based on driving modes (normal, sport, off-road, etc.). Digital cluster solutions also provide a uniform look and feel across the full original equipment manufacturer (OEM) model range and enable OEMs to integrate new features such as HUDs and driver monitoring, as well as to differentiate among various car models with software while using the same cluster hardware system.

As digital cluster graphical content and display resolution increases, microcontroller (MCU)-based solutions cannot satisfy the system requirements. Only a powerful applications processor can handle the increased requirements.

The Texas Instruments (TI) Jacinto™ 6 system-on-chip (SoC) family offers a scalable solution from entry to premium digital clusters while addressing the graphics, safety and fast-boot requirements of cluster systems. This white paper will describe a digital cluster system and software solution based on Jacinto 6 SoCs, discuss software and ecosystem support and cover a number digital cluster proof of concepts running on the Jacinto 6 processor family.

Digital cluster system requirements

Moving from an analog to digital instrument cluster introduces a number of unique challenges, as there are many key system requirements in a digital cluster system solution.

The first requirement is graphics performance and high resolution display support. As digital cluster solutions are replacing analog clusters, OEMs and drivers expect smooth, picture-realistic graphics performance with relevant graphical content. The needles for speed and RPM need to be rendered at 60fps to guarantee smooth movement. Display resolution requirements are increasing, making high resolution display support critical.

Today, a 12.3-inch 1920x720p resolution display is typically used, but some OEMs are looking to move to 2880x1080p in the next generation to support higher quality graphics and a better driver experience. Rendering graphics on such high-resolution displays at high frame rates requires an application processor with powerful graphics and memory throughput performance.

The second system requirement is safety. While not all graphics content is safety-related, tell-tale alerts such as check-engine and faulty brake warnings are. Thus, cluster systems require ASIL-B certification for tell-tale rendering. In addition, audio warnings, such as an improperly closed door alert or seat-belt chimes, that are part of a safety component might require an ASIL-A rating for the audio driver in a cluster system.

The third system requirement is fast system boot. Drivers expect to have all gauges active as soon as they turn on the ignition. This requires the full system – including display and graphics – to be active in less than 1s from cold start.

OEMs are increasingly integrating new features into digital cluster systems, including HUDs driven from the cluster SoC or a driver monitoring solution. Thus, seamless integration of content from the head unit to the cluster display is a must-have feature. This will entail moving data from the head unit over a car network such as Ethernet Audio Video Bridging (eAVB) and rendering and displaying it on the cluster screen. Transferring data as a video stream may require the cluster SoC to have video decode capabilities.

Finally, digital cluster system bill of materials (BOM) will need to be optimized. This requires a scalable, software-compatible solution that OEMs/Tier 1s can scale up and down in price and performance; multi-display, multi-camera support; and the integration of automotive peripherals such as Controller Area Network (CAN) and eAVB. While power and thermal performance are sometimes overlooked system parameters, they also impact system BOM as the digital cluster system might require additional components such as fan.

Digital cluster system block diagram

Figure 1 shows a high-level system block diagram for a digital cluster solution based on TI Jacinto 6 SoCs. In a typical digital cluster system, the application processor runs a high-level operating system such as Linux, QNX or Integrity and manages all system components.

Besides the application processor, the block diagram includes many other system components, such as:

- A power-management integrated circuit (PMIC) to manage system power.
- Flash to store boot images and the files system. Two common flash interfaces on the Jacinto 6 are Quad Serial Peripheral Interface (QSPI) and Embedded Multimedia Card (eMMC).
- A vehicle MCU to manage input/output, full system wakeup and potentially the CAN stack. The application processor might also handle network stacks such as CAN and eAVB.
- A camera input to feed input from the head unit, rear-view or driver-monitoring cameras.
- A flat panel display (FPD)-Link serializer/deserializer for remote displays.

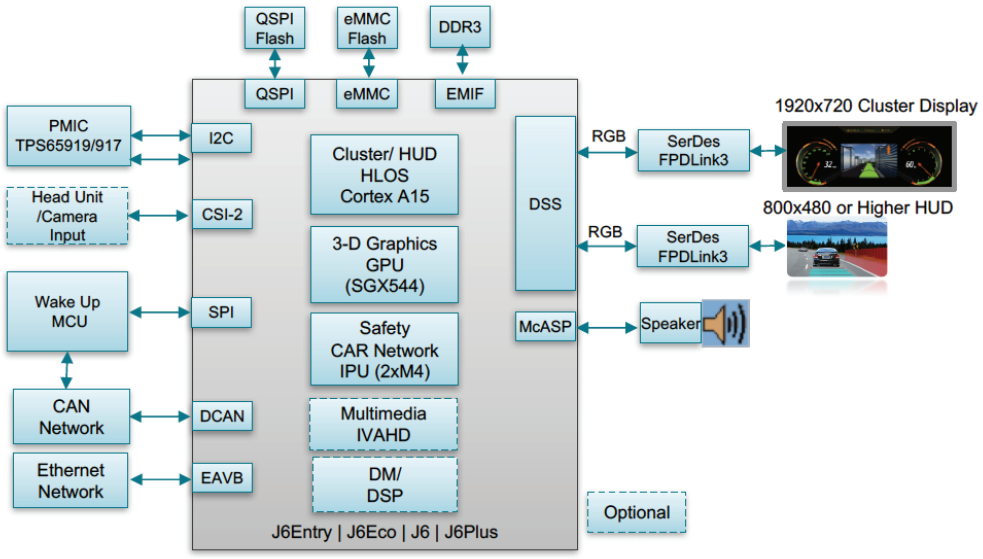

***Figure 1**. Digital cluster system block diagram.*

Jacinto 6 Platform for Digital Cluster

Jacinto 6 SoC family provides a scalable, software compatible platform that addresses digital cluster system requirements.

The Jacinto 6 SoC architecture for digital cluster systems

The Jacinto 6 SoC family is a multi-core heterogeneous architecture, as shown in Figure 2. In addition to powerful microprocessor units (MPUs), dedicated hardware accelerators handle specific tasks to enable the best performance, power and cost trade-offs. Jacinto 6 processing cores include general-purpose MPUs based on Arm® Cortex®-A15 cores, which run high-level operating systems such as Linux, QNX or Integrity and manage key system components and middleware, including graphics and displays. Jacinto 6 graphics processing units (GPUs) handle all graphics rendering. There are both 3-D and 2-D graphics cores. The auxiliary MPUs (AMPUs) are smaller ARM cores. In the Jacinto 6 family, they are multiple Cortex-M4 cores that can handle CAN or Ethernet communication, as well as all safety-critical components. Digital signal processors (DSPs) are optionally available and enable additional features such as driver monitoring and identification. Multimedia cores handle the video decode and encode requirements of the cluster system. In addition to processing cores, application processor memory throughput is critical to handle all data movements and avoid system performance bottlenecks. Also, there are a set of peripherals, including CAN, eAVB, multidisplay output and multi-camera input, to enable the best system BOM cost.

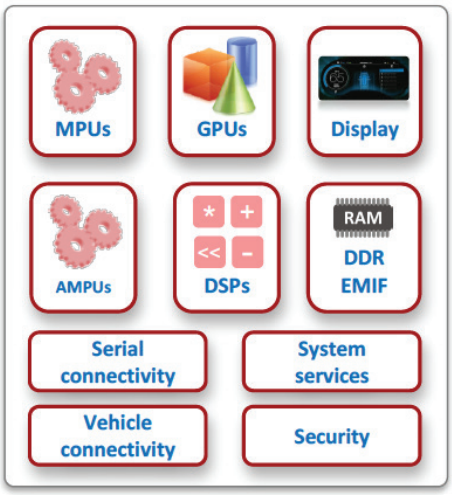

***Figure 2**. Jacinto 6 multicore heterogeneous architecture.*

Feature	Jacinto 6 Entry (DRA71x)	Jacinto 6 Eco (DRA72x)	Jacinto 6 (DRA74x)	Jacinto 6 Plus (DRA76x)
Cluster Display Resolution	1920x720 @60fps →		2880x1080@60fps	
	J6-Entry • 1x A15 & 4x M4 • 1x SGX544 • 17x17 package	Pin2Pin compatible J6-Eco • 1x A15 & 4x M4 • 1x SGX544 • 23x23 package	Jacinto 6 • 2x A15 & 4x M4 • 2x SGX544 • 23x23 package	J6-Plus • 2x A15 & 4x M4 • 2x SGX544 • 23x23 package
MPU (DMIPs)	Up to 3.5K	Up to 5.25K	Up to 10.6K	Up to 12.7K
Aux MPU (Mhz)	2x Dual-M4 (212)	2x Dual-M4 (212)	2x Dual-M4 (212)	2x Dual-M4 (212)
3D GPU (GFLOPS)	SGX544 (Up to 13.6)	SGX544 (Up to 17)	SGX544-MP2 (Up to 34)	SGX544-MP2 (Up to 42.5)
2D GPU (Mhz)	GC320 (354)	GC320 (354)	GC320 (354)	GC320 (354)
Memory BW (GB/s)	Up to 5.3	Up to 5.3	Up to 8.5	Up to 10.7
Optional cores	IVA-HD (Multimedia HD video decode and encode for infotainment content integration) C66x DSP (for driver monitoring system integration)			
Power Management	TPS65919	TPS65917	TPS65917 or TPS659039	TPS659039
Software Compatibility	Software Compatible			

***Figure 3**. Jacinto 6 digital cluster roadmap.*

Jacinto 6 Processor Roadmap for Digital Cluster

There are a number of devices in Jacinto 6 family targeted for digital cluster solutions. The Jacinto 6 processor roadmap for cluster is shown in **Figure 3**.

Jacinto 6 family performance scalability is highlighted in **Figure 4** below:

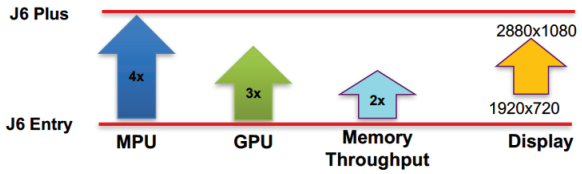

***Figure 4**. Jacinto 6 family performance scalability.*

Graphics performance and display subsystem

Graphics performance is one of the most – if not the most – critical criteria for a digital cluster system. As shown in **Figure 5**, Jacinto 6 SoCs include a high-performance graphics subsystem, featuring:

- A 3-D GPU based on Imagination Tech's SGX544 to handle all 3-D graphics rendering as well as support for OpenGL ES application programming interfaces (APIs).
- A 2-D GPU based on Vivante's GC320 to handle both multilayer composition and 2-D graphic rendering, as well as support for 2-D graphics APIs.
- A powerful display subsystem with four independent input pipelines with overlay support, support for up to four concurrent HD displays for driver digital cluster and HUDs, and an independent write-back pipeline for safety frame checking.
- High resolution display support from 1920x720 at 60fps with Jacinto 6 Entry, the lowest cost processor in the Jacinto family, and Jacinto 6 Eco to 2880x1080 at 60 fps with Jacinto 6 and Jacinto 6 Plus SoC.

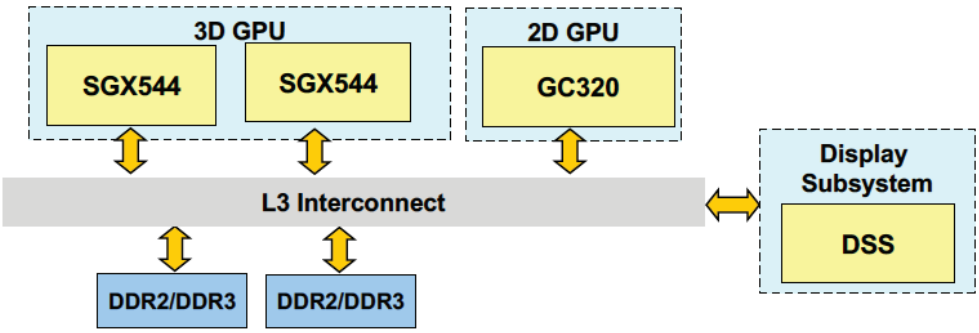

***Figure 5**. Jacinto 6 graphics and display subsystem architecture.*

Safety support

There are a number of safety features embedded into Jacinto 6 SoCs that can help achieve the safety goals at the system level. Some of these features include:

- Hardware firewalls and MMUs to enable freedom from interference, which is critical to achieve ASIL-B safety goal,
- Separation of peripherals into safety and non-safety domains with hardware firewalls,
- Display write-back path for frame monitoring,
- Error- correction support on external memory interfaces,
- Memory access and L3 interconnect prioritization to provide robustness for heavy double-data-rate (DDR) load and interconnect loads,
- Secure boot and run-time security support with high-security (HS) devices,
- Auxiliary MPU (M4s) and DSPs, used to isolate safety critical components including frame-monitoring and watchdog timers.

By leveraging auxiliary MPU cores on the Jacinto 6 and hardware firewalls, TI developed and demonstrated an ASIL-B software architecture with a proof of concept (POC); see **Figure 6**.

In this architecture, all safety-critical components (tell-tales, display driver and CAN stack) run on an auxiliary MPU core based on a safety real-time operating system (RTOS). The MPU running a high-level operating system (HLOS) handles all non-safety critical components, including 3-D graphics.

Hardware firewalls isolate safety-critical components from non-safety-critical SoC components, as well as isolating memory regions accessed by the safety RTOS to guarantee freedom from interference.

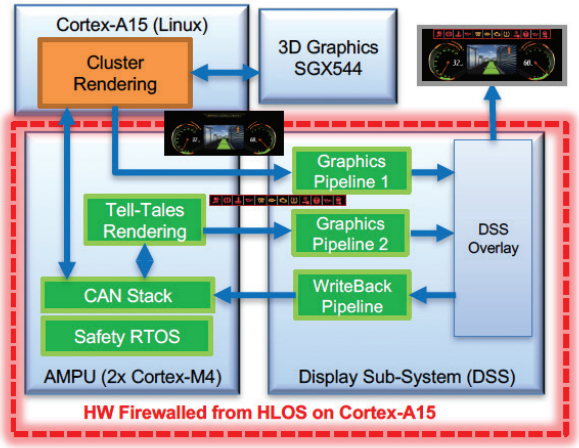

***Figure 6**. Jacinto 6 safety architecture based on AMPU.*

Finally, display subsystem write-back pipelines send frames going out to the display back to the memory for further frame checking in order to ensure the proper rendering of tell-tales.

Early and fast boot

Jacinto 6 SoCs provide the capabilities needed to meet the fast boot requirements of digital cluster systems, with powerful MPUs to load and execute boot images; fast flash interfaces including QSPI and eMMC to move data to external DDR memory; and auxiliary MPU cores to load and start a secondary RTOS boot image in parallel with HLOS, enabling bringing-up display and other boot features very early in the boot process.

System BOM optimization

Jacinto 6 SoCs provide a number of features to optimize the system BOM for a digital cluster solution, including:

- 100% software compatible platform from Jacinto 6 Entry to Jacinto 6 Plus,
- Pin-to-pin compatibility options from Jacinto 6 Eco, Jacinto 6 and Jacinto 6 Plus,
- Cost-optimized power solutions (PMICs) for each Jacinto 6 SoC,
- Multi-HD display support to enable HUD integration,
- Multi-camera input to enable rear camera and/or driver-monitoring camera inputs,
- Optional DSP and multimedia cores to integrate features such as driver monitoring and identification, and smartphone projection without significant increase in system cost. **Figure 7** shows a reference architecture,
- Automotive peripherals including eAVB, CAN and Media Oriented Systems Transport (MOST),
- A rich set of high-speed and connectivity interfaces including Peripheral Component Interconnect Express (PCIe), USB, I2S, etc.,
- A six-layer PCB design to save board cost,
- Power and thermal performance to reduce system cost.

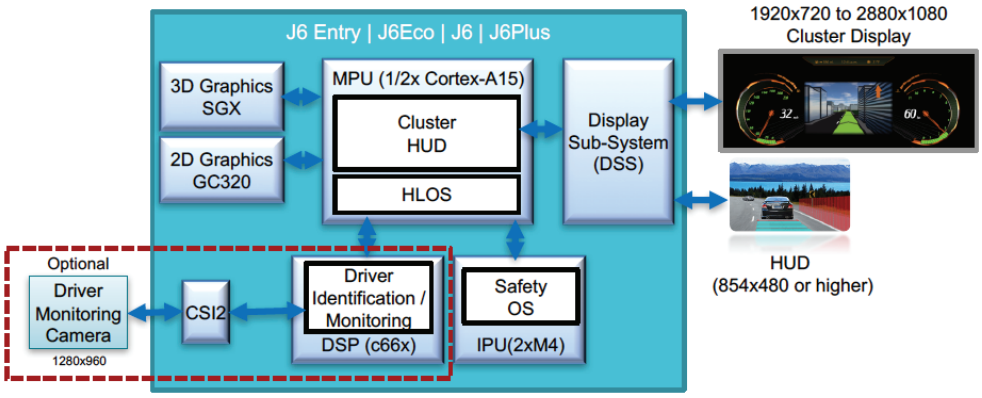

***Figure 7**. Jacinto 6 architecture to integrate driver monitoring and HUDs.*

Software and ecosystem support

The software-compatible Jacinto 6 platform has very mature software and ecosystem support. These HLOS and RTOS software development kits (SDKs) are available for all Jacinto 6 devices:

- Linux SDK.
- Automotive-grade Linux.
- Mentor Connected OS GENIVI Linux.
- Green Hills Integrity SDK.
- QNX SDKs (both on QNX 6.5 SP1 and QNX 6.6 kernels).
- Mentor Nucleus on Cortex-A15 and Cortex-M4s.
- TI SysBIOS on Cortex-M4s and C66x DSPs.

Figure 8 shows all of the major third party solutions available on the Jacinto 6 platform. For example, all major human machine interface (HMI) toolkits from Altia, Crank Storyboard, DisTI GLStudio, Rightware Kanzi and Socionext CGIStudio are already ported to the Jacinto 6 platform.

POCs

Over the years, a number of digital cluster POCs have been created on the Jacinto 6 platform to demonstrate graphics performance, safety support, early and fast boot, CAN integration and other features:

- Jacinto 6 Entry stand-alone cluster POC based on Linux running on a Cortex-A15 and Mentor Nucleus RTOS on a Cortex-M4 demonstrating 60fps cluster performance on a 1920 by 720 display and safety architecture based on auxiliary MPU core.
- Jacinto 6 stand-alone cluster POC based on Green Hills Integrity running on a Cortex -A15 demonstrating safety architecture.
- Jacinto 6 Entry enables safety certifiable digital cluster at optimized cost.

Features/Functions	Partner Names	Partners Logo
Graphics / HMI partners Industry-leading HMI development tool kits	Altia | Crank | Elektrobit Mentor Embedded Rightware Kanzi | DiSTI Socionext |	altia socionext Mentor Automotive Crank RIGHTWARE DiSTI
Hypervisor partners	GlobalLogic | Green Hills Software | QNX | Mentor Embedded | OpenSynergy	GlobalLogic Mentor Automotive Green Hills QNX OPENSYNERGY
RTOS / Early features	QNX | Mentor Embedded Green Hills Software Texas Instruments	Mentor Automotive Green Hills QNX Texas Instruments
Automotive Stack	Cetitec | Excelfore Mentor Embedded | Elektrobit | Vector Software	CETITEC excelfore Mentor Automotive vector ARC CORE

***Figure 8**. Jacinto 6 digital cluster ecosystem support.*

Conclusion

The digital cluster market is an exciting one that will continue to grow. TI's Jacinto 6 SoC family is a very compelling platform for the stand-alone cluster market, addressing both current as well as next-generation digital cluster solution requirements with a scalable, mature, cost-competitive and software-compatible platform, along with mature and comprehensive software SDKs and ecosystem support.

For more details, see http://www.ti.com/jacinto.

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