KeyStone Architecture II
Gigabit Ethernet (GbE) Switch Subsystem for K2E and K2L Devices

User's Guide

Literature Number: SPRUHZ3A
August 2014–Revised April 2015

Contents

List of Figures

List of Tables

Preface

About This Manual

This document gives a functional description of the Ethernet Switch Subsystem module. The Ethernet Switch Subsystem consists of the Ethernet Media Access Controller (EMAC) module, Serial Gigabit Media Independent Interface (SGMII) modules, Physical Layer (PHY) device Management Data Input/Output (MDIO) module, Ethernet Switch module, and other associated submodules that are integrated on the device.

Notational Conventions

This document uses the following conventions:

- Commands and keywords are in **boldface** font.
- Arguments for which you supply values are in *italic* font.
- Terminal sessions and information the system displays are in screen font.
- Information you must enter is in **boldface screen font**.
- Elements in square brackets ([ ]) are optional.

Notes use the following conventions:

NOTE: Means reader take note. Notes contain helpful suggestions or references to material not covered in the publication.

The information in a caution or a warning is provided for your protection. Please read each caution and warning carefully.

CAUTION

Indicates the possibility of service interruption if precautions are not taken.

WARNING

Indicates the possibility of damage to equipment if precautions are not taken.

Related Documentation from Texas Instruments

Multicore Navigator for KeyStone Devices User's Guide	SPRUGR9
Network Coprocessor (NETCP) for K2E and K2L Devices User's Guide	SPRUHZ0
Packet Accelerator 2 (PA) for K2E and K2L Devices User's Guide	SPRUHZ2
Phase Locked Loop (PLL) Controller for KeyStone Devices User's Guide	SPRUGV2
Security Accelerator 2 (SA2) for K2E and K2L Devices User's Guide	SPRUHZ1

Introduction

NOTE: The information in this document should be used in conjunction with information in the device-specific Keystone Architecture data manual that applies to the part number of your device.

This document provides a functional description of the Ethernet switch subsystem for the TCI6630K2L, 66AK2Ex, and AM5K2Ex devices. The Ethernet switch subsystem consists of the serial gigabit media-independent interface (SGMII) modules, physical layer (PHY) device management data input/output (MDIO) module, Ethernet switch module, and other associated submodules that are integrated on the device. Included in this document are the features of the MDIO, SGMII, and Ethernet switch, a discussion of their architecture and operation, an overview of the internal and external connections, and descriptions of the registers for each module.

Topic **Page**

1.1 Purpose of the Peripheral

The gigabit Ethernet (GbE) switch subsystem is one of the main components of the network coprocessor (NetCP) for K2E/K2L peripheral. The GbE switch subsystem works together with the Packet Accelerator (PA2) and Security Accelerator (SA2) to form a network processing solution. The purpose of the gigabit Ethernet switch subsystem in the NetCP is to provide an interface to transfer data between the host device and another connected device in compliance with the Ethernet protocol.

NOTE: For the purposes of this document, the terms 'ingress' and 'egress' are from the perspective of the center of the GbE switch. For example, a packet generated by the host and sent out of the device through Ethernet port 1 will go through the 'ingress' process of the switch at host port 0 and will go through the 'egress' process of the switch at port 1. As another example, a packet that is received at Ethernet port 3 that is destined for the host will go through the 'ingress' process of the switch at port 3 and will go through the 'egress' process of the switch at host port 0.

1.2 Features

The GbE switch subsystem has the following features:

- N-1 10/100/1000 Ethernet ports with SGMII interfaces (where N = 5 for a 5-port switch and N = 9 for a 9-port switch)
- SGMII Interface
- Wire-rate switching (802.1d)
- Non-Blocking switch fabric
- Flexible logical FIFO-based packet buffer structure
- Eight priority level QOS support (802.1p)
- Host port 0 Streaming Interface
- IEEE 1588 Clock Synchronization Support
- Ethernet port reset isolation
- Address Lookup Engine
- 1024 or 8192 addresses plus VLANs (see the ALE_STATUS Register)
- Wire-rate lookup
- VLAN support
- Host controlled time-based aging and/or auto-aging
- Spanning tree support
- L2 address lock and L2 filtering support
- MAC authentication (802.1x)
- Receive or destination-based Multicast and Broadcast limits
- MAC address blocking
- Source port locking
- OUI host accept/deny feature
- Flow Control Support (802.3x)
- Priority-Based Flow Control Support (802.1QBB)
- EtherStats and 802.3 Stats RMON statistics gathering (per port)
- MAC transmit to MAC receive loopback mode (digital loopback) support
- SGMII or SerDes loopback modes (transmit to receive)
- Maximum frame size 9600 bytes (9604 with VLAN)
- MDIO module for PHY management
- Programmable interrupt control with selected interrupt pacing

- Emulation support
- Asynchronous Streaming Packet Interface

The gigabit Ethernet (GbE) switch subsystem does not support 1000-MHz half-duplex mode

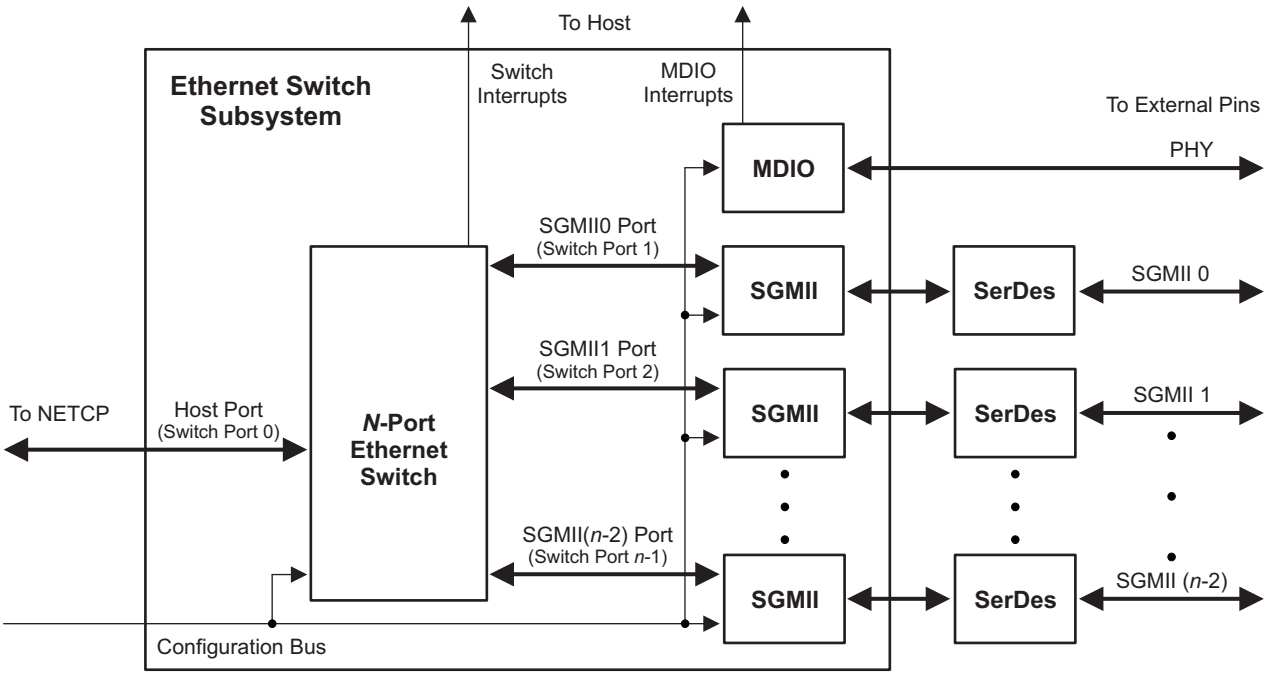
1.3 Gigabit Ethernet Switch Subsystem Functional Block Diagram

The GbE switch subsystem consists of the following major modules:

- Gigabit Ethernet switch
- MDIO module
- N-1 SGMII modules (N = 5 for a 5-port switch and N = 9 for a 9-port switch)
  - SGMII0
  - SGMII1
  - SGMII2
  - SGMII3
  - SGMII4 (Only available in devices with a 9-port switch)
  - SGMII5 (Only available in devices with a 9-port switch)
  - SGMII6 (Only available in devices with a 9-port switch)
  - SGMII7 (Only available in devices with a 9-port switch)

Figure 1-1 shows the gigabit Ethernet (GbE) switch subsystem functional block diagram. It has N ports (where N is either 5 or 9), bus configuration through the network coprocessor (NetCP), and a set of interrupts going to the host.

Figure 1-1. Ethernet Switch Subsystem Block Diagram for an N Port Switch



The SGMII modules connect through a SerDes to external pins, and have the Ethernet switch as their source. All SGMII modules in the subsystem follow the same protocol and methods.

- Port 0 is the host port, which allows bidirectional communication between the GbE Switch and the NetCP.
- Port 1 is the SGMII 0 port, which allows bidirectional communication between the GbE switch and the SGMII 0 module.
- Port 2 is the SGMII 1 port, which allows bidirectional communication between the GbE switch and the SGMII 1 module.
- Port 3 is the SGMII 2 port, which allows bidirectional communication between the GbE switch and the SGMII 2 module.
- Port 4 is the SGMII 3 port, which allows bidirectional communication between the GbE switch and the SGMII 3 module.
- Port 5 is the SGMII 4 port, which allows bidirectional communication between the GbE switch and the SGMII 4 module. (Only available in devices with a 9-port switch)
- Port 6 is the SGMII 5 port, which allows bidirectional communication between the GbE switch and the SGMII 5 module. (Only available in devices with a 9-port switch)
- Port 7 is the SGMII 6 port, which allows bidirectional communication between the GbE switch and the SGMII 6 module. (Only available in devices with a 9-port switch)
- Port 8 is the SGMII 7 port, which allows bidirectional communication between the GbE switch and the SGMII 7 module. (Only available in devices with a 9-port switch)
- Interrupts from the GbE switch are connected to the host processor to allow communication of the switch status.
- A configuration bus connects the GbE to the NetCP to allow the user to configure the switch.

The SGMII modules each have a separate connection to the GbE switch, the SerDes, and the configuration bus.

- The SGMII connection to the GbE switch allows bidirectional communication between the SGMII module and the switch.
- The SGMII connection to the SerDes allows bidirectional communication between the SGMII module and the SerDes.
- A configuration bus connects each SGMII to the NetCP to allow the user to configure the SGMII modules.

The MDIO module, as shown in Figure 1-1, contains a connection to an external PHY device, a set of interrupts going to the host, and bus configuration through the network coprocessor.

- The connection to an external PHY device allows the MDIO module to monitor the link status of up to 32 addresses.
- Interrupts from the MDIO module are connected to the host to allow communication of changes in link status.
- A configuration bus connects the MDIO to the NetCP to allow the user to configure the MDIO.

1.4 Industry Standard(s) Compliance Statement

The gigabit Ethernet switch subsystem conforms to the following industry standards:

- Supports IEEE 802.3 specification
- Supports IEEE 1588 specification

Architecture

Topic **Page**

2.1 Clock Control

This section describes the clocks used by the gigabit Ethernet (GbE) switch subsystem.

The GbE switch subsystem uses the following clocks:

- GbE switch subsystem clock
- SGMII SerDes reference clock
- IEEE 1588 time synchronization clock
- MDIO clock
- GMII clock

2.1.1 Gigabit Switch Subsystem Clock

The gigabit Ethernet (GbE) switch subsystem clock, which operates at 350 MHz, is used for most of the logic in the GbE switch subsystem. The GbE switch subsystem clock domain must be enabled before using the GbE switch subsystem.

2.1.2 SGMII SerDes Reference Clock

For more information on the SerDes as well as its reference clock, see the device-specific data manual and *SerDes User's Guide* (SPRUHO3).

2.1.3 MDIO Clock

The MDIO clock is divided down from the peripheral system clock. The MDIO clock can operate at up to 2.5 MHz, but typically operates at 1.0 MHz.

2.1.4 IEEE 1588 Time Synchronization Clock

The IEEE 1588 time synchronization clock is used for the time synchronization module in the GbE switch. There are several possible inputs that can be used for the time synchronization clock. To select an input clock source for the CPTS_RCLK, program the CPTS_RFTCLK_SEL field in the CPTS_RFTCLK_SEL register. For a list of clock sources corresponding to the values in the CPTS_RFTCLK_SEL register, see the device-specific data manual.

2.1.5 GMII Clock

The GMII clock frequencies are fixed by the 802.3 specification as follows:

- 2.5 MHz at 10 Mbps
- 25 MHz at 100 Mbps
- 125 MHz at 1000 Mbps

2.2 Memory Map

The memory map for the modules in the GbE switch subsystem are shown in the table below. The addresses listed are offset addresses, which are dependent on a device-specific base address. For the base address of the GbE switch subsystem, see the memory map in the device-specific data manual.

Table 2-1. Gigabit Ethernet Switch Subsystem Modules

Module Region	Offset Address[1]
Gigabit Ethernet (GbE) switch subsystem	000h
Port 1 SGMII module	100h
Port 2 SGMII module	200h
Port 3 SGMII module	300h
Port 4 SGMII module	400h
Port 5 SGMII module	500h
Port 6 SGMII module	600h
Port 7 SGMII module	700h
Port 8 SGMII module	800h
Reserved	900h-EFFh
MDIO module	F00h
Reserved	1000h-1FFFFh
Gigabit Ethernet (GbE) switch module	20000h

(1) The addresses provided in the table are offsets from a device specific base address. To determine the base address of these registers, see the device-specific data manual.

2.3 Gigabit Ethernet Switch Architecture

This section describes the architecture of the gigabit Ethernet (GbE) switch module.

NOTE: For the purposes of this document, the terms ‘ingress’ and ‘egress’ are from the perspective of the center of the GbE switch. For example, a packet generated by the host and sent out of the device through Ethernet port 1 will go through the ‘ingress’ process of the switch at host port 0 and will go through the ‘egress’ process of the switch at port 1. As another example, a packet that is received at Ethernet port 3 that is destined for the host will go through the ‘ingress’ process of the switch at port 3 and will go through the ‘egress’ process of the switch at host port 0.

The GbE provides an interface between the packet streaming switch in the NetCP and the SGMII modules in the Ethernet switch subsystem. The following submodules are part of the GbE switch:

- Streaming Packet Interface (Section 2.3.1)
- Media Access Controller Submodule Architecture (Section 2.3.2)
- MAC Receive FIFO Architecture (Section 2.3.3)
- Statistics Submodule Architecture (Section 2.3.5)
- Time Synchronization Submodule Architecture (Section 2.3.6)
- Address Lookup Engine (ALE) Submodule Architecture (Section 2.3.7)
- Error Correction Code (ECC) Submodule (Section 2.3.8)

The gigabit Ethernet switch has N ports (either five or nine depending on your device): host port 0 communicates with the packet streaming switch, Ethernet port 1 communicates with the SGMII0 module, Ethernet port 2 communicates with the SGMII1 module, and so on up to Ethernet port N-1.

To interface to the packet streaming switch, the GbE switch contains transmit and receive interfaces to convert between the signals used by the GbE switch and the signals used by the packet streaming switch. To facilitate communication with the SGMII modules, each Ethernet-facing port has a MAC submodule to convert between the signals internal to the switch and the GMII signals required by the SGMII modules.

The GbE switch also contains several other submodules that provide additional features. The GbE switch has a module for each port that provides Ethernet statistics for the packets transmitted and received by the Ethernet switch subsystem. The GbE switch also contains a time synchronization submodule to support IEEE 1588 clock synchronization. The GbE switch provides an address lookup engine (ALE), which is responsible for forwarding and filtering packets based on address. There also is an ECC module in the switch that implements error detection and correction on the packet headers in the switch RAMs. Each of these submodules is covered in more detail in the respective submodule sections.

2.3.1 Streaming Packet Interface

This section describes the details of the streaming packet interface. The streaming packet interface is responsible for communication between the GbE switch and the packet streaming switch in the NetCP.

2.3.1.1 Transmit Streaming Packet Interface (Host Port 0 Switch Egress)

The transmit interface is responsible for transmitting packets from the GbE switch host port 0 to the packet streaming switch in the NetCP. The GbE switch has one transmit streaming packet interface (TXST). All packets received on an Ethernet port that are destined for the NetCP through host port 0 use the TXST interface. The data on the streaming interface is equivalent to MAC output data with the difference being that 128-bit streaming interface data is output instead of outputting 8-bit GMII data.

In addition to the packet data, the transmit streaming interface also provides additional information that is placed in the descriptor of the received packet by the receive flow of the packet DMA. Included in this extra information is source identification. If the packet originated from Ethernet port 1, then the value in P1_SRC_ID field of the P0_SRC_ID_A register will be placed in the SRC_ID field in the descriptor of the receive packet. If the packet originated from Ethernet port 2, then the value in P2_SRC_ID field will be used and so on up to Ethernet port 4. For a 9-port switch, with eight Ethernet ports, there is the P0_SRC_ID_B register that contains the Pn_SRC_ID fields for Ethernet ports 5-8 that will be placed in the SRC_ID field in the descriptor.

Also included in the extra information placed in the descriptor of the received packet is:

- Whether or not CRC was passed with the packet:
  - Determined by the P0_TX_CRC_REM bit in the CPSW_CONTROL register
- What type of CRC was passed with the packet:
  - Either Ethernet CRC or Castagnoli CRC which is determined by the P0_TX_CRC_TYPE bit in the CPSW_CONTROL register (this is not determined by the type of CRC that the packet had on Ethernet port ingress)
- The streaming packet interface thread that the packet was received on (discussed in the paragraph below)

The transmit streaming packet interface (TXST) has eight egress threads for each external Ethernet port (32 threads in a 5-port switch or 64 threads in a 9-port switch). Each of the individual egress threads represents the Ethernet port that the packet was received on as well as the hardware switch priority of the packet. Each packet is sent on a single thread and although there are multiple threads, only a single thread has transmit data at any given time. The egress thread that a packet uses in the TXST is decided as follows:

- Packet received at Ethernet port 1
  - Thread selected is from 0-7 based on the hardware switch priority, where priority 0 corresponds to thread 0, priority 1 corresponds to thread 1 and so on up to priority 7 corresponding to thread 7.
- Packet received at Ethernet port 2
  - Thread selected is from 8-15 based on the hardware switch priority, where priority 0 corresponds to thread 8, priority 1 corresponds to thread 9 and so on up to priority 7 corresponding to thread 15.
- This pattern is followed up to thread 31 on a 5-port switch and up to thread 63 on a 9-port switch. Check your device specific data manual to find out how many ports your device contains.

2.3.1.1.1 CRC Handling (Host Port 0 Egress)

The P0_TX_CRC_REM bit in the CPSW_CONTROL register determines if host port egress packets have CRC included or not. If P0_TX_CRC_REM is set to 1 then all packets that are transmitted from port 0 do not contain CRC. If P0_TX_CRC_REM is cleared to 0 then all packets that are transmitted from port 0 contain CRC. The CRC type, if present, is determined by the P0_TX_CRC_TYPE bit in the CPSW_CONTROL register. If the P0_TX_CRC_TYPE bit is cleared to 0 then the CRC present in each packet after host port egress is Ethernet CRC. If the P0_TX_CRC_TYPE bit is set to 1 then the CRC present in each packet after host port egress is Castagnoli CRC.

NOTE: The CRC type present in the packet after host port egress is determined solely by the P0_TX_CRC_TYPE bit in the CPSW_CONTROL Register regardless of the CRC type present in the packet during Ethernet port ingress.

2.3.1.1.2 Transmit VLAN Processing

Transmit packets are NOT modified during switch egress when the VLAN_AWARE bit in the CPSW_CONTROL register is cleared to 0. This means that the switch is not in VLAN-aware mode.

The next three sections cover transmit processing when the switch is in VLAN-aware mode for different packet types. The GbE switch is in VLAN-aware mode when the VLAN_AWARE bit is set in the CPSW_CONTROL register. While in VLAN-aware mode, VLAN is added, removed, or replaced according to the type of packet as well as the FORCE_UNTAGGED_EGRESS bit in the packet header as explained below.

2.3.1.1.2.1 Untagged Packets (No VLAN or Priority Tag Header)

Untagged packets are all packets that are not a VLAN packet or a priority tagged packet. According to the FORCE_UNTAGGED_EGRESS bit in the packet header the packet may exit the switch with a VLAN tag inserted or the packet may leave the switch unchanged. The two cases are discussed below.

- Insert VLAN Case:
  Untagged input packets have the header packet VLAN inserted when the FORCE_UNTAGGED_EGRESS bit in the transmit packet header is de-asserted. For untagged packets, the The VLAN EtherType = 0x8100 is inserted after the source address followed by the two-byte header packet VLAN. The header packet VLAN is composed of the header packet priority along with the PORT_CFI and and PORT_VID values from the Pn_PORT_VLAN register where n is the port that the untagged packet entered the switch through. The packet length/type field is output four bytes later than it is input and is not removed or replaced. If the CRC is present in the packet data (PASS_CRC is asserted), then the packet CRC is replaced with a hardware generated CRC.
- No Change Case:
  Untagged input packets are output unchanged when the FORCE_UNTAGGED_EGRESS transmit packet header bit is asserted.

2.3.1.1.2.2 Priority Tagged Packets (VLAN VID == 0 && EN_VID0_MODE ==0)

Priority tagged packets are packets that contain a VLAN header with VID = 0. According to the FORCE_UNTAGGED_EGRESS bit in the packet header, priority tagged packets may exit the switch with their VLAN ID and priority replaced or they may have their priority tag completely removed. The two cases are discussed below.

NOTE: In order for a priority tagged packet to fall into this category the EN_VID0_MODE bit in the ALE_CONTROL register must also be set to 0. If the EN_VIDO_MODE bit in the ALE_CONTROL register is set to 1, then packets with a VLAN VID of 0 will fall into the VLAN Tagged Packets category in Section 2.3.1.1.2.3 below.

- Replace Priority and VLAN ID Case:
  Priority tagged input packets have the packet VLAN ID and the packet priority replaced with the header packet VLAN ID and the header packet priority when the transmit packet header FORCE_UNTAGGED_EGRESS bit is de-asserted. The header packet VLAN ID comes from the PORT_VID bits in the Pn_PORT_VLAN register where n is the port where the packet entered the switch. The header packet priority is based on the packet priority to header packet priority mapping in the Pn_RX_PRI_MAP register where n is the port where the packet entered the switch.
- Remove VLAN Header Case:
  Priority tagged input packets have the 4-byte packet VLAN information removed when the transmit packet header FORCE_UNTAGGED_EGRESS bit is asserted. The 0x8100 EtherType is removed as is the two byte packet VLAN. Input 64-67 byte priority tagged packets go out with the VLAN removed and padded to 64-bytes if the PASS_CRC input bit is asserted. The input CRC bytes are used as the pad data. Input 64-byte priority-tagged packets use all four input CRC bytes as pad, input 65-byte priority-tagged packets use three of the input CRC bytes as pad, and so on. No pad is performed if the PASS_CRC input bit is not asserted - input 64-67 byte (on the wire) priority-tagged packets go out as 60-63 byte packets. The output CRC is replaced with a generated CRC when the VLAN is removed.

2.3.1.1.2.3 VLAN Tagged Packets (VLAN VID != 0 || (EN_VID0_MODE ==1 && VLAN VID ==0))

VLAN tagged packets are packets that contain a VLAN header specifying the VLAN the packet belongs to (VID), the packet priority (PRI), and the drop eligibility indicator (CFI). According to the FORCE_UNTAGGED_EGRESS bit in the packet header, VLAN tagged packets may exit the switch with their VLAN priority replaced or they may have their VLAN header completely removed. The two cases are discussed below.

- Replace Priority Case:
  VLAN tagged input packets are output with the packet priority replaced with the header packet priority when the transmit packet header FORCE_UNTAGGED_EGRESS bit is deasserted. The header packet priority is based on the packet priority to header packet priority mapping in the Pn_RX_PRI_MAP register where n is the port where the packet entered the switch. If the CRC is present in the packet data (PASS_CRC is asserted), then the packet CRC is replaced with a generated CRC.
- Remove VLAN Header Case:
  VLAN tagged input packets have the 4-byte packet VLAN information removed when the transmit packet header FORCE_UNTAGGED_EGRESS bit is asserted. The 0x8100 EtherType is removed as is the two byte packet VLAN. Input 64-67 byte priority tagged packets go out with the VLAN removed and padded to 64-bytes if the PASS_CRC input bit is asserted. The input CRC bytes are used as the pad data. Input 64-byte priority tagged packets use all four input CRC bytes as pad, input 65-byte priority tagged packets use three of the input CRC bytes as pad, and so on. No pad is performed if the PASS_CRC input bit is not asserted - input 64-67 byte (on the wire) priority tagged packets go out as 60-63 byte packets. The output CRC is replaced with a generated CRC when the VLAN is removed.

2.3.1.2 Receive Streaming Packet Interface (Host Port 0 Switch Ingress)

The receive streaming interface on port 0 of the GbE switch is responsible for receiving packets from the packet streaming switch in the NetCP. The GbE switch has one receive streaming packet interface for port 0. The CPPI receive port is equivalent to a MAC port with the difference being that the data is provided to the GbE switch in the 128-bit streaming interface data format instead of 8-bit GMII data format.

In addition to the packet data, the receive streaming interface also can provide additional control information that resides in the information words of the descriptor that was transmitted to the GbE switch. The three tables below show the information that may be passed along with which descriptor information word to put it in. See the Multicore Navigator User's Guide (SPRUGR9) as well as the descriptor structure definitions in the CPPI LLD (Low Level Driver) for more information on these bits.

Table 2-2. Descriptor Information Word 1 for Host Port 0 Switch Ingress Packets

Dest Tag -Lo Bits	Field	Description
7-0 (descriptor information word 1 bits 7-0)	TO_PORT	Directed packet to port. Setting these bits to a non-zero value indicates that the packet is a directed packet. Packets with the these bits set will bypass the ALE and send the packet directly to the port indicated. • 0 = Not directed • 1 = Send packet to GbE switch port 1 • 2 = Send packet to GbE switch port 2 • ... • N-1 = Send packet to GbE switch port N-1 • Others = Reserved

Table 2-3. Descriptor Information Word 2 for Host Port 0 Switch Ingress Packets

Protocol Specific Flags Bits	Field	Description
3 (descriptor information word 2 bit 19)	PASS_CRC	Signals whether or not CRC is passed with the packet. • 0 = CRC is not passed with the packet (CRC_TYPE below in bit 2 is a don't care). • 1 = CRC of type CRC_TYPE is passed with the packet.
2 (descriptor information word 2 bit 18)	CRC_TYPE	CRC Type • 0 = Ethernet CRC • 1 = Castagnoli CRC

Table 2-4. Extended Packet Info Word 1 for Host Port 0 Switch Ingress Packets

Extended Packet Info 1 Bits	Field	Description
31 (extended packet info word 1 bit 31)	TIMESTAMP_EN	Timestamp Enable. When set, this bit indicates that the packet will generate a time sync event on Ethernet egress (if the CPTS is configured properly) with the associated DOMAIN, MSG_TYPE, and SEQUENCE_ID.
27-20 (extended packet info word 1 bits 27-20)	DOMAIN	Time sync domain of the time sync event that is created by setting TIMESTAMP_EN to 1.
19-16 (extended packet info word 1 bits 19-16)	MSG_TYPE	Time sync message type of the time sync event that is created by setting TIMESTAMP_EN to 1.
15-0 (extended packet info word 1 bits 15-0)	SEQUENCE_ID	Time sync sequence ID of the time sync event that is create by setting TIMESTAMP_EN to 1.

Setting the PASS_CRC bit indicates that the CRC is passed with the packet data. The packet is a directed packet when any of the TO_PORT bits are non-zero. The packet will be sent to the port indicated. A packet may only be directed to a single port. For directed packets the destination lookup process in the ALE is skipped. However, in VLAN aware mode (VLAN_AWARE bit set to 1 in the CPSW_CONTROL register and ALE_VLAN_AWARE set to 1 in the ALE_CONTROL register) the lookup still takes place but only to determine if the packet should have the VLAN tag removed during egress (forced untagged egress).

Packets longer than the P0_RX_MAXLEN value are dropped. Packets shorter than 60-bytes are padded to 64-bytes (after adding pad and CRC) if P0_RX_PAD is set to 1 in the CPSW_CONTROL register and if PASS_CRC is cleared to 0 in the protocol specific section of the descriptor, otherwise they are dropped. This means that packets shorter than 64-bytes are dropped if the PASS_CRC info bit is set to 1 in the descriptor regardless of the value of P0_RX_PAD in the CPSW_CONTROL register (packets are padded only if they are short and do not have CRC).

2.3.1.2.1 Host Port 0 Receive Packet Priority Handling

Packets received on the host port have a received packet priority (0 to 7 with 7 being the highest priority). The received packet priority is determined as follows:

1. If the incoming packet is a VLAN/priority-tagged packet, then the packet's received packet priority is set to the VLAN priority.
2. Else if the packet is an IPv4 packet and the DSCP_IPV4_EN bit is set in the P0_CONTROL register, then the packet's received packet priority is set to a priority 0 to 7 determined by the 6-bit DSCP field. The DSCP field is mapped to a priority 0 to 7 through the P0_RX_DSCP_MAPx registers.
3. Else if the packet is an IPv6 packet and the DSCP_IPV6_EN bit is set in the P0_CONTROL register, then the packet's received packet priority is set to a priority 0 to 7 determined by the 6-bit DSCP field. The DSCP field is mapped to a priority 0 to 7 through the P0_RX_DSCP_MAPx registers.
4. Else the received packet priority is set to the priority of the port that it is entering the device through (Host port 0 in this case). Host port 0's priority is set in bits [15:13] of the P0_PORT_VLAN register.

The received packet priority (from above) is mapped through the receive port's associated packet priority to header packet priority mapping register (P0_RX_PRI_MAP) to obtain the header packet priority. The header packet priority is then used as the actual transmit packet priority if the VLAN information is to be sent on switch egress.

The host port also has a received packet thread. The received packet thread is determined exactly as the received packet priority, from above, except for untagged packets (number 4 above). For untagged packets, the received packet thread is the streaming packet interface thread that the packet was received on (instead of the port VLAN priority). The received packet thread is mapped at each destination FIFO through the header priority to switch priority mapping register (Pn_TX_PRI_MAP) to obtain the hardware switch priority. The hardware switch priority is then used to determine which destination FIFO queue the packet will be placed on while awaiting transmission. The received packet thread only determines which hardware switch priority the packet should be sent to, the egress VLAN rules are identical to packets that are received on Ethernet ports (as determined by the header packet priority).

2.3.1.2.2 CRC Handling (Host Port 0 Ingress)

Host port 0 ingress packets can be passed in with or without a CRC. Host port packets are not checked for CRC correctness on ingress, however they are checked for correctness on Ethernet port egress. This means that if a packet enters host port 0 with a CRC error, that packet will have the same CRC error when it is transmitted from the host port to an Ethernet port. If a host port ingress packet does not have the PASSED_CRC bit set in its descriptor then a CRC will be generated for the packet on host port ingress. If the PASSED_CRC bit is set, then the packet is received and forwarded unchanged. The CRC type is input in the descriptor CRC_TYPE bit and can be either Ethernet or Castagnoli and can be different from packet to packet. The P0_TX_CRC_TYPE bit in the CPSW_CONTROL register is for host port transmit (egress) only and is a configuration setting (cannot be changed from packet to packet).

2.3.1.2.3 Host Port 0 Receive Rate Limiting

Rate-limit mode is intended to allow some host port 0 receive (switch ingress) channels and some Ethernet port transmit (switch egress) priorities to be rate-limited. Non rate-limited traffic (bulk traffic) is allowed on non rate-limited channels and FIFO priorities. The bulk traffic does not impact the rate-limited traffic. Rate-limited traffic must be configured to be sent to rate-limited queues (via packet priority handling). The allocated rates for rate-limited traffic must not be oversubscribed. For example, if port 1 is sending 15% rate-limited traffic to port 2 priority 3, and port 0 is also sending 10% rate-limited traffic to port 2 priority 3, then the port 2 priority 3 egress rate must be configured to be 25% plus a percent or two for margin. The switch must be configured to allow some percentage of non rate-limited traffic. Non rate-limited traffic must be configured to be sent to non rate-limited queues. No packets originating from the host should be dropped, but non rate-limited traffic received on an Ethernet port can be dropped.

Port 0 receive operations can be configured to rate limit the host port ingress data for each receive thread (priority). Rate limiting is enabled for a thread when the P0_RX_RLIM[7:0] bit associated with that thread is set in the P0_PRI_CTL Register. Bulk traffic does not impact rate-limited traffic. No bulk thread will be enabled to send unless there are TX_HOST_BLKS_REM (from the Pn_PRI_CTL register) number of unused blocks remaining in the port n transmit FIFOs. The “blocks remaining check” ensures that bulk traffic from the host will not block rate-limited traffic from the host. Rate-limited channels must be the highest priority channels. For example, if two rate limited channels are required, then P0_RX_RLIM[7:0] should be set to 11000000 with the MSB corresponding to channel 7. When any channels are configured to be rate-limited, the priority type must be fixed for receive (P0_RX_PTYPE cleared to 0 in the P0_PRI_CTL register). Round-robin priority type is not allowed when rate-limiting. Each of the eight receive priorities has two associated registers to control the rate at which the priority is allowed to send data (P0_PRIx_SEND and P0_PRIx_IDLE) when the channel is rate limiting. Each priority has a send count (P0_PRIx_SEND) and an idle count (P0_PRIx_IDLE). In general, smaller values for the idle and send values are better than larger values. The transfer rate includes the inter-packet gap (12 bytes) and the preamble (8 bytes). The rate in Mbits/second that each priority is allowed to send is controlled by the below equation:

Priority Transfer rate in Mbit/s = ((P0_PRIx_IDLE/(P0_PRIx_IDLE + P0_PRIx_SEND)) * frequency * 256 (1)

Where frequency = VBUSP_GCLK frequency (350 for 350Mhz) and x = priority from 7 down to 0.

2.3.1.2.4 Host Port 0 Receive Flow Control

The host port FIFO has flow control for receive operations (packet ingress from the host) that is always enabled and is initiated when triggered. Host port receive flow control is accomplished through pushback. The pushback causes the host port logical receive FIFO to fill up with packet data. Once the receive FIFO is full the flow control occurs by de-asserting the ready signal on the receive streaming interface. This stops packets from entering the host port until there is space available in the receive FIFO.

2.3.2 Media Access Controller Submodule Architecture

This section describes the architecture of the media-access-controller (MAC) submodule. The MAC submodule is IEEE 802.3 compliant and supports 10/100/1000 megabit per second (Mbps) modes of operation. The MAC module provides an interface between the GbE switch and the SGMII modules. For transmit operations, the MAC module converts between data signals used by the GbE switch and GMII signals used by the SGMII modules. For receive operations, the MAC module converts between GMII signals from the SGMII module to the signals used by the GbE switch. Transmit and receive operations are described in more detail in subsequent sections.

In addition to translating between the SGMII modules and the GbE switch, the MAC module is responsible for operations related to IEEE 802.3 Ethernet frames. For all packets, the MAC module adds or removes the preamble, start of frame delimiter, and interpacket gap to a packet. The MAC module verifies and optionally generates CRC checksums.

2.3.2.1 Data Receive Operations

This section describes the data-receive operations of the MAC module.

2.3.2.1.1 Receive Control

The MAC module is responsible for interpreting GMII data received from the SGMII module. Interpretation of GMII data involves the following operations:

- Detection and removal of the preamble
- Detection and removal of the start-of-frame delimiter
- Extraction of the address
- Extraction of the frame length
- Data handling
- Error checking and reporting
- Cyclic redundancy checking (CRC)
- Statistics signal generation

All statistics signal generation is reported to the proper statistics module in the GbE switch.

2.3.2.1.2 Receive Interframe Interval

The 802.3 required interpacket gap (IPG) is 24 GMII clocks (96 bit times) for 10/100 Mbps modes, and 12 GMII clocks (96 bit times) for 1000 Mbps mode. However, the MAC module can tolerate a reduced IPG (2 GMII clocks in 10/100 mode and 5 GMII clocks in 1000 mode) with a correct preamble and start of frame delimiter.

This interval between frames must include (in the following order):

1. An interpacket gap (IPG)
2. A seven-octet preamble (all octets 0x55)
3. A one-octet start of frame delimiter (0x5D)

2.3.2.1.3 Ethernet Port Receive Packet Priority Handling

Packets received on Ethernet ports have a received packet priority: 0 to 7 with 7 being the highest priority. The received packet priority is determined as follows:

1. If the incoming packet is a VLAN/priority tagged packet then the packet's received packet priority is set to the VLAN priority.
2. Else if the packet is an IPv4 packet and the DSCP_IPV4_EN bit is set in the Pn_CONTROL register, the packet's received packet priority is set to a priority 0 to 7 determined by the 6-bit DSCP field. The DSCP field is mapped to a priority 0 to 7 through the Pn_RX_DSCP_MAPx registers.
3. Else if the packet is an IPv6 packet and the DSCP_IPV6_EN bit is set in the Pn_CONTROL register, the packet's received packet priority is set to a priority 0 to 7 determined by the 6-bit DSCP field. The DSCP field is mapped to a priority 0 to 7 through the Pn_RX_DSCP_MAPx registers.
4. Else the received packet priority is set to the priority of the port that it is entering the device through. Each port's priority is set in bits [15:13] of the Pn_PORT_VLAN register.

The received packet priority (from above) is mapped through the receive port's associated packet priority to header-packet priority mapping register (Pn_RX_PRI_MAP) to obtain the header-packet priority. The header-packet priority is then used as the actual transmit packet priority if the VLAN information is to be sent on switch egress.

The header-packet priority is mapped at each destination FIFO through the header priority to switch priority mapping register (Pn_TX_PRI_MAP) to obtain the hardware switch priority. The hardware switch priority is then used to determine which destination FIFO queue the packet will be placed on while awaiting transmission.

2.3.2.1.4 CRC Handling (Ethernet Port Ingress)

All Ethernet ports check the ingress packet CRC in all modes/speeds. The receive port can check either Ethernet CRC or Castagnoli CRC as determined by the CRC_TYPE bit in the Pn_MAC_CTL register.

2.3.2.1.5 Receive Flow Control

This section describes the receive flow control functionality. When under heavy load, the MAC module can limit further frame reception through receive frame flow control. Receive flow control is enabled by setting the RX_FLOW_EN bit in the Pn_MAC_CTL register. When enabled, flow control events are triggered by the receive FIFO in the GbE switch module. When receive flow control is enabled, and a flow control event is triggered, receive flow control is initiated. When in half-duplex mode (FULLDUPLEX bit cleared to 0 in the Pn_MAC_CTL register) receive flow control is collision based. While in full duplex mode (FULLDUPLEX bit set to 1 in the Pn_MAC_CTL register) flow control issues either 802.3X pause frames or Priority Based Flow Control (PFC) pause frames. The type of pause frames sent in full duplex mode is determined by the RX_FLOW_PRI bits in the Pn_PRI_CTL register. In all cases, receive flow control prevents frame reception by issuing the flow control appropriate for the current mode of operation.

2.3.2.1.5.1 Collision Based Receive Flow Control

Collision-based receive flow control provides a means of preventing frame reception when the port is operating in half-duplex mode (the FULLDUPLEX bit is cleared in the Pn_MAC_CTL register). When receive flow control is enabled and triggered, the port generates collisions for received frames. The jam sequence transmitted is the twelve-byte sequence C3.C3.C3.C3.C3.C3.C3.C3.C3.C3.C3.C3 (hex). The jam sequence begins no later than the moment the source address begins to be received. Note that these forced collisions are not limited to a maximum of 16 consecutive collisions and are independent of the normal back-off algorithm. Receive flow control does not depend on the value of the incoming frame destination address. A collision is generated for any incoming packet, regardless of the destination address.

2.3.2.1.5.2 IEEE 802.3X Based Receive Flow Control

IEEE 802.3x-based receive flow control provides a means of preventing frame reception when the port is operating in full-duplex mode (the FULLDUPLEX bit is set in Pn_MAC_CTL register). When receive flow control is enabled and triggered, the port transmits a pause frame to request that the sending station stop transmitting for the period indicated within the transmitted pause frame. If all ports have receive flow control enabled, then each Pn_TX_BLKS_PRI register should be written with all zeros in order to maximize FIFO memory usage.

The MAC module transmits a pause frame to the reserved multicast address at the first available opportunity. If the MAC module is idle, a pause frame is transmitted immediately, otherwise the pause frame is sent following the completion of the frame currently being transmitted. When issuing a pause frame, the frame contains 0xFFFF, which is the maximum possible pause time value. The MAC module counts the receive pause frame time, decrementing 0xFF00 down to 0, and retransmits an outgoing pause frame if the count reaches 0. When the flow control request is removed, the MAC module transmits a pause frame with a zero pause time to cancel the pause request.

NOTE: Transmitted pause frames are only a request to the other end station to stop transmitting. Frames that are received during the pause interval are received normally (provided the receive FIFO is not full). If the receive FIFO is full the FIFO will overrun and STATn_RX_TOP_FIFO_DROP will increment.

Pause frames are transmitted if enabled and triggered regardless of whether the port is observing the pause time period from an incoming pause frame.

The MAC module transmits pause frames as described below:

- The 48-bit reserved multicast destination address 01.80.C2.00.00.01
- The 48-bit source address found in the Pn_PAUSE_SA_H and Pn_PAUSE_SA_L registers
- The 16-bit length/type field containing the value 88.08
- The 16-bit pause opcode equal to 00.01
- The 16-bit pause time value FF.FF. A pause-quantum is 512 bit-times. Pause frames sent to cancel a pause request will have a pause time value of 00.00.
- Zero padding to 64-byte data length (The MAC module will transmit only 64-byte pause frames)
- The 32-bit frame-check sequence (CRC word)

All quantities above are hexadecimal and are transmitted most-significant byte first. The least-significant bit is transferred first in each byte.

If RX_FLOW_EN is cleared to 0 while the pause time is non-0, the pause time will be cleared to 0, and a 0-count pause frame will be sent.

Receive flow control is triggered (when enabled), when a packet at the top of the Receive FIFO cannot be sent to all destination ports due to a lack of FIFO memory space at one or more destination ports. The flow control packet runout is then contained in the receive FIFO. The flow control trigger is cleared, and pause off sent, when all packets in the receive FIFO have been transferred to their destination ports.

2.3.2.1.5.3 802.1Qbb Receive Priority Based Flow Control (PFC)

IEEE 802.1Qbb based receive flow control provides a means of preventing frame reception when the port is operating in full-duplex mode (FULLDUPLEX must be set to 1 in the Pn_MAC_CTL register). When receive PFC flow control is enabled and triggered for a priority, the port will transmit a PFC pause frame to request that the sending station stop transmitting on that priority (and perhaps others) for the period indicated within the transmitted pause frame (FF.FF pause time). When the triggering condition is removed, or when PFC flow control is disabled, the port will transmit a pause frame to cancel the pause request (00.00 pause time). Priority-based pause frames can have one to eight priorities enabled as determined by the priority enable vector in the pause frame. Pause frames can give some priorities pause on and others pause off in the same frame.

An enabled priority will have either a pause on value (FF.FF) or a pause off value (00.00). Priorities with a zero enable bit in the pause frame priority enable vector are unchanged by the pause frame on the sending station side. The RX_FLOW_PRI bits in the Pn_PRI_CTL register indicate which port receive priorities are enabled for PFC. The priority enable vector in the pause frame only refers to the priorities that have a valid pause on or pause off sent in the sent pause frame.

The MAC module will transmit a pause frame to the reserved multicast address at the first available opportunity (immediately if currently idle, or following the completion of the frame currently being transmitted). The pause frame will contain the maximum possible value for the pause time (FF.FF) on each priority to be paused along with a set priority enable vector bit. The MAC will count the receive pause frame time (decrements FF.00 down to zero) and retransmit an outgoing pause frame if the count reaches zero. When the flow control trigger is removed for a specific priority, the MAC will transmit a pause frame with a set priority enable vector bit and a zero pause time on that priority to cancel the pause request.

NOTE: Transmitted pause frames are only a request to the other end station to stop transmitting. Frames that are received during the pause interval are received normally (provided the receive FIFO is not full). If the receive FIFO is full the FIFO will overrun and STATn_RX_TOP_FIFO_DROP will increment.

Pause frames will be transmitted if enabled and triggered regardless of whether or not the port is observing the pause time period from an incoming pause frame on the priority to be paused or not.

The MAC module transmits pause frames as described below:

- The 48-bit reserved multicast destination address 01.80.C2.00.00.01
- The 48-bit source address found in the Pn_PAUSE_SA_H and Pn_PAUSE_SA_L registers
- The 16-bit length/type field containing the value 88.08
- The 16-bit pause opcode equal to 01.01
- The 16-bit priority enable vector. The lower 8-bits are used for priorities 7 down to 0.
- The 16-bit pause time value for each priority. The pause on value is FF.FF and the pause off value is 00.00. A pause-quantum is 512 bit-times
- Zero padding to 64-byte data length (The MAC module will transmit only 64 byte pause frames)
- The 32-bit frame-check sequence (CRC word)

All quantities above are hexadecimal and are transmitted most-significant byte first. The least-significant bit is transferred first in each byte.

If RX_FLOW_EN is cleared to zero while the pause time is nonzero, then the pause time will be clear to zero and a zero count pause frame will be sent. For any priority that has flow control enabled then the associated priority in the Pn_TX_BLKS_PRI register should be written with zero.

2.3.2.1.5.4 Priority Based Flow Control (PFC) Trigger Rules

There are five rules that can each set and clear a PFC trigger condition for each enabled priority. The five rules are listed below and each discussed in a subsequent section:

- Destination Based Rule
- Sum of Outflows Rule
- Sum of Blocks Per Port Rule
- Sum of Blocks Total Rule
- Top of Receive FIFO Rule

Ethernet ports issue transmit PFC pause frames when any priority is triggered for any rule. Port 0 issues flow control on the associated receive thread when any priority is triggered for any rule. There are no pause frames sent on port 0 transmit (no port 0 outflow). Receive priority remapping is taken into account for all rules on all ports. Transmit priority remapping is taken into account for the sum of outflows rule, the sum of blocks per port rule, and the destination based rule. Transmit priority remapping is not taken into account for the sum of blocks total rule or the top of receive FIFO rule. The intent of PFC is to shutdown lower priorities as traffic congestion increases so that the higher priorities can continue to operate. Systems with only 1518 byte packets may only need to configure the destination based rule. Systems with jumbo packets on lower priorities may need to configure the other more aggressive rules on those priorities in order to preclude increasing high priority packet latency.

2.3.2.1.5.5 Destination Based Rule

The destination based rule is the primary rule for PFC and should be configured when PFC is enabled. The rule is evaluated for PFC trigger when the destination ports are determined on address lookup at packet reception (bottom of receive FIFO). The conditions of all packet destination port transmit FIFOs at packet reception determine whether or not one or more receive port priorities will be triggered. Each packet destination port is evaluated for each priority and the results are combined to produce the priority flow control trigger(s) on the receive port.

A priority trigger is cleared at any time the clear condition is satisfied for that priority on all destination port FIFOs (all transmit FIFOs that set the trigger). The intent of the rule is to progressively trigger receive PFC with decreasing priority as the FIFO allocated blocks (TX_BLK_CNT bits in the Pn_BLK_CNT register) increases, and have the effect of priority outflow increase with decreasing priority. The add amount for outflow is zero if the outflow is not set. The add amount for outlflow the value of ADD_VAL_X in the Pn_TX_DEST_OUTFLOW_ADDVAL_L and Pn_TX_DEST_OUTFLOW_ADDVAL_H registers if the outflow is set for a particular priority.

A PFC priority is triggered by conditions in ***any*** destination transmit FIFO by the below equation at ***packet reception***. Priority X PFC trigger set if:

((addvalX[4:0] & {5{tx_d_trig_setX}}) + tx_blk_cnt[4:0]) >= tx_d_thresh_setX[4:0] (2)

A PFC priority is cleared by conditions in ***all*** destination transmit FIFOs by the below equation ***at any time*** after the set has occurred. Priority X PFC trigger cleared if:

((addvalX[4:0] & {5{tx_d_trig_setX}}) + tx_blk_cnt[4:0]) <= tx_d_thresh_clrX[4:0] (3)

Where:

- x is the priority from 0 to 7
- addvalX is from Pn_TX_DEST_OUTFLOW_ADDVAL_(L/H) and has a maximum value of 11 decimal
- tx_d_trig_setX is set when transmit flow control (outflow) is triggered on the destination tx FIFO priority (by receiving a pause frame with the associated priority paused).
- tx_blk_cnt is the total number of blocks allocated on all priorities in the destination transmit FIFO (0 to 20).
- tx_d_thresh_setX is from Pn_TX_DEST_THRESH_SET_(L/H)
- tx_d_thresh_clrX is from Pn_TX_DEST_THRESH_CLR_(L/H)
- tx_d_thresh_setX must be greater than tx_d_thresh_clrX

2.3.2.1.5.6 Sum of Outflows Rule

The Sum of Outflows rule is a global control that sets and clears PFC triggers on a receive port due to conditions in all other Ethernet port transmit FIFOs regardless of receive traffic. An outflow is set for a transmit FIFO priority when a PFC pause frame is received on the port with a non-zero pause quanta for that priority indicating that the port should not transmit on that priority. An outflow is clear for a priority when the transmit pause condition is removed either due to receiving a pause frame with a zero pause quanta or by the pause timer expiring for the priority. Port 0 does not have transmit flow control.

The sum of outflows rule is intended to be used in some systems to pass along outflow on lower priorities with larger packet sizes. Triggering PFC on priorities due to this rule also prevents packet transmission from Ethernet ports to the host for the duration of the pause time on the triggered priorities. When configured to trigger due to this rule, pause frames will be sent on Ethernet ports regardless of receive traffic.

A PFC priority is triggered by conditions in ***all other Ethernet*** transmit FIFOs by the below equation at any time. Priority X PFC trigger set if:

sum of all other Ethernet port priX_outflows >= tx_g_oflow_thresh_setX[4:0] (4)

A PFC priority is cleared by conditions in all other Ethernet transmit FIFOs by the below equation ***at any time***. Priority X PFC trigger cleared if:

sum of all other Ethernet port priX_outflows <= tx_g_oflow_thresh_clrX[4:0] (5)

Where:

- X is the priority
- tx_g_oflow_thresh_setX is from CPSW_TX_OUTFLOW_THRESH_SET
- tx_g_oflow_thresh_clrX is from CPSW_TX_OUTFLOW_THRESH_CLR
- tx_g_oflow_thresh_setX must be greater than tx_g_oflow_thresh_clrX

2.3.2.1.5.7 Sum of Blocks Per Port Rule

The Sum of Blocks Per Port rule is an aggressive global control that sets and clears PFC triggers on receive ports due to conditions in any other port transmit FIFO regardless of receive traffic. When any transmit FIFO has a trigger condition set, all other receive ports will trigger PFC for that priority. This rule is intended to be configured in systems with high traffic rate jumbo packets on lower priorities.

A PFC priority is triggered by conditions in ***any other*** transmit FIFOs by the below equation ***at any time***. Priority X PFC trigger set if:

sum of all Tx FIFO blocks allocated on the port >= tx_g_obuf_thresh_setX[4:0] (6)

A PFC priority is cleared when conditions in ***all other Ethernet*** transmit FIFOs satisfy the below equation ***at any time***. Priority X PFC trigger cleared if:

sum of all tx FIFO blocks allocated on the port <= thresh_clrX[4:0] (7)

Where:

- X is the priority
- thresh_setX is from Pn_TX_BUFFER_THRESH_SET_(L/H)
- thresh_clrX is from Pn_TX_BUFFER_THRESH_CLR_(L/H)
- thresh_setX must be greater than thresh_clrX for each priority.

2.3.2.1.5.8 Sum of Blocks Total Rule

The Sum of Blocks Total rule is an extremely aggressive global control that sets and clears PFC triggers on receive ports due to conditions in all transmit FIFOs regardless of receive traffic. When any priority has a trigger condition set, all receive ports will trigger PFC for that priority. The intent of this rule is to shutdown lower priorities with jumbo packets as the total switch congestion increases. ***Switches with N>=6 should not use this rule***.

A PFC priority is triggered by conditions in ***all*** transmit FIFO by the below equation ***at any time***. Priority X PFC trigger set if:

sum of all tx FIFO blocks allocated in all ports >= tx_g_obuf_thresh_setX[4:0] (8)

A PFC priority is cleared when conditions in ***all*** transmit FIFO's satisfy the below equation ***at any time***. Priority X PFC trigger cleared if:

sum of all tx FIFO blocks allocated in all ports <= tx_g_obuf_thresh_clrX[4:0] (9)

Where:

- X is the priority
- tx_g_obuf_thresh_setX is from CPSW_TX_BUFFER_THRESH_SET_(L/H)
- tx_g_obuf_thresh_clrX is from CPSW_TX_BUFFER_THRESH_CLR_(L/H)
- tx_g_obuf_thresh_setX must be greater than tx_g_obuf_thresh_clrX for each priority

2.3.2.1.5.9 Top of Receive FIFO Rule

The Top of Receive FIFO Rule sets PFC triggers on the associated receive port for all priorities. This rule requires no configuration and is enabled when PFC flow control is enabled. The Top of Receive FIFO rule triggers when a received packet cannot be transferred to an intended destination port due to insufficient space in that destination port transmit FIFO. The receive FIFO exists to accept flow control runout (especially for 802.3 flow control). The trigger condition for this rule is cleared when the receive FIFO is emptied after runout. Preferable PFC configurations preclude this rule from triggering. If a lower priority packet triggers this rule then higher priority packets could be in the runout after the lower priority packet(s), which would increase the switch latency of the higher priority packets.

This rule ensures that there is no packet loss on any priority in any configuration. However, PFC configuration should ensure that this rule is triggered only by high priority packets or preferably not at all. The TORF bit in the Pn_MAC_STATUS register indicates that this rule has triggered. The TORF_PRI field in the Pn_MAC_STATUS register indicates the lowest priority that has triggered this rule since the last clearing of the status register fields. More aggressive shutdown of lower priorities in the other rules is preferable to having this rule trigger.

2.3.2.2 Data Transmission

This section describes transmit data operations for the MAC module. The MAC module accepts data from the GbE switch, converts the data to GMII format, and transmits the data to the SGMII module. Data transmission is synchronized to the transmit clock rate.

2.3.2.2.1 Transmit Control

This section describes transmit control operations for the MAC module. If a collision is detected on a transmit packet in half-duplex mode, the MAC module outputs a jam sequence. If the collision was late (after the first 64 bytes have been transmitted) the collision is ignored. If the collision is not late, the controller will back off before retrying the frame transmission. When operating in full duplex mode, the carrier sense (CRS) and collision sensing modes are disabled.

2.3.2.2.2 Transmit VLAN Processing

This section covers transmit processing when in VLAN-aware mode. The GbE switch is in VLAN-aware mode when the VLAN_AWARE bit is set in the CPSW_CONTROL register and the ALE_VLAN_AWARE bit is set in the ALE_CONTROL register. While in VLAN-aware mode, VLAN is added, removed, or replaced during Ethernet port transmit according to the same rules as the streaming packet interface transmit (egress) output packet VLAN process. See Section 2.3.1.1.2.

Transmit packets are not modified when VLAN_AWARE is cleared to 0 in the CPSW_CONTROL register.

2.3.2.2.3 CRC Handling (Ethernet Port Egress)

Ethernet ports transmit each egress packet with the CRC selected by the CRC_TYPE bit in the Pn_MAC_CRL register, regardless of the type of CRC that the packet had on ingress to the switch. At the egress port after passing through the switch, the packet CRC is checked for correctness and if the CRC is correct then the packet is output with the generated selected output CRC. If the packet CRC is incorrect, due either to a bit flip in a memory or an error CRC passed in on host ingress, then the generated egress CRC type is used with at least a single byte of the CRC inverted to indicate the error. If the packet length including CRC is divisible by 4, then all four CRC bytes will be inverted on error. If there are three bytes remainder after dividing the packet length by 4 then three bytes will be inverted (and so on down to one byte remainder).

2.3.2.2.4 Adaptive Performance Optimization (APO)

This section describes adaptive performance optimization (APO) implemented in the MAC module. The Ethernet MAC port incorporates APO logic that may be enabled by setting the TX_PACE bit in the Pn_MAC_CTL register. When the TX_PACE bit is set, transmission pacing to enhance performance is enabled. Adaptive performance pacing introduces delays into the normal transmission of frames, delaying transmission attempts between stations. By introducing delays, the probability of collisions will be reduced during heavy traffic (as indicated by frame deferrals and collisions), thereby increasing the chance of successful transmission.

When a frame is deferred, suffers a single collision, multiple collisions, or excessive collisions, the pacing counter is loaded with an initial value of 31. When a frame is transmitted successfully (without experiencing a deferral, single collision, multiple collision, or excessive collision) the pacing counter is decremented by 1, down to 0.

With pacing enabled, a new frame is permitted to immediately (after one IPG) attempt transmission only if the pacing counter is 0. If the pacing counter is non-0, the frame is delayed by the pacing delay, which is equivalent to approximately four Interpacket gap delays. APO affects only the IPG preceding the first attempt at transmitting a frame. It does not affect the back-off algorithm for retransmitted frames.

2.3.2.2.5 Interpacket Gap Enforcement

This section describes the enforcement of interpacket gap for the MAC module. The measurement reference for the IPG of 96 bit times is changed depending on frame traffic conditions. If a frame is successfully transmitted without collision, and the MCRS signal is deasserted within approximately 48 bit times of the MTXEN signal being deasserted, 96 bit times is measured from MTXEN. If the frame suffered a collision, or if the MCRS signal is not de-asserted until more than approximately 48 bit times after MTXEN is deasserted, 96 bit times (approximately, but not less) is measured from MCRS.

The transmit IPG can be shortened by eight bit times when enabled and triggered. The TX_SHORT_GAP_EN bit in the Pn_MAC_CTL register enables the TX_SHORT_GAP input to determine whether the transmit IPG is shorted by eight bit times.

2.3.2.2.6 Back Off

The MAC module implements the 802.3 binary exponential back-off algorithm for half-duplex based collisions.

2.3.2.2.7 Programmable Transmit Interpacket Gap

The transmit interpacket gap (IPG) is programmable through the Pn_MAC_TX_GAP register. The default value is decimal 12. The transmit IPG may be increased to the maximum value of 0x1ff. Increasing the IPG is not compatible with transmit pacing. The short gap feature will override the increased gap value, so the short gap feature may not be compatible with an increased IPG.

2.3.2.2.8 Short Gap

The Ethernet port transmit inter-packet gap (IPG) may be shortened by eight bit times when enabled and triggered. The TX_SHORT_GAP_EN bit each Pn_MAC_CTL register enables the gap to be shortened when triggered. The condition is triggered when the port's associated transmit packet FIFO has a user defined number of FIFO blocks used. The associated transmit FIFO blocks used value determines if the gap is shortened, and so on. The CPSW_GAP_THRESH register value determines the short gap threshold. If the blocks used is greater than or equal to the GAP_THRESH value in the CPSW_GAP_THRESH register then short gap is triggered.

2.3.2.2.9 Ethernet Port Transmit Rate Limiting

Rate-limit mode is intended to allow some host port 0 receive (switch ingress) channels and some Ethernet port transmit (switch egress) priorities to be rate-limited. Non-rate-limited traffic (bulk traffic) is allowed on non-rate-limited channels and FIFO priorities. The bulk traffic does not impact the rate-limited traffic. Rate-limited traffic must be configured to be sent to rate-limited queues (via packet priority handling). The allocated rates for rate-limited traffic must not be oversubscribed. For example, if port 1 is sending 15% rate-limited traffic to port 2 priority 3, and port 0 is also sending 10% rate-limited traffic to port 2 priority 3, then the port 2 priority 3 egress rate must be configured to be 25% plus a percent or two for margin. The switch must be configured to allow some percentage of non rate-limited traffic. Non rate-limited traffic must be configured to be sent to non rate-limited queues. No packets originating from the host should be dropped, but non rate-limited traffic received on an Ethernet port can be dropped.

Ethernet port transmit operations can be configured to rate limit egress data for each egress priority. Rate limiting is enabled for a priority when the TX_RLIM[7:0] bit associated with that priority is set in the Pn_PRI_CTL register. Bulk traffic does not impact the overall rates at which rate-limited priorities are sent. Bulk priorities are enabled to send only during times that rate-limited priorities are not allowed to send due to rate limits being reached. Rate-limited channels must be the highest priority channels. For example, if two rate-limited channels are required then TX_RLIM[7:0] should be set to 11000000 with the MSB corresponding to channel 7.

When any channels are configured to be rate-limiting, the priority type must be fixed for receive. Round-robin priority type is not allowed when rate-limiting. Each of the eight receive priorities has two associated registers to control the rate at which the priority is allowed to send data (Pn_PRIx_SEND and Pn_PRIx_IDLE where n is the port number and x is the priority 7 down to 0) when the channel is rate-limiting. Each priority has a send count (Pn_PRIx_SEND) and an idle count (Pn_PRIx_IDLE). In general, smaller values for the idle and send values are better than bigger values. The transfer rate includes the inter-packet gap (12 bytes) and the preamble (8 bytes). The rate in Mbits/second that each priority is allowed to send is controlled by the below equation:

Priority Transfer rate in Mbit/s = ((Pn_PRIx_IDLE/(Pn_PRIx_IDLE + Pn_PRIx_SEND)) * frequency * 256 (10)

Where

- frequency = VBUSP_GCLK frequency (350 for 350 Mhz)
- n = port number
- x = priority from 7 down to 0

2.3.2.2.10 Transmit Flow Control

This section describes the transmit flow control implemented in the MAC module. When enabled, incoming pause frames or priority flow control frames are acted upon to prevent the MAC from transmitting any further frames. Two types of transmit flow control are supported in the MAC module: IEEE 802.3X based transmit flow control and 802.1Qbb priority based transmit flow control. Each type is discussed in its own section below.

2.3.2.2.10.1 IEEE 802.3X Based Transmit Flow Control

When IEEE 802.3X-based transmit flow control is enabled, incoming pause frames are acted upon to prevent the MAC module from transmitting any further frames. Incoming pause frames are acted upon only when the FULLDUPLEX and TX_FLOW_EN bits are set in the Pn_MAC_CTL register. Pause frames are not acted upon in half-duplex mode. Pause frame action will be taken if enabled, but normally the frame will be filtered and not transferred to memory. MAC control frames will be transferred to memory if the RX_CMF_EN (copy MAC Frames) bit in the Pn_MAC_CTL register is set. The TX_FLOW_EN and FULLDUPLEX bits effect whether or not MAC control frames are acted upon, but they have no effect upon whether or not MAC control frames are transferred to memory or filtered.

Pause frames are a subset of MAC control frames with an opcode field=0x0001. Incoming pause frames will be acted upon by the port only if all the following conditions are met:

- TX_FLOW_EN is set in the Pn_MAC_CTL register
- The frame's length is 64 to RX_MAXLEN bytes inclusive
- The frame contains no CRC error or align/code errors

The pause-time value from valid frames is extracted from the two bytes following the opcode. The pause time will be loaded into the port's transmit pause timer and the transmit pause time period will begin.

If a valid pause frame is received during the transmit pause time period of a previous transmit pause frame then:

- If the destination address is not equal to the reserved multicast address or any enabled or disabled unicast address, then the transmit pause timer will immediately expire, or
- If the new pause time value is 0, then the transmit pause timer will immediately expire, else
- The port transmit pause timer will immediately be set to the new pause frame pause time value. (Any remaining pause time from the previous pause frame will be discarded.)

If the TX_FLOW_EN field in the Pn_MAC_CTL register is cleared, then the pause-timer will immediately expire.

The port will not start the transmission of a new data frame any sooner than 512-bit times after a pause frame with a non-zero pause time has finished being received (MRXDV going inactive). No transmission will begin until the pause timer has expired (the port may transmit pause frames in order to initiate outgoing flow control). Any frame already in transmission when a pause frame is received will be completed and unaffected.

Incoming pause frames consist of:

- A 48-bit destination address equal to:
  - The reserved multicast destination address 01.80.C2.00.00.01, or
  - The 48-bit MAC source address found in the Pn_PAUSE_SA_H and Pn_PAUSE_SA_L registers
- The 48-bit source address of the transmitting device
- The 16-bit length/type field containing the value 88.08
- The 16-bit pause opcode equal to 00.01
- The 16-bit pause_time. A pause-quantum is 512 bit-times
- Padding to 64-byte data length
- The 32-bit frame-check sequence (CRC word)

All quantities above are hexadecimal and are transmitted most-significant byte first. The least-significant bit is transferred first in each byte.

The padding is required to make up the frame to a minimum of 64 bytes. The standard allows pause frames longer than 64 bytes to be discarded or interpreted as valid pause frames. The MAC module will recognize any pause frame between 64 bytes and RX_MAXLEN bytes in length.

2.3.2.2.10.2 802.1Qbb Priority Based Transmit Flow Control (PFC)

Incoming PFC pause frames are acted upon, when enabled, to prevent the Mac from transmitting any further frames. Incoming pause frames are only acted upon when the FULLDUPLEX and TX_FLOW_EN bits in the Pn_MAC_CTL register are set and the associated TX_FLOW_PRI[7:0] bits are set in Pn_PRI_CTL register. Pause frames are not acted upon in half-duplex mode. Pause frame action will be taken if enabled, but normally the frame will be filtered and not transferred to memory. MAC control frames are transferred to memory if the RX_CMF_EN (Copy MAC Frames) bit in the Pn_MAC_CTL register is set. The TX_FLOW_EN and FULLDUPLEX bits effect whether or not MAC control frames are acted upon, but they have no effect upon whether or not MAC control frames are transferred to memory or filtered.

PFC Pause frames are a subset of MAC Control Frames with an opcode field=0x0101. Incoming PFC pause frames will be acted upon by the port only if all the following conditions are met:

- TX_FLOW_EN is set in the Pn_MAC_CTL register
- TX_FLOW_PRI[7:0] bits are set in Pn_PRI_CTL
- The frame's length is 64 to RX_MAXLEN bytes inclusive (from the Pn_RX_MAXLEN register)
- The frame contains no CRC error or align/code errors.

The PFC pause time value from valid frames will be extracted from the priority pause times in the pause frame that are associated with the pause frame priority enable bits. The pause time for each enabled priority will be loaded into the port's priority transmit pause timer and the transmit pause time period will begin.

If a valid pause frame is received during the transmit pause time period of a previous transmit pause frame:

- If the destination address is not equal to the reserved multicast address or any enabled or disabled unicast address, then the transmit pause timer will immediately expire, or
- If the new pause time value is zero then the transmit pause timer will immediately expire, else
- The port transmit pause timer will immediately be set to the new pause frame pause time value. (Any remaining pause time from the previous pause frame will be discarded).

If TX_FLOW_EN in Pn_MAC_CTL is cleared, then the pause-timer immediately expires.

The port will not start the transmission of a new data frame any sooner than 512-bit times after a pause frame with a non-zero pause time has finished being received (MRXDV going inactive). No transmission will begin until the pause timer has expired (the port may transmit pause frames in order to initiate outgoing flow control). Any frame already in transmission when a pause frame is received will be completed and unaffected.

Incoming PFC pause frames consist of the below:

- A 48-bit destination address equal to:
  - The reserved multicast destination address 01.80.C2.00.00.01, or
  - The 48-bit MAC source address found in the Pn_PAUSE_SA_H and Pn_PAUSE_SA_L registers
- The 48-bit source address of the transmitting device.
- The 16-bit length/type field containing the value 88.08
- The 16-bit pause opcode equal to 01.01
- The 16-bit priority enable vector. The lower 8 bits are used for priorities 7 down to 0.
- A 16-bit pause time value for each priority. The pause on value is FF.FF and the pause off value is 00.00. A pause-quantum is 512 bit-times.
- Padding to at least 64-byte packet length.
- The 32-bit frame-check sequence (CRC word).

All quantities above are hexadecimal and are transmitted most-significant byte first. The least-significant bit is transferred first in each byte.

The padding is required to make up the frame to a minimum of 64 bytes. The standard allows pause frames longer than 64 bytes to be discarded or interpreted as valid pause frames. The MAC will recognize any pause frame between 64 bytes and RX_MAXLEN bytes in length.

2.3.2.2.11 Speed, Duplex Mode, and Pause Frame Support Negotiation

The MAC module can operate in half duplex or full duplex in 10/100 Mbps modes, and can operate only in full duplex in 1000 Mbps mode. Pause frame support is included in 10/100/1000 Mbps modes as configured by the host.

2.3.2.2.12 Frame Classification

Received frames are proper (good) frames if they are between 64 and Pn_RX_MAXLEN in length (inclusive) and contain no errors (code/align/CRC).

Received frames are long frames if their frame count exceeds the value in the Pn_RX_MAXLEN register. The default Pn_RX_MAXLEN register value is 1518 (decimal). Long received frames are either oversized or jabber frames. Long frames with no errors are oversized frames. Long frames with CRC, code, or alignment errors are jabber frames.

Received frames are short frames if their frame count is less than 64 bytes. Short frames that contain no errors are runt frames. Short frames with CRC, code, or alignment errors are fragment frames. If the RX_CSF_EN bit in the Pn_MAC_CONTROL register is set, undersized frames from 33 to 63 bytes will be forwarded only to the host on a best effort basis (meaning that the ALE may or may not be able to keep up with the packet rate and the short packet may be dropped due to bandwidth limitations). If the RX_CSF_EN and RX_CEF_EN bits are both set in the Pn_MAC_CONTROL register, fragment frames from 33 to 63 bytes will be forwarded only to the host on a best effort basis. Ethernet port received frames shorter than 33 bytes are dropped in all cases.

A received long packet will always contain Pn_RX_MAXLEN number of bytes transferred to memory (if RX_CEF_EN = 1). An example with Pn_RX_MAXLEN = 1518 is below:

- If the frame length is 1518, then the packet is not a long packet and there will be 1518 bytes transferred to memory
- If the frame length is 1519, there will be 1518 bytes transferred to memory. The last three bytes will be the first three CRC bytes

- If the frame length is 1520, there will be 1518 bytes transferred to memory. The last two bytes will be the first two CRC bytes
- If the frame length is 1521, there will be 1518 bytes transferred to memory. The last byte will be the first CRC byte
- If the frame length is 1522, there will be 1518 bytes transferred to memory. The last byte will be the last data byte

2.3.3 MAC Receive FIFO Architecture

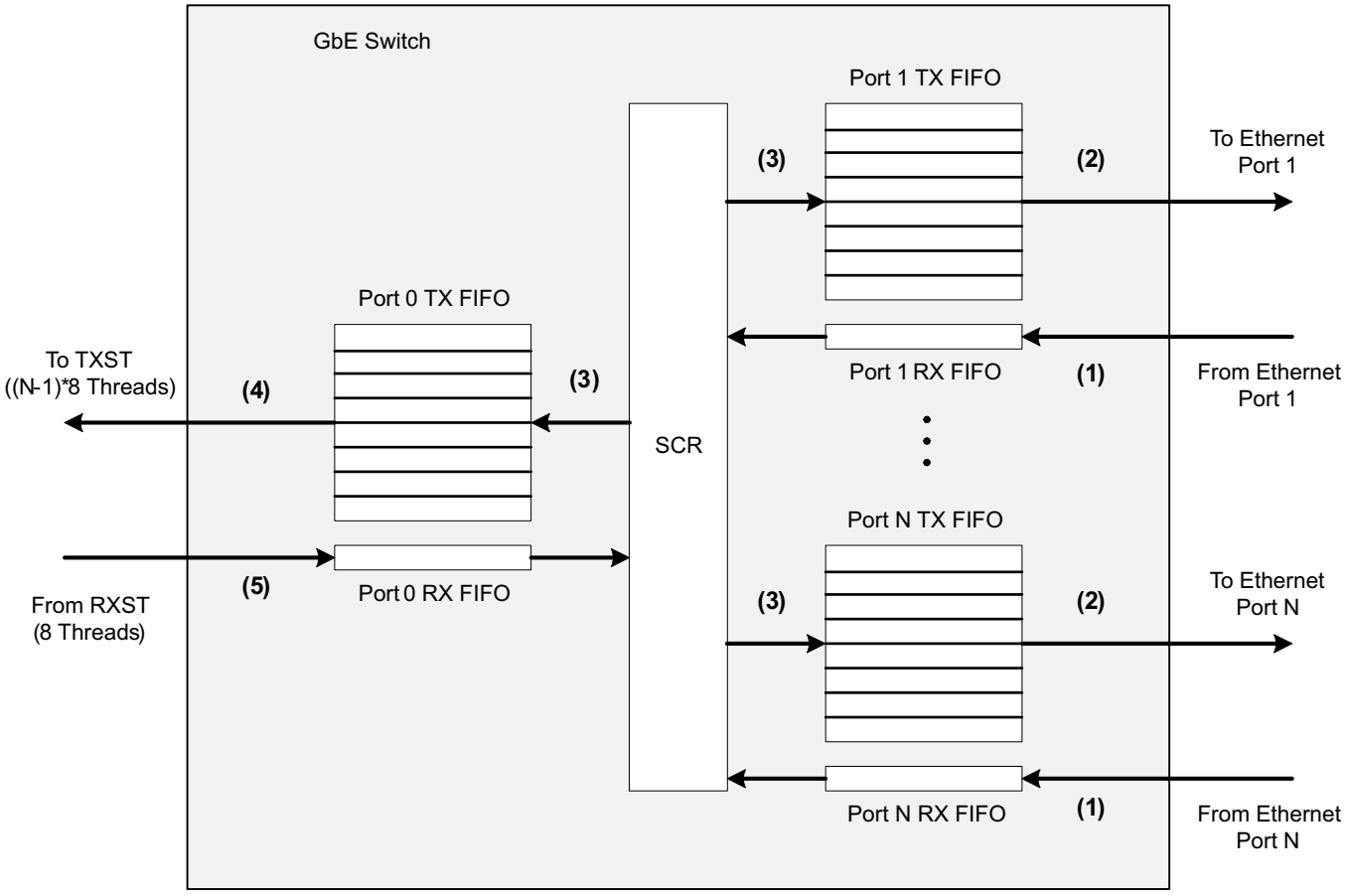
This section describes the architecture of the Ethernet port's receive FIFOs. Internal to the GbE switch, all Ethernet ports have an identical associated packet FIFO. Each transmit packet FIFO contains eight logical transmit queues (priority 0 through 7 with 7 the highest priority). Each transmit FIFO memory contains 81,920 bytes total organized as 2560 by 256-bit words. Each FIFO also contains a single memory for the receive queue. Each receive FIFO memory contains a total of 32768 bytes total organized as 1024 by 256-bit words.

2.3.4 Priority Mapping and Transmit VLAN Priority

There are three priorities that are used inside the GbE Switch: **packet priority**, **header packet priority**, and **switch priority**. The **header packet priority** is used as the outgoing VLAN priority if the packet is egressing from the switch with a VLAN tag. The **switch priority** determines which of the 8 FIFO priority queues the packet uses during egress.

Figure 2-1 below, as well as the corresponding explanation that follows, explains each of the priorities, how they are determined, and how they are used. A number in parentheses in the figure indicates a process (Ethernet port ingress, host port egress, etc.). Each bullet in the text following the diagram explains one of the 5 processes pointed out in the figure.

Figure 2-1. GbE Switch Priority Mapping and Transmit VLAN Processing



From Figure 2-1 above:

- (1) is the ingress process that occurs at the external Ethernet ports
  - The incoming packet is assigned a **packet priority** based on either its VLAN priority, IPv4 or IPv6 DSCP value, or the ingress port's priority. This **packet priority** is then mapped to a **header packet priority** using the Pn_RX_PRI_MAP register where n is the port where the packet entered the switch. This process is explained in further detail in Section 2.3.2.1.3.
- (2) is the egress process that occurs at the external Ethernet ports
  - If the switch is in VLAN Aware mode then the VLAN header may be added, replaced, or removed during the egress process. If the VLAN header is to be added or replaced, the VLAN priority will come from the **header packet priority** that was determined in process (1) or (5). Transmit VLAN processing is the same for both the host port and the external Ethernet ports and is described in Section 2.3.1.1.2.
- (3) is the process by which it is decided which priority TX queue to place the packet on in the Port N TX FIFO during egress
  - Each Port's TX FIFO has 8 queues that each correspond to a priority that is used when determining which packet will egress from the switch next at that port. The **header packet priority** (Ethernet port ingress, process (1)) or the receive packet thread (host port 0 ingress, process (5)) gets mapped through the Pn_TX_PRI_MAP register (where n is the egress port number) to determine the **switch priority** of the packet. The **switch priority** determines which TX FIFO queue to place the packet in. The FIFO architecture is described in Section 2.3.3. The header packet priority to switch priority mapping is discussed in Section 2.3.2.1.3. The received packet thread is described in Section 2.3.1.2.1.
- (4) is the egress process that occurs at Host Port 0 toward the transmit streaming interface (TXST)
  - The TXST has 8 egress threads for each external Ethernet port (32 threads in a 5-port switch and 64 threads in a 9-port switch). The TX thread that is selected for a packet is determined by the Ethernet port of ingress and the **switch priority** of the packet that was determined in process (3). This is described in more detail in Section 2.3.1.1.
  - If the switch is in VLAN Aware mode then the VLAN header may be added, replaced, or removed during the egress process. If the VLAN header is to be added or replaced, the VLAN priority will come from the **header packet priority** that was determined in process (1). Transmit VLAN processing is the same for both the host port and the external Ethernet ports and is described in Section 2.3.1.1.2.
- (5) is the ingress process that occurs at Host Port 0
  - The incoming packet is assigned a **packet priority** based on either its VLAN priority, IPv4 or IPv6 DSCP value, or the host port's priority. This packet priority is then mapped to a **header packet priority** using the Pn_RX_PRI_MAP register. This is discussed in Section 2.3.1.2.1.
  - Host port 0 also has a received packet thread. The receive packet thread is based on either the packet's VLAN priority, IPv4 or IPv6 DSCP value, or the streaming interface (RXST) thread that the packet entered host port 0 on. This is discussed in Section 2.3.1.2.1.

2.3.5 Statistics Submodule Architecture

This section describes the architecture of the statistics modules in the GbE switch (see Section 3.5.3.)

The GbE switch has a statistics module for each port that records events associated with packets entering and exiting the switch at that port. The statistics for host port 0 are recorded in STAT0, the statistics for Ethernet port 1 are recorded in STAT1, and so on for all of the ports. Each statistic register is 32-bits wide and automatically increments when a certain statistics condition is met. Each statistic will rollover from 0xFFFFFFFF to 0x00000000.

2.3.5.1 Accessing Statistics Registers

This section describes how to correctly read and write to the registers in the statistics modules while the modules are disabled or enabled. By default, the statistics modules are disabled. While disabled, all statistics registers can be read and written normally, so writing 0x00000000 clears a statistics register. After the statistics modules are enabled, all statistics can still be read normally; however, register writes will become write to decrement, meaning that the value written to the register will be subtracted from the register value, with the result being stored in the register (new register value = old register value - write value). If the value written is greater than the value in the statistics register, then 0 will be written to that register. When a statistics module is enabled, writing a value of 0xFFFFFFFF will clear a statistics location. When writing to a statistics register, 32-bit accesses must be used. The statistics modules can be enabled by writing to the corresponding bits in the CPSW_STAT_PORT_EN register.

2.3.5.2 Statistics Interrupts

This section describes interrupts generated by the statistics modules. Each of the statistics modules have the ability to send an interrupt to the host. The interrupt for the STAT0 module will occur on the STAT_PEND_RAW[0] signal, the interrupt for the STAT1 module will occur on the STAT_PEND_RAW[1] signal, and so on for all of the statistics modules. The interrupt will be triggered when any of the values in the statistics registers become greater than or equal to 0x80000000. The statistics interrupt is removed by writing to decrement any statistics value greater than 0x80000000.

2.3.5.3 Receive Statistics Descriptions

2.3.5.3.1 Good Receive Frames

The good receive frames statistic is the total number of good frames received on the port. A good frame has the following characteristics:

- Any data or MAC control frame that matched a unicast, broadcast, or multicast address, or matched due to promiscuous mode
- Was of length 64 to Pn_RX_MAXLEN bytes inclusive
- Had no CRC error, alignment error, or code error

See the receive align/code errors and receive CRC errors statistic descriptions for definitions of alignment, code, and CRC errors. Overruns have no effect on this statistic.

2.3.5.3.2 Broadcast Receive Frames

The broadcast receive frames statistic is the total number of good broadcast frames received on the port. A good broadcast frame has the following characteristics:

- Any data or MAC control frame that was destined for address 0xFFFFFFFFFFFF only
- Was of length 64 to Pn_RX_MAXLEN bytes inclusive
- Had no CRC error, alignment error, or code error

See the receive align/code errors and receive CRC errors statistic descriptions for definitions of alignment, code, and CRC errors. Overruns have no effect on this statistic.

2.3.5.3.3 Multicast Receive Frames

The multicast receive frames statistic is total number of good multicast frames received on the port. A good multicast frame has the following characteristics:

- Any data or MAC control frame that was destined for any multicast address other than 0xFFFFFFFFFFFF
- Was of length 64 to Pn_RX_MAXLEN bytes inclusive
- Had no CRC error, alignment error, or code error

See the receive align/code errors and receive CRC errors statistic descriptions for definitions of alignment, code, and CRC errors. Overruns have no effect on this statistic.

2.3.5.3.4 Pause Receive Frames

The pause receive frames statistic is the total number of IEEE 802.3X pause frames received by the port (whether acted upon or not). Such a frame has the following characteristics:

- Contained any unicast, broadcast, or multicast address
- Contained the length/type field value 88.08 (hex) and the opcode 0x0001
- Was of length 64 to Pn_RX_MAXLEN bytes inclusive
- Had no CRC error, alignment error or code error
- Pause-frames had been enabled in the MAC module on that port (TX_FLOW_EN = 1 in the Pn_MAC_CTL register)

The port could have been in either half-duplex or full-duplex mode.

See the receive align/code errors and receive CRC errors statistic descriptions for definitions of alignment, code and CRC errors. Overruns have no effect on this statistic.

-OR-

The pause receive frames statistics is the total number of priority based flow control (802.1Qbb) pause frames received by the port (whether acted upon or not). Such a frame has the following characteristics:

- Contained any unicast, broadcast, or multicast address
- Contained the length/type field value 88.08 (hex) and the opcode 0x0001
- Was of length 64 to Pn_RX_MAXLEN bytes inclusive
- Had no CRC error
- Priority based flow control pause frames are enabled on the port. (TX_FLOW_EN = 1 in the Pn_MAC_CTL Register and TX_FLOW_PRI[7:0] bits are set in the corresponding Pn_PRI_CTL register)

See the Receive CRC errors statistic descriptions for definitions of CRC errors. Overruns have no effect upon this statistic

2.3.5.3.5 Receive CRC Errors

The receive CRC errors statistic is the total number of frames received on the port that experienced a CRC error. Such a frame has the following characteristics:

- Was any data or MAC control frame that matched a unicast, broadcast, or multicast address, or matched due to promiscuous mode
- Was of length 64 to Pn_RX_MAXLEN bytes inclusive
- Had no code/align error, and
- Had a CRC error

Overruns have no effect on this statistic.

A CRC error has the following characteristics:

- A frame containing an even number of nibbles
- Fails the frame check sequence test

2.3.5.3.6 Receive Align/Code Errors

The receive align/code errors statistic is the total number of frames received on the port that experienced an alignment error or code error. Such a frame has the following characteristics:

- Was any data or MAC control frame that matched a unicast, broadcast. or multicast address, or matched due to promiscuous mode
- Was of length 64 to Pn_RX_MAXLEN bytes inclusive
- Had either an alignment error or a code error

Over-runs have no effect on this statistic.

An alignment error has the following characteristics:

- A frame containing an odd number of nibbles
- Fails the frame check sequence test if the final nibble is ignored

A code error is defined to be a frame that has been discarded because the port's MRXER pin driven with a 1 for at least one bit-time's duration at any point during the frame's reception.

NOTE: RFC 1757 etherStatsCRCAlignErrors Ref. 1.5 can be calculated by summing the receive align/code errors and receive CRC errors (see above).

2.3.5.3.7 Oversize Receive Frames

The oversize receive frames statistic is total number of oversized frames received on the port. An oversized frame has the following characteristics:

- Was any data or MAC control frame that matched a unicast, broadcast, or multicast address, or matched due to promiscuous mode
- Was greater than Pn_RX_MAXLEN in bytes
- Had no CRC error, alignment error, or code error

See the receive align/code errors and receive CRC errors statistic descriptions for definitions of alignment, code, and CRC errors. Overruns have no effect on this statistic.

2.3.5.3.8 Receive Jabber Frames

The receive jabber frames statistic is the total number of jabber frames received on the port. A jabber frame has the following characteristics:

- Was any data or MAC control frame that matched a unicast, broadcast, or multicast address, or matched due to promiscuous mode
- Was more than Pn_RX_MAXLEN bytes long
- Had a CRC error, an alignment error, or a code error

See the receive align/code errors and receive CRC errors statistic descriptions for definitions of alignment, code, and CRC errors. Overruns have no effect on this statistic.

2.3.5.3.9 Undersize (Short) Receive Frames

The undersize receive frames statistic is the total number of undersized frames received on the port. An undersized frame has the following characteristics:

- Any data frame that matched a unicast, broadcast, or multicast address, or matched due to promiscuous mode
- Was less than 64 bytes long
- Had no CRC error, alignment error, or code error

See the receive align/code errors and receive CRC errors statistic descriptions for definitions of alignment, code, and CRC errors. Overruns have no effect on this statistic.

2.3.5.3.10 Receive Fragments

The receive fragments statistic is the total number of frame fragments received on the port. A frame fragment has the following characteristics:

- Any data frame (address matching does not matter)
- Was less than 64 bytes long
- Had a CRC error, an alignment error, or a code error
- Was not the result of a collision caused by half duplex, collision based flow control

See the receive align/code errors and receive CRC errors statistic descriptions for definitions of alignment, code, and CRC errors. Overruns have no effect on this statistic.

2.3.5.3.11 Receive Bottom of FIFO Drop

This statistic register counts different events for the Ethernet ports than it does for host port 0. The distinction is explained below.

Ethernet Ports:

The receive bottom of FIFO drop statistic is the total number of frames received on a port that overran the port's receive FIFO and were dropped (bottom of receive FIFO). Port 0 receive (host port ingress) should not drop packets on receive because port 0 receive flow control should be enabled. The Ethernet ports will only drop packets in the receive FIFO when receive flow control is enabled and the sending port ignores sent pause frame and then overruns the receive FIFO. The overrun frame has the following characteristics:

- Any data or MAC control frame which matched a unicast, broadcast or multicast address, or matched due to promiscuous mode
- Was any length (including <64 bytes and > Pn_RX_MAXLEN bytes)
- Was dropped due to a lack of memory space in the receive FIFO

NOTE: This stat should be zero if proper flow control is being followed.

Host Port 0:

This statistic also counts frames dropped on port 0 that were 17 to 33 bytes (only for port 0). For Ethernet ports, the drop count for frames shorter than 33 bytes is included in the undersized or fragment count. Port 0 gives an indication that a packet with 33 bytes was dropped. No other statistics are counted for frames shorter than 33 bytes.

2.3.5.3.12 Portmask Drop

The portmask drop statistic is the total number of frames received on a port that were dropped by the ALE (the ALE did not forward the packet to any port). A portmask drop frame has the following characteristics:

- Any data or MAC control frame
- Was any length greater than 32 bytes
- Was dropped by the ALE due to a zero port mask (was not sent to any destination port)

The frame could have been dropped due to error or other counted reason, so it could be counted in another statistic register also.

2.3.5.3.13 Receive Top of FIFO Drop

The receive top of FIFO drop statistic is the total number of frames received on a port that had a START of frame (SOF) overrun on any destination port egress (when attempting to load the packet from the top of the ingress port receive FIFO into any other port's transmit FIFO). If a multicast/broadcast packet is dropped by multiple destination ports then this statistic will increment by the number of ports that dropped the packet. A receive top Of FIFO drop frame has the following characteristics:

- Any data or MAC control frame which matched a unicast, broadcast or multicast address, or matched due to promiscuous mode
- Was any length (including less than 64 bytes and more than Pn_RX_MAXLEN bytes)
- Had no CRC error, alignment error, or code error.
- Had a SOF of frame overrun on another port egress.

2.3.5.3.14 ALE Drop

The ALE drop statistic is the total number of frames received on a port such that the destination address was not equal to the source address and the packet was not destined to the port it was received on, but the frame was not forwarded to any port (the port mask was zero). An ALE drop frame has the following characteristics:

- Any data or MAC control frame which matched a unicast, broadcast or multicast address, or matched due to promiscuous mode
- Was any length (including less than 64 bytes and more than Pn_RX_MAXLEN bytes)
- Had no CRC error, alignment error, or code error
- Destination address was not equal to the source address
- The packet was not destined for the port it was receive on
- Had a zero port mask

2.3.5.3.15 ALE Overrun Drop

The ALE overrun drop statistic is the total number of frames received on a port that were dropped (zero port mask) due to exceeding the maximum ALE lookup rate (Host port 0 should not have ALE Overrun Drops because the ingress rate is controlled to prevent it).

NOTE: This statistic should be zero. Non-zero indicates a system clock issue or indicates that short packets were sent with RX_CSF_EN = 1 (in the Pn_MAC_CTL Register) at a rate that exceeded the maximum lookup rate.

An ALE overrun drop frame has the following characteristics:

- Any data or MAC control frame which matched a unicast, broadcast or multicast address, or matched due to promiscuous mode
- Was any length (including less than 64 bytes and more than Pn_RX_MAXLEN bytes)
- The maximum ALE lookup rate was exceeded so the lookup was aborted and the packet was dropped.

2.3.5.3.16 ALE Rate Limit Drop

The ALE rate limit drop statistic is the total number of frames received on a port that were dropped (zero port mask) due to receive rate limiting on this port or due to transmit rate limiting on any destination port (not sent to all expected destination ports if transmit rate limiting). An ALE rate limit drop frame has the following characteristics:

- Any data or MAC control frame which matched a unicast, broadcast or multicast address, or matched due to promiscuous mode
- Was any length (including less than 64 bytes and more than Pn_RX_MAXLEN bytes)
- Had no CRC error, alignment error, or code error
- The receive rate was exceeded and the packet was dropped, or the transmit rate was exceeded to any destination port and the packet was dropped to one or more expected destination ports (indicates that the destinations were pruned due to rate limiting).

2.3.5.3.17 ALE VLAN Ingress Check Drop

The ALE VLAN ingress check statistic is the total number of frames received on a port that were dropped (zero port mask) due to VLAN ingress check failure. An ALE VLAN ingress check drop frame has the following characteristics:

- Any data or MAC control frame which matched a unicast, broadcast or multicast address, or matched due to promiscuous mode
- Was any length (including less than 64 bytes and more than Pn_RX_MAXLEN bytes)
- Had no CRC error, alignment error, or code error
- The VLAN ID ingress check failed (the receive port was not in the group)
- The address lookup did not return a match with the super bit set

2.3.5.3.18 ALE Destination Equals Source (DA=SA) Drop

The ALE destination equals source drop statistic register is the total number of frames received on a port that were dropped (zero port mask) due to the destination address being equal to the source address. An ALE DA=SA drop frame has the following characteristics:

- Any data or MAC control frame which matched a unicast, broadcast or multicast address, or matched due to promiscuous mode
- Was any length (including less than 64 bytes and more than Pn_RX_MAXLEN bytes)
- Had no CRC error, alignment error, or code error
- The destination address was equal to the source address
- The source address was not an entry in the ALE table.

2.3.5.3.19 Block Address Drop

The block address drop statistic register is the total number of frames received on a port that were dropped (zero port mask) due to the destination or source address being blocked. A block address drop frame has the following characteristics:

- Any data or MAC control frame which matched a unicast, broadcast or multicast address, or matched due to promiscuous mode
- Was any length (including less than 64 bytes and more than Pn_RX_MAXLEN bytes)
- Had no CRC error, alignment error, or code error
- The source or destination address matched a table entry that had the block bit set.

2.3.5.3.20 ALE Secure Drop

The ALE secure drop statistic register is the total number of frames received on a port that were dropped (zero port mask) due to a secure violation (the source address is owned by a different receive port). An ALE secure drop frame has the following characteristics:

- Any data or MAC control frame which matched a unicast, broadcast or multicast address, or matched due to promiscuous mode
- Was any length (including less than 64 bytes and more than Pn_RX_MAXLEN bytes)
- Had no CRC error, alignment error, or code error
- The source address has an entry in the ALE table with the secure bit set and a port number that does not match the receive port number

2.3.5.3.21 ALE Authentication Drop

The ALE authentication drop statistic register is the total number of frames received on a port that were dropped (zero port mask) due to authentication failure. An ALE authentication drop frame has the following characteristics:

- Any data or MAC control frame which matched a unicast, broadcast or multicast address, or matched due to promiscuous mode
- Was any length (including less than 64 bytes and more than Pn_RX_MAXLEN bytes)
- Had no CRC error, alignment error, or code error
- MAC authorization mode is enabled (EN_AM bit is set to 1 in the ALE_CONTROL register)
- The source address is not equal to the destination address
- The source address is not an ALE table entry
- The destination address is not an ALE table entry with the super bit set

2.3.5.3.22 ALE Unknown Unicast

The ALE unknown unicast statistic register is the total number of frames received on a port that had a unicast destination address with an unknown source address. An ALE unknown unicast frame has the following characteristics:

- Any data or MAC control frame which matched a unicast, broadcast or multicast address, or matched due to promiscuous mode
- Was of length 64 to Pn_RX_MAXLEN bytes inclusive
- Had no CRC error, alignment error, or code error
- The source address was not an ALE table entry

NOTE: The ALE unknown unicast byte count statistic register (STATn_ALE_UNKN_UNI_BCNT) is the number of bytes contained in the ALE Unknown Unicast frames.

2.3.5.3.23 ALE Unknown Multicast

The ALE unknown multicast statistic register is the total number of frames received on a port that had a multicast destination address with an unknown source address. An ALE unknown multicast frame has the following characteristics:

- Any data frame with a multicast destination address
- Was of length 64 to Pn_RX_MAXLEN bytes inclusive
- Had no CRC error, alignment error, or code error
- The source address was not an ALE table entry

NOTE: The ALE unknown multicast byte count statistic register (STATn_ALE_UNKN_MLT_BCNT) is the number of bytes contained in the ALE Unknown Multicast frames.

2.3.5.3.24 ALE Unknown Broadcast

The ALE unknown broadcast statistic register is the total number of frames received on a port that had a broadcast destination address with an unknown source address. An ALE unknown broadcast frame has the following characteristics:

- Any data frame with a broadcast destination address
- Was of length 64 to Pn_RX_MAXLEN bytes inclusive
- Had no CRC error, alignment error, or code error
- The source address was not an ALE table entry

NOTE: The ALE unknown broadcast byte count statistic register (STATn_ALE_UNKN_BRD_BCNT) is the number of bytes contained in the ALE Unknown Broadcast frames.

2.3.5.3.25 Receive Octets

The receive octets statistics register is the total number of bytes in all good frames received on the port. A good frame has the following characteristics:

- Any data or MAC control frame which matched a unicast, broadcast or multicast address, or matched due to promiscuous mode
- Was of length 64 to Pn_RX_MAXLEN bytes inclusive
- Had no CRC error, alignment error, or code error

See the Receive Align/Code Errors and Receive CRC errors statistic descriptions for definitions of alignment, code and CRC errors. Overruns have no effect upon this statistic.

2.3.5.4 Transmit (Only) Statistics Descriptions

The maximum and minimum transmit frame size is software controllable.

2.3.5.4.1 Good Transmit Frames

The good transmit frames statistic is the total number of good frames transmitted on the port. A good frame has the following characteristics:

- Any data or MAC control frame that was destined for any unicast, broadcast or multicast address
- Was any length
- Had no late or excessive collisions, no carrier loss, and no underrun

2.3.5.4.2 Broadcast Transmit Frames

The broadcast transmit frames statistic is the total number of good broadcast frames transmitted on the port. A good broadcast frame has the following characteristics:

- Any data or MAC control frame destined for address 0xFFFFFFFFFFFF only
- Was of any length
- Had no late or excessive collisions, no carrier loss, and no underrun

2.3.5.4.3 Multicast Transmit Frames

The multicast transmit frames statistic is the total number of good multicast frames transmitted on the port. A good multicast frame has the following characteristics:

- Any data or MAC control frame destined for any multicast address other than 0xFFFFFFFFFFFF
- Was of any length
- Had no late or excessive collisions, no carrier loss, and no underrun

2.3.5.4.4 Pause Transmit Frames

The pause transmit frames statistic indicates the number of IEEE 802.3X pause frames transmitted by the port.

Pause frames cannot underrun or contain a CRC error because they are created in the transmitting MAC, so these error conditions have no effect on the statistic. Pause frames sent by software will not be included in this count.

Because pause frames are transmitted only in full duplex, carrier loss and collisions have no effect on this statistic.

Transmitted pause frames are always 64-byte multicast frames, so they will appear in the transmit multicast frames and 64 octet frames statistics.

2.3.5.4.5 Collisions

The collisions statistic records the total number of times that the port experienced a collision. Collisions occur under two circumstances:

1. When a transmit data or MAC control frame has the following characteristics:
   - Was destined for any unicast, broadcast or multicast address
   - Was any size
   - Had no carrier loss and no underrun
   - Experienced a collision
     A jam sequence is sent for every non-late collision, so this statistic will increment on each occasion if a frame experiences multiple collisions (and increments on late collisions).
     CRC errors have no effect on this statistic.
2. When the port is in half-duplex mode, flow control is active, and a frame reception begins

2.3.5.4.6 Single Collision Transmit Frames

The single collision transmit frames statistic is the total number of frames transmitted on the port that experienced exactly one collision. Such a frame has the following characteristics:

- Was any data or MAC control frame destined for any unicast, broadcast, or multicast address
- Was any size
- Had no carrier loss and no underrun
- Experienced one collision before successful transmission. The collision was not late

CRC errors have no effect on this statistic.

2.3.5.4.7 Multiple Collision Transmit Frames

The multiple collision transmit frames statistic is the total number of frames transmitted on the port that experienced multiple collisions. Such a frame has the following characteristics:

- Was any data or MAC control frame destined for any unicast, broadcast, or multicast address
- Was any size
- Had no carrier loss and no underrun
- Experienced 2 to 15 collisions before being successfully transmitted. None of the collisions were late.

CRC errors have no effect on this statistic.

2.3.5.4.8 Excessive Collisions

The excessive collisions statistic is the total number of frames for which transmission was abandoned due to excessive collisions. Such a frame has the following characteristics:

- Was any data or MAC control frame destined for any unicast, broadcast, or multicast address
- Was any size
- Had no carrier loss and no underrun
- Experienced 16 collisions before abandoning all attempts at transmitting the frame. None of the collisions were late.

CRC errors have no effect on this statistic.

2.3.5.4.9 Late Collisions

The late collisions statistic is the total number of frames on the port for which transmission was abandoned because they experienced a late collision. Such a frame has the following characteristics:

- Was any data or MAC control frame destined for any unicast, broadcast, or multicast address
- Was any size
- Experienced a collision later than 512 bit-times into the transmission. There may have been up to 15 previous (non-late) collisions that had previously required the transmission to be re-attempted.

The late collisions statistic dominates over the single, multiple and excessive collisions statistics - if a late collision occurs the frame will not be counted in any of these other three statistics.

CRC errors, carrier loss, and underrun have no effect on this statistic.

2.3.5.4.10 Deferred Transmit Frames

The deferred transmit frames statistic is the total number of frames transmitted on the port that first experienced deferment. Such a frame has the following characteristics:

- Was any data or MAC control frame destined for any unicast, broadcast, or multicast address
- Was any size
- Had no carrier loss and no underrun
- Experienced no collisions before being successfully transmitted
- Found the medium busy when transmission was first attempted, so had to wait

CRC errors have no effect on this statistic.

NOTE: See RFC1623 Ref. 2.6 dot3StatsDeferredTransmissions.

2.3.5.4.11 Carrier Sense Errors

The carrier sense errors statistic is the total number of frames on the port that experienced carrier loss. Such a frame has the following characteristics:

- Was any data or MAC control frame destined for any unicast, broadcast, or multicast address
- Was any size
- The carrier sense condition was lost or never asserted when transmitting the frame (the frame is not retransmitted)

This is a transmit-only statistic. Carrier Sense is a don’t care for received frames. Transmit frames with carrier sense errors are sent until completion and are not aborted.

CRC errors and underrun have no effect on this statistic.

2.3.5.4.12 Transmit Octets

The transmit octets statistic is the total number of bytes in all good frames transmitted on the port. A good frame has the following characteristics:

- Any data or MAC control frame that was destined for any unicast, broadcast, or multicast address
- Was any size
- Had no late or excessive collisions, no carrier loss, and no underrun

2.3.5.4.13 Transmit Priority 0-7

The transmit priority 0-7 statistic register is the total number of frames transmitted on the port from transmit FIFO priority 0-7. Collision retries and pause frames do not affect this statistic. A transmit priority 0-7 frame has the following characteristics:

- Any frame transmitted from priority 0-7
- Was any size
- Collision retries are not counted in this statistic
- Pause frames are not counted in this statistic
- Carrier sense errors do not affect this statistic

NOTE: The transmit priority 0-7 byte count statistic register (STATn_TX_PRIm_BCNT) is the number of bytes contained transmit priority 0-7 frames.

2.3.5.4.14 Transmit Priority 0-7 Drop

The transmit priority 0-7 drop statistic register is the total number of transmit frames on the port that overran the transmit FIFO priority 0-7 and were dropped. A transmit priority 0-7 drop frame has the following characteristics:

- Any frame destined to be transmitted from priority 0-7
- Was any size
- Was dropped due to priority 0-7 FIFO overrun (start of packet overrun)

NOTE: The transmit priority 0-7 drop byte count statistic register (STATn_TX_PRIm_DROP_BCNT) is the number of bytes contained transmit priority 0-7 drop frames.

2.3.5.4.15 Transmit Memory Protect Errors

The transmit memory protect errors statistic register is the total number of transmit frames on the port that had a memory protect CRC error on egress. A transmit memory protect error frame has the following characteristics.

- Any frame destined to be transmitted
- Was any size
- Had a memory protect CRC error on egress

NOTE: Frames destined for the host with memory protect errors are dropped by the transmit streaming interface signals. Frames destined for Ethernet ports will have at least one byte of the generated port type CRC inverted on egress. This statistic is eight bits wide only and will not rollover but will limit at 0xFF. A non-zero value in this statistic will issue a STAT_PEND[n] interrupt where n is the associated port.

2.3.5.5 Receive and Transmit (Shared) Statistics Descriptions

2.3.5.5.1 Net Octets

The net octets statistic is the total number of bytes of frame data received and transmitted on the port. Each frame counted:

- Was any data or MAC control frame destined for any unicast, broadcast or multicast address (address match does not matter)
- Was of any size (including < 64 byte and > Pn_RX_MAXLEN byte frames).

Also counted in this statistic are:

- Every byte transmitted before a carrier-loss was experienced
- Every byte transmitted before each collision was experienced, (i.e., multiple retries are counted each time)
- Every byte received if the port is in half-duplex mode until a jam sequence was transmitted to initiate flow control. (The jam sequence was not counted to prevent double-counting)

Error conditions such as alignment errors, CRC errors, code errors, overruns and underruns do not affect the recording of bytes by this statistic.

The objective of this statistic is to give a reasonable indication of Ethernet utilization.

2.3.5.5.2 Receive + Transmit 64 Octet Frames

The receive and transmit 64 octet frames statistic is the total number of 64-byte frames received and transmitted on the port. Such a frame has the following characteristics:

- Any data or MAC control frame that was destined for any unicast, broadcast, or multicast address
- Did not experience late collisions, excessive collisions, or carrier sense error
- Was exactly 64 bytes long

If the frame was being transmitted and experienced carrier loss that resulted in a frame of this size being transmitted, then the frame will be recorded in this statistic.

CRC errors, code/align errors, and overruns do not affect the recording of frames in this statistic.

2.3.5.5.3 Receive + Transmit 65-127 Octet Frames

The receive and transmit 64-127 octet frames statistic is the total number of frames of size 65 to 127 bytes received and transmitted on the port. Such a frame has the following characteristics:

- Any data or MAC control frame that was destined for any unicast, broadcast, or multicast address
- Did not experience late collisions, excessive collisions, or carrier sense error
- Was 65 to 127 bytes long

CRC errors, code/align errors, underruns and overruns do not affect the recording of frames in this statistic.

2.3.5.5.4 Receive + Transmit 128-255 Octet Frames

The receive and transmit 128-255 octet frames statistic is the total number of frames of size 128 to 255 bytes received and transmitted on the port. Such a frame has the following characteristics:

- Any data or MAC control frame that was destined for any unicast, broadcast, or multicast address
- Did not experience late collisions, excessive collisions, or carrier sense error
- Was 128 to 255 bytes long

CRC errors, code/align errors, underruns, and overruns do not affect the recording of frames in this statistic.

NOTE: For receive reference only, see RFC1757 Ref. 1.13 etherStatsPkts128to255Octets.

2.3.5.5.5 Receive + Transmit 256-511 Octet Frames

The receive and transmit 256-511 octet frames statistic is the total number of frames of size 256 to 511 bytes received and transmitted on the port. Such a frame has the following characteristics:

- Any data or MAC control frame that was destined for any unicast, broadcast, or multicast address
- Did not experience late collisions, excessive collisions, or carrier sense error
- Was 256 to 511 bytes long

CRC errors, code/align errors, underruns and overruns do not affect the recording of frames in this statistic.

2.3.5.5.6 Receive + Transmit 512-1023 Octet Frames

The receive and transmit 512-1023 octet frames statistic is the total number of frames of size 512 to 1023 bytes received and transmitted on the port. Such a frame has the following characteristics:

- Any data or MAC control frame that was destined for any unicast, broadcast, or multicast address
- Did not experience late collisions, excessive collisions, or carrier sense error
- Was 512 to 1023 bytes long

CRC errors, code/align errors and overruns do not affect the recording of frames in this statistic.

2.3.5.5.7 Receive + Transmit 1024 and Above Octet Frames

The receive and transmit 1024 and above octet frames statistic is the total number of frames of size 1024 to RX_MAXLEN bytes for receive or 1024 or more bytes for transmit on the port. Such a frame has the following characteristics:

- Any data or MAC control frame that was destined for any unicast, broadcast, or multicast address
- Did not experience late collisions, excessive collisions, or carrier sense error
- Was 1024 to RX_MAXLEN bytes long on receive, or 1024 or more bytes on transmit

CRC errors, code/align errors, underruns and overruns do not affect the recording of frames in this statistic.

2.3.6 Time Synchronization Submodule Architecture

This section describes the time synchronization module in the GbE switch.

The time synchronization module is used to facilitate host control of time synchronization operations in accordance with Annex D, E, and F of the IEEE 1588 specification. Much of the IEEE 1588 standard is outside of the scope of the time synchronization module, and must be handled by host software. The main purpose of the time synchronization module is to detect time synchronization events and generate timestamps, and then provide this information to host software for processing.

The time synchronization module can generate either 32-bit or 64-bit timestamps which is determined by the 64_BIT bit in the CPTS_CTL register. While in 32-bit mode, the upper 32 bits of each time stamp are forced to 0.

The time synchronization submodule detects the following eight types of time synchronization events:

- Time stamp push event
- Time stamp rollover event (32-bit mode only)
- Time stamp half rollover event (32-bit mode only)
- Hardware time stamp push event
- Ethernet receive event
- Ethernet transmit event
- Time stamp compare event
- Host event

Each of these eight events is covered in more detail later in this section.

2.3.6.1 Time Synchronization Submodule Components

The time synchronization module has several components that together provide the functionality of the time synchronization module. The time synchronization module is made up of the following components:

- Time Stamp Counter (Section 2.3.6.1.1)
- Ethernet Port Interfaces (Section 2.3.6.1.2)
- Event FIFO (Section 2.3.6.1.3)
- Event Pending Interface (Section 2.3.6.1.4)

Each component is described individually.

2.3.6.1.1 Time Stamp Counter

This section describes the time stamp counter for the time synchronization module. The time stamp counter contains a 64-bit value that is maintained internally within the time synchronization module. The value in the time stamp counter is initialized to 0 when the CPTS_EN bit in the CPTS_CTL register is cleared to 0. When the CPTS_EN bit is set to 1, the time stamp value increments on each rising edge of the CPTS_RCLK. The time stamp value can be written by using the TS_LOAD_EN bit in the CPTS_LOAD_EN register as well as the CPTS_LOAD_VAL_H and CPTS_LOAD_VAL_L registers; however, this functionality is provided primarily for test purposes. If operating in 32-bit mode host software must maintain the required number of upper bits of the time stamp value, and must be incremented when the rollover event is detected.

2.3.6.1.2 Ethernet Port Interfaces

This section describes the Ethernet port interfaces to the time synchronization module. The time synchronization module contains identical port interfaces on each external Ethernet port. Each of the time synchronization Ethernet port interfaces contains separate receive and transmit interfaces. The receive interface is used to generate time sync events for valid time synchronization packets that are received on that port. Similarly, the transmit interface is used to generate time sync events for time synchronization packets that are transmitted on that port. Details concerning receive synchronization events can be found in Section 2.3.6.2.5.

Details concerning transmit synchronization events can be found in Section 2.3.6.2.6.

2.3.6.1.3 Event FIFO

This section describes the event FIFO in the time synchronization submodule. The event FIFO contains time synchronization events that are waiting to be processed by host software. Events can be processed using interrupts by enabling the event pending interface, or by polling the CPTS_INTSTAT_RAW register. The event FIFO can hold 16 or 24 events determined by the number of ports your device contains (2*n+6 events, where n is the number of ports in the switch). Events must be processed in a timely manner to prevent overruns. The time synchronization submodule does not contain any logic to indicate when an overrun has occurred.

2.3.6.1.4 Event Pending Interface

This section describes the event pending interface. The event pending interface is used to signal to the host processor when a time synchronization event is detected in the event FIFO. This interface is valid only when using interrupts to process events. The event pending interface is active when the TS_PEND_EN bit in the CPTS_INT_ENABLE register is set to 1. When this bit is set, interrupts will be used to notify the host of any time synchronization events that are detected by the time synchronization module. When the TS_PEND_EN bit in the CPTS_INT_ENABLE register is set to 0, the event pending interface is inactive.

2.3.6.2 Time Synchronization Events

This section describes time synchronization events.

Time synchronization events are pushed onto the event FIFO, which can then be read in the CPTS_EVENT_INFOx registers (where x is 0-3). Table 2-5 shows the time synchronization event fields. See the CPTS_EVENT_INFOx registers (Section 3.5.4.13) for register bit field information.

Table 2-5. Time Synchronization Event Fields

Name	Description
Time Stamp	The time stamp field contains the 64-bit time stamp value for a given packet that contains the section where a clock cycle time stamp can be placed when configured for it. The timestamp value is valid only for time stamp push events, Ethernet receive events, and Ethernet transmit events. The time stamp value is not valid for counter roll over event types. The lower 32 bits of the timestamp will be stored in the CPTS_EVENT_INFO0 register while the upper 32 bits will be stored in the CPTS_EVENT_INFO3 register. If the CPTS is operating in 32-bit mode then the upper 32 bits (in CPTS_EVENT_INFO3) will be forced to 0.
Port Number	The port number is used to indicate the port number of an Ethernet event (1 to 4 encoded)-OR- the hardware push number (1 to 8 encoded)
Event Type	The event field contains the type of event that is represented. The available event types are: • Software time stamp push event • Time stamp rollover event (32-bit mode only) • Time stamp half rollover event (32-bit mode only) • Hardware time stamp push event • Ethernet receive event • Ethernet transmit event • Time stamp compare event • Host event
Message Type	The message type field contains the message type value that was found in an Ethernet receive or transmit event. This field is valid only for Ethernet receive and transmit events.
Sequence ID	The sequence ID field contains the 16-bit sequence ID that was contained in an Ethernet receive or transmit time sync packet. This field is valid only for Ethernet receive and transmit events.
Domain	The 8-bit Domain is the value that was contained in an Ethernet transmit or receive time sync packet. This field is valid only for Ethernet transmit or receive events.

The subsequent sections describe the different event types supported by the time synchronization submodule.

2.3.6.2.1 Time Stamp Push Event

This section describes the time stamp push event. The time stamp push event is an event generated by host software, and is used to obtain the current time stamp value. The time stamp push event is initiated by writing a 1 to bit 0 of the CPTS_PUSH register. After writing the CPTS_PUSH register, the time stamp event is generated and pushed into the time synchronization event FIFO with the time stamp push event code. The time stamp value that is returned will be the value of the time stamp at the time that the CPTS_PUSH register was written.

2.3.6.2.2 Time Stamp Counter Rollover Event

This section describes the time stamp counter rollover event. The time stamp rollover event is used to indicate that the 32-bit time stamp maintained by the time synchronization module has rolled over from 0xFFFFFFFF to 0x00000000. When the rollover occurs, the time stamp rollover event will be pushed into the event FIFO for processing by host software with the time stamp counter rollover event code. The host should use this event to increment any upper time stamp bits that are being maintained in software. This event occurs only in 32-bit mode.

2.3.6.2.3 Time Stamp Counter Half Rollover Event

This section describes the time stamp counter half-rollover event. The half-rollover event indicates to software that the time stamp value maintained internally by the time synchronization module has incremented from 0x7FFF_FFFF to 0x8000_0000. The half-rollover event is included to enable software to correct a misaligned event condition. This event occurs only in 32-bit mode.

The half-rollover event is included to enable software to determine the correct time for each event that contains a valid timestamp value - such as an Ethernet event. If an Ethernet event occurs around a counter rollover (full rollover), then the rollover event could possibly be loaded into the event FIFO before the Ethernet event is loaded into the event FIFO even though the Ethernet event time was actually taken before the rollover. This misaligned event condition arises because an Ethernet event time stamp occurs at the beginning of a packet and time passes before the packet is determined to be a valid synchronization packet. The misaligned event condition occurs if the rollover occurs in the middle, after the packet time stamp has been taken, but before the packet has been determined to be a valid time sync packet.

Host software must detect and correct for the misaligned event condition. For every event time stamp after a rollover, and before a half-rollover, software must examine the most significant bit of the time stamp (TIME_STAMP_L[31]). If the most significant bit of the time stamp is 1, then the time stamp value was before the rollover occurred. If the most significant bit of the time stamp is 0, then the event time stamp was taken after the rollover and no correction is required. The misaligned event can occur only on the rollover boundary and not on the half-rollover boundary. Software does not correct for the misaligned time stamp between a half-rollover and a rollover event, only between a rollover event and a half-rollover event.

When a full rollover occurs, software increments the software time stamp upper value. The misaligned case indicates to software that the misaligned event time stamp has a valid upper value that is pre-increment, so one must be subtracted from the upper value to allow software to calculate the correct time for the misaligned event.

2.3.6.2.4 Hardware Time Stamp Push Event

There are eight hardware time stamp inputs (HW1/8_TS_PUSH) that can cause hardware time stamp push events to be loaded into the event FIFO of the time synchronization module. The PORT_NUMBER field in the event indicates the hardware push input that caused the event (encoded). The hardware time stamp inputs are asynchronous and are low frequency signals. The CPTS logic synchronizes and performs a rising edge detect on the incoming asynchronous input. Each hardware timestamp input must be asserted for at least 10 periods of the fastest clock that will be selected for the timestamp block (CPTS_RCLK). Hardware timestamps are intended to be extremely low frequency signals such that the event FIFO does not overrun. Software must keep up with the event FIFO and ensure that no overrun occurs or events will be lost.

Check your device-specific data manual to see which external pins, if any, are connected to the time synchronization module in order to trigger hardware time stamp push events.

2.3.6.2.5 Ethernet Receive Event

This section describes Ethernet port receive events. All Ethernet ports can generate Ethernet receive events. Each port has an identical interface and can independently generate time synchronization events for valid received time sync packets. For every packet received on the Ethernet ports, a timestamp will be captured by the receive module inside the CPTS for the corresponding port. The time stamp will be captured by the receive module regardless of whether or not the packet is a time synchronization packet to make sure that the time stamp is captured as soon as possible. The packet is sampled on both the rising and falling edges of the CPTS_RCLK, and the time stamp will be captured once the start of frame delimiter for the receive packet is detected.

After the time stamp has been captured, the receive interface will begin parsing the packet to determine if it is a valid Ethernet time synchronization packet. The GbE switch 1588v2 decoder determines if the packet is a valid ethernet receive time synchronization event. The receive interface for the port will use the following criteria to determine if the packet is a valid Annex D, Annex E, or Annex F time synchronization Ethernet receive event:

Annex D (Ethernet Receive)

1. Receive annex D time sync is enabled (RX_ANNEXD_EN is set in the Pn_TS_CTL register).
2. One of the sequences below is true.
   a. The first packet LTYPE matches 0x0800
   b. The first packet LTYPE matches TS_VLAN_LTYPE1 in the Pn_TS_VLAN register and RX_VLN_LT1_EN is set in the Pn_TS_CTL register and the second packet LTYPE matches 0x0800
   c. The first packet LTYPE matches TS_VLAN_LTYPE2 in the Pn_TS_VLAN register and RX_VLN_LT2_EN is set in the Pn_TS_CTL register and the second packet LTYPE matches 0x0800
   d. The first packet LTYPE matches TS_VLAN_LTYPE1 in the Pn_TS_VLAN register and RX_VLN_LT1_EN is set in the Pn_TS_CTL register and the second packet LTYPE matches TS_VLAN_LTYPE2 in the Pn_TS_VLAN register and RX_VLN_LT2_EN is set in the Pn_TS_CTL register and the third packet LTYPE matches 0x0800
3. Byte 14 (the byte after the LTYPE) contains 0x45 (IPv4).

NOTE: The byte numbering assumes that there are no VLANs. The byte number is intended to show the relative order of the bytes.

4. Byte 20 contains 0bXXX00000 (5 lower bits zero) and Byte 21 contains 0x00 (fragment offset zero)
5. Byte 22 contains 0x00 if the TS_TTL_NONZERO_EN bit in the switch Pn_TS_CTL_LTYPE2 register is cleared to 0 -OR- byte 22 contains any value if TS_TTL_NONZERO_EN is set to 1. Byte 22 is the time to live field.
6. Byte 23 contains 0x11 (Next Header UDP Fixed).
7. The TS_UNI_EN bit in the Pn_TS_CTL_LTYPE2 register is cleared to 0 and Bytes 30 through 33 contain:
   a. Decimal 224.0.1.129 and the TS_129 bit in the Pn_TS_CTL_LTYPE2 register is set, or
   b. Decimal 224.0.1.130 and the TS_130 bit in the Pn_TS_CTL_LTYPE2 register is set, or
   c. Decimal 224.0.1.131 and the TS_131 bit in the Pn_TS_CTL_LTYPE2 register is set, or
   d. Decimal 224.0.1.132 and the TS_132 bit in the Pn_TS_CTL_LTYPE2 register is set, or
   e. Decimal 224.0.0.107 and the TS_107 bit in the Pn_TS_CTL_LTYPE2 register is set
   f. -OR-
   g. The TS_UNI_EN bit in the Pn_TS_CTL_LTYPE2 register is set and Bytes 30 through 33 contain any values.
8. Bytes 36 and 37 contain:
   a. Decimal 0x01 and 0x3f respectively and the TS_319 bit in the Pn_TS_CTL_LTYPE2 register is set -OR-
   b. Decimal 0x01 and 0x40 respectively and the TS_320 bit in the Pn_TS_CTL_LTYPE2 register is set.
9. The PTP message begins in byte 42.
10. The packet message type is enabled in the MSG_TYPE_EN field in the Pn_TS_CTL register.
11. The packet was received without error (not long/short/mac_ctl/CRC/code/align).

Annex E (Ethernet Receive)

1. Receive annex E time sync is enabled (RX_ANNEXE_EN bit is set in the switch Pn_TS_CTL register).
2. One of the sequences below is true.
   a. The first packet LTYPE matches 0x86dd.
   b. The first packet LTYPE matches TS_VLAN_LTYPE1 in the Pn_TS_VLAN register and RX_VLN_LT1_EN is set in the Pn_TS_CTL register and the second packet LTYPE matches 0x86dd
   c. The first packet LTYPE matches TS_VLAN_LTYPE2 in the Pn_TS_VLAN register and RX_VLN_LT2_EN is set in the Pn_TS_CTL register and the second packet LTYPE matches 0x86dd
   d. The first packet LTYPE matches TS_VLAN_LTYPE1 in the Pn_TS_VLAN register and RX_VLN_LT1_EN is set in the Pn_TS_CTL register and the second packet LTYPE matches TS_VLAN_LTYPE2 in the Pn_TS_VLAN register and RX_VLN_LT2_EN is set in the Pn_TS_CTL register and the third packet LTYPE matches 0x86dd
3. Byte 14 (the byte after the LTYPE) contains 0x6X (IPv6).
4. Byte 20 contains 0x11 (UDP Fixed Next Header).
5. Byte 21 contains 0x01 (Hop Limit = 1).
6. The TS_UNI_EN bit in the Pn_TS_CTL_LTYPE2 register is cleared to 0 and Bytes 38 through 53 contain:
   a. FF0M:0:0:0:0:0:0:0181 and the TS_129 bit in the Pn_TS_CTL_LTYPE2 register is set, or
   b. FF0M:0:0:0:0:0:0:0182 and the TS_130 bit in the Pn_TS_CTL_LTYPE2 register is set, or
   c. FF0M:0:0:0:0:0:0:0183 and the TS_131 bit in the Pn_TS_CTL_LTYPE2 register is set, or
   d. FF0M:0:0:0:0:0:0:0184 and the TS_132 bit in the Pn_TS_CTL_LTYPE2 register is set, or
   e. FF0M:0:0:0:0:0:0:006B and the TS_107 bit in the Pn_TS_CTL_LTYPE2 register is set

   NOTE: All values above are 16-bit hex numbers where M is enabled in the TS_MCAST_TYPE_EN field in the Pn_TS_CTL2 register.

   -OR-

   f. The TS_UNI_EN bit in the Pn_TS_CTL_LTYPE2 register is set to 1 and Bytes 38 through 53 contain any value.
7. Bytes 56 and 57 contain (UDP Header in bytes 54 through 61):
   a. Decimal 0x01 and 0x3f respectively and the TS_319 bit in the Pn_TS_CTL_LTYPE2 register is set, or
   b. Decimal 0x01 and 0x40 respectively and the TS_320 bit in the Pn_TS_CTL_LTYPE2 register is set.
8. The PTP message begins in byte 62.
9. The packet message type is enabled in the MSG_TYPE_EN field in the Pn_TS_CTL register.
10. The packet was received without error (not long/short/mac_ctl/CRC/code/align).

Annex F (Ethernet Receive)

1. Receive Annex F time sync is enabled (RX_ANNEXF_EN is set in the switch Pn_TS_CTL register).
2. One of the sequences below is true:
   a. The first packet LTYPE matches TS_LTYPE1 in the Pn_TS_SEQ_LTYPE register. LTYPE 1 should be used when only one time sync LTYPE is to be enabled.
   b. The first packet LTYPE matches TS_LTYPE2 in the Pn_TS_CTL_LTYPE2 register and LTYPE2_EN is set in the Pn_TS_CTL register.
   c. The first packet LTYPE matches TS_VLAN_LTYPE1 in the Pn_TS_VLAN register and RX_VLN_LT1_EN is set in the Pn_TS_CTL register and the second packet LTYPE matches TS_LTYPE1 in the Pn_TS_SEQ_LTYPE register
   d. The first packet LTYPE matches TS_VLAN_LTYPE1 in the Pn_TS_VLAN register and RX_VLN_LT1_EN is set in the Pn_TS_CTL register and the second packet LTYPE matches TS_LTYPE2 in the Pn_TS_CTL_LTYPE2 register and LTYPE2_EN is set in the Pn_TS_CTL register.
   e. The first packet LTYPE matches TS_VLAN_LTYPE2 in the Pn_TS_VLAN register and RX_VLN_LT2_EN is set in the Pn_TS_CTL register and the second packet LTYPE matches TS_LTYPE1 in the Pn_TS_SEQ_LTYPE register.
   f. The first packet LTYPE matches TS_VLAN_LTYPE2 in the Pn_TS_VLAN register and RX_VLN_LT2_EN is set in the Pn_TS_CTL register and the second packet LTYPE matches TS_LTYPE2 in the Pn_TS_CTL_LTYPE2 register and LTYPE2_EN is set in the Pn_TS_CTL register.
   g. The first packet LTYPE matches TS_VLAN_LTYPE1 in the Pn_TS_VLAN register and RX_VLN_LT1_EN is set in the Pn_TS_CTL register and the second packet LTYPE matches TS_VLAN_LTYPE2 in the Pn_TS_VLAN register and RX_VLN_LT2_EN is set in the Pn_TS_CTL register and the third packet LTYPE matches TS_LTYPE1 in the Pn_TS_SEQ_LTYPE register.
   h. The first packet LTYPE matches TS_VLAN_LTYPE1 in the Pn_TS_VLAN register and RX_VLN_LT1_EN is set in the Pn_TS_CTL register and the second packet LTYPE matches TS_VLAN_LTYPE2 in the Pn_TS_VLAN register and RX_VLN_LT2_EN is set in the Pn_TS_CTL register and the third packet LTYPE matches TS_LTYPE2 in the Pn_TS_CTL_LTYPE2 register and LTYPE2_EN is set in the Pn_TS_CTL register
3. The PTP message begins in the byte after the LTYPE.
4. The packet message type is enabled in the MSG_TYPE_EN field in the Pn_TS_CTL register.
5. The packet was received without error (not long/short/mac_ctl/CRC/code/align).

If all of the criteria described above are met for either Annex D, Annex E, or Annex F, and the packet is determined to be a valid time synchronization packet, then the RX interface will push an Ethernet receive event into the event FIFO. For more information about event formatting, see Table 2-5. For more information on how to detect and process receive events, see Section 2.3.6.4.

2.3.6.2.6 Ethernet Transmit Event

This section describes Ethernet port transmit events. All Ethernet ports can generate Ethernet transmit events. Each port has an identical interface and can independently generate time synchronization events for valid transmit time sync packets. For every packet transmitted on the Ethernet ports, the port transmit interface will begin parsing the packet to determine if it is a valid Ethernet time synchronization packet. The CPTS transmit interface for the port will use to the following criteria to determine if the packet is a valid time synchronization Ethernet transmit event. The GbE switch 1588v2 decoder determines if the packet is a valid ethernet receive time synchronization event. To be a valid Ethernet transmit time synchronization event, the conditions listed below must be true for either Annex D, Annex E, or Annex F:

Annex D (Ethernet Transmit)

1. Transmit annex D time sync is enabled (TX_ANNEXD_EN is set in the Pn_TS_CTL register).
2. One of the sequences below is true.
   a. The first packet LTYPE matches 0x0800
   b. The first packet LTYPE matches TS_VLAN_LTYPE1 in the Pn_TS_VLAN register and TX_VLN_LT1_EN is set in the Pn_TS_CTL register and the second packet LTYPE matches 0x0800
   c. The first packet LTYPE matches TS_VLAN_LTYPE2 in the Pn_TS_VLAN register and TX_VLN_LT2_EN is set in the Pn_TS_CTL register and the second packet LTYPE matches 0x0800
   d. The first packet LTYPE matches TS_VLAN_LTYPE1 in the Pn_TS_VLAN register and TX_VLN_LT1_EN is set in the Pn_TS_CTL register and the second packet LTYPE matches TS_VLAN_LTYPE2 in the Pn_TS_VLAN register and TX_VLN_LT2_EN is set in the Pn_TS_CTL register and the third packet LTYPE matches 0x0800
3. Byte 14 (the byte after the LTYPE) contains 0x45 (IPv4).

NOTE: The byte numbering assumes that there are no VLANs. The byte number is intended to show the relative order of the bytes.

4. Byte 20 contains 0bXXX00000 (5 lower bits zero) and Byte 21 contains 0x00 (fragment offset zero)
5. Byte 22 contains 0x00 if the TS_TTL_NONZERO_EN bit in the switch Pn_TS_CTL_LTYPE2 register is cleared to 0 -OR- byte 22 contains any value if TS_TTL_NONZERO_EN is set to 1. Byte 22 is the time to live field.
6. Byte 23 contains 0x11 (Next Header UDP Fixed).
7. The TS_UNI_EN bit in the Pn_TS_CTL_LTYPE2 register is cleared to 0 and Bytes 30 through 33 contain:
   a. Decimal 224.0.1.129 and the TS_129 bit in the Pn_TS_CTL_LTYPE2 register is set, or
   b. Decimal 224.0.1.130 and the TS_130 bit in the Pn_TS_CTL_LTYPE2 register is set, or
   c. Decimal 224.0.1.131 and the TS_131 bit in the Pn_TS_CTL_LTYPE2 register is set, or
   d. Decimal 224.0.1.132 and the TS_132 bit in the Pn_TS_CTL_LTYPE2 register is set, or
   e. Decimal 224.0.0.107 and the TS_107 bit in the Pn_TS_CTL_LTYPE2 register is set, or
   f. The TS_UNI_EN bit in the Pn_TS_CTL_LTYPE2 register is set and Bytes 30 through 33 contain any values.
8. Bytes 36 and 37 contain:
   a. Decimal 0x01 and 0x3f respectively and the TS_319 bit in the Pn_TS_CTL_LTYPE2 register is set -OR-
   b. Decimal 0x01 and 0x40 respectively and the TS_320 bit in the Pn_TS_CTL_LTYPE2 register is set.
9. The PTP message begins in byte 42.
10. The packet message type is enabled in the MSG_TYPE_EN field in the Pn_TS_CTL register.
11. The packet was sent by host port 0.

Annex E (Ethernet Transmit)

1. Transmit annex E time sync is enabled (TX_ANNEXE_EN bit is set in the switch Pn_TS_CTL register).
2. One of the sequences below is true.
   a. The first packet LTYPE matches 0x86dd.
   b. The first packet LTYPE matches TS_VLAN_LTYPE1 in the Pn_TS_VLAN register and RX_VLN_LT1_EN is set in the Pn_TS_CTL register and the second packet LTYPE matches 0x86dd
   c. The first packet LTYPE matches TS_VLAN_LTYPE2 in the Pn_TS_VLAN register and RX_VLN_LT2_EN is set in the Pn_TS_CTL register and the second packet LTYPE matches 0x86dd
   d. The first packet LTYPE matches TS_VLAN_LTYPE1 in the Pn_TS_VLAN register and RX_VLN_LT1_EN is set in the Pn_TS_CTL register and the second packet LTYPE matches TS_VLAN_LTYPE2 in the Pn_TS_VLAN register and RX_VLN_LT2_EN is set in the Pn_TS_CTL register and the third packet LTYPE matches 0x86dd
3. Byte 14 (the byte after the LTYPE) contains 0x6X (IPv6).
4. Byte 20 contains 0x11 (UDP Fixed Next Header).
5. Byte 21 contains 0x01 (Hop Limit = 1).
6. The TS_UNI_EN bit in the Pn_TS_CTL_LTYPE2 register is cleared to 0 and Bytes 38 through 53 contain:
   a. FF0M:0:0:0:0:0:0:0181 and the TS_129 bit in the Pn_TS_CTL_LTYPE2 register is set, or
   b. FF0M:0:0:0:0:0:0:0182 and the TS_130 bit in the Pn_TS_CTL_LTYPE2 register is set, or
   c. FF0M:0:0:0:0:0:0:0183 and the TS_131 bit in the Pn_TS_CTL_LTYPE2 register is set, or
   d. FF0M:0:0:0:0:0:0:0184 and the TS_132 bit in the Pn_TS_CTL_LTYPE2 register is set, or
   e. FF0M::0:0:0:0:0:006B and the TS_107 bit in the Pn_TS_CTL_LTYPE2 register is set

   NOTE: All values above are 16-bit hex numbers where M is enabled in the TS_MCAST_TYPE_EN field in the Pn_TS_CTL2 register.

   -OR-
   f. The TS_UNI_EN bit in the Pn_TS_CTL_LTYPE2 register is set to 1 and Bytes 38 through 53 contain any value.
7. Bytes 56 and 57 contain (UDP Header in bytes 54 through 61):
   a. Decimal 0x01 and 0x3f respectively and the TS_319 bit in the Pn_TS_CTL_LTYPE2 register is set, or
   b. Decimal 0x01 and 0x40 respectively and the TS_320 bit in the Pn_TS_CTL_LTYPE2 register is set.
8. The PTP message begins in byte 62.
9. The packet message type is enabled in the MSG_TYPE_EN field in the Pn_TS_CTL register.
10. The packet was sent by host port 0.

Annex F (Ethernet Transmit)

1. Transmit Annex F time sync is enabled (TX_ANNEXF_EN is set in the switch Pn_TS_CTL register).
2. One of the sequences below is true:
   a. The first packet LTYPE matches TS_LTYPE1 in the Pn_TS_SEQ_LTYPE register. LTYPE 1 should be used when only one time sync LTYPE is to be enabled.
   b. The first packet LTYPE matches TS_LTYPE2 in the Pn_TS_CTL_LTYPE2 register and LTYPE2_EN is set in the Pn_TS_CTL register.
   c. The first packet LTYPE matches TS_VLAN_LTYPE1 in the Pn_TS_VLAN register and RX_VLN_LT1_EN is set in the Pn_TS_CTL register and the second packet LTYPE matches TS_LTYPE1 in the Pn_TS_SEQ_LTYPE register
   d. The first packet LTYPE matches TS_VLAN_LTYPE1 in the Pn_TS_VLAN register and TX_VLN_LT1_EN is set in the Pn_TS_CTL register and the second packet LTYPE matches TS_LTYPE2 in the Pn_TS_CTL_LTYPE2 register and LTYPE2_EN is set in the Pn_TS_CTL register.
   e. The first packet LTYPE matches TS_VLAN_LTYPE2 in the Pn_TS_VLAN register and TX_VLN_LT2_EN is set in the Pn_TS_CTL register and the second packet LTYPE matches TS_LTYPE1 in the Pn_TS_SEQ_LTYPE register.
   f. The first packet LTYPE matches TS_VLAN_LTYPE2 in the Pn_TS_VLAN register and TX_VLN_LT2_EN is set in the Pn_TS_CTL register and the second packet LTYPE matches TS_LTYPE2 in the Pn_TS_CTL_LTYPE2 register and LTYPE2_EN is set in the Pn_TS_CTL register.
   g. The first packet LTYPE matches TS_VLAN_LTYPE1 in the Pn_TS_VLAN register and TX_VLN_LT1_EN is set in the Pn_TS_CTL register and the second packet LTYPE matches TS_VLAN_LTYPE2 in the Pn_TS_VLAN register and TX_VLN_LT2_EN is set in the Pn_TS_CTL register and the third packet LTYPE matches TS_LTYPE1 in the Pn_TS_SEQ_LTYPE register.
   h. The first packet LTYPE matches TS_VLAN_LTYPE1 in the Pn_TS_VLAN register and TX_VLN_LT1_EN is set in the Pn_TS_CTL register and the second packet LTYPE matches TS_VLAN_LTYPE2 in the Pn_TS_VLAN register and TX_VLN_LT2_EN is set in the Pn_TS_CTL register and the third packet LTYPE matches TS_LTYPE2 in the Pn_TS_CTL_LTYPE2 register and LTYPE2_EN is set in the Pn_TS_CTL register
3. The packet message type is enabled in the MSG_TYPE_EN field in the Pn_TS_CTL register.
4. The packet was sent by host port 0.

If all of the criteria described above are met, and the packet is determined to be a valid time synchronization packet, then the time stamp for the transmit event will not be generated until the start of frame delimiter of the packet is actually transmitted. The start of frame delimiter will be sampled on every rising and falling edge of the CPTS_RCLK. Once the packet is transmitted, then the TX interface will push an Ethernet transmit event into the event FIFO. For more information about event formatting please see Table 2-5. For more information on how to detect and process transmit events, see Section 2.3.6.4.

2.3.6.2.7 Timestamp Compare Event

The time synchronization module can generate an event for a time stamp comparison. The TS_COMP output signal will also be asserted when this event is generated. The TS_COMP signal will be asserted for a number of CPTS_RCLK cycles equal to the value in the CPTS_TS_COMP_LENGTH register.

The event is generated when the TIME_STAMP[31:0] (and TIME_STAMP[63:32] in 64-bit mode) value compares with the TS_COMP_VAL_L[31:0] value in the CPTS_TS_COMP_VAL_L register (and TS_COMP_VAL_H[31:0] value in the CPTS_TS_COMP_VAL_H register in 64-bit mode) and the TS_COMP_LENGTH[15:0] value in the CPTS_TS_COMP_LENGTH register is non-zero.

NOTE: The TS_COMP_LENGTH[15:0] value should be written by software after the TS_COMP_VAL_L[31:0] register (and the TS_COMP_VAL_H[31:0] register) is written and should be zero when the comparison value is written.

2.3.6.2.8 Host Event

The host can send a packet to be transmitted on an Ethernet port that will generate a time synchronization event. The host sets the TIMESTAMP_EN bit and sends the DOMAIN, MSG_TYPE, and SEQUENCE_ID in the additional control information that resides in the protocol specific section of the descriptor that is transmitted to the GbE switch (see Section 2.3.1.2). An event is then generated and placed on the event FIFO once the packet is transmitted. Host events allow the user to timestamp exactly when a software generated packet exits the device.

2.3.6.3 Time Synchronization Initialization

The time synchronization registers and GbE switch should be configured as shown below:

2.3.6.3.1 Time Synchronization Module Configuration

Step 1. Clear the CPTS_EN bit to 0 in the CPTS_CTL register. The CPTS module is in reset while this bit is 0.

Step 2. Write the CPTS_RFTCLK_SEL value in the CPTS_RFTCLK_SEL register with the desired reference clock multiplexor value. This value is allowed to be written only when the CPTS_EN bit is cleared to 0.

Step 3. Write a 1 to the CPTS_EN bit in the CPTS_CTL register.

Step 4. Program the registers used for the Annex D, Annex E, and Annex F receive and transmit decoding as specified above (See Section 2.3.6.2.5 and Section 2.3.6.2.6).

Step 5. Enable the interrupt by writing a 1 to the TS_PEND_EN bit in the CPTS_INT_ENABLE register (if using interrupts and not polling).

2.3.6.4 Detecting and Processing Time Synchronization Events

This section describes detecting and processing time synchronization events. Section 2.3.6.4.1 discusses how to detect time synchronization events through the use of interrupts and through the use of register polling. Section 2.3.6.4.2 discusses how to use the register interface to pop time synchronization events from the event FIFO.

NOTE: These sections cover only how to detect an event, and pop the event from the event FIFO for processing. It is up to the application software as to how to process the time synchronization event.

2.3.6.4.1 Detecting Time Synchronization Events

This section describes detecting time synchronization events. The time synchronization module allows time synchronization events to be detected through the use of interrupts or through the use of polling.

If using interrupts, then the time synchronization event pending interrupt will signal when an event is pending. To enable the time synchronization interrupt write a 1 to the TS_PEND_EN bit in the CPTS_INT_ENABLE register. This will enable the TS_PEND interrupt to be passed to the Network Coprocessor.

If polling is the preferred method for detecting time synchronization events, then events can be detected by directly reading the CPTS_INTSTAT_RAW register. When the TS_PEND_RAW bit in the CPTS_INTSTAT_RAW register is a 1, then it means that there are one or more events pending in the event FIFO. If using polling make sure that the TS_PEND_EN bit in the CPTS_INT_ENABLE register is set to 0.

2.3.6.4.2 Popping Time Synchronization Events from the Event FIFO

This section describes how to pop time synchronization events from the event FIFO. Once a time synchronization event has been detected, Section 2.3.6.4.2.1 can be used to pop time synchronization events from the event FIFO. If there is more than one event in the event FIFO, multiple events can be processed back-to-back before returning from the event processing routine. Assume that Step 1 below takes place either after a TS_PEND interrupt has occurred -OR- after the TS_PEND_RAW bit in the CPTS_INTSTAT_RAW register has changed to 1 as discovered through polling.

2.3.6.4.2.1 Popping Time Synchronization Events from the Event FIFO

Step 1. Read the CPTS_EVENT_INFO0, CPTS_EVENT_INFO1, CPTS_EVENT_INFO2, and CPTS_EVENT_INFO3 register values.

Step 2. Write a 1 to the EVENT_POP bit of the CPTS_EVENT_POP register to pop the previously read values off the event FIFO.

Step 3. If not processing multiple events, go to step 5. Otherwise, wait for at least 4 CPTS_RCLK periods, plus 4 CPU/3 clock periods.

Step 4. Read the TS_PEND_RAW bit in the CPTS_INTSTAT_RAW register to determine if another valid event is in the event FIFO. If the TS_PEND_RAW bit is nonzero, go to step 1. Otherwise, go to the next step.

Step 5. Return from the event processing routine. If using interrupts instead of polling this includes processing the end of interrupt as required by upper level modules which is outside the scope of this document.

2.3.7 Address Lookup Engine (ALE) Submodule Architecture

The Address Lookup Engine (ALE) processes all received packets to determine which port(s) if any that the packet should the forwarded to. The ALE uses the incoming packet received port number, destination address, source address, length/type, and VLAN information to determine how the packet should be forwarded. The ALE outputs the port mask to the switch fabric that indicates the port(s) the packet should be forwarded to. The ALE is enabled when the ENABLE_ALE bit in the ALE_CONTROL Register is set. All packets are dropped when the ENABLE_ALE bit is cleared to 0.

In normal operation, the MAC modules are configured to issue an abort, instead of an end of packet, at the end of a packet that contains an error (runt, frag, oversize, jabber, CRC, alignment, code, etc.) or at the end of a mac control packet. However, when the CEF, CSF, or CMF MAC configuration bit(s) are set, error frames, short frames or MAC control frames have a normal end of packet instead of an abort at the end of the packet. When the ALE receives a packet that contains errors, or a MAC control frame, and does not receive an abort, the packet will be forwarded only to the host port (port 0). Packets with errors that are forwarded to the host port have no VLAN untagging or drop occur due to rate limiting. No ALE learning occurs on packets with errors or MAC control frames. Learning is based on source address and lookup is based on destination address. Directed packets from the host are not learned, updated, or touched.

The ALE may be configured to operate in bypass mode by setting the ALE_BYPASS bit in the ALE_CONTROL register. When in bypass mode, all packets received by the MAC modules are forwarded only to the host port (port 0). In bypass mode, the ALE processes host port transmit packets (packets coming into the switch at port 0, destined for any of the external Ethernet ports) the same as it would when in normal mode. The host port is also capable of sending packets directly to the external Ethernet ports, bypassing the ALE, using directed packets.

The ALE may be configured to operate in OUI deny mode by setting the EN_OUI_DENY bit in the ALE_CONTROL register. When in OUI deny mode, any packet with a non-matching OUI source address will be dropped to the host unless the packet destination address matches with a supervisory table entry. Non-matching OUI source address broadcast/multicast packets will be dropped to the host unless the packet destination address is entered into the table with the super bit set. Non-matching OUI source address unicast packets will be dropped to the host unless the unicast destination address is in the table with block and secure both set. When EN_OUI_DENY is cleared, any packet source address matching an

OUI address table entry will be dropped to the host unless the destination address matches with a supervisory address table entry. Broadcast packets matching the OUI source address will be dropped to the host unless the broadcast destination address is entered into the table with the super bit set. Unicast packets matching the OUI source address will be dropped to the host unless the unicast destination address is in the table with block and secure both set.

Multicast supervisory packets are designated by the super bit in the table entry. Unicast supervisory packets are indicated when block and secure are both set. Supervisory packets are not dropped due to rate limiting, OUI, or VLAN processing.

2.3.7.1 ALE Table

The ALE table contains multiple table entry types. Each table entry represents either a free entry, a multicast address entry, a VLAN/multicast address pair entry, a unicast address entry, an OUI unicast address entry, a VLAN/unicast address pair entry, or a VLAN entry. Software should ensure that there are not double address entries in the table. The double entry used would be indeterminate. The number of entries that the table can contain is device specific. Check the ALE_STATUS register to determine the number of entries that your device's ALE table can contain.

Source Address learning occurs for packets with a unicast, multicast or broadcast destination address, and a unicast or multicast (including broadcast) source address. Multicast source addresses have the group bit (bit 40) cleared before ALE processing begins, which changes the multicast source address to a unicast source address. A multicast address of all ones is the broadcast address, which may be added to the table. A learned unicast source address is added to the table with the following control bits:

Table 2-6. ALE Table Learned Address Control Bits

Unicast Type	11
Block	0
Secure	0

If a received packet has a source address that is equal to the destination address, the following occurs:

- The address is learned if the address is not found in the table
- The address is updated if the address is found
- The packet is dropped

2.3.7.2 Reading Entries from the ALE Table

This section provides the procedure for reading entries from the ALE table. To read an entry from the ALE table, the user must perform the following steps:

1. Program the ENTRY_POINTER field and the WRITE_RDZ field in the ALE_TBLCTL Register
   - The ENTRY_POINTER value is the entry number that will be accessed in the ALE table. Valid entry numbers are from 0 to the maximum number of entries minus 1. The maximum number of entries can be determine by the ALE_STATUS Register.
   - Setting the WRITE_RDZ field to 0 will cause the entry values to be read from the table
2. Once the write to ALE_TBLCTL Register has completed, the entry in the ALE table at the ENTRY_POINTER location will be programmed in to the ALE_TBLW[0:2] Registers

2.3.7.3 Writing Entries to the ALE Table

This section provides the procedure for writing entries to the ALE table. To add an entry to the ALE table, the user must use the following steps:

1. Program the ALE_TBLW[0:2] registers with the desired values for the desired entry type.
2. Program the ENTRY_POINTER and WRITE_RDZ fields of the ALE_TBLCTL register to add the entry to the table.
   - The ENTRY_POINTER value is the entry number that will be written to in the ALE table. Valid entry numbers are from 0 to the maximum number of entries minus 1. The maximum number of entries can be determine by the ALE_STATUS register.
   - Setting the WRITE_RDZ field to 1 will cause the entry to be added to the table.

When adding an entry to the ALE Table, the entry must be one of the types defined in the ALE Table Entry Types section. Before adding an entry to the ENTRY_POINTER location in the ALE table, the user may want to read the entry to see if the entry is free (ENTRY_TYPE = 00). For the procedure to read an entry from the ALE table, see Section 2.3.7.2.

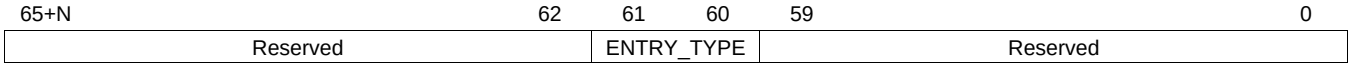
2.3.7.4 ALE Table Entry Types

This section will describe the allowable configurations for entries to the ALE table. All entries in the ALE table must be one of the following types. ALE table entries can be read using the procedure described in Section 2.3.7.2. Entries can be added to ALE table using the procedure described in Section 2.3.7.3.

2.3.7.4.1 Free Table Entry

The format for a free table entry is shown in Figure 2-2, and the required field configuration is described in Table 2-7. A free table entry is an entry in the table this is currently unused. The variable N below is 5 for a 5-port switch and 9 for a 9-port switch. Check your device-specific data manual to see how many ports your switch contains.

Figure 2-2. Free Table Entry



For a free table entry, the fields must be set as shown in Table 2-7. General descriptions of the ALE table entry fields are provided in Table 2-14.

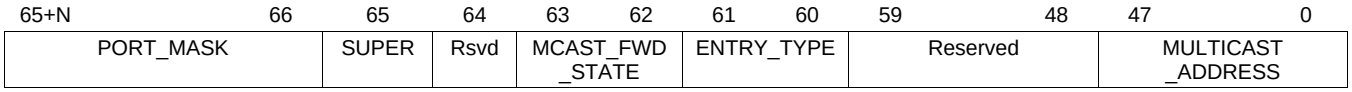
Table 2-7. Free Table Entry Field Configuration

Field Name	Configuration
ENTRY_TYPE[1:0]	00

2.3.7.4.2 Multicast Address Table Entry

The format for a multicast address table entry is shown in Figure 2-3, and the required field configuration is described in Table 2-8. The variable N below is 5 for a 5-port switch and 9 for a 9-port switch. Check your device specific data manual to see how many ports your switch contains.

Figure 2-3. Multicast Address Table Entry



For a multicast address table entry, the fields must be set as shown in Table 2-8. General descriptions of the ALE table entry fields are provided in Table 2-14.

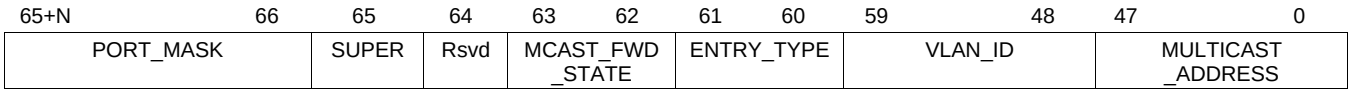
Table 2-8. Multicast Address Table Entry Field Configuration

Field Name	Configuration
PORT_MASK[N-1:0]	User configurable
SUPER	User configurable
MCAST_FWD_STATE[1:0]	User configurable
ENTRY_TYPE[1:0]	01
MULTICAST_ADDRESS[47:0]	User configurable

2.3.7.4.3 VLAN/Multicast Address Table Entry

The format for a VLAN/multicast address table entry is shown in Figure 2-4, and the required field configuration is described in Table 2-9. The variable N below is 5 for a 5-port switch and 9 for a 9-port switch. Check your device specific data manual to see how many ports your switch contains.

Figure 2-4. VLAN/Multicast Table Entry



For a VLAN/multicast address table entry, the fields must be set as shown in Table 2-9. General descriptions of the ALE table entry fields are provided in Table 2-14.

Table 2-9. VLAN/Multicast Address Table Entry Field Configuration

Field Name	Configuration
PORT_MASK[N-1:0]	User configurable
SUPER	User configurable
MCAST_FWD_STATE[1:0]	User configurable
ENTRY_TYPE[1:0]	11
VLAN_ID[11:0]	User configurable
MULTICAST_ADDRESS[47:0]	User configurable

2.3.7.4.4 Unicast Address Table Entry

The format for a unicast address table entry is shown in Figure 2-5, and the required field configuration is described in Table 2-10. The variable N below is 5 for a 5-port switch and 9 for a 9-port switch. Check your device specific data manual to see how many ports your switch contains.

Figure 2-5. Unicast Table Entry

65+N	64+N 66	65	64	63 62	61 60	59 48	47 0
Reserved	PORT _NUMBER	BLOCK	SECURE	UNICAST _TYPE	ENTRY_TYPE	Reserved	UNICAST_ADDRESS

For a unicast address table entry, the fields must be set as shown in Table 2-10. General descriptions of the ALE table entry fields are provided in Table 2-14.

Table 2-10. Unicast Address Table Entry Field Configuration

Field Name	Configuration
PORT_NUMBER[N-2:0]	User configurable
BLOCK	User configurable
SECURE	User configurable
UNICAST_TYPE[1:0]	00 or X1
ENTRY_TYPE[1:0]	01
UNICAST_ADDRESS[47:0]	User configurable

2.3.7.4.5 OUI Unicast Address Table Entry

The format for an OUI unicast address table entry is shown in Figure 2-6, and the required field configuration is described in Table 2-11. The variable N below is 5 for a 5-port switch and 9 for a 9-port switch. Check your device specific data manual to see how many ports your switch contains.

Figure 2-6. OUI Unicast Table Entry

65+N 64	63 62	61 60	59 48	47 24	23 0
Reserved	UNICAST _TYPE	ENTRY_TYPE	Reserved	UNICAST _OUI	Reserved

For an OUI unicast address table entry, the fields must be set as shown in Table 2-11. General descriptions of the ALE table entry fields are provided in Table 2-14.

Table 2-11. OUI Unicast Address Table Entry Field Configuration

Field Name	Configuration
UNICAST_TYPE[1:0]	10
ENTRY_TYPE[1:0]	01
UNICAST_OUI[23:0]	User configurable

2.3.7.4.6 VLAN/Unicast Table Entry

The format for a VLAN/unicast address table entry is shown in Figure 2-7, and the required field configuration is described in Table 2-12. The variable N below is 5 for a 5-port switch and 9 for a 9-port switch. Check your device specific data manual to see how many ports your switch contains.

Figure 2-7. VLAN/Unicast Table Entry

65+N	64+N 66	65	64	63 62	61 60	59 48	47 0
Reserved	PORT_NUMBER	BLOCK	SECURE	UNICAST_TYPE	ENTRY_TYPE	VLAN_ID	UNICAST_ADDRESS

For a VLAN/unicast address table entry, the fields must be set as shown in Table 2-12. General descriptions of the ALE table entry fields are provided in Table 2-14.

Table 2-12. VLAN/Unicast Table Entry Field Configuration

Field Name	Configuration
PORT_NUMBER[N-2:0]	User configurable
BLOCK	User configurable
SECURE	User configurable
UNICAST_TYPE[1:0]	00 or X1
ENTRY_TYPE[1:0]	11
VLAN_ID[11:0]	User configurable
UNICAST_ADDRESS[47:0]	User configurable

2.3.7.4.7 VLAN Table Entry

The format for a VLAN table entry is shown in Figure 2-8, and the required field configuration is described in Table 2-13. The variable N below is 5 for a 5-port switch and 9 for a 9-port switch. Check your device specific data manual to see how many ports your switch contains.

Figure 2-8. VLAN Table Entry

65+N 66	65	64 62	61 60	59 48	47	46 44
NO_LEARN_MASK	VLAN_FORCE_INGRESS_CHECK	000	ENTRY_TYPE	VLAN_ID	Reserved	REG_MCAST_FLOOD_INDEX

43 24+N	23+N 24	23	22 20	19 N	N-1 0
Reserved	FORCE_UNTAGGED_EGRESS	Reserved	UNREG_MCAST_FLOOD_INDEX	Reserved	VLAN_MEMBER_LIST

For a VLAN table entry, the fields must be set as shown in Table 2-13. General descriptions of the ALE table entry fields are provided in Table 2-14.

Table 2-13. VLAN Table Entry Field Configuration

Field Name	Configuration
NO_LEARN_MASK[N-1:0]	User configurable
VLAN_FORCE_INGRESS_CHECK	User configurable
ENTRY_TYPE[1:0]	10
VLAN_ID[11:0]	User configurable
REG_MCAST_FLOOD_INDEX[2:0]	User configurable
FORCE_UNTAGGED_EGRESS[N-1:0]	User configurable
UNREG_MCAST_FLOOD_INDEX[2:0]	User configurable
VLAN_MEMBER_LIST [N-1:0]	User configurable

2.3.7.4.8 ALE Table Entry Field Descriptions

General ALE Table entry field descriptions are shown below in Table 2-14.

Table 2-14. ALE Table Entry Field Descriptions

ALE Table Entry Field Name	Description
ENTRY_TYPE[1:0]	Table Entry Type. • 00 = Free Entry • 01 = Address Entry: unicast or multicast determined by bit 40 of the MAC destination address • 10 = VLAN entry • 11 = VLAN Address Entry: unicast or multicast determined by bit 40 of the MAC destination address
SUPER	Supervisory Packet. Indicates that the packet with a matching multicast destination address is a supervisory packet. • 0 = Non-supervisory packet • 1 = Supervisory packet
PORT_MASK[N-1:0]	Port Mask. This field is the port bit mask that is returned with a found multicast destination address. There may be multiple bits set indicating that the multicast packet may be forwarded to multiple ports (but not the receiving port).
PORT_NUMBER	Port Number. This field indicates which port number (not port mask) that the packet with a unicast destination address may be forwarded. Packets with unicast destination addresses are forwarded only to a single port (but not the receiving port).
BLOCK	Block. The block bit indicates that a packet with a matching source or destination address should be dropped (block the address). • 0 = Address is not blocked. • 1 = Drop a packet with a matching source or destination address (SECURE must be 0) If BLOCK and SECURE are both set, then they no longer mean block and secure. When both are set, the BLOCK and SECURE bits indicate that the packet is a unicast supervisory (SUPER) packet and they determine the unicast forward state test criteria. If both bits are set then the packet is forwarded if the receive port is in the Forwarding/Blocking/Learning state. If both bits are not set then the packet is forwarded if the receive port is in the forwarding state.
SECURE	Secure. This bit indicates that a packet with a matching source address should be dropped if the received port number is not equal to the table entry PORT_NUMBER. • 0 = Received port number is a don't care • 1 = Drop the packet if the received port is not the secure port for the source address and do not update the address (BLOCK must be 0)
UNICAST_TYPE[1:0]	Unicast Type. This field indicates the type of unicast address the table entry contains. • 00 = Unicast address that is not ageable • 01 = Ageable unicast address that has not been touched • 10 = OUI address - lower 24-bits are don't cares (not ageable) • 11 = Ageable unicast address that has been touched
MCAST_FWD_STATE[1:0]	Multicast Forward State. Indicates the port state(s) required for the received port on a destination address lookup in order for the multicast packet to be forwarded to the transmit port(s). A transmit port must be in the Forwarding state in order to forward the packet. If the transmit PORT_MASK has multiple set bits then each forward decision is independent of the other transmit port(s) forward decision. • 00 = Forwarding • 01 = Blocking/Forwarding/Learning • 10 = Forwarding/Learning • 11 = Forwarding The forward state test returns a true value if both the receive and transmit ports are in the required state.
VLAN_ID	VLAN_ID. This is the 12-bit VLAN ID.
VLAN_FORCE_INGRESS_CHECK	VLAN Force Ingress Check – If the receive port is not a member of this VLAN the packet is dropped. This is similar to the VID_INGRESS_CHECK bit in the ALE_PORTCTL *n* register except this check is for this VLAN only (not all VLANs).
NO_LEARN_MASK	No Learn Mask – When a bit is set in this mask, a packet with an unknown source address received on the associated port will not be learned (i.e. When a VLAN packet is received and the source address is not in the table, the source address will not be added to the table).

Table 2-14. ALE Table Entry Field Descriptions (continued)

ALE Table Entry Field Name	Description
ADDRESS	Packet Address. This is the 48-bit packet MAC address. For an OUI address, only the upper 24-bits of the address are used in the source or destination address lookup. Otherwise, all 48-bits are used in the lookup.
VLAN_MEMBER_LIST	VLAN Member List. This six bit field indicates which port(s) are a member of the associated VLAN.
UNREG_MCAST_FLOOD_INDEX	Unregistered Multicast Flood Index. Index into ALE_VLAN_MASK_MUX *n* register array that is used to create the unregistered multicast flood mask. The flood mask is used for multicast when the multicast address is not found.
REG_MCAST_FLOOD_INDEX	Registered Multicast Flood Index. Index into ALE_VLAN_MASK_MUX *n* register array that is used to create the registered multicast flood mask. The flood mask is used for multicast when the multicast address is found.
FORCE_UNTAGGED_EGRESS	Force Untagged Packet Egress. Causes the packet VLAN tag to be removed on egress.

2.3.7.5 ALE Packet Forwarding Process

This section describes the packet forwarding process used by the ALE. For each packet sent to the ALE, it will decide whether or not the packet should be dropped or forwarded. If the packet is forwarded, then the ALE needs to determine which switch port or ports a packet the should be forwarded to. Each port has an associated packet forwarding state that can be set to one of four values:

- Disabled
- Blocked
- Learning
- Forwarding

By default, all ports are disabled. To enable a port, the host must set the packet forwarding state in the respective ALE_PORTCTL register. The receive packet processes are described in the following sections. The state of each port will affect whether or not a packet is forwarded.

There are four processes that an packet may go through to determine packet forwarding. The processes are:

- Ingress Filtering
- VLAN Aware Lookup
- VLAN Unaware Lookup
- Egress

The packet forwarding process begins with the ingress filtering process. In the packet ingress process, there is one forward state test for unicast destination addresses, and another forward state test for multicast addresses. The forward state test that is used is determined by bit 40 of the destination address in the packet, which will designate the packet as multicast or unicast.The multicast forward state test indicates the port states required for the receiving port in order for the multicast packet to be forwarded to the transmit port(s). A transmit port must be in the Forwarding state for the packet to be forwarded for transmission. The MCAST_FWD_STATE indicates the required port state for the receiving port as indicated in the ALE table entry field descriptions above.

The unicast forward state test indicates the port state required for the receiving port in order to forward the unicast packet. The transmit port must be in the Forwarding state in order to forward the packet. The block and secure bits determine the unicast forward state test criteria. If both bits are set then the packet is forwarded if the receive port is in the Forwarding/Blocking/Learning state. If both bits are not set then the packet is forwarded if the receive port is in the Forwarding state. The transmit port must be in the Forwarding state regardless.

In general, packets received with errors are dropped by the address lookup engine in the ingress filtering process without learning, updating, or touching the addresses in the ALE table. The error condition and the abort are indicated by the ingress port to the ALE. Packets with errors may be passed to the host (not aborted) by a n ingress port if the RX_CMF_EN, RX_CEF_EN, or RX_CSF_EN bit(s) have been set in the P *n* _MAC_CTL register in the MAC module. Error packets that are passed to the host by the ingress port are considered to be bypass packets by the ALE and are sent only to the host. Error packets do not learn, update, or touch addresses in the ALE table regardless of whether they are aborted or sent to the host. Packets with long or short errors received by the host are dropped. The host will pass packets with CRC errors to the Ethernet ports.

- RX_CEF_EN – This bit in the P *n* _MAC_CTL register enables frames that are fragments, long, jabber, CRC, code, and alignment errors to be forwarded
- RX_CSF_EN – This bit in the P *n* _MAC_CTL register enables short frames to be forwarded
- RX_CMF_EN – This bit in the P *n* _MAC_CTL register enables MAC control frames to be forwarded.

If RX_CEF_EN, RX_CSF_EN, RX_CMF_EN bits are enabled in the configuration, then the packets that are sent with the errors that correspond to these flags' descriptions (i.e., these bits) will be copied to memory. Their corresponding error flag in the descriptor will be enabled.

2.3.7.5.1 Switch Ingress Filtering Process

This section outlines the switch ingress packet filtering process.

Table 2-15. Switch Ingress Filtering Process

if ((ALE_BYPASS) AND (host port is not the receive port)) then use host portmask and go to Egress process (ALE_BYPASS is found in the ALE_CONTROL register)
if (directed packet) then use directed port number and go to Egress process (directed packets originate only from the host port and have the TO_PORT bits set in their descriptor)
If (Receive PORT_STATE is Disabled) then discard the packet (PORT_STATE is found in the ALE_PORTCTLn Register where n is the receive port number)
if ((error packet) AND (host port is not the receive port)) then use host portmask and go to Egress process
if (((unicast source address found in an ALE table entry) AND (BLOCK bit is set in that found table entry)) OR ((unicast destination address found in an ALE table entry) AND (BLOCK bit is set in that found table entry))) then discard the packet
if ((broadcast/multicast rate limit enabled) AND (rate limit exceeded) AND (rate limits are receive port based) then if (((multicast or broadcast destination address found in an ALE table entry) AND (not SUPER in that entry)) OR (multicast/broadcast destination address not found in an ALE table entry)) then discard the packet (bcast/mcast rate limit enabling is controlled by the EN_RL bit of the ALE_CONTROL Register) (the bcast/mcast rate limits are set for each port in the ALE_PORTCTLn Register) (rate limits can be RX port or TX port based determined by the RL_TX bit in the ALE_CONTROL Register)
if ((not forward state test valid) AND (destination address found)) then discard the packet for any port not meeting the requirements (unicast destination addresses use the unicast forward state test and multicast destination addresses use the multicast forward state test. Both tests are described above in Section 2.3.7.5.
if ((destination address not found in an ALE table entry) AND ((not transmit port forwarding) OR (not receive port forwarding))) then discard the packet to any ports not meeting the above requirements

Table 2-15. Switch Ingress Filtering Process (continued)

if (source address found in an ALE table entry) AND (SECURE bit is set in that table entry) AND (receive port number! = PORT_NUMBER from that same table entry)) then discard the packet
if ((not a supervisory packet) AND (DROP_UNTAGGED) AND ((non-tagged packet) or ((priority tagged) AND not(EN_VID0_MODE)) then discard the packet (supervisory packets are multicast packets found in an ALE table entry with their SUPER bit set, broadcast packets found in an ALE table entry with their SUPER bit set, or unicast packets found in an ALE table entry with both the BLOCK and SECURE bits set) (DROP_UNTAGGED is set in the ALE_PORTCTLn register where n is the receiving port) (priority tagged packets are packets that contain a VLAN header only for the priority bits and have a VID of 0) (EN_VID0_MODE is found in the ALE_CONTROL register)

If (VLAN_Unaware)
FORCE_UNTAGGED_EGRESS = "000000"
REG_MCAST_FLOOD_MASK = "111111"
UNREG_MCAST_FLOOD_MASK = "111111"
VLAN_MEMBER_LIST = "111111"
else if (matching VLAN table entry NOT found that matches the incoming packets VLAN ID)
FORCE_UNTAGGED_EGRESS = ALE_UNKN_VLAN_FORCE_UNTAG_EGR register
REG_MCAST_FLOOD_MASK = ALE_UNKN_VLAN_REG_MLT_FLOOD register
UNREG_MCAST_FLOOD_MASK = ALE_UNKN_VLAN_UNREG_MLT_FLOOD register
VLAN_MEMBER_LIST = ALE_UNKN_VLAN_MBR_LIST register
else #a matching VLAN table entry is found that matches the incoming packets VLAN ID
FORCE_UNTAGGED_EGRESS = FORCE_UNTAGGED_EGRESS field from the matching VLAN table entry
REG_MCAST_FLOOD_MASK = REG_MCAST_FLOOD_MASK field from the matching VLAN table entry
UNREG_MCAST_FLOOD_MASK = UNREG_MCAST_FLOOD_MASK field from the matching VLAN table entry
VLAN_MEMBER_LIST = VLAN_MEMBER_LIST field from the matching VLAN table entry
(VLAN Unaware means that VLAN_AWARE = 0 in the CPSW_CONTROL register and ALE_VLAN_AWARE = 0 in the ALE_CONTROL register)
(the four values on the left side of these equations are used throughout the remaining lookup process as well as the egress process; all packets match one of the above cases during switch ingress)

IF ((not a supervisory packet) AND (VID_INGRESS_CHECK) AND (the receive port is not in the VLAN_MEMBER_LIST)) then discard the packet (supervisory packets are multicast packets found in an ALE table entry with their SUPER bit set, broadcast packets found in an ALE table entry with their SUPER bit set, or unicast packets found in an ALE table entry with both the BLOCK and SECURE bits set) (VID_INGRESS_CHECK is set in the ALE_PORTCTLn register) (the VLAN_MEMBER_LIST is set in the step above)
if ((the ALE is in MAC authorization mode) AND (source address is not found in an ALE table entry) AND NOT ((destination address found in an ALE table entry) AND (SUPER bit set in that entry))) then discard the packet (the EN_AM bit in the ALE_CONTROL register controls whether or not the ALE is in MAC authorization mode)
if (destination address equals source address) then discard the packet
if (VLAN_AWARE) go to VLAN aware lookup process else go to VLAN unaware lookup process (VLAN_AWARE means that the VLAN_AWARE bit is set in the CPSW_CONTROL register as well as the ALE_VLAN_AWARE bit in the ALE_CONTROL register)

2.3.7.5.2 ALE VLAN Aware Lookup Process

This section describes the behavior of the ALE VLAN aware lookup process.

Table 2-16. ALE VLAN Aware Lookup Process

if ((unicast packet) AND (destination address matches an ALE unicast entry address OR destination address and VLAN matches an ALE unicast/VLAN entry) AND (not a supervisory packet)) then portmask is the logical "AND" of the PORT_NUMBER from the matching ALE entry and the VLAN_MEMBER_LIST and go to Egress process (supervisory packets are multicast packets found in an ALE table entry with their SUPER bit set, broadcast packets found in an ALE table entry with their SUPER bit set, or unicast packets found in an ALE table entry with both the BLOCK and SECURE bits set)
if ((unicast packet) AND (destination address matches an ALE unicast entry address OR destination address and VLAN matches an ALE unicast/VLAN entry) AND (packet is a supervisory packet)) then portmask is the PORT_NUMBER from the matching ALE entry and go to Egress process (supervisory packets are multicast packets found in an ALE table entry with their SUPER bit set, broadcast packets found in an ALE table entry with their SUPER bit set, or unicast packets found in an ALE table entry with both the BLOCK and SECURE bits set)
if (unicast packet) #destination address not found to match an ALE unicast or unicast/VLAN table entry then use VLAN_MEMBER_LIST excluding the host port (if UNI_FLOOD_TO_HOST is not set) and go to Egress process (the UNI_FLOOD_TO_HOST bit is in the ALE_CONTROL register. If UNI_FLOOD_TO_HOST is set to 1 then the host port is not excluded from the port mask and depending on the VLAN_MEMBER_LIST the packets may be forwarded to the host. If UNI_FLOOD_TO_HOST is cleared to 0 then unicast packets that do not match a ALE table entry are never forwarded to the host port)
if ((multicast packet) AND (destination address matches an ALE multicast entry address OR destination address and VLAN matches an ALE multicast/VLAN entry) AND (not a supervisory packet)) then portmask is the logical "AND" of REG_MCAST_FLOOD_MASK and the PORT_MASK from the matching multicast or multicast/VLAN table entry and VLAN_MEMBER_LIST and go to Egress process (supervisory packets are multicast packets found in an ALE table entry with their SUPER bit set, broadcast packets found in an ALE table entry with their SUPER bit set, or unicast packets found in an ALE table entry with both the BLOCK and SECURE bits set)
if ((multicast packet) AND (destination address matches an ALE multicast entry address OR destination address and VLAN matches an ALE multicast/VLAN entry) AND (packet is a supervisory packet)) then portmask is the PORT_MASK from the matching multicast or multicast/VLAN table entry and go to Egress process (supervisory packets are multicast packets found in an ALE table entry with their SUPER bit set, broadcast packets found in an ALE table entry with their SUPER bit set, or unicast packets found in an ALE table entry with both the BLOCK and SECURE bits set)
if ((multicast packet) #destination address not found to match an ALE multicast or multicast/VLAN table entry then portmask is the logical "AND" of UNREG_MCAST_FLOOD_MASK and VLAN_MEMBER_LIST then go to Egress process
if (broadcast packet) then use VLAN_MEMBER_LIST and go to Egress process

2.3.7.5.3 ALE VLAN Unaware Lookup Process

This section describes the behavior of the ALE VLAN unaware lookup process.

Table 2-17. ALE VLAN Unaware Lookup Process

if ((unicast packet) AND (destination address matches an ALE unicast entry address OR destination address and VLAN matches an ALE unicast/VLAN entry) AND (not a supervisory packet)) then portmask is the logical "AND" of the PORT_NUMBER from the matching ALE entry and the VLAN_MEMBER_LIST and go to Egress process (supervisory packets are multicast packets found in an ALE table entry with their SUPER bit set, broadcast packets found in an ALE table entry with their SUPER bit set, or unicast packets found in an ALE table entry with both the BLOCK and SECURE bits set)
if ((unicast packet) AND (destination address matches an ALE unicast entry address OR destination address and VLAN matches an ALE unicast/VLAN entry) AND (packet is a supervisory packet)) then portmask is the PORT_NUMBER from the matching ALE entry and go to Egress process (supervisory packets are multicast packets found in an ALE table entry with their SUPER bit set, broadcast packets found in an ALE table entry with their SUPER bit set, or unicast packets found in an ALE table entry with both the BLOCK and SECURE bits set)
if (unicast packet) # destination address not found to match an ALE unicast or unicast/VLAN table entry then use VLAN_MEMBER_LIST excluding the host port (if UNI_FLOOD_TO_HOST is not set) and go to Egress process (the UNI_FLOOD_TO_HOST bit is in the ALE_CONTROL register. If UNI_FLOOD_TO_HOST is set to 1 then the host port is not excluded from the port mask and depending on the VLAN_MEMBER_LIST the packets may be forwarded to the host. If UNI_FLOOD_TO_HOST is cleared to 0 then unicast packets that do not match a ALE table entry are never forwarded to the host port)
if ((multicast packet) AND (destination address matches an ALE multicast entry address OR destination address and VLAN matches an ALE multicast/VLAN entry) AND (not a supervisory packet)) then portmask is the logical "AND" of REG_MCAST_FLOOD_MASK and the PORT_MASK from the matching multicast or multicast/VLAN table entry and VLAN_MEMBER_LIST and go to Egress process (supervisory packets are multicast packets found in an ALE table entry with their SUPER bit set, broadcast packets found in an ALE table entry with their SUPER bit set, or unicast packets found in an ALE table entry with both the BLOCK and SECURE bits set)
if ((multicast packet) AND (destination address matches an ALE multicast entry address OR destination address and VLAN matches an ALE multicast/VLAN entry) AND (packet is a supervisory packet)) then portmask is the PORT_MASK from the matching multicast or multicast/VLAN table entry and go to Egress process (supervisory packets are multicast packets found in an ALE table entry with their SUPER bit set, broadcast packets found in an ALE table entry with their SUPER bit set, or unicast packets found in an ALE table entry with both the BLOCK and SECURE bits set)
if ((multicast packet) # destination address not found to match an ALE multicast or multicast/VLAN table entry then portmask is the logical "AND" of UNREG_MCAST_FLOOD_MASK and VLAN_MEMBER_LIST then go to Egress process
if(broadcast packet) then use VLAN_MEMBER_LIST and go to Egress process

2.3.7.5.4 ALE Egress Process

This section describes behavior of the ALE egress process.

Table 2-18. ALE Egress Process

Clear receive port from portmask (don’t send packet to receive port)
Clear disabled ports from portmask
if ((EN_OUI_DENY) AND (OUI source address not found) AND (not ALE_BYPASS) AND (not error packet) AND (not a supervisory packet)) then clear host port from portmask (EN_OUI_DENY is found in the ALE_CONTROL) (supervisory packets are multicast packets found in an ALE table entry with their SUPER bit set, broadcast packets found in an ALE table entry with their SUPER bit set, or unicast packets found in an ALE table entry with both the BLOCK and SECURE bits set)
if ((not ENABLE_OUI_DENY) AND (OUI source address found) AND (not ALE_BYPASS) AND (not error packet) AND (not a supervisory packet)) then clear host port from portmask (EN_OUI_DENY is found in the ALE_CONTROL) (supervisory packets are multicast packets found in an ALE table entry with their SUPER bit set, broadcast packets found in an ALE table entry with their SUPER bit set, or unicast packets found in an ALE table entry with both the BLOCK and SECURE bits set)
if ((ENABLE_RATE_LIMIT) AND (RATE_LIMIT_TX)) then if (not a supervisory packet) AND (rate limit exceeded on any tx port) then clear rate limited tx port from portmask
if (portmask is 0) then discard packet
Send packet to portmask ports

2.3.7.6 ALE Learning Process

The learning process is applied to each receive packet that is not aborted. The learning process is a concurrent process with the packet forwarding process.

Table 2-19. ALE Learning Process

If (directed) then do not learn, update, or set TOUCHED else continue (directed packets originate only from the host port and must have the TO_PORT bits set in its descriptor)
If (NOT (Learning or Forwarding) OR (EN_AM) OR (packet error) OR (NO_LEARN)) then do not learn or update address else continue (EN_AM is found in the ALE_CONTROL register) (NO_LEARN is found in the ALE_PORTCTLn register where n is the port where the packet entered the switch)
if ((Non-tagged packet) AND (DROP_UNTAGGED)) then do not learn or update address else continue (DROP_UNTAGGED is found in the ALE_PORTCTLn register where n is the port where the packet entered the switch)
if ((VLAN_AWARE) AND (packet VLAN ID does not match a VLAN table entry) AND (UNKNOWN_VLAN_MEMBER_LIST = "00...0")) then do not learn or update address else continue (VLAN_AWARE means that the VLAN_AWARE bit in the CPSW_CONTROL register as well as the ALE_VLAN_AWARE bit are bot set to 1)
if ((VID_INGRESS_CHECK) AND (Receive port is not in VLAN_MEMBER_LIST) AND (packet VLAN ID matches a VLAN table entry)) then do not learn or update address else continue (VID_INGRESS_CHECK is found in the ALE_PORTCTLn register where n is the port where the packet entered the switch)
if ((source address matches unicast or unicast/VLAN table entry) AND (receive port number != PORT_NUMBER from the matching table entry) AND (SECURE or BLOCK)) then do not update address else continue
if ((source address matches a table entry) AND (receive port number != PORT_NUMBER)) then update address else continue
if ((source address matches unicast or unicast/VLAN table entry) AND (AGEABLE) AND (not TOUCHED)) then set TOUCHED else continue (AGEABLE and TOUCHED are set in the unicast type field of the ALE table entry)
if ((source address does not match an ALE table entry) AND (VLAN_AWARE) AND NOT (LEARN_NO_VID)) then learn address with VLAN (VLAN_AWARE means that the VLAN_AWARE bit in the CPSW_CONTROL register as well as the ALE_VLAN_AWARE bit are bot set to 1) (LEARN_NO_VID is found in the ALE_CONTROL register)
if ((source address does not match an ALE table entry) AND ((not VLAN_AWARE) OR (VLAN_AWARE AND LEARN_NO_VID))) then learn address without VLAN (VLAN_AWARE means that the VLAN_AWARE bit in the CPSW_CONTROL register as well as the ALE_VLAN_AWARE bit in the ALE_CONTROL register are bot set to 1) (LEARN_NO_VID is found in the ALE_CONTROL register)

2.3.8 Error Correction Code (ECC) Submodule Architecture

The ECC submodule uses error detection and correction logic on the packet headers of the packets while they are inside the GbE switch. The ECC submodule uses a shared register interface for the status and control registers of the ECC RAMs that are being protected. The ECC_VECTOR Register is used to select which ECC RAM the status and control registers are currently reading from or writing to (see Table 2-20 as well as the ECC_VECTOR register in the Registers section). The ECC_ENABLE bit in the ECC_CTL register is not used (ECC is always enabled). The GbE Switch FIFO RAMS implement ECC only on packet headers. The packet data is protected by Castignoli CRC while being passed between the FIFOs inside the GbE switch (regardless of the input packet CRC type or output CRC type). The ALE RAM has complete ECC.

Table 2-20. ECC Submodule RAMs

RAM Number	RAM Purpose
0	ALE RAM (Complete ECC)
1	Port 0 RX FIFO RAM (ECC on packet headers only)
2	Port 0 TX FIFO RAM (ECC on packet headers only)
3	Port 1 RX FIFO RAM (ECC on packet headers only)
4	Port 1 TX FIFO RAM (ECC on packet headers only)
5	Port 2 RX FIFO RAM (ECC on packet headers only)
6	Port 2 TX FIFO RAM (ECC on packet headers only)
7	Port 3 RX FIFO RAM (ECC on packet headers only)
8	Port 3 TX FIFO RAM (ECC on packet headers only)
9	Port 4 RX FIFO RAM (ECC on packet headers only)
10	Port 4 TX FIFO RAM (ECC on packet headers only)
11	Port 5 RX FIFO RAM (ECC on packet headers only)
12	Port 5 TX FIFO RAM (ECC on packet headers only)
13	Port 6 RX FIFO RAM (ECC on packet headers only)
14	Port 6 TX FIFO RAM (ECC on packet headers only)
15	Port 7 RX FIFO RAM (ECC on packet headers only)
16	Port 7 TX FIFO RAM (ECC on packet headers only)
17	Port 8 RX FIFO RAM (ECC on packet headers only)
18	Port 8 TX FIFO RAM (ECC on packet headers only)

2.3.8.1 Packet Header ECC

Only packet header bits are protected by the ECC submodule in the GbE switch RAMs. The ECC_ROW field in the ECC_ERR_CTRL1 register is not implemented – the ECC_BIT1 field is implemented to determine which bit of the packet header is flipped for a single bit error (SEC) when the ECC_CRC_MODE bit is cleared to 0 in the CPSW_CONTROL register.

The ECC status registers return the RAM address that was flipped (ECC_ROW field in the ECC_ERR_STATUS1 register) along with the bit position of the error (ECC_BIT1 value in the ECC_ERR_STATUS2 register). Forcing double bit errors in testing can cause indeterminate switch operation if multiple used packet header bits are flipped given that only single-bit errors are fixed by the ECC logic. Header bits 207 down to 200 are not currently used in the switch and may be used to test double-bit errors without the possibility of requiring a reset for the switch to recover from the double-bit error. No header bits are flipped when ECC_CRC_MODE is set to 1 in the CPSW_CONTROL register.

The packet header is 256 bits (see Table 2-21). The header data is stored in bits 207 down to 0 and the header ECC code is stored in bits 255 down to 208. If any bit is flipped in the ECC code, the flipped bit will be corrected, but the index of the flipped bit will be reported as bit zero in the ECC_BIT1 value of the ECC_ERR_STATUS2 register. This implies that when the ECC submodule reports that there is a single-bit error (SEC) on 'bit 0', it can mean two things: either SEC on data bit 0 or SEC somewhere inside the ECC code.

2.3.8.2 Packet Protect CRC

Each packet received without error is passed through the switch memories with a generated Castignoli protect CRC. The protect CRC is checked on switch egress for correctness and removed. If the CRC is correct (no RAM bit errors), then the packet is output with the selected port CRC type. If a protect CRC error is detected on host egress then the TXST_DROP signal will be asserted so that the packet is dropped to the host. If a protect CRC error is detected on Ethernet egress then the egress CRC will be generated on the packet and at least one byte of the CRC will be inverted on output. CRC memory protect errors do not assert the ECC_INTR signal. CRC memory protect errors are counted in the associated port statistics registers and issue an interrupt on STAT_PEND if any CRC memory protect error occurs (and the statistics for that port are enabled).

When the ECC_CRC_MODE bit in the CPSW_CONTROL register is set to 1, the ECC submodule will flip the associated column bit in any FIFO memory data read operation, inducing a CRC protect error when the protect CRC is checked. In this mode, errors detected in the packet headers will introduce errors in the corresponding packet data which will cause CRC protect errors. No packet header bits are flipped when ECC_CRC_MODE is set to 1.

2.3.8.3 ECC Submodule RAM Control

The ECC logic for each FIFO ram (receive and transmit) is divided into eight separate ECC encoders/decoders that encode/decode 26 bits of data each. Each of the eight encoders (0 to 7) generates 6 bits of ECC code (48 code bits total), and each of the eight decoders (0 to 7) checks 6 bits of ECC code across the 26-bits of data (208 data bits total). The 48 bits of ECC code are passed through the ram in the upper 48 unused bits in the header word. The header data bits and ECC code bits are shown in Table 2-21. The ecc_bit1[15:0] value returned on error is a 16-bit value that is the concatenation of 5 bits of 0, 3-bits of the encoder/decoder number (0 to 7), 3 bits of 0, and 5 bits of index into the indicated 26-bit encoder/decoder. For example, an ecc_bit1 value of 0x0308 is bit 8 of encoder/decoder 3, which is header bit 86 (((26*3) + 8).

Table 2-21. ECC Submodule Header Data Bit to Encoder/Decoder Mapping

Header Data Bits	Encoder/Decoder
25:0	Encoder/Decoder 0 Data
51:26	Encoder/Decoder 1 Data
77:52	Encoder/Decoder 2 Data
103:78	Encoder/Decoder 3 Data
129:104	Encoder/Decoder 4 Data
155:130	Encoder/Decoder 5 Data
181:156	Encoder/Decoder 6 Data
207:182	Encoder/Decoder 7 Data
213:208	Encoder/Decoder 0 ECC
219:214	Encoder/Decoder 1 ECC
225:220	Encoder/Decoder 2 ECC
231:226	Encoder/Decoder 3 ECC
237:232	Encoder/Decoder 4 ECC
243:238	Encoder/Decoder 5 ECC
249:244	Encoder/Decoder 6 ECC
255:250	Encoder/Decoder 7 ECC

2.3.8.4 ECC Submodule Registers

There are three types of register accesses in the ECC submodule:

- Global registers that are common to all ECC RAMs - This includes the ECC_REVISION and ECC_VECTOR registers. Every ECC RAM serviced by the ECC module is assigned a unique ID by the module (see Table 2-20). Writing this ID to the ECC_VECTOR register selects the ECC RAM to be controlled or read the ECC status from.
- ECC control and status registers -These are specific to each ECC RAM and selected by the RAM ID written to the ECC_VECTOR register. The accesses to these registers are done using shared registers. Note that due to the long latencies on the shared registers, the reads to the ECC control and status registers are triggered by a write to the ECC_VECTOR register. This is described below.
- Interrupt registers -These include the standard interrupt status, interrupt enable, clear and end of interrupt registers. These are also discussed below.

2.3.8.4.1 Reading Shared ECC Submodule Registers

Due to the long latencies, on the order of several thousands of clock cycles, while using the shared registers, the reads to the ECC control and status registers for each ECC RAM are triggered by writing a “read” message to the ECC_VECTOR register as described below:

1. Software writes the ECC_VECTOR (RAM ID), TRIGGER_READ, and READ_ADDRESS bits in the ECC_VECTOR register. The READ_ADDRESS corresponds to any of the ECC control or status registers which require the use of shared registers. The ECC_VECTOR register description explains the READ_ADDRESS field (see Section 3.5.6.2).
2. Software then polls the READ_DONE bit ECC_VECTOR register to check if it is 1. This indicates that the read operation has completed and the shared register is ready.
3. Software reads the data from the ECC control or status register that was requested. Read data is returned the following clock cycle.

2.3.8.4.2 Writing Shared ECC Submodule Registers

Due to the use of shared registers for the control and status registers of the ECC RAMs writing to a register is a two-step process:

1. Software writes the ECC_VECTOR (RAM ID) bits in the ECC_VECTOR register corresponding to the ECC RAM that the user wishes to control.
2. Software then writes the data to the ECC control or status register for the ECC RAM that was selected in the ECC_VECTOR register.

2.3.8.4.3 ECC Submodule Interrupts

The ECC submodule aggregates all the level pending status from the ECC RAMs to a single end of interrupt (EOI) handshake based interrupt to the host. Software is expected to follow the sequence described below:

1. Software enables the interrupts for the ECC RAM(s) by writing to the Interrupt Enable register (ECC_INT_EN_SET register).
2. On receiving an interrupt, software checks the Interrupt Status register (ECC_INT_STATUS register) to see which ECC RAM(s) caused the error.

NOTE: The interrupt status read is not a read to a shared register. The ECC_INT_STATUS register can be read directly.

3. Software uses the method described above (see Section 2.3.8.4.1) to read the ECC_ERR_STATUS1 register and will need to use the same method again if a read to the ECC_ERR_STATUS2 register is necessary.
4. After the interrupt has been serviced, software will clear the interrupt status by writing to bits 8, 9 or 10 of the ECC_ERR_STATUS1 register depending on the type of ECC error as specified by bits 0, 1, and 2 in the same register.

NOTE: Software has to poll the ECC_ERR_STATUS1 register to guarantee that the status bit has been cleared. Otherwise there is no indication that the write has actually completed because of the nature of the shared registers.

5. Software will write to the end of interrupt register (ECC_EOI) to clear the interrupt.

2.4 Serial Gigabit Media Independent Interface (SGMII) Architecture

This section provides an overview of the SGMII architecture. The main function of this module is to translate between the GMII data format used by the Ethernet MAC module and the 8B/10B encoded data format used by the SerDes module. The SGMII module is also responsible for establishing a link and autonegotiating with other devices. This section will cover the receive interface, the transmit interface, and several configurations for connecting to other PHY or SGMII devices.

2.4.1 SGMII Receive Interface

The SGMII receive interface converts the 8B/10B encoded receive input from the SerDes into the GMII signals required by the MAC module.

2.4.2 SGMII Transmit Interface

The SGMII transmit interface converts the GMII input data from the MAC module into the 8B/10B encoded output required by the SerDes module. The MAC module does not source the transmit error signal. Any transmit frame from the MAC with an error will be indicated as an error. Transmit error is assumed to be zero at all times, and is not input to the CRC module.

When operating in 10/100 mode, the GMII_MTXD(7:0) data bus uses only the lower nibble.

Any packet in data transmission from the Ethernet MAC while the link signal is deasserted will be ignored. Only packets that begin after the rising edge of link will be transferred.

2.4.3 Modes of Operation

This section describes the modes of operation supported by the SGMII module.

2.4.3.1 Digital Loopback

This section describes the loopback mode supported by the SGMII, and give instructions on how to configure the SGMII module in loopback mode.

The SGMII module supports the ability to internally connect the transmit signals to the receive signals. It is important to note that this is digital loopback, because the transmit and receive signals are connected before reaching the SerDes module. When in this configuration, the transmit clock (TX_CLK) is used for transmit and receive clocking. Loopback mode can be entered by asserting the LOOPBACK bit in the SGMII_CONTROL register. When entering or exiting loopback mode, it is important to reset the transmit and receive logic using the RT_SOFT_RESET bit in the SOFT_RESET register.

The sequence for entering or exiting loopback mode is shown in Procedure 2-3.

2.4.3.1.1 Digital Loopback Configuration

Step 1. Clear to 0 the MR_AN_ENABLE bit in the SGMII_CONTROL register.

Step 2. Write to 1 the RT_SOFT_RESET bit in the SGMII_SOFT_RESET register.

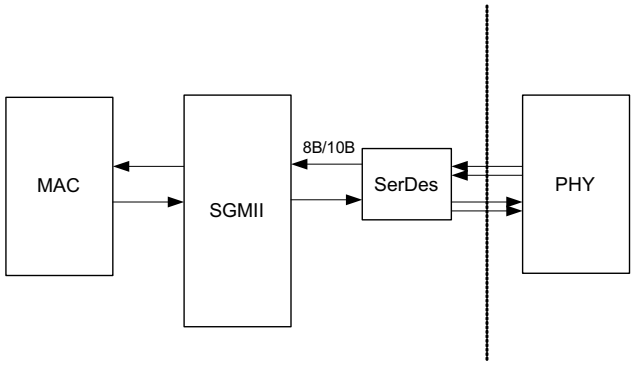
Step 3. Write to 1 the LOOPBACK bit in the SGMII_CONTROL register.

Step 4. Write to zero the RT_SOFT_RESET bit in the SGMII_SOFT_RESET register.

2.4.3.2 SGMII to PHY Configuration

This section describes how to configure the SGMII to connect with an external PHY when operating SGMII mode. Figure 2-9 shows an example of this configuration.

Figure 2-9. SGMII Mode with PHY Configuration



To connect with an external PHY, the PHY will be the master, and the SGMII module needs to be configured in slave mode. The procedure for setting the SGMII in slave mode is shown below:

Step 1. Set up the SGMII and enable autonegotiation:

a. Set bit 0 of the SGMII_MR_ADV_ABILITY register

```
SGMII_MR_ADV_ABILITY &=0xFFFF0000; /* Clear the register contents */
SGMII_MR_ADV_ABILITY |= 0x00000001;
```

b. Enable auto-negotiation by setting the MR_AN_ENABLE bit in the SGMII_CONTROL register:

```
SGMII_CONTROL |= 0x00000001; /* Enable autonegotiation */
```

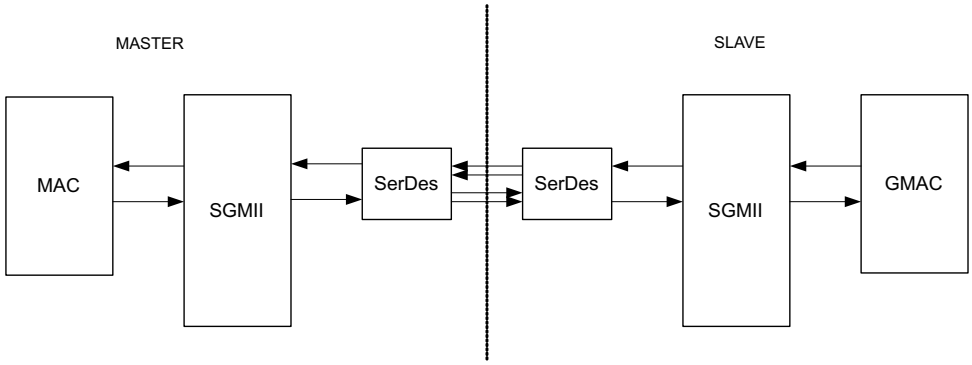
Step 2. Poll the SGMII_STATUS register to determine when auto-negotiation is complete without error. The AN_ERROR bit in the SGMII_STATUS register will be set if the mode was commanded to be half-duplex gigabit.

Step 3. In the MAC module, set the EXT_EN bit in the Pn_MAC_CTL register to allow the speed and duplex mode to be set by the signals from the SGMII.

2.4.3.3 SGMII to SGMII with Auto-Negotiation Configuration

This section describes how to configure an SGMII device to connect with another SGMII device with auto-negotiation. The diagram below shows an example of this configuration.

Figure 2-10. SGMII Master to SGMII Slave with Auto-Negotiation Configuration



When connecting two SGMII devices with auto-negotiation, one SGMII device must be configured as the master, and the other SGMII device must be configured as the slave.

2.4.3.3.1 SGMII Master Mode with Auto-Negotiation

The procedure for setting the SGMII in master mode with auto-negotiation is shown below:

Step 1. Set up the SGMII and enable auto-negotiation:

a. Set the SGMII_MR_ADV_ABILITY register

```
SGMII_MR_ADV_ABILITY |= 0x00009801; /* Full duplex gigabit configuration */
SGMII_MR_ADV_ABILITY &= 0xFFFF0000; /*Clear the register contents */
```

b. Enable auto-negotiation by setting the MR_AN_ENABLE bit in the SGMII_CONTROL register:

```
SGMII_CONTROL |= 0x00000021; /* Master Mode with autonegotiation enabled */
```

Step 2. Poll the LINK and MR_AN_COMPLETE bits in the SGMII_STATUS register to determine when the link is up and auto-negotiation is complete.

Step 3. In the MAC module, the user can optionally set the EXT_EN bit in the Pn_MAC_CTL register to allow the speed and duplex mode to be set by the signals from the SGMII.

2.4.3.3.2 SGMII Slave Mode with Auto-Negotiation

The procedure for setting the SGMII in slave mode with auto-negotiation is shown below:

Step 1. Set up the SGMII and enable auto-negotiation:

a. Set the SGMII_MR_ADV_ABILITY register

```
SGMII_MR_ADV_ABILITY &= 0xFFFF0000; /*Clear the register contents*/
SGMII_MR_ADV_ABILITY |= 0x00000001;
```

b. Enable auto-negotiation by setting the MR_AN_ENABLE bit in the SGMII_CONTROL register:

```
SGMII_CONTROL |= 0x00000001; /* Enable auto-negotiation */
```

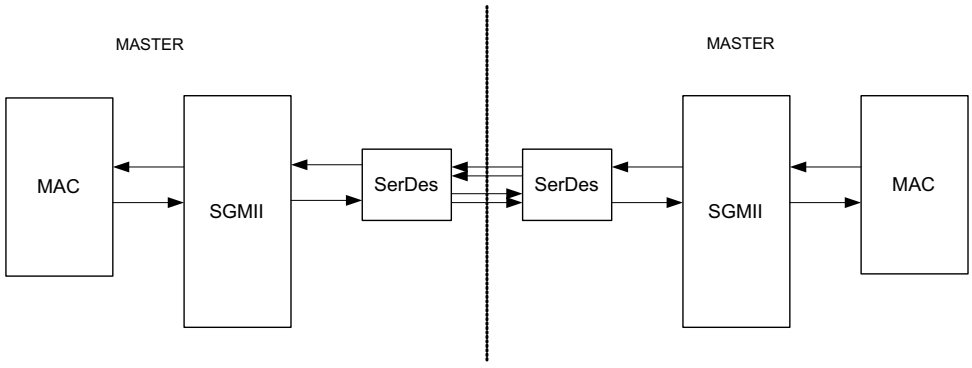
Step 2. Poll the SGMII_STATUS register to determine when auto-negotiation is complete without error. The AN_ERROR bit in the SGMII_STATUS register will be set if the mode was commanded to be half-duplex gigabit.

Step 3. In the MAC module, set the EXT_EN bit in the Pn_MAC_CTL register to allow the speed and duplex mode to be set by the signals from the SGMII.

2.4.3.4 SGMII to SGMII with Forced Link Configuration

This section describes how to configure an SGMII device to connect with another SGMII device with a forced link. in Figure 2-11 shows an example of this configuration.

Figure 2-11. SGMII Master to SGMII Master with Forced Link Configuration



When connecting two SGMII devices with forced link, both SGMII devices must be configured as masters.

The procedure for setting the SGMII in master mode with forced link is shown below:

Step 1. Setup the SGMII:

a. Set the SGMII_MR_ADV_ABILITY register

```
SGMII_MR_ADV_ABILITY &= 0xFFFF0000; /* Clear the register contents */
SGMII_MR_ADV_ABILITY |= 0x00009801; /* Full duplex gigabit configuration */
```

b. Set the device in master mode without auto-negotiation by setting the MASTER bit in the SGMII_CONTROL register:

```
SGMII_CONTROL |= 0x00000020; /* Master Mode, no auto-negotiation */
```

Step 2. Poll the LINK bit in the SGMII_STATUS register to determine when the link is up.

Step 3. In the MAC module, the user must set the EXT_EN bit in the Pn_MAC_CTL register to allow the speed and duplex mode to be set by the signals from the SGMII.

2.5 Management Data Input/Output (MDIO) Architecture

This section describes the architecture of the Management Data Input/Output (MDIO) module. The MDIO module manages up to 32 physical layer (PHY) devices connected to the Ethernet Media Access Controller (EMAC). The MDIO module allows almost transparent operation of the MDIO interface with little maintenance from the DSP.

The MDIO module enumerates all PHY devices in the system by continuously polling 32 MDIO addresses. Once it detects a PHY device, the MDIO module reads the PHY status register to monitor the PHY link state. The MDIO module stores link change events that can interrupt the CPU. The event storage allows the DSP to poll the link status of the PHY device without continuously performing MDIO module accesses. When the system must access the MDIO module for configuration and negotiation, the MDIO module performs the MDIO read or write operation independent of the DSP. This independent operation allows the DSP to poll for completion or interrupt the CPU once the operation has completed.

The MDIO module in the GbE switch supports both Clause 22 and Clause 45 frame formats. The user can select which frame format will be used for the communication with each of the connected PHY devices. PHY 0 can be using Clause 22 while PHY 1 is using Clause 45, for example. The MDIO module also allows software to directly control the MDIO output pins through register writes while in manual mode.

2.5.1 Global PHY Detection and Link State Monitoring

The MDIO module will remain idle until enabled by setting the ENABLE bit in the MDIO_CONTROL register. The module will then continuously poll the link status bits from within the Generic Status register of all enabled 32 PHY addresses. Individual PHYs can be enabled or disabled for polling through the associated bit in the MDIO_POLL_EN register. The MDIO_LINK and MDIO_ALIVE register bit values are updated on the poll of each PHY. The MDIO_ALIVE register is updated if the PHY acknowledged the read of the Generic Status register. In addition, any PHY register read transactions initiated by the host also update the MDIO_ALIVE register bit associated with the PHY.

In Normal Mode, the link status of two of the 32 possible PHY addresses can also be determined using the MLINK pin inputs instead of the MDIO state machine. The LINKSEL bit in the MDIO_USERPHYSELn register determines the status input that is used. A change in the link status of the two PHYs being monitored will set the appropriate bit in the MDIO_LINKINTRAW register and the MDIO_LINKINTMASKED register, if enabled by the LINKINTENB bit in the MDIO_USERPHYSELn register.

In State Change Mode, a change in any PHY status will be indicated on the MDIOLINKINT[0] interrupt if enabled. This is discussed further in the MDIO Interrupts section below.

2.5.2 PHY Register User Access

When the DSP must access the MDIO for configuration and negotiation, the PHY access module performs the actual MDIO read or write operation independent of the DSP. Thus, the DSP can poll for completion or receive an interrupt when the read or write operation has been performed. There are two user access registers, MDIO_USERACCESS0 and MDIO_USERACCESS1, which allow the software to submit up to two access requests simultaneously. The requests are processed sequentially.

At any time, the host can define a transaction for the MDIO module to undertake using the DATA, PHYADR _MMD, REGADR, and WRITE fields in the MDIO_USERACCESS *n* register as well as the USER_ADDR *n* field in the MDIO_USERADDRESS *n* register for Clause 45 Frame Formats. When the host sets the GO bit in this register, the MDIO module will begin the transaction without any further intervention from the host. Upon completion, the MDIO interface will clear the GO bit and set the MDIO_USERINTRAW bit in the MDIO_USERINTRAW register corresponding to the MDIO_USERACCESS *n* register being used. The corresponding bit in the MDIO_USERINTMASKED register may also be set depending on the mask setting in the MDIO_USERINTMASKSET and MDIO_USERINTMASKCLR registers. A round-robin arbitration scheme is used to schedule transactions that may be queued by the host in different MDIO_USERACCESS *n* registers. The host should check the status of the GO bit in the MDIO_USERACCESS *n* register before initiating a new transaction to ensure that the previous transaction has completed. The host can use the ACK bit in the MDIO_USERACCESS *n* register to determine the status of a read transaction. In addition, any PHY register read transactions initiated by the host also cause the MDIO_ALIVE register to be updated.

2.5.2.1 Writing Data to a PHY Register

The MDIO module includes a user access register (MDIO_USERACCESS *n*) to directly access a specified PHY device. To write a PHY register, perform the following steps:

1. Ensure that the GO bit in the MDIO_USERACCESS *n* register is cleared.
2. If using Clause 45, Write to the USER_ADDR *n* field of the MDIO_USERADDRESS *n* register corresponding to the PHY register address.
3. Write to the GO, WRITE, REGADR _MMD, PHYADR, and DATA bits in MDIO_USERACCESS *n* corresponding to the desired PHY and PHY register or PHY MMD for Clause 45.
4. The write operation to the PHY is scheduled and completed by the MDIO module.
5. Completion of the write operation will clear the GO bit to 0, and sets the corresponding bit in the MDIO_USERINTRAW register for the corresponding MDIO_USERACCESS *n*.
   - If interrupts have been enabled on this bit using the MDIO_USERINTMASKSET register, then the bit is also set in the MDIO_USERINTMASKED register and an interrupt is triggered on the DSP.
   - If interrupts have not been enabled, then completion can be determined by polling the GO bit in MDIO_USERACCESS *n* for a 0.
   - polling the GO bit in USERACCESSn for a 0.

2.5.2.2 Reading Data from a PHY Register

The MDIO module includes a user access register (MDIO_USERACCESS *n*) to directly access a specified PHY device. To read a PHY register, perform the following:

1. Ensure that the GO bit in the MDIO_USERACCESS *n* register is cleared.
2. If using Clause 45, Write to the USER_ADDR *n* field of the MDIO_USERADDRESS *n* register corresponding to the PHY register address.
3. Write to the GO, REGADR _MMD, and PHYADR bits in USERACCESS *n* corresponding to the desired PHY and PHY register or PHY MMD for Clause 45.
4. The read data value is available in the DATA bits of MDIO_USERACCESS *n* after the module completes the read operation on the serial bus.
5. Completion of a successful read operation will clear the GO bit, set the ACK bit, and set the corresponding bit in the MDIO_USERINTRAW register for the MDIO_USERACCESS *n* used.
   - If interrupts have been enabled on this bit using the MDIO_USERINTMASKSET register, then the bit is also set in the MDIO_USERINTMASKED register and an interrupt is triggered on the DSP.
   - If interrupts have not been enabled, then completion can be determined by polling the GO bit in MDIO_USERACCESS *n* for a 0, and the ACK bit for a 1.

2.5.3 MDIO Interrupts

The MDIO module provides two sets of interrupts that can be enabled by the user. The first set of interrupts is triggered when there is a change in link state of a PHY that is being monitored. The second set of interrupts will occur when a PHY register access initiated through the MDIO_USERACCESS registers has completed.

2.5.3.1 MDIO Link Status Interrupts

The MDIO module has two modes for the link status interrupts: Normal Mode and State Change Mode. The mode of the module is determined by the STATECHANGEMODE bit in the MDIO_CONTROL2 register. Both modes are discussed below.

2.5.3.1.1 Normal Mode

The MDIO module will assert the MDIO_LINKINT signals if there is a change in the link state of the PHY corresponding to the address in the PHYADR_MON field of the MDIO_USERPHYSEL *n* register and the corresponding LINKINTENB bit is set.

The MDIO_LINKINTMASKED event is also captured in the MDIO_LINKINTMASKED register. LINKINTMASKED[0] and LINKINTMASKED[1] correspond to the MDIO_USERPHYSEL0 and MDIO_USERPHYSEL1 registers, respectively.

2.5.3.1.2 State Change Mode

The MDIO will assert MDIO_LINKINT[0] when any bit in the MDIO_ALIVE or MDIO_LINK registers change due to MDIO operations. The MDIO_LINKINT event is also captured in the MDIO_LINKINTMASKED register. MDIO_LINKINT[1] output is unused in State Change Mode. The MDIO_USERPHYSEL *n* registers are unused in state change mode.

2.5.3.2 MDIO User Access Interrupts

When the GO bit in the MDIO_USERACCESS registers transitions from 1 to 0, indicating the completion of a user access, and the corresponding MDIO_USERINTMASKED bit in the MDIO_USERINTMASKSET register is set, the MDIO_USERINTMASKED signal is asserted to 1.

The MDIO_USERINTMASKED event is also captured in the MDIO_USERINTMASKED register. MDIO_USERINTMASKED[0] and MDIO_USERINTMASKED[1] correspond to the MDIO_USERACCESS0 and MDIO_USERACCESS1 registers, respectively.

2.5.4 Initializing the MDIO Module

To have the application software or device driver initialize the MDIO device, perform the following steps:

1. Configure the PREAMBLE and CLKDIV bits in the MDIO_CONTROL register.
2. Enable the MDIO module by setting the ENABLE bit in the MDIO_CONTROL register.
3. The MDIO_ALIVE register can be read after a delay to determine which PHYs responded, and the MDIO_LINK register can determine which of those (if any) already have a link.
4. Set up the appropriate PHY addresses in the MDIO_USERPHYSEL *n* register, and set the LINKINTENB bit to enable a link change event interrupt if desirable.
5. If an interrupt on a general MDIO register access is desired, set the corresponding bit in the MDIO_USERINTMASKSET register to use the MDIO_USERACCESS *n* register. If only one PHY is to be used, the application software can set up one of the MDIO_USERACCESS *n* registers to trigger a completion interrupt. The other register is not set up.

2.6 Serializer/Deserializer (SerDes) Architecture

SerDes module information for this device is not provided in this user's guide. Check for availability of the SerDes User's Guide on the device product page.

2.7 Reset Considerations

The GbE switch subsystem supports reset isolation of the two Ethernet switch ports in KeyStone I, or four in KeyStone II. The intent of reset isolation is to allow packets to switch between the two Ethernet ports while the remainder of the system is undergoing a reset. When the ISOLATE input is asserted the below occur simultaneously:

- The GbE switch host port (port 0) is removed from ALE processing (packets received on ports 1 and 2 intended for port 0 will be dropped)
- Packets from the queue manager subsystem intended the GbE switch host port (port 0) are dropped. Any packet currently in progress when ISOLATE is asserted is dropped due to a receive packet code error (and possible a CRC or FRAG error)
- GbE switch host port (port 0) egress packets in queue are dropped
- (For KeyStone II) The asynchronous FIFOs on the streaming packet interface are reset.

For more information about reset isolation for the GbE switch subsystem, see the device-specific data manual.

2.8 Initialization

This section describes the GbE switch subsystem initialization procedure.

2.8.1 GbE Switch Subsystem Initialization Procedure

Step 1. Configure the CPSW_CONTROL register

Step 2. Configure the MAC1_SA and MAC2_SA (MAC3_SA and MAC4_SA if KeyStone II) source address hi and lo registers

Step 3. Enable the desired statistics ports by programming the CPSW_STAT_PORT_EN register

Step 4. Configure the ALE

Step 5. Configure MAC modules

Step 6. Configure the MDIO and external PHY (if used)

Step 7. Configure the SGMII modules

2.9 Interrupt Support

2.9.1 Interrupt Events

This section describes the interrupts generated in the GbE switch subsystem. Within the GbE switch subsystem, there are three modules that can generate interrupts: the MDIO module, the statistics module, and the time synchronization module. For more information about the interrupts generated by the MDIO module, see Section 2.5. For more information about the interrupts generated by the statistics modules, see Section 2.3.5. For more information about the interrupts generated by the time synchronization module, see Section 2.3.6.

2.10 Power Management

The gigabit Ethernet (GbE) switch subsystem provides power management in the form of clock gating. The clock gating process can be accomplished through software with register writes to the CMD_IDLE bits of the Ethernet ports as well as through register writes to the Power Sleep Controller of the device. The software procedure is as follows:

1. For each Ethernet port write a 1 to the CMD_IDLE bit in the Pn_MAC_CTL register.
2. Read the IDLE bit in the Pn_MAC_STATUS register of each port to ensure that all Ethernet ports are idle.
3. Once all ports are idle, use software to write to the Power Sleep Controller to put the Ethernet SGMIIs clock domain into the SWRSTDISABLE state.
4. Use software to poll until the Power Sleep Controller signals that the state transition of the clock domain is completed.

NOTE: Although the NetCP does have a power domain that can be enabled or disabled, the GbE switch subsystem is only one of the modules in that power domain, and the power cannot be enabled or disabled for the individual modules in the NetCP.

For more information, see the device specific data manual as well as the Power Sleep Controller User's Guide.

Registers

This chapter describes the registers available in the Ethernet switch subsystem and its submodules. For clarity, the registers for each module and submodule are described separately. Provided for each register is a bit field description and a memory offset address. The offset address values provided are relative to the associated base address of the module. See the device-specific data manual for the memory address of these registers.

Topic **Page**

3.1 Summary of Modules

Table 3-1 shows the module regions in the gigabit Ethernet switch subsystem and the corresponding address offset for each module.

Table 3-1. Gigabit Ethernet Switch Subsystem Modules

Offset Address[1]	Module Region	Section
000h	Gigabit Ethernet (GbE) switch subsystem	Section 3.2
100h	Port 1 SGMII module	Section 3.3
200h	Port 2 SGMII module	Section 3.3
300h	Port 3 SGMII module	Section 3.3
400h	Port 4 SGMII module	Section 3.3
500h	Port 5 SGMII module	Section 3.3
600h	Port 6 SGMII module	Section 3.3
700h	Port 7 SGMII module	Section 3.3
800h	Port 8 SGMII module	Section 3.3
900h-EFFh	Reserved	Reserved
F00h	MDIO module	Section 3.4
1000h-1FFFFh	Reserved	Reserved
20000h	Gigabit Ethernet (GbE) switch module	Section 3.5

(1) The addresses provided in the table are offsets from a device specific base address. To determine the base address of these registers, see the device-specific data manual.

Table 3-2 lists all gigabit Ethernet switch subsystem registers.

Table 3-2. Gigabit Ethernet Switch Subsystem Complete Register Listing

Offset Address[(1)]	Module	Acronym	Register Name	Section
000h	GbE Switch Subsystem	ES_SS_IDVER	Ethernet Switch Subsystem Identification and Version Register	Section 3.2.1
004h	GbE Switch Subsystem	ES_SS_SYNCE_COUNT	Ethernet Switch Subsystem Synchronous Ethernet Count Register	Section 3.2.2
008h	GbE Switch Subsystem	ES_SS_SYNCE_MUX	Ethernet Switch Subsystem Synchronous Ethernet Clock Select Register	Section 3.2.3
00Ch-0FCh	Reserved	Reserved	Reserved	Reserved
100h	Port 1 SGMII	SGMII_IDVER	Identification and Version Register	Section 3.3.1
104h	Port 1 SGMII	SGMII_SOFT_RESET	Soft Reset Register	Section 3.3.2
108h-10Ch	Reserved	Reserved	Reserved	Reserved
110h	Port 1 SGMII	SGMII_CONTROL	Control Register	Section 3.3.3
114h	Port 1 SGMII	SGMII_STATUS	Status Register (read only)	Section 3.3.4
118h	Port 1 SGMII	SGMII_MR_ADV_ABILITY	Advertised Ability Register	Section 3.3.5
11Ch	Port 1 SGMII	SGMII_MR_NP_TX	Transmit Next Page Register	Section 3.3.6
120h	Port 1 SGMII	SGMII_MR_LP_ADV_ABILITY	Link Partner Advertised Ability (read only)	Section 3.3.7
124h	Port 1 SGMII	SGMII_MR_NP_RX	Link Partner Receive Next Page Register (read only)	Section 3.3.8
128h-1FCh	Reserved	Reserved	Reserved	Reserved
200h	Port 2 SGMII	SGMII_IDVER	Identification and Version Register	Section 3.3.1
204h	Port 2 SGMII	SGMII_SOFT_RESET	Soft Reset Register	Section 3.3.2
208h-20Ch	Reserved	Reserved	Reserved	Reserved
210h	Port 2 SGMII	SGMII_CONTROL	Control Register	Section 3.3.3
214h	Port 2 SGMII	SGMII_STATUS	Status Register (read only)	Section 3.3.4
218h	Port 2 SGMII	SGMII_MR_ADV_ABILITY	Advertised Ability Register	Section 3.3.5
21Ch	Port 2 SGMII	SGMII_MR_NP_TX	Transmit Next Page Register	Section 3.3.6
220h	Port 2 SGMII	SGMII_MR_LP_ADV_ABILITY	Link Partner Advertised Ability (read only)	Section 3.3.7
224h	Port 2 SGMII	SGMII_MR_NP_RX	Link Partner Receive Next Page Register (read only)	Section 3.3.8
228h-2FCh	Reserved	Reserved	Reserved	Reserved
300h	Port 3 SGMII	SGMII_IDVER	Identification and Version Register	Section 3.3.1
304h	Port 3 SGMII	SGMII_SOFT_RESET	Soft Reset Register	Section 3.3.2
308h-30Ch	Reserved	Reserved	Reserved	Reserved
310h	Port 3 SGMII	SGMII_CONTROL	Control Register	Section 3.3.3

(1) The actual addresses of these registers are device specific. See your device-specific data manual to verify the register addresses.

Table 3-2. Gigabit Ethernet Switch Subsystem Complete Register Listing (continued)

Offset Address[(1)]	Module	Acronym	Register Name	Section
314h	Port 3 SGMII	SGMII_STATUS	Status Register (read only)	Section 3.3.4
318h	Port 3 SGMII	SGMII_MR_ADV_ABILITY	Advertised Ability Register	Section 3.3.5
31Ch	Port 3 SGMII	SGMII_MR_NP_TX	Transmit Next Page Register	Section 3.3.6
320h	Port 3 SGMII	SGMII_MR_LP_ADV_ABILITY	Link Partner Advertised Ability (read only)	Section 3.3.7
324h	Port 3 SGMII	SGMII_MR_NP_RX	Link Partner Receive Next Page Register (read only)	Section 3.3.8
328h-3FCh	Reserved	Reserved	Reserved	Reserved
400h	Port 4 SGMII	SGMII_IDVER	Identification and Version Register	Section 3.3.1
404h	Port 4 SGMII	SGMII_SOFT_RESET	Soft Reset Register	Section 3.3.2
408h-40Ch	Reserved	Reserved	Reserved	Reserved
410h	Port 4 SGMII	SGMII_CONTROL	Control Register	Section 3.3.3
414h	Port 4 SGMII	SGMII_STATUS	Status Register (read only)	Section 3.3.4
418h	Port 41 SGMII	SGMII_MR_ADV_ABILITY	Advertised Ability Register	Section 3.3.5
41Ch	Port 4 SGMII	SGMII_MR_NP_TX	Transmit Next Page Register	Section 3.3.6
420h	Port 4 SGMII	SGMII_MR_LP_ADV_ABILITY	Link Partner Advertised Ability (read only)	Section 3.3.7
424h	Port 4 SGMII	SGMII_MR_NP_RX	Link Partner Receive Next Page Register (read only)	Section 3.3.8
428h-4FCh	Reserved	Reserved	Reserved	Reserved
500h	Port 5 SGMII	SGMII_IDVER	Identification and Version Register	Section 3.3.1
504h	Port 5 SGMII	SGMII_SOFT_RESET	Soft Reset Register	Section 3.3.2
508h-50Ch	Reserved	Reserved	Reserved	Reserved
510h	Port 5 SGMII	SGMII_CONTROL	Control Register	Section 3.3.3
514h	Port 5 SGMII	SGMII_STATUS	Status Register (read only)	Section 3.3.4
518h	Port 5 SGMII	SGMII_MR_ADV_ABILITY	Advertised Ability Register	Section 3.3.5
51Ch	Port 5 SGMII	SGMII_MR_NP_TX	Transmit Next Page Register	Section 3.3.6
520h	Port 5 SGMII	SGMII_MR_LP_ADV_ABILITY	Link Partner Advertised Ability (read only)	Section 3.3.7
524h	Port 5 SGMII	SGMII_MR_NP_RX	Link Partner Receive Next Page Register (read only)	Section 3.3.8
528h-5FCh	Reserved	Reserved	Reserved	Reserved
600h	Port 6 SGMII	SGMII_IDVER	Identification and Version Register	Section 3.3.1
604h	Port 6 SGMII	SGMII_SOFT_RESET	Soft Reset Register	Section 3.3.2
608h-60Ch	Reserved	Reserved	Reserved	Reserved
610h	Port 6 SGMII	SGMII_CONTROL	Control Register	Section 3.3.3

Table 3-2. Gigabit Ethernet Switch Subsystem Complete Register Listing (continued)

Offset Address[1]	Module	Acronym	Register Name	Section
614h	Port 6 SGMII	SGMII_STATUS	Status Register (read only)	Section 3.3.4
618h	Port 6 SGMII	SGMII_MR_ADV_ABILITY	Advertised Ability Register	Section 3.3.5
61Ch	Port 6 SGMII	SGMII_MR_NP_TX	Transmit Next Page Register	Section 3.3.6
620h	Port 6 SGMII	SGMII_MR_LP_ADV_ABILITY	Link Partner Advertised Ability (read only)	Section 3.3.7
624h	Port 6 SGMII	SGMII_MR_NP_RX	Link Partner Receive Next Page Register (read only)	Section 3.3.8
628h-6FCh	Reserved	Reserved	Reserved	Reserved
700h	Port 7 SGMII	SGMII_IDVER	Identification and Version Register	Section 3.3.1
704h	Port 7 SGMII	SGMII_SOFT_RESET	Soft Reset Register	Section 3.3.2
708h-70Ch	Reserved	Reserved	Reserved	Reserved
710h	Port 7 SGMII	SGMII_CONTROL	Control Register	Section 3.3.3
714h	Port 7 SGMII	SGMII_STATUS	Status Register (read only)	Section 3.3.4
718h	Port 7 SGMII	SGMII_MR_ADV_ABILITY	Advertised Ability Register	Section 3.3.5
71Ch	Port 7 SGMII	SGMII_MR_NP_TX	Transmit Next Page Register	Section 3.3.6
720h	Port 7 SGMII	SGMII_MR_LP_ADV_ABILITY	Link Partner Advertised Ability (read only)	Section 3.3.7
724h	Port 7 SGMII	SGMII_MR_NP_RX	Link Partner Receive Next Page Register (read only)	Section 3.3.8
728h-7FCh	Reserved	Reserved	Reserved	Reserved
800h	Port 8 SGMII	SGMII_IDVER	Identification and Version Register	Section 3.3.1
804h	Port 8 SGMII	SGMII_SOFT_RESET	Soft Reset Register	Section 3.3.2
808h-80Ch	Reserved	Reserved	Reserved	Reserved
810h	Port 8 SGMII	SGMII_CONTROL	Control Register	Section 3.3.3
814h	Port 8 SGMII	SGMII_STATUS	Status Register (read only)	Section 3.3.4
818h	Port 8 SGMII	SGMII_MR_ADV_ABILITY	Advertised Ability Register	Section 3.3.5
81Ch	Port 8 SGMII	SGMII_MR_NP_TX	Transmit Next Page Register	Section 3.3.6
820h	Port 8 SGMII	SGMII_MR_LP_ADV_ABILITY	Link Partner Advertised Ability (read only)	Section 3.3.7
824h	Port 8 SGMII	SGMII_MR_NP_RX	Link Partner Receive Next Page Register (read only)	Section 3.3.8
828h-8FCh	Reserved	Reserved	Reserved	Reserved
F00h	MDIO	MDIO_VERSION	MDIO Version Register	Section 3.4.1
F04h	MDIO	MDIO_CONTROL	MDIO Control Register	Section 3.4.2
F08h	MDIO	MDIO_ALIVE	PHY Alive Status Register	Section 3.4.3
F0Ch	MDIO	MDIO_LINK	PHY Link Status Register	Section 3.4.4

Table 3-2. Gigabit Ethernet Switch Subsystem Complete Register Listing (continued)

Offset Address[(1)]	Module	Acronym	Register Name	Section
F10h	MDIO	MDIO_LINKINTRAW	MDIO Link Status Change Interrupt (Unmaksed) Register	Section 3.4.5
F14h	MDIO	MDIO_LINKINTMASKED	MDIO Link Status Change Interrupt (Masked) Register	Section 3.4.6
F18h	MDIO	MDIO_LINKINTMASKSET	MDIO Link Status Change Interrupt Mask Set Register	Section 3.4.7
F1Ch	MDIO	MDIO_LINKINTMASKCLR	MDIO Link Status Change Interrupt Mask Clear Register	Section 3.4.8
F20h	MDIO	MDIO_USERINTRAW	MDIO User Command Complete Interrupt (Unmasked) Register	Section 3.4.9
F24h	MDIO	MDIO_USERINTMASKED	MDIO User Command Complete Interrupt (Masked) Register	Section 3.4.10
F28h	MDIO	MDIO_USERINTMASKSET	MDIO User Interrupt Mask Set Register	Section 3.4.11
F2Ch	MDIO	MDIO_USERINTMASKCLEAR	MDIO User Interrupt Mask Clear Register	Section 3.4.12
F30h	MDIO	MDIO_MANUAL_IF	MDIO Manual Interface Register	Section 3.4.13
F34h	MDIO	MDIO_CONTROL2	MDIO Control 2 Register	Section 3.4.14
F38h	MDIO	MDIO_POLL_EN	MDIO Poll Enable Register	Section 3.4.15
F3Ch	MDIO	MDIO_CLAUSE	MDIO Clause 22 or 45 Enable Register	Section 3.4.16
F40h	MDIO	MDIO_USERADDRESS0	MDIO User Address Register 0	Section 3.4.17
F44h	MDIO	MDIO_USERADDRESS1	MDIO User Address Register 1	Section 3.4.18
F48h–F7Ch	Reserved	Reserved	Reserved	Reserved
F80h	MDIO	MDIO_USERACCESS0	MDIO User Access Register 0	Section 3.4.19
F84h	MDIO	MDIO_USERPHYSEL0	MDIO User PHY Select Register 0	Section 3.4.20
F88h	MDIO	MDIO_USERACCESS1	MDIO User Access Register 1	Section 3.4.21
F8Ch	MDIO	MDIO_USERPHYSEL1	MDIO User PHY Select Register 1	Section 3.4.22
F90h-1FFFCh	Reserved	Reserved	Reserved	Reserved
20000h	GbE Switch	CPSW_IDVER	GbE switch identification and version register	Section 3.5.1.1
20004h	GbE Switch	CPSW_CONTROL	GbE switch Control Register	Section 3.5.1.2
20008h-2000Ch	Reserved	Reserved	Reserved	Reserved
20010h	GbE Switch	CPSW_EM_CONTROL	GbE switch Emulation Control Register	Section 3.5.1.3
20014h	GbE Switch	CPSW_STAT_PORT_EN	GbE switch Statistics Port Enable Register	Section 3.5.1.4
20018h	GbE Switch	CPSW_PTYPE	GbE switch Transmit Priority Type Register	Section 3.5.1.5
2001Ch	GbE Switch	CPSW_SOFT_IDLE	GbE switch Software Idle Register	Section 3.5.1.6
20020h	GbE Switch	CPSW_THRU_RATE	GbE switch Thru Rate Register	Section 3.5.1.7

Table 3-2. Gigabit Ethernet Switch Subsystem Complete Register Listing (continued)

Offset Address[1]	Module	Acronym	Register Name	Section
20024h	GbE Switch	CPSW_GAP_THRESH	Transmit FIFO Short Gap Threshold Register	Section 3.5.1.8
20028h	GbE Switch	CPSW_TX_START_WDS	Transmit FIFO Start Words Register	Section 3.5.1.9
2002Ch	Reserved	Reserved	Reserved	Reserved
20030h	GbE Switch	CPSW_TX_OUTFLOW_THRESH_SET	Global Transmit Out Flow Threshold Set Register	Section 3.5.1.10
20034h	GbE Switch	CPSW_TX_OUTFLOW_THRESH_CLR	Global Transmit Out Flow Threshold Clear Register	Section 3.5.1.11
20038h	GbE Switch	CPSW_TX_BUFFER_THRESH_SET_L	Global Transmit Buffer Threshold Set Register Low	Section 3.5.1.12
2003Ch	GbE Switch	CPSW_TX_BUFFER_THRESH_SET_H	Global Transmit Buffer Threshold Set Register High	Section 3.5.1.13
20040h	GbE Switch	CPSW_TX_BUFFER_THRESH_CLR_L	Global Transmit Buffer Threshold Clear Register Low	Section 3.5.1.14
20044h	GbE Switch	CPSW_TX_BUFFER_THRESH_CLR_H	Global Transmit Buffer Threshold Clear Register High	Section 3.5.1.15
20048h-21000h	Reserved	Reserved	Reserved	Reserved
21004h	Host Port 0	P0_CONTROL	Host Port 0 Control Register	Section 3.5.2.1
21008h-2100Ch	Reserved	Reserved	Reserved	Reserved
21010h	Host Port 0	P0_BLK_CNT	Host Port 0 FIFO Block Usage Count	Section 3.5.2.2
21014h	Host Port 0	P0_PORT_VLAN	Host Port 0 VLAN Register	Section 3.5.2.3
21018h	Host Port 0	P0_TX_PRI_MAP	Host Port 0 Transmit Header Priority to Switch Priority Mapping Register	Section 3.5.2.4
2101Ch	Host Port 0	P0_PRI_CTL	Host Port 0 Priority Control Register	Section 3.5.2.5
21020h	Host Port 0	P0_RX_PRI_MAP	Host Port 0 Receive Packet Priority to Header Priority Mapping Register	Section 3.5.2.6
21024h	Host Port 0	P0_RX_MAXLEN	Host Port 0 Receive Frame Max Length Register	Section 3.5.2.7
21028h	Host Port 0	P0_TX_BLKS_PRI	Host Port 0 Transmit Block Sub Per Priority Register	Section 3.5.2.8
2102Ch-2111Ch	Reserved	Reserved	Reserved	Reserved
21120h	Host Port 0	P0_RX_DSCP_MAP0	Host Port 0 Receive IPv4/IPv6 DSCP Priority Mapping Register 0	Section 3.5.2.9
21124h	Host Port 0	P0_RX_DSCP_MAP1	Host Port 0 Receive IPv4/IPv6 DSCP Priority Mapping Register 1	Section 3.5.2.10
21128h	Host Port 0	P0_RX_DSCP_MAP2	Host Port 0 Receive IPv4/IPv6 DSCP Priority Mapping Register 2	Section 3.5.2.11
2112Ch	Host Port 0	P0_RX_DSCP_MAP3	Host Port 0 Receive IPv4/IPv6 DSCP Priority Mapping Register 3	Section 3.5.2.12
21130h	Host Port 0	P0_RX_DSCP_MAP4	Host Port 0 Receive IPv4/IPv6 DSCP Priority Mapping Register 4	Section 3.5.2.13
21134h	Host Port 0	P0_RX_DSCP_MAP5	Host Port 0 Receive IPv4/IPv6 DSCP Priority Mapping Register 5	Section 3.5.2.14
21138h	Host Port 0	P0_RX_DSCP_MAP6	Host Port 0 Receive IPv4/IPv6 DSCP Priority Mapping Register 6	Section 3.5.2.15
2113Ch	Host Port 0	P0_RX_DSCP_MAP7	Host Port 0 Receive IPv4/IPv6 DSCP Priority Mapping Register 7	Section 3.5.2.16

Table 3-2. Gigabit Ethernet Switch Subsystem Complete Register Listing (continued)

Offset Address[(1)]	Module	Acronym	Register Name	Section
21140h	Host Port 0	P0_PRI0_SEND	Host Port 0 Receive Priority 0 Send Count Value Register	Section 3.5.2.17
21144h	Host Port 0	P0_PRI1_SEND	Host Port 0 Receive Priority 1 Send Count Value Register	Section 3.5.2.18
21148h	Host Port 0	P0_PRI2_SEND	Host Port 0 Receive Priority 2 Send Count Value Register	Section 3.5.2.19
2114Ch	Host Port 0	P0_PRI3_SEND	Host Port 0 Receive Priority 3 Send Count Value Register	Section 3.5.2.20
21150h	Host Port 0	P0_PRI4_SEND	Host Port 0 Receive Priority 4 Send Count Value Register	Section 3.5.2.21
21154h	Host Port 0	P0_PRI5_SEND	Host Port 0 Receive Priority 5 Send Count Value Register	Section 3.5.2.22
21158h	Host Port 0	P0_PRI6_SEND	Host Port 0 Receive Priority 6 Send Count Value Register	Section 3.5.2.23
2115Ch	Host Port 0	P0_PRI7_SEND	Host Port 0 Receive Priority 7 Send Count Value Register	Section 3.5.2.24
21160h	Host Port 0	P0_PRI0_IDLE	Host Port 0 Receive Priority 0 Idle Count Value Register	Section 3.5.2.25
21164h	Host Port 0	P0_PRI1_IDLE	Host Port 0 Receive Priority 1 Idle Count Value Register	Section 3.5.2.26
21168h	Host Port 0	P0_PRI2_IDLE	Host Port 0 Receive Priority 2 Idle Count Value Register	Section 3.5.2.27
2116Ch	Host Port 0	P0_PRI3_IDLE	Host Port 0 Receive Priority 3 Idle Count Value Register	Section 3.5.2.28
21170h	Host Port 0	P0_PRI4_IDLE	Host Port 0 Receive Priority 4 Idle Count Value Register	Section 3.5.2.29
21174h	Host Port 0	P0_PRI5_IDLE	Host Port 0 Receive Priority 5 Idle Count Value Register	Section 3.5.2.30
21178h	Host Port 0	P0_PRI6_IDLE	Host Port 0 Receive Priority 6 Idle Count Value Register	Section 3.5.2.31
2117Ch	Host Port 0	P0_PRI7_IDLE	Host Port 0 Receive Priority 7 Idle Count Value Register	Section 3.5.2.32
21180h	Host Port 0	P0_TX_DEST_THRESH_SET_L	Host Port 0 Transmit Destination Threshold Set Low Register	Section 3.5.2.33
21184h	Host Port 0	P0_TX_DEST_THRESH_SET_H	Host Port 0 Transmit Destination Threshold Set High Register	Section 3.5.2.34
21188h	Host Port 0	P0_TX_DEST_THRESH_CLR_L	Host Port 0 Transmit Destination Threshold Clear Low Register	Section 3.5.2.35
2118Ch	Host Port 0	P0_TX_DEST_THRESH_CLR_H	Host Port 0 Transmit Destination Threshold Clear High Register	Section 3.5.2.36
21190h	Host Port 0	P0_TX_BUFFER_THRESH_SET_L	Host Port 0 Global Transmit Buffer Threshold Set Register Low	Section 3.5.2.37
21194h	Host Port 0	P0_TX_BUFFER_THRESH_SET_H	Host Port 0 Global Transmit Buffer Threshold Set Register High	Section 3.5.2.38
21198h	Host Port 0	P0_TX_BUFFER_THRESH_CLR_L	Host Port 0 Global Transmit Buffer Threshold Clear Register Low	Section 3.5.2.39
2119Ch	Host Port 0	P0_TX_BUFFER_THRESH_CLR_H	Host Port 0 Global Transmit Buffer Threshold Clear Register High	Section 3.5.2.40
211A0h-212FCh	Reserved	Reserved	Reserved	Reserved
21300h	Host Port 0	P0_SRC_ID_A	Host Port 0 Source ID A Register	Section 3.5.2.41
21304h	Host Port 0	P0_SRC_ID_B	Host Port 0 Source ID B Register	Section 3.5.2.42

Table 3-2. Gigabit Ethernet Switch Subsystem Complete Register Listing (continued)

Offset Address[(1)]	Module	Acronym	Register Name	Section
21308h-2131Ch	Reserved	Reserved	Reserved	Reserved
21320h	Host Port 0	P0_HOST_BLKS_PRI	Host Port 0 Host Blocks Priority Register	Section 3.5.2.43
21324h-21FFCh	Reserved	Reserved	Reserved	Reserved
22000-22FFCh	Ethernet Port 1	Ethernet Port 1 Registers	See Table 3-3 with n = 1	Section 3.5.2
23000-23FFCh	Ethernet Port 2	Ethernet Port 2 Registers	See Table 3-3 with n = 2	Section 3.5.2
24000-24FFCh	Ethernet Port 3	Ethernet Port 3 Registers	See Table 3-3 with n = 3	Section 3.5.2
25000-25FFCh	Ethernet Port 4	Ethernet Port 4 Registers	See Table 3-3 with n = 4	Section 3.5.2
26000-26FFCh	Ethernet Port 5	Ethernet Port 5 Registers	See Table 3-3 with n = 5	Section 3.5.2
27000-27FFCh	Ethernet Port 6	Ethernet Port 6 Registers	See Table 3-3 with n = 6	Section 3.5.2
28000-28FFCh	Ethernet Port 7	Ethernet Port 7 Registers	See Table 3-3 with n = 7	Section 3.5.2
29000-29FFCh	Ethernet Port 8	Ethernet Port 8 Registers	See Table 3-3 with n = 8	Section 3.5.2
2A000h-39FFCh	Reserved	Reserved	Reserved	Reserved
3A000h	STAT0	STAT0_RXGOODFRAMES	Host Port 0 Total number of good frames received	Section 3.5.3.1
3A004h	STAT0	STAT0_RXBROADCASTFRAMES	Host Port 0 Total number of good broadcast frames received	Section 3.5.3.2
3A008h	STAT0	STAT0_RXMULTICASTFRAMES	Host Port 0 Total number of good multicast frames received	Section 3.5.3.3
3A00Ch	Reserved	Reserved	Reserved	Reserved
3A010h	STAT0	STAT0_RXCRCERRORS	Host Port 0 Total number of CRC errors received	Section 3.5.3.5
3A014h	Reserved	Reserved	Reserved	Reserved
3A018h	STAT0	STAT0_RXOVERSIZEDFRAMES	Host Port 0 Total number of oversized frames received	Section 3.5.3.7
3A01Ch	Reserved	Reserved	Reserved	Reserved
3A020h	STAT0	STAT0_RXUNDERSIZEDFRAMES	Host Port 0 Total number of undersized frames received	Section 3.5.3.9
3A024h	Reserved	Reserved	Reserved	Reserved
3A028h	STAT0	STAT0_ALE_DROP	Host Port 0 Total number of frames dropped by the ALE	Section 3.5.3.11
3A02Ch	STAT0	STAT0_ALE_OVERRUN_DROP	Host Port 0 Total number of frames dropped due to exceeding the maximum ALE lookup rate	Section 3.5.3.12
3A030h	STAT0	STAT0_RXOCTETS	Host Port 0 Total number of received bytes in good frames	Section 3.5.3.13
3A034h	STAT0	STAT0_TXGOODFRAMES	Host Port 0 Total number of good frames transmitted	Section 3.5.3.14
3A038h	STAT0	STAT0_TXBROADCASTFRAMES	Host Port 0 Total number of good broadcast frames transmitted	Section 3.5.3.15
3A03Ch	STAT0	STAT0_TXMULTICASTFRAMES	Host Port 0 Total number of good multicast frames transmitted	Section 3.5.3.16
3A040h-3A060h	Reserved	Reserved	Reserved	Reserved

Table 3-2. Gigabit Ethernet Switch Subsystem Complete Register Listing (continued)

Offset Address[(1)]	Module	Acronym	Register Name	Section
3A064h	STAT0	STAT0_TXOCTETS	Host Port 0 Total number of octets transmitted	Section 3.5.3.25
3A068h	STAT0	STAT0_64OCTETFRAMES	Host Port 0 Total number of 64 octet frames transmitted and received on the port	Section 3.5.3.26
3A06Ch	STAT0	STAT0_65T127OCTETFRAMES	Host Port 0 Total number of 65-127 octet frames transmitted and received on the port	Section 3.5.3.27
3A070h	STAT0	STAT0_128T255OCTETFRAMES	Host Port 0 Total number of 128-255 octet frames transmitted and received on the port	Section 3.5.3.28
3A074h	STAT0	STAT0_256T511OCTETFRAMES	Host Port 0 Total number of 256-511 octet frames transmitted and received on the port	Section 3.5.3.29
3A078h	STAT0	STAT0_512T1023OCTETFRAMES	Host Port 0 Total number of 512-1023 octet frames transmitted and received on the port	Section 3.5.3.30
3A07Ch	STAT0	STAT0_1024TUPOCTETFRAMES	Host Port 0 Total number of 1023-(P0_RX_MAXLEN) octet frames transmitted and received on the port	Section 3.5.3.31
3A080h	STAT0	STAT0_NETOCTETS	Host Port 0 Total number of bytes of frame data received and transmitted on the port	Section 3.5.3.32
3A084h	STAT0	STAT0_RX_BOTTOM_FIFO_DROP	Host Port 0 Total number of frames received at port 0 that were dropped because they overran the receive FIFO	Section 3.5.3.33
3A088h	STAT0	STAT0_PORTMASK_DROP	Host Port 0 Total number of frames received at port 0 that were dropped by the ALE	Section 3.5.3.34
3A08Ch	STAT0	STAT0_RX_TOP_FIFO_DROP	Host Port 0 Total number of frames received at port 0 that were dropped due to a start of frame (SOF) overrun on any destination port egress	Section 3.5.3.35
3A090h	STAT0	STAT0_ALE_RATE_LIMIT_DROP	Host Port 0 Total number of frames that were dropped due to receive rate limiting on port 0 or transmit rate limiting on any destination port	Section 3.5.3.36
3A094h	STAT0	STAT0_ALE_VID_INGRESS_DROP	Host Port 0 Total number of frames that were dropped due to VLAN ingress check failure	Section 3.5.3.37
3A098h	STAT0	STAT0_ALE_DA_EQ_SA_DROP	Host Port 0 Total number of frames that were dropped due to destination address being the same as source address	Section 3.5.3.38
3A09Ch-3A0A4h	Reserved	Reserved	Reserved	Reserved
3A0A8h	STAT0	STAT0_ALE_UNKN_UNI	Host Port 0 Total number of frames received at port 0 that had a unicast destination address with an unknown source address	Section 3.5.3.39
3A0ACh	STAT0	STAT0_ALE_UNKN_UNI_BCNT	Host Port 0 Total number of bytes contained in the frames that qualify for the P0_ALE_UNKN_UNI register	Section 3.5.3.40
3A0B0h	STAT0	STAT0_ALE_UNKN_MLT	Host Port 0 Total number of frames received at port 0 that had a multicast destination address with an unknown source address	Section 3.5.3.41
3A0B4h	STAT0	STAT0_ALE_UNKN_MLT_BCNT	Host Port 0 Total number of bytes contained in the frames that qualify for the P0_ALE_UNKN_MLT register	Section 3.5.3.42

Table 3-2. Gigabit Ethernet Switch Subsystem Complete Register Listing (continued)

Offset Address[1]	Module	Acronym	Register Name	Section
3A0B8h	STAT0	STAT0_ALE_UNKN_BRD	Host Port 0 Total number of frames received at port 0 that had a broadcast destination address with an unknown source address	Section 3.5.3.43
3A0BCh	STAT0	STAT0_ALE_UNKN_BRD_BCNT	Host Port 0 Total number of bytes contained in the frames that qualify for the P0_ALE_UNKN_BRD register	Section 3.5.3.44
3A0C0h-3A178h	Reserved	Reserved	Reserved	Reserved
3A17Ch	STAT0	STAT0_TX_MEM_PROTECT_ERROR	Host Port 0 Total number of frames transmitted that had a memory protect CRC error on egress	Section 3.5.3.45
3A180h	STAT0	STAT0_TX_PRI0	Host Port 0 Total number of packets transmitted with Priority 0	Section 3.5.3.46
3A184h	STAT0	STAT0_TX_PRI1	Host Port 0 Total number of packets transmitted with Priority 1	Section 3.5.3.46
3A188h	STAT0	STAT0_TX_PRI2	Host Port 0 Total number of packets transmitted with Priority 2	Section 3.5.3.46
3A18Ch	STAT0	STAT0_TX_PRI3	Host Port 0 Total number of packets transmitted with Priority 3	Section 3.5.3.46
3A190h	STAT0	STAT0_TX_PRI4	Host Port 0 Total number of packets transmitted with Priority 4	Section 3.5.3.46
3A194h	STAT0	STAT0_TX_PRI5	Host Port 0 Total number of packets transmitted with Priority 5	Section 3.5.3.46
3A198h	STAT0	STAT0_TX_PRI6	Host Port 0 Total number of packets transmitted with Priority 6	Section 3.5.3.46
3A19Ch	STAT0	STAT0_TX_PRI7	Host Port 0 Total number of packets transmitted with Priority 7	Section 3.5.3.46
3A1A0h	STAT0	STAT0_TX_PRI0_BCNT	Host Port 0 Total number of bytes transmitted with Priority 0	Section 3.5.3.47
3A1A4h	STAT0	STAT0_TX_PRI1_BCNT	Host Port 0 Total number of bytes transmitted with Priority 1	Section 3.5.3.47
3A1A8h	STAT0	STAT0_TX_PRI2_BCNT	Host Port 0 Total number of bytes transmitted with Priority 2	Section 3.5.3.47
3A1ACh	STAT0	STAT0_TX_PRI3_BCNT	Host Port 0 Total number of bytes transmitted with Priority 3	Section 3.5.3.47
3A1B0h	STAT0	STAT0_TX_PRI4_BCNT	Host Port 0 Total number of bytes transmitted with Priority 4	Section 3.5.3.47
3A1B4h	STAT0	STAT0_TX_PRI5_BCNT	Host Port 0 Total number of bytes transmitted with Priority 5	Section 3.5.3.47
3A1B8h	STAT0	STAT0_TX_PRI6_BCNT	Host Port 0 Total number of bytes transmitted with Priority 6	Section 3.5.3.47
3A1BCh	STAT0	STAT0_TX_PRI7_BCNT	Host Port 0 Total number of bytes transmitted with Priority 7	Section 3.5.3.47
3A1C0h	STAT0	STAT0_TX_PRI0_DROP	Host Port 0 Total number of packets dropped during transmit with Priority 0	Section 3.5.3.48
3A1C4h	STAT0	STAT0_TX_PRI1_DROP	Host Port 0 Total number of packets dropped during transmit with Priority 1	Section 3.5.3.48
3A1C8h	STAT0	STAT0_TX_PRI2_DROP	Host Port 0 Total number of packets dropped during transmit with Priority 2	Section 3.5.3.48
3A1CCh	STAT0	STAT0_TX_PRI3_DROP	Host Port 0 Total number of packets dropped during transmit with Priority 3	Section 3.5.3.48
3A1D0h	STAT0	STAT0_TX_PRI4_DROP	Host Port 0 Total number of packets dropped during transmit with Priority 4	Section 3.5.3.48
3A1D4h	STAT0	STAT0_TX_PRI5_DROP	Host Port 0 Total number of packets dropped during transmit with Priority 5	Section 3.5.3.48

Table 3-2. Gigabit Ethernet Switch Subsystem Complete Register Listing (continued)

Offset Address[(1)]	Module	Acronym	Register Name	Section
3A1D8h	STAT0	STAT0_TX_PRI6_DROP	Host Port 0 Total number of packets dropped during transmit with Priority 6	Section 3.5.3.48
3A1DCh	STAT0	STAT0_TX_PRI7_DROP	Host Port 0 Total number of packets dropped during transmit with Priority 7	Section 3.5.3.48
3A1E0h	STAT0	STAT0_TX_PRI0_DROP_BCNT	Host Port 0 Total number of bytes dropped during transmit with Priority 0	Section 3.5.3.49
3A1E4h	STAT0	STAT0_TX_PRI1_DROP_BCNT	Host Port 0 Total number of bytes dropped during transmit with Priority 1	Section 3.5.3.49
3A1E8h	STAT0	STAT0_TX_PRI2_DROP_BCNT	Host Port 0 Total number of bytes dropped during transmit with Priority 2	Section 3.5.3.49
3A1ECh	STAT0	STAT0_TX_PRI3_DROP_BCNT	Host Port 0 Total number of bytes dropped during transmit with Priority 3	Section 3.5.3.49
3A1F0h	STAT0	STAT0_TX_PRI4_DROP_BCNT	Host Port 0 Total number of bytes dropped during transmit with Priority 4	Section 3.5.3.49
3A1F4h	STAT0	STAT0_TX_PRI5_DROP_BCNT	Host Port 0 Total number of bytes dropped during transmit with Priority 5	Section 3.5.3.49
3A1F8h	STAT0	STAT0_TX_PRI6_DROP_BCNT	Host Port 0 Total number of bytes dropped during transmit with Priority 6	Section 3.5.3.49
3A1FCh	STAT0	STAT0_TX_PRI7_DROP_BCNT	Host Port 0 Total number of bytes dropped during transmit with Priority 7	Section 3.5.3.49
3A200h-3A3FCh	STAT1	Ethernet Port 1 Statistics	See Table 3-4 with n = 1	Section 3.5.3
3A400h-3A5FCh	STAT2	Ethernet Port 2 Statistics	See Table 3-4 with n = 2	Section 3.5.3
3A600h-3A7FCh	STAT3	Ethernet Port 3 Statistics	See Table 3-4 with n = 3	Section 3.5.3
3A800h-3A9FCh	STAT4	Ethernet Port 4 Statistics	See Table 3-4 with n = 4	Section 3.5.3
3AA00h-3ABFCh	STAT5	Ethernet Port 5 Statistics	See Table 3-4 with n = 5	Section 3.5.3
3AC00h-3ADFCh	STAT6	Ethernet Port 6 Statistics	See Table 3-4 with n = 6	Section 3.5.3
3AE00h-3AFFCh	STAT7	Ethernet Port 7 Statistics	See Table 3-4 with n = 7	Section 3.5.3
3B000h-3B1FCh	STAT8	Ethernet Port 8 Statistics	See Table 3-4 with n = 8	Section 3.5.3
3B200h-3CFFCh	Reserved	Reserved	Reserved	Reserved
3D000	CPTS	CPTS_IDVER	Identification and Version Register	Section 3.5.4.1
3D004	CPTS	CPTS_CTL	Time Sync Control Register	Section 3.5.4.2
3D008	CPTS	CPTS_RFTCLK_SEL	Reference Clock Select Register	Section 3.5.4.3
3D00C	CPTS	CPTS_TS_PUSH	Time Stamp Event Push Register	Section 3.5.4.4
3D010h	CPTS	CPTS_TS_LOAD_VAL_L	Time Stamp Load Value Register (lower 32 bits)	Section 3.5.4.5
3D014	CPTS	CPTS_TS_LOAD_EN	Time Stamp Load Enable Register	Section 3.5.4.6
3D018	CPTS	CPTS_TS_COMP_VAL_L	Time Stamp Comparison Value Register (lower 32 bits)	Section 3.5.4.7
3D01C	CPTS	CPTS_TS_COMP_LENGTH	Time Stamp Comparison Length Register	Section 3.5.4.8

Table 3-2. Gigabit Ethernet Switch Subsystem Complete Register Listing (continued)

Offset Address[1]	Module	Acronym	Register Name	Section
3D020h	CPTS	CPTS_INTSTAT_RAW	Interrupt Status Raw Register	Section 3.5.4.9
3D024h	CPTS	CPTS_INTSTAT_MASKED	Interrupt Status Masked Register	Section 3.5.4.10
3D028h	CPTS	CPTS_INT_ENABLE	Interrupt Enable Register	Section 3.5.4.11
3D02Ch	Reserved	Reserved	Reserved	Reserved
3D030h	CPTS	CPTS_EVENT_POP	Event Interrupt Pop Register	Section 3.5.4.12
3D034h	CPTS	CPTS_EVENT_INFO0	Lower 32-bits of the event timestamp value	Section 3.5.4.13
3D038h	CPTS	CPTS_EVENT_INFO1	Event Information Register	Section 3.5.4.14
3D03Ch	CPTS	CPTS_EVENT_INFO2	Additional Event Information Register	Section 3.5.4.15
3D040h	CPTS	CPTS_EVENT_INFO3	Upper 32-bits of the Event Timestamp Value (64-bit mode only)	Section 3.5.4.16
3D044h	CPTS	CPTS_TS_LOAD_VAL_H	Time Stamp Load Value Register (upper 32 bits)	Section 3.5.4.17
3D048h	CPTS	CPTS_TS_COMP_VAL_H	Time Stamp Comparison Value Register (upper 32 bits)	Section 3.5.4.18
3D04Ch-3DFFCh	Reserved	Reserved	Reserved	Reserved
3E000h	ALE	ALE_IDVER	Address Lookup Engine ID/Version Register	Section 3.5.5.1
3E004h	ALE	ALE_STATUS	Address Lookup Engine Status Register	Section 3.5.5.2
3E008h	ALE	ALE_CONTROL	Address Lookup Engine Control Register	Section 3.5.5.3
3E00Ch	Reserved	Reserved	Reserved	Reserved
3E010h	ALE	ALE_PRESCALE	Address Lookup Engine Prescale Register	Section 3.5.5.4
3E014h	ALE	ALE_AGING_TIMER	Address Lookup Engine Aging Timer Register	Section 3.5.5.5
3E018h-3E01Ch	Reserved	Reserved	Reserved	Reserved
3E020h	ALE	ALE_TBLCTL	Address Lookup Engine Table Control	Section 3.5.5.7
3E024h-3E030h	Reserved	Reserved	Reserved	Reserved
3E034h	ALE	ALE_TBLW2	Address Lookup Engine Table Word 2 Register	Section 3.5.5.8
3E038h	ALE	ALE_TBLW1	Address Lookup Engine Table Word 1 Register	Section 3.5.5.9
3E03Ch	ALE	ALE_TBLW0	Address Lookup Engine Table Word 0 Register	Section 3.5.5.10
3E040h	ALE	ALE_PORTCTL0	Address Lookup Engine Port 0 Control Register	Section 3.5.5.11
3E044h	ALE	ALE_PORTCTL1	Address Lookup Engine Port 1 Control Register	Section 3.5.5.11
3E048h	ALE	ALE_PORTCTL2	Address Lookup Engine Port 2 Control Register	Section 3.5.5.11
3E04Ch	ALE	ALE_PORTCTL3	Address Lookup Engine Port 3 Control Register	Section 3.5.5.11

Table 3-2. Gigabit Ethernet Switch Subsystem Complete Register Listing (continued)

Offset Address[(1)]	Module	Acronym	Register Name	Section
3E050h	ALE	ALE_PORTCTL4	Address Lookup Engine Port 4 Control Register	Section 3.5.5.11
3E054h	ALE	ALE_PORTCTL5	Address Lookup Engine Port 5 Control Register	
3E058h	ALE	ALE_PORTCTL6	Address Lookup Engine Port 6 Control Register	Section 3.5.5.11
3E05Ch	ALE	ALE_PORTCTL7	Address Lookup Engine Port 7 Control Register	Section 3.5.5.11
3E060h	ALE	ALE_PORTCTL8	Address Lookup Engine Port 8 Control Register	Section 3.5.5.11
3E064h-3EF8Ch	Reserved	Reserved	Reserved	Reserved
3E090h	ALE	ALE_UNKN_VLAN_MBR_LIST	Address Lookup Engine Unknown VLAN Member List Register	Section 3.5.5.12
3E094h	ALE	ALE_UNKN_VLAN_MLT_FLOOD	Address Lookup Engine Unknown VLAN Multicast Flood Mask Register	Section 3.5.5.13
3E098h	ALE	ALE_UNKN_VLAN_REG_MLT_FLOOD	Address Lookup Engine Unknown VLAN Registered Multicast Flood Mask Register	Section 3.5.5.14
3E09Ch	ALE	ALE_UNKN_VLAN_FORCE_UNTAG_EGR	Address Lookup Engine Unknown VLAN Force Untagged Egress Register	Section 3.5.5.15
3E0A0h-3E0BC	Reserved	Reserved	Reserved	Reserved
3E0C0h	ALE	ALE_VLAN_MASK_MUX0	Address Lookup Engine Mask Mux 0 Select Register	Section 3.5.5.16
3E0C4h	ALE	ALE_VLAN_MASK_MUX1	Address Lookup Engine Mask Mux 1 Select Register	Section 3.5.5.16
3E0C8h	ALE	ALE_VLAN_MASK_MUX2	Address Lookup Engine Mask Mux 2 Select Register	Section 3.5.5.16
3E0CCh	ALE	ALE_VLAN_MASK_MUX3	Address Lookup Engine Mask Mux 3 Select Register	Section 3.5.5.16
3E0D0h	ALE	ALE_VLAN_MASK_MUX4	Address Lookup Engine Mask Mux 4 Select Register	Section 3.5.5.16
3E0D4h	ALE	ALE_VLAN_MASK_MUX5	Address Lookup Engine Mask Mux 5 Select Register	Section 3.5.5.16
3E0D8h	ALE	ALE_VLAN_MASK_MUX6	Address Lookup Engine Mask Mux 6 Select Register	Section 3.5.5.16
3E0DCh	ALE	ALE_VLAN_MASK_MUX7	Address Lookup Engine Mask Mux 7 Select Register	Section 3.5.5.16
3E0E0h-3EFFC	Reserved	Reserved	Reserved	Reserved
3F000h	ECC Module	ECC_REVISION	ECC Module Revision Register	Section 3.5.6.1
3F004h	Reserved	Reserved	Reserved	Reserved
3F008h	ECC Module	ECC_VECTOR	ECC Module Vector Register	Section 3.5.6.2
3F00Ch	ECC Module	ECC_STATUS	ECC Module Status Register	Section 3.5.6.3
3F010h	ECC Module	ECC_WRAPPER_REVISION	ECC Module Wrapper Revision Register	Section 3.5.6.4
3F014h	ECC Module	ECC_CTRL	ECC Module Control Register	Section 3.5.6.5
3F018h	ECC Module	ECC_ERR_CTRL1	ECC Module Error Control 1 Register	Section 3.5.6.6
3F01Ch	ECC Module	ECC_ERR_CTRL2	ECC Module Error Control 2 Register	Section 3.5.6.7

Table 3-2. Gigabit Ethernet Switch Subsystem Complete Register Listing (continued)

Offset Address[(1)]	Module	Acronym	Register Name	Section
3F020h	ECC Module	ECC_ERR_STATUS1	ECC Module Error Status 1 Register	Section 3.5.6.8
3F024h	ECC Module	ECC_ERR_STATUS2	ECC Module Error Status 2 Register	Section 3.5.6.9
3F028h-3F038	Reserved	Reserved	Reserved	Reserved
3F03Ch	ECC Module	ECC_EOI	ECC Module EOI Register	Section 3.5.6.10
3F040h	ECC Module	ECC_INT_STATUS	ECC Module Interrupt Status Register	Section 3.5.6.11
3F044h-3F07C	Reserved	Reserved	Reserved	Reserved
3F080h	ECC Module	ECC_INT_EN_SET	ECC Module Interrupt Enable Set Register	Section 3.5.6.12
3F084h-3F0BC	Reserved	Reserved	Reserved	Reserved
3F0C0h	ECC Module	ECC_INT_EN_CLEAR	ECC Module Interrupt Enable Clear Register	Section 3.5.6.13
3F0C4h-3F0FC	Reserved	Reserved	Reserved	Reserved

Table 3-3 lists all the registers for each external Ethernet port. In a 5 port switch there are 4 external Ethernet ports and in a 9 port switch there are 8 external Ethernet ports. Check your device specific data manual to see if you device has a 5 port or 9 port switch. The port registers for host port 0 are listed above in Table 3-2.

Table 3-3. Ethernet Port n Complete Register Listing (n = 1 to 4 in a 5 port switch or n = 1 to 8 in a 9 port switch)

Offset Address[1]	Module	Acronym	Register Name	Section
000h	Reserved	Reserved	Reserved	Reserved
004h	Ethernet Port n	Pn_CONTROL	Ethernet Port n Control Register	Section 3.5.2.1
008h -00Ch	Reserved	Reserved	Reserved	Reserved
010h	Ethernet Port n	Pn_BLK_CNT	Ethernet Port n FIFO Block Usage Count	Section 3.5.2.2
014h	Ethernet Port n	Pn_PORT_VLAN	Ethernet Port n VLAN Register	Section 3.5.2.3
018h	Ethernet Port n	Pn_TX_PRI_MAP	Ethernet Port n Transmit Header Priority to Switch Priority Mapping Register	Section 3.5.2.4
01Ch	Ethernet Port n	Pn_PRI_CTL	Ethernet Port n Priority Control Register	Section 3.5.2.5
020h	Ethernet Port n	Pn_RX_PRI_MAP	Ethernet Port n Receive Packet Priority to Header Priority Mapping Register	Section 3.5.2.6
024h	Ethernet Port n	Pn_RX_MAXLEN	Ethernet Port n Receive Frame Max Length Register	Section 3.5.2.7
028h	Ethernet Port n	Pn_TX_BLKS_PRI	Ethernet Port n Transmit Block Sub Per Priority Register	Section 3.5.2.8
02Ch -11Ch	Reserved	Reserved	Reserved	Reserved
120h	Ethernet Port n	Pn_RX_DSCP_MAP0	Ethernet Port n Receive IPv4/IPv6 DSCP Priority Mapping Register 0	Section 3.5.2.9
124h	Ethernet Port n	Pn_RX_DSCP_MAP1	Ethernet Port n Receive IPv4/IPv6 DSCP Priority Mapping Register 1	Section 3.5.2.10
128h	Ethernet Port n	Pn_RX_DSCP_MAP2	Ethernet Port n Receive IPv4/IPv6 DSCP Priority Mapping Register 2	Section 3.5.2.11
12Ch	Ethernet Port n	Pn_RX_DSCP_MAP3	Ethernet Port n Receive IPv4/IPv6 DSCP Priority Mapping Register 3	Section 3.5.2.12
130h	Ethernet Port n	Pn_RX_DSCP_MAP4	Ethernet Port n Receive IPv4/IPv6 DSCP Priority Mapping Register 4	Section 3.5.2.13
134h	Ethernet Port n	Pn_RX_DSCP_MAP5	Ethernet Port n Receive IPv4/IPv6 DSCP Priority Mapping Register 5	Section 3.5.2.14
138h	Ethernet Port n	Pn_RX_DSCP_MAP6	Ethernet Port n Receive IPv4/IPv6 DSCP Priority Mapping Register 6	Section 3.5.2.15
13Ch	Ethernet Port n	Pn_RX_DSCP_MAP7	Ethernet Port n Receive IPv4/IPv6 DSCP Priority Mapping Register 7	Section 3.5.2.16
140h	Ethernet Port n	Pn_PRI0_SEND	Ethernet Port n Receive Priority 0 Send Count Value Register	Section 3.5.2.17
144h	Ethernet Port n	Pn_PRI1_SEND	Ethernet Port n Receive Priority 1 Send Count Value Register	Section 3.5.2.18
148h	Ethernet Port n	Pn_PRI2_SEND	Ethernet Port n Receive Priority 2 Send Count Value Register	Section 3.5.2.19
14Ch	Ethernet Port n	Pn_PRI3_SEND	Ethernet Port n Receive Priority 3 Send Count Value Register	Section 3.5.2.20
150h	Ethernet Port n	Pn_PRI4_SEND	Ethernet Port n Receive Priority 4 Send Count Value Register	Section 3.5.2.21

[1] The offsets listed in this table are offsets based on the Ethernet port n starting address found in Table 3-2.

Table 3-3. Ethernet Port n Complete Register Listing (n = 1 to 4 in a 5 port switch or n = 1 to 8 in a 9 port switch) (continued)

Offset Address[1]	Module	Acronym	Register Name	Section
154h	Ethernet Port n	Pn_PRI5_SEND	Ethernet Port n Receive Priority 5 Send Count Value Register	Section 3.5.2.22
158h	Ethernet Port n	Pn_PRI6_SEND	Ethernet Port n Receive Priority 6 Send Count Value Register	Section 3.5.2.23
15Ch	Ethernet Port n	Pn_PRI7_SEND	Ethernet Port n Receive Priority 7 Send Count Value Register	Section 3.5.2.24
160h	Ethernet Port n	Pn_PRI0_IDLE	Ethernet Port n Receive Priority 0 Idle Count Value Register	Section 3.5.2.25
164h	Ethernet Port n	Pn_PRI1_IDLE	Ethernet Port n Receive Priority 1 Idle Count Value Register	Section 3.5.2.26
168h	Ethernet Port n	Pn_PRI2_IDLE	Ethernet Port n Receive Priority 2 Idle Count Value Register	Section 3.5.2.27
16Ch	Ethernet Port n	Pn_PRI3_IDLE	Ethernet Port n Receive Priority 3 Idle Count Value Register	Section 3.5.2.28
170h	Ethernet Port n	Pn_PRI4_IDLE	Ethernet Port n Receive Priority 4 Idle Count Value Register	Section 3.5.2.29
174h	Ethernet Port n	Pn_PRI5_IDLE	Ethernet Port n Receive Priority 5 Idle Count Value Register	Section 3.5.2.30
178h	Ethernet Port n	Pn_PRI6_IDLE	Ethernet Port n Receive Priority 6 Idle Count Value Register	Section 3.5.2.31
17Ch	Ethernet Port n	Pn_PRI7_IDLE	Ethernet Port n Receive Priority 7 Idle Count Value Register	Section 3.5.2.32
180h	Ethernet Port n	Pn_TX_DEST_THRESH_SET_L	Ethernet Port n Transmit Destination Threshold Set Low Register	Section 3.5.2.33
184h	Ethernet Port n	Pn_TX_DEST_THRESH_SET_H	Ethernet Port n Transmit Destination Threshold Set High Register	Section 3.5.2.34
188h	Ethernet Port n	Pn_TX_DEST_THRESH_CLR_L	Ethernet Port n Transmit Destination Threshold Clear Low Register	Section 3.5.2.35
18Ch	Ethernet Port n	Pn_TX_DEST_THRESH_CLR_H	Ethernet Port n Transmit Destination Threshold Clear High Register	Section 3.5.2.36
190h	Ethernet Port n	Pn_TX_BUFFER_THRESH_SET_L	Ethernet Port n Global Transmit Buffer Threshold Set Register Low	Section 3.5.2.37
194h	Ethernet Port n	Pn_TX_BUFFER_THRESH_SET_H	Ethernet Port n Global Transmit Buffer Threshold Set Register High	Section 3.5.2.38
198h	Ethernet Port n	Pn_TX_BUFFER_THRESH_CLR_L	Ethernet Port n Global Transmit Buffer Threshold Clear Register Low	Section 3.5.2.39
19Ch	Ethernet Port n	Pn_TX_BUFFER_THRESH_CLR_H	Ethernet Port n Global Transmit Buffer Threshold Clear Register High	Section 3.5.2.40
1A0h -2FCh	Reserved	Reserved	Reserved	Reserved
300h	Ethernet Port n	Pn_TX_DEST_OUTFLOW_ADDVAL_L	Ethernet Port n Transmit Destination Out Flow Add Values Register Low	Section 3.5.2.44
304h	Ethernet Port n	Pn_TX_DEST_OUTFLOW_ADDVAL_H	Ethernet Port n Transmit Destination Out Flow Add Values Register High	Section 3.5.2.45
308h	Ethernet Port n	Pn_PAUSE_SA_L	Ethernet Port n Pause Frame Source Address Register Low	Section 3.5.2.46
30Ch	Ethernet Port n	Pn_PAUSE_SA_H	Ethernet Port n Pause Frame Source Address Register High	Section 3.5.2.47
310h	Ethernet Port n	Pn_TS_CTL	Ethernet Port n Time Sync Control Register	Section 3.5.2.48
314h	Ethernet Port n	Pn_TS_SEQ_LTYPE	Ethernet Port n Time Sync LTYPE and SEQ_ID_OFFSET register	Section 3.5.2.49
318h	Ethernet Port n	Pn_TS_VLAN	Ethernet Port n Time Sync VLAN LTYPE1 and VLAN LTYPE2 Register	Section 3.5.2.50

Table 3-3. Ethernet Port n Complete Register Listing (n = 1 to 4 in a 5 port switch or n = 1 to 8 in a 9 port switch) (continued)

Offset Address[(1)]	Module	Acronym	Register Name	Section
31Ch	Ethernet Port n	Pn_TS_CTL_LTYPE2	Ethernet Port n Time Sync Control and LTYPE2 Register	Section 3.5.2.51
320h	Ethernet Port n	Pn_TS_CTL2	Ethernet Port n Time Sync Control 2 Register	Section 3.5.2.52
324h -32Ch	Reserved	Reserved	Reserved	Reserved
330h	Ethernet Port n	Pn_MAC_CTL	Ethernet Port n MAC Control Register	Section 3.5.2.53
334h	Ethernet Port n	Pn_MAC_STATUS	Ethernet Port n MAC Status Register	Section 3.5.2.54
338h	Ethernet Port n	Pn_MAC_SOFT_RESET	Ethernet Port n MAC Soft Reset Register	Section 3.5.2.55
33Ch	Ethernet Port n	Pn_MAC_BACKOFF_TEST	Ethernet Port n MAC Backoff Test Register	Section 3.5.2.56
340h	Ethernet Port n	Pn_MAC_RX_PAUSETIMER	Ethernet Port n 802.3 Receive Pause Timer Register	Section 3.5.2.57
344h -34Ch	Reserved	Reserved	Reserved	Reserved
350h	Ethernet Port n	Pn_MAC_RX_PRI0_PAUSETIMER	Ethernet Port n Priority Flow Control Priority 0 Receive Pause Timer Register	Section 3.5.2.58
354h	Ethernet Port n	Pn_MAC_RX_PRI1_PAUSETIMER	Ethernet Port n Priority Flow Control Priority 1 Receive Pause Timer Register	Section 3.5.2.59
358h	Ethernet Port n	Pn_MAC_RX_PRI2_PAUSETIMER	Ethernet Port n Priority Flow Control Priority 2 Receive Pause Timer Register	Section 3.5.2.60
35Ch	Ethernet Port n	Pn_MAC_RX_PRI3_PAUSETIMER	Ethernet Port n Priority Flow Control Priority 3 Receive Pause Timer Register	Section 3.5.2.61
360h	Ethernet Port n	Pn_MAC_RX_PRI4_PAUSETIMER	Ethernet Port n Priority Flow Control Priority 4 Receive Pause Timer Register	Section 3.5.2.62
364h	Ethernet Port n	Pn_MAC_RX_PRI5_PAUSETIMER	Ethernet Port n Priority Flow Control Priority 5 Receive Pause Timer Register	Section 3.5.2.63
368h	Ethernet Port n	Pn_MAC_RX_PRI6_PAUSETIMER	Ethernet Port n Priority Flow Control Priority 6 Receive Pause Timer Register	Section 3.5.2.64
36Ch	Ethernet Port n	Pn_MAC_RX_PRI7_PAUSETIMER	Ethernet Port n Priority Flow Control Priority 7 Receive Pause Timer Register	Section 3.5.2.65
370h	Ethernet Port n	Pn_MAC_TX_PAUSETIMER	Ethernet Port n 802.3 Transmit Pause Timer Register	Section 3.5.2.66
374h -37Ch	Reserved	Reserved	Reserved	Reserved
380h	Ethernet Port n	Pn_MAC_TX_PRI0_PAUSETIMER	Ethernet Port n Priority Flow Control Priority 0 Transmit Pause Timer Register	Section 3.5.2.67
384h	Ethernet Port n	Pn_MAC_TX_PRI1_PAUSETIMER	Ethernet Port n Priority Flow Control Priority 1 Transmit Pause Timer Register	Section 3.5.2.68
388h	Ethernet Port n	Pn_MAC_TX_PRI2_PAUSETIMER	Ethernet Port n Priority Flow Control Priority 2 Transmit Pause Timer Register	Section 3.5.2.69
38Ch	Ethernet Port n	Pn_MAC_TX_PRI3_PAUSETIMER	Ethernet Port n Priority Flow Control Priority 3 Transmit Pause Timer Register	Section 3.5.2.70
390h	Ethernet Port n	Pn_MAC_TX_PRI4_PAUSETIMER	Ethernet Port n Priority Flow Control Priority 4 Transmit Pause Timer Register	Section 3.5.2.71
394h	Ethernet Port n	Pn_MAC_TX_PRI5_PAUSETIMER	Ethernet Port n Priority Flow Control Priority 5 Transmit Pause Timer Register	Section 3.5.2.72
398h	Ethernet Port n	Pn_MAC_TX_PRI6_PAUSETIMER	Ethernet Port n Priority Flow Control Priority 6 Transmit Pause Timer Register	Section 3.5.2.73
39Ch	Ethernet Port n	Pn_MAC_TX_PRI7_PAUSETIMER	Ethernet Port n Priority Flow Control Priority 7 Transmit Pause Timer Register	Section 3.5.2.74

Table 3-3. Ethernet Port n Complete Register Listing (n = 1 to 4 in a 5 port switch or n = 1 to 8 in a 9 port switch) (continued)

Offset Address[1]	Module	Acronym	Register Name	Section
3A0h	Ethernet Port n	Pn_MAC_EMCONTROL	Ethernet Port n MAC Emulation Control Register	Section 3.5.2.75
3A4h	Ethernet Port n	Pn_MAC_TX_GAP	Ethernet Port n MAC Transmit Inter Packet Gap Register	Section 3.5.2.76
3A8h -FFCh	Reserved	Reserved	Reserved	Reserved

Table 3-4 lists the statistics registers for each external Ethernet port. In a 5 port switch there are 4 external Ethernet ports and in a 9 port switch there are 8 external Ethernet ports. Check your device specific data manual to see if you device has a 5 port or 9 port switch. The statistics registers for host port 0 are listed above in Table 3-2.

Table 3-4. Ethernet Port n Statistics Register Listing (n = 1 to 8)

Offset Address[(1)]	Module	Acronym	Register Name	Section
000h	STATn	STATn_RXGOODFRAMES	Total number of good frames received	Section 3.5.3.1
004h	STATn	STATn_RXBROADCASTFRAMES	Total number of good broadcast frames received	Section 3.5.3.2
008h	STATn	STATn_RXMULTICASTFRAMES	Total number of good multicast frames received	Section 3.5.3.3
00Ch	STATn	STATn_RXPAUSEFRAMES	Total number of pause frames received	Section 3.5.3.4
010h	STATn	STATn_RXCRCERRORS	Total number of CRC errors received	Section 3.5.3.5
014h	STATn	STATn_RXALIGNCODEERRORS	Total number of align/code errors received	Section 3.5.3.6
018h	STATn	STATn_RXOVERSIZEDFRAMES	Total number of oversized frames received	Section 3.5.3.7
01Ch	STATn	STATn_RXJABBERFRAMES	Total number of jabber frames received	Section 3.5.3.8
020h	STATn	STATn_RXUNDERSIZEDFRAMES	Total number of undersized frames received	Section 3.5.3.9
024h	STATn	STATn_RXFRAGMENTS	Total number of fragments received	Section 3.5.3.10
028h	STATn	STATn_ALE_DROP	Total number of frames dropped by the ALE	Section 3.5.3.11
02Ch	STATn	STATn_ALE_OVERRUN_DROP	Total number of frames dropped due to exceeding the maximum ALE lookup rate	Section 3.5.3.12
030h	STATn	STATn_RXOCTETS	Total number of received bytes in good frames	Section 3.5.3.13
034h	STATn	STATn_TXGOODFRAMES	Total number of good frames transmitted	Section 3.5.3.14
038h	STATn	STATn_TXBROADCASTFRAMES	Total number of good broadcast frames transmitted	Section 3.5.3.15
03Ch	STATn	STATn_TXMULTICASTFRAMES	Total number of good multicast frames transmitted	Section 3.5.3.16
040h	STATn	STATn_TXPAUSEFRAMES	Total number of pause transmit frames	Section 3.5.3.17
044h	STATn	STATn_TXDEFERREDFRAMES	Total number of deferred transmit frames	Section 3.5.3.18
048h	STATn	STATn_TXCOLLISIONFRAMES	Total number of collisions	Section 3.5.3.19
04Ch	STATn	STATn_TXSINGLECOLLISIONFRAMES	Total number of single collision transmit frames	Section 3.5.3.20
050h	STATn	STATn_TXMULTCOLLISIONFRAMES	Total number of multiple collision transmit frames	Section 3.5.3.21
054h	STATn	STATn_TXEXCESSIVECOLLISIONFRAMES	Total number of excessive collision transmit frames	Section 3.5.3.22
058h	STATn	STATn_TXLATECOLLISIONFRAMES	Total number of late collisions	Section 3.5.3.23
05Ch	Reserved	Reserved	Reserved	Reserved
060h	STATn	STATn_TXCARRIERSENSEERRORS	Total number of carrier sense errors	Section 3.5.3.24

(1) The offsets listed in this table are offsets based on the STATn starting address found in Table 3-2.

Table 3-4. Ethernet Port n Statistics Register Listing (n = 1 to 8) (continued)

Offset Address[1]	Module	Acronym	Register Name	Section
064h	STATn	STATn_TXOCTETS	Total number of octets transmitted	Section 3.5.3.25
068h	STATn	STATn_64OCTETFRAMES	Total number of 64 octet frames transmitted and received on the port	Section 3.5.3.26
06Ch	STATn	STATn_65T127OCTETFRAMES	Total number of 65-127 octet frames transmitted and received on the port	Section 3.5.3.27
070h	STATn	STATn_128T255OCTETFRAMES	Total number of 128-255 octet frames transmitted and received on the port	Section 3.5.3.28
074h	STATn	STATn_256T511OCTETFRAMES	Total number of 256-511 octet frames transmitted and received on the port	Section 3.5.3.29
078h	STATn	STATn_512T1023OCTETFRAMES	Total number of 512-1023 octet frames transmitted and received on the port	Section 3.5.3.30
07Ch	STATn	STATn_1024TUPOCTETFRAMES	Total number of 1023-(P0_RX_MAXLEN) octet frames transmitted and received on the port	Section 3.5.3.31
080h	STATn	STATn_NETOCTETS	Total number of bytes of frame data received and transmitted on the port	Section 3.5.3.32
084h	STATn	STATn_RX_BOTTOM_FIFO_DROP	Total number of frames received at port 0 that were dropped because they overran the receive FIFO	Section 3.5.3.33
088h	STATn	STATn_PORTMASK_DROP	Total number of frames received at port 0 that were dropped by the ALE	Section 3.5.3.34
08Ch	STATn	STATn_RX_TOP_FIFO_DROP	Total number of frames received at port 0 that were dropped due to a start of frame (SOF) overrun on any destination port egress	Section 3.5.3.35
090h	STATn	STATn_ALE_RATE_LIMIT_DROP	Total number of frames that were dropped due to receive rate limiting on port 0 or transmit rate limiting on any destination port	Section 3.5.3.36
094h	STATn	STATn_ALE_VID_INGRESS_DROP	Total number of frames that were dropped due to VLAN ingress check failure	Section 3.5.3.37
098h	STATn	STATn_ALE_DA_EQ_SA_DROP	Total number of frames that were dropped due to destination address being the same as source address	Section 3.5.3.38
09Ch-0A4h	Reserved	Reserved	Reserved	Reserved
0A8h	STATn	STATn_ALE_UNKN_UNI	Total number of frames received at port 0 that had a unicast destination address with an unknown source address	Section 3.5.3.39
0ACh	STATn	STATn_ALE_UNKN_UNI_BCNT	Total number of bytes contained in the frames that qualify for the P0_ALE_UNKN_UNI register	Section 3.5.3.40
0B0h	STATn	STATn_ALE_UNKN_MLT	Total number of frames received at port 0 that had a multicast destination address with an unknown source address	Section 3.5.3.41
0B4h	STATn	STATn_ALE_UNKN_MLT_BCNT	Total number of bytes contained in the frames that qualify for the P0_ALE_UNKN_MLT register	Section 3.5.3.42
0B8h	STATn	STATn_ALE_UNKN_BRD	Total number of frames received at port 0 that had a broadcast destination address with an unknown source address	Section 3.5.3.43
0BCh	STATn	STATn_ALE_UNKN_BRD_BCNT	Total number of bytes contained in the frames that qualify for the P0_ALE_UNKN_BRD register	Section 3.5.3.44
0C0h-178h	Reserved	Reserved	Reserved	Reserved
17Ch	STATn	STATn_TX_MEM_PROTECT_ERROR	Total number of frames transmitted that had a memory protect CRC error on egress	Section 3.5.3.45
180h	STATn	STATn_TX_PRI0	Total number of packets transmitted with Priority 0	Section 3.5.3.46
184h	STATn	STATn_TX_PRI1	Total number of packets transmitted with Priority 1	Section 3.5.3.46

Table 3-4. Ethernet Port n Statistics Register Listing (n = 1 to 8) (continued)

Offset Address[(1)]	Module	Acronym	Register Name	Section
188h	STATn	STATn_TX_PRI2	Total number of packets transmitted with Priority 2	Section 3.5.3.46
18Ch	STATn	STATn_TX_PRI3	Total number of packets transmitted with Priority 3	Section 3.5.3.46
190h	STATn	STATn_TX_PRI4	Total number of packets transmitted with Priority 4	Section 3.5.3.46
194h	STATn	STATn_TX_PRI5	Total number of packets transmitted with Priority 5	Section 3.5.3.46
198h	STATn	STATn_TX_PRI6	Total number of packets transmitted with Priority 6	Section 3.5.3.46
19Ch	STATn	STATn_TX_PRI7	Total number of packets transmitted with Priority 7	Section 3.5.3.46
1A0h	STATn	STATn_TX_PRI0_BCNT	Total number of bytes transmitted with Priority 0	Section 3.5.3.47
1A4h	STATn	STATn_TX_PRI1_BCNT	Total number of bytes transmitted with Priority 1	Section 3.5.3.47
1A8h	STATn	STATn_TX_PRI2_BCNT	Total number of bytes transmitted with Priority 2	Section 3.5.3.47
1ACh	STATn	STATn_TX_PRI3_BCNT	Total number of bytes transmitted with Priority 3	Section 3.5.3.47
1B0h	STATn	STATn_TX_PRI4_BCNT	Total number of bytes transmitted with Priority 4	Section 3.5.3.47
1B4h	STATn	STATn_TX_PRI5_BCNT	Total number of bytes transmitted with Priority 5	Section 3.5.3.47
1B8h	STATn	STATn_TX_PRI6_BCNT	Total number of bytes transmitted with Priority 6	Section 3.5.3.47
1BCh	STATn	STATn_TX_PRI7_BCNT	Total number of bytes transmitted with Priority 7	Section 3.5.3.47
1C0h	STATn	STATn_TX_PRI0_DROP	Total number of packets dropped during transmit with Priority 0	Section 3.5.3.48
1C4h	STATn	STATn_TX_PRI1_DROP	Total number of packets dropped during transmit with Priority 1	Section 3.5.3.48
1C8h	STATn	STATn_TX_PRI2_DROP	Total number of packets dropped during transmit with Priority 2	Section 3.5.3.48
1CCh	STATn	STATn_TX_PRI3_DROP	Total number of packets dropped during transmit with Priority 3	Section 3.5.3.48
1D0h	STATn	STATn_TX_PRI4_DROP	Total number of packets dropped during transmit with Priority 4	Section 3.5.3.48
1D4h	STATn	STATn_TX_PRI5_DROP	Total number of packets dropped during transmit with Priority 5	Section 3.5.3.48
1D8h	STATn	STATn_TX_PRI6_DROP	Total number of packets dropped during transmit with Priority 6	Section 3.5.3.48
1DCh	STATn	STATn_TX_PRI7_DROP	Total number of packets dropped during transmit with Priority 7	Section 3.5.3.48
1E0h	STATn	STATn_TX_PRI0_DROP_BCNT	Total number of bytes dropped during transmit with Priority 0	Section 3.5.3.49
1E4h	STATn	STATn_TX_PRI1_DROP_BCNT	Total number of bytes dropped during transmit with Priority 1	Section 3.5.3.49
1E8h	STATn	STATn_TX_PRI2_DROP_BCNT	Total number of bytes dropped during transmit with Priority 2	Section 3.5.3.49
1ECh	STATn	STATn_TX_PRI3_DROP_BCNT	Total number of bytes dropped during transmit with Priority 3	Section 3.5.3.49
1F0h	STATn	STATn_TX_PRI4_DROP_BCNT	Total number of bytes dropped during transmit with Priority 4	Section 3.5.3.49

Table 3-4. Ethernet Port n Statistics Register Listing (n = 1 to 8) (continued)

Offset Address[(1)]	Module	Acronym	Register Name	Section
1F4h	STATn	STATn_TX_PRI5_DROP_BCNT	Total number of bytes dropped during transmit with Priority 5	Section 3.5.3.49
1F8h	STATn	STATn_TX_PRI6_DROP_BCNT	Total number of bytes dropped during transmit with Priority 6	Section 3.5.3.49
1FCh	STATn	STATn_TX_PRI7_DROP_BCNT	Total number of bytes dropped during transmit with Priority 7	Section 3.5.3.49

3.2 Gigabit Ethernet (GbE) Switch Subsystem Module

This section describes the registers for the gigabit Ethernet switch subsystem.

Table 3-5 lists the registers in the gigabit Ethernet switch subsystem and the corresponding offset address for each register.

Table 3-5. Ethernet Switch Subsystem Module

Offset Address[(1)]	Acronym	Register Name	Section
000h	ES_SS_IDVER	Ethernet switch subsystem Identification and Version Register	Section 3.2.1
004h	ES_SS_SYNCE_COUNT	Ethernet switch subsystem Synchronous Ethernet Count Register	Section 3.2.2
008h	ES_SS_SYNCE_MUX	Ethernet switch subsystem Synchronous Ethernet Clock Select Register	Section 3.2.3
00Ch-0FCh	Reserved	Reserved	Reserved

(1) The actual addresses of these registers are device specific. See your device-specific data manual to verify the register addresses.

3.2.1 Ethernet Switch Subsystem Identification and Version Register (ES_SS_IDVER)

The gigabit Ethernet switch subsystem Identification and Version Register is shown in Figure 3-1 and described in Table 3-6.

Figure 3-1. Ethernet Switch Subsystem Identification and Version Register (ES_SS_IDVER)

31	16
ES_SS_IDENT	
R-4EE6h	

15	11	10	8	7	0
ES_SS_RTL_VER		ES_SS_MAJ_VER		ES_SS_MINOR_VER	
R-7h or R-8h		R-1h		R-0h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-6. Ethernet Switch Subsystem Identification and Version Register (ES_SS_IDVER) Field Descriptions

Bits	Field	Description
31-16	ES_SS_IDENT	Ethernet switch subsystem identification value
15-11	ES_SS_RTL_VER	Ethernet switch subsystem RTL version value . 5 port switch has a default value of 7 in these bits and 9 port switch has a default value of 8 in these bits.
10-8	ES_SS_MAJ_VER	Ethernet switch subsystem major version value
7-0	ES_SS_MINOR_VER	Ethernet switch subsystem minor version value

3.2.2 Ethernet Switch Subsystem Synchronous Ethernet Count Register (ES_SS_SYNCE_COUNT)

The gigabit Ethernet switch subsystem Synchronous Ethernet Count Register is shown in Figure 3-2 and described in Table 3-7.

Figure 3-2. Ethernet Switch Subsystem Synchronous Ethernet Count Register (ES_SS_SYNCE_COUNT)

31	0
SYNCE_CNT	
R/W-0h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-7. Ethernet Switch Subsystem Synchronous Ethernet Count Register (ES_SS_SYNCE_COUNT) Field Descriptions

Bits	Field	Description
31-0	SYNCE_CNT	Synchronous Ethernet Count Value - This value determines the toggle rate of the TS_SYNCE output. When this value is zero the TS_SYNCE output is disabled (low). When this value is non-zero, the TS_SYNCE output toggles each time the SYCNE_CNT value is reached. If this value is to be changed to another non-zero value then it should be written with a zero value before writing the new non-zero value.

3.2.3 Ethernet Switch Subsystem Synchronous Ethernet Clock Select Register (ES_SS_SYNCE_MUX)

The gigabit Ethernet switch subsystem Synchronous Ethernet Count Register is shown in Figure 3-3 and described in Table 3-8.

Figure 3-3. Ethernet Switch Subsystem Synchronous Ethernet Clock Select Register (ES_SS_SYNCE_MUX)

31	3	2	0
Reserved		SYNCE_SEL	
R-0h		R/W-0h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-8. Ethernet Switch Subsystem Synchronous Ethernet Clock Select Register (ES_SS_SYNCE_MUX) Field Descriptions

Bits	Field	Description
31-3	Reserved	Reserved
2-0	SYNCE_SEL	Synchronous Ethernet Select Value - This value selects the receive clock used to clock the TS_SYNCE counter and output. • 000 - Select RXBLCK[0] • 001 - Select RXBLCK[1] • 010 - Select RXBLCK[2] • 011 - Select RXBLCK[3] • 100 - Select RXBLCK[4] • 101 - Select RXBLCK[5] • 110 - Select RXBLCK[6] • 111 - Select RXBLCK[7]

3.3 Serial Gigabit Media Independent Interface (SGMII) module

This section describes the registers available in the gigabit Ethernet switch subsystem SGMII module.

There are four (in a 5 port switch) or eight (in a 9 port switch) SGMII modules in the gigabit Ethernet switch subsystem, each with its own set of identical registers. The register address offsets listed in Table 3-9 are relative to the SGMII module. See Table 3-1 for the address offset of each SGMII module. A complete list of all of the registers in the GbE switch subsystem is provided in Table 3-2.

Table 3-9 lists the registers in the SGMII module and the corresponding address offset for each register.

Table 3-9. SGMII Registers

Offset Address[1]	Acronym	Register Name	Section
00h	SGMII_IDVER	Identification and Version Register	Section 3.3.1
04h	SGMII_SOFT_RESET	Soft Reset Register	Section 3.3.2
08h-0Ch	Reserved	Reserved	Reserved
10h	SGMII_CONTROL	Control Register	Section 3.3.3
14h	SGMII_STATUS	Status Register (read only)	Section 3.3.4
18h	SGMII_MR_ADV_ABILITY	Advertised Ability Register	Section 3.3.5
1Ch	SGMII_MR_NP_TX	Transmit Next Page Register	Section 3.3.6
20h	SGMII_MR_LP_ADV_ABILITY	Link Partner Advertised Ability (read only)	Section 3.3.7
24h	SGMII_MR_NP_RX	Link Partner Receive Next Page Register (read only)	Section 3.3.8
28h-FCh	Reserved	Reserved	Reserved

(1) The actual addresses of these registers are device specific. See your device-specific data manual to verify the register addresses.

3.3.1 SGMII Identification and Version Register (SGMII_IDVER)

The SGMII Identification and Version Register is shown in Figure 3-4 and described in Table 3-10.

Figure 3-4. SGMII Identification and Version Register (SGMII_IDVER)

31	16
SGMII_IDENT	
R-4EC2h	

15	11	10	8	7	6	5	0
SGMII_RTL_VER		SGMII_MAJ_VER		SGMII _CUSTOM		SGMII_MINOR_VER	
R-0h		R-1h		R-0h		R-2h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-10. SGMII Identification and Version Register (SGMII_IDVER) Field Descriptions

Bits	Field	Description
31-16	SGMII_IDENT	SGMII identification value
15-11	SGMII_RTL_VER	SGMII RTL version value
10-8	SGMII_MAJOR_VER	SGMII major version value
7-6	SGMII_CUSTOM	SGMII custom value
5-0	SGMII_MINOR_VER	SGMII minor version value

3.3.2 SGMII Software Reset Register (SGMII_SOFT_RESET)

The Software Reset Register is shown in Figure 3-5 and described in Table 3-11.

Figure 3-5. SGMII Software Reset Register (SGMII_SOFT_RESET)

31	2	1	0
Reserved		RT_SOFT _RESET	SOFT _RESET
R-0h		R/W-0h	R/W-0h

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-11. SGMII Software Reset Register (SGMII_SOFT_RESET) Field Descriptions

Bits	Field	Description
31-2	Reserved	Reserved
1	RT_SOFT_RESET	Receive and Transmit Software Reset. Writing a 1 to this bit causes the CPSGMII transmit and receive logic to be in the reset condition. The reset condition is removed when a 0 is written to this bit. This bit is intended to be used when changing between loopback mode and normal mode of operation.
0	SOFT_RESET	Software Reset. Writing a 1 to this bit causes the CPSGMII logic to be reset. Software reset occurs immediately. This bit reads as a 0.

3.3.3 SGMII Control Register (SGMII_CONTROL)

The SGMII Control Register is shown in Figure 3-6 and described in Table 3-12.

Figure 3-6. SGMII Control Register (SGMII_CONTROL)

31					7	6
Reserved						TEST_PATT_EN
R-0h						R/W-0h
5	4	3	2	1		0
MASTER	LOOPBACK	MR_NP_LOADED	FAST_LNK_TIMER	MR_AN_RESTART		MR_AN _ENABLE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h		R/W-0h

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-12. SGMII Control Register (SGMII_CONTROL) Field Descriptions

Bits	Field	Description
31-7	Reserved	Reserved
6	TEST_PATT_EN	Test Pattern Enable. Force the output of K28.5 on TX_ENC for test purposes. • 0 = Normal operation • 1 = Forced K28.5 on transmit output
5	MASTER	Master Mode. • 0 = Slave Mode • 1 = Master mode Set to 1 for one side of a direct connection. When this bit is set, the control logic uses the Mr_Adv_Ability register to determine speed and duplexity instead of the Mr_Lp_Adv_Ability register. Master mode allows a CPSGMII direct connection with auto-negotiation or with a forced link.
4	LOOPBACK	Loopback mode. • 0 = Not in internal loopback mode • 1 = Internal loopback mode. The transmit clock (TX_CLK) is used for transmit and receive.
3	MR_NP_LOADED	Next Page Loaded. Writing a 1 to this bit informs the auto-negotiation process that the next page register has been loaded. This bit is cleared by the auto-negotiation state machine before the MR_PAGE_RX status bit is set. This bit is not used when the SGMII_MODE input is asserted.
2	FAST_LNK_TIMER	Fast Link Timer • 0 = The link timer value is 10ms in FIBER mode and 1.6ms in SGMII mode • 1 = The link timer value is 2us in FIBER and SGMII mode. This is included for test purposes
1	MR_AN_RESTART	Auto-Negotiation Restart. Writing a 1 and then a 0 to this bit causes the auto-negotiation process to be restarted.
0	MR_AN_ENABLE	Auto-Negotiation Enable. Writing a 1 to this bit enables the auto-negotiation process.

3.3.4 SGMII Status Register (SGMII_STATUS)

The SGMII Status Register is shown in Figure 3-7 and described in Table 3-13.

Figure 3-7. SGMII Status Register (SGMII_STATUS)

31	6	5	4	3	2	1	0
Reserved		FIB_SIG _DETECT	LOCK	MR_PAGE_RX	MR_AN_COMPLETE	AN_ERROR	LINK
R-0h		R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-13. SGMII Status Register (SGMII_STATUS) Field Descriptions

Bits	Field	Description
31-5	Reserved	Reserved
5	FIB_SIG_DETECT	Fiber Signal Detect. This is the FIB_SIG_DETECT input pin.
4	LOCK	Lock. This is the LOCK input pin. Indicates that the SerDes PLL is locked.
3	MR_PAGE_RX	Next Page Received. This bit is set to 1 by the auto-negotiation state machine when the next page has been received. This bit is cleared to zero by a host write of a 1 to the MR_NP_LOADED bit in the SGMII_CONTROL register. This value is not valid until the LOCK status bit is asserted.
2	MR_AN_COMPLETE	Auto-negotiation complete. This value is not valid until the LOCK status bit is asserted. • 0 = Auto-negotiation is not complete • 1 = Auto-negotiation is complete
1	AN_ERROR	Auto-negotiation error. For SGMII mode, an auto-negotiation error occurs when halfduplex gigabit is commanded. This value is not valid until the LOCK status bit is asserted. • 0 = No auto-negotiation error. • 1 = Auto-negotiation error.
0	LINK	Link indicator. This value is not valid until the LOCK status bit is asserted. • 0 = Link is not up. • 1 = Link is up.

3.3.5 SGMII Advertised Ability Register (SGMII_MR_ADV_ABILITY)

The Advertised Ability Register is shown in Figure 3-8 and described in Table 3-14.

Figure 3-8. SGMII Advertised Ability Register (SGMII_MR_ADV_ABILITY)

31	16	15	0
Reserved		MR_ADV_ABILITY	
R-0		R/W-0	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-14. SGMII Advertised Ability Register (SGMII_MR_ADV_ABILITY) Field Descriptions

Bits	Field	Description
31-16	Reserved	Reserved
15-0	MR_ADV_ABILITY	Advertised Ability. This value corresponds to the tx_config_reg[15-0] register value in the SGMII specification.

The following tables show the MR_ADV_ABILITY and MR_LP_ADV_ABILITY register values for SGMII mode.

3.3.5.1 SGMII MODE

The advertised ability and link partner advertised ability settings for SGMII mode are shown in Table 3-15.

Table 3-15. Advertised Ability and Link Partner Advertised Ability for SGMII Mode

TX_CONFIG_REG[15-0]	MAC	PHY
15	Link. • 0 = Link is down • 1 = Link is up	0
14	auto-negotiation acknowledge	1
13	0	0
12	Duplex mode. • 0 = Half-duplex mode • 1 = Fullduplex mode	0
11-10	Speed. • 10 = gig • 01 = 100 mbit • 00 = 10 mbit	00
9-1	0	0
0	1	1

3.3.6 SGMII Next Page Transmit Register (SGMII_MR_NP_TX)

The SGMII Next Page Transmit Register is shown in Figure 3-9 and described in Table 3-16.

Figure 3-9. SGMII Next Page Transmit Register (SGMII_MR_NP_TX)

31	16	15	0
Reserved		MR_NP_TX	
R-0		R/W-0	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-16. SGMII Next Page Transmit Register (SGMII_MR_NP_TX) Field Descriptions

Bits	Field	Description
31-16	Reserved	Reserved
15-0	MR_NP_TX	Next Page Transmit. This value corresponds to the MR_NP_TX[16:1] value in the IEEE specification. Next page is only used in FIBER mode.

3.3.7 SGMII Link Partner Advertised Ability Register (SGMII_MR_LP_ADV_ABILITY)

The Link Partner Advertised Ability Register is shown in Figure 3-10 and described in Table 3-17.

Figure 3-10. SGMII Link Partner Advertised Ability Register (SGMII_MR_LP_ADV_ABILITY)

31	16	15	0
Reserved		MR_LP_ADV_ABILITY	
R-0		R-0	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-17. SGMII Link Partner Advertised Ability Register (SGMII_MR_LP_ADV_ABILITY) Field Descriptions

Bits	Field	Description
31-16	Reserved	Reserved
15-0	MR_LP_ADV_ABILITY	Link Partner Advertised Ability. Readable when auto-negotiation is complete. This value corresponds to the TX_CFG[15-0] register value in the SGMII specification.

3.3.8 SGMII Link Partner Next Page Received Register (SGMII_MR_LP_NP_RX)

The SGMII Link Partner Next Page Received Register is shown in Figure 3-11 and described in Table 3-18.

Figure 3-11. SGMII Link Partner Next Page Received Register (SGMII_MR_LP_NP_RX)

31	16	15	0
Reserved		MR_LP_NP_RX	
R-0		R/W-0	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-18. SGMII Link Partner Next Page Received Register (SGMII_MR_LP_NP_RX) Field Descriptions

Bits	Field	Description
31-16	Reserved	Reserved
15-0	MR_LP_NP_RX	Link Partner Next Page Received. Readable when the next page is received. These bits are defined in the IEEE 802.3 standard. Next page is only used in FIBER mode.

3.4 Management Data Input/Output (MDIO) module

This section describes the registers available in the Ethernet switch subsystem MDIO module.

The register offset addresses listed in Table 3-19 are relative to the MDIO module offset address. See Table 3-1 for the offset address of the MDIO module. A complete list of all of the registers in the GbE switch subsystem is provided in Table 3-2.

Table 3-19 lists the registers in the Ethernet switch subsystem and the corresponding address offset for each register.

Table 3-19. MDIO Registers

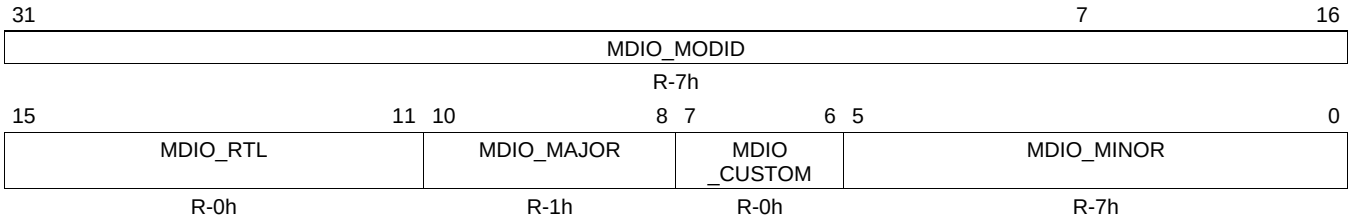
Offset Address[(1)]	Acronym	Register Name	Section
00h	MDIO_VERSION	MDIO Version Register	Section 3.4.1
04h	MDIO_CONTROL	MDIO Control Register	Section 3.4.2
08h	MDIO_ALIVE	PHY Alive Status Register	Section 3.4.3
0Ch	MDIO_LINK	PHY Link Status Register	Section 3.4.4
10h	MDIO_LINKINTRAW	MDIO Link Status Change Interrupt (Unmaksed) Register	Section 3.4.5
14h	MDIO_LINKINTMASKED	MDIO Link Status Change Interrupt (Masked) Register	Section 3.4.6
18h	MDIO_LINKINTMASKSET	MDIO Link Status Change Interrupt Mask Set Register	Section 3.4.7
1Ch	MDIO_LINKINTMASKCLR	MDIO Link Status Change Interrupt Mask Clear Register	Section 3.4.8
20h	MDIO_USERINTRAW	MDIO User Command Complete Interrupt (Unmasked) Register	Section 3.4.9
24h	MDIO_USERINTMASKED	MDIO User Command Complete Interrupt (Masked) Register	Section 3.4.10
28h	MDIO_USERINTMASKSET	MDIO User Interrupt Mask Set Register	Section 3.4.11
2Ch	MDIO_USERINTMASKCLEAR	MDIO User Interrupt Mask Clear Register	Section 3.4.12
30h	MDIO_MANUAL_IF	MDIO Manual Interface Register	Section 3.4.13
34h	MDIO_CONTROL2	MDIO Control 2 Register	Section 3.4.14
38h	MDIO_POLL_EN	MDIO Poll Enable Register	Section 3.4.15
3Ch	MDIO_CLAUSE	MDIO Clause 22 or 45 Enable Register	Section 3.4.16
40h	MDIO_USERADDRESS0	MDIO User Address Register 0	Section 3.4.17
44h	MDIO_USERADDRESS1	MDIO User Address Register 1	Section 3.4.18
48h–7Ch	Reserved	Reserved	Reserved
80h	MDIO_USERACCESS0	MDIO User Access Register 0	Section 3.4.19
84h	MDIO_USERPHYSEL0	MDIO User PHY Select Register 0	Section 3.4.20
88h	MDIO_USERACCESS1	MDIO User Access Register 1	Section 3.4.21
8Ch	MDIO_USERPHYSEL1	MDIO User PHY Select Register 1	Section 3.4.22
90h–FFh	Reserved	Reserved	Reserved

(1) The actual addresses of these registers are device specific. See your device-specific data manual to verify the register addresses.

3.4.1 MDIO Version Register (MDIO_VERSION)

The MDIO Version Register is shown in Figure 3-12 and described in Table 3-20.

Figure 3-12. MDIO Version Register (MDIO_VERSION)



Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-20. MDIO Version Register (MDIO _VERSION) Field Descriptions

Bits	Field	Description
31-16	MDIO_MODID	MDIO Module Identification Value.
15-11	MDIO_RTL	MDIO RTL Version Value.
10-8	MDIO_MAJOR	MDIO Major Version Value.
7-6	MDIO_CUSTOM	MDIO Custom Version Value.
5-0	MDIO_MINOR	MDIO Minor Version Value.

3.4.2 MDIO Control Register (MDIO_CONTROL)

The MDIO Control Register is shown in Figure 3-13 and described in Table 3-21.

Figure 3-13. MDIO Control Register (MDIO_CONTROL)

31	30	29	28 24	23 21	20	19	18
IDLE	ENABLE	Reserved	HIGHEST_USER_CHAN	Reserved	PREAMBLE	FAULT	FAULT_DETECT_EN
R-1h	R/W-0h	R-0h	R-1h	R-0h	R/W-oh	R/W-0h	R/W-0h

17	16	15 0
INT_TEST_EN	Reserved	CLKDIV
R/W-0h	R-0h	R/W-00FFh

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-21. MDIO Control Register (MDIO_CONTROL) Field Descriptions

Bits	Field	Description
31	IDLE	MDIO state machine IDLE status bit. • 0 = State machine is not in the idle state. • 1 = State machine is in the idle state.
30	ENABLE	Enable control. If the MDIO state machine is active at the time it is disabled, it will complete the current operation before halting and setting the idle bit. • 0 =Disables the MDIO state machine. • 1 = Enables the MDIO state machine.
29	Reserved	Reserved
28-24	HIGHEST_USER_CHAN	Highest user channel. This field specifies the highest user access channel that is available in the module and is currently set to 1. This implies that USERACCESS1 is the highest available user access channel.
23-21	Reserved	Reserved
20	PREAMBLE	Preamble disable. • 0 = Standard MDIO preamble is used. • 1 = Disables this device from sending MDIO frame preambles.
19	FAULT	Fault indicator.This bit is set to 1 if the MDIO pins fail to read back what the device is driving onto them. This indicates a physical layer fault and the module state machine is reset. Writing a 1 to it clears this bit. • 0 = No failure. • 1 = Physical layer fault. The MDIO state machine is reset.
18	FAULT_DETECT_EN	Fault detect enable. This bit has to be set to 1 to enable the physical layer fault detection. • 0 = Disables the physical layer fault detection. • 1 = Enables the physical layer fault detection.
17	INT_TEST_EN	Interrupt test enable. This bit can be set to 1 to enable the host to set the LINKINT bits in the MDIO_LINKINTRAW register and the USERINT bits in both the MDIO_USERINTRAW and MDIO_USERINTMASKED registers for test purposes.
16	Reserved	Reserved
15-0	CLKDIV	Clock Divider. This field specifies the division ratio between the VBUS peripheral clock and the frequency of MDCLK. MDCLK is disabled when CLKDIV is set to 0. The Peripheral clock frequency is driven by the DSERDES line rate divided by 10 on KeyStone I devices.The peripheral clock frequency is driven by NETCP clock on KeyStone II devices. MDCLK frequency = peripheral clock frequency/(CLKDIV+1).

3.4.3 PHY Alive Status Register (MDIO_ALIVE)

The PHY Alive Status Register is shown in Figure 3-14 and described in Table 3-22.

Figure 3-14. PHY Alive Status Register (MDIO_ALIVE)

31	0
ALIVE	
R/W-0h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-22. PHY Alive Status Register (MDIO_ALIVE) Field Descriptions

Bits	Field	Description
31-0	ALIVE	MDIO Alive. Each of the 32 bits of this register is set if the most recent access to the PHY with address corresponding to the register bit number was acknowledged by the PHY, the bit is reset if the PHY fails to acknowledge the access. Both the user and polling accesses to a PHY will cause the corresponding alive bit to be updated. The alive bits are meant only to be used to give an indication of the presence or not of a PHY with the corresponding address. Writing a 1 to any bit will clear it, writing a 0 has no effect. • 0 = The PHY fails to acknowledge the access • 1 = The most recent access to the PHY with an address corresponding to the register bit number was acknowledged by the PHY

3.4.4 PHY Link Status Register (MDIO_LINK)

The PHY Link Status Register is shown in Figure 3-15 and described in Table 3-23.

Figure 3-15. PHY Link Status Register (MDIO_LINK)

31	0
LINK	
R-0h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-23. PHY Link Status Register (MDIO_LINK) Field Descriptions

Bits	Field	Description
31-0	LINK	MDIO Link state. This register is updated after a read of the Generic Status Register of a PHY. The bit is set if the PHY with the corresponding address has link and the PHY acknowledges the read transaction. The bit is reset if the PHY indicates it does not have link or fails to acknowledge the read transaction. Writes to the register have no effect. In addition, in Normal Mode Operation, the status of the two PHYs specified in the MDIO_USERPHYSEL registers can be determined using the MLINK input pins. This is determined by the LINKSEL bit in the MDIO_USERPHYSEL register. In State Change Mode the MLINK input pins are unused. • 0 = The PHY indicates that it does not have a link or fails to acknowledge the read transaction • 1 = The PHY with the corresponding address has a link and the PHY acknowledges the read transaction

3.4.5 MDIO Link Status Change Interrupt (Unmasked) Register (MDIO_LINKINTRAW)

The PHY Link Status Change Interrupt (unmasked) Register is shown in Figure 3-16 and described in Table 3-24.

Figure 3-16. MDIO Link Status Change Interrupt (Unmasked) Register (MDIO_LINKINTRAW)

31	2	1	0
Reserved		LINKINTRAW	
R-0h		R/W-0h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-24. MDIO Link Status Change Interrupt (Unmasked) Register (MDIO_LINKINTRAW) Field Descriptions

Bits	Field	Description
31-2	Reserved	Reserved
1-0	LINKINTRAW	Normal Mode Operation: MDIO link change event, raw value. When asserted 1, a bit indicates that there was an MDIO link change event (i.e. change in the MDIO_LINK register) corresponding to the PHY address in the MDIO_USERPHYSEL register. LINKINTRAW[0] and LINKINTRAW[1] correspond to MDIO_USERPHYSEL0 and MDIO_USERPHYSEL1, respectively. Writing a 1 will clear the event and writing 0 has no effect. If the INT_TEST_EN bit in the MDIO_CONTROL register is set, the host may set LINKINTRAW bits to 1 which may be used for test purposes. State Change Mode Operation: MDIO link change event, raw value. The LINKINTRAW[0] bit will be asserted to 1 when any bit (for any PHY) in the MDIO_ALIVE or MDIO_LINK register changes due to MDIO operations. The LINKINTRAW[1] bit is unused in State Change Mode. State Change Mode allows any state change in any PHY to issue an interrupt. if the INT_TEST_EN bit in the MDIO_CONTROL register is set, the host may set the LINKINTRAW[0] bit to 1 which may be used for test purposes.

3.4.6 MDIO Link Status Change Interrupt (Masked) Register (MDIO_LINKINTMASKED)

The MDIO Link Status Change Interrupt (masked) Register is shown in Figure 3-17 and described in Table 3-25.

Figure 3-17. MDIO Link Status Change Interrupt (Masked) Register (MDIO_LINKINTMASKED)

31	2	1	0
Reserved		LINKINTMASKED	
R-0h		R/W-0h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

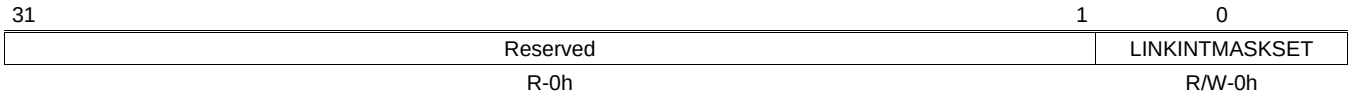
Table 3-25. MDIO Link Status Change Interrupt (Masked) Register (MDIO_LINKINTMASKED) Field Descriptions

Bits	Field	Description
31-2	Reserved	Reserved
1-0	LINKINTMASKED	Normal Mode Operation: MDIO link change interrupt, masked value. When asserted 1, a bit indicates that there was an MDIO link change event (i.e. change in the MDIO_LINK register) corresponding to the PHY address in the MDIO_USERPHYSEL register and the corresponding LINKINTENB bit was set. LINKINTMASKED[0] and LINKINTMASKED[1] correspond to MDIO_USERPHYSEL0 and MDIO_USERPHYSEL1, respectively. Writing a 1 will clear the interrupt and writing 0 has no effect. State Change Mode Operation: MDIO link change interrupt, masked value. The LINKINTMASKED[0] bit will be asserted to 1 when LINKINTRAW[0] is asserted to 1 and when the LINKINTMASKSET bit is set to 1. Writing a 1 will clear LINKINTMASKED[0] (and the MDIO_LINKINT[0] output) and writing 0 has no effect. The LINKINTMASKED[1] bit is not used in State Change Mode.

3.4.7 MDIO Link Status Change Interrupt (Masked) Set Register (MDIO_LINKINTMASKSET)

The MDIO Link Status Change Interrupt (masked) Set Register is shown in Figure 3-18 and described in Table 3-26.

Figure 3-18. MDIO Link Status Change Interrupt (Masked) Set Register (MDIO_LINKINTMASKSET)



Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-26. MDIO Link Status Change Interrupt (Masked) Set Register (MDIO_LINKINTMASKSET) Field Descriptions

Bits	Field	Description
31-1	Reserved	Reserved
0	LINKINTMASKSET	Normal Mode Operation: MDIO link interrupt mask set. This register is not used in normal mode. In normal mode the MDIO_LINKINT[1:0] interrupts are enabled with the LINKINT_ENB bit in the associated MDIO_USERPHYSEL0/1 register. State Change Mode Operation: MDIO link interrupt mask set. Writing this bit to 1 will enable the MDIO link status change interrupt (MDIO_LINKINT[0]) to be asserted when MDIO_LINKINTRAW[0] is asserted.

3.4.8 MDIO Link Status Change Interrupt (Masked) Clear Register (MDIO_LINKINTMASKCLR)

The MDIO Link Status Change Interrupt (masked) Clear Register is shown in Figure 3-19 and described in Table 3-27.

Figure 3-19. MDIO Link Status Change Interrupt (Masked) Clear Register (MDIO_LINKINTMASKCLR)

31	1	0
Reserved		LINKINTMASKCLR
R-0h		R/W-0h

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-27. MDIO Link Status Change Interrupt (Masked) Clear Register (MDIO_LINKINTMASKCLR) Field Descriptions

Bits	Field	Description
31-1	Reserved	Reserved
0	LINKINTMASKCLR	Normal Mode Operation: MDIO link interrupt mask clear. This register is not used in normal mode. In normal mode the MDIO_LINKINT[1:0] interrupts are enabled with the LINKINT_ENB bit in the associated MDIO_USERPHYSEL0/1 register. State Change Mode Operation: MDIO link interrupt mask clear. Writing this bit to 1 will enable the MDIO link status change interrupt (MDIO_LINKINT[0]) to be asserted when MDIO_LINKINTRAW[0] is asserted.

3.4.9 MDIO User Command Complete Interrupt (Unmasked) Register (MDIO_USERINTRAW)

The MDIO User Command Complete Interrupt (unmasked) Register is shown in Figure 3-20 and described in Table 3-28.

Figure 3-20. MDIO User Command Complete Interrupt (Unmasked) Register (MDIO_USERINTRAW)

31	2	1	0
Reserved		USERINTRAW	
R-0h		R/W-0h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-28. MDIO User Command Complete Interrupt (Unmasked) Register (MDIO_USERINTRAW) Field Descriptions

Bits	Field	Description
31-2	Reserved	Reserved
1-0	USERINTRAW	MDIO user command complete event bits. When asserted to 1, a bit indicates that the previously scheduled PHY read or write command using that particular MDIO_USERACCESS register has completed. Writing a 1 will clear the event. Writing 0 has no effect. If the INT_TEST_EN bit in the MDIO_CONTROL register is set, the host may set the USERINTRAW bits to a 1. This mode may be used for test purposes.

3.4.10 MDIO User Command Complete Interrupt (Masked) Register (MDIO_USERINTMASKED)

The MDIO User Command Complete Interrupt (masked) Register is shown in Figure 3-21 and described in Table 3-29.

Figure 3-21. MDIO User Command Complete Interrupt (Masked) Register (MDIO_USERINTMASKED)

31	2	1	0
Reserved		USERINT MASKED	
R-0h		R/W-0h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-29. MDIO User Command Complete Interrupt (Masked) Register (MDIO_USERINTMASKED) Field Descriptions

Bits	Field	Description
31-2	Reserved	Reserved
1-0	USERINTMASKED	Masked value of MDIO user command complete interrupt. When asserted to 1, a bit indicates that the previously scheduled PHY read or write command using that particular MDIO_USERACCESS register has completed and the corresponding USERINTMASKSET bit is set to 1. Writing a 1 will clear the interrupt. Writing a 0 has no effect. If the INT_TEST_EN bit in the MDIO_CONTROL register is set, the host may set the USERINTMASKED bits to a 1. This mode may be used for test purposes.

3.4.11 MDIO User Command Complete Interrupt Mask Set Register (MDIO_USERINTMASKSET)

The MDIO user command complete interrupt mask set register is shown in Figure 3-22 and described in Table 3-30.

Figure 3-22. MDIO User Command Complete Interrupt Mask Set Register (MDIO_USERINTMASKSET)

31	2	1	0
Reserved		USERINT MASKSET	
R-0h		R/W-0h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-30. MDIO User Command Complete Interrupt Mask Set Register (MDIO_USERINTMASKSET) Field Descriptions

Bits	Field	Description
31-2	Reserved	Reserved
1-0	USERINTMASKSET	MDIO user interrupt mask set for USERINTMASKED[1-0], respectively. Setting a bit to 1 will enable MDIO user command complete interrupts for that particular MDIO_USERACCESS register. MDIO user interrupt for a particular MDIO_USERACCESS register is disabled if the corresponding bit is 0. Writing a 0 to this register has no effect.

3.4.12 MDIO User Command Complete Interrupt Mask Clear Register (MDIO_USERINTMASKCLEAR)

The MDIO User Command Complete Interrupt Mask Clear Register is shown in Figure 3-23 and described in Table 3-31.

Figure 3-23. MDIO User Command Complete Interrupt Mask Clear Register (MDIO_USERINTMASKCLEAR)

31	2	1	0
Reserved		USERINT MASKCLEAR	
R-0h		R/W-0h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-31. MDIO User Command Complete Interrupt Mask Clear Register (MDIO_USERINTMASKCLEAR) Field Descriptions

Bits	Field	Description
31-2	Reserved	Reserved
1-0	USERINTMASKCLEAR	MDIO user command complete interrupt mask clear for USERINTMASKED[1-0], respectively. Setting a bit to 1 will disable further user command complete interrupts for that particular MDIO_USERACCESS register. Writing a 0 to this register has no effect.

3.4.13 MDIO Manual Interface Register (MDIO_MANUAL_IF)

The MDIO Manual Interface Register is shown in Figure 3-24 and described in Table 3-32.

Figure 3-24. MDIO Manual Interface Register (MDIO_MANUAL_IF)

31	3	2	1	0
Reserved		MDCLK_O	MDIO_OE	MDIO_PIN
R-0h		R/W-0h	R/W-0h	R/W-0h

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-32. MDIO Manual Interface Register (MDIO_MANUAL_IF) Field Descriptions

Bits	Field	Description
31-3	Reserved	Reserved
2	MDCLK_O	MDIO Clock Output. This value is the MDCLK_O output value when the MANUALMODE bit is set in the MDIO_POLL_IPG register
1	MDIO_OE	MDIO Output Enable. This value is inverted and output on the MDIO_OE_N output when the MANUALMODE bit is set in the MDIO_POLL_IPG register.
0	MDIO_PIN	MDIO Pin Value. This is the external MDIO data pin value when the MANUALMODE bit is set in the MDIO_POLL_IPG register. That is, this value is driven on the MDIO_O (the MDIO serial data output) when MDIO_OE is set to 1. The read value for this bit comes from MDIO_I (the MDIO serial data input). If MDIO_OE is set to 1 and MDIO_PIN is written with a 1 then MDIO_PIN should read a 1 if there are no external devices pulling the MDIO data line low.

3.4.14 MDIO Control 2 Register (MDIO_CONTROL2)

The MDIO Control 2 Register is shown in Figure 3-25 and described in Table 3-33.

Figure 3-25. MDIO Manual Interface Register (MDIO_MANUAL_IF)

31	30	29 8	7 0
MANUAL MODE	STATECHANGEMODE	Reserved	IPG_VALUE
R/W-0h	R/W-0h	R-0h	R/W-0h

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-33. MDIO Manual Interface Register (MDIO_MANUAL_IF) Field Descriptions

Bits	Field	Description
31	MANUALMODE	Manual Mode. When set to 1, the MDIO pins are directly controlled by software through the bits in the MDIO_MANUAL_IF register.
30	STATECHANGEMODE	State Change Mode. When set to 1, the MDIO is operating in State Change Mode. When cleared to 0, the MDIO is operating in Normal Mode. State Change Mode effects interrupt operations.
29-8	Reserved	Reserved
7-0	IPG_VALUE	Polling Inter Poll Gap Value. This value is the number of MDCLK_O clocks between each poll when polling is enabled.

3.4.15 MDIO Poll Enable Register (MDIO_POLL_EN)

The MDIO Poll Enable Register is shown in Figure 3-26 and described in Table 3-34.

Figure 3-26. MDIO Poll Enable Register (MDIO_POLL_EN)

31	0
POLL_ENABLE	
R/W-FFFFFFFFh	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-34. MDIO Poll Enable Register (MDIO_POLL_EN) Field Descriptions

Bits	Field	Description
31-0	POLL_ENABLE	Poll Enable. When set to 1, the bit indicates that the associated PHY will be included in polling operations. When cleared to 0, the associated PHY will not be polled. Each bit in this field is associated with a PHY. Bit 0 is associated with PHY 0 and so on. Due to a limitation in the hardware, bit 31 must always be set (regardless of the value of the PREAMBLE disable bit in the MDIO_CONTROL register. However, there does not have to be a PHY at address 31.

3.4.16 MDIO Clause Mode Register (MDIO_CLAUSE)

The MDIO Clause Mode Register is shown in Figure 3-27 and described in Table 3-35.

Figure 3-27. MDIO Clause Mode Register (MDIO_CLAUSE)

31	0
CLAUSE_MODE	
R/W-0h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-35. MDIO Clause Mode Register (MDIO_CLAUSE) Field Descriptions

Bits	Field	Description
31-0	CLAUSE_MODE	MDIO Clause Mode. When a CLAUSE_MODE bit is cleared to 0 the PHY associated with the bit is operating in Clause 22 mode. When set to 1, the PHY associated with the CLAUSE_MODE bit is operating in the Clause 45 mode. Bit 0 is associated with PHY 0 and so on.

3.4.17 MDIO User Address Register 0 (MDIO_USERADDRESS0)

The MDIO User Address Register 0 is shown in Figure 3-28 and described in Table 3-36.

Figure 3-28. MDIO User Address Register 0 (MDIO_USERADDRESS0)

31	16	15	0
Reserved		USER_ADDR0	
R-0h		R/W-0h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-36. MDIO User Address Register 0 (MDIO_USERADDRESS0) Field Descriptions

Bits	Field	Description
31-0	USER_ADDR0	User Address 0. In Clause 45 mode, this field value is the address transferred before each MDIO_USERACCESS0 access. This is not used for PHYs operating in Clause 22 mode as there is no address transfer proceeding each MDIO_USERACCESS0 access

3.4.18 MDIO User Address Register 1 (MDIO_USERADDRESS1)

The MDIO User Address Register 1 is shown in Figure 3-29 and described in Table 3-37.

Figure 3-29. MDIO User Address Register 1 (MDIO_USERADDRESS1)

31	16	15	0
Reserved		USER_ADDR1	
R-0h		R/W-0h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-37. MDIO User Address Register 1 (MDIO_USERADDRESS1) Field Descriptions

Bits	Field	Description
31-0	USER_ADDR1	User Address 1. In Clause 45 mode, this field value is the address transferred before each MDIO_USERACCESS1 access. This is not used for PHYs operating in Clause 22 mode as there is no address transfer proceeding each MDIO_USERACCESS1 access

3.4.19 MDIO User Access Register 0 (MDIO_USERACCESS0)

The MDIO User Access Register is shown in Figure 3-30 and described in Table 3-38.

Figure 3-30. MDIO User Access Register 0 (MDIO_USERACCESS0)

31	30	29	28 26	25 21	20 16
GO	WRITE	ACK	Reserved	REGADR_MMD	PHYADR
R/W-0h	R/W-0h	R/W-0h	R-0h	R/W-0h	R/W-0h

15 0
DATA
R/W-0h

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-38. MDIO User Access Register 0 (MDIO_USERACCESS0) Field Descriptions

Bits	Field	Description
31	GO	Go bit. Writing a 1 to this bit causes the MDIO state machine to perform an MDIO access when it is convenient for it to do so--this is not an instantaneous process. Writing a 0 to this bit has no effect. This bit can be written only if the MDIO state machine is enabled. This bit will self clear when the requested access has been completed. Any writes to the MDIO_USERACCESS0 register are blocked when the GO bit is 1.
30	WRITE	Write enable bit. Setting this bit to 1 causes the MDIO transaction to be a register write, otherwise it is a register read.
29	ACK	Acknowledge bit. This bit is set if the PHY acknowledged the read transaction.
28-26	Reserved	Reserved
25-21	REGADR_MMD	Register address bits. This field specifies the PHY register to be accessed for this transaction in clause 22 mode or the MMD value in Clause 45 mode.
20-16	PHYADR	PHY address bits. This field specifies the PHY to be accessed for this transaction.
15-0	DATA	User data bits. These bits specify the data value read from or to be written to the specified PHY register.

3.4.20 MDIO User PHY Select Register 0 (MDIO_USERPHYSEL0)

The MDIO User PHY Select Register 0 is shown in Figure 3-31 and described in Table 3-39.

Figure 3-31. MDIO User PHY Select Register 0 (MDIO_USERPHYSEL0)

31	8	7	6	5	4	0
Reserved		LINKSEL	LINKINT ENB	Reserved	PHYADR_MON	
R-0h		R/W-0h	R/W-0h	R-0h	R/W-0h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-39. MDIO User PHY Select Register 0 (MDIO_USERPHYSEL0) Field Descriptions

Bits	Field	Description
31-8	Reserved	Reserved
7	LINKSEL	Link status determination select bit. Default value is 0, which implies that the link status is determined by the MDIO state machine. This is the only option supported on this device. Link status determination select bit. • 0 = (Default value) Link status is determined by the MDIO state machine. • 1 = Link status is determined using the MLINK pin.
6	LINKINTENB	Link change interrupt enable. Set to 1 to enable link change status interrupts for PHY address specified in PHYADR_MON. Link change interrupts are disabled if this bit is set to 0. • 0 = Link change interrupts are disabled. • 1 = Link change status interrupts for PHY address specified in PHYADR_MON bits are enabled.
5	Reserved	Reserved
4-0	PHYADR_MON	PHY address whose link status is to be monitored.

3.4.21 MDIO User Access Register 1 (MDIO_USERACCESS1)

The MDIO User Access Register 1 is shown in Figure 3-32 and described in Table 3-40.

Figure 3-32. MDIO User Access Register 1 (MDIO_USERACCESS1)

31	30	29	28 26	25 21	20 16
GO	WRITE	ACK	Reserved	REGADR_MMD	PHYADR
R/W-0h	R/W-0h	R/W-0h	R-0h	R/W-0h	R/W-0h

15 0
DATA
R/W-0h

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-40. MDIO User Access Register 1 (MDIO_USERACCESS1) Field Descriptions

Bits	Field	Description
31	GO	Go bit. Writing a 1 to this bit causes the MDIO state machine to perform an MDIO access when it is convenient for it to do so--this is not an instantaneous process. Writing a 0 to this bit has no effect. This bit can be written only if the MDIO state machine is enabled. This bit will self clear when the requested access has been completed. Any writes to the USERACCESS1 register are blocked when the GO bit is 1.
30	WRITE	Write enable bit. Setting this bit to 1 causes the MDIO transaction to be a register write, otherwise it is a register read.
29	ACK	Acknowledge bit. This bit is set if the PHY acknowledged the read transaction.
28-26	Reserved	Reserved
25-21	REGADR_MMD	Register address bits. This field specifies the PHY register to be accessed for this transaction in clause 22 mode or the MMD value in Clause 45 mode.
20-16	PHYADR	PHY address bits. This field specifies the PHY to be accessed for this transaction.
15-0	DATA	User data bits. These bits specify the data value read from or to be written to the specified PHY register.

3.4.22 MDIO User PHY Select Register 1 (MDIO_USERPHYSEL1)

The MDIO User PHY Select Register 1 is shown in Figure 3-33 and described in Table 3-41.

Figure 3-33. MDIO User PHY Select Register 1 (MDIO_USERPHYSEL1)

31	8	7	6	5	4	0
Reserved		LINKSEL	LINKINT ENB	Reserved	PHYADR_MON	
R-0h		R/W-0h	R/W-0h	R-0h	R/W-0h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-41. MDIO User PHY Select Register 1 (MDIO_USERPHYSEL1) Field Descriptions

Bits	Field	Description
31-8	Reserved	Reserved
7	LINKSEL	Link status determination select bit. Default value is 0, which implies that the link status is determined by the MDIO state machine. This is the only option supported on this device. Link status determination select bit. • 0 = (Default value) Link status is determined by the MDIO state machine. • 1 = Link status is determined using the MLINK pin.
6	LINKINTENB	Link change interrupt enable. Set to 1 to enable link change status interrupts for PHY address specified in PHYADR_MON. Link change interrupts are disabled if this bit is set to 0. • 0 = Link change interrupts are disabled. • 1 = Link change status interrupts for PHY address specified in PHYADR_MON bits are enabled.
5	Reserved	Reserved
4-0	PHYADR_MON	PHY address whose link status is to be monitored.

3.5 Ethernet Switch Module

This section describes the registers available in the Ethernet switch module.

The submodule offset addresses listed in Table 3-42 are relative to the Ethernet switch module offset address. See Table 3-1 for the offset address of the Ethernet switch module. A complete list of all of the registers in the GbE switch subsystem is provided in Table 3-2.

Table 3-42 shows the submodules contained in the Ethernet switch module.

Table 3-42. Ethernet Switch Submodules

Offset Address[1]	Acronym	Submodule Name	Section
00000h	GbE Switch	Ethernet switch submodule	Section 3.5.1
01000h	Host Port 0	Host Port 0 submodule	Section 3.5.2
02000h	Ethernet Port 1	Ethernet Port 1 submodule	Section 3.5.2
03000h	Ethernet Port 2	Ethernet Port 2 submodule	Section 3.5.2
04000h	Ethernet Port 3	Ethernet Port 3 submodule	Section 3.5.2
05000h	Ethernet Port 4	Ethernet Port 4 submodule	Section 3.5.2
06000h	Ethernet Port 5	Ethernet Port 5 submodule	Section 3.5.2
07000h	Ethernet Port 6	Ethernet Port 6 submodule	Section 3.5.2
08000h	Ethernet Port 7	Ethernet Port 7 submodule	Section 3.5.2
09000h	Ethernet Port 8	Ethernet Port 8 submodule	Section 3.5.2
1A000h	STAT0	Host Port 0 Statistics submodule	Section 3.5.3
1A200h	STAT1	Host Port 1 Statistics submodule	Section 3.5.3
1A400h	STAT2	Host Port 2 Statistics submodule	Section 3.5.3
1A600h	STAT3	Host Port 3 Statistics submodule	Section 3.5.3
1A800h	STAT4	Host Port 4 Statistics submodule	Section 3.5.3
1AA00h	STAT5	Host Port 5 Statistics submodule	Section 3.5.3
1AC00h	STAT6	Host Port 6 Statistics submodule	Section 3.5.3
1AE00h	STAT7	Host Port 7 Statistics submodule	Section 3.5.3
1B000h	STAT8	Host Port 8 Statistics submodule	Section 3.5.3
1D000h	CPTS	Time Sync submodule	Section 3.5.4
1E000h	ALE	Address lookup engine submodule	Section 3.5.5
1F000h	ECC	ECC submodule	Section 3.5.6

[1] The actual addresses of these registers are device specific. See your device-specific data manual to verify the register addresses.

3.5.1 Gigabit Ethernet (GbE) Switch Module

This section describes the registers available in the gigabit Ethernet switch module.

The register offset addresses listed in Table 3-43 are relative to the Ethernet switch module offset address. See Table 3-1 for the offset address of the Ethernet switch module. A complete list of all of the registers in the GbE switch subsystem is provided in Table 3-2.

Table 3-43. Ethernet Switch Submodule Registers

Offset Address[1]	Acronym	Description	Section
0000h	CPSW_IDVER	GbE switch identification and version register	Section 3.5.1.1
0004h	CPSW_CONTROL	GbE switch Control Register	Section 3.5.1.2
0008h-0Ch	Reserved	Reserved	Reserved
0010h	CPSW_EM_CONTROL	GbE switch Emulation Control Register	Section 3.5.1.3
0014h	CPSW_STAT_PORT_EN	GbE switch Statistics Port Enable Register	Section 3.5.1.4
0018h	CPSW_PTYPE	GbE switch Transmit Priority Type Register	Section 3.5.1.5
001Ch	CPSW_SOFT_IDLE	GbE switch Software Idle Register	Section 3.5.1.6
0020h	CPSW_THRU_RATE	GbE switch Thru Rate Register	Section 3.5.1.7
0024h	CPSW_GAP_THRESH	Transmit FIFO Short Gap Threshold Register	Section 3.5.1.8
0028h	CPSW_TX_START_WDS	Transmit FIFO Start Words Register	Section 3.5.1.9
002Ch	Reserved	Reserved	Reserved
0030h	CPSW_TX_OUTFLOW_THRESH_SET	Global Transmit Out Flow Threshold Set Register	Section 3.5.1.10
0034h	CPSW_TX_OUTFLOW_THRESH_CLR	Global Transmit Out Flow Threshold Clear Register	Section 3.5.1.11
0038h	CPSW_TX_BUFFER_THRESH_SET_L	Global Transmit Buffer Threshold Set Register Low	Section 3.5.1.12
003Ch	CPSW_TX_BUFFER_THRESH_SET_H	Global Transmit Buffer Threshold Set Register High	Section 3.5.1.13
0040h	CPSW_TX_BUFFER_THRESH_CLR_L	Global Transmit Buffer Threshold Clear Register Low	Section 3.5.1.14
0044h	CPSW_TX_BUFFER_THRESH_CLR_H	Global Transmit Buffer Threshold Clear Register High	Section 3.5.1.15
0048h-1000h	Reserved	Reserved	Reserved

(1) The actual addresses of these registers are device specific. See your device-specific data manual to verify the register addresses.

3.5.1.1 GbE Switch Identification and Version Register (CPSW_IDVER)

The GbE Switch Identification and Version Register is shown in Figure 3-34 and described in Table 3-44.

Figure 3-34. GbE Switch Identification and Version Register (CPSW_IDVER)

31	16
CPSW_IDVER	
R-4EE5h	

15 11	10 8	7 6	5 0
CPSW_RTL_VER	CPSW_MAJ_VER	CPSW_CUSTOM_VER	CPSW_MINOR_VER
R-7h	R-1h	R-0h	R-0h

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-44. GbE Switch Identification and Version Register (CPSW_IDVER) Field Descriptions

Bits	Field	Description
31-16	CPSW_IDENT	Identification Value
15-11	CPSW_RTL_VER	RTL Version Value
10-8	CPSW_MAJ_VER	Major Version Value
7-6	CPSW_CUSTOM_VER	Custom Version Value
5-0	CPSW_MINOR_VERS	Minor Version Value

3.5.1.2 GbE Switch Control Register (CPSW_CONTROL)

The GbE Switch Control Register is shown in Figure 3-35 and described in Table 3-45.

Figure 3-35. GbE Switch Control Register (CPSW_CONTROL)

31	30	16	15	14
ECC_CRC_MODE	Reserved		P0_RX_PASS_CRC_ERR	P0_RX_PAD
R/W-0h	R-0h		R/W-0h	R/W-0h

13	12	11	3	2	1	0
P0_TX_CRC_REM	P0_TX_CRC_TYPE	PN_PASS_PRI_TAG		P0_ENABLE	VLAN_AWARE	Reserved
R/W-0h	R/W-0h	R/W-0h		R/W-0h	R/W-0h	R-0h

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-45. GbE Switch Control Register (CPSW_CONTROL) Field Descriptions

Bits	Field	Description
31	ECC_CRC_MODE	ECC CRC Mode. • 0 = ECC errors induced through the ECC submodule flip bits in the packet headers (not in packet data). • 1 = ECC errors induced through the ECC submodule flip bits in the packet data (not in the packet headers).
30-16	Reserved	Reserved
15	P0_RX_PASS_CRC_ERR	Port 0 Pass Received CRC Errors. • 0 = Packets received with CRC errors on Port 0 are dropped. • 1 = Packets received with CRC errors on Port 0 are transferred to the destination ports.
14	P0_RX_PAD	Port 0 Receive Short Packet Pad. • 0 = Short packets are dropped. • 1 = Short packets are padded to 64-bytes (with pad and added CRC) if the CRC is not passed in. Short packets are dropped if the CRC is passed (in the Info0 word).
13	P0_TX_CRC_REM	Port 0 Transmit CRC Remove. • 0 = Do not remove the CRC on Port 0 transmit (egress) packets. • 1 = Remove the CRC on all Port 0 transmit (egress) packets.
12	P0_TX_CRC_TYPE	Port 0 Transmit CRC Type. The type of CRC on all Port 0 transmit packet (egress), regardless of the CRC type of the ingress Ethernet port. • 0 = Ethernet CRC on Port 0 transmit. • 1 = Castagnoli CRC on Port 0 transmit.
11-3	PN_PASS_PRI_TAG	Port n Pass Priority Tagged (N = 0 to 4 for 5 port CPSW, N = 0 to 8 for 9 Port CPSW). • 0 = Priority tagged packets have the zero VID replaced with the input port Pn_PORT_VLAN[11-0] on ingress. • 1 = Priority tagged packets are processed unchanged. For example, bit 3 corresponds to port 0. If bit 3 is set to 0 then any priority tagged packet entering the switch at port 0 that has a zero VID will have its priority tag replaced with the tag found in P0_PORT_VLAN[11-0] register on switch ingress. If bit 3 is set to 1 then the priority tag will remain unchanged during switch ingress through port 0. • Bit 11 - Port8_PASS_PRI_TAG (only for 9 port CPSW) • Bit 10 - Port7_PASS_PRI_TAG (only for 9 port CPSW) • Bit 9 - Port6_PASS_PRI_TAG (only for 9 port CPSW) • Bit 8 - Port5_PASS_PRI_TAG (only for 9 port CPSW) • Bit 7 - Port4_PASS_PRI_TAG • Bit 6 - Port3_PASS_PRI_TAG • Bit 5 - Port2_PASS_PRI_TAG • Bit 4 - Port1_PASS_PRI_TAG • Bit 3 - Port0_PASS_PRI_TAG
2	P0_ENABLE	Port 0 Enable. • 0 = Host port 0 packet operations are disabled. • 1 = Host port 0 packet operations are enabled.

Table 3-45. GbE Switch Control Register (CPSW_CONTROL) Field Descriptions (continued)

Bits	Field	Description
1	VLAN_AWARE	VLAN Aware Mode. • 0 = GbE switch is in the VLAN unaware mode. • 1 = GbE switch is in the VLAN aware mode.
0	Reserved	Reserved

3.5.1.3 Emulation Control Register (CPSW_EM_CONTROL)

The Emulation Control Register is shown in Figure 3-36 and described in Table 3-46.

Figure 3-36. Emulation Control Register (CPSW_EM_CONTROL)

31	2	1	0
Reserved		SOFT	FREE
R-0h		R/W-0h	R/W-0h

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-46. Emulation Control Register (EM_CONTROL) Field Descriptions

Bits	Field	Description
31-2	Reserved	Reserved
1	SOFT	Emulation soft bit
0	FREE	Emulation free bit

3.5.1.4 Statistics Port Enable Register (CPSW_STAT_PORT_EN)

The Statistics Port Enable Register is shown in Figure 3-37 and described in Table 3-47.

Figure 3-37. Statistics Port Enable Register (CPSW_STAT_PORT_EN)

31							9	8
Reserved								P8_STAT_EN
R-0h								R/W-0h
7	6	5	4	3	2	1		0
P7_STAT_EN	P6_STAT_EN	P5_STAT_EN	P4_STAT_EN	P3_STAT_EN	P2_STAT_EN	P1_STAT_EN		P0_STAT_EN
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h		R/W-0h

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-47. Statistics Port Enable Register (CPSW_STAT_PORT_EN) Field Descriptions

Bits	Field	Description
31-9	Reserved	Reserved
8	P8_STAT_EN	Port 8 Statistics Enable. • 0= Port 8 statistics are not enabled. • 1 = Port 8 statistics are enabled.
7	P7_STAT_EN	Port 7 Statistics Enable. • 0= Port 7 statistics are not enabled. • 1 = Port 7 statistics are enabled.
63	P6_STAT_EN	Port 6 Statistics Enable. • 0= Port 6 statistics are not enabled. • 1 = Port 6 statistics are enabled.
5	P5_STAT_EN	Port 5 Statistics Enable. • 0= Port 5 statistics are not enabled. • 1 = Port 5 statistics are enabled.
4	P4_STAT_EN	Port 4 Statistics Enable. • 0= Port 4 statistics are not enabled. • 1 = Port 4 statistics are enabled.
3	P3_STAT_EN	Port 3 Statistics Enable. • 0= Port 3 statistics are not enabled. • 1 = Port 3 statistics are enabled.
2	P2_STAT_EN	Port 2 Statistics Enable. • 0= Port 2 statistics are not enabled. • 1 = Port 2 statistics are enabled.
1	P1_STAT_EN	Port 1 Statistics Enable. • 0= Port 1 statistics are not enabled. • 1 = Port 1 statistics are enabled.
0	P0_STAT_EN	Port 0 Statistics Enable. • 0= Port 0 statistics are not enabled. • 1 = Port 0 statistics are enabled.

3.5.1.5 Priority Type Register (CPSW_PTYPE)

The Priority Type Register is shown in Figure 3-38 and described in Table 3-48.

Figure 3-38. Priority Type Register (CPSW_PTYPE)

31	17	16	15	14	13
Reserved		P8_PTYPE_ESC	P7_PTYPE_ESC	P6_PTYPE_ESC	P5_PTYPE_ESC
R-0h		R/W-0h	R/W-0h	R/W-0h	R/W-0h

12	11	10	9	8	7 5	4 0
P4_PTYPE_ESC	P3_PTYPE_ESC	P2_PTYPE_ESC	P1_PTYPE_ESC	P0_PTYPE_ESC	Reserved	ESC_PRI_LD_VAL
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h	R/W-0h

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-48. Priority Type Register (CPSW_PTYPE) Field Descriptions

Bits	Field	Description
31-17	Reserved	Reserved
16	P8_PTYPE_ESC	Port 8 Priority Type Escalate. • 0 = Port 8 priority type fixed. • 1 = Port 8 priority type escalate.
15	P7_PTYPE_ESC	Port 7 Priority Type Escalate. • 0 = Port 7 priority type fixed. • 1 = Port 7 priority type escalate.
14	P6_PTYPE_ESC	Port 6 Priority Type Escalate. • 0 = Port 6 priority type fixed. • 1 = Port 6 priority type escalate.
13	P5_PTYPE_ESC	Port 5 Priority Type Escalate. • 0 = Port 5 priority type fixed. • 1 = Port 5 priority type escalate.
12	P4_PTYPE_ESC	Port 4 Priority Type Escalate. • 0 = Port 4 priority type fixed. • 1 = Port 4 priority type escalate.
11	P3_PTYPE_ESC	Port 3 Priority Type Escalate. • 0 = Port 3 priority type fixed. • 1 = Port 3 priority type escalate.
10	P2_PTYPE_ESC	Port 2 Priority Type Escalate. • 0 = Port 2 priority type fixed. • 1 = Port 2 priority type escalate.
9	P1_PTYPE_ESC	Port 1 Priority Type Escalate. • 0 = Port 1 priority type fixed. • 1 = Port 1 priority type escalate.
8	P0_PTYPE_ESC	Port 0 Priority Type Escalate. • 0 = Port 0 priority type fixed. • 1 = Port 0 priority type escalate.
7-5	Reserved	Reserved
4-0	ESC_PRI_LD_VAL	Escalate Priority Load Value. When a port is in escalate priority, this is the number of higher priority packets sent before the next lower priority is allowed to send a packet. Escalate priority allows lower priority packets to be sent at a fixed rate relative to the next higher priority. The minimum value of ESC_PRI_LD_VAL is 2.

3.5.1.6 Software Idle Register (CPSW_SOFT_IDLE)

The Software Idle Register is shown in Figure 3-39 and described in Table 3-49.

Figure 3-39. Software Idle Register (CPSW_SOFT_IDLE)

31	1	0
Reserved		SOFT_IDLE
R-0h		R/W-0h

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-49. Software Idle Register (CPSW_SOFT_IDLE) Field Descriptions

Bits	Field	Description
31-1	Reserved	Reserved
0	SOFT_IDLE	Software Idle. • 0 = Not in idle. • 1 = Command a CPSW software idle. When set to 1, no packets will be started to be unloaded from ports 0 through 4 receive unload. Packets that are currently being unloaded are unaffected.

3.5.1.7 Through Rate Register (CPSW_THRU_RATE)

The Through Rate Register is shown in Figure 3-40 and described in Table 3-50.

Figure 3-40. Through Rate Register (CPSW_THRU_RATE)

31 16	15 12	11 4	3 0
Reserved	ENET_RX_THRU_RATE	Reserved	CPPI_RX_THRU_RATE
R-0h	R/W-3h	R-0h	R/W-3h

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-50. Through Rate Register (CPSW_THRU_RATE) Field Descriptions

Bits	Field	Description
31-16	Reserved	Reserved
15-12	ENET_RX_THRU_RATE	Ethernet Port Switch FIFO Receive Through Rate. This register value is the maximum throughput of the Ethernet ports to the crossbar SCR. The default is one 8-byte word for every 3 VBUSP_GCLK periods maximum. The minimum value is 2. This field defaults to 3 and is not intended to be changed.
11-4	Reserved	Reserved
3-0	CPPI_RX_THRU_RATE	CPPI FIFO (Host port 0) Receive Through Rate. This register value is the maximum throughput of the CPPI FIFO (Host port 0) into the CPSW. The minimum value is 2. This field defaults to 3 and is not intended to be changed.

3.5.1.8 Ethernet Port Short Gap Threshold Register (CPSW_GAP_THRESH)

The Ethernet Port Short Gap Threshold Register is shown in Figure 3-41 and described in Table 3-51.

Figure 3-41. Ethernet Port Short Gap Threshold Register (CPSW_GAP_THRESH)

31	5	4	0
Reserved		GAP_THRESH	
R-0h		R/W-Bh	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-51. Ethernet Port Short Gap Threshold Register (CPSW_GAP_THRESH) Field Descriptions

Bits	Field	Description
31-5	Reserved	Reserved
4-0	GAP_THRESH	Ethernet Port Short Gap Threshold. This is the Ethernet port associated FIFO transmit block usage value for triggering TX_SHORT_GAP.

3.5.1.9 FIFO Packet Transmit (Egress) Start Words Register (CPSW_TX_START_WDS)

The FIFO Packet Transmit (Egress) Start Words Register is shown in Figure 3-42 and described in Table 3-52.

Figure 3-42. FIFO Packet Transmit (Egress) Start Words Register (CPSW_TX_START_WDS)

31	11	10	0
Reserved		TX_START_WDS	
R-0h		R/W-8h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-52. FIFO Packet Transmit (Egress) Start Words Register (CPSW_TX_START_WDS) Field Descriptions

Bits	Field	Description
31-11	Reserved	Reserved
10-0	TX_START_WDS	FIFO Packet Transmit (Egress) Start Words. This value is the number of required 32-bit packet words in an Ethernet transmit FIFO before the packet egress will begin. This value is non-zero to preclude Ethernet transmit underrun. Decimal 8 is the recommended value. It should not be increased unnecessarily to prevent adding to the switch latency.

3.5.1.10 Priority Based Flow Control Global Outflow Usage Threshold Set Register (CPSW_TX_OUTFLOW_THRESH_SET)

The Priority Base Flow Control Global Outflow Usage Threshold Set Register is shown in Figure 3-43 and described in Table 3-53.

Figure 3-43. Priority Based Flow Control Global Outflow Usage Threshold Set Register (CPSW_TX_OUTFLOW_THRESH_SET)

31 28	27 24	23 20	19 16
TX_G_OFLOW_THRESH_SET7	TX_G_OFLOW_THRESH_SET6	TX_G_OFLOW_THRESH_SET5	TX_G_OFLOW_THRESH_SET4
R/W-Fh	R/W-Fh	R/W-Fh	R/W-Fh
15 12	11 8	7 4	3 0
TX_G_OFLOW_THRESH_SET3	TX_G_OFLOW_THRESH_SET2	TX_G_OFLOW_THRESH_SET1	TX_G_OFLOW_THRESH_SET0
R/W-Fh	R/W-Fh	R/W-Fh	R/W-Fh

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-53. Priority Based Flow Control Global Outflow Usage Threshold Set Register (CPSW_TX_OUTFLOW_THRESH_SET) Field Descriptions

Bits	Field	Description
31-28	TX_G_OFLOW_THRESH_SET7	• Priority Based Flow Control Global Outflow Usage Threshold Set for Priority 7.
27-24	TX_G_OFLOW_THRESH_SET6	• Priority Based Flow Control Global Outflow Usage Threshold Set for Priority 6.
23-20	TX_G_OFLOW_THRESH_SET5	• Priority Based Flow Control Global Outflow Usage Threshold Set for Priority 5.
19-16	TX_G_OFLOW_THRESH_SET4	• Priority Based Flow Control Global Outflow Usage Threshold Set for Priority 4.
15-12	TX_G_OFLOW_THRESH_SET3	• Priority Based Flow Control Global Outflow Usage Threshold Set for Priority 3.
11-8	TX_G_OFLOW_THRESH_SET2	• Priority Based Flow Control Global Outflow Usage Threshold Set for Priority 2.
7-4	TX_G_OFLOW_THRESH_SET1	• Priority Based Flow Control Global Outflow Usage Threshold Set for Priority 1.
3-0	TX_G_OFLOW_THRESH_SET0	• Priority Based Flow Control Global Outflow Usage Threshold Set for Priority 0.

3.5.1.11 Priority Based Flow Control Global Outflow Usage Threshold Clear Register (CPSW_TX_OUTFLOW_THRESH_CLR)

The Priority Base Flow Control Global Outflow Usage Threshold Clear Register is shown in Figure 3-44 and described in Table 3-54.

Figure 3-44. Priority Based Flow Control Global Outflow Usage Threshold Clear Register (CPSW_TX_OUTFLOW_THRESH_CLR)

31 28	27 24	23 20	19 16
TX_G_OFLOW_THRESH_CLR7	TX_G_OFLOW_THRESH_CLR6	TX_G_OFLOW_THRESH_CLR5	TX_G_OFLOW_THRESH_CLR4
R/W-Fh	R/W-Fh	R/W-Fh	R/W-Fh
15 12	**11 8**	**7 4**	**3 0**
TX_G_OFLOW_THRESH_CLR3	TX_G_OFLOW_THRESH_CLR2	TX_G_OFLOW_THRESH_CLR1	TX_G_OFLOW_THRESH_CLR0
R/W-Fh	R/W-Fh	R/W-Fh	R/W-Fh

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-54. Priority Based Flow Control Global Outflow Usage Threshold Clear Register (CPSW_TX_OUTFLOW_THRESH_CLR) Field Descriptions

Bits	Field	Description
31-28	TX_G_OFLOW_THRESH_CLR7	• Priority Based Flow Control Global Outflow Usage Threshold Clear for Priority 7.
27-24	TX_G_OFLOW_THRESH_CLR6	• Priority Based Flow Control Global Outflow Usage Threshold Clear for Priority 6.
23-20	TX_G_OFLOW_THRESH_CLR5	• Priority Based Flow Control Global Outflow Usage Threshold Clear for Priority 5.
19-16	TX_G_OFLOW_THRESH_CLR4	• Priority Based Flow Control Global Outflow Usage Threshold Clear for Priority 4.
15-12	TX_G_OFLOW_THRESH_CLR3	• Priority Based Flow Control Global Outflow Usage Threshold Clear for Priority 3.
11-8	TX_G_OFLOW_THRESH_CLR2	• Priority Based Flow Control Global Outflow Usage Threshold Clear for Priority 2.
7-4	TX_G_OFLOW_THRESH_CLR1	• Priority Based Flow Control Global Outflow Usage Threshold Clear for Priority 1.
3-0	TX_G_OFLOW_THRESH_CLR0	• Priority Based Flow Control Global Outflow Usage Threshold Clear for Priority 0.

3.5.1.12 Priority Based Flow Control Global Buffer Usage Threshold Set Low Register (CPSW_TX_BUFFER_THRESH_SET_L)

The Priority Base Flow Control Global Buffer Usage Threshold Set Low Register is shown in Figure 3-45 and described in Table 3-55.

Figure 3-45. Priority Based Flow Control Global Buffer Usage Threshold Set Low Register (CPSW_TX_BUFFER_THRESH_SET_L)

31 24	23 16	15 8	7 0
TX_G_BUF_THRESH_SET3	TX_G_BUF_THRESH_SET2	TX_G_BUF_THRESH_SET1	TX_G_BUF_THRESH_SET0
R/W-FFh	R/W-FFh	R/W-FFh	R/W-FFh

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-55. Priority Based Flow Control Global Buffer Usage Threshold Set Low Register (CPSW_TX_BUFFER_THRESH_SET_L) Field Descriptions

Bits	Field	Description
31-24	TX_G_BUF_THRESH_SET3	• Priority Based Flow Control Global Buffer Usage Threshold Set for Priority 3.
23-16	TX_G_BUF_THRESH_SET2	• Priority Based Flow Control Global Buffer Usage Threshold Set for Priority 2.
15-8	TX_G_BUF_THRESH_SET1	• Priority Based Flow Control Global Buffer Usage Threshold Set for Priority 1.
7-0	TX_G_BUF_THRESH_SET0	• Priority Based Flow Control Global Buffer Usage Threshold Set for Priority 0.

3.5.1.13 Priority Based Flow Control Global Buffer Usage Threshold Set High Register (CPSW_TX_BUFFER_THRESH_SET_H)

The Priority Base Flow Control Global Buffer Usage Threshold Set High Register is shown in Figure 3-46 and described in Table 3-56.

Figure 3-46. Priority Based Flow Control Global Buffer Usage Threshold Set High Register (CPSW_TX_BUFFER_THRESH_SET_H)

31 24	23 16	15 8	7 0
TX_G_BUF_THRESH_SET7	TX_G_BUF_THRESH_SET6	TX_G_BUF_THRESH_SET5	TX_G_BUF_THRESH_SET4
R/W-FFh	R/W-FFh	R/W-FFh	R/W-FFh

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-56. Priority Based Flow Control Global Buffer Usage Threshold Set High Register (CPSW_TX_BUFFER_THRESH_SET_H) Field Descriptions

Bits	Field	Description
31-24	TX_G_BUF_THRESH_SET7	• Priority Based Flow Control Global Buffer Usage Threshold Set for Priority 7.
23-16	TX_G_BUF_THRESH_SET6	• Priority Based Flow Control Global Buffer Usage Threshold Set for Priority 6.
15-8	TX_G_BUF_THRESH_SET5	• Priority Based Flow Control Global Buffer Usage Threshold Set for Priority 5.
7-0	TX_G_BUF_THRESH_SET4	• Priority Based Flow Control Global Buffer Usage Threshold Set for Priority 4.

3.5.1.14 Priority Based Flow Control Global Buffer Usage Threshold Clear Low Register (CPSW_TX_BUFFER_THRESH_CLR_L)

The Priority Base Flow Control Global Buffer Usage Threshold Clear Low Register is shown in Figure 3-47 and described in Table 3-57.

Figure 3-47. Priority Based Flow Control Global Buffer Usage Threshold Clear Low Register (CPSW_TX_BUFFER_THRESH_CLR_L)

31 24	23 16	15 8	7 0
TX_G_BUF_THRESH_CLR3	TX_G_BUF_THRESH_CLR2	TX_G_BUF_THRESH_CLR1	TX_G_BUF_THRESH_CLR0
R/W-FFh	R/W-FFh	R/W-FFh	R/W-FFh

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-57. Priority Based Flow Control Global Buffer Usage Threshold Clear Low Register (CPSW_TX_BUFFER_THRESH_CLR_L) Field Descriptions

Bits	Field	Description
31-24	TX_G_BUF_THRESH_CLR3	• Priority Based Flow Control Global Buffer Usage Threshold Clear for Priority 3.
23-16	TX_G_BUF_THRESH_CLR2	• Priority Based Flow Control Global Buffer Usage Threshold Clear for Priority 2.
15-8	TX_G_BUF_THRESH_CLR1	• Priority Based Flow Control Global Buffer Usage Threshold Clear for Priority 1.
7-0	TX_G_BUF_THRESH_CLR0	• Priority Based Flow Control Global Buffer Usage Threshold Clear for Priority 0.

3.5.1.15 Priority Based Flow Control Global Buffer Usage Threshold Clear High Register (CPSW_TX_BUFFER_THRESH_CLR_H)

The Priority Base Flow Control Global Buffer Usage Threshold Clear High Register is shown in Figure 3-48 and described in Table 3-58.

Figure 3-48. Priority Based Flow Control Global Buffer Usage Threshold Clear High Register (CPSW_TX_BUFFER_THRESH_CLR_H)

31 24	23 16	15 8	7 0
TX_G_BUF_THRESH_CLR7	TX_G_BUF_THRESH_CLR6	TX_G_BUF_THRESH_CLR5	TX_G_BUF_THRESH_CLR4
R/W-FFh	R/W-FFh	R/W-FFh	R/W-FFh

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-58. Priority Based Flow Control Global Buffer Usage Threshold Clear High Register (CPSW_TX_BUFFER_THRESH_CLR_H) Field Descriptions

Bits	Field	Description
31-24	TX_G_BUF_THRESH_CLR7	• Priority Based Flow Control Global Buffer Usage Threshold Clear for Priority 7.
23-16	TX_G_BUF_THRESH_CLR6	• Priority Based Flow Control Global Buffer Usage Threshold Clear for Priority 6.
15-8	TX_G_BUF_THRESH_CLR5	• Priority Based Flow Control Global Buffer Usage Threshold Clear for Priority 5.
7-0	TX_G_BUF_THRESH_CLR4	• Priority Based Flow Control Global Buffer Usage Threshold Clear for Priority 4.

3.5.2 Switch Port Submodules

This section describes the registers available in the switch port submodules. There are two types of switch ports: internal facing host ports and external facing Ethernet ports. Every device has one host port (port 0) and multiple Ethernet ports (port 1 - port n, where n = 4 for a 5 port switch and n = 8 for a 9 port switch).

The two types of ports have many register definitions in common so the definitions below will use the notation Pn_REGISTER_NAME where n = 0 to 4 in a 5 port switch and n = 0 to 8 in a 9 port switch. If a type of register exists for the host port but not the Ethernet ports, or vice versa, it will be mentioned in the register description.

The register offset addresses listed in Table 3-59 are relative to the Ethernet switch module offset address. See Table 3-1 for the offset address of the Ethernet switch module. A complete list of all of the registers in the GbE switch subsystem is provided in Table 3-2.

Table 3-59. Common Switch Port Submodule Registers (n = 0-4 for a 5 port switch or n = 0-8 for a 9 port switch)

Offset Address[(1)]	Acronym	Description	Section
000h	Reserved	Reserved	Reserved
004h	Pn_CONTROL	Port n Control Register	Section 3.5.2.1
008h-00Ch	Reserved	Reserved	Reserved
010h	Pn_BLK_CNT	Port n FIFO Block Usage Count	Section 3.5.2.2
014h	Pn_PORT_VLAN	Port n VLAN Register	Section 3.5.2.3
018h	Pn_TX_PRI_MAP	Port n Transmit Header Priority to Switch Priority Mapping Register	Section 3.5.2.4
01Ch	Pn_PRI_CTL	Port n Priority Control Register	Section 3.5.2.5
020h	Pn_RX_PRI_MAP	Port n Receive Packet Priority to Header Priority Mapping Register	Section 3.5.2.6
024h	Pn_RX_MAXLEN	Port n Receive Frame Max Length Register	Section 3.5.2.7
028h	Pn_TX_BLKS_PRI	Port n Transmit Block Sub Per Priority Register	Section 3.5.2.8
02Ch-11Ch	Reserved	Reserved	Reserved
120h	Pn_RX_DSCP_MAP0	Port n Receive IPv4/IPv6 DSCP Priority Mapping Register 0	Section 3.5.2.9
124h	Pn_RX_DSCP_MAP1	Port n Receive IPv4/IPv6 DSCP Priority Mapping Register 1	Section 3.5.2.10
128h	Pn_RX_DSCP_MAP2	Port n Receive IPv4/IPv6 DSCP Priority Mapping Register 2	Section 3.5.2.11
12Ch	Pn_RX_DSCP_MAP3	Port n Receive IPv4/IPv6 DSCP Priority Mapping Register 3	Section 3.5.2.12
130h	Pn_RX_DSCP_MAP4	Port n Receive IPv4/IPv6 DSCP Priority Mapping Register 4	Section 3.5.2.13
134h	Pn_RX_DSCP_MAP5	Port n Receive IPv4/IPv6 DSCP Priority Mapping Register 5	Section 3.5.2.14
138h	Pn_RX_DSCP_MAP6	Port n Receive IPv4/IPv6 DSCP Priority Mapping Register 6	Section 3.5.2.15
13Ch	Pn_RX_DSCP_MAP7	Port n Receive IPv4/IPv6 DSCP Priority Mapping Register 7	Section 3.5.2.16
140h	Pn_PRI0_SEND	Port n Receive Priority 0 Send Count Value Register	Section 3.5.2.17
144h	Pn_PRI1_SEND	Port n Receive Priority 1 Send Count Value Register	Section 3.5.2.18
148h	Pn_PRI2_SEND	Port n Receive Priority 2 Send Count Value Register	Section 3.5.2.19
14Ch	Pn_PRI3_SEND	Port n Receive Priority 3 Send Count Value Register	Section 3.5.2.20

(1) The actual addresses of these registers are device specific. See your device-specific data manual to verify the register addresses.

Table 3-59. Common Switch Port Submodule Registers (n = 0-4 for a 5 port switch or n = 0-8 for a 9 port switch) (continued)

Offset Address[1]	Acronym	Description	Section
150h	Pn_PRI4_SEND	Port n Receive Priority 4 Send Count Value Register	Section 3.5.2.21
154h	Pn_PRI5_SEND	Port n Receive Priority 5 Send Count Value Register	Section 3.5.2.22
158h	Pn_PRI6_SEND	Port n Receive Priority 6 Send Count Value Register	Section 3.5.2.23
15Ch	Pn_PRI7_SEND	Port n Receive Priority 7 Send Count Value Register	Section 3.5.2.24
160h	Pn_PRI0_IDLE	Port n Receive Priority 0 Idle Count Value Register	Section 3.5.2.25
164h	Pn_PRI1_IDLE	Port n Receive Priority 1 Idle Count Value Register	Section 3.5.2.26
168h	Pn_PRI2_IDLE	Port n Receive Priority 2 Idle Count Value Register	Section 3.5.2.27
16Ch	Pn_PRI3_IDLE	Port n Receive Priority 3 Idle Count Value Register	Section 3.5.2.28
170h	Pn_PRI4_IDLE	Port n Receive Priority 4 Idle Count Value Register	Section 3.5.2.29
174h	Pn_PRI5_IDLE	Port n Receive Priority 5 Idle Count Value Register	Section 3.5.2.30
178h	Pn_PRI6_IDLE	Port n Receive Priority 6 Idle Count Value Register	Section 3.5.2.31
17Ch	Pn_PRI7_IDLE	Port n Receive Priority 7 Idle Count Value Register	Section 3.5.2.32
180h	Pn_TX_DEST_THRESH_SET_L	Port n Transmit Destination Threshold Set Low Register	Section 3.5.2.33
184h	Pn_TX_DEST_THRESH_SET_H	Port n Transmit Destination Threshold Set High Register	Section 3.5.2.34
188h	Pn_TX_DEST_THRESH_CLR_L	Port n Transmit Destination Threshold Clear Low Register	Section 3.5.2.35
18Ch	Pn_TX_DEST_THRESH_CLR_H	Port n Transmit Destination Threshold Clear High Register	Section 3.5.2.36
190h	Pn_TX_BUFFER_THRESH_SET_L	Port n Global Transmit Buffer Threshold Set Register Low	Section 3.5.2.37
194h	Pn_TX_BUFFER_THRESH_SET_H	Port n Global Transmit Buffer Threshold Set Register High	Section 3.5.2.38
198h	Pn_TX_BUFFER_THRESH_CLR_L	Port n Global Transmit Buffer Threshold Clear Register Low	Section 3.5.2.39
19Ch	Pn_TX_BUFFER_THRESH_CLR_H	Port n Global Transmit Buffer Threshold Clear Register High	Section 3.5.2.40
1A0h-2FCh	Reserved	Reserved	Reserved
300h-FFCh	Continued in Table 3-60 for host port 0 or Table 3-61 for Ethernet ports	The remainder of the port registers are specific to either the host port or to the Ethernet ports. See Table 3-60 for the remainder of the host port registers and see Table 3-61 for the remainder of the Ethernet port registers.	Continued in Table 3-60 or Table 3-61

Table 3-60. Host Port 0 Specific Submodule Registers

Offset Address[1]	Acronym	Description	Section
300h	P0_SRC_ID_A	Host Port 0 Source ID A Register	Section 3.5.2.41
304h	P0_SRC_ID_B	Host Port 0 Source ID B Register	Section 3.5.2.42
308h-31Ch	Reserved	Reserved	Reserved
320h	P0_HOST_BLKS_PRI	Host Port 0 Host Blocks Priority Register	Section 3.5.2.43
324h-FFCh	Reserved	Reserved	Reserved

(1) The actual addresses of these registers are device specific. See your device-specific data manual to verify the register addresses.

Table 3-61. Ethernet Port n Specific Submodule Registers (n = 1-4 for a 5 port switch or n = 1-8 for a 9 port switch)

Offset Address[1]	Acronym	Description	Section
300h	Pn_TX_DEST_OUTFLOW_ADDVAL_L	Port n Transmit Destination Out Flow Add Values Register Low	Section 3.5.2.44
304h	Pn_TX_DEST_OUTFLOW_ADDVAL_H	Port n Transmit Destination Out Flow Add Values Register High	Section 3.5.2.45
308h	Pn_PAUSE_SA_L	Port n Pause Frame Source Address Register Low	Section 3.5.2.46
30Ch	Pn_PAUSE_SA_H	Port n Pause Frame Source Address Register High	Section 3.5.2.47
310h	Pn_TS_CTL	Port n Time Sync Control Register	Section 3.5.2.48
314h	Pn_TS_SEQ_LTYPE	Port n Time Sync LTYPE and SEQ_ID_OFFSET register	Section 3.5.2.49
318h	Pn_TS_VLAN	Port n Time Sync VLAN LTYPE1 and VLAN LTYPE2 Register	Section 3.5.2.50
31Ch	Pn_TS_CTL_LTYPE2	Port n Time Sync Control and LTYPE2 Register	Section 3.5.2.51
320h	Pn_TS_CTL2	Port n Time Sync Control 2 Register	Section 3.5.2.52
324h-32Ch	Reserved	Reserved	Reserved
330h	Pn_MAC_CTL	Port n MAC Control Register	Section 3.5.2.53
334h	Pn_MAC_STATUS	Port n MAC Status Register	Section 3.5.2.54
338h	Pn_MAC_SOFT_RESET	Port n MAC Soft Reset Register	Section 3.5.2.55
33Ch	Pn_MAC_BACKOFF_TEST	Port n MAC Backoff Test Register	Section 3.5.2.56
340h	Pn_MAC_RX_PAUSETIMER	Port n 802.3 Receive Pause Timer Register	Section 3.5.2.57
344h-34Ch	Reserved	Reserved	Reserved
350h	Pn_MAC_RX_PRI0_PAUSETIMER	Port n Priority Flow Control Priority 0 Receive Pause Timer Register	Section 3.5.2.58
354h	Pn_MAC_RX_PRI1_PAUSETIMER	Port n Priority Flow Control Priority 1 Receive Pause Timer Register	Section 3.5.2.59
358h	Pn_MAC_RX_PRI2_PAUSETIMER	Port n Priority Flow Control Priority 2 Receive Pause Timer Register	Section 3.5.2.60
35Ch	Pn_MAC_RX_PRI3_PAUSETIMER	Port n Priority Flow Control Priority 3 Receive Pause Timer Register	Section 3.5.2.61
360h	Pn_MAC_RX_PRI4_PAUSETIMER	Port n Priority Flow Control Priority 4 Receive Pause Timer Register	Section 3.5.2.62
364h	Pn_MAC_RX_PRI5_PAUSETIMER	Port n Priority Flow Control Priority 5 Receive Pause Timer Register	Section 3.5.2.63
368h	Pn_MAC_RX_PRI6_PAUSETIMER	Port n Priority Flow Control Priority 6 Receive Pause Timer Register	Section 3.5.2.64
36Ch	Pn_MAC_RX_PRI7_PAUSETIMER	Port n Priority Flow Control Priority 7 Receive Pause Timer Register	Section 3.5.2.65
370h	Pn_MAC_TX_PAUSETIMER	Port n 802.3 Transmit Pause Timer Register	Section 3.5.2.66
374h-37Ch	Reserved	Reserved	Reserved
380h	Pn_MAC_TX_PRI0_PAUSETIMER	Port n Priority Flow Control Priority 0 Transmit Pause Timer Register	Section 3.5.2.67
384h	Pn_MAC_TX_PRI1_PAUSETIMER	Port n Priority Flow Control Priority 1 Transmit Pause Timer Register	Section 3.5.2.68
388h	Pn_MAC_TX_PRI2_PAUSETIMER	Port n Priority Flow Control Priority 2 Transmit Pause Timer Register	Section 3.5.2.69
38Ch	Pn_MAC_TX_PRI3_PAUSETIMER	Port n Priority Flow Control Priority 3 Transmit Pause Timer Register	Section 3.5.2.70
390h	Pn_MAC_TX_PRI4_PAUSETIMER	Port n Priority Flow Control Priority 4 Transmit Pause Timer Register	Section 3.5.2.71
394h	Pn_MAC_TX_PRI5_PAUSETIMER	Port n Priority Flow Control Priority 5 Transmit Pause Timer Register	Section 3.5.2.72

(1) The actual addresses of these registers are device specific. See your device-specific data manual to verify the register addresses.

Table 3-61. Ethernet Port n Specific Submodule Registers (n = 1-4 for a 5 port switch or n = 1-8 for a 9 port switch) (continued)

Offset Address[1]	Acronym	Description	Section
398h	Pn_MAC_TX_PRI6_PAUSETIMER	Port n Priority Flow Control Priority 6 Transmit Pause Timer Register	Section 3.5.2.73
39Ch	Pn_MAC_TX_PRI7_PAUSETIMER	Port n Priority Flow Control Priority 7 Transmit Pause Timer Register	Section 3.5.2.74
3A0h	Pn_MAC_EMCONTROL	Port n MAC Emulation Control Register	Section 3.5.2.75
3A4h	Pn_MAC_TX_GAP	Port n MAC Transmit Inter Packet Gap Register	Section 3.5.2.76
3A8h-FFCh	Reserved	Reserved	Reserved

3.5.2.1 Port n Control Register (Pn_CONTROL)

The Port n Control Register is shown in Figure 3-49 and described in Table 3-62.

Figure 3-49. Port n Control Register (Pn_CONTROL)

31	3	2	1	0
Reserved		DSCP_IPV6_EN	DSCP_IPV4_EN	Reserved
R-0h		R/W-0h	R/W-0h	R-0h

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-62. Port n Control Register (Pn_CONTROL) Field Descriptions

Bits	Field	Description
31-3	Reserved	Reserved
2	DSCP_IPV6_EN	Port n IPv6 Enable. • 0 = IPv6 DSCP priority mapping is disabled • 1 = IPv6 DSCP priority mapping is enabled
1	DSCP_IPV4_EN	Port n IPv4 Enable. • 0 = IPv4 DSCP priority mapping is disabled • 1 = IPv4 DSCP priority mapping is enabled
0	Reserved	Reserved

3.5.2.2 Port n FIFO Block Usage Count Register (Pn_BLK_CNT)

The Port n FIFO Block Usage Count Register is shown in Figure 3-50 and described in Table 3-63.

Figure 3-50. Port n FIFO Block Usage Count Register (Pn_BLK_CNT)

31	13	12	8	7	6	5	0
Reserved		TX_BLK_CNT		Reserved		RX_BLK_CNT	
R-0h		R-0h		R-0h		R-1h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-63. Port n FIFO Block Usage Count Register (Pn_BLK_CNT) Field Descriptions

Bits	Field	Description
31-13	Reserved	Reserved
12-8	TX_BLK_CNT	Port n Transmit Block Count Usage. This value is the number of blocks allocated to the FIFO logical transmit queues.
7-6	Reserved	Reserved
5-0	RX_BLK_CNT	Port n Received Block Count Usage. This value is the number of blocks allocated to the port's FIFO receive queue.

3.5.2.3 Port n VLAN Register (Pn_PORT_VLAN)

The Port n VLAN Register is shown in Figure 3-51 and described in Table 3-64.

Figure 3-51. Port n VLAN Register (Pn_PORT_VLAN)

31	16	15	13	12	11	0
Reserved		PORT_PRI		PORT_CFI	PORT_VID	
R-0h		R/W-0h		R/W-0h	R/W-0h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-64. Port n VLAN Register (Pn_PORT_VLAN) Field Descriptions

Bits	Field	Description
31-16	Reserved	Reserved
15-13	PORT_PRI	Port n VLAN Priority (7 is the highest).
12	PORT_CFI	Port n CFI bit.
11-0	PORT_VID	Port n VLAN ID

3.5.2.4 Port n Transmit Priority Mapping Register (Pn_TX_PRI_MAP)

The Port n Transmit Priority Mapping Register is shown in Figure 3-52 and described in Table 3-65.

Figure 3-52. Port n Transmit Priority Mapping Register (Pn_TX_PRI_MAP)

31	30 28	27	26 24	23	22 20	19	18 16
Reserved	PRI7	Reserved	PRI6	Reserved	PRI5	Reserved	PRI4
R-0h	R/W-7h	R-0h	R/W-6h	R-0h	R/W-5h	R-0h	R/W-4h
15	14 12	11	10 8	7	6 4	3	2 0
Reserved	PRI3	Reserved	PRI2	Reserved	PRI1	Reserved	PRI0
R-0h	R/W-3h	R-0h	R/W-2h	R-0h	R/W-1h	R-0h	R/W-0h

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-65. Port n Transmit Priority Mapping Register (Pn_TX_PRI_MAP) Field Descriptions

Bits	Field	Description
31	Reserved	Reserved
30-28	PRI7	Priority 7. A packet header priority of 0x7 is given this switch queue priority.
27	Reserved	Reserved
26-24	PRI6	Priority 6. A packet header priority of 0x6 is given this switch queue priority.
23	Reserved	Reserved
22-20	PRI5	Priority 5. A packet header priority of 0x5 is given this switch queue priority.
19	Reserved	Reserved
18-16	PRI4	Priority 4. A packet header priority of 0x4 is given this switch queue priority.
15	Reserved	Reserved
14-12	PRI3	Priority 3. A packet header priority of 0x3 is given this switch queue priority.
11	Reserved	Reserved
10-8	PRI2	Priority 2. A packet header priority of 0x2 is given this switch queue priority.
7	Reserved	Reserved
6-4	PRI1	Priority 1. A packet header priority of 0x1 is given this switch queue priority.
3	Reserved	Reserved
2-0	PRI0	Priority 0. A packet header priority of 0x0 is given this switch queue priority.

3.5.2.5 Port n Priority Control Register (Pn_PRI_CTL)

The Port n Priority Control Register has a different register mapping and field description based on whether the port is the host port or an external Ethernet port. The Priority Control Register for host port 0 is shown in Figure 3-53 and described in Table 3-66. The Priority Control Register for the external Ethernet ports is shown in Figure 3-54 and described in Table 3-67.

Figure 3-53. Port 0 Priority Control Register (P0_PRI_CTL)

31 24	23 16	15 9	8	7 0
Reserved	P0_RX_FLOW_PRI	Reserved	P0_RX_PTYPE	P0_RX_RLIM
R-0h	R/W-0h	R-0h	R/W-0h	R/W-0h

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-66. Port 0 Priority Control Register (P0_PRI_CTL) Field Descriptions

Bits	Field	Description
31-24	Reserved	Reserved
23-16	P0_RX_FLOW_PRI	Receive Priority Based Flow Control Enable. • 1 = Receive Priority Based Flow Control Enabled • 0 = Receive Priority Based Flow Control Disabled Each bit corresponds to a priority: • Bit 23 - Priority 7 • Bit 22 - Priority 6 • Bit 21 - Priority 5 • Bit 20 - Priority 4 • Bit 19 - Priority 3 • Bit 18 - Priority 2 • Bit 17 - Priority 1 • Bit 16 - Priority 0
15-9	Reserved	Reserved
8	P0_RX_PTYPE	Receive Priority Type • 1 = Round Robin Priority • 0 = Fixed Priority
7-0	P0_RX_RLIM	Receive Rate Limit Enable. P0_RX_PTYPE must be set to 0 (fixed priority) if any P0_RX_RLIM bit is set. This is for port 0 receive rate limiting into the switch (ingress). Port 0 transmit (egress) is not rate limited. • 00000000 = No rate-limited channels • 10000000 = Channel 7 is rate-limited • 11000000 = Channels 7 down to 6 are rate-limited • 11100000 = Channels 7 down to 5 are rate-limited • 11110000 = Channels 7 down to 4 are rate-limited • 11111000 = Channels 7 down to 3 are rate-limited • 11111100 = Channels 7 down to 2 are rate-limited • 11111110 = Channels 7 down to 1 are rate-limited • 11111111 = Channels 7 down to 0 are rate-limited • all other = Invalid. This bus must be set MSB towards LSB.

The Priority Control Register for the external Ethernet ports is shown in Figure 3-54 and described in Table 3-67.

Figure 3-54. External Ethernet Port n Priority Control Register (Pn_PRI_CTL)

31 24	23 16	15 12	11 8	7 0
TX_FLOW_PRI	RX_FLOW_PRI	TX_HOST_BLKS_REM	Reserved	TX_RLIM
R/W-0h	R/W-0h	R/W-9h	R-0h	R/W-0h

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-67. External Ethernet Port n Priority Control Register (Pn_PRI_CTL) Field Descriptions

Bits	Field	Description
31-24	TX_FLOW_PRI	Transmit Priority Based Flow Control Enable. • 1 = Transmit Priority Based Flow Control Enabled • 0 = Transmit Priority Based Flow Control Disabled Each bit corresponds to a priority: • Bit 31 - Priority 7 • Bit 30 - Priority 6 • Bit 29 - Priority 5 • Bit 28 - Priority 4 • Bit 27 - Priority 3 • Bit 26 - Priority 2 • Bit 25 - Priority 1 • Bit 24 - Priority 0
23-16	RX_FLOW_PRI	Receive Priority Based Flow Control Enable. • 1 = Receive Priority Based Flow Control Enabled • 0 = Receive Priority Based Flow Control Disabled Each bit corresponds to a priority: • Bit 23 - Priority 7 • Bit 22 - Priority 6 • Bit 21 - Priority 5 • Bit 20 - Priority 4 • Bit 19 - Priority 3 • Bit 18 - Priority 2 • Bit 17 - Priority 1 • Bit 16 - Priority 0
15-12	TX_HOST_BLKS_REM	Transmit FIFO blocks that must be free before a non rate-limited host port 0 receive thread can begin sending a packet to this port.
11-8	Reserved	Reserved
7-0	TX_RLIM	Transmit Priority Rate Limit Enable. This is for port n transmit (egress). • 00000000 = No rate-limited channels • 10000000 = Priority 7 is rate-limited • 11000000 = Priority 7 down to 6 are rate-limited • 11100000 = Priority 7 down to 5 are rate-limited • 11110000 = Priority 7 down to 4 are rate-limited • 11111000 = Priority 7 down to 3 are rate-limited • 11111100 = Priority 7 down to 2 are rate-limited • 11111110 = Priority 7 down to 1 are rate-limited • 11111111 = Priority 7 down to 0 are rate-limited • all other = Invalid. This bus must be set MSB towards LSB.

3.5.2.6 Port n Receive Priority Mapping Register (Pn_RX_PRI_MAP)

The Port n Receive Priority Mapping Register is shown in Figure 3-55 and described in Table 3-68.

Figure 3-55. Port n Receive Priority Mapping Register (Pn_RX_PRI_MAP)

31	30 28	27	26 24	23	22 20	19	18 16
Reserved	PRI7	Reserved	PRI6	Reserved	PRI5	Reserved	PRI4
R-0h	R/W-7h	R-0h	R/W-6h	R-0h	R/W-5h	R-0h	R/W-4h
15	14 12	11	10 8	7	6 4	3	2 0
Reserved	PRI3	Reserved	PRI2	Reserved	PRI1	Reserved	PRI0
R-0h	R/W-3h	R-0h	R/W-2h	R-0h	R/W-1h	R-0h	R/W-0h

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-68. Port n Receive Priority Mapping Register (Pn_RX_PRI_MAP) Field Descriptions

Bits	Field	Description
31	Reserved	Reserved
30-28	PRI7	Priority 7. A packet priority of 0x7 is mapped (changed) to this header packet priority.
27	Reserved	Reserved
26-24	PRI6	Priority 6. A packet priority of 0x6 is mapped (changed) to this header packet priority.
23	Reserved	Reserved
22-20	PRI5	Priority 5. A packet priority of 0x5 is mapped (changed) to this header packet priority.
19	Reserved	Reserved
18-16	PRI4	Priority 4. A packet priority of 0x4 is mapped (changed) to this header packet priority.
15	Reserved	Reserved
14-12	PRI3	Priority 3. A packet priority of 0x3 is mapped (changed) to this header packet priority.
11	Reserved	Reserved
10-8	PRI2	Priority 2. A packet priority of 0x2 is mapped (changed) to this header packet priority.
7	Reserved	Reserved
6-4	PRI1	Priority 1. A packet priority of 0x1 is mapped (changed) to this header packet priority.
3	Reserved	Reserved
2-0	PRI0	Priority 0. A packet priority of 0x0 is mapped (changed) to this header packet priority.

3.5.2.7 Port n Receive Frame Maximum Length Register (Pn_RX_MAXLEN)

The Port n Receive Frame Maximum Length Register is shown in Figure 3-56 and described in Table 3-69.

Figure 3-56. Port n Receive Frame Maximum Length Register (Pn_RX_MAXLEN)

31	14	13	0
Reserved		RX_MAXLEN	
R-0h		R/W-5EEh	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-69. Port n Receive Frame Maximum Length Register (Pn_RX_MAXLEN) Field Descriptions

Bits	Field	Description
31-14	Reserved	Reserved
13-0	RX_MAXLEN	RX Maximum Frame Length. This field determines the maximum length of a received frame. The reset value is 1518 (dec). Frames with byte counts greater than RX_MAXLEN are long frames. Long frames with no errors are oversized frames. Long frames with CRC, code, or alignment error are jabber frames. The maximum value is 9604 (including VLAN).

3.5.2.8 Port n Transmit Blocks Priority Register (Pn_TX_BLKS_PRI)

The Port n Transmit Blocks Priority Register is shown in Figure 3-57 and described in Table 3-70.

Figure 3-57. Port n Transmit Blocks Priority Register (Pn_TX_BLKS_PRI)

31 28	27 24	23 20	19 16	15 12	11 8	7 4	3 0
TX_BLKS_PRI7	TX_BLKS_PRI6	TX_BLKS_PRI5	TX_BLKS_PRI4	TX_BLKS_PRI3	TX_BLKS_PRI2	TX_BLKS_PRI1	TX_BLKS_PRI0
R/W-0h	R/W-1h	R/W-2h	R/W-4h	R/W-5h	R/W-6h	R/W-7h	R/W-8h

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-70. Port n Transmit Blocks Priority Register (Pn_TX_BLKS_PRI) Field Descriptions

Bits	Field	Description
31-28	TX_BLKS_PRI7	Port Transmit Blocks Priority 7
27-24	TX_BLKS_PRI6	Port Transmit Blocks Priority 6
23-20	TX_BLKS_PRI5	Port Transmit Blocks Priority 5
19-16	TX_BLKS_PRI4	Port Transmit Blocks Priority 4
15-12	TX_BLKS_PRI3	Port Transmit Blocks Priority 3
11-8	TX_BLKS_PRI2	Port Transmit Blocks Priority 2
7-4	TX_BLKS_PRI1	Port Transmit Blocks Priority 1
3-0	TX_BLKS_PRI0	Port Transmit Blocks Priority 0

3.5.2.9 Port n Receive IPv4/IPv6 DSCP Priority Mapping Register 0 (Pn_RX_DSCP_MAP0)

The Port n Receive IPv4/IPv6 DSCP Priority Mapping Register 0 is shown in Figure 3-58 and described in Table 3-71.

Figure 3-58. Port n Receive IPv4/IPv6 DSCP Priority Mapping Register 0 (Pn_RX_DSCP_MAP0)

31	30 28	27	26 24	23	22 20	19	18 16
Reserved	DSCP_PRI7	Reserved	DSCP_PRI6	Reserved	DSCP_PRI5	Reserved	DSCP_PRI4
R-0h	R/W-0h	R-0h	R/W-0h	R-0h	R/W-0h	R-0h	R/W-0h
15	14 12	11	10 8	7	6 4	3	2 0
Reserved	DSCP_PRI3	Reserved	DSCP_PRI2	Reserved	DSCP_PRI1	Reserved	DSCP_PRI0
R-0h	R/W-0h	R-0h	R/W-0h	R-0h	R/W-0h	R-0h	R/W-0h

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-71. Port n Receive IPv4/IPv6 DSCP Priority Mapping Register 0 (Pn_RX_DSCP_MAP0) Field Descriptions

Bits	Field	Description
31	Reserved	Reserved
30-28	DSCP_PRI7	A DSCP V4/V6 packet TOS of 7 (decimal) is mapped to this receive priority.
27	Reserved	Reserved
26-24	DSCP_PRI6	A DSCP V4/V6 packet TOS of 6 (decimal) is mapped to this receive priority.
23	Reserved	Reserved
22-20	DSCP_PRI5	A DSCP V4/V6 packet TOS of 5 (decimal) is mapped to this receive priority.
19	Reserved	Reserved
18-16	DSCP_PRI4	A DSCP V4/V6 packet TOS of 4 (decimal) is mapped to this receive priority.
15	Reserved	Reserved
14-12	DSCP_PRI3	A DSCP V4/V6 packet TOS of 3 (decimal) is mapped to this receive priority.
11	Reserved	Reserved
10-8	DSCP_PRI2	A DSCP V4/V6 packet TOS of 2 (decimal) is mapped to this receive priority.
7	Reserved	Reserved
6-4	DSCP_PRI1	A DSCP V4/V6 packet TOS of 1 (decimal) is mapped to this receive priority.
3	Reserved	Reserved
2-0	DSCP_PRI0	A DSCP V4/V6 packet TOS of 0 (decimal) is mapped to this receive priority.

3.5.2.10 Port n Receive IPv4/IPv6 DSCP Priority Mapping Register 1 (Pn_RX_DSCP_MAP1)

The Port n Receive IPv4/IPv6 DSCP Priority Mapping Register 1 is shown in Figure 3-59 and described in Table 3-72.

Figure 3-59. Port n Receive IPv4/IPv6 DSCP Priority Mapping Register 1 (Pn_RX_DSCP_MAP1)

31	30 28	27	26 24	23	22 20	19	18 16
Reserved	DSCP_PRI15	Reserved	DSCP_PRI14	Reserved	DSCP_PRI13	Reserved	DSCP_PRI12
R-0h	R/W-0h	R-0h	R/W-0h	R-0h	R/W-0h	R-0h	R/W-0h
15	14 12	11	10 8	7	6 4	3	2 0
Reserved	DSCP_PRI11	Reserved	DSCP_PRI10	Reserved	DSCP_PRI9	Reserved	DSCP_PRI8
R-0h	R/W-0h	R-0h	R/W-0h	R-0h	R/W-0h	R-0h	R/W-0h

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-72. Port n Receive IPv4/IPv6 DSCP Priority Mapping Register 1 (Pn_RX_DSCP_MAP1) Field Descriptions

Bits	Field	Description
31	Reserved	Reserved
30-28	DSCP_PRI15	A DSCP V4/V6 packet TOS of 15 (decimal) is mapped to this receive priority.
27	Reserved	Reserved
26-24	DSCP_PRI14	A DSCP V4/V6 packet TOS of 14 (decimal) is mapped to this receive priority.
23	Reserved	Reserved
22-20	DSCP_PRI13	A DSCP V4/V6 packet TOS of 13 (decimal) is mapped to this receive priority.
19	Reserved	Reserved
18-16	DSCP_PRI12	A DSCP V4/V6 packet TOS of 12 (decimal) is mapped to this receive priority.
15	Reserved	Reserved
14-12	DSCP_PRI11	A DSCP V4/V6 packet TOS of 11 (decimal) is mapped to this receive priority.
11	Reserved	Reserved
10-8	DSCP_PRI10	A DSCP V4/V6 packet TOS of 10 (decimal) is mapped to this receive priority.
7	Reserved	Reserved
6-4	DSCP_PRI9	A DSCP V4/V6 packet TOS of 9 (decimal) is mapped to this receive priority.
3	Reserved	Reserved
2-0	DSCP_PRI8	A DSCP V4/V6 packet TOS of 8 (decimal) is mapped to this receive priority.

3.5.2.11 Port n Receive IPv4/IPv6 DSCP Priority Mapping Register 2 (Pn_RX_DSCP_MAP2)

The Port n Receive IPv4/IPv6 DSCP Priority Mapping Register 2 is shown in Figure 3-60 and described in Table 3-73.

Figure 3-60. Port n Receive IPv4/IPv6 DSCP Priority Mapping Register 2 (Pn_RX_DSCP_MAP2)

31	30 28	27	26 24	23	22 20	19	18 16
Reserved	DSCP_PRI23	Reserved	DSCP_PRI22	Reserved	DSCP_PRI21	Reserved	DSCP_PRI20
R-0h	R/W-0h	R-0h	R/W-0h	R-0h	R/W-0h	R-0h	R/W-0h
15	14 12	11	10 8	7	6 4	3	2 0
Reserved	DSCP_PRI19	Reserved	DSCP_PRI18	Reserved	DSCP_PRI17	Reserved	DSCP_PRI16
R-0h	R/W-0h	R-0h	R/W-0h	R-0h	R/W-0h	R-0h	R/W-0h

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-73. Port n Receive IPv4/IPv6 DSCP Priority Mapping Register 2 (Pn_RX_DSCP_MAP2) Field Descriptions

Bits	Field	Description
31	Reserved	Reserved
30-28	DSCP_PRI23	A DSCP V4/V6 packet TOS of 23 (decimal) is mapped to this receive priority.
27	Reserved	Reserved
26-24	DSCP_PRI22	A DSCP V4/V6 packet TOS of 22 (decimal) is mapped to this receive priority.
23	Reserved	Reserved
22-20	DSCP_PRI21	A DSCP V4/V6 packet TOS of 21 (decimal) is mapped to this receive priority.
19	Reserved	Reserved
18-16	DSCP_PRI20	A DSCP V4/V6 packet TOS of 20 (decimal) is mapped to this receive priority.
15	Reserved	Reserved
14-12	DSCP_PRI19	A DSCP V4/V6 packet TOS of 19 (decimal) is mapped to this receive priority.
11	Reserved	Reserved
10-8	DSCP_PRI18	A DSCP V4/V6 packet TOS of 18 (decimal) is mapped to this receive priority.
7	Reserved	Reserved
6-4	DSCP_PRI17	A DSCP V4/V6 packet TOS of 17 (decimal) is mapped to this receive priority.
3	Reserved	Reserved
2-0	DSCP_PRI16	A DSCP V4/V6 packet TOS of 16 (decimal) is mapped to this receive priority.

3.5.2.12 Port n Receive IPv4/IPv6 DSCP Priority Mapping Register 3 (Pn_RX_DSCP_MAP3)

The Port n Receive IPv4/IPv6 DSCP Priority Mapping Register 3 is shown in Figure 3-61 and described in Table 3-74.

Figure 3-61. Port n Receive IPv4/IPv6 DSCP Priority Mapping Register 3 (Pn_RX_DSCP_MAP3)

31	30 28	27	26 24	23	22 20	19	18 16
Reserved	DSCP_PRI31	Reserved	DSCP_PRI30	Reserved	DSCP_PRI29	Reserved	DSCP_PRI28
R-0h	R/W-0h	R-0h	R/W-0h	R-0h	R/W-0h	R-0h	R/W-0h
15	14 12	11	10 8	7	6 4	3	2 0
Reserved	DSCP_PRI27	Reserved	DSCP_PRI26	Reserved	DSCP_PRI25	Reserved	DSCP_PRI24
R-0h	R/W-0h	R-0h	R/W-0h	R-0h	R/W-0h	R-0h	R/W-0h

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-74. Port n Receive IPv4/IPv6 DSCP Priority Mapping Register 3 (Pn_RX_DSCP_MAP3) Field Descriptions

Bits	Field	Description
31	Reserved	Reserved
30-28	DSCP_PRI31	A DSCP V4/V6 packet TOS of 31 (decimal) is mapped to this receive priority.
27	Reserved	Reserved
26-24	DSCP_PRI30	A DSCP V4/V6 packet TOS of 30 (decimal) is mapped to this receive priority.
23	Reserved	Reserved
22-20	DSCP_PRI29	A DSCP V4/V6 packet TOS of 29 (decimal) is mapped to this receive priority.
19	Reserved	Reserved
18-16	DSCP_PRI28	A DSCP V4/V6 packet TOS of 28 (decimal) is mapped to this receive priority.
15	Reserved	Reserved
14-12	DSCP_PRI27	A DSCP V4/V6 packet TOS of 27 (decimal) is mapped to this receive priority.
11	Reserved	Reserved
10-8	DSCP_PRI26	A DSCP V4/V6 packet TOS of 26 (decimal) is mapped to this receive priority.
7	Reserved	Reserved
6-4	DSCP_PRI25	A DSCP V4/V6 packet TOS of 25 (decimal) is mapped to this receive priority.
3	Reserved	Reserved
2-0	DSCP_PRI24	A DSCP V4/V6 packet TOS of 24 (decimal) is mapped to this receive priority.

3.5.2.13 Port n Receive IPv4/IPv6 DSCP Priority Mapping Register 4 (Pn_RX_DSCP_MAP4)

The Port n Receive IPv4/IPv6 DSCP Priority Mapping Register 4 is shown in Figure 3-62 and described in Table 3-75.

Figure 3-62. Port n Receive IPv4/IPv6 DSCP Priority Mapping Register 4 (Pn_RX_DSCP_MAP4)

31	30 28	27	26 24	23	22 20	19	18 16
Reserved	DSCP_PRI39	Reserved	DSCP_PRI38	Reserved	DSCP_PRI37	Reserved	DSCP_PRI36
R-0h	R/W-0h	R-0h	R/W-0h	R-0h	R/W-0h	R-0h	R/W-0h
15	14 12	11	10 8	7	6 4	3	2 0
Reserved	DSCP_PRI35	Reserved	DSCP_PRI34	Reserved	DSCP_PRI33	Reserved	DSCP_PRI32
R-0h	R/W-0h	R-0h	R/W-0h	R-0h	R/W-0h	R-0h	R/W-0h

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-75. Port n Receive IPv4/IPv6 DSCP Priority Mapping Register 4 (Pn_RX_DSCP_MAP4) Field Descriptions

Bits	Field	Description
31	Reserved	Reserved
30-28	DSCP_PRI39	A DSCP V4/V6 packet TOS of 39 (decimal) is mapped to this receive priority.
27	Reserved	Reserved
26-24	DSCP_PRI38	A DSCP V4/V6 packet TOS of 38 (decimal) is mapped to this receive priority.
23	Reserved	Reserved
22-20	DSCP_PRI37	A DSCP V4/V6 packet TOS of 37 (decimal) is mapped to this receive priority.
19	Reserved	Reserved
18-16	DSCP_PRI36	A DSCP V4/V6 packet TOS of 36 (decimal) is mapped to this receive priority.
15	Reserved	Reserved
14-12	DSCP_PRI35	A DSCP V4/V6 packet TOS of 35 (decimal) is mapped to this receive priority.
11	Reserved	Reserved
10-8	DSCP_PRI34	A DSCP V4/V6 packet TOS of 34 (decimal) is mapped to this receive priority.
7	Reserved	Reserved
6-4	DSCP_PRI33	A DSCP V4/V6 packet TOS of 33 (decimal) is mapped to this receive priority.
3	Reserved	Reserved
2-0	DSCP_PRI32	A DSCP V4/V6 packet TOS of 32 (decimal) is mapped to this receive priority.

3.5.2.14 Port n Receive IPv4/IPv6 DSCP Priority Mapping Register 5 (Pn_RX_DSCP_MAP5)

The Port n Receive IPv4/IPv6 DSCP Priority Mapping Register 5 is shown in Figure 3-63 and described in Table 3-76.

Figure 3-63. Port n Receive IPv4/IPv6 DSCP Priority Mapping Register 5 (Pn_RX_DSCP_MAP5)

31	30 28	27	26 24	23	22 20	19	18 16
Reserved	DSCP_PRI47	Reserved	DSCP_PRI46	Reserved	DSCP_PRI45	Reserved	DSCP_PRI44
R-0h	R/W-0h	R-0h	R/W-0h	R-0h	R/W-0h	R-0h	R/W-0h
15	14 12	11	10 8	7	6 4	3	2 0
Reserved	DSCP_PRI43	Reserved	DSCP_PRI42	Reserved	DSCP_PRI41	Reserved	DSCP_PRI40
R-0h	R/W-0h	R-0h	R/W-0h	R-0h	R/W-0h	R-0h	R/W-0h

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-76. Port n Receive IPv4/IPv6 DSCP Priority Mapping Register 5 (Pn_RX_DSCP_MAP5) Field Descriptions

Bits	Field	Description
31	Reserved	Reserved
30-28	DSCP_PRI47	A DSCP V4/V6 packet TOS of 47 (decimal) is mapped to this receive priority.
27	Reserved	Reserved
26-24	DSCP_PRI46	A DSCP V4/V6 packet TOS of 46 (decimal) is mapped to this receive priority.
23	Reserved	Reserved
22-20	DSCP_PRI45	A DSCP V4/V6 packet TOS of 45 (decimal) is mapped to this receive priority.
19	Reserved	Reserved
18-16	DSCP_PRI44	A DSCP V4/V6 packet TOS of 44 (decimal) is mapped to this receive priority.
15	Reserved	Reserved
14-12	DSCP_PRI43	A DSCP V4/V6 packet TOS of 43 (decimal) is mapped to this receive priority.
11	Reserved	Reserved
10-8	DSCP_PRI42	A DSCP V4/V6 packet TOS of 42 (decimal) is mapped to this receive priority.
7	Reserved	Reserved
6-4	DSCP_PRI41	A DSCP V4/V6 packet TOS of 41 (decimal) is mapped to this receive priority.
3	Reserved	Reserved
2-0	DSCP_PRI40	A DSCP V4/V6 packet TOS of 40 (decimal) is mapped to this receive priority.

3.5.2.15 Port n Receive IPv4/IPv6 DSCP Priority Mapping Register 6 (Pn_RX_DSCP_MAP6)

The Port n Receive IPv4/IPv6 DSCP Priority Mapping Register 6 is shown in Figure 3-64 and described in Table 3-77.

Figure 3-64. Port n Receive IPv4/IPv6 DSCP Priority Mapping Register 6 (Pn_RX_DSCP_MAP6)

31	30 28	27	26 24	23	22 20	19	18 16
Reserved	DSCP_PRI55	Reserved	DSCP_PRI54	Reserved	DSCP_PRI53	Reserved	DSCP_PRI52
R-0h	R/W-0h	R-0h	R/W-0h	R-0h	R/W-0h	R-0h	R/W-0h
15	14 12	11	10 8	7	6 4	3	2 0
Reserved	DSCP_PRI51	Reserved	DSCP_PRI50	Reserved	DSCP_PRI49	Reserved	DSCP_PRI48
R-0h	R/W-0h	R-0h	R/W-0h	R-0h	R/W-0h	R-0h	R/W-0h

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-77. Port n Receive IPv4/IPv6 DSCP Priority Mapping Register 6 (Pn_RX_DSCP_MAP6) Field Descriptions

Bits	Field	Description
31	Reserved	Reserved
30-28	DSCP_PRI55	A DSCP V4/V6 packet TOS of 55 (decimal) is mapped to this receive priority.
27	Reserved	Reserved
26-24	DSCP_PRI54	A DSCP V4/V6 packet TOS of 54 (decimal) is mapped to this receive priority.
23	Reserved	Reserved
22-20	DSCP_PRI53	A DSCP V4/V6 packet TOS of 53 (decimal) is mapped to this receive priority.
19	Reserved	Reserved
18-16	DSCP_PRI52	A DSCP V4/V6 packet TOS of 52 (decimal) is mapped to this receive priority.
15	Reserved	Reserved
14-12	DSCP_PRI51	A DSCP V4/V6 packet TOS of 51 (decimal) is mapped to this receive priority.
11	Reserved	Reserved
10-8	DSCP_PRI50	A DSCP V4/V6 packet TOS of 50 (decimal) is mapped to this receive priority.
7	Reserved	Reserved
6-4	DSCP_PRI49	A DSCP V4/V6 packet TOS of 49 (decimal) is mapped to this receive priority.
3	Reserved	Reserved
2-0	DSCP_PRI48	A DSCP V4/V6 packet TOS of 48 (decimal) is mapped to this receive priority.

3.5.2.16 Port n Receive IPv4/IPv6 DSCP Priority Mapping Register 7 (Pn_RX_DSCP_MAP7)

The Port n Receive IPv4/IPv6 DSCP Priority Mapping Register 7 is shown in Figure 3-64 and described in Table 3-77.

Figure 3-65. Port n Receive IPv4/IPv6 DSCP Priority Mapping Register 7 (Pn_RX_DSCP_MAP7)

31	30 28	27	26 24	23	22 20	19	18 16
Reserved	DSCP_PRI63	Reserved	DSCP_PRI62	Reserved	DSCP_PRI61	Reserved	DSCP_PRI60
R-0h	R/W-0h	R-0h	R/W-0h	R-0h	R/W-0h	R-0h	R/W-0h
15	14 12	11	10 8	7	6 4	3	2 0
Reserved	DSCP_PRI59	Reserved	DSCP_PRI58	Reserved	DSCP_PRI57	Reserved	DSCP_PRI56
R-0h	R/W-0h	R-0h	R/W-0h	R-0h	R/W-0h	R-0h	R/W-0h

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-78. Port n Receive IPv4/IPv6 DSCP Priority Mapping Register 7 (Pn_RX_DSCP_MAP7) Field Descriptions

Bits	Field	Description
31	Reserved	Reserved
30-28	DSCP_PRI63	A DSCP V4/V6 packet TOS of 63 (decimal) is mapped to this receive priority.
27	Reserved	Reserved
26-24	DSCP_PRI62	A DSCP V4/V6 packet TOS of 62 (decimal) is mapped to this receive priority.
23	Reserved	Reserved
22-20	DSCP_PRI61	A DSCP V4/V6 packet TOS of 61 (decimal) is mapped to this receive priority.
19	Reserved	Reserved
18-16	DSCP_PRI60	A DSCP V4/V6 packet TOS of 60 (decimal) is mapped to this receive priority.
15	Reserved	Reserved
14-12	DSCP_PRI59	A DSCP V4/V6 packet TOS of 59 (decimal) is mapped to this receive priority.
11	Reserved	Reserved
10-8	DSCP_PRI58	A DSCP V4/V6 packet TOS of 58 (decimal) is mapped to this receive priority.
7	Reserved	Reserved
6-4	DSCP_PRI57	A DSCP V4/V6 packet TOS of 57 (decimal) is mapped to this receive priority.
3	Reserved	Reserved
2-0	DSCP_PRI56	A DSCP V4/V6 packet TOS of 56 (decimal) is mapped to this receive priority.

3.5.2.17 Port n Receive Priority 0 Send Count Value Register (Pn_PRI0_SEND)

The Port n Receive Priority 0 Send Count Value Register is shown in Figure 3-66 and described in Table 3-79.

Figure 3-66. Port n Receive Priority 0 Send Count Value Register (Pn_PRI0_SEND)

31	18	17	0
Reserved		PRI0_SEND	
R-0h		R/W-0h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-79. Port n Receive Priority 0 Send Count Value Register (Pn_PRI0_SEND) Field Descriptions

Bits	Field	Description
31-18	Reserved	Reserved
17-0	PRI0_SEND	Priority 0 Send Count.

3.5.2.18 Port n Receive Priority 1 Send Count Value Register (Pn_PRI1_SEND)

The Port n Receive Priority 1 Send Count Value Register is shown in Figure 3-67 and described in Table 3-80.

Figure 3-67. Port n Receive Priority 1 Send Count Value Register (Pn_PRI1_SEND)

31	18	17	0
Reserved		PRI1_SEND	
R-0h		R/W-0h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-80. Port n Receive Priority 1 Send Count Value Register (Pn_PRI1_SEND) Field Descriptions

Bits	Field	Description
31-18	Reserved	Reserved
17-0	PRI1_SEND	Priority 1 Send Count.

3.5.2.19 Port n Receive Priority 2 Send Count Value Register (Pn_PRI2_SEND)

The Port n Receive Priority 2 Send Count Value Register is shown in Figure 3-68 and described in Table 3-81.

Figure 3-68. Port n Receive Priority 2 Send Count Value Register (Pn_PRI2_SEND)

31	18	17	0
Reserved		PRI2_SEND	
R-0h		R/W-0h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-81. Port n Receive Priority 2 Send Count Value Register (Pn_PRI2_SEND) Field Descriptions

Bits	Field	Description
31-18	Reserved	Reserved
17-0	PRI2_SEND	Priority 2 Send Count.

3.5.2.20 Port n Receive Priority 3 Send Count Value Register (Pn_PRI3_SEND)

The Port n Receive Priority 3 Send Count Value Register is shown in Figure 3-69 and described in Table 3-82.

Figure 3-69. Port n Receive Priority 3 Send Count Value Register (Pn_PRI3_SEND)

31	18	17	0
Reserved		PRI3_SEND	
R-0h		R/W-0h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-82. Port n Receive Priority 3 Send Count Value Register (Pn_PRI3_SEND) Field Descriptions

Bits	Field	Description
31-18	Reserved	Reserved
17-0	PRI3_SEND	Priority 3 Send Count.

3.5.2.21 Port n Receive Priority 4 Send Count Value Register (Pn_PRI4_SEND)

The Port n Receive Priority 4 Send Count Value Register is shown in Figure 3-70 and described in Table 3-83.

Figure 3-70. Port n Receive Priority 4 Send Count Value Register (Pn_PRI4_SEND)

31	18	17	0
Reserved		PRI4_SEND	
R-0h		R/W-0h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-83. Port n Receive Priority 4 Send Count Value Register (Pn_PRI4_SEND) Field Descriptions

Bits	Field	Description
31-18	Reserved	Reserved
17-0	PRI4_SEND	Priority 4 Send Count.

3.5.2.22 Port n Receive Priority 5 Send Count Value Register (Pn_PRI5_SEND)

The Port n Receive Priority 5 Send Count Value Register is shown in Figure 3-71 and described in Table 3-84.

Figure 3-71. Port n Receive Priority 5 Send Count Value Register (Pn_PRI5_SEND)

31	18	17	0
Reserved		PRI5_SEND	
R-0h		R/W-0h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-84. Port n Receive Priority 5 Send Count Value Register (Pn_PRI5_SEND) Field Descriptions

Bits	Field	Description
31-18	Reserved	Reserved
17-0	PRI5_SEND	Priority 5 Send Count.

3.5.2.23 Port n Receive Priority 6 Send Count Value Register (Pn_PRI6_SEND)

The Port n Receive Priority 6 Send Count Value Register is shown in Figure 3-72 and described in Table 3-85.

Figure 3-72. Port n Receive Priority 6 Send Count Value Register (Pn_PRI6_SEND)

31	18	17	0
Reserved		PRI6_SEND	
R-0h		R/W-0h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-85. Port n Receive Priority 6 Send Count Value Register (Pn_PRI6_SEND) Field Descriptions

Bits	Field	Description
31-18	Reserved	Reserved
17-0	PRI6_SEND	Priority 6 Send Count.

3.5.2.24 Port n Receive Priority 7 Send Count Value Register (Pn_PRI7_SEND)

The Port n Receive Priority 7 Send Count Value Register is shown in Figure 3-73 and described in Table 3-86.

Figure 3-73. Port n Receive Priority 7 Send Count Value Register (Pn_PRI7_SEND)

31	18	17	0
Reserved		PRI7_SEND	
R-0h		R/W-0h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-86. Port n Receive Priority 7 Send Count Value Register (Pn_PRI7_SEND) Field Descriptions

Bits	Field	Description
31-18	Reserved	Reserved
17-0	PRI7_SEND	Priority 7 Send Count.

3.5.2.25 Port n Receive Priority 0 Idle Count Value Register (Pn_PRI0_IDLE)

The Port n Receive Priority 0 Idle Count Value Register is shown in Figure 3-74 and described in Table 3-87.

Figure 3-74. Port n Receive Priority 0 Idle Count Value Register (Pn_PRI0_IDLE)

31	18	17	0
Reserved		PRI0_IDLE	
R-0h		R/W-0h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-87. Port n Receive Priority 0 Idle Count Value Register (Pn_PRI0_IDLE) Field Descriptions

Bits	Field	Description
31-18	Reserved	Reserved
17-0	PRI0_IDLE	Priority 0 Idle Count.

3.5.2.26 Port n Receive Priority 1 Idle Count Value Register (Pn_PRI1_IDLE)

The Port n Receive Priority 1 Idle Count Value Register is shown in Figure 3-75 and described in Table 3-88.

Figure 3-75. Port n Receive Priority 1 Idle Count Value Register (Pn_PRI1_IDLE)

31	18	17	0
Reserved		PRI1_IDLE	
R-0h		R/W-0h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-88. Port n Receive Priority 1 Idle Count Value Register (Pn_PRI1_IDLE) Field Descriptions

Bits	Field	Description
31-18	Reserved	Reserved
17-0	PRI1_IDLE	Priority 1 Idle Count.

3.5.2.27 Port n Receive Priority 2 Idle Count Value Register (Pn_PRI2_IDLE)

The Port n Receive Priority 2 Idle Count Value Register is shown in Figure 3-76 and described in Table 3-89.

Figure 3-76. Port n Receive Priority 2 Idle Count Value Register (Pn_PRI2_IDLE)

31	18	17	0
Reserved		PRI2_IDLE	
R-0h		R/W-0h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-89. Port n Receive Priority 2 Idle Count Value Register (Pn_PRI2_IDLE) Field Descriptions

Bits	Field	Description
31-18	Reserved	Reserved
17-0	PRI2_IDLE	Priority 2 Idle Count.

3.5.2.28 Port n Receive Priority 3 Idle Count Value Register (Pn_PRI3_IDLE)

The Port n Receive Priority 3 Idle Count Value Register is shown in Figure 3-77 and described in Table 3-90.

Figure 3-77. Port n Receive Priority 3 Idle Count Value Register (Pn_PRI3_IDLE)

31	18	17	0
Reserved		PRI3_IDLE	
R-0h		R/W-0h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-90. Port n Receive Priority 3 Idle Count Value Register (Pn_PRI3_IDLE) Field Descriptions

Bits	Field	Description
31-18	Reserved	Reserved
17-0	PRI3_IDLE	Priority 3 Idle Count.

3.5.2.29 Port n Receive Priority 4 Idle Count Value Register (Pn_PRI4_IDLE)

The Port n Receive Priority 4 Idle Count Value Register is shown in Figure 3-78 and described in Table 3-91.

Figure 3-78. Port n Receive Priority 4 Idle Count Value Register (Pn_PRI4_IDLE)

31	18	17	0
Reserved		PRI4_IDLE	
R-0h		R/W-0h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-91. Port n Receive Priority 4 Idle Count Value Register (Pn_PRI4_IDLE) Field Descriptions

Bits	Field	Description
31-18	Reserved	Reserved
17-0	PRI4_IDLE	Priority 4 Idle Count.

3.5.2.30 Port n Receive Priority 5 Idle Count Value Register (Pn_PRI5_IDLE)

The Port n Receive Priority 5 Idle Count Value Register is shown in Figure 3-79 and described in Table 3-92.

Figure 3-79. Port n Receive Priority 5 Idle Count Value Register (Pn_PRI5_IDLE)

31	18	17	0
Reserved		PRI5_IDLE	
R-0h		R/W-0h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-92. Port n Receive Priority 5 Idle Count Value Register (Pn_PRI5_IDLE) Field Descriptions

Bits	Field	Description
31-18	Reserved	Reserved
17-0	PRI5_IDLE	Priority 5 Idle Count.

3.5.2.31 Port n Receive Priority 6 Idle Count Value Register (Pn_PRI6_IDLE)

The Port n Receive Priority 6 Idle Count Value Register is shown in Figure 3-80 and described in Table 3-93.

Figure 3-80. Port n Receive Priority 6 Idle Count Value Register (Pn_PRI6_IDLE)

31	18	17	0
Reserved		PRI6_IDLE	
R-0h		R/W-0h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-93. Port n Receive Priority 6 Idle Count Value Register (Pn_PRI6_IDLE) Field Descriptions

Bits	Field	Description
31-18	Reserved	Reserved
17-0	PRI6_IDLE	Priority 6 Idle Count.

3.5.2.32 Port n Receive Priority 7 Idle Count Value Register (Pn_PRI7_IDLE)

The Port n Receive Priority 7 Idle Count Value Register is shown in Figure 3-81 and described in Table 3-94.

Figure 3-81. Port n Receive Priority 7 Idle Count Value Register (Pn_PRI7_IDLE)

31	18	17	0
Reserved		PRI7_IDLE	
R-0h		R/W-0h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-94. Port n Receive Priority 7 Idle Count Value Register (Pn_PRI7_IDLE) Field Descriptions

Bits	Field	Description
31-18	Reserved	Reserved
17-0	PRI7_IDLE	Priority 7 Idle Count.

3.5.2.33 Port n Transmit Destination Threshold Set Low Register (Pn_TX_DEST_THRESH_SET_L)

The Port n Transmit Destination Threshold Set Low Register is shown in Figure 3-82 and described in Table 3-95.

Figure 3-82. Port n Transmit Destination Threshold Set Low Register (Pn_TX_DEST_THRESH_SET_L)

31 29	28 24	23 21	20 16	15 13	12 8	7 5	4 0
Reserved	THRESH_SET3	Reserved	THRESH_SET2	Reserved	THRESH_SET1	Reserved	THRESH_SET0
R-0h	R/W-1Fh	R-0h	R/W-1Fh	R-0h	R/W-1Fh	R-0h	R/W-1Fh

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-95. Port n Transmit Destination Threshold Set Low Register (Pn_TX_DEST_THRESH_SET_L) Field Descriptions

Bits	Field	Description
31-29	Reserved	Reserved
28-24	THRESH_SET3	Port Priority Based Flow Control Threshold Set Value for Priority 3.
23-21	Reserved	Reserved
20-16	THRESH_SET2	Port Priority Based Flow Control Threshold Set Value for Priority 2.
15-13	Reserved	Reserved
12-8	THRESH_SET1	Port Priority Based Flow Control Threshold Set Value for Priority 1.
7-5	Reserved	Reserved
4-0	THRESH_SET0	Port Priority Based Flow Control Threshold Set Value for Priority 0.

3.5.2.34 Port n Transmit Destination Threshold Set High Register (Pn_TX_DEST_THRESH_SET_H)

The Port n Transmit Destination Threshold Set High Register is shown in Figure 3-83 and described in Table 3-96.

Figure 3-83. Port n Transmit Destination Threshold Set High Register (Pn_TX_DEST_THRESH_SET_H)

31 29	28 24	23 21	20 16	15 13	12 8	7 5	4 0
Reserved	THRESH_SET7	Reserved	THRESH_SET6	Reserved	THRESH_SET5	Reserved	THRESH_SET4
R-0h	R/W-1Fh	R-0h	R/W-1Fh	R-0h	R/W-1Fh	R-0h	R/W-1Fh

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-96. Port n Transmit Destination Threshold Set High Register (Pn_TX_DEST_THRESH_SET_H) Field Descriptions

Bits	Field	Description
31-29	Reserved	Reserved
28-24	THRESH_SET7	Port Priority Based Flow Control Threshold Set Value for Priority 7.
23-21	Reserved	Reserved
20-16	THRESH_SET6	Port Priority Based Flow Control Threshold Set Value for Priority 6.
15-13	Reserved	Reserved
12-8	THRESH_SET5	Port Priority Based Flow Control Threshold Set Value for Priority 5.
7-5	Reserved	Reserved
4-0	THRESH_SET4	Port Priority Based Flow Control Threshold Set Value for Priority 4.

3.5.2.35 Port n Transmit Destination Threshold Clear Low Register (Pn_TX_DEST_THRESH_CLR_L)

The Port n Transmit Destination Threshold Clear Low Register is shown in Figure 3-84 and described in Table 3-97.

Figure 3-84. Port n Transmit Destination Threshold Clear Low Register (Pn_TX_DEST_THRESH_CLR_L)

31 29	28 24	23 21	20 16	15 13	12 8	7 5	4 0
Reserved	THRESH_CLR3	Reserved	THRESH_CLR2	Reserved	THRESH_CLR1	Reserved	THRESH_CLR0
R-0h	R/W-0h	R-0h	R/W-0h	R-0h	R/W-0h	R-0h	R/W-0h

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-97. Port n Transmit Destination Threshold Clear Low Register (Pn_TX_DEST_THRESH_CLR_L) Field Descriptions

Bits	Field	Description
31-29	Reserved	Reserved
28-24	THRESH_CLR3	Port Priority Based Flow Control Threshold Clear Value for Priority 3.
23-21	Reserved	Reserved
20-16	THRESH_CLR2	Port Priority Based Flow Control Threshold Clear Value for Priority 2.
15-13	Reserved	Reserved
12-8	THRESH_CLR1	Port Priority Based Flow Control Threshold Clear Value for Priority 1.
7-5	Reserved	Reserved
4-0	THRESH_CLR0	Port Priority Based Flow Control Threshold Clear Value for Priority 0.

3.5.2.36 Port n Transmit Destination Threshold Clear High Register (Pn_TX_DEST_THRESH_CLR_H)

The Port n Transmit Destination Threshold Clear High Register is shown in Figure 3-85 and described in Table 3-98.

Figure 3-85. Port n Transmit Destination Threshold Clear High Register (Pn_TX_DEST_THRESH_CLR_H)

31 29	28 24	23 21	20 16	15 13	12 8	7 5	4 0
Reserved	THRESH_CLR7	Reserved	THRESH_CLR6	Reserved	THRESH_CLR5	Reserved	THRESH_CLR4
R-0h	R/W-0h	R-0h	R/W-0h	R-0h	R/W-0h	R-0h	R/W-0h

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-98. Port n Transmit Destination Threshold Clear High Register (Pn_TX_DEST_THRESH_CLR_H) Field Descriptions

Bits	Field	Description
31-29	Reserved	Reserved
28-24	THRESH_CLR7	Port Priority Based Flow Control Threshold Clear Value for Priority 7.
23-21	Reserved	Reserved
20-16	THRESH_CLR6	Port Priority Based Flow Control Threshold Clear Value for Priority 6.
15-13	Reserved	Reserved
12-8	THRESH_CLR5	Port Priority Based Flow Control Threshold Clear Value for Priority 5.
7-5	Reserved	Reserved
4-0	THRESH_CLR4	Port Priority Based Flow Control Threshold Clear Value for Priority 4.

3.5.2.37 Port n Global Transmit Buffer Threshold Set Low Register (Pn_TX_BUFFER_THRESH_SET_L)

The Port n Global Transmit Buffer Threshold Set Low Register is shown in Figure 3-82 and described in Table 3-95.

Figure 3-86. Port n Global Transmit Buffer Threshold Set Low Register (Pn_TX_BUFFER_THRESH_SET_L)

31 29	28 24	23 21	20 16	15 13	12 8	7 5	4 0
Reserved	THRESH_SET3	Reserved	THRESH_SET2	Reserved	THRESH_SET1	Reserved	THRESH_SET0
R-0h	R/W-1Fh	R-0h	R/W-1Fh	R-0h	R/W-1Fh	R-0h	R/W-1Fh

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-99. Port n Global Transmit Buffer Threshold Set Low Register (Pn_TX_BUFFER_THRESH_SET_L) Field Descriptions

Bits	Field	Description
31-29	Reserved	Reserved
28-24	THRESH_SET3	Port Priority Based Flow Control Threshold Set Value for Priority 3.
23-21	Reserved	Reserved
20-16	THRESH_SET2	Port Priority Based Flow Control Threshold Set Value for Priority 2.
15-13	Reserved	Reserved
12-8	THRESH_SET1	Port Priority Based Flow Control Threshold Set Value for Priority 1.
7-5	Reserved	Reserved
4-0	THRESH_SET0	Port Priority Based Flow Control Threshold Set Value for Priority 0.

3.5.2.38 Port n Global Transmit Buffer Threshold Set High Register (Pn_TX_BUFFER_THRESH_SET_H)

The Port n Global Transmit Buffer Threshold Set High Register is shown in Figure 3-87 and described in Table 3-100.

Figure 3-87. Port n Global Transmit Buffer Threshold Set High Register (Pn_TX_BUFFER_THRESH_SET_H)

31 29	28 24	23 21	20 16	15 13	12 8	7 5	4 0
Reserved	THRESH_SET7	Reserved	THRESH_SET6	Reserved	THRESH_SET5	Reserved	THRESH_SET4
R-0h	R/W-1Fh	R-0h	R/W-1Fh	R-0h	R/W-1Fh	R-0h	R/W-1Fh

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-100. Port n Global Transmit Buffer Threshold Set High Register (Pn_TX_BUFFER_THRESH_SET_H) Field Descriptions

Bits	Field	Description
31-29	Reserved	Reserved
28-24	THRESH_SET7	Port Priority Based Flow Control Threshold Set Value for Priority 7.
23-21	Reserved	Reserved
20-16	THRESH_SET6	Port Priority Based Flow Control Threshold Set Value for Priority 6.
15-13	Reserved	Reserved
12-8	THRESH_SET5	Port Priority Based Flow Control Threshold Set Value for Priority 5.
7-5	Reserved	Reserved
4-0	THRESH_SET4	Port Priority Based Flow Control Threshold Set Value for Priority 4.

3.5.2.39 Port n Global Transmit Buffer Threshold Clear Low Register (Pn_TX_BUFFER_THRESH_CLR_L)

The Port n Global Transmit Buffer Threshold Clear Low Register is shown in Figure 3-88 and described in Table 3-101.

Figure 3-88. Port n Global Transmit Buffer Threshold Clear Low Register (Pn_TX_BUFFER_THRESH_CLR_L)

31–29	28–24	23–21	20–16	15–13	12–8	7–5	4–0
Reserved	THRESH_CLR3	Reserved	THRESH_CLR2	Reserved	THRESH_CLR1	Reserved	THRESH_CLR0
R-0h	R/W-0h	R-0h	R/W-0h	R-0h	R/W-0h	R-0h	R/W-0h

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-101. Port n Global Transmit Buffer Threshold Clear Low Register (Pn_TX_BUFFER_THRESH_CLR_L) Field Descriptions

Bits	Field	Description
31-29	Reserved	Reserved
28-24	THRESH_CLR3	Port Priority Based Flow Control Threshold Clear Value for Priority 3.
23-21	Reserved	Reserved
20-16	THRESH_CLR2	Port Priority Based Flow Control Threshold Clear Value for Priority 2.
15-13	Reserved	Reserved
12-8	THRESH_CLR1	Port Priority Based Flow Control Threshold Clear Value for Priority 1.
7-5	Reserved	Reserved
4-0	THRESH_CLR0	Port Priority Based Flow Control Threshold Clear Value for Priority 0.

3.5.2.40 Port n Global Transmit Buffer Destination Threshold Clear High Register (Pn_TX_BUFFER_THRESH_CLR_H)

The Port n Global Transmit Buffer Threshold Clear High Register is shown in Figure 3-89 and described in Table 3-102.

Figure 3-89. Port n Global Transmit Buffer Threshold Clear High Register (Pn_TX_BUFFER_THRESH_CLR_H)

31 29	28 24	23 21	20 16	15 13	12 8	7 5	4 0
Reserved	THRESH_CLR7	Reserved	THRESH_CLR6	Reserved	THRESH_CLR5	Reserved	THRESH_CLR4
R-0h	R/W-0h	R-0h	R/W-0h	R-0h	R/W-0h	R-0h	R/W-0h

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-102. Port n Global Transmit Buffer Threshold Clear High Register (Pn_TX_BUFFER_THRESH_CLR_H) Field Descriptions

Bits	Field	Description
31-29	Reserved	Reserved
28-24	THRESH_CLR7	Port Priority Based Flow Control Threshold Clear Value for Priority 7.
23-21	Reserved	Reserved
20-16	THRESH_CLR6	Port Priority Based Flow Control Threshold Clear Value for Priority 6.
15-13	Reserved	Reserved
12-8	THRESH_CLR5	Port Priority Based Flow Control Threshold Clear Value for Priority 5.
7-5	Reserved	Reserved
4-0	THRESH_CLR4	Port Priority Based Flow Control Threshold Clear Value for Priority 4.

3.5.2.41 Host Port 0 Source ID A Register (P0_SRC_ID_A)

The Host Port 0 Source ID A Register is shown in Figure 3-90 and described in Table 3-103.

Figure 3-90. Host Port 0 Source ID A Register (P0_SRC_ID_A)

31 24	23 16	15 8	7 0
P4_SRC_ID	P3_SRC_ID	P2_SRC_ID	P1_SRC_ID
R/W-4h	R/W-3h	R/W-2h	R/W-1h

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-103. Host Port 0 Source ID A Register (P0_SRC_ID_A) Field Descriptions

Bits	Field	Description
31-24	P4_SRC_ID	Port 4 CPPI Info Word0 Source ID Value. This value is contained in the CPPI Info Word 0 SRC_ID field for packets received on Ethernet port 4.
23-16	P3_SRC_ID	Port 3 CPPI Info Word0 Source ID Value. This value is contained in the CPPI Info Word 0 SRC_ID field for packets received on Ethernet port 3.
15-8	P2_SRC_ID	Port 2 CPPI Info Word0 Source ID Value. This value is contained in the CPPI Info Word 0 SRC_ID field for packets received on Ethernet port 2.
7-0	P1_SRC_ID	Port 1 CPPI Info Word0 Source ID Value. This value is contained in the CPPI Info Word 0 SRC_ID field for packets received on Ethernet port 1.

3.5.2.42 Host Port 0 Source ID B Register (P0_SRC_ID_B)

The Host Port 0 Source ID B Register is shown in Figure 3-91 and described in Table 3-104.

Figure 3-91. Host Port 0 Source ID B Register (P0_SRC_ID_B)

31 24	23 16	15 8	7 0
P8_SRC_ID	P7_SRC_ID	P6_SRC_ID	P5_SRC_ID
R/W-8h	R/W-7h	R/W-6h	R/W-5h

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-104. Host Port 0 Source ID A Register (P0_SRC_ID_A) Field Descriptions

Bits	Field	Description
31-24	P8_SRC_ID	Port 8 CPPI Info Word0 Source ID Value. This value is contained in the CPPI Info Word 0 SRC_ID field for packets received on Ethernet port 8.
23-16	P7_SRC_ID	Port 7 CPPI Info Word0 Source ID Value. This value is contained in the CPPI Info Word 0 SRC_ID field for packets received on Ethernet port 7.
15-8	P6_SRC_ID	Port 6 CPPI Info Word0 Source ID Value. This value is contained in the CPPI Info Word 0 SRC_ID field for packets received on Ethernet port 6.
7-0	P5_SRC_ID	Port 5 CPPI Info Word0 Source ID Value. This value is contained in the CPPI Info Word 0 SRC_ID field for packets received on Ethernet port 5.

3.5.2.43 Host Port 0 Host Blocks Priority Register (P0_HOST_BLKS_PRI)

The Host Port 0 Host Blocks Priority Register is shown in Figure 3-92 and described in Table 3-105.

Figure 3-92. Host Port 0 Host Blocks Priority Register (P0_HOST_BLKS_PRI)

31 28	27 24	23 20	19 16	15 12	11 8	7 4	3 0
HST_BLKS_PRI7	HST_BLKS_PRI6	HST_BLKS_PRI5	HST_BLKS_PRI4	HST_BLKS_PRI3	HST_BLKS_PRI2	HST_BLKS_PRI1	HST_BLKS_PRI0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-105. Host Port 0 Host Blocks Priority Register (P0_HOST_BLKS_PRI) Field Descriptions

Bits	Field	Description
31-28	HST_BLKS_PRI7	Host Blocks Per Priority 7.
27-24	HST_BLKS_PRI6	Host Blocks Per Priority 6.
23-20	HST_BLKS_PRI5	Host Blocks Per Priority 5.
19-16	HST_BLKS_PRI4	Host Blocks Per Priority 4.
15-12	HST_BLKS_PRI3	Host Blocks Per Priority 3.
11-8	HST_BLKS_PRI2	Host Blocks Per Priority 2.
7-4	HST_BLKS_PRI1	Host Blocks Per Priority 1.
3-0	HST_BLKS_PRI0	Host Blocks Per Priority 0.

3.5.2.44 Ethernet Port n Transmit Destination Out Flow Add Values Low Register (Pn_TX_DEST_OUTFLOW_ADDVAL_L)

The Ethernet Port n Transmit Destination Out Flow Add Values Low Register is shown in Figure 3-93 and described in Table 3-106.

Figure 3-93. Ethernet Port n Transmit Destination Out Flow Add Values Low Register (Pn_TX_DEST_OUTFLOW_ADDVAL_L)

31 29	28 24	23 21	20 16	15 13	12 8	7 5	4 0
Reserved	ADD_VAL_3	Reserved	ADD_VAL_2	Reserved	ADD_VAL_1	Reserved	ADD_VAL_0
R-0h	R/W-0h	R-0h	R/W-0h	R-0h	R/W-0h	R-0h	R/W-0h

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-106. Ethernet Port n Transmit Destination Out Flow Add Values Low Register (Pn_TX_DEST_OUTFLOW_ADDVAL_L) Field Descriptions

Bits	Field	Description
31-29	Reserved	Reserved
28-24	ADD_VAL_3	Port PFC Destination Based Out Flow Add Value for Priority 3 (Decimal 11 is the maximum value for ADD_VAL_3).
23-21	Reserved	Reserved
20-16	ADD_VAL_2	Port PFC Destination Based Out Flow Add Value for Priority 2 (Decimal 11 is the maximum value for ADD_VAL_2).
15-13	Reserved	Reserved
12-8	ADD_VAL_1	Port PFC Destination Based Out Flow Add Value for Priority 1 (Decimal 11 is the maximum value for ADD_VAL_1).
7-5	Reserved	Reserved
4-0	ADD_VAL_0	Port PFC Destination Based Out Flow Add Value for Priority 0 (Decimal 11 is the maximum value for ADD_VAL_0).

3.5.2.45 Ethernet Port n Transmit Destination Out Flow Add Values High Register (Pn_TX_DEST_OUTFLOW_ADDVAL_H)

The Ethernet Port n Transmit Destination Out Flow Add Values High Register is shown in Figure 3-94 and described in Table 3-107.

Figure 3-94. Ethernet Port n Transmit Destination Out Flow Add Values High Register (Pn_TX_DEST_OUTFLOW_ADDVAL_H)

31 29	28 24	23 21	20 16	15 13	12 8	7 5	4 0
Reserved	ADD_VAL_7	Reserved	ADD_VAL_6	Reserved	ADD_VAL_5	Reserved	ADD_VAL_4
R-0h	R/W-0h	R-0h	R/W-0h	R-0h	R/W-0h	R-0h	R/W-0h

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-107. Ethernet Port n Transmit Destination Out Flow Add Values High Register (Pn_TX_DEST_OUTFLOW_ADDVAL_H) Field Descriptions

Bits	Field	Description
31-29	Reserved	Reserved
28-24	ADD_VAL_7	Port PFC Destination Based Out Flow Add Value for Priority 7 (Decimal 11 is the maximum value for ADD_VAL_7).
23-21	Reserved	Reserved
20-16	ADD_VAL_6	Port PFC Destination Based Out Flow Add Value for Priority 6 (Decimal 11 is the maximum value for ADD_VAL_6).
15-13	Reserved	Reserved
12-8	ADD_VAL_5	Port PFC Destination Based Out Flow Add Value for Priority 5 (Decimal 11 is the maximum value for ADD_VAL_5).
7-5	Reserved	Reserved
4-0	ADD_VAL_4	Port PFC Destination Based Out Flow Add Value for Priority 4 (Decimal 11 is the maximum value for ADD_VAL_4).

3.5.2.46 Ethernet Port n Pause Frame Source Address Low Register (Pn_PAUSE_SA_L)

The Ethernet Port n Pause Frame Source Address Low Register is shown in Figure 3-95 and described in Table 3-108.

Figure 3-95. Ethernet Port n Pause Frame Source Address Low Register (Pn_PAUSE_SA_L)

31 16	15 8	7 0
Reserved	MAC_SRC_ADDR_7_0	MAC_SRC_ADDR_15_8
R-0h	R/W-0h	R/W-0h

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-108. Ethernet Port n Pause Frame Source Address Low Register (Pn_PAUSE_SA_L) Field Descriptions

Bits	Field	Description
31-16	Reserved	Reserved
15-8	MAC_SRC_ADDR_7_0	Ethernet Port Source Address Bits 7 down to 0 (byte 0). This source address is only used for transmit pause frames.
7-0	MAC_SRC_ADDR_15_8	Ethernet Port Source Address Bits 15 down to 8 (byte 1). This source address is only used for transmit pause frames.

3.5.2.47 Ethernet Port n Pause Frame Source Address High Register (Pn_PAUSE_SA_H)

The Ethernet Port n Pause Frame Source Address High Register is shown in Figure 3-96 and described in Table 3-109.

Figure 3-96. Ethernet Port n Pause Frame Source Address High Register (Pn_PAUSE_SA_H)

31 24	23 16	15 8	7 0
MAC_SRC_ADDR_23_16	MAC_SRC_ADDR_31_24	MAC_SRC_ADDR_39_32	MAC_SRC_ADDR_47_40
R/W-0h	R/W-0h	R/W-0h	R/W-0h

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-109. Ethernet Port n Pause Frame Source Address High Register (Pn_PAUSE_SA_H) Field Descriptions

Bits	Field	Description
31-24	MAC_SRC_ADDR_23_16	Ethernet Port Source Address Bits 23 down to 16 (byte 2). This source address is only used for transmit pause frames.
23-16	MAC_SRC_ADDR_31_24	Ethernet Port Source Address Bits 31 down to 24 (byte 3). This source address is only used for transmit pause frames.
15-8	MAC_SRC_ADDR_39_32	Ethernet Port Source Address Bits 39 down to 32 (byte 4). This source address is only used for transmit pause frames.
7-0	MAC_SRC_ADDR_47_40	Ethernet Port Source Address Bits 47 down to 40 (byte 5). This source address is only used for transmit pause frames.

3.5.2.48 Ethernet Port n Time Sync Control Register (Pn_TS_CTL)

The Ethernet Port n Time Sync Control Register is shown in Figure 3-97 and described in Table 3-110.

Figure 3-97. Ethernet Port n Time Sync Control Register (Pn_TS_CTL)

31	16	15	12	11	10	9	8
MSG_TYPE_EN		Reserved		TX_HOST_TS_EN	TX_ANNEXE_EN	RX_ANNEXE_EN	LTYPE2_EN
R/W-0h		R-0h		R/W-0h	R/W-0h	R/W-0h	R/W-0h

7	6	5	4	3	2	1	0
TX_ANNEXD_EN	TX_VLN_LT2_EN	TX_VLN_LT1_EN	TX_ANNEXF_EN	RX_ANNEXD_EN	RX_VLN_LT2_EN	RX_VLN_LT1_EN	RX_ANNEXF_EN
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-110. Ethernet Port n Time Sync Control Register (Pn_TS_CTL) Field Descriptions

Bits	Field	Description
31-16	MSG_TYPE_EN	Time Sync Message Type Enable. Each bit in this field enables the corresponding message type in receive and transmit time sync messages (Bit 0 enables message type 0, etc.).
15-12	Reserved	Reserved
11	TX_HOST_TS_EN	Time Sync Transmit Host Time Stamp Enable.
10	TX_ANNEXE_EN	Time Sync Transmit Annex E Enable.
9	RX_ANNEXE_EN	Time Sync Receive Annex E Enable.
8	LTYPE2_EN	Time Sync LTYPE 2 Enable (transmit and receive).
7	TX_ANNEXD_EN	Time Sync Transmit Annex D Enable.
6	TX_VLN_LT2_EN	Time Sync Transmit VLAN LTYPE2 Enable.
5	TX_VLN_LT1_EN	Time Sync Transmit VLAN LTYPE1 Enable.
4	TX_ANNEXF_EN	Time Sync Transmit Annex F Enable.
3	RX_ANNEXD_EN	Time Sync Receive Annex D Enable.
2	RX_VLN_LT2_EN	Time Sync Receive VLAN LTYPE2 Enable.
1	RX_VLN_LT1_EN	Time Sync Receive VLAN LTYPE1 Enable.
0	RX_ANNEXF_EN	Time Sync Receive Annex F Enable.

3.5.2.49 Ethernet Port n Time Sync LTYPE and SEQ_ID_OFFSET Register (Pn_TS_SEQ_LTYPE)

The Ethernet Port n Time Sync LTYPE and SEQ_ID_OFFSET Register is shown in Figure 3-98 and described in Table 3-111.

Figure 3-98. Ethernet Port n Time Sync LTYPE and SEQ_ID_OFFSET Register (Pn_TS_SEQ_LTYPE)

31 22	21 16	15 0
Reserved	TS_SEQ_ID_OFFSET	TS_LTYPE1
R-0h	R/W-1Eh	R/W-0h

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-111. Ethernet Port n Time Sync LTYPE and SEQ_ID_OFFSET Register (Pn_TS_SEQ_LTYPE) Field Descriptions

Bits	Field	Description
31-22	Reserved	Reserved
21-16	TS_SEQ_ID_OFFSET	Time Sync Sequence ID Offset. This is the number of octets that the sequence ID is offset in the TX and RX time sync message header. The minimum value is 6.
15-0	TS_LTYPE1	Time Sync LTYPE1. This is the port's time sync LTYPE1 value.

3.5.2.50 Ethernet Port n Time Sync VLAN LTYPE1 and VLAN LTYPE2 Register (Pn_TS_VLAN)

The Ethernet Port n Time Sync VLAN LTYPE1 and VLAN LTYPE2 Register is shown in Figure 3-99 and described in Table 3-112.

Figure 3-99. Ethernet Port n Time Sync VLAN LTYPE1 and VLAN LTYPE 2 Register (Pn_TS_VLAN)

31	16	15	0
TS_VLAN_LTYPE2		TS_VLAN_LTYPE1	
R/W-8100h		R/W-8100h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-112. Ethernet Port n Time Sync VLAN LTYPE1 and VLAN LTYPE2 Register (Pn_TS_VLAN) Field Descriptions

Bits	Field	Description
31-16	TS_VLAN_LTYPE2	Time Sync VLAN LTYPE2. This VLAN LTYPE value is used for the port TX and RX time sync decode.
15-0	TS_VLAN_LTYPE1	Time Sync VLAN LTYPE1. This VLAN LTYPE value is used for the port TX and RX time sync decode.

3.5.2.51 Ethernet Port n Time Sync Control and LTYPE2 Register (Pn_TS_CTL_LTYPE2)

The Ethernet Port n Time Sync Control and LTYPE2 Register is shown in Figure 3-100 and described in Table 3-113.

Figure 3-100. Ethernet Port n Time Sync Control and LTYPE2 Register (Pn_TS_CTL_LTYPE2)

31	25	24	23	22	21	20	19	18	17	16
Reserved		TS_UNI_EN	TS_TTL_NONZERO_EN	TS_320	TS_319	TS_132	TS_131	TS_130	TS_129	TS_107
R-0h		R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

15	0
TS_LTYPE2	
R/W-0h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-113. Ethernet Port n Time Sync Control and LTYPE2 Register (Pn_TS_CTL_LTYPE2) Field Descriptions

Bits	Field	Description
31-25	Reserved	Reserved
24	TS_UNI_EN	Time Sync Unicast Enable. • 0 = Unicast disabled • 1 = Unicast enabled
23	TS_TTL_NONZERO_EN	Time Sync Time to Live Non-zero Enable. • 0 = TTL must be zero • 1 = TTL may be non-zero
22	TS_320	Time Sync Destination Port Number 320 Enable. • 0 = Disabled • 1 = Destination port number 320 (decimal) is enabled
21	TS_319	Time Sync Destination Port Number 319 Enable. • 0 = Disabled • 1 = Destination port number 319 (decimal) is enabled
20	TS_132	Time Sync Destination IP Address 132 Enable. • 0 = Disabled • 1 = Destination IP address 224.0.1.132 is enabled
19	TS_131	Time Sync Destination IP Address 131 Enable. • 0 = Disabled • 1 = Destination IP address 224.0.1.131 is enabled
18	TS_130	Time Sync Destination IP Address 130 Enable. • 0 = Disabled • 1 = Destination IP address 224.0.1.130 is enabled
17	TS_129	Time Sync Destination IP Address 129 Enable. • 0 = Disabled • 1 = Destination IP address 224.0.1.129 is enabled
16	TS_107	Time Sync Destination IP Address 107 Enable. • 0 = Disabled • 1 = Destination IP address 224.0.1.107 is enabled
15-0	TS_LTYPE2	Time Sync LTYPE2. This is the time sync LTYPE2 value for this port.

3.5.2.52 Ethernet Port n Time Sync Control 2 Register (Pn_TS_CTL2)

The Ethernet Port n Time Sync Control 2 Register is shown in Figure 3-101 and described in Table 3-114.

Figure 3-101. Ethernet Port n Time Sync Control 2 Register (Pn_TS_CTL2)

31	22	21	16	15	0
Reserved		DOMAIN_OFFSET		TS_MCAST_TYPE_EN	
R-0h		R/W-4h		R/W-0h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-114. Ethernet Port n Time Sync Control 2 Register (Pn_TS_CTL2) Field Descriptions

Bits	Field	Description
31-22	Reserved	Reserved
21-16	DOMAIN_OFFSET	Domain Offset Value.
15-0	TS_MCAST_TYPE_EN	Multicast Type Enable.

3.5.2.53 Ethernet Port n MAC Control Register (Pn_MAC_CTL)

The Ethernet Port n MAC Control Register is shown in Figure 3-102 and described in Table 3-115.

Figure 3-102. Ethernet Port n MAC Control Register (Pn_MAC_CTL)

31							25	24
Reserved								RX_CMF_EN
R-0h								R/W-0h
23	22	21	20	19	18	17		16
RX_CSF_EN	RX_CEF_EN	TX_SG_LIM_EN	EXT_EN_TXv_FLO	EXT_EN_RX_FLO	EXT_EN	GIG_FORCE		IFCTL_B
R/W-0h	R/W-0h				R/W-0h	R/W-0h		R/W-0h
15	14		13	12	11	10	9	8
IFCTL_A	Reserved			CRC_TYPE	CMD_IDLE	TX_SHORT_GAP_EN	Reserved	
R/W-0h	R-0h			R/W-0h	R/W-0h	R/W-0h	R-0h	
7	6	5	4	3	2	1		0
GIG	TX_PACE	GMII_EN	TX_FLOW_EN	RX_FLOW_EN	MTEST	LOOPBACK		FULLDUPLEX
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h		R/W-0h

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-115. Ethernet Port n MAC Control Register (Pn_MAC_CTL) Field Descriptions

Bits	Field	Description
31-25	Reserved	Reserved
24	RX_CMF_EN	Receive Copy MAC Control Frames Enable. Enables MAC control frames to be transferred to memory. MAC control frames are normally acted upon (if enabled), but not copied to memory. MAC control frames that are pause frames will be acted upon if enabled in the Pn_MAC_CTL register, regardless of the value of RX_CMF_EN. Frames transferred to memory due to RX_CMF_EN will have the CONTROL bit set in their EOP buffer descriptor. • 0 = MAC control frames are filtered (but acted upon if enabled). • 1 = MAC control frames are transferred to memory.
23	RX_CSF_EN	RX Copy Short Frames Enable – Enables frames or fragments shorter than 64 bytes to be copied to memory. Frames transferred to memory due to RX_CSF_EN will have the FRAGMENT or UNDERSIZED bit set in their receive footer. Fragments are short frames that contain CRC/align/code errors and undersized are short frames without errors. • 0 = Short frames are filtered. • 1 = Short frames are transferred to memory.
22	RX_CEF_EN	RX Copy Error Frames Enable – Enables frames containing errors to be transferred to memory. The appropriate error bit will be set in the frame receive footer. Frames containing errors will be filtered when RX_CEF_EN is not set. • 0 = Frames containing errors are filtered. • 1 = Frames containing errors are transferred to memory.
21	TX_SG_LIM_EN	Transmit Short Gap Limit Enable. When set this bit limits the number of short gap packets transmitted to 100ppm. Each time a short gap packet is sent, a counter is loaded with10,000 and decremented on each wire side clock. Another short gap packet will not be sent out until the counter decrements to zero. This mode is included to preclude the host from filling up the FIFO and sending every packet out with short gap which would violate the maximum number of packets per second allowed.
20	EXT_EN_TX_FLO	External Transmit Flow Control Enable. Enables the TX_FLOW_EN to be selected from the EXT_TX_FLOW_EN input signal and not from the TX_FLOW_EN bit in this register.
19	EXT_EN_RX_FLO	External Receive Flow Control Enable. Enables the RX_FLOW_EN to be selected from the EXT_RX_FLOW_EN input signal and not from the RX_FLOW_EN bit in this register.
18	EXT_EN	External Control Enable. Enables the fullduplex and gigabit mode to be selected from the FULLDUPLEX_IN and GIG_IN input signals and not from the FULLDUPLEX and GIG bits in this register. The FULLDUPLEX_MODE bit reflects the actual fullduplex mode selected.
17	GIG_FORCE	Gigabit Mode Force. This bit is used to force the Ethernet MAC into gigabit mode if the input GMII_MTCLK has been stopped by the PHY.
16	IFCTL_B	Interface Control B. Intended as a general purpose output bit to be used to control external gaskets associated with the GMII (GMII to RGMII etc.).

Table 3-115. Ethernet Port n MAC Control Register (Pn_MAC_CTL) Field Descriptions (continued)

Bits	Field	Description
15	IFCTL_A	Interface Control A. Intended as a general purpose output bit to be used to control external gaskets associated with the GMII (GMII to RGMII etc.).
14-13	Reserved	Reserved
12	CRC_TYPE	Port CRC Type. • 0 = Ethernet CRC • 1 = Castagnoli CRC
11	CMD_IDLE	Command Idle. • 0 = Idle not commanded. • 1 = Idle Commanded (read IDLE in Pn_MAC_STATUS).
10	TX_SHORT_GAP_EN	Transmit Short Gap Enable. • 0 = Transmit with a short IPG is disabled. • 1 = Transmit with a short IPG (when TX_SHORT_GAP input is asserted) is enabled.
9-8	Reserved	Reserved
7	GIG	Gigabit Mode. The GIG_OUT output is the value of this bit. • 0 = 10/100 mode. • 1 = Gigabit mode (full duplex only).
6	TX_PACE	Transmit Pacing Enable. • 0 = Transmit Pacing Disabled. • 1 = Transmit Pacing Enabled.
5	GMII_EN	• GMII Enable. • 0 = GMII receive and transmit held in reset. • 1 = GMII receive and transmit released from reset.
4	TX_FLOW_EN	Transmit Flow Control Enable. Determines if incoming pause frames are acted upon in full-duplex mode. Incoming pause frames are not acted upon in half-duplex mode regardless of this bit setting. The RX_MBP_ENABLE bits determine whether or not received pause frames are transferred to memory. • 0 = Transmit Flow Control Disabled. • Full-duplex mode – Incoming pause frames are not acted upon. • 1 = Transmit Flow Control Enabled. • Full-duplex mode – Incoming pause frames are acted upon.
3	RX_FLOW_EN	Receive Flow Control Enable. • 0 = Receive Flow Control Disabled • Half-duplex mode – No flow control generated collisions are sent. • Full-duplex mode – No outgoing pause frames are sent. • 1 = Receive Flow Control Enabled • Half-duplex mode – Collisions are initiated when receive flow control is triggered. • Full-duplex mode - Outgoing pause frames are sent when receive flow control is triggered.
2	MTEST	Manufacturing Test Mode. This bit must be set to allow writes to the backoff test (Pn_MAC_BACKOFF_TEST) and pause timer (Pn_MAC_xxx_PAUSETIMER) registers.
1	LOOPBACK	Loop Back Mode. Loopback mode forces internal fullduplex mode regardless of whether the FULLDUPLEX bit is set or not. The LOOPBACK bit should be changed only when GMII_EN is deasserted. • 0 = Not looped back. • 1 = Loop Back Mode enabled.
0	FULLDUPLEX	Full Duplex mode. Gigabit mode forces fullduplex mode regardless of whether the FULLDUPLEX bit is set or not. The FULLDUPLEX_OUT output is the value of this register bit. • 0 = half duplex mode. • 1 = full duplex mode.

3.5.2.54 Ethernet Port n MAC Status Register (Pn_MAC_STATUS)

The Ethernet Port n MAC Status Register is shown in Figure 3-103 and described in Table 3-116.

Figure 3-103. Ethernet Port n MAC Status Register (Pn_MAC_STATUS)

31	30 28	27	26 24	23 16	15 8
IDLE	Reserved	TORF	TORF_PRI	TX_PFC_FLOW_ACT	RX_PFC_FLOW_ACT
R-1h	R-0h	R/W-0h	R/W-0h	R-0h	R-0h

7	6	5	4	3	2	1	0
Reserved	EXT_TX_FLO_EN	EXT_RX_FLO_EN	EXT_GIG	EXT_FD	Reserved	RX_FLOW_ACT	TX_FLOW_ACT
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-116. Ethernet Port n MAC Status Register (Pn_MAC_STATUS) Field Descriptions

Bits	Field	Description
31	IDLE	Ethernet Idle. The Ethernet port is in the idle state (value after and idle command) • 0 = The port is not in the idle state • 1 = The port is in the idle state
31-27	Reserved	Reserved
27	TORF	Top of Receive FIFO Flow Control Trigger Occurred. This bit is write 1 to clear.
26-24	TORF_PRI	The lowest priority that caused top of receive FIFO flow control trigger since the last write to clear. This field is write 0x7 to clear.
23-16	TX_PFC_FLOW_ACT	Transmit Priority Based Flow Control Active (one bit per priority, 7 down to 0)
15-8	RX_PFC_FLOW_ACT	Receive Priority Based Flow Control Active (one bit per priority, 7 down to 0)
7	Reserved	Reserved
6	EXT_TX_FLO_EN	External Transmit Flow Control Enable. This is the value of the EXT_TX_FLOW_EN input bit.
5	EXT_RX_FLO_EN	External Receive Flow Control Enable. This is the value of the EXT_RX_FLOW_EN input bit.
4	EXT_GIG	External GIG. This is the value of the EXT_GIG input bit.
3	EXT_FD	External Fullduplex. This is the value of the EXT_FULLDUPLEX input bit.
2	Reserved	Reserved
1	RX_FLOW_ACT	Receive Flow Control Active. When asserted, indicates that receive flow control is enabled and triggered.
0	TX_FLOW_ACT	Transmit Flow Control Active. When asserted, this bit indicates that the pause time period is being observed for a received pause frame. No new transmissions will begin while this bit is asserted except for the transmission of pause frames. Any transmission in progress when this bit is asserted will complete.

3.5.2.55 Ethernet Port n MAC Soft Reset Register (Pn_MAC_SOFT_RESET)

The Ethernet Port n MAC Soft Reset Register is shown in Figure 3-104 and described in Table 3-117.

Figure 3-104. Ethernet Port n MAC Soft Reset Register (Pn_MAC_SOFT_RESET)

31	1	0
Reserved		SOFT_RESET
R-0h		R/W-0h

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-117. Ethernet Port n MAC Soft Reset Register (Pn_MAC_SOFT_RESET) Field Descriptions

Bits	Field	Description
31-1	Reserved	Reserved
0	SOFT_RESET	Software Reset. Writing a 1 to this bit causes the Ethernet MAC logic to be reset. After writing a 1 to this bit, it may be polled to determine if the reset has occurred. If a 1 is read, the reset has not yet occurred. If a 0 is read then reset has occurred.

3.5.2.56 Ethernet Port n MAC Backoff Test Register (Pn_MAC_BACKOFF_TEST)

The Ethernet Port n MAC Backoff Test Register is shown in Figure 3-105 and described in Table 3-118.

Figure 3-105. Ethernet Port n MAC Backoff Test Register (Pn_MAC_BACKOFF_TEST)

31	30 26	25 16	15 12	11 10	9 0
Reserved	PACEVAL	RNDNUM	COLL_COUNT	Reserved	TX_BACKOFF
R-0h	R/W-0h	R/W-0h	R-0h	R-0h	R-0h

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-118. Ethernet Port n MAC Backoff Test Register (Pn_MAC_BACKOFF_TEST) Field Descriptions

Bits	Field	Description
31	Reserved	Reserved
30-26	PACEVAL	Pacing Current Value. A non-zero value in this field indicates that transmit pacing is active. A transmit frame collision or deferral causes PACEVAL to loaded with decimal 31, good frame transmissions (with no collisions or deferrals) cause PACEVAL to be decremented down to zero. When PACEVAL is nonzero, the transmitter delays 4 IPGs between new frame transmissions after each successfully transmitted frame that had no deferrals or collisions. Transmit pacing helps reduce “capture” effects improving overall network bandwidth.
25-16	RNDNUM	Backoff Random Number Generator. This field allows the Backoff Random Number Generator to be read (or written in test mode only). This field can be written only when the MTEST bit in the Pn_MAC_CTL register has previously been set. Reading this field returns the generator’s current value. The value is reset to zero and begins counting on the clock after the de-assertion of reset.
15-12	COLL_COUNT	Collision Count – The number of collisions the current frame has experienced.
11-10	Reserved	Reserved
9-0	TX_BACKOFF	Backoff Count. This field allows the current value of the backoff counter to be observed for test purposes. This field is loaded automatically according to the backoff algorithm, and is decremented by one for each slot time after the collision.

3.5.2.57 Ethernet Port n 802.3 Receive Pause Timer Register (Pn_MAC_RX_PAUSETIMER)

The Ethernet Port n 802.3 Receive Pause Timer Register is shown in Figure 3-106 and described in Table 3-119.

Figure 3-106. Ethernet Port n 802.3 Receive Pause Timer Register (Pn_MAC_RX_PAUSETIMER)

31	16	15	0
Reserved		RX_PAUSETIMER	
R-0h		R/W-0h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-119. Ethernet Port n 802.3 Receive Pause Timer Register (Pn_MAC_RX_PAUSETIMER) Field Descriptions

Bits	Field	Description
31-16	Reserved	Reserved
15-0	RX_PAUSETIMER	RX Pause Timer Value. This field allows the contents of the receive Pause timer to be observed (and written in test mode). The receive pause timer is loaded with 0xFF00 when the Ethernet port sends an outgoing pause frame (with pause time of 0xFFFF). The receive pause timer is decremented at slot time intervals. If the receive pause timer decrements to zero, then another outgoing pause frame will be sent and the load/decrement process will be repeated. This register is for 802.3 Based flow control and is not used for 802.1qbb Priority Based Flow Control (PFC).

3.5.2.58 Ethernet Port n Priority Flow Control Priority 0 Receive Pause Timer Register (Pn_MAC_RX_PRI0_PAUSETIMER)

The Ethernet Port n Priority Flow Control Priority 0 Receive Pause Timer Register is shown in Figure 3-107 and described in Table 3-120.

Figure 3-107. Ethernet Port n Priority Flow Control Priority 0 Receive Pause Timer Register (Pn_MAC_RX_PRI0_PAUSETIMER)

31	16	15	0
Reserved		RX_PRI0_PAUSETIMER	
R-0h		R/W-0h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-120. Ethernet Port n Priority Flow Control Priority 0 Receive Pause Timer Register (Pn_MAC_RX_PRI0_PAUSETIMER) Field Descriptions

Bits	Field	Description
31-16	Reserved	Reserved
15-0	RX_PRI0_PAUSETIMER	RX Priority 0 Pause Timer Value. This field allows the contents of the receive pause timer to be observed (and written in test mode). The receive pause timer is loaded with 0xFF00 when the Ethernet port sends an outgoing pause frame (with pause time of 0xFFFF). The receive pause timer is decremented at slot time intervals. If the receive pause timer decrements to zero, then another outgoing pause frame will be sent and the load/decrement process will be repeated. This register is for 802.1qbb Priority Based flow control (PFC)

3.5.2.59 Ethernet Port n Priority Flow Control Priority 1 Receive Pause Timer Register (Pn_MAC_RX_PRI1_PAUSETIMER)

The Ethernet Port n Priority Flow Control Priority 1 Receive Pause Timer Register is shown in Figure 3-108 and described in Table 3-121.

Figure 3-108. Ethernet Port n Priority Flow Control Priority 1 Receive Pause Timer Register (Pn_MAC_RX_PRI1_PAUSETIMER)

31	16	15	0
Reserved		RX_PRI1_PAUSETIMER	
R-0h		R/W-0h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-121. Ethernet Port n Priority Flow Control Priority 1 Receive Pause Timer Register (Pn_MAC_RX_PRI1_PAUSETIMER) Field Descriptions

Bits	Field	Description
31-16	Reserved	Reserved
15-0	RX_PRI1_PAUSETIMER	RX Priority 1 Pause Timer Value. This field allows the contents of the receive pause timer to be observed (and written in test mode). The receive pause timer is loaded with 0xFF00 when the Ethernet port sends an outgoing pause frame (with pause time of 0xFFFF). The receive pause timer is decremented at slot time intervals. If the receive pause timer decrements to zero, then another outgoing pause frame will be sent and the load/decrement process will be repeated. This register is for 802.1qbb Priority Based flow control (PFC)

3.5.2.60 Ethernet Port n Priority Flow Control Priority 2 Receive Pause Timer Register (Pn_MAC_RX_PRI2_PAUSETIMER)

The Ethernet Port n Priority Flow Control Priority 2 Receive Pause Timer Register is shown in Figure 3-109 and described in Table 3-122.

Figure 3-109. Ethernet Port n Priority Flow Control Priority 2 Receive Pause Timer Register (Pn_MAC_RX_PRI2_PAUSETIMER)

31	16	15	0
Reserved		RX_PRI2_PAUSETIMER	
R-0h		R/W-0h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-122. Ethernet Port n Priority Flow Control Priority 2 Receive Pause Timer Register (Pn_MAC_RX_PRI2_PAUSETIMER) Field Descriptions

Bits	Field	Description
31-16	Reserved	Reserved
15-0	RX_PRI2_PAUSETIMER	RX Priority 2 Pause Timer Value. This field allows the contents of the receive pause timer to be observed (and written in test mode). The receive pause timer is loaded with 0xFF00 when the Ethernet port sends an outgoing pause frame (with pause time of 0xFFFF). The receive pause timer is decremented at slot time intervals. If the receive pause timer decrements to zero, then another outgoing pause frame will be sent and the load/decrement process will be repeated. This register is for 802.1qbb Priority Based flow control (PFC)

3.5.2.61 Ethernet Port n Priority Flow Control Priority 3 Receive Pause Timer Register (Pn_MAC_RX_PRI3_PAUSETIMER)

The Ethernet Port n Priority Flow Control Priority 3 Receive Pause Timer Register is shown in Figure 3-110 and described in Table 3-123.

Figure 3-110. Ethernet Port n Priority Flow Control Priority 3 Receive Pause Timer Register (Pn_MAC_RX_PRI3_PAUSETIMER)

31	16	15	0
Reserved		RX_PRI3_PAUSETIMER	
R-0h		R/W-0h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-123. Ethernet Port n Priority Flow Control Priority 3 Receive Pause Timer Register (Pn_MAC_RX_PRI3_PAUSETIMER) Field Descriptions

Bits	Field	Description
31-16	Reserved	Reserved
15-0	RX_PRI3_PAUSETIMER	RX Priority 3 Pause Timer Value. This field allows the contents of the receive pause timer to be observed (and written in test mode). The receive pause timer is loaded with 0xFF00 when the Ethernet port sends an outgoing pause frame (with pause time of 0xFFFF). The receive pause timer is decremented at slot time intervals. If the receive pause timer decrements to zero, then another outgoing pause frame will be sent and the load/decrement process will be repeated. This register is for 802.1qbb Priority Based flow control (PFC)

3.5.2.62 Ethernet Port n Priority Flow Control Priority 4 Receive Pause Timer Register (Pn_MAC_RX_PRI4_PAUSETIMER)

The Ethernet Port n Priority Flow Control Priority 4 Receive Pause Timer Register is shown in Figure 3-111 and described in Table 3-124.

Figure 3-111. Ethernet Port n Priority Flow Control Priority 4 Receive Pause Timer Register (Pn_MAC_RX_PRI4_PAUSETIMER)

31	16	15	0
Reserved		RX_PRI4_PAUSETIMER	
R-0h		R/W-0h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-124. Ethernet Port n Priority Flow Control Priority 4 Receive Pause Timer Register (Pn_MAC_RX_PRI4_PAUSETIMER) Field Descriptions

Bits	Field	Description
31-16	Reserved	Reserved
15-0	RX_PRI4_PAUSETIMER	RX Priority 4 Pause Timer Value. This field allows the contents of the receive pause timer to be observed (and written in test mode). The receive pause timer is loaded with 0xFF00 when the Ethernet port sends an outgoing pause frame (with pause time of 0xFFFF). The receive pause timer is decremented at slot time intervals. If the receive pause timer decrements to zero, then another outgoing pause frame will be sent and the load/decrement process will be repeated. This register is for 802.1qbb Priority Based flow control (PFC)

3.5.2.63 Ethernet Port n Priority Flow Control Priority 5 Receive Pause Timer Register (Pn_MAC_RX_PRI5_PAUSETIMER)

The Ethernet Port n Priority Flow Control Priority 5 Receive Pause Timer Register is shown in Figure 3-112 and described in Table 3-125.

Figure 3-112. Ethernet Port n Priority Flow Control Priority 5 Receive Pause Timer Register (Pn_MAC_RX_PRI5_PAUSETIMER)

31	16	15	0
Reserved		RX_PRI5_PAUSETIMER	
R-0h		R/W-0h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-125. Ethernet Port n Priority Flow Control Priority 5 Receive Pause Timer Register (Pn_MAC_RX_PRI5_PAUSETIMER) Field Descriptions

Bits	Field	Description
31-16	Reserved	Reserved
15-0	RX_PRI5_PAUSETIMER	RX Priority 5 Pause Timer Value. This field allows the contents of the receive pause timer to be observed (and written in test mode). The receive pause timer is loaded with 0xFF00 when the Ethernet port sends an outgoing pause frame (with pause time of 0xFFFF). The receive pause timer is decremented at slot time intervals. If the receive pause timer decrements to zero, then another outgoing pause frame will be sent and the load/decrement process will be repeated. This register is for 802.1qbb Priority Based flow control (PFC)

3.5.2.64 Ethernet Port n Priority Flow Control Priority 6 Receive Pause Timer Register (Pn_MAC_RX_PRI6_PAUSETIMER)

The Ethernet Port n Priority Flow Control Priority 6 Receive Pause Timer Register is shown in Figure 3-113 and described in Table 3-126.

Figure 3-113. Ethernet Port n Priority Flow Control Priority 6 Receive Pause Timer Register (Pn_MAC_RX_PRI6_PAUSETIMER)

31	16	15	0
Reserved		RX_PRI6_PAUSETIMER	
R-0h		R/W-0h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-126. Ethernet Port n Priority Flow Control Priority 6 Receive Pause Timer Register (Pn_MAC_RX_PRI6_PAUSETIMER) Field Descriptions

Bits	Field	Description
31-16	Reserved	Reserved
15-0	RX_PRI6_PAUSETIMER	RX Priority 6 Pause Timer Value. This field allows the contents of the receive pause timer to be observed (and written in test mode). The receive pause timer is loaded with 0xFF00 when the Ethernet port sends an outgoing pause frame (with pause time of 0xFFFF). The receive pause timer is decremented at slot time intervals. If the receive pause timer decrements to zero, then another outgoing pause frame will be sent and the load/decrement process will be repeated. This register is for 802.1qbb Priority Based flow control (PFC)

3.5.2.65 Ethernet Port n Priority Flow Control Priority 7 Receive Pause Timer Register (Pn_MAC_RX_PRI7_PAUSETIMER)

The Ethernet Port n Priority Flow Control Priority 7 Receive Pause Timer Register is shown in Figure 3-114 and described in Table 3-127.

Figure 3-114. Ethernet Port n Priority Flow Control Priority 7 Receive Pause Timer Register (Pn_MAC_RX_PRI7_PAUSETIMER)

31	16	15	0
Reserved		RX_PRI7_PAUSETIMER	
R-0h		R/W-0h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-127. Ethernet Port n Priority Flow Control Priority 7 Receive Pause Timer Register (Pn_MAC_RX_PRI7_PAUSETIMER) Field Descriptions

Bits	Field	Description
31-16	Reserved	Reserved
15-0	RX_PRI7_PAUSETIMER	RX Priority 7 Pause Timer Value. This field allows the contents of the receive pause timer to be observed (and written in test mode). The receive pause timer is loaded with 0xFF00 when the Ethernet port sends an outgoing pause frame (with pause time of 0xFFFF). The receive pause timer is decremented at slot time intervals. If the receive pause timer decrements to zero, then another outgoing pause frame will be sent and the load/decrement process will be repeated. This register is for 802.1qbb Priority Based flow control (PFC)

3.5.2.66 Ethernet Port n 802.3 Transmit Pause Timer Register (Pn_MAC_TX_PAUSETIMER)

The Ethernet Port n 802.3 Transmit Pause Timer Register is shown in Figure 3-115 and described in Table 3-128.

Figure 3-115. Ethernet Port n 802.3 Transmit Pause Timer Register (Pn_MAC_TX_PAUSETIMER)

31	16	15	0
Reserved		TX_PAUSETIMER	
R-0h		R/W-0h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-128. Ethernet Port n 802.3 Transmit Pause Timer Register (Pn_MAC_TX_PAUSETIMER) Field Descriptions

Bits	Field	Description
31-16	Reserved	Reserved
15-0	TX_PAUSETIMER	802.3 TX Pause Timer Value. This field allows the contents of the transmit Pause timer to be observed (and written in test mode). The transmit pause timer is loaded by a received (incoming) pause frame, and then decremented, at slottime intervals, down to zero at which time Ethernet Port transmit frames are again enabled. This register is for 802.3 Based flow control and is not used for 802.1qbb Priority Based Flow Control (PFC).

3.5.2.67 Ethernet Port n Priority Flow Control Priority 0 Transmit Pause Timer Register (Pn_MAC_TX_PRI0_PAUSETIMER)

The Ethernet Port n Priority Flow Control Priority 0 Transmit Pause Timer Register is shown in Figure 3-116 and described in Table 3-129.

Figure 3-116. Ethernet Port n Priority Flow Control Priority 0 Transmit Pause Timer Register (Pn_MAC_TX_PRI0_PAUSETIMER)

31	16	15	0
Reserved		TX_PRI0_PAUSETIMER	
R-0h		R/W-0h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-129. Ethernet Port n Priority Flow Control Priority 0 Transmit Pause Timer Register (Pn_MAC_TX_PRI0_PAUSETIMER) Field Descriptions

Bits	Field	Description
31-16	Reserved	Reserved
15-0	TX_PRI0_PAUSETIMER	PFC Transmit Priority 0 Pause Timer Value. This field allows the contents of the transmit pause timer to be observed (and written in test mode). The transmit pause timer is loaded by a received (incoming) pause frame, and then decremented, at slottime intervals, down to zero at which time Ethernet Port transmit frames are again enabled. This register is for 802.1qbb Priority Based flow control (PFC).

3.5.2.68 Ethernet Port n Priority Flow Control Priority 1 Transmit Pause Timer Register (Pn_MAC_TX_PRI1_PAUSETIMER)

The Ethernet Port n Priority Flow Control Priority 1 Transmit Pause Timer Register is shown in Figure 3-117 and described in Table 3-130.

Figure 3-117. Ethernet Port n Priority Flow Control Priority 1 Transmit Pause Timer Register (Pn_MAC_TX_PRI1_PAUSETIMER)

31	16	15	0
Reserved		TX_PRI1_PAUSETIMER	
R-0h		R/W-0h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-130. Ethernet Port n Priority Flow Control Priority 1 Transmit Pause Timer Register (Pn_MAC_TX_PRI1_PAUSETIMER) Field Descriptions

Bits	Field	Description
31-16	Reserved	Reserved
15-0	TX_PRI1_PAUSETIMER	PFC Transmit Priority 1 Pause Timer Value. This field allows the contents of the transmit pause timer to be observed (and written in test mode). The transmit pause timer is loaded by a received (incoming) pause frame, and then decremented, at slottime intervals, down to zero at which time Ethernet Port transmit frames are again enabled. This register is for 802.1qbb Priority Based flow control (PFC).

3.5.2.69 Ethernet Port n Priority Flow Control Priority 2 Transmit Pause Timer Register (Pn_MAC_TX_PRI2_PAUSETIMER)

The Ethernet Port n Priority Flow Control Priority 2 Transmit Pause Timer Register is shown in Figure 3-118 and described in Table 3-131.

Figure 3-118. Ethernet Port n Priority Flow Control Priority 2 Transmit Pause Timer Register (Pn_MAC_TX_PRI2_PAUSETIMER)

31	16	15	0
Reserved		TX_PRI2_PAUSETIMER	
R-0h		R/W-0h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-131. Ethernet Port n Priority Flow Control Priority 2 Transmit Pause Timer Register (Pn_MAC_TX_PRI2_PAUSETIMER) Field Descriptions

Bits	Field	Description
31-16	Reserved	Reserved
15-0	TX_PRI2_PAUSETIMER	PFC Transmit Priority 2 Pause Timer Value. This field allows the contents of the transmit pause timer to be observed (and written in test mode). The transmit pause timer is loaded by a received (incoming) pause frame, and then decremented, at slottime intervals, down to zero at which time Ethernet Port transmit frames are again enabled. This register is for 802.1qbb Priority Based flow control (PFC).

3.5.2.70 Ethernet Port n Priority Flow Control Priority 3 Transmit Pause Timer Register (Pn_MAC_TX_PRI3_PAUSETIMER)

The Ethernet Port n Priority Flow Control Priority 3 Transmit Pause Timer Register is shown in Figure 3-119 and described in Table 3-132.

Figure 3-119. Ethernet Port n Priority Flow Control Priority 3 Transmit Pause Timer Register (Pn_MAC_TX_PRI3_PAUSETIMER)

31	16	15	0
Reserved		TX_PRI3_PAUSETIMER	
R-0h		R/W-0h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-132. Ethernet Port n Priority Flow Control Priority 3 Transmit Pause Timer Register (Pn_MAC_TX_PRI3_PAUSETIMER) Field Descriptions

Bits	Field	Description
31-16	Reserved	Reserved
15-0	TX_PRI3_PAUSETIMER	PFC Transmit Priority 3 Pause Timer Value. This field allows the contents of the transmit pause timer to be observed (and written in test mode). The transmit pause timer is loaded by a received (incoming) pause frame, and then decremented, at slottime intervals, down to zero at which time Ethernet Port transmit frames are again enabled. This register is for 802.1qbb Priority Based flow control (PFC).

3.5.2.71 Ethernet Port n Priority Flow Control Priority 4 Transmit Pause Timer Register (Pn_MAC_TX_PRI4_PAUSETIMER)

The Ethernet Port n Priority Flow Control Priority 4 Transmit Pause Timer Register is shown in Figure 3-120 and described in Table 3-133.

Figure 3-120. Ethernet Port n Priority Flow Control Priority 4 Transmit Pause Timer Register (Pn_MAC_TX_PRI4_PAUSETIMER)

31	16	15	0
Reserved		TX_PRI4_PAUSETIMER	
R-0h		R/W-0h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-133. Ethernet Port n Priority Flow Control Priority 4 Transmit Pause Timer Register (Pn_MAC_TX_PRI4_PAUSETIMER) Field Descriptions

Bits	Field	Description
31-16	Reserved	Reserved
15-0	TX_PRI4_PAUSETIMER	PFC Transmit Priority 4 Pause Timer Value. This field allows the contents of the transmit pause timer to be observed (and written in test mode). The transmit pause timer is loaded by a received (incoming) pause frame, and then decremented, at slottime intervals, down to zero at which time Ethernet Port transmit frames are again enabled. This register is for 802.1qbb Priority Based flow control (PFC).

3.5.2.72 Ethernet Port n Priority Flow Control Priority 5 Transmit Pause Timer Register (Pn_MAC_TX_PRI5_PAUSETIMER)

The Ethernet Port n Priority Flow Control Priority 5 Transmit Pause Timer Register is shown in Figure 3-121 and described in Table 3-134.

Figure 3-121. Ethernet Port n Priority Flow Control Priority 5 Transmit Pause Timer Register (Pn_MAC_TX_PRI5_PAUSETIMER)

31	16	15	0
Reserved		TX_PRI5_PAUSETIMER	
R-0h		R/W-0h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-134. Ethernet Port n Priority Flow Control Priority 5 Transmit Pause Timer Register (Pn_MAC_TX_PRI5_PAUSETIMER) Field Descriptions

Bits	Field	Description
31-16	Reserved	Reserved
15-0	TX_PRI5_PAUSETIMER	PFC Transmit Priority 5 Pause Timer Value. This field allows the contents of the transmit pause timer to be observed (and written in test mode). The transmit pause timer is loaded by a received (incoming) pause frame, and then decremented, at slottime intervals, down to zero at which time Ethernet Port transmit frames are again enabled. This register is for 802.1qbb Priority Based flow control (PFC).

3.5.2.73 Ethernet Port n Priority Flow Control Priority 6 Transmit Pause Timer Register (Pn_MAC_TX_PRI6_PAUSETIMER)

The Ethernet Port n Priority Flow Control Priority 6 Transmit Pause Timer Register is shown in Figure 3-122 and described in Table 3-135.

Figure 3-122. Ethernet Port n Priority Flow Control Priority 6 Transmit Pause Timer Register (Pn_MAC_TX_PRI6_PAUSETIMER)

31	16	15	0
Reserved		TX_PRI6_PAUSETIMER	
R-0h		R/W-0h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-135. Ethernet Port n Priority Flow Control Priority 6 Transmit Pause Timer Register (Pn_MAC_TX_PRI6_PAUSETIMER) Field Descriptions

Bits	Field	Description
31-16	Reserved	Reserved
15-0	TX_PRI6_PAUSETIMER	PFC Transmit Priority 6 Pause Timer Value. This field allows the contents of the transmit pause timer to be observed (and written in test mode). The transmit pause timer is loaded by a received (incoming) pause frame, and then decremented, at slottime intervals, down to zero at which time Ethernet Port transmit frames are again enabled. This register is for 802.1qbb Priority Based flow control (PFC).

3.5.2.74 Ethernet Port n Priority Flow Control Priority 7 Transmit Pause Timer Register (Pn_MAC_TX_PRI7_PAUSETIMER)

The Ethernet Port n Priority Flow Control Priority 7 Transmit Pause Timer Register is shown in Figure 3-123 and described in Table 3-136.

Figure 3-123. Ethernet Port n Priority Flow Control Priority 7 Transmit Pause Timer Register (Pn_MAC_TX_PRI7_PAUSETIMER)

31	16	15	0
Reserved		TX_PRI7_PAUSETIMER	
R-0h		R/W-0h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-136. Ethernet Port n Priority Flow Control Priority 7 Transmit Pause Timer Register (Pn_MAC_TX_PRI7_PAUSETIMER) Field Descriptions

Bits	Field	Description
31-16	Reserved	Reserved
15-0	TX_PRI7_PAUSETIMER	PFC Transmit Priority 7 Pause Timer Value. This field allows the contents of the transmit pause timer to be observed (and written in test mode). The transmit pause timer is loaded by a received (incoming) pause frame, and then decremented, at slottime intervals, down to zero at which time Ethernet Port transmit frames are again enabled. This register is for 802.1qbb Priority Based flow control (PFC).

3.5.2.75 Ethernet Port n MAC Emulation Control Register (Pn_MAC_EMCONTROL)

The Ethernet Port n MAC Emulation Control Register is shown in Figure 3-124 and described in Table 3-137.

Figure 3-124. Ethernet Port n MAC Emulation Control Register (Pn_MAC_EMCONTROL)

31	2	1	0
Reserved		SOFT	FREE
R-0h		R/W-0h	R/W-0h

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-137. Ethernet Port n MAC Emulation Control Register (Pn_MAC_EMCONTROL) Field Descriptions

Bits	Field	Description
31-2	Reserved	Reserved
1	SOFT	Emulation Soft Bit
0	FREE	Emulation Free Bit

3.5.2.76 Ethernet Port n MAC Transmit Inter Packet Gap Register (Pn_MAC_TX_GAP)

The Ethernet Port n MAC Transmit Inter Packet Gap Register is shown in Figure 3-125 and described in Table 3-138.

Figure 3-125. Ethernet Port n MAC Transmit Inter Packet Gap Register (Pn_MAC_TX_GAP)

31	16	15	0
Reserved		TX_GAP	
R-0h		R/W-Ch	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-138. Ethernet Port n MAC Transmit Inter Packet Gap Register (Pn_MAC_TX_GAP) Field Descriptions

Bits	Field	Description
31-16	Reserved	Reserved
15-0	TX_GAP	Transmit Inter-Packet Gap. Decimal 12 is the default gap value and only bit 8 down to 0 are used. This can be increased from 12 to increase the gap between packets.

3.5.3 Statistics (STAT) Submodule

This section describes the registers available in the port statistics submodules. Each port has its own set of statistics registers so the definitions below will use the notation STATn_REGISTER_NAME where n = 0 to 4 in a 5 port switch and n = 0 to 8 in a 9 port switch.

A small subset of the statistics registers below will only apply to the external Ethernet ports of the switch and will not apply to the host port. When this is the case it will be mentioned in the register description that the statistic does not exist for the host port.

The register offset addresses listed in Table 3-139 are relative to the Ethernet switch module offset address. See Table 3-1 for the offset address of the Ethernet switch module. A complete list of all of the registers in the GbE switch subsystem is provided in Table 3-2.

Table 3-139 lists the registers in the Statistics (STATn) modules and the corresponding offset address for each register.

Table 3-139. Port Statistics Submodule Registers (n = 0-4 for a 5 port switch or n = 0-8 for a 9 port switch)

Offset Address[(1)]	Acronym	Description	Section
000h	STATn_RXGOODFRAMES	Total number of good frames received	Section 3.5.3.1
004h	STATn_RXBROADCASTFRAMES	Total number of good broadcast frames received	Section 3.5.3.2
008h	STATn_RXMULTICASTFRAMES	Total number of good multicast frames received	Section 3.5.3.3
00Ch	STATn_RXPAUSEFRAMES	Total number of pause frames received	Section 3.5.3.4
010h	STATn_RXCRCERRORS	Total number of CRC errors received	Section 3.5.3.5
014h	STATn_RXALIGNCODEERRORS	Total number of align/code errors received	Section 3.5.3.6
018h	STATn_RXOVERSIZEDFRAMES	Total number of oversized frames received	Section 3.5.3.7
01Ch	STATn_RXJABBERFRAMES	Total number of jabber frames received	Section 3.5.3.8
020h	STATn_RXUNDERSIZEDFRAMES	Total number of undersized frames received	Section 3.5.3.9
024h	STATn_RXFRAGMENTS	Total number of fragments received	Section 3.5.3.10
028h	STATn_ALE_DROP	Total number of frames dropped by the ALE	Section 3.5.3.11
02Ch	STATn_ALE_OVERRUN_DROP	Total number of frames dropped due to exceeding the maximum ALE lookup rate	Section 3.5.3.12
030h	STATn_RXOCTETS	Total number of received bytes in good frames	Section 3.5.3.13
034h	STATn_TXGOODFRAMES	Total number of good frames transmitted	Section 3.5.3.14
038h	STATn_TXBROADCASTFRAMES	Total number of good broadcast frames transmitted	Section 3.5.3.15
03Ch	STATn_TXMULTICASTFRAMES	Total number of good multicast frames transmitted	Section 3.5.3.16
040h	STATn_TXPAUSEFRAMES	Total number of pause transmit frames	Section 3.5.3.17
044h	STATn_TXDEFERREDFRAMES	Total number of deferred transmit frames	Section 3.5.3.18
048h	STATn_TXCOLLISIONFRAMES	Total number of collisions	Section 3.5.3.19

(1) The actual addresses of these registers are device specific. See your device-specific data manual to verify the register addresses.

Table 3-139. Port Statistics Submodule Registers (n = 0-4 for a 5 port switch or n = 0-8 for a 9 port switch) (continued)

Offset Address[(1)]	Acronym	Description	Section
04Ch	STATn_TXSINGLECOLLISIONFRAMES	Total number of single collision transmit frames	Section 3.5.3.20
050h	STATn_TXMULTCOLLISIONFRAMES	Total number of multiple collision transmit frames	Section 3.5.3.21
054h	STATn_TXEXCESSIVECOLLISIONFRAMES	Total number of excessive collision transmit frames	Section 3.5.3.22
058h	STATn_TXLATECOLLISIONFRAMES	Total number of late collisions	Section 3.5.3.23
05Ch	Reserved	Reserved	Reserved
060h	STATn_TXCARRIERSENSEERRORS	Total number of carrier sense errors	Section 3.5.3.24
064h	STATn_TXOCTETS	Total number of octets transmitted	Section 3.5.3.25
068h	STATn_64OCTETFRAMES	Total number of 64 octet frames transmitted and received on the port	Section 3.5.3.26
06Ch	STATn_65T127OCTETFRAMES	Total number of 65-127 octet frames transmitted and received on the port	Section 3.5.3.27
070h	STATn_128T255OCTETFRAMES	Total number of 128-255 octet frames transmitted and received on the port	Section 3.5.3.28
074h	STATn_256T511OCTETFRAMES	Total number of 256-511 octet frames transmitted and received on the port	Section 3.5.3.29
078h	STATn_512T1023OCTETFRAMES	Total number of 512-1023 octet frames transmitted and received on the port	Section 3.5.3.30
07Ch	STATn_1024TUPOCTETFRAMES	Total number of 1023-(P0_RX_MAXLEN) octet frames transmitted and received on the port	Section 3.5.3.31
080h	STATn_NETOCTETS	Total number of bytes of frame data received and transmitted on the port	Section 3.5.3.32
084h	STATn_RX_BOTTOM_FIFO_DROP	Total number of frames received at port 0 that were dropped because they overran the receive FIFO	Section 3.5.3.33
088h	STATn_PORTMASK_DROP	Total number of frames received at port 0 that were dropped by the ALE	Section 3.5.3.34
08Ch	STATn_RX_TOP_FIFO_DROP	Total number of frames received at port 0 that were dropped due to a start of frame (SOF) overrun on any destination port egress	Section 3.5.3.35
090h	STATn_ALE_RATE_LIMIT_DROP	Total number of frames that were dropped due to receive rate limiting on port 0 or transmit rate limiting on any destination port	Section 3.5.3.36
094h	STATn_ALE_VID_INGRESS_DROP	Total number of frames that were dropped due to VLAN ingress check failure	Section 3.5.3.37
098h	STATn_ALE_DA_EQ_SA_DROP	Total number of frames that were dropped due to destination address being the same as source address	Section 3.5.3.38
09Ch-0A4h	Reserved	Reserved	Reserved
0A8h	STATn_ALE_UNKN_UNI	Total number of frames received at port 0 that had a unicast destination address with an unknown source address	Section 3.5.3.39
0ACh	STATn_ALE_UNKN_UNI_BCNT	Total number of bytes contained in the frames that qualify for the P0_ALE_UNKN_UNI register	Section 3.5.3.40
0B0h	STATn_ALE_UNKN_MLT	Total number of frames received at port 0 that had a multicast destination address with an unknown source address	Section 3.5.3.41
0B4h	STATn_ALE_UNKN_MLT_BCNT	Total number of bytes contained in the frames that qualify for the P0_ALE_UNKN_MLT register	Section 3.5.3.42
0B8h	STATn_ALE_UNKN_BRD	Total number of frames received at port 0 that had a broadcast destination address with an unknown source address	Section 3.5.3.43
0BCh	STATn_ALE_UNKN_BRD_BCNT	Total number of bytes contained in the frames that qualify for the P0_ALE_UNKN_BRD register	Section 3.5.3.44

Table 3-139. Port Statistics Submodule Registers (n = 0-4 for a 5 port switch or n = 0-8 for a 9 port switch) (continued)

Offset Address[1]	Acronym	Description	Section
0C0h-178h	Reserved	Reserved	Reserved
17Ch	STATn_TX_MEM_PROTECT_ERROR	Total number of frames transmitted that had a memory protect CRC error on egress	Section 3.5.3.45
180h	STATn_TX_PRI0	Total number of packets transmitted with Priority 0	Section 3.5.3.46
184h	STATn_TX_PRI1	Total number of packets transmitted with Priority 1	Section 3.5.3.46
188h	STATn_TX_PRI2	Total number of packets transmitted with Priority 2	Section 3.5.3.46
18Ch	STATn_TX_PRI3	Total number of packets transmitted with Priority 3	Section 3.5.3.46
190h	STATn_TX_PRI4	Total number of packets transmitted with Priority 4	Section 3.5.3.46
194h	STATn_TX_PRI5	Total number of packets transmitted with Priority 5	Section 3.5.3.46
198h	STATn_TX_PRI6	Total number of packets transmitted with Priority 6	Section 3.5.3.46
19Ch	STATn_TX_PRI7	Total number of packets transmitted with Priority 7	Section 3.5.3.46
1A0h	STATn_TX_PRI0_BCNT	Total number of bytes transmitted with Priority 0	Section 3.5.3.47
1A4h	STATn_TX_PRI1_BCNT	Total number of bytes transmitted with Priority 1	Section 3.5.3.47
1A8h	STATn_TX_PRI2_BCNT	Total number of bytes transmitted with Priority 2	Section 3.5.3.47
1ACh	STATn_TX_PRI3_BCNT	Total number of bytes transmitted with Priority 3	Section 3.5.3.47
1B0h	STATn_TX_PRI4_BCNT	Total number of bytes transmitted with Priority 4	Section 3.5.3.47
1B4h	STATn_TX_PRI5_BCNT	Total number of bytes transmitted with Priority 5	Section 3.5.3.47
1B8h	STATn_TX_PRI6_BCNT	Total number of bytes transmitted with Priority 6	Section 3.5.3.47
1BCh	STATn_TX_PRI7_BCNT	Total number of bytes transmitted with Priority 7	Section 3.5.3.47
1C0h	STATn_TX_PRI0_DROP	Total number of packets dropped during transmit with Priority 0	Section 3.5.3.48
1C4h	STATn_TX_PRI1_DROP	Total number of packets dropped during transmit with Priority 1	Section 3.5.3.48
1C8h	STATn_TX_PRI2_DROP	Total number of packets dropped during transmit with Priority 2	Section 3.5.3.48
1CCh	STATn_TX_PRI3_DROP	Total number of packets dropped during transmit with Priority 3	Section 3.5.3.48
1D0h	STATn_TX_PRI4_DROP	Total number of packets dropped during transmit with Priority 4	Section 3.5.3.48
1D4h	STATn_TX_PRI5_DROP	Total number of packets dropped during transmit with Priority 5	Section 3.5.3.48
1D8h	STATn_TX_PRI6_DROP	Total number of packets dropped during transmit with Priority 6	Section 3.5.3.48
1DCh	STATn_TX_PRI7_DROP	Total number of packets dropped during transmit with Priority 7	Section 3.5.3.48
1E0h	STATn_TX_PRI0_DROP_BCNT	Total number of bytes dropped during transmit with Priority 0	Section 3.5.3.49

Table 3-139. Port Statistics Submodule Registers (n = 0-4 for a 5 port switch or n = 0-8 for a 9 port switch) (continued)

Offset Address[(1)]	Acronym	Description	Section
1E4h	STATn_TX_PRI1_DROP_BCNT	Total number of bytes dropped during transmit with Priority 1	Section 3.5.3.49
1E8h	STATn_TX_PRI2_DROP_BCNT	Total number of bytes dropped during transmit with Priority 2	Section 3.5.3.49
1ECh	STATn_TX_PRI3_DROP_BCNT	Total number of bytes dropped during transmit with Priority 3	Section 3.5.3.49
1F0h	STATn_TX_PRI4_DROP_BCNT	Total number of bytes dropped during transmit with Priority 4	Section 3.5.3.49
1F4h	STATn_TX_PRI5_DROP_BCNT	Total number of bytes dropped during transmit with Priority 5	Section 3.5.3.49
1F8h	STATn_TX_PRI6_DROP_BCNT	Total number of bytes dropped during transmit with Priority 6	Section 3.5.3.49
1FCh	STATn_TX_PRI7_DROP_BCNT	Total number of bytes dropped during transmit with Priority 7	Section 3.5.3.49

3.5.3.1 Port n Good Receive Frames Register (STATn_RXGOODFRAMES)

The Good Receive Frames Register is shown in Figure 3-126 and described in Table 3-140.

Figure 3-126. Port n Good Receive Frames Register (STATn_RXGOODFRAMES)

31	0
RXGOODFRAMES	
R-0h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-140. Port n Good Receive Frames Register (STATn_RXGOODFRAMES) Field Descriptions

Bits	Field	Description
31-0	RXGOODFRAMES	The total number of good frames received on the port. A frame must match all of the following criteria to be considered a good frame: • The frame was a data or MAC control frame that matched a unicast, broadcast or multicast address, or matched due to promiscuous mode • The frame was of length 64 to RX_MAXLEN bytes inclusive • The frame did not have a CRC error, alignment error, or code error Overruns have no effect on this statistic.

3.5.3.2 Port n Broadcast Receive Frames Register (STATn_RXBROADCASTFRAMES)

The Broadcast Receive Frames Register is shown in Figure 3-127 and described in Table 3-141.

Figure 3-127. Port n Broadcast Receive Frames Register (STATn_RXBROADCASTFRAMES)

31	0
RXBROADCASTFRAMES	
R-0h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-141. Port n Broadcast Receive Frames Register (STATn_RXBROADCASTFRAMES) Field Descriptions

Bits	Field	Description
31-0	RXBROADCASTFRAMES	The total number of good broadcast frames received on the port. A frame must match all of the following criteria to be considered a good broadcast frame: • The frame was a data or MAC control frame that was destined for address FFFFFFFFFFFFh • The frame was of length 64 to RX_MAXLEN bytes inclusive • The frame did not have a CRC error, alignment error, or code error Overruns have no effect on this statistic.

3.5.3.3 Port n Multicast Receive Frames Register (STATn_RXMULTICASTFRAMES)

The Multicast Receive Frames Register is shown in Figure 3-128 and described in Table 3-142.

Figure 3-128. Port n Multicast Receive Frames Register (STATn_RXMULTICASTFRAMES)

31	0
RXMULTICASTFRAMES	
R-0h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-142. Port n Multicast Receive Frames Register (STATn_RXMULTICASTFRAMES) Field Descriptions

Bits	Field	Description
31-0	RXMULTICASTFRAMES	The total number of good multicast frames received on the port. A frame must match all of the following criteria to be considered a good multicast frame: • The frame was a data or MAC control frame that was destined for any multicast address other than FFFFFFFFFFFFh • The frame was of length 64 to RX_MAXLEN bytes inclusive • The frame did not have a CRC error, alignment error, or code error Overruns have no effect on this statistic.

3.5.3.4 Port n Pause Receive Frames Register (STATn_RXPAUSEFRAMES)

The Pause Receive Frames Register is shown in Figure 3-129 and described in Table 3-143. This register only exists for the external Ethernet ports, it does not apply to host port 0.

Figure 3-129. Port n Pause Receive Frames Register (STATn_RXPAUSEFRAMES)

31	0
RXPAUSEFRAMES	
R-0h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-143. Port n Pause Receive Frames Register (STATn_RXPAUSEFRAMES) Field Descriptions

Bits	Field	Description
31-0	RXPAUSEFRAMES	The total number of IEEE 802.3X pause frames received on the port. A frame must match all of the following criteria to be considered a pause frame: • The frame contained a unicast, broadcast, or multicast address • The frame contains the length/type field value 88.08h and the opcode 0001h • The frame was of length 64 to RX_MAXLEN bytes inclusive • The frame did not have a CRC error, alignment error or code error • Pause-frames were enabled on the port (TX_FLOW_EN = 1). The port could have been in half or full-duplex mode. Overruns have no effect on this statistic. - OR - The total number of priority based flow control (802.1Qbb) pause frames received by the port (whether acted upon or not). A frame must match all of the following criteria to be considered a priority based flow control pause frame: • The frame contained any unicast, broadcast, or multicast address • The frame contained the length/type field value 88.08 hex) and the opcode 0x0001 • The frame was of length 64 to RX_MAXLEN bytes inclusive • The frame had no CRC error • Priority based flow control pause frames were enabled on the port Overruns have no effect on this statistic.

3.5.3.5 Port n Receive CRC Errors Register (STATn_RXCRCERRORS)

The Receive CRC Errors Register is shown in Figure 3-130 and described in Table 3-144.

Figure 3-130. Port n Receive CRC Errors Register (STATn_RXCRCERRORS)

31	0
RXCRCERRORS	
R-0h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-144. Port n Receive CRC Errors Register (STATn_RXCRCERRORS) Field Descriptions

Bits	Field	Description
31-0	RXCRCERRORS	The total number of frames received on the port that experienced a CRC error. A frame must match all of the following criteria to be considered a CRC error frame: • The frame was a data or MAC control frame that matched a unicast, broadcast, or multicast address, or matched due to promiscuous mode • The frame was of length 64 to RX_MAXLEN bytes inclusive • The frame did not have an alignment error or code error • The frame had a CRC error A CRC error must meet the following two conditions: • A frame that contains an even number of nibbles • A frame that fails the Frame Check Sequence test Overruns have no effect on this statistic.

3.5.3.6 Port n Receive Align/Code Errors Register (STATn_RXALIGNCODEERRORS)

The Receive Align/Code Errors Register is shown in Figure 3-131 and described in Table 3-145. This register only exists for the external Ethernet ports, it does not apply to host port 0.

Figure 3-131. Port n Receive Align/Code Errors Register (STATn_RXALIGNCODEERRORS)

31	0
RXALIGNCODEERRORS	
R-0h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-145. Port n Receive Align/Code Errors Register (STATn_RXALIGNCODEERRORS) Field Descriptions

Bits	Field	Description
31-0	RXALIGN CODEERRORS	The total number of frames received on the port that experienced an alignment error or code error. A frame must match all of the following criteria to be considered an alignment or code error frame: • The frame was a data or MAC control frame that matched a unicast, broadcast, or multicast address, or matched due to promiscuous mode • The frame was of length 64 to RX_MAXLEN bytes inclusive • The frame had an alignment error or code error An alignment error must meet the following two conditions: • A frame that contains an odd number of nibbles • A frame that fails the Frame Check Sequence test if the final nibble is ignored A code error must meet the following condition: • A frame that has been discarded because the port's MRXER pin driven with a 1 for at least one bit-time's duration at any point during the frame's reception Overruns have no effect on this statistic.

3.5.3.7 Port n Oversize Receive Frames Register (STATn_RXOVERSIZEDFRAMES)

The Oversize Receive Frames Register is shown in Figure 3-132 and described in Table 3-146.

Figure 3-132. Port n Oversize Receive Frames Register (STATn_RXOVERSIZEDFRAMES)

31	0
RXOVERSIZEDFRAMES	
R-0h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-146. Port n Oversized Receive Frames Register (STATn_RXOVERSIZEDFRAMES) Field Descriptions

Bits	Field	Description
31-0	RXOVERSIZED FRAMES	The total number of oversized frames received on the port. A frame must match all of the following criteria to be considered an oversized frame: • The frame was a data or MAC control frame that matched a unicast, broadcast, or multicast address, or matched due to promiscuous mode • The frame was greater than RX_MAXLEN bytes • The frame did not have a CRC error, alignment error, or code error Overruns have no effect on this statistic.

3.5.3.8 Port n Receive Jabber Frames Register (STATn_RXJABBERFRAMES)

The Receive Jabber Frames Register is shown in Figure 3-133 and described in Table 3-147. This register only exists for the external Ethernet ports, it does not apply to host port 0.

Figure 3-133. Port n Receive Jabber Frames Register (STATn_RXJABBERFRAMES)

31	0
RXJABBERFRAMES	
R-0h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

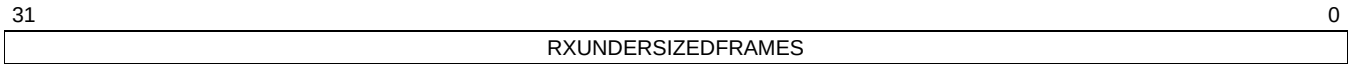
Table 3-147. Port n Receive Jabber Frames Register (STATn_RXJABBERFRAMES) Field Descriptions

Bits	Field	Description
31-0	RXJABBER FRAMES	The total number of jabber frames received on the port. A frame must match all of the following criteria to be considered a jabber frame: • The frame was a data or MAC control frame that matched a unicast, broadcast, or multicast address, or matched due to promiscuous mode • The frame was greater than RX_MAXLEN bytes • The frame did had a CRC error, alignment error, or code error Overruns have no effect on this statistic.

3.5.3.9 Port n Undersize (Short) Receive Frames Register (STATn_RXUNDERSIZEDFRAMES)

The Undersize (Short) Receive Frames Register is shown in Figure 3-134 and described in Table 3-148.

Figure 3-134. Port n Undersize (Short) Receive Frames Register (STATn_RXUNDERSIZEDFRAMES)



Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-148. Port n Undersized (Short) Receive Frames Register (STATn_RXUNDERSIZEDFRAMES) Field Descriptions

Bits	Field	Description
31-0	RXUNDERSIZED FRAMES	The total number of undersized frames received on the port. A frame must match all of the following criteria to be considered an undersized frame: • The frame was a data or MAC control frame that matched a unicast, broadcast, or multicast address, or matched due to promiscuous mode • The frame was less than 64 bytes • The frame did not have a CRC error, alignment error, or code error Overruns have no effect on this statistic.

3.5.3.10 Port n Receive Fragment Register (STATn_RXFRAGMENTS)

The Receive Fragment Register is shown in Figure 3-135 and described in Table 3-149. This register only exists for the external Ethernet ports, it does not apply to host port 0.

Figure 3-135. Port n Receive Fragment Register (STATn_RXFRAGMENTS)

31	0
RXFRAGMENTS	
R-0h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-149. Port n Receive Fragment Frames Register (STATn_RXFRAGMENTS) Field Descriptions

Bits	Field	Description
31-0	RXFRAGMENTS	The total number of frame fragments received on the port. A frame fragment must match all of the following criteria to be considered a frame fragment: • The frame was a data frame (address matching does not matter) • The frame was less than 64 bytes • The frame had a CRC error, alignment error, or code error • The frame was not the result of a collision caused by half duplex, collision based flow control Overruns have no effect on this statistic.

3.5.3.11 Port n ALE Drop Frames Register (STATn_ALE_DROP)

The ALE Drop Frames Register is shown in Figure 3-136 and described in Table 3-150.

Figure 3-136. Port n ALE Drop Frames Register (STATn_ALE_DROP)

31	0
ALE_DROP_FRAMES	
R-0h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-150. Port n ALE Drop Frames Register (STATn_ALE_DROP) Field Descriptions

Bits	Field	Description
31-0	ALE_DROP_FRAMES	The total number of frames received on a port such that the destination address was not equal to the source address and the packet was not destined to the port it was received on, but the frame was not forwarded to any port (the PORT_MASK was zero). A frame must match all of the following criteria to be considered an ALE drop frame: • The frame was a data or MAC control frame that matched a unicast, broadcast, or multicast address, or matched due to promiscuous mode • The frame was of length 64 to RX_MAXLEN bytes inclusive • The frame did not have a CRC error, alignment error, or code error • The frame destination address was not equal to the frame source address • The packet was not destined for the port it was received on • The packet had a zero PORT_MASK

3.5.3.12 Port n ALE Overrun Drop Frames Register (STATn_ALE_OVERRUN_DROP)

The ALE Overrun Drop Frames Register is shown in Figure 3-137 and described in Table 3-151.

Figure 3-137. Port n ALE Overrun Drop Frames Register (STATn_ALE_OVERRUN_DROP)

31	0
ALE_OVERRUN_DROP_FRAMES	
R-0h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-151. Port n ALE Overrun Drop Frames Register (STATn_ALE_OVERRUN_DROP) Field Descriptions

Bits	Field	Description
31-0	ALE_DROP_FRAMES	The total number of frames received on a port that were dropped (zero PORT_MASK) due to exceeding the maximum ALE lookup rate (Port 0 should not have ALE Overrun Drops because the ingress rate is controlled to prevent it). This statistic should be zero and when non-zero indicates a system clock issue or indicates that short packets were sent with RX_CSF_EN at a rate that exceeded the maximum lookup rate. A frame must match all of the following criteria to be considered an ALE overrun drop frame: • The frame was a data or MAC control frame that matched a unicast, broadcast, or multicast address, or matched due to promiscuous mode • The frame was of length 64 to RX_MAXLEN bytes inclusive • The maximum ALE lookup rate was exceeded so the lookup was aborted and the packet was dropped

3.5.3.13 Port n Receive Octets Register (STATn_RXOCTETS)

The Receive Octets Register is shown in Figure 3-138 and described in Table 3-152.

Figure 3-138. Port n Receive Octets Register (STATn_RXOCTETS)

31	0
RXOCTETS	
R-0h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-152. Port n Receive Octets Register (STATn_RXOCTETS) Field Descriptions

Bits	Field	Description
31-0	RXOCTETS	The total number of bytes in all good frames received on the port. A frame must match all of the following criteria to be considered a good frame: • The frame was a data or MAC control frame that matched a unicast, broadcast or multicast address, or matched due to promiscuous mode • The frame was of length 64 to RX_MAXLEN bytes inclusive • The frame did not have a CRC error, alignment error, or code error Overruns have no effect on this statistic.

3.5.3.14 Port n Good Transmit Frames Register (STATn_TXGOODFRAMES)

The Good Transmit Frames Register is shown in Figure 3-139 and described in Table 3-153.

Figure 3-139. Port n Good Transmit Frames Register (STATn_TXGOODFRAMES)

31	0
TXGOODFRAMES	
R-0h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-153. Port n Good Transmit Frames Register (STATn_TXGOODFRAMES) Field Descriptions

Bits	Field	Description
31-0	TXGOODFRAMES	The total number of good frames transmitted on the port. A frame must match all of the following criteria to be considered a good frame: • The frame was a data or MAC control frame that was destined for a unicast, broadcast or multicast address • The frame was of any length • The frame did not have late or excessive collisions, no carrier loss, and no underrun

3.5.3.15 Port n Broadcast Transmit Frames Register (STATn_TXBROADCASTFRAMES)

The Broadcast Transmit Frames Register is shown in Figure 3-140 and described in Table 3-154.

Figure 3-140. Port n Broadcast Transmit Frames Register (STATn_TXBROADCASTFRAMES)

31	0
TXBROADCASTFRAMES	
R-0h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-154. Port n Broadcast Transmit Frames Register STATn_TXBROADCASTFRAMES) Field Descriptions

Bits	Field	Description
31-0	TXBROADCAST FRAMES	The total number of good broadcast frames transmitted on the port. A frame must match all of the following criteria to be considered a good broadcast frame: • The frame was a data or MAC control frame that was destined for address FFFFFFFFFFFFh • The frame was of any length • The frame did not have late or excessive collisions, no carrier loss, and no underrun

3.5.3.16 Port n Multicast Transmit Frames (STATn_TXMULTICASTFRAMES)

The Multicast Transmit Frames Register is shown in Figure 3-141 and described in Table 3-155.

Figure 3-141. Port n Multicast Transmit Frames (STATn_TXMULTICASTFRAMES)

31	0
TXMULTICASTFRAMES	
R-0h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-155. Port n Multicast Transmit Frames Register (STATn_TXMULTICASTFRAMES) Field Descriptions

Bits	Field	Description
31-0	TXMULTICAST FRAMES	The total number of good multicast frames transmitted on the port. A frame must match all of the following criteria to be considered a good multicast frame: • The frame was a data or MAC control frame that was destined for any multicast address other than FFFFFFFFFFFFh • The frame was of any length • The frame did not have late or excessive collisions, no carrier loss, and no underrun

3.5.3.17 Port n Pause Transmit Frames Register (STATn_TXPAUSEFRAMES)

The Pause Transmit Frames Register is shown in Figure 3-142 and described in Table 3-156. This register only exists for the external Ethernet ports, it does not apply to host port 0.

Figure 3-142. Port n Pause Transmit Frames Register (STATn_TXPAUSEFRAMES)

31	0
TXPAUSEFRAMES	
R-0h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-156. Port n Pause Transmit Frames Register (STATn_TXPAUSEFRAMES) Field Descriptions

Bits	Field	Description
31-0	TXPAUSE FRAMES	The total number of IEEE 802.3X pause frames transmitted on the port. Pause frames cannot underrun or contain a CRC error because they are created in the transmitting MAC, so these error conditions have no effect on the statistic. Pause frames sent by software will not be included in this count. Since pause frames are only transmitted in full duplex mode, carrier loss and collisions have no effect on this statistic. Transmitted pause frames are always 64 byte multicast frames, so these frames will appear in the TXMULTICASTFRAMES and 64OCTECTFRAMES statistics.

3.5.3.18 Port n Deferred Transmit Frames Register (STATn_TXDEFERREDFRAMES)

The Deferred Transmit Frames Register is shown in Figure 3-143 and described in Table 3-157. This register only exists for the external Ethernet ports, it does not apply to host port 0.

Figure 3-143. Port n Deferred Transmit Frames Register (STATn_TXDEFERREDFRAMES)

31	0
TXDEFERREDFRAMES	
R-0h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-157. Port n Deferred Transmit Frames Register (STATn_TXDEFERREDFRAMES) Field Descriptions

Bits	Field	Description
31-0	TXDEFERRED FRAMES	The total number of frames transmitted on the port that first experienced deferment. A frame must match all of the following criteria to be considered a deferred frame: • The frame was a data or MAC control frame that was destined for a unicast, broadcast or multicast address • The frame was of any length • The frame did not have carrier loss or underrun • The frame did not experience any collisions before being successfully transmitted • The frame found the medium busy when transmission was first attempted, so had to wait CRC errors have no effect on this statistic.

3.5.3.19 Port n Transmit Frames Collision Register (STATn_TXCOLLISIONFRAMES)

The Transmit Frames Collision Register is shown in Figure 3-144 and described in Table 3-158. This register only exists for the external Ethernet ports, it does not apply to host port 0.

Figure 3-144. Port n Transmit Frames Collision Register (STATn_TXCOLLISIONFRAMES)

31	0
TXCOLLISIONFRAMES	
R-0h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-158. Port n Transmit Frames Collision Register (STATn_TXCOLLISIONFRAMES) Field Descriptions

Bits	Field	Description
31-0	TXCOLLISION FRAMES	This statistic records the total number of times that this port has experienced a collision. Collisions occur under two circumstances: 1. When all of the following conditions are true for a transmit data or MAC control frame: • The frame was destined for any unicast, broadcast or multicast address • The frame was of any size • The frame had no carrier loss and no underrun • The frame experienced a collision. A jam sequence is sent for every non-late collision, so this statistic will increment on each occasion if a frame experiences multiple collisions (and increments on late collisions). CRC errors have no effect on this statistic. 2. When the port is in half-duplex mode, flow control is active, and a frame reception begins.

3.5.3.20 Port n Transmit Frames Single Collision Register (STATn_TXSINGLECOLLFRAMES)

The Transmit Frames Single Collision Register is shown in Figure 3-145 and described in Table 3-159. This register only exists for the external Ethernet ports, it does not apply to host port 0.

Figure 3-145. Port n Transmit Frames Single Collision Register (STATn_TXSINGLECOLLFRAMES)

31	0
TXSINGLECOLLFRAMES	
R-0h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-159. Port n Transmit Frames Single Collision Register (STATn_TXSINGLECOLLFRAMES) Field Descriptions

Bits	Field	Description
31-0	TXSINGLECOLL FRAMES	The total number of frames transmitted on the port that experience exactly one collision. A frame must match all of the following criteria to be considered a single collision frame: • The frame was a data or MAC control frame that was destined for a unicast, broadcast or multicast address • The frame was of any length • The frame did not have carrier loss or underrun • The frame experienced one collision before successful transmission, and the collision was not late CRC errors have no effect on this statistic.

3.5.3.21 Port n Transmit Frames Multiple Collision Register (STATn_TXMULTCOLLFRAMES)

The Transmit Frames Multiple Collision Register is shown in Figure 3-146 and described in Table 3-160. This register only exists for the external Ethernet ports, it does not apply to host port 0.

Figure 3-146. Port n Transmit Frames Multiple Collision Register (STATn_TXMULTCOLLFRAMES)

31	0
TXMULTCOLLFRAMES	
R-0h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-160. Port n Transmit Frames Multiple Collision Register (STATn_TXMULTCOLLFRAMES) Field Descriptions

Bits	Field	Description
31-0	TXMULTCOLL FRAMES	The total number of frames transmitted on the port that experience multiple collisions. A frame must match all of the following criteria to be considered a multiple collision frame: • The frame was a data or MAC control frame that was destined for a unicast, broadcast or multicast address • The frame was of any length • The frame did not have carrier loss or underrun • The frame experienced 2-15 collisions before successful transmission, and none of the collisions were late CRC errors have no effect on this statistic.

3.5.3.22 Port n Transmit Excessive Collision Register (STATn_TXEXCESSIVECOLLISIONS)

The Transmit Excessive Collision Register is shown in Figure 3-147 and described in Table 3-161. This register only exists for the external Ethernet ports, it does not apply to host port 0.

Figure 3-147. Port n Transmit Excessive Collision Register (STATn_TXEXCESSIVECOLLISIONS)

31	0
TXEXCESSIVECOLLISIONS	
R-0h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-161. Port n Transmit Excessive Collisions Register (STATn_TXECESSIVECOLLISIONS) Field Descriptions

Bits	Field	Description
31-0	TXEXCESSIVE COLLISIONS	The total number of frames on the port where transmission was abandoned due to excessive collisions. Such a frame must match all of the following criteria: • The frame was a data or MAC control frame that was destined for a unicast, broadcast or multicast address • The frame was of any length • The frame did not have carrier loss or underrun • The frame experienced 16 collisions before abandoning all attempts at transmitting the frame, and none of the collisions were late CRC errors have no effect on this statistic.

3.5.3.23 Port n Transmit Late Collisions Register (STATn_TXLATECOLLISIONS)

The Transmit Late Collisions Register is shown in Figure 3-148 and described in Table 3-162. This register only exists for the external Ethernet ports, it does not apply to host port 0.

Figure 3-148. Port n Transmit Late Collisions Register (STATn_TXLATECOLLISIONS)

31	0
TXLATECOLLISIONS	
R-0h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-162. Port n Transmit Late Collisions Register (STATn_TXLATECOLLISIONS) Field Descriptions

Bits	Field	Description
31-0	TXLATECOLLISIONS	The total number of frames on the port where transmission was abandoned due to a late collision. Such a frame must match all of the following criteria: • The frame was a data or MAC control frame that was destined for a unicast, broadcast or multicast address • The frame was of any length • The frame did not have carrier loss or underrun • The frame experienced a collision later than 512 bit-times into the transmission. There may have been up to 15 previous (non-late) collisions that had previously required the transmission to be re-attempted. The Late Collisions statistic dominates over the single, multiple and excessive Collisions statistics - if a late collision occurs the frame will not be counted in any of these other three statistics. CRC errors, carrier loss, and underrun have no effect on this statistic.

3.5.3.24 Port n Transmit Carrier Sense Errors Register (STATn_TXCARRIERSENSEERRORS)

The Transmit Carrier Sense Errors Register is shown in Figure 3-149 and described in Table 3-163. This register only exists for the external Ethernet ports, it does not apply to host port 0.

Figure 3-149. Port n Transmit Carrier Sense Errors Register (STATn_TXCARRIERSENSEERRORS)

31	0
TXCARRIERSENSEERRORS	
R-0h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

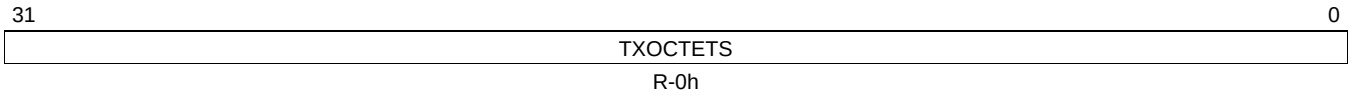
Table 3-163. Port n Transmit Carrier Sense Errors Register (STATn_TXCARRIERSENSEERRORS) Field Descriptions

Bits	Field	Description
31-0	TXCARRIERSENSE ERRORS	The total number of frames on the port that experience carrier loss. Such a frame must match all of the following criteria: • The frame was a data or MAC control frame that was destined for a unicast, broadcast or multicast address • The frame was of any length • The carrier sense condition was lost or never asserted when transmitting the frame (the frame is not retransmitted). This is a transmit only statistic. Carrier Sense is a don't care for received frames. Transmit frames with carrier sense errors are sent until completion and are not aborted. CRC errors and underrun have no effect on this statistic.

3.5.3.25 Port n Transmit Octets Register (STATn_TXOCTETS)

The Transmit Octets Register is shown in Figure 3-150 and described in Table 3-164.

Figure 3-150. Port n Transmit Octets Register (STATn_TXOCTETS)



Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-164. Port n Transmit Octets Register (STATn_TXOCTETS) Field Descriptions

Bits	Field	Description
31-0	TXOCTETS	The total number of bytes in all good frames transmitted on the port. A frame must match all of the following criteria to be considered a good frame: • The frame was a data or MAC control frame that was destined for any unicast, broadcast or multicast address • The frame was any size • The frame had no late or excessive collisions, no carrier loss, and no underrun

3.5.3.26 Port n Receive and Transmit 64 Octet Frames Register (STATn_64OCTETFRAMES)

The Receive and Transmit 64 Octet Frames Register is shown in Figure 3-151 and described in Table 3-165.

Figure 3-151. Port n Receive and Transmit 64 Octet Frames Register (STATn_64OCTETFRAMES)

31	0
64OCTETFRAMES	
R-0h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-165. Port n Receive and Transmit 64 Octet Frames Register (STATn_64OCTETFRAMES) Field Descriptions

Bits	Field	Description
31-0	64OCTET FRAMES	The total number of 64-byte frames received and transmitted on the port. Such a frame must match all of the following criteria: • The frame was a data or MAC control frame that was destined for any unicast, broadcast or multicast address • The frame did not experience late collisions, excessive collisions, or carrier sense error, and • The frame was exactly 64 bytes long. (If the frame was being transmitted and experienced carrier loss that resulted in a frame of this size being transmitted, then the frame will be recorded in this statistic). CRC errors, code/align errors, and overruns do not affect the recording of frames in this statistic.

3.5.3.27 Port n Receive and Transmit 65-127 Octet Frames Register (STATn_65T127OCTETFRAMES)

The Receive and Transmit 65-127 Octet Frames Register is shown in Figure 3-152 and described in Table 3-166.

Figure 3-152. Port n Receive and Transmit 65-127 Octet Frames Register (STATn_65T127OCTETFRAMES)

31	0
65T127OCTETFRAMES	
R-0h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-166. Port n Receive and Transmit 65-127 Octet Frames Register (STATn_65T127OCTETFRAMES) Field Descriptions

Bits	Field	Description
31-0	65T127OCTET FRAMES	The total number of frames of size 65 to 127 bytes received and transmitted on the port. Such a frame must match all of the following criteria: • The frame was a data or MAC control frame that was destined for any unicast, broadcast or multicast address • The frame was did not experience late collisions, excessive collisions, or carrier sense error • The frame was 65 to 127 bytes long CRC errors, code/align errors, underruns, and overruns do not affect the recording of frames in this statistic.

3.5.3.28 Port n Receive and Transmit 128-255 Octet Frames Register (STATn_128T255OCTETFRAMES)

The Receive and Transmit 128-255 Octet Frames Register is shown in Figure 3-153 and described in Table 3-167.

Figure 3-153. Port n Receive and Transmit 128-255 Octet Frames Register (STATn_128T255OCTETFRAMES)

31	0
128T255OCTETFRAMES	
R-0h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-167. Port n Receive and Transmit 128-255 Octet Frames Register (STATn_128T255OCTETFRAMES) Field Descriptions

Bits	Field	Description
31-0	128T255OCTET FRAMES	The total number of frames of size 128 to 255 bytes received and transmitted on the port. Such a frame must match all of the following criteria: • The frame was a data or MAC control frame that was destined for any unicast, broadcast or multicast address • The frame did not experience late collisions, excessive collisions, or carrier sense error • The frame was 128 to 255 bytes long CRC errors, code/align errors, underruns and overruns do not affect the recording of frames in this statistic.

3.5.3.29 Port n Receive and Transmit 256-511 Octet Frames Register (STATn_256T511OCTETFRAMES)

The Receive and Transmit 256-511 Octet Frames Register is shown in Figure 3-154 and described in Table 3-168.

Figure 3-154. Port n Receive and Transmit 256-511 Octet Frames Register (STATn_256T511OCTETFRAMES)

31	0
256T511OCTETFRAMES	
R-0h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-168. Port n Receive and Transmit 256-511 Octet Frames Register (STATn_256T511OCTETFRAMES) Field Descriptions

Bits	Field	Description
31-0	256T511OCTET FRAMES	The total number of frames of size 256 to 511 bytes received and transmitted on the port. Such a frame must match all of the following criteria: • The frame was a data or MAC control frame that was destined for any unicast, broadcast or multicast address • The frame did not experience late collisions, excessive collisions, or carrier sense error • The frame was 256 to 511 bytes long CRC errors, code/align errors, underruns and overruns do not affect the recording of frames in this statistic.

3.5.3.30 Port n Receive and Transmit 512-1023 Octet Frames Register (STATn_512T1023OCTETFRAMES)

The Receive and Transmit 512-1023 Octet Frames Register is shown in Figure 3-155 and described in Table 3-169.

Figure 3-155. Port n Receive and Transmit 512-1023 Octet Frames Register (STATn_512T1023OCTETFRAMES)

31	0
512T1023OCTETFRAMES	
R-0h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-169. Port n Receive and Transmit 512-1023 Octet Frames Register (STATn_512T1023OCTETFRAMES) Field Descriptions

Bits	Field	Description
31-0	512T1023OCTET FRAMES	The total number of frames of size 512 to 1023 bytes received and transmitted on the port. Such a frame must match all of the following criteria: • The frame was a data or MAC control frame that was destined for any unicast, broadcast or multicast address • The frame did not experience late collisions, excessive collisions, or carrier sense error • The frame was 512 to 1023 bytes long CRC errors, code/align errors and overruns do not affect the recording of frames in this statistic.

3.5.3.31 Port n Receive and Transmit 1024 and Up Octet Frames Register (STATn_1024TUPOCTETFRAMES)

The Receive and Transmit 1024 And Up Octet Frames Register is shown in Figure 3-156 and described in Table 3-170.

Figure 3-156. Port n Receive and Transmit 1024 and Up Octet Frames Register (STATn_1024TUPOCTETFRAMES)

31	0
1024TUPOCTETFRAMES	
R-0h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-170. Port n Receive and Transmit 1024 and Up Octet Frames Register (STATn_1024TUPOCTETFRAMES) Field Descriptions

Bits	Field	Description
31-0	1024TUPOCTET FRAMES	The total number of frames of size 1024 to RX_MAXLEN bytes for receive or 1024 up for transmit on the port. Such a frame must match all of the following criteria: • The frame was a data or MAC control frame that was destined for any unicast, broadcast or multicast address • The frame did not experience late collisions, excessive collisions, or carrier sense error • The frame was 1024 to RX_MAXLEN bytes long on receive, or any size on transmit CRC errors, code/align errors, underruns and overruns do not affect the recording of frames in this statistic.

3.5.3.32 Port n Net Octets Register (STATn_NETOCTETS)

The Net Octets Register is shown in Figure 3-157 and described in Table 3-171.

Figure 3-157. Port n Net Octets Register (STATn_NETOCTETS)

31	0
NETOCTETS	
R-0h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-171. Port n Net Octets Register (STATn_NETOCTETS) Field Descriptions

Bits	Field	Description
31-0	NETOCTETS	The total number of bytes of frame data received and transmitted on the port. Each frame must match all of the following criteria to be counted: • The frame was a data or MAC control frame destined for any unicast, broadcast, or multicast address (address match does not matter) • The frame was of any length, including a length of less than 64 bytes or greater than RX_MAXLEN bytes This statistic also counts: • Every byte transmitted before a carrier-loss was experienced • Every byte transmitted before each collision was experienced (i.e. multiple retries are counted each time) • Every byte received if the port is in half-duplex mode until a jam sequence was transmitted to initiate flow control. (The jam sequence was not counted to prevent double-counting). Error conditions such as alignment errors, CRC errors, code errors, overruns, and underruns do not affect the recording of bytes by this statistic. The objective of this statistic is to give a reasonable indication of Ethernet utilization.

3.5.3.33 Port n Receive Bottom of FIFO Drop Register (STATn_RX_BOTTOM_FIFO_DROP)

The Receive Bottom of FIFO Drop Register is shown in Figure 3-158 and described in Table 3-172.

Figure 3-158. Port n Receive Bottom of FIFO Drop Register (STATn_RX_BOTTOM_FIFO_DROP)

31	0
RX_BOTTOM_FIFO_DROP	
R-0h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-172. Port n Receive Bottom of FIFO Drop Register (STATn_RX_BOTTOM_FIFO_DROP) Field Descriptions

Bits	Field	Description
31-0	RX_BOTTOM_FIFO_DROP	The total number of frames received on the port that overran the port's receive FIFO and were dropped (bottom of receive FIFO). Host port 0 should not drop packets on receive because port 0 receive flow control should be enabled. The Ethernet ports will only drop packets in the receive FIFO when receive flow control is enabled and the sending port ignores sent pause frame and then overruns the receive FIFO. A frame must match all of the following criteria to be considered a bottom of FIFO drop frame: • The frame was a data or MAC control frame that matched a unicast, broadcast, or multicast address, or matched due to promiscuous mode • The frame was any length, including length less than 64 bytes or greater than RX_MAXLEN bytes • The packet was dropped on the port due to a lack of memory space in the receive FIFO This statistic also counts frames dropped on host port 0 that were 17 to 33 bytes (only for port 0). For Ethernet ports, the drop count for frames shorter than 33 bytes is included in the undersized or fragment count. Port 0 simply gives an indication that a packet with 33 bytes was dropped. No other statistics are counted for frames shorter than 33 bytes.

3.5.3.34 Port n Port Mask Drop Register (STATn_PORTMASK_DROP)

The Port Mask Drop Register is shown in Figure 3-159 and described in Table 3-173.

Figure 3-159. Port n Port Mask Drop Register (STATn_PORTMASK_DROP)

31	0
PORTMASK_DROP	
R-0h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-173. Port n Port Mask Drop Register (STATn_PORTMASK_DROP) Field Descriptions

Bits	Field	Description
31-0	PORTMASK_DROP	The total number of frames received on a port that were dropped by the ALE (the ALE did not forward the packet to any port). A frame must match all of the following criteria to be considered a port mask drop frame: • The frame was a data or MAC control frame that matched a unicast, broadcast, or multicast address, or matched due to promiscuous mode • The frame was any length greater than 32 bytes • The frame was dropped by the ALE - ALE_PORTMASK = 0 (was not sent to any destination port) • The frame could have been dropped due to error or other counted reason, so it could be counted elsewhere also Note: This statistic does not count in the overall total as it includes every packet received greater than 32 bytes that had a zero port mask.

3.5.3.35 Port n Receive Top of FIFO Drop Register (STATn_RX_TOP_FIFO_DROP)

The Receive Top of FIFO Drop Register is shown in Figure 3-160 and described in Table 3-174.

Figure 3-160. Port n Receive Top of FIFO Drop Register (STATn_RX_TOP_FIFO_DROP)

31	0
RX_TOP_FIFO_DROP	
R-0h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-174. Port n Receive Top of FIFO Drop Register (STATn_RX_TOP_FIFO_DROP) Field Descriptions

Bits	Field	Description
31-0	RX_TOP_FIFO_DROP	The total number of frames received on the port that had a start of frame (SOF) overrun on any destination port egress (when attempting to load the packet from the top of the ingress port receive FIFO into any other port's transmit FIFO). If a multicast/broadcast packet is dropped by multiple destination ports then this statistic will increment by the number of ports that dropped the packet. A frame must match all of the following criteria to be considered a top of FIFO drop frame: • The frame was a data or MAC control frame that matched a unicast, broadcast, or multicast address, or matched due to promiscuous mode • The frame was any length, including length less than 64 bytes or greater than RX_MAXLEN bytes • The frame had no CRC error, alignment error, or code error • The packet had a start of frame (SOF) overrun on another port egress

3.5.3.36 Port n ALE Rate Limit Drop Register (STATn_ALE_RATE_LIMIT_DROP)

The ALE Rate Limit Drop Register is shown in Figure 3-161 and described in Table 3-175.

Figure 3-161. Port n ALE Rate Limit Drop Register (STATn_ALE_RATE_LIMIT_DROP)

31	0
ALE_RL_DROP	
R-0h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

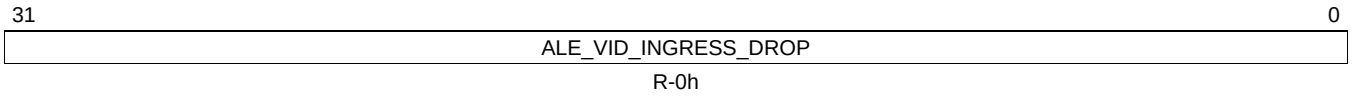
Table 3-175. Port n Receive Top of FIFO Drop Register (STATn_ALE_RATE_LIMIT_DROP) Field Descriptions

Bits	Field	Description
31-0	ALE_RL_DROP	The total number of frames received on the port that were dropped (zero port mask) due to receive rate limiting on this port or due to transmit rate limiting on any destination port (not sent to all expected destination ports if transmit rate limiting). A frame must match all of the following criteria to be considered an ALE rate limit drop frame: • The frame was a data or MAC control frame that matched a unicast, broadcast, or multicast address, or matched due to promiscuous mode • The frame was any length, including length less than 64 bytes or greater than RX_MAXLEN bytes • The frame had no CRC error, alignment error, or code error • The receive rate was exceeded and the packet was dropped to one or more expected destination ports (indicates that the destinations were pruned due to rate limiting).

3.5.3.37 Port n ALE VLAN ID Ingress Check Drop Register (STATn_ALE_VID_INGRESS_DROP)

The ALE VLAN ID Ingress Check Drop Register is shown in Figure 3-162 and described in Table 3-176.

Figure 3-162. Port n ALE VLAN ID Ingress Check Drop Register (STATn_ALE_VID_INGRESS_DROP)



Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-176. Port n ALE VLAN ID Ingress Check Drop Register (STATn_ALE_VID_INGRESS_DROP) Field Descriptions

Bits	Field	Description
31-0	ALE_VID_INGRESS_DROP	The total number of frames received on the port that were dropped (zero port mask) due to VLAN ingress check failure. A frame must match all of the following criteria to be considered an ALE VLAN ID ingress check drop frame: • The frame was a data or MAC control frame that matched a unicast, broadcast, or multicast address, or matched due to promiscuous mode • The frame was any length, including length less than 64 bytes or greater than RX_MAXLEN bytes • The frame had no CRC error, alignment error, or code error • The VLAN ID ingress check failed (the receive port was not in the group) • The ALE address lookup did not return a match with the SUPER bit set

3.5.3.38 Port n Destination Equals Source Drop Register (STATn_ALE_DA_EQ_SA_DROP)

The ALE Destination Equals Source Drop Register is shown in Figure 3-163 and described in Table 3-177.

Figure 3-163. Port n ALE Destination Equals Source Drop Register (STATn_ALE_DA_EQ_SA_DROP)

31	0
ALE_DA_EQ_SA_DROP	
R-0h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-177. Port n ALE Destination Equals Source Drop Register (STATn_ALE_DA_EQ_SA_DROP) Field Descriptions

Bits	Field	Description
31-0	ALE_DA_EQ_SA_DROP	The total number of frames received on the port that were dropped (zero port mask) due to destination address equal to source address. A frame must match all of the following criteria to be considered for destination equal source dropping: • The frame was a data or MAC control frame that matched a unicast, broadcast, or multicast address, or matched due to promiscuous mode • The frame was any length, including length less than 64 bytes or greater than RX_MAXLEN bytes • The frame had no CRC error, alignment error, or code error • The frame destination address was equal to the source address • The frame source address was not an entry in the ALE table

3.5.3.39 Port n ALE Unknown Unicast Destination Register (STATn_ALE_UNKN_UNI)

The ALE Unknown Unicast Destination Register is shown in Figure 3-164 and described in Table 3-178.

Figure 3-164. Port n ALE Unknown Unicast Destination Register (STATn_ALE_UNKN_UNI)

31	0
ALE_UNKN_UNI	
vvvvR-0h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-178. Port n ALE Unknown Unicast Destination Register (STATn_ALE_UNKN_UNI) Field Descriptions

Bits	Field	Description
31-0	ALE_UNKN_UNI	The total number of frames received on the port that had a unicast destination address with an unknown source address. Such a frame must match all of the following criteria: • The frame was any data frame with a unicast destination address • The frame source address was not an ALE table entry • The frame was of length 64 to RX_MAXLEN bytes inclusive • The frame had no CRC error, alignment error, or code error

3.5.3.40 Port n ALE Unknown Unicast Destination Byte Count Register (STATn_ALE_UNKN_UNI_BCNT)

The ALE Unknown Unicast Destination Byte Count Register is shown in Figure 3-165 and described in Table 3-179.

Figure 3-165. Port n ALE Unknown Unicast Destination Byte Count Register (STATn_ALE_UNKN_UNI_BCNT)

31	0
ALE_UNKN_UNI_BCNT	
R-0h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-179. Port n ALE Unknown Unicast Destination Byte Count Register (STATn_ALE_UNKN_UNI_BCNT) Field Descriptions

Bits	Field	Description
31-0	ALE_UNKN_UNI_BCNT	The total number of bytes contained in the ALE Unknown Unicast frames (STATn_ALE_UNKN_UNI register).

3.5.3.41 Port n ALE Unknown Multicast Destination Register (STATn_ALE_UNKN_MLT)

The ALE Unknown Multicast Destination Register is shown in Figure 3-166 and described in Table 3-180.

Figure 3-166. Port n ALE Unknown Multicast Destination Register (STATn_ALE_UNKN_MLT)

31	0
ALE_UNKN_MLT	
R-0h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-180. Port n ALE Unknown Multicast Destination Register (STATn_ALE_UNKN_MLT) Field Descriptions

Bits	Field	Description
31-0	ALE_UNKN_MLT	The total number of frames received on the port that had a multicast destination address with an unknown source address. Such a frame must match all of the following criteria: • The frame was any data frame with a multicast destination address • The frame source address was not an ALE table entry • The frame was of length 64 to RX_MAXLEN bytes inclusive • The frame had no CRC error, alignment error, or code error

3.5.3.42 Port n ALE Unknown Multicast Destination Byte Count Register (STATn_ALE_UNKN_MLT_BCNT)

The ALE Unknown Multicast Destination Byte Count Register is shown in Figure 3-167 and described in Table 3-181.

Figure 3-167. Port n ALE Unknown Multicast Destination Byte Count Register (STATn_ALE_UNKN_MLT_BCNT)

31	0
ALE_UNKN_MLT_BCNT	
R-0h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-181. Port n ALE Unknown Multicast Destination Byte Count Register (STATn_ALE_UNKN_MLT_BCNT) Field Descriptions

Bits	Field	Description
31-0	ALE_UNKN_MLT_BCNT	The total number of bytes contained in the ALE Unknown Multicast frames (STATn_ALE_UNKN_MLT register).

3.5.3.43 Port n ALE Unknown Broadcast Destination Register (STATn_ALE_UNKN_BRD)

The ALE Unknown Broadcast Destination Register is shown in Figure 3-168 and described in Table 3-182.

Figure 3-168. Port n ALE Unknown Broadcast Destination Register (STATn_ALE_UNKN_BRD)

31	0
ALE_UNKN_BRD	
R-0h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-182. Port n ALE Unknown Broadcast Destination Register (STATn_ALE_UNKN_BRD) Field Descriptions

Bits	Field	Description
31-0	ALE_UNKN_BRD	The total number of frames received on the port that had a broadcast destination address with an unknown source address. Such a frame must match all of the following criteria: • The frame was any data frame with a broadcast destination address • The frame source address was not an ALE table entry • The frame was of length 64 to RX_MAXLEN bytes inclusive • The frame had no CRC error, alignment error, or code error

3.5.3.44 Port n ALE Unknown Broadcast Destination Byte Count Register (STATn_ALE_UNKN_BRD_BCNT)

The ALE Unknown Broadcast Destination Byte Count Register is shown in Figure 3-169 and described in Table 3-183.

Figure 3-169. Port n ALE Unknown Broadcast Destination Byte Count Register (STATn_ALE_UNKN_BRD_BCNT)

31	0
ALE_UNKN_BRD_BCNT	
R-0h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

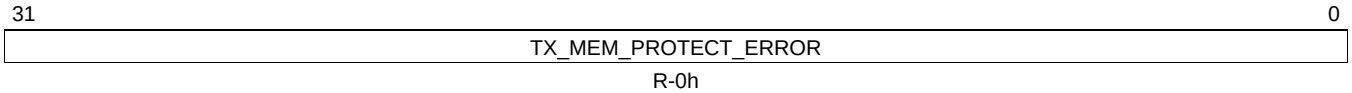
Table 3-183. Port n ALE Unknown Broadcast Destination Byte Count Register (STATn_ALE_UNKN_BRD_BCNT) Field Descriptions

Bits	Field	Description
31-0	ALE_UNKN_BRD_BCNT	The total number of bytes contained in the ALE Unknown Broadcast frames (STATn_ALE_UNKN_BRD register).

3.5.3.45 Port n Transmit Memory Protect Error Frames Register (STATn_TX_MEM_PROTECT_ERROR)

The Transmit Memory Protect Error Frames Register is shown in Figure 3-170 and described in Table 3-184.

Figure 3-170. Port n Transmit Memory Protect Error Frames Register (STATn_TX_MEM_PROTECT_ERROR)



Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-184. Port n Transmit Memory Protect Error Frames Register (STATn_TX_MEM_PROTECT_ERROR) Field Descriptions

Bits	Field	Description
31-0	TX_MEM_PROTECT_ERROR	The total number of transmit frames on the port that had a memory protect CRC error on egress. Such a frame must match all of the following criteria: • Any frame destined to be transmitted • The frame was any length, including length less than 64 bytes or greater than RX_MAXLEN bytes • The frame had a memory protect CRC error on egress

3.5.3.46 Port n Transmit Priority m Frames Register (STATn_TX_PRIm)

The Transmit Priority m Frames Register is shown in Figure 3-171 and described in Table 3-185. Each port (n = 0 to 4 in a 5 port switch or n = 0 to 8 in a 9 port switch) has one register for each of the eight priorities (m = 0 to 7).

Figure 3-171. Port n Transmit Priority m Frames Register (STATn_TX_PRIm)

31	0
TX_PRIm	
R-0h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-185. Port n Transmit Priority m Frames Register (STATn_TX_PRIm) Field Descriptions

Bits	Field	Description
31-0	TX_PRIm	The total number of transmit frames on the port from transmit FIFO priority m where m = 0 to 7. Such a frame must match all of the following criteria: • Any frame transmitted from priority m where m = 0 to 7 • The frame was any length, including length less than 64 bytes or greater than RX_MAXLEN bytes • Collision retries are not counted in this statistic • Pause frames are not counted in this statistic • Carrier sense errors do not affect this statistic

3.5.3.47 Port n Transmit Priority m Frames Byte Count Register (STATn_TX_PRIm_BCNT)

The Transmit Priority m Frames Byte Count Register is shown in Figure 3-172 and described in Table 3-186. Each port (n = 0 to 4 in a 5 port switch or n = 0 to 8 in a 9 port switch) has one byte count register for each of the eight priorities (m = 0 to 7).

Figure 3-172. Port n Transmit Priority m Frames Byte Count Register (STATn_TX_PRIm_BCNT)

31	0
TX_PRIm_BCNT	
R-0h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-186. Port n Transmit Priority m Frames Byte Count Register (STATn_TX_PRIm_BCNT) Field Descriptions

Bits	Field	Description
31-0	TX_PRIm_BCNT	The total number of bytes contained in the Transmit Priority m Frames (STATn_TX_PRIm register).

3.5.3.48 Port n Transmit Priority m Drop Frames Register (STATn_TX_PRIm_DROP)

The Transmit Priority m Drop Frames Register is shown in Figure 3-173 and described in Table 3-187. Each port (n = 0 to 4 in a 5 port switch or n = 0 to 8 in a 9 port switch) has one register for each of the eight priorities (m = 0 to 7).

Figure 3-173. Port n Transmit Priority m Drop Frames Register (STATn_TX_PRIm_DROP)

31	0
TX_PRIm_DROP	
R-0h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-187. Port n Transmit Priority m Drop Frames Register (STATn_TX_PRIm_DROP) Field Descriptions

Bits	Field	Description
31-0	TX_PRIm _DROP	The total number of transmit frames on the port that overran the transmit FIFO priority m (where m = 0 to 7) and were dropped. Such a frame must match all of the following criteria: • Any frame destined to be transmitted from priority m where m = 0 to 7 • The frame was any length, including length less than 64 bytes or greater than RX_MAXLEN bytes • The frame was dropped due to priority m (where m = 0 to 7) FIFO overrun (start of packet overrun)

3.5.3.49 Port n Transmit Priority m Drop Frames Byte Count Register (STATn_TX_PRIm_DROP_BCNT)

The Transmit Priority m Drop Frames Byte Count Register is shown in Figure 3-174 and described in Table 3-188. Each port (n = 0 to 4 in a 5 port switch or n = 0 to 8 in a 9 port switch) has one byte count register for each of the eight priorities (m = 0 to 7).

Figure 3-174. Port n Transmit Priority m Drop Frames Byte Count Register (STATn_TX_PRIm_DROP_BCNT)

31	0
TX_PRIm_DROP_BCNT	
R-0h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-188. Port n Transmit Priority m Drop Frames Byte Count Register (STATn_TX_PRIm_DROP_BCNT) Field Descriptions

Bits	Field	Description
31-0	TX_PRIm_DROP_BCNT	The total number of bytes contained in the Transmit Priority m Drop Frames (STATn_TX_PRIm_DROP register).

3.5.4 Time Synchronization (CPTS) Submodule

This section describes the registers available in the Time Synchronization (CPTS) submodule.

There is one CPTS submodule in the Ethernet switch module for time synchronization. The register offset addresses listed in this section in Table 3-189 are relative to the CPTS submodule. See Table 3-1 for the offset address of the CPTS submodule. A complete list of all of the registers in the GbE switch subsystem is provided in Table 3-2.

Table 3-189 lists the registers in the CPTS submodule and the corresponding offset address for each register.

Table 3-189. CPTS Registers

Offset Address[(1)]	Acronym	Register Name	Section
00h	CPTS_IDVER	Identification and Version Register	Section 3.5.4.1
04h	CPTS_CTL	Time Sync Control Register	Section 3.5.4.2
08h	CPTS_RFTCLK_SEL	Reference Clock Select Register	Section 3.5.4.3
0Ch	CPTS_TS_PUSH	Time Stamp Event Push Register	Section 3.5.4.4
10h	CPTS_TS_LOAD_VAL_L	Time Stamp Load Value Register (lower 32 bits)	Section 3.5.4.5
14h	CPTS_TS_LOAD_EN	Time Stamp Load Enable Register	Section 3.5.4.6
18h	CPTS_TS_COMP_VAL_L	Time Stamp Comparison Value Register (lower 32 bits)	Section 3.5.4.7
1Ch	CPTS_TS_COMP_LENGTH	Time Stamp Comparison Length Register	Section 3.5.4.8
20h	CPTS_INTSTAT_RAW	Interrupt Status Raw Register	Section 3.5.4.9
24h	CPTS_INTSTAT_MASKED	Interrupt Status Masked Register	Section 3.5.4.10
28h	CPTS_INT_ENABLE	Interrupt Enable Register	Section 3.5.4.11
2Ch	Reserved	Reserved	Reserved
30h	CPTS_EVENT_POP	Event Interrupt Pop Register	Section 3.5.4.12
34h	CPTS_EVENT_INFO0	Lower 32-bits of the Event Timestamp Value	Section 3.5.4.13
38h	CPTS_EVENT_INFO1	Event Information Register	Section 3.5.4.14
3Ch	CPTS_EVENT_INFO2	Additional Event Information Register	Section 3.5.4.15
40h	CPTS_EVENT_INFO3	Upper 32-bits of the Event Timestamp Value (64-bit mode only)	Section 3.5.4.16
44h	CPTS_TS_LOAD_VAL_H	Time Stamp Load Value Register (upper 32 bits)	Section 3.5.4.17
48h	CPTS_TS_COMP_VAL_H	Time Stamp Comparison Value Register (upper 32 bits)	Section 3.5.4.18
4Ch-FCh	Reserved	Reserved	Reserved

(1) The actual addresses of these registers are device specific. See your device-specific data manual to verify the register addresses.

3.5.4.1 CPTS Identification and Version Register (CPTS_IDVER)

The CPTS Identification And Version Register is shown in Figure 3-175 and described in Table 3-190.

Figure 3-175. CPTS Identification and Version Register (CPTS_IDVER)

31	16
CPTS_IDENT	
R-4E8Ah	

15	11	10	8	7	0
CPTS_RTL_VER		CPTS_MAJOR_VER		CPTS_MINOR_VER	
R-0h		R-1h		R-6h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-190. CPTS Identification and Version Register (CPTS_IDVER) Field Descriptions

Bits	Field	Description
31-16	CPTS_IDENT	CPTS Identification Value
15-11	CPTS_RTL_VER	RTL Version Value
10-8	CPTS_MAJOR_VER	Major Version Value
7-0	CPTS_MINOR_VER	Minor Version Value

3.5.4.2 Time Sync Control Register (CPTS_CTL)

The Time Sync Control Register is shown in Figure 3-176 and described in Table 3-191.

Figure 3-176. Time Sync Control Register (CPTS_CTL)

31	28	27	16	15	14	13	12	11	10
TS_SYNC_SEL		Reserved		HW8_PUSH_EN	HW7_PUSH_EN	HW6_PUSH_EN	HW5_PUSH_EN	HW4_PUSH_EN	HW3_PUSH_EN
R/W-0h		R-0h		R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

9	8	7	6	5	4	3	2	1	0
HW2_PUSH_EN	HW1_PUSH_EN	Reserved		64_BIT	SEQ_EN	HR_EN	TS_COMP_POL	INT_TEST	CPTS_EN
R/W-0h	R/W-0h	R-0h		R/W-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-191. Time Sync Control Register (CPTS_CTL) Field Descriptions

Bits	Field	Description
31-28	TS_SYNC_SEL	TS_SYNC Output Timestamp Counter Bit Select • 0000 = TS_SYNC output is disabled • 0001 = TS_SYNC output is enabled and is selected from time stamp counter bit 17 • 0010 = TS_SYNC output is enabled and is selected from time stamp counter bit 18 • ... • 1110 = TS_SYNC output is enabled and is selected from time stamp counter bit 30 • 1111 = TS_SYNC output is enabled and is selected from time stamp counter bit 31
27-16	Reserved	Reserved
15	HW8_PUSH_EN	Hardware Timestamp Push Event 8 Enable.
14	HW7_PUSH_EN	Hardware Timestamp Push Event 7 Enable.
13	HW6_PUSH_EN	Hardware Timestamp Push Event 6 Enable.
12	HW5_PUSH_EN	Hardware Timestamp Push Event 5 Enable.
11	HW4_PUSH_EN	Hardware Timestamp Push Event 4 Enable.
10	HW3_PUSH_EN	Hardware Timestamp Push Event 3 Enable.
9	HW2_PUSH_EN	Hardware Timestamp Push Event 2 Enable.
8	HW1_PUSH_EN	Hardware Timestamp Push Event 1 Enable.
7-6	Reserved	Reserved
5	64_BIT	64-Bit Mode Enable. • 0 = The timestamp is 32-bits with the upper 32-bits forced to zero • 1 = The timestamp is 64-bits
4	SEQ_EN	Sequence Enable. • 0 = The timestamp value increments with the selected RFTCLK • 1 = The timestamp for received packets is the sequence number of the received packet (first packet is 0, second packet is 1, and so on)
3	HR_EN	Host Receive Timestamp Enable. • 0 = Timestamps are disabled on received packets to the host • 1 = Timestamps are enabled on received packets to the host (CPTS_EN must also be set to 1)
2	TS_COMP_POL	TS_COMP Polarity. • 0 = TS_COMP is asserted low • 1 = TS_COMP is asserted high
1	INT_TEST	Interrupt Testing Enable. When set to 1, this bit allows the raw interrupt (TS_PEND_RAW bit in the CPTS_INTSTAT_RAW register) to be written to facilitate interrupt testing.
0	CPTS_EN	Time Sync Enable. When disabled (cleared to 0), the CPTS_RCLK domain is held in reset. • 0 = Time Sync Disabled • 1 = Time Sync Enabled

3.5.4.3 RFTCLK Select Register (CPTS_RFTCLK_SEL)

The CPTS_RFTCLK_SEL Select Register is shown in Figure 3-177 and described in Table 3-192.

Figure 3-177. RFTCLK Select Register (CPTS_RFTCLK_SEL)

31	5	4	0
Reserved		CPTS_RFTCLK_SEL	
R-0h		R/W-0h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-192. RFTCLK Select Register (CPTS_RFTCLK_SEL) Field Descriptions

Bits	Field	Description
31-5	Reserved	Reserved
4-0	CPTS_RFTCLK_SEL	Reference Clock Select. This signal is used to control an external multiplexer that selects one of up to 32 clocks for time sync reference (RFTCLK). This CPTS_RFTCLK_SEL value can be written only when both the CPTS_EN and HR_EN bits are both cleared to 0 in the TS_CTL register. For more information on the clock sources for this module, please see the device specific data manual.

3.5.4.4 Time Stamp Event Push Register (CPTS_TS_PUSH)

The Time Stamp Event Push Register is shown in Figure 3-178 and described in Table 3-193.

Figure 3-178. Time Stamp Event Push Register (CPTS_TS_PUSH)

31	1	0
Reserved		TS_PUSH
R-0h		R/W-0h

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-193. Time Stamp Event Push Register (CPTS_TS_PUSH) Field Descriptions

Bits	Field	Description
31-1	Reserved	Reserved
0	TS_PUSH	Time Stamp Event Push. When a logic high is written to this bit a time stamp event is pushed onto the event FIFO. The time stamp value is the time of the write of this register, not the time of the event read. The time stamp value can then be read on interrupt via the event registers. Software should not push a second time stamp event onto the event FIFO until the first time stamp value has been read from the event FIFO (there should be only one time stamp event in the event FIFO at any given time). This bit is write only and always reads 0.

3.5.4.5 Time Stamp Load Value Register (lower 32 bits) (CPTS_TS_LOAD_VAL_L)

The Time Stamp Load Value Register (lower 32 bits) is shown in Figure 3-179 and described in Table 3-194.

Figure 3-179. Time Stamp Load Value Register (lower 32 bits) (CPTS_TS_LOAD_VAL_L)

31	0
TS_LOAD_VAL_L	
R/W-0h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-194. Time Stamp Load Value Register (lower 32 bits) (CPTS_TS_LOAD_VAL_L) Field Descriptions

Bits	Field	Description
31-0	TS_LOAD_VAL_L	Time Stamp Load Low Value. Writing the TS_LOAD_EN bit in the CPTS_TS_LOAD_EN register causes TS_LOAD_VAL_L (and TS_LOAD_VAL_H when in 64 bit mode) to be written into the time stamp. The time stamp value is read by initiating a time stamp push event, not by reading this register. When reading this register, the value read is not the time stamp, but is the value that was last written to this register.

3.5.4.6 Time Stamp Load Enable Register (CPTS_TS_LOAD_EN)

The Time Stamp Load Enable Register is shown in Figure 3-180 and described in Table 3-195.

Figure 3-180. Time Stamp Load Enable Register (CPTS_TS_LOAD_EN)

31	1	0
Reserved		TS_LOAD_EN
R-0h		W-0h

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-195. Time Stamp Load Enable Register (CPTS_TS_LOAD_EN) Field Descriptions

Bits	Field	Description
31-1	Reserved	Reserved
0	TS_LOAD_EN	Time Stamp Load Enable Register. Writing a one to this bit enables the time stamp value to be written with the value in TS_LOAD_VAL_L (and TS_LOAD_VAL_H in 64 bit mode). This bit is write only and will be cleared by the hardware after one clock. The upper 32 bits of the timestamp are forced to 0 in 32 bit mode.

3.5.4.7 Time Stamp Comparison Value Register (lower 32 bits) (CPTS_TS_COMP_VAL_L)

The Time Stamp Comparison Value Register (lower 32 bits) is shown in Figure 3-181 and described in Table 3-196.

Figure 3-181. Time Stamp Comparison Value Register (lower 32 bits) (CPTS_TS_COMP_VAL_L)

31	0
TS_COMP_VAL_L	
R/W-0h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-196. Time Stamp Comparison Value Register (lower 32 bits) (CPTS_TS_COMP_VAL_L) Field Descriptions

Bits	Field	Description
31-0	TS_COMP_VAL_L	Time Stamp Comparison Low Value. Writing a non-zero value to the TS_COMP_LENGTH bits in the CPTS_TS_COMP_LENGTH register causes a pulse of TS_COMP_LENGTH CPTS_RCLK periods on the TS_COMP output as well as a comparison event when the time stamp counter value is equivalent to the TS_COMP_VAL_L (combined with the TS_COMP_VAL_H bits when in 64 bit mode).

3.5.4.8 Time Stamp Comparison Length Register (CPTS_TS_COMP_LENGTH)

The Time Stamp Comparison Length Register is shown in Figure 3-182 and described in Table 3-197.

Figure 3-182. Time Stamp Comparison Length Register (CPTS_TS_COMP_LENGTH)

31	16	15	0
Reserved		TS_COMP_LENGTH	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-197. Time Stamp Comparison Length Register (CPTS_TS_COMP_LENGTH) Field Descriptions

Bits	Field	Description
31-16	Reserved	Reserved
15-0	TS_COMP_LENGTH	Time Stamp Comparison Length. This value determines how many cycles the TS_COMP output signal will be asserted when a Timestamp Compare Event occurs. Writing a non-zero value to this field enables the time stamp comparison event and TS_COMP signal output. This value should be 0 while the TS_COMP_VAL_L and TS_COMP_VAL_H values are being written.

3.5.4.9 Interrupt Status Raw Register (CPTS_INTSTAT_RAW)

The Interrupt Status Raw Register is shown in Figure 3-183 and described in Table 3-198.

Figure 3-183. Interrupt Status Raw Register (CPTS_INTSTAT_RAW)

31	1	0
Reserved		TS_PEND_RAW
R-0h		R/W-0h

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-198. Interrupt Status Raw Register (CPTS_INTSTAT_RAW) Field Descriptions

Bits	Field	Description
31-1	Reserved	Reserved
0	TS_PEND_RAW	Time Sync Raw Pending Interrupt Register. A 1 in this bit indicates that there is one or more events in the event FIFO. This bit is writable when INT_TEST is set to 1 in the CPTS_CTL register.

3.5.4.10 Interrupt Status Masked Register (CPTS_INTSTAT_MASKED)

The Interrupt Status Masked Register is shown in Figure 3-184 and described in Table 3-199.

Figure 3-184. Interrupt Status Masked Register (CPTS_INTSTAT_MASKED)

31	1	0
Reserved		TS_PEND
R-0h		R-0h

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-199. Interrupt Status Masked Register (CPTS_INTSTAT_MASKED) Field Descriptions

Bits	Field	Description
31-1	Reserved	Reserved.
0	TS_PEND	Time Sync Masked Pending Interrupt Register. Masked interrupt read (after enable).

3.5.4.11 Interrupt Enable Register (CPTS_INT_ENABLE)

The Interrupt Enable Register is shown in Figure 3-185 and described in Table 3-200.

Figure 3-185. Interrupt Enable Register (CPTS_INT_ENABLE)

31	1	0
Reserved		TS_PEND_EN
R-0h		R/W-0h

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-200. Interrupt Enable Register (CPTS_INT_ENABLE) Field Descriptions

Bits	Field	Description
31-1	Reserved	Reserved
0	TS_PEND_EN	Time Sync Interrupt Enable Register. Enables time sync masked interrupts.

3.5.4.12 Event Pop Register (CPTS_EVENT_POP)

The Event Pop Register is shown in Figure 3-186 and described in Table 3-201.

Figure 3-186. Event Pop Register (CPTS_EVENT_POP)

31	1	0
Reserved		EVENT_POP
R-0h		W-0h

Legend: R = Read only; W = Write only; R/W = Read/Write; - *n* = value after reset

Table 3-201. Event Pop Register (CPTS_EVENT_POP) Field Descriptions

Bits	Field	Description
31-1	Reserved	Reserved
0	EVENT_POP	Event Pop. When a logic high is written to this bit an event is popped off the event FIFO. The event FIFO pop occurs as part of the interrupt process after the event has been read in the CPTS_EVENT0-CPTS_EVENT3 registers. Popping an event discards the event and causes the next event, if any, to be moved to the top of the FIFO ready to be read by software on interrupt.

3.5.4.13 Event Information 0 Register (CPTS_EVENT_INFO0)

The Event Information 0 Register is shown in Figure 3-187 and described in Table 3-202.

Figure 3-187. Event Information 0 Register (CPTS_EVENT_INFO0)

31	0
TIME_STAMP_L	
R-x	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

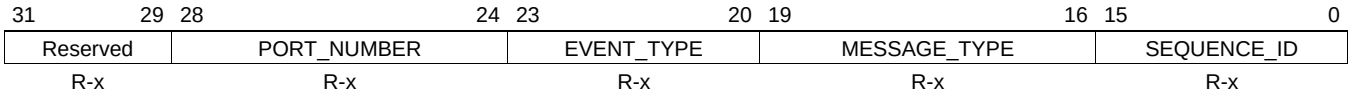
Table 3-202. Event Information 0 Register (CPTS_EVENT_INFO0) Field Descriptions

Bits	Field	Description
31-0	TIME_STAMP_L	Lower 32 Bits of Time Stamp. The timestamp is valid for transmit, receive, and time stamp push event types. The timestamp value is not valid for counter roll event types.

3.5.4.14 Event Information 1 Register (CPTS_EVENT_INFO1)

The Event Information 1 Register is shown in Figure 3-188 and described in Table 3-203.

Figure 3-188. Event Information 1 Register (CPTS_EVENT_INFO1)



Legend: N/A = Not applicable - there are no reset values for this register

Table 3-203. Event Information 1 Register (CPTS_EVENT_INFO1) Field Descriptions

Bits	Field	Description
31-29	Reserved	Reserved
28-24	PORT_NUMBER	Indicates the port number (encoded) of an Ethernet event or the encoded hardware timestamp number.
23-20	EVENT_TYPE	Time Sync Event Type. • 0000 = Time Stamp Push Event • 0001 = Time Stamp Rollover Event (32-bit mode only) • 0010 = Time Stamp Half Rollover Event (32-bit mode only) • 0011 = Hardware Time Stamp Push Event • 0100 = Ethernet Receive Event • 0101 = Ethernet Transmit Event • 0110 = Time Stamp Compare Event • 0111 = Host Transmit Event • 1000 -1111 = Reserved
19-16	MESSAGE_TYPE	Message Type. The message type value that was contained in an Ethernet transmit or receive time sync packet. This field is valid only for Ethernet transmit or receive events.
15-0	SEQUENCE_ID	Sequence ID. The 16-bit sequence ID is the value that was contained in an Ethernet transmit or receive time sync packet. This field is valid only for Ethernet transmit or receive events.

3.5.4.15 Event Information 2 Register (CPTS_EVENT_INFO2)

The Event Information 2 Register is shown in Figure 3-189 and described in Table 3-204.

Figure 3-189. Event Information 2 Register (CPTS_EVENT_INFO2)

31	8	7	0
Reserved		DOMAIN	
R-x		R-x	

Legend: N/A = Not applicable - there are no reset values for this register

Table 3-204. Event Information 2 Register (CPTS_EVENT_INFO2) Field Descriptions

Bits	Field	Description
31-8	Reserved	Reserved
7-0	DOMAIN	Domain. The 8-bit domain is the value that was contained in an Ethernet transmit or receive time sync packet. This field is valid only for Ethernet transmit or receive events.

3.5.4.16 Event Information 3 Register (CPTS_EVENT_INFO3)

The Event Information 3 Register is shown in Figure 3-190 and described in Table 3-205.

Figure 3-190. Event Information 3 Register (CPTS_EVENT_INFO3)

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-205. Event Information 3 Register (CPTS_EVENT_INFO3) Field Descriptions

Bits	Field	Description
31-0	TIME_STAMP_H	Upper 32 Bits of Time Stamp. The timestamp is valid for transmit, receive, and time stamp push event types. The timestamp value is not valid for counter roll event types.

3.5.4.17 Time Stamp Load Value Register (upper 32 bits) (CPTS_TS_LOAD_VAL_H)

The Time Stamp Load Value Register (upper 32 bits) is shown in Figure 3-191 and described in Table 3-206.

Figure 3-191. Time Stamp Load Value Register (upper 32 bits) (CPTS_TS_LOAD_VAL_H)

31	0
TS_LOAD_VAL_H	
R/W-0h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-206. Time Stamp Load Value Register (upper 32 bits) (CPTS_TS_LOAD_VAL_H) Field Descriptions

Bits	Field	Description
31-0	TS_LOAD_VAL_H	Time Stamp Load High Value. Writing the TS_LOAD_EN bit in the CPTS_TS_LOAD_EN register causes TS_LOAD_VAL_L (and TS_LOAD_VAL_H when in 64 bit mode) to be written into the time stamp. The time stamp value is read by initiating a time stamp push event, not by reading this register. When reading this register, the value read is not the time stamp, but is the value that was last written to this register. This register is unused in 32-bit mode.

3.5.4.18 Time Stamp Comparison Value Register (upper 32 bits) (CPTS_TS_COMP_VAL_H)

The Time Stamp Comparison Value Register (upper 32 bits) is shown in Figure 3-192 and described in Table 3-207.

Figure 3-192. Time Stamp Comparison Value Register (upper 32 bits) (CPTS_TS_COMP_VAL_H)

31	0
TS_COMP_VAL_H	
R/W-0h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-207. Time Stamp Comparison Value Register (upper 32 bits) (CPTS_TS_COMP_VAL_H) Field Descriptions

Bits	Field	Description
31-0	TS_COMP_VAL_H	Time Stamp Comparison High Value. Writing a non-zero value to the TS_COMP_LENGTH bits in the CPTS_TS_COMP_LENGTH register causes a pulse of TS_COMP_LENGTH CPTS_RCLK periods on the TS_COMP output as well as a comparison event when the time stamp counter value is equivalent to the TS_COMP_VAL_L (combined with the TS_COMP_VAL_H bits when in 64 bit mode). This register is unused in 32-bit mode. The upper 32 bits in this register should be written before the lower 32 bits in the CPTS_TS_COMP_VAL_L register.

3.5.5 Address Lookup Engine (ALE) submodule

This section describes the registers available in the Address Lookup Engine (ALE) submodule.

There is one ALE submodule in the Ethernet switch module for packet routing and forwarding. The register offset addresses listed in this section in Table 3-208 are relative to the ALE submodule. See for the offset address of the ALE submodule. A complete list of all of the registers in the GbE switch subsystem is provided in (KeyStone I) and in (KeyStone II).

There is one ALE submodule in the Ethernet switch module for packet routing and forwarding. The register offset addresses listed in this section in Table 3-208 are relative to the ALE submodule. See Table 3-1 for the offset address of the ALE submodule. A complete list of all of the registers in the GbE switch subsystem is provided in Table 3-2.

Table 3-208 lists the registers in the ALE submodule and the corresponding offset address for each register.

Table 3-208. ALE Registers

Offset Address[(1)]	Register Mnemonic	Register Name	Section
00h	ALE_IDVER	Address Lookup Engine ID/Version Register	Section 3.5.5.1
04h	ALE_STATUS	Address Lookup Engine Status Register	Section 3.5.5.2
08h	ALE_CONTROL	Address Lookup Engine Control Register	Section 3.5.5.3
0Ch	Reserved	Reserved	Reserved
10h	ALE_PRESCALE	Address Lookup Engine Prescale Register	Section 3.5.5.4
14h	ALE_AGING_TIMER	Address Lookup Engine Aging Timer Register	Section 3.5.5.5
18h-1Ch	Reserved	Reserved	Reserved
20h	ALE_TBLCTL	Address Lookup Engine Table Control	Section 3.5.5.7
24h-30h	Reserved	Reserved	Reserved
34h	ALE_TBLW2	Address Lookup Engine Table Word 2 Register	Section 3.5.5.8
38h	ALE_TBLW1	Address Lookup Engine Table Word 1 Register	Section 3.5.5.9
3Ch	ALE_TBLW0	Address Lookup Engine Table Word 0 Register	Section 3.5.5.10
40h	ALE_PORTCTL0	Address Lookup Engine Port 0 Control Register	Section 3.5.5.11
44h	ALE_PORTCTL1	Address Lookup Engine Port 1 Control Register	Section 3.5.5.11
48h	ALE_PORTCTL2	Address Lookup Engine Port 2 Control Register	Section 3.5.5.11
4Ch	ALE_PORTCTL3	Address Lookup Engine Port 3 Control Register	Section 3.5.5.11
50h	ALE_PORTCTL4	Address Lookup Engine Port 4 Control Register	Section 3.5.5.11
54h	ALE_PORTCTL5	Address Lookup Engine Port 5 Control Register	Section 3.5.5.11
58h	ALE_PORTCTL6	Address Lookup Engine Port 6 Control Register	Section 3.5.5.11
5Ch	ALE_PORTCTL7	Address Lookup Engine Port 7 Control Register	Section 3.5.5.11
60h	ALE_PORTCTL8	Address Lookup Engine Port 8 Control Register	Section 3.5.5.11
64h-8Ch	Reserved	Reserved	Reserved
90h	ALE_UNKN_VLAN_MBR_LIST	Address Lookup Engine Unknown VLAN Member List Register	Section 3.5.5.12
94h	ALE_UNKN_VLAN_MLT_FLOOD	Address Lookup Engine Unknown VLAN Multicast Flood Mask Register	Section 3.5.5.13
98h	ALE_UNKN_VLAN_REG_MLT_FLOOD	Address Lookup Engine Unknown VLAN Registered Multicast Flood Mask Register	Section 3.5.5.14
9Ch	ALE_UNKN_VLAN_FORCE_UNTAG_EGR	Address Lookup Engine Unknown VLAN Force Untagged Egress Register	Section 3.5.5.15
A0h-BCh	Reserved	Reserved	Reserved
C0h	ALE_VLAN_MASK_MUX0	Address Lookup Engine Mask Mux 0 Select Register	Section 3.5.5.16
C4h	ALE_VLAN_MASK_MUX1	Address Lookup Engine Mask Mux 1 Select Register	Section 3.5.5.16
C8h	ALE_VLAN_MASK_MUX2	Address Lookup Engine Mask Mux 2 Select Register	Section 3.5.5.16

(1) The actual addresses of these registers are device specific. See your device-specific data manual to verify the register addresses.

Table 3-208. ALE Registers (continued)

Offset Address[(1)]	Register Mnemonic	Register Name	Section
CCh	ALE_VLAN_MASK_MUX3	Address Lookup Engine Mask Mux 3 Select Register	Section 3.5.5.16
D0h	ALE_VLAN_MASK_MUX4	Address Lookup Engine Mask Mux 4 Select Register	Section 3.5.5.16
D4h	ALE_VLAN_MASK_MUX5	Address Lookup Engine Mask Mux 5 Select Register	Section 3.5.5.16
D8h	ALE_VLAN_MASK_MUX6	Address Lookup Engine Mask Mux 6 Select Register	Section 3.5.5.16
DCh	ALE_VLAN_MASK_MUX7	Address Lookup Engine Mask Mux 7 Select Register	Section 3.5.5.16
E0h-FCh	Reserved	Reserved	Reserved

3.5.5.1 ALE Identification and Version Register (ALE_IDVER)

The ALE Identification And Version Register is shown in Figure 3-193 and described in Table 3-209.

Figure 3-193. ALE Identification and Version Register (ALE_IDVER)

31	16
ALE_IDENT	
R-29h	

15	11	10	8	7	0
ALE_RTL_VER		ALE_MAJOR_VER		ALE_MINOR_VER	
R-2h		R-1h		R-4h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

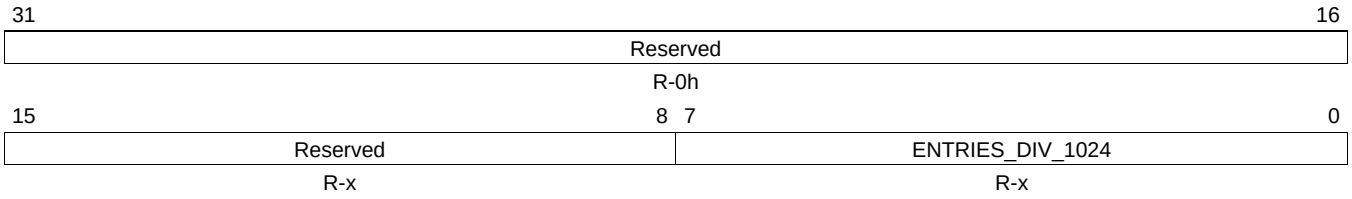
Table 3-209. ALE Identification and Version Register (ALE_IDVER) Field Descriptions

Bits	Field	Description
31-16	ALE_IDENT	ALE Identification Value.
15-11	ALE_RTL_VER	ALE RTL Version Value.
10-8	ALE_MAJ_VER	ALE Major Version Value.
7-0	ALE_MINOR_VER	ALE Minor Version Value.

3.5.5.2 ALE Status Register (ALE_STATUS)

The ALE Status Register is shown in Figure 3-194 and described in Table 3-210.

Figure 3-194. ALE Status Register (ALE_STATUS)



Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-210. ALE Status Register (ALE_STATUS) Field Descriptions

Bits	Field	Description
31-8	Reserved	Reserved
7-0	ENTRIES_DIV_1024	This is the number of table entries total divided by 1024. For example, a value of 1 indicates 1024 table entries and a value of 8 indicates 8192 table entries.

3.5.5.3 ALE Control Register (ALE_CONTROL)

The ALE Control Register is shown in Figure 3-195 and described in Table 3-211.

Figure 3-195. ALE Control Register (ALE_CONTROL)

31	30	29	28 24	23 21	20 14	13	12 9
ENABLE_ALE	CLEAR_TABLE	AGE_OUT _NOW	Reserved	UPD_BW _CTRL	Reserved	UNK_VLAN_NL	Reserved
R/W-0h	R/W-0h	R/W-0h	R-0h	R/W-0h	R-0h	R/W-0h	R-0h

8	7	6	5	4	3	2	1	0
UNI_FLD _HOST	LEARN_NO _VID	EN_VID0 _MODE	EN_OUI_DENY	ALE_BYPASS	RL_TX	ALE_VLAN_AWARE	EN_ AM	EN_ RL
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-211. ALE Control Register (ALE_CONTROL) Field Descriptions

Bits	Field	Description
31	ENABLE_ALE	Enable ALE. • 0 = Drop all packets. • 1 = Enable ALE packet processing.
30	CLEAR_TABLE	Clear ALE address table. Setting this bit causes the ALE hardware to write all table bit values to 0. Software must perform a clear table operation as part of the ALE setup/configuration process. Setting this bit causes all ALE accesses to be held up for 64 clocks while the clear is performed. Access to all ALE registers will be blocked (wait states) until the 64 clocks have completed. This bit cannot be read as 1 because the read is blocked until the clear table is completed, at which time this bit is cleared to 0.
29	AGE_OUT_NOW	Age Out Address Table Now. Setting this bit causes the ALE hardware to remove (free up) any ageable table entry that does not have a set touch bit. This bit is cleared when the age out process has completed. This bit may be read. The age out process takes a minimum of 4096 clock cycles best case (no ale packet processing during ageout) and a maximum of 66550 clock cycles worst case.
28 - 24	Reserved	Reserved
23-21	UPD_BW_CTRL	The UPD_BW_CTRL field allows for up to 8 times the rate in which adds, updates, touches, writes, and aging updates can occur. At frequencies of 350Mhz, the table update rate should be at its lowest or 5 Million updates per second. When operating the switch core at frequencies or above, the UPD_BW_CTRL can be programmed more aggressive. If the UPD_BW_CTRL is set but the frequency of the switch subsystem is below the associated value, ALE will drop packets due to insufficient time to complete lookup under high traffic loads. • 0 - 350Mhz, 5M • 1 - 359Mhz, 11M • 2 - 367Mhz, 16M • 3 - 375Mhz, 22M • 4 - 384Mhz, 28M • 5 - 392Mhz, 34M • 6 - 400Mhz, 39M • 7 - 409Mhz, 45M
20-14	Reserved	Reserved
13	UVLAN_NO_LEARN	Unknown VLAN No Learn. When set to 1 this will prevent source addresses of unknown VLAN IDs from being automatically added into the lookup table if learning is enabled.
12-9	Reserved	Reserved
8	UNI_FLOOD_TO_HOST	Unknown Unicast Packets Flood to Host. • 0 - Unknown unicast packets are dropped to the host. • 1 - Unknown unicast packets flood to the host also.
7	LEARN_NO_VID	Learn No VID. • 0 = VID is learned with the source address. • 1 = VID is not learned with the source address (source address is not tied to VID). This determines the entry type that is created in the ALE table.

Table 3-211. ALE Control Register (ALE_CONTROL) Field Descriptions (continued)

Bits	Field	Description
6	EN_VID0_MODE	Enable VLAN ID = 0 Mode. • 0 = Process the priority tagged packet (that is tagged with VID = 0) with VID = PORT_VLAN[11-0]. • 1 = Process the priority tagged packet (that is tagged with VID = 0) with VID = 0.
5	EN_OUI_DENY	OUI Enable OUI Deny Mode. When set to 1, any packet with a non-matching source address will be dropped to the host unless the packet destination address matches a supervisory destination address table entry. When cleared to 0, any packet source address matching an OUI address table entry will be dropped to the host unless the destination address matches with a supervisory destination address table entry.
4	ALE_BYPASS	ALE Bypass. • 0 = ALE bypass is disabled. • 1 = ALE bypass is enabled. Packets received on non-host ports are sent to the host. Note-packets originating from the GbE switch host port (port 0) will not bypass the ALE. To bypass the ALE for packets originating from port 0, use a directed packet.
3	RL_TX	Rate Limit Transmit mode. • 0 = Broadcast and multicast rate limit counters are received port based. • 1 = Broadcast and multicast rate limit counters are transmit port based.
2	ALE_VLAN_AWARE	ALE VLAN Aware. Determines how traffic is forwarded. • 0 = Simple switch rules. • 1 = VLAN aware rules. Packets forwarded based on VLAN membership.
1	EN_AM	Enable MAC Authorization Mode. MAC authorization mode requires that all table entries be made by the host software. There are no learned addresses in authorization mode and the packet will be dropped if the source address is not found (and the destination address is not a multicast address with the SUPER table entry bit set). • 0 = The ALE is not in MAC authorization mode. • 1 = The ALE is in MAC authorization mode.
0	EN_RL	Enable Broadcast and Multicast Rate Limit. • 0 = Broadcast/Multicast rates not limited. • 1 = Broadcast/Multicast packet reception limited to the port control register rate limit fields.

3.5.5.4 ALE Prescale Register (ALE_PRESCALE)

The ALE Prescale Register is shown in Figure 3-196 and described in Table 3-212.

Figure 3-196. ALE Prescale Register (ALE_PRESCALE)

31	20	19	0
Reserved		ALE_PRESCALE	
R-0h		R/W-0h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-212. ALE Prescale Register (ALE_PRESCALE) Field Descriptions

Bits	Field	Description
31 - 20	Reserved	Reserved
19 - 0	ALE_PRESCALE	ALE Prescale Register. The input clock is divided by this value for use in the multicast/broadcast rate limiters. The minimum operating value is 10h. The prescaler is off when the value is 0.

3.5.5.5 ALE Aging Timer Register (ALE_AGING_TIMER)

The ALE Aging Timer Register is shown in Figure 3-197 and described in Table 3-213.

Figure 3-197. ALE Aging Timer Register (ALE_AGING_TIMER)

31	30	29 24	23 0
PRESCALE_1_DIS	PRESCALE_2_DIS	Reserved	ALE_AGING_TIMER
R/W-0h	R/W-0h	R-0h	R/W-0h

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-213. ALE Aging Timer Register (ALE_AGING_TIMER) Field Descriptions

Bits	Field	Description
31	PRESCALE_1_DIS	ALE Prescaler 1 Disable. When set to 1, removes 1,000 from the auto aging multiplier. This is included for test purposes.
30	PRESCALE_2_DIS	ALE Prescaler 2 Disable. When set to 1, removes 1,000 from the auto aging multiplier. This is included for test purposes.
29-24	Reserved	Reserved
23-0	ALE_AGING_TIMER	ALE Aging Timer. When non-zero, auto-aging is enabled. The ALE_AGING_TIMER value (minus 1) times 1,000,000 is the number of clock cycles after which auto-aging will automatically be initiated. If either PRESCALE_1_DIS or PRESCALE_2_DIS is set then the multiplier is 1,000 instead of 1,000,000. If both PRESCALE_1_DIS and PRESCALE_2_DIS are set then the multiplier is 1 instead of 1,000,000. Auto aging is initiated each time the count reaches zero. When the ALE_AGING_TIMER is zero, auto-aging is disabled (but software can still initiate aging by setting AGE_OUT_NOW in the ALE_CONTROL register). There is no auto-aging if ENABLE_ALE is zero in the ALE_CONTROL register, or if CLEAR_TABLE is set in the ALE_CONTROL register, or if AGE_OUT_NOW is set in the ALE_CONTROL register (while the events are occurring).

3.5.5.6 ALE Unknown VLAN Register (UNKNOWN_VLAN)

The ALE unknown VLAN register is shown in Figure 3-198 and described in Table 3-214.

Figure 3-198. ALE Unknown VLAN Register (UNKNOWN_VLAN)

31 30	29 24	23 22	21 16
Reserved	UNKNOWN_FORCE_UNTAGGED_EGRESS	Reserved	UNKNOWN_REG_MCAST_FLOOD_MASK
R-0h	R/W-0h	R-0h	R/W-0h

15 14	13 8	7 6	5 0
Reserved	UNKNOWN_MCAST_FLOOD_MASK	Reserved	UNKNOWN_VLAN_MEMBER_LIST
R-0h	R/W-0h	R-0h	R/W-0h

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-214. ALE Unknown VLAN Register (UNKNOWN_VLAN) Field Descriptions

Bits	Field	Description
31 - 30	Reserved	Reserved
29 - 24	UNKNOWN_FORCE_UNTAGGED_EGRESS	Unknown VLAN Force Untagged Egress.
23 - 22	Reserved	Reserved
21 - 16	UNKNOWN_REG_MCAST_FLOOD_MASK	Unknown VLAN Registered Multicast Flood Mask.
15 - 14	Reserved	Reserved
13 - 8	UNKNOWN_MCAST_FLOOD_MASK	Unknown VLAN Multicast Flood Mask.
7 - 6	Reserved	Reserved
5 - 0	UNKNOWN_VLAN_MEMBER_LIST	Unknown VLAN Member List.

3.5.5.7 ALE Table Control Register (ALE_TBLCTL)

The ALE Table Control Register is shown in Figure 3-199 and described in Table 3-215.

Figure 3-199. ALE Table Control Register (ALE_TBLCTL)

31	30	Y+1	Y	0
WRITE_RDZ	Reserved		ENTRY_POINTER	
R/W-0h	R-0h		R/W-0h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-215. ALE Table Control Register (ALE_TBLCTL) Field Descriptions

Bits	Field	Description
31	WRITE_RDZ	Write Bit. Writing a 1 to this bit causes the three table word register values to be written to the ENTRY_POINTER location in the address table. Writing a 0 to this bit causes the three table word register values to be loaded from the ENTRY_POINTER location in the address table so that they may be subsequently read. A read of any ALE address location will be stalled until the read or write has completed. This bit is always read as 0.
30-(Y+1)	Reserved	Reserved
Y-0	ENTRY_POINTER	Table Entry Pointer. The ENTRY_POINTER contains the table entry value that will be read/written with accesses to the table word registers. The number of entries in the ALE table determine the width of the entry pointer field (variable Y). Y = 9 for 1024 entries. Y = 12 for 8192 entries.

3.5.5.8 ALE Table Word 2 Register (ALE_TBLW2)

The ALE Table Word 2 Register is shown in Figure 3-200 and described in Table 3-216.

Figure 3-200. ALE Table Word 2 Register (ALE_TBLW2)

31	Y+1	Y	0
Reserved		ENTRY2	
R-0h		R/W-x	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

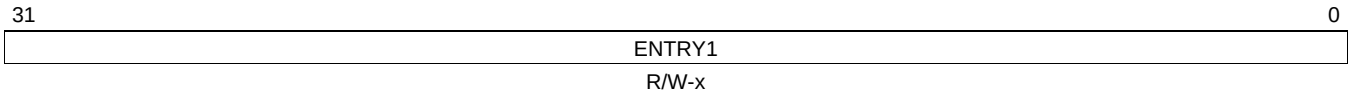
Table 3-216. ALE Table Word 2 Register (ALE_TBLW2) Field Descriptions

Bits	Field	Description
31-(Y+1)	Reserved	Reserved
Y-0	ENTRY2	Table entry bits 70-64 when using a 5 port switch (Y = 6) or table entry bits 74-64 when using a 9 port switch (Y = 10).

3.5.5.9 ALE Table Word 1 Register (ALE_TBLW1)

The ALE Table Word 1 Register is shown in Figure 3-201 and described in Table 3-217.

Figure 3-201. ALE Table Word 1 Register (ALE_TBLW1)



Legend: R = Read only; R/W = Read/Write; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-217. ALE Table Word 1 Register (ALE_TBLW2) Field Descriptions

Bits	Field	Description
31 - 0	ENTRY1	Table entry bits 63-32

3.5.5.10 ALE Table Word 0 Register (ALE_TBLW0)

The ALE Table Word 0 Register is shown in Figure 3-202 and described in Table 3-218.

Figure 3-202. ALE Table Word 0 Register (ALE_TBLW0)

31	0
ENTRY0	
R/W-x	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-218. ALE Table Word 0 Register (ALE_TBLW0) Field Descriptions

Bits	Field	Description
31 - 0	ENTRY0	Table entry bits 31-0

3.5.5.11 ALE Port Control Register (ALE_PORTCTLn)

The ALE Port Control Register n is shown in Figure 3-203 and described in Table 3-219. The variable n varies from 0 to 4 in the 5 port switch or 0 to 8 in the 9 port switch. Check you device specific data manual to see which switch your device contains.

Figure 3-203. ALE Port Control Register n (ALE_PORTCTLn)

31	24	23	16	15	13
BCAST_LIMIT		MCAST_LIMIT		Reserved	
R/W-0h		R/W-0h		R-0h	

12	11	6	5	4	3	2	1	0
DIS_AM	Reserved		NO_SA_UPDATE	NO_LEARN	VID_INGRESS_CHECK	DROP_UNTAGGED	PORT_STATE	
R/W-0h	R-0h		R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

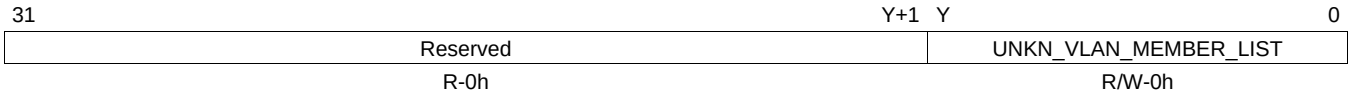
Table 3-219. ALE Port Control Register n (ALE_PORTCTLn) Field Descriptions

Bits	Field	Description
31-24	BCAST_LIMIT	Broadcast Packet Rate Limit. Each prescale pulse loads this field into the port broadcast rate limit counter. The port counters are decremented with each packet received or transmitted depending on whether the mode is transmit or receive. If the counters decrement to 0, then further packets are rate limited until the next prescale pulse. Broadcast rate limiting is enabled by a non-zero value in this field.
23-16	MCAST_LIMIT	Multicast Packet Rate Limit. Each prescale pulse loads this field into the port multicast rate limit counter. The port counters are decremented with each packet received or transmitted depending on whether the mode is transmit or receive. If the counters decrement to 0, then further packets are rate limited until the next prescale pulse. Multicast rate limiting is enabled by a non-zero value in this field.
15-13	Reserved	• Reserved
12	DIS_AM	Disable MAC Authorization Mode. When set to 1, this bit disables MAC authorization mode for this port (when the EN_AM bit in the ALE_CONTROL register is set to 1).
11-6	Reserved	• Reserved
5	NO_SA_UPDATE	No Source Address Update. When set to 1, an ingress packet on this port will not cause a matching source address entry port number to be changed (to this port). When cleared to 0, an ingress packet on this port will cause a matching source address entry port number to be changed to this port number (if it was previously a different port).
4	NO_LEARN	No Learn Mode. When set the port is disabled from learning source addresses.
3	VID_INGRESS_CHECK	VLAN ID Ingress Check. If VLAN ID is found in a VLAN table entry and the receive port is not a VLAN member then drop the packet.
2	DROP_UNTAGGED	Drop Untagged Packets. Drop non-VLAN tagged ingress packets.
1-0	PORT_STATE	Port State. • 0 = Disabled • 1 = Blocked • 2 = Learn • 3 = Forward

3.5.5.12 ALE Unknown VLAN Member List Register (ALE_UNKN_VLAN_MBR_LIST)

The ALE Unknown VLAN Member List Register is shown in Figure 3-204 and described in Table 3-220.

Figure 3-204. ALE Unknown VLAN Member List Register (ALE_UNKN_VLAN_MBR_LIST)



Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-220. ALE Unknown VLAN Member List Register (ALE_UNKN_VLAN_MBR_LIST) Field Descriptions

Bits	Field	Description
31-(Y+1)	Reserved	Reserved
Y-0	UNKN_VLAN_MEMBER_LIST	Unknown VLAN Member List. This is a port mask where each bit corresponds to a port in the switch. Y = 4 for a 5 port switch and Y = 8 for a 9 port switch.

3.5.5.13 ALE Unknown VLAN Unregistered Multicast Flood Mask Register (ALE_UNKN_VLAN_UNREG_MLT_FLOOD)

The ALE Unknown VLAN Unregistered Multicast Flood Mask Register is shown in Figure 3-205 and described in Table 3-221.

Figure 3-205. ALE Unknown VLAN Unregistered Multicast Flood Mask Register (ALE_UNKN_VLAN_UNREG_MLT_FLOOD)

31	Y+1	Y	0
Reserved		UNKN_VLAN_UNREG_MLT_FLOOD_MASK	
R-0h		R/W-0h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-221. ALE Unknown VLAN Unregistered Multicast Flood Mask Register (ALE_UNKN_VLAN_UNREG_MLT_FLOOD) Field Descriptions

Bits	Field	Description
31-(Y+1)	Reserved	Reserved
Y-0	UNKN_VLAN_UNREG_MLT_FLOOD_MASK	Unknown VLAN Unregistered Multicast Flood Mask. This is a port mask where each bit corresponds to a port in the switch. Y = 4 for a 5 port switch and Y = 8 for a 9 port switch.

3.5.5.14 ALE Unknown VLAN Registered Multicast Flood Mask Register (ALE_UNKN_VLAN_REG_MLT_FLOOD)

The ALE Unknown VLAN Registered Multicast Flood Mask Register is shown in Figure 3-206 and described in Table 3-222.

Figure 3-206. ALE Unknown VLAN Registered Multicast Flood Mask Register (ALE_UNKN_VLAN_REG_MLT_FLOOD)

31	Y+1	Y	0
Reserved		UNKN_VLAN_REG_MLT_FLOOD_MASK	
R-0h		R/W-0h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-222. ALE Unknown VLAN Registered Multicast Flood Mask Register (ALE_UNKN_VLAN_REG_MLT_FLOOD) Field Descriptions

Bits	Field	Description
31-(Y+1)	Reserved	Reserved
Y-0	UNKN_VLAN_REG_MLT _FLOOD_MASK	Unknown VLAN Registered Multicast Flood Mask. This is a port mask where each bit corresponds to a port in the switch. Y = 4 for a 5 port switch and Y = 8 for a 9 port switch.

3.5.5.15 ALE Unknown VLAN Force Untagged Egress Register (ALE_UNKN_VLAN_FORCE_UNTAG_EGR)

The ALE Unknown VLAN Forced Untagged Egress Register is shown in Figure 3-208 and described in Table 3-224.

Figure 3-207. ALE Unknown VLAN Force Untagged Egress Register (ALE_UNKN_VLAN_FORCE_UNTAG_EGR)

31	Y+1	Y	0
Reserved		UNKN_VLAN_FORCE_UNTAG_EGR_MASK	
R-0h		R/W-0h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-223. ALE Unknown VLAN Force Untagged Egress Register (ALE_UNKN_VLAN_FORCE_UNTAG_EGR) Field Descriptions

Bits	Field	Description
31-(Y+1)	Reserved	Reserved
Y-0	UNKN_VLAN_FORCE_UNTAG_EGR_MASK	Unknown VLAN Force Untagged Egress Mask. This is a port mask where each bit corresponds to a port in the switch. Y = 4 for a 5 port switch and Y = 8 for a 9 port switch.

3.5.5.16 ALE VLAN Mask Mux Select Register n (ALE_VLAN_MASK_MUXn)

The ALE VLAN Mask Mux Select Register n is shown in Figure 3-208 and described in Table 3-224. The variable n varies from 0 to 7.

Figure 3-208. ALE VLAN Mask Mux Select Register n (ALE_VLAN_MASK_MUXn)

31	Y+1	Y	0
Reserved		VLAN_MASK_MUX_X	
R-0h		R/W-0h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-224. ALE VLAN Mask Mux Select Register n (ALE_VLAN_MASK_MUXn) Field Descriptions

Bits	Field	Description
31-(Y+1)	Reserved	Reserved
Y-0	VLAN_MASK_MUX_X	VLAN Mask Mux Register Array X. The UNREG_MCAST_FLOOD_INDEX and REG_MCAST_FLOOD_INDEX values from the VLAN table entry are used to determine which of the eight ALE_VLAN_MASK_MUXn registers (n = 0 to 7) are used to obtain the registered and unregistered multicast flood masks. The value of ALE_VLAN_MASK_MUX0 is read only and all 1s (all ports are in the mask and will be flooded). These bits are a port mask where each bit corresponds to a port in the switch. Y = 4 for a 5 port switch and Y = 8 for a 9 port switch.

3.5.6 ECC Submodule

This section describes the registers available in the ECC submodule.

The register offset addresses listed in this section in Table 3-225 are relative to the ECC submodule. See Table 3-1 for the offset address of the ECC submodule. A complete list of all of the registers in the GbE switch subsystem is provided in Table 3-2.

Table 3-225 lists the registers in the ECC submodule and the corresponding offset address for each register.

Table 3-225. ECC Registers

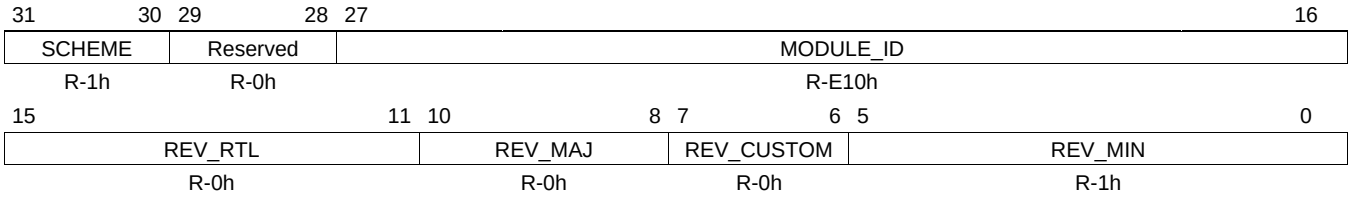
Offset Address[1]	Register Mnemonic	Register Name	Section
00h	ECC_REVISION	ECC Module Revision Register	Section 3.5.6.1
04h	Reserved	Reserved	Reserved
08h	ECC_VECTOR	ECC Module Vector Register	Section 3.5.6.2
0Ch	ECC_STATUS	ECC Module Status Register	Section 3.5.6.3
10h	ECC_WRAPPER_REVISION	ECC Module Wrapper Revision Register	Section 3.5.6.4
14h	ECC_CTRL	ECC Module Control Register	Section 3.5.6.5
18h	ECC_ERR_CTRL1	ECC Module Error Control 1 Register	Section 3.5.6.6
1Ch	ECC_ERR_CTRL2	ECC Module Error Control 2 Register	Section 3.5.6.7
20h	ECC_ERR_STATUS1	ECC Module Error Status 1 Register	Section 3.5.6.8
24h	ECC_ERR_STATUS2	ECC Module Error Status 2 Register	Section 3.5.6.9
28h-38	Reserved	Reserved	Reserved
3Ch	ECC_EOI	ECC Module EOI Register	Section 3.5.6.10
40h	ECC_INT_STATUS	ECC Module Interrupt Status Register	Section 3.5.6.11
44h-7C	Reserved	Reserved	Reserved
80h	ECC_INT_EN_SET	ECC Module Interrupt Enable Set Register	Section 3.5.6.12
84h-BC	Reserved	Reserved	Reserved
C0h	ECC_INT_EN_CLEAR	ECC Module Interrupt Enable Clear Register	Section 3.5.6.13
C4h-FC	Reserved	Reserved	Reserved

(1) The actual addresses of these registers are device specific. See your device-specific data manual to verify the register addresses.

3.5.6.1 ECC Module Revision Register (ECC_REVISION)

The ECC Module Revision Register is shown in Figure 3-209 and described in Table 3-226.

Figure 3-209. ECC Revision Register (ECC_REVISION)



Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-226. ECC Revision Register (ECC_REVISION) Field Descriptions

Bits	Field	Description
31-30	SCHEME	Scheme that this register is compliant with.
29-28	Reserved	Reserved
27-16	MODULE_ID	ECC Module ID.
15-11	REV_RTL	ECC Module RTL revision.
10-8	REV_MAJ	ECC Module Major revision.
7-6	REV_CUSTOM	ECC Module Custom revision.
5-0	REV_MIN	ECC Module Minor Revision

3.5.6.2 ECC Module Vector Register (ECC_VECTOR)

The ECC Module Vector Register is shown in Figure 3-210 and described in Table 3-227.

Figure 3-210. ECC Module Vector Register (ECC_VECTOR)

31 25	24	23 16	15	14 11	10 0
Reserved	READ_DONE	READ_ADDRESS	TRIGGER_READ	Reserved	ECC_VECTOR
R-0h	R-0h	R/W-0h	R/W-0h	R-0h	R/W-0h

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

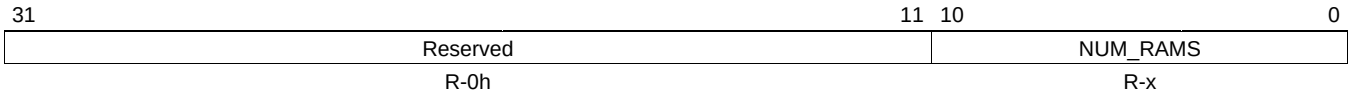
Table 3-227. ECC Module Vector Register (ECC_VECTOR) Field Descriptions

Bits	Field	Description
31-25	Reserved	Reserved
24	READ_DONE	Status indicating that the serial VBUS read is complete.
23-16	READ_ADDRESS	Read Address. Can be any of the following address offsets which correspond to the ECC register listed: • 0x10 - ECC_WRAPPER_REVISION • 0x14 - ECC_CONTROL • 0x18 - ECC_ERR_CTRL1 • 0x1C - ECC_ERR_CTRL2 • 0x20 - ECC_ERR_STATUS1 • 0x24 - ECC_ERR_STATUS2
15	TRIGGER_READ	Read Trigger. Trigger a read operation to the specified read address that requires a serial VBUS access.
14-11	Reserved	Reserved
10-0	ECC_VECTOR	ECC RAM ID to select which ECC RAM to control or read status from.

3.5.6.3 ECC Status Register (ECC_STATUS)

The ECC Status Revision Register is shown in Figure 3-211 and described in Table 3-228.

Figure 3-211. ECC Status Register (ECC_STATUS)



Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

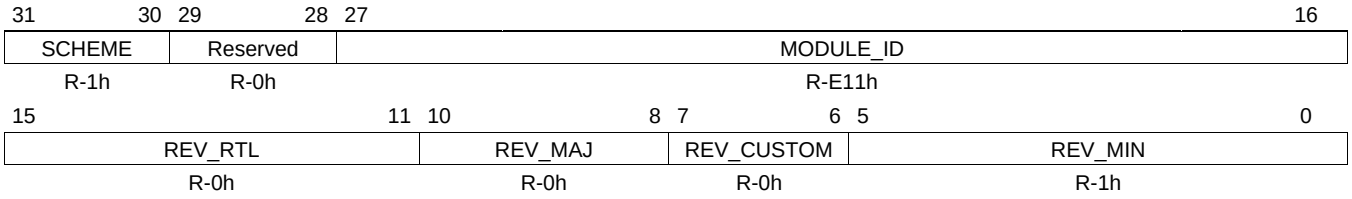
Table 3-228. ECC Status Register (ECC_STATUS) Field Descriptions

Bits	Field	Description
31-11	Reserved	Reserved
10-0	NUM_RAMS	Number of ECC RAMs serviced by the ECC module.

3.5.6.4 ECC Wrapper Revision Register (ECC_WRAPPER_REVISION)

The ECC Wrapper Revision Register is shown in Figure 3-212 and described in Table 3-229.

Figure 3-212. ECC Wrapper Revision Register (ECC_WRAPPER_REVISION)



Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-229. ECC Wrapper Revision Register (ECC_WRAPPER_REVISION) Field Descriptions

Bits	Field	Description
31-30	SCHEME	Scheme that this register is compliant with.
29-28	Reserved	Reserved
27-16	MODULE_ID	ECC Module ID.
15-11	REV_RTL	ECC Module RTL revision.
10-8	REV_MAJ	ECC Module Major revision.
7-6	REV_CUSTOM	ECC Module Custom revision.
5-0	REV_MIN	ECC Module Minor Revision

3.5.6.5 ECC Control Register (ECC_CTRL)

The ECC Control Register is shown in Figure 3-213 and described in Table 3-230.

Figure 3-213. ECC Control Register (ECC_CONTROL)

31 7	6	5	4	3	2	1	0
Reserved	ERROR _ONCE	FORCE_N _ROW	FORCE_DED	FORCE_SEC	ENABLE_RMW	ECC_CHECK	ECC_ENABLE
R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-1h	R/W-1h	R/W-1h

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-230. ECC Control Register (ECC_CONTROL) Field Descriptions

Bits	Field	Description
31-7	Reserved	Reserved
6	ERROR_ONCE	If this bit is set to 1, the FORCE_SEC/FORCE_DED will inject an error to the specified row only once. The FORCE_SEC bit will be cleared once a writeback happens. If writeback is not enabled, this error will be cleared the cycle following the read when the data is corrected. For double-bit errors, the FORCE_DED bit will be cleared the cycle following the double-bit error. Any subsequent read will not force an error.
5	FORCE_N_ROWS	Force single/double bit error on the next RAM read.
4	FORCE_DED	Force double-bit error. Cleared the cycle following the error if ERROR_ONCE is asserted to 1.
3	FORCE_SEC	Force single-bit error. Cleared on a writeback or the cycle following the error if ERROR_ONCE is asserted to 1.
2	ENABLE_RMW	Enable read-modify-write on partial word writes.
1	ECC_CHECK	Enable ECC Check. ECC is completely bypassed if both ECC_ENABLE and ECC_CHECK are 0.
0	ECC_ENABLE	Enable ECC generation. This bit is not used. ECC is always enabled.

3.5.6.6 ECC Error Control 1 Register (ECC_ERR_CTRL1)

The ECC Error Control 1 Register is shown in Figure 3-214 and described in Table 3-231.

Figure 3-214. ECC Error Control 1 Register (ECC_ERR_CTRL1)

31	16	15	0
ECC_BIT1		ECC_ROW	
R/W-0h		R/W-0h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-231. ECC Error Control 1 Register (ECC_ERR_CTRL1) Field Descriptions

Bits	Field	Description
31-16	ECC_BIT1	Column/Data bit that needs to be flipped when FORCE_SEC or FORCE_DED is set to 1 in the ECC_CONTROL register.
15-0	ECC_ROW	Row address where FORCE_SEC or FORCE_DED needs to be applied. This is ignored if FORCE_N_ROW is set to 1 in the ECC_CONTROL register.

3.5.6.7 ECC Error Control 2 Register (ECC_ERR_CTRL2)

The ECC Error Control 2 Register is shown in Figure 3-215 and described in Table 3-232.

Figure 3-215. ECC Error Control 2 Register (ECC_ERR_CTRL2)

31	16	15	0
Reserved		ECC_BIT2	
R-0h		R/W-0h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-232. ECC Error Control 2 Register (ECC_ERR_CTRL2) Field Descriptions

Bits	Field	Description
31-16	Reserved	Reserved
15-0	ECC_BIT2	Data bit that needs to be flipped when FORCE_DED is set to 1 in the ECC_CONTROL register.

3.5.6.8 ECC Error Status Register 1 (ECC_ERR_STATUS1)

The ECC Error Status Register 1 is shown in Figure 3-216 and described in Table 3-233.

Figure 3-216. ECC Error Status Register 1 (ECC_ERR_STATUS1)

31	16
ECC_ROW	
R-0h	

15	11	10	9	8	7	3	2	1	0
Reserved		CLR_ECC_OTHER	CLR_ECC_DED	CLR_ECC_SEC	Reserved		ECC_OTHER	ECC_DED	ECC_SEC
R-0h		R/W-0h	R/W-0h	R/W-0h	R-0h		R/W-0h	R/W-0h	R/W-0h

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-233. ECC Error Status Register 1 (ECC_ERR_STATUS1) Field Descriptions

Bits	Field	Description
31-16	ECC_ROW	Indicates the row/address where the single or double-bit error occurred.
15-11	Reserved	Reserved
10	CLR_ECC_OTHER	Reading a 1 in this bit indicates a successive single-bit error. Writing a 1 will clear this bit to 0.
9	CLR_ECC_DED	Reading a 1 in this bit indicates a pending double-bit error. Writing a 1 will clear this bit to 0.
8	CLR_ECC_SEC	Reading a 1 in this bit indicates a pending single-bit error. Writing a 1 will clear this bit to 0.
7-3	Reserved	Reserved
2	ECC_OTHER	Reading a 1 in this bit indicates a successive single-bit error has occurred while a writeback is still pending. Writing a 1 will set this bit to 1. Writing a 1 to the CLR_ECC_OTHER bit will clear this bit to 0.
1	ECC_DED	Reading a 1 in this bit indicates a pending double-bit error. Writing a 1 will set this bit to 1. Writing a 1 to the CLR_ECC_DED bit will clear this bit to 0.
0	ECC_SEC	Reading a 1 in this bit indicates a pending single-bit error. Writing a 1 will set this bit to 1. Writing a 1 to the CLR_ECC_SEC bit will clear this bit to 0.

3.5.6.9 ECC Error Status Register 2 (ECC_ERR_STATUS2)

The ECC Error Status 2 Register is shown in Figure 3-217 and described in Table 3-234.

Figure 3-217. ECC Error Status Register 2 (ECC_ERR_STATUS2)

31	16	15	0
Reserved		ECC_BIT1	
R-0h		R/W-0h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-234. ECC Error Status Register 2 (ECC_ERR_STATUS2) Field Descriptions

Bits	Field	Description
31-16	Reserved	Reserved
15-0	ECC_BIT1	Indicates the bit position in the RAM data that is in error. For example, a value of 1 indicates that bit 1 in the data is in error. This is valid only for single bit errors (SEC)

3.5.6.10 ECC EOI Register (ECC_EOI)

The ECC EOI Register is shown in Figure 3-218 and described in Table 3-235.

Figure 3-218. ECC EOI Register (ECC_EOI)

31	1	0
Reserved		EOI_WR
R-0h		R/W-0

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-235. ECC EOI Register (ECC_EOI) Field Descriptions

Bits	Field	Description
31-1	Reserved	Reserved
0	EOI_WR	Write to this register indicates that software has acknowledged the pending interrupt and the next interrupt can be sent to the host.

3.5.6.11 ECC Interrupt Status Register (ECC_INT_STATUS)

The ECC Interrupt Status Register is shown in Figure 3-219 and described in Table 3-236.

Figure 3-219. ECC Interrupt Status Register (ECC_INT_STATUS)

31	19	18	0
Reserved		SRC_INTR	
R-0h		R-0h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-236. ECC Interrupt Status Register (ECC_INT_STATUS) Field Descriptions

Bits	Field	Description
31-19	Reserved	Reserved
18-0	SRC_INTR	Level interrupt status. • 0 - Not pending • 1 - Pending status Each bit corresponds to an ECC RAM as below (depending on your device you will have either a 5 port switch or a 9 port switch, check your device specific data manual): • Bit 0 - ALE RAM • Bit 1 - Port 0 FIFO RX RAM • Bit 2 - Port 0 FIFO TX RAM • Bit 3 - Port 1 FIFO RX RAM • Bit 4 - Port 1 FIFO TX RAM • ... • Bit 15 - Port 7 FIFO RX RAM • Bit 16 - Port 7 FIFO TX RAM • Bit 17 - Port 8 FIFO RX RAM • Bit 18 - Port 8 FIFO TX RAM

3.5.6.12 ECC Interrupt Enable Set Register (ECC_INT_EN_SET)

The ECC Interrupt Enable Set Register is shown in Figure 3-220 and described in Table 3-237.

Figure 3-220. ECC Interrupt Enable Set Register (ECC_INT_EN_SET)

31	19	18	0
Reserved		ENABLE	
R-0h		R/W-0h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-237. ECC Interrupt Enable Set Register (ECC_INT_EN_SET) Field Descriptions

Bits	Field	Description
31-19	Reserved	Reserved
18-0	ENABLE	Write a 1 to enable interrupts from the associated ECC RAM. Each bit corresponds to an ECC RAM as below (depending on your device you will have either a 5 port switch or a 9 port switch, check your device specific data manual): • Bit 0 - ALE RAM • Bit 1 - Port 0 FIFO RX RAM • Bit 2 - Port 0 FIFO TX RAM • Bit 3 - Port 1 FIFO RX RAM • Bit 4 - Port 1 FIFO TX RAM • ... • Bit 15 - Port 7 FIFO RX RAM • Bit 16 - Port 7 FIFO TX RAM • Bit 17 - Port 8 FIFO RX RAM • Bit 18 - Port 8 FIFO TX RAM

3.5.6.13 ECC Interrupt Enable Clear Register (ECC_INT_EN_CLEAR)

The ECC Interrupt Enable Clear Register is shown in Figure 3-221 and described in Table 3-238.

Figure 3-221. ECC Interrupt Enable Clear Register (ECC_INT_EN_CLEAR)

31	19	18	0
Reserved		ENABLE_CLEAR	
R-0h		R/W-0h	

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 3-238. ECC Interrupt Enable Clear Register (ECC_INT_EN_CLEAR) Field Descriptions

Bits	Field	Description
31-19	Reserved	Reserved
18-0	ENABLE_CLEAR	Write a 1 to disable interrupts from the associated ECC RAM. Each bit corresponds to an ECC RAM as below (depending on your device you will have either a 5 port switch or a 9 port switch, check your device specific data manual): • Bit 0 - ALE RAM • Bit 1 - Port 0 FIFO RX RAM • Bit 2 - Port 0 FIFO TX RAM • Bit 3 - Port 1 FIFO RX RAM • Bit 4 - Port 1 FIFO TX RAM • ... • Bit 15 - Port 7 FIFO RX RAM • Bit 16 - Port 7 FIFO TX RAM • Bit 17 - Port 8 FIFO RX RAM • Bit 18 - Port 8 FIFO TX RAM

Revision History

Changes from August 1, 2014 to May 1, 2015 **Page**

- Updated Descriptor Information Word 1 for Host Port 0 Switch Ingress Packets table. 33
- Updated Descriptor Information Word 2 for Host Port 0 Switch Ingress Packets table. 33
- Updated Extended Packet Info Word 1 for Host Port 0 Switch Ingress Packets table. 33

IMPORTANT NOTICE FOR TI DESIGN INFORMATION AND RESOURCES

Texas Instruments Incorporated ('TI") technical, application or other design advice, services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using any particular TI Resource in any way, you (individually or, if you are acting on behalf of a company, your company) agree to use it solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources.

You understand and agree that you remain responsible for using your independent analysis, evaluation and judgment in designing your applications and that you have full and exclusive responsibility to assure the safety of your applications and compliance of your applications (and of all TI products used in or for your applications) with all applicable regulations, laws and other applicable requirements. You represent that, with respect to your applications, you have all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. You agree that prior to using or distributing any applications that include TI products, you will thoroughly test such applications and the functionality of such TI products as used in such applications. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

You are authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING TI RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY YOU AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

You agree to fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of your non-compliance with the terms and provisions of this Notice.

This Notice applies to TI Resources. Additional terms apply to the use and purchase of certain types of materials, TI products and services. These include; without limitation, TI's standard terms for semiconductor products http://www.ti.com/sc/docs/stdterms.htm), evaluation modules, and samples (http://www.ti.com/sc/docs/sampterms.htm).

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265