KeyStone II Architecture Network Coprocessor (NETCP) for K2E and K2L Devices

User's Guide

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Preface

About This Manual

The network coprocessor (NETCP) is a hardware accelerator that processes data packets with a main focus on processing Ethernet packets. NETCP has a gigabit Ethernet (GbE) module to send and receive packets from an IEEE 802.3-compliant network, a packet accelerator (PA) to perform packet classification operations such as header matching, and packet modification operations such as checksum generation, and a security accelerator (SA) to encrypt and decrypt data packets.

Notational Conventions

This document uses the following conventions:

- Commands and keywords are in **boldface** font.
- Arguments for which you supply values are in *italic* font.
- Terminal sessions and information the system displays are in screen font.
- Information you must enter is in **boldface screen font**.
- Elements in square brackets ([ ]) are optional.

Notes use the following conventions:

NOTE: Means reader take note. Notes contain helpful suggestions or references to material not covered in the publication.

The information in a caution or a warning is provided for your protection. Please read each caution and warning carefully.

CAUTION

Indicates the possibility of service interruption if precautions are not taken.

WARNING

Indicates the possibility of damage to equipment if precautions are not taken.

Related Documentation from Texas Instruments

Gigabit Ethernet (GbE) Switch Subsystem for K2E and K2L Devices User's Guide	SPRUHZ3
Interrupt Controller (INTC) for KeyStone Devices User's Guide	SPRUGW4
Multicore Navigator for KeyStone Devices User's Guide	SPRUGR9
Packet Accelerator 2 (PA2) for K2E and K2L Devices User's Guide	SPRUHZ2
Security Accelerator 2 (SA2) for K2E and K2L Devices User's Guide	SPRUHZ1

Introduction

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1.1 Purpose of the Peripheral

This document provides a functional description of the network co-processor (NETCP) for the TCI6630K2L, 66AK2Ex, and AM5K2Ex devices, herein called K2L and K2E devices. The NETCP for K2L and K2E devices is a hardware accelerator whose main focus is to process network-related packets. Protocols supported span layer 2 (MAC), layer 3 (IPV4/IPV6), and layer 4 (UDP/TCP/GTP-U).

The following modules are part of the NETCP:

- A gigabit Ethernet (GbE) switch. The GbE switch sends and receives packets from an IEEE 802.3-compliant network and may have five or nine ports. See the device-specific data manual for specific details regarding port count.
- A packet accelerator version 2.0 (PA2). The PA2 performs packet classification operations such as header matching, and packet modification operations such as checksum generation.
- A security accelerator version 2.0 (SA2). The SA2 encrypts and decrypts data packets.

The NETCP can receive packets from the GbE switch modules, or packets can be delivered to the NETCP through a packet DMA engine from soft cores (i.e. DSP/ARM) or another supported peripheral. The NETCP has an additional packet DMA engine managed by a local instance of the queue manager sub system (QMSS) reserved for PA2-SA2 intercommunication.

1.2 Terminology Used in This Document

The following acronyms and abbreviations appear in this user's guide.

Term	Definition
GbE	Gigabit Ethernet
MAC	Media Access Controller
MDIO	Management Data Input/Output
NETCP	Network Coprocessor for K2E and K2L devices
PA2	Packet Accelerator version 2.0
PKTDMA	Packet DMA
PSI	Packet Streaming Interface
QMSS	Queue Manager subsystem
SA2	Security Accelerator version 2.0
SerDes	Serializer/Deserializer
SGMII	Serial Gigabit Media Independent Interface
LQM	Local Queue Manager

1.3 Features

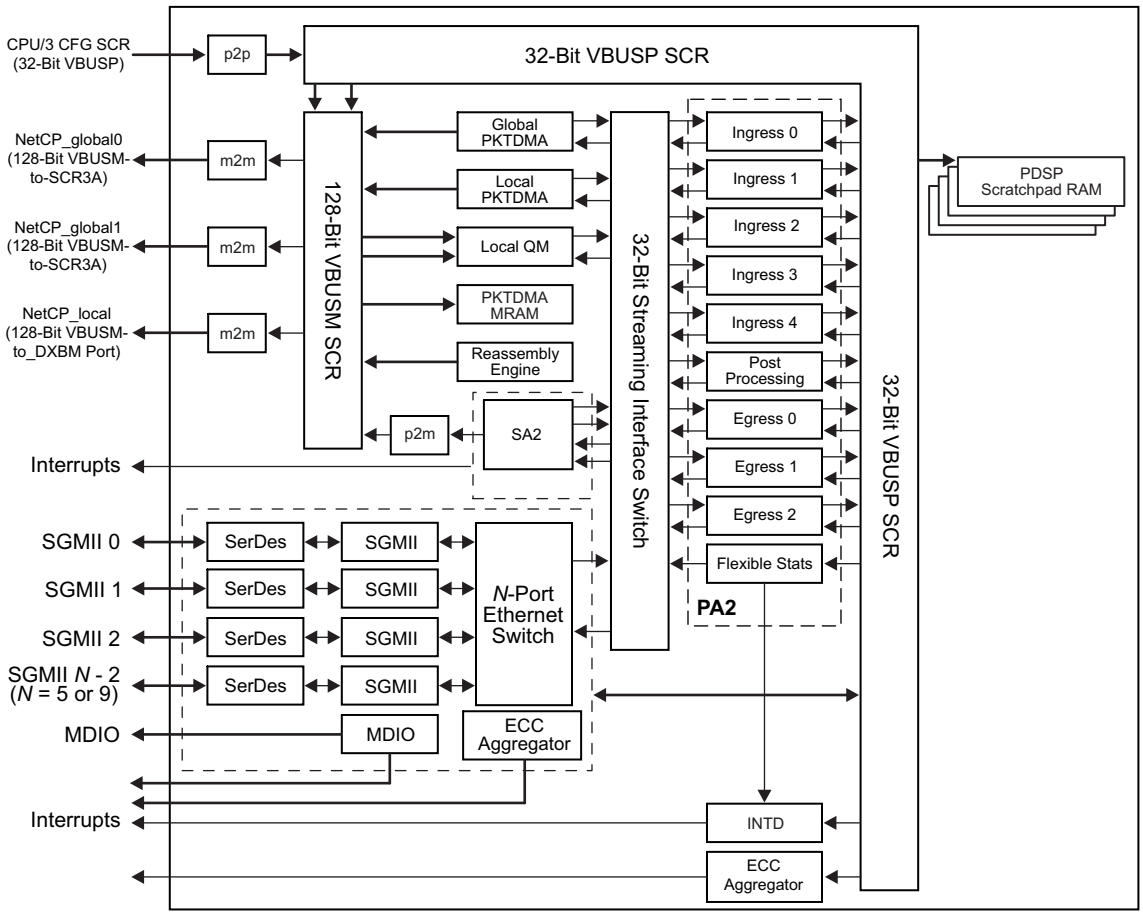
The NETCP has the following features:

- Packet DMA controller (global PKTDMA) for interfacing to the queue manager subsystem
  - 21 packet DMA transmit channels
  - 91 packet DMA receive channels
  - 96 receive flows
- Packet DMA controller (local PKTDMA) managed by local queue manager for inter PA2-SA2 communication.
  - 21 packet DMA transmit channels
  - 91 packet DMA receive channels
  - 96 receive flows
- Packet accelerator version 2.0 for packet header processing operations
  - Five ingress engines for L2-L4 processing
    - L3 reassembly
    - ACL processing
    - Multi-route capabilities
  - One post-process engine for CRC operations on ingress
  - Three egress engines for to-network L2-L3 operations
    - L2 Framing
    - IP fragmentation
    - L4 checksum
    - IPSEC ESP over IPSEC AH preparation
- Security accelerator version 2.0 for encryption and decryption operations
  - IPSEC protocol stack
  - SRTP protocol stack
  - 3GPP protocol stack, wireless air cipher standard
  - True random number generator
  - Public key accelerator
- Gigabit Ethernet switch subsystem for interfacing to an 802.3-compliant Ethernet network
  - Four or eight serial gigabit media independent interface (SGMII) modules
    - K2L (4)
    - K2E (8)
  - Five or nine-port gigabit Ethernet switch
    - K2L (5)
    - K2E (9)
  - Time Synchronization for compliance with IEEE 1588

1.4 Functional Block Diagram

Figure 1-1 shows the network coprocessor (NETCP) functional block diagram. The NETCP has seven major modules that are connected through the packet streaming switch.

Figure 1-1. KeyStone II Network Coprocessor Functional Block Diagram



The seven major modules are:

- Global Packet DMA (PKTDMA) controller
- Local Packet DMA (PKTDMA) controller
- Packet accelerator version 2 (PA2)
- Security accelerator version 2 (SA2)
- Gigabit Ethernet (GbE) switch subsystem
- Reassembly engine (RA)
- Local queue manager (LQM)

1.5 Industry Standard(s) Compliance Statement

The modules in the NETCP support a variety of standards, which are covered in detail in the respective module user's guides. For more information about the standards supported by each module, see the following:

- Packet Accelerator 2 (PA2) for K2E and K2L Devices User's Guide (SPRUHZ2)
- Security Accelerator (SA2) for K2E and K2L Devices User's Guide (SPRUHZ1)
- Gigabit Ethernet (GbE) Switch Subsystem for K2E and K2L Devices User's Guide (SPRUHZ3)
- Multicore Navigator User Guide (*for Packet DMA*) (SPRUGR9)

Architecture

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2.1 Clock Control

The network coprocessor (NETCP) has three primary clock domains:

- Packet Accelerator version 2.0 (PA2) + Reassembly Engine (RA)
- Security Accelerator version 2.0 (SA2)
- Gigabit Ethernet (GbE) Switch subsystem

Each of these three clock domains share a common source clock, which is expected to operate at 350 MHz. Before using the PA2 + RA, SA2, or GbE switch modules, their respective clock domains must be enabled. In some devices, this clock may be generated from a PLL. For more information about generating and enabling these clocks, as well as if a PLL is used, see the device-specific data manual.

The NETCP also has secondary clocks, which are used exclusively by the GbE switch subsystem for time synchronization, MDIO, and SGMII SerDes interfaces. For more information about selecting and configuring those clocks, see the *GbE Switch Subsystem User's Guide* (SPRUHZ3).

2.2 Memory Map

Table 2-1 shows the memory map of the network coprocessor (NETCP) for K2E and K2L devices.

Table 2-1. Keystone II Network Coprocessor Memory Map for K2E and K2L Devices

Region	Address Offset(1)
Packet accelerator v2.0	0000:0000h
Reassembly engine	0000:0400h
GbE thread mapper	0000:0500h
Reserved	0000:05800h-0000:07FFh
Reassembly engine (continued)	0000:0800h
ECC aggregator	0000:0C00h
Reserved	0000:1000h-0000:5FFFh
Packet accelerator v2.0 (continued)	0000:6000h
Reserved	0000:6100h-0000:6FFFh
Packet accelerator v2.0 (continued)	0000:7000h
Reserved	0002:8000h-0007:FFFFh
Security accelerator v2.0	00008:0000h
Reserved	0010:0000h-0018:1FFFh
Local PKTDMA	0018:2000h
Reserved	0018:2180h-0018:2FFFh
Local PKTDMA TX channel configuration	0018:3000h
Local PKTDMA RX channel configuration	0018:4000h
Local PKTDMA RX flow config	0018:5000h
Global PKTDMA	0018:6000h
Reserved	0018:6180h-0018:6FFFh
Global PKTDMA TX channel configuration	0018:7000h
Global PKTDMA RX channel configuration	0018:8000h
Global PKTDMA RX flow config	0018:9000h
Reserved	0018:A000h-0019:FFFF
Local queue manager	001A:0000h
Reserved	001B:2000h-001B:7FFFh
Local queue manager (continued)	001B:8000h
Reserved	001B:8800h-001B:BFFF
Local queue manager (continued)	001B:C000h

(1) These register address offsets are relative to the base of the NETCP module. See the device-specific data manual to determine the base of the NETCP module.

Table 2-1. Keystone II Network Coprocessor Memory Map for K2E and K2L Devices (continued)

Region	Address Offset[1]
Reserved	001B:C800h-001F:FFFFh
Gigabit Ethernet switch subsystem	0020:0000h
Packet accelerator v2.0 (continued)	0040:0000h

2.3 Packet Streaming Switch Architecture

This section gives an overview of the packet streaming switch (PSI) in the NETCP. The purpose of the PSI is to provide a means of transferring data between modules within the NETCP. Table 2-2 shows all connections between the modules provided by the packet streaming switch.

Table 2-2. Keystone II Packet Streaming Switch Module Connections for K2E and K2L Devices

Transmit Ports	Receive Ports														
	pkt dma_g	pkt dma_l	gbe_ switch	ingress 0	ingress 1	ingress 2	ingress 3	post_ process	egress 0	egress 1	egress 2	RA	sa_ port1	sa_ port2	flexible_ stats
pktdma_g		1	1	1	1	1	1	1	1	1	1	1	1	1	1
pktdma_l			1	1	1	1	1	1	1	1	1	1	1	1	
gbe_switch*	1	1		1	1	1	1	1	1	1	1				
sa_port1	1	1													
sa_port2	1	1													
ingress0	1	1	1		1	1	1	1	1	1	1	1	1	1	
ingress1	1	1	1	1		1	1	1	1	1	1	1	1	1	
ingress2	1	1	1	1	1		1	1	1	1	1	1	1	1	
ingress3	1	1	1	1	1	1		1	1	1	1	1	1	1	
ingress4	1	1	1	1	1	1	1		1	1	1	1	1	1	
post_process	1	1	1	1	1	1	1	1		1	1	1	1	1	
egress0	1	1	1	1	1	1	1	1	1		1	1	1	1	
egress1	1	1	1	1	1	1	1	1	1	1		1	1	1	
egress2	1	1	1	1	1	1	1	1	1	1	1		1	1	
RA	1	1		1	1	1	1	1	1	1	1				
flexible_stats	1														

NOTE: *GbE Switch has 64 threads, corresponding to each ingress port / priority combination (8ingress Ethernet ports * 8 priorities). Threads 0-7 are priorities 0-7 for Ethernet port 0. Threads 8-15 are priorities 0-7 for Ethernet port 1, and so on. The packet streaming switch thread mapper is used to map the 64 threads coming out of the GbE Switch (one per port/priority pair), and map them to assets within the NETCP. Each thread from the GbE switch can be mapped to one of the following 10 destinations based on the value programmed into its register field. If mapped to a PKTDMA (global or local), thread 0 from the switch will map to thread 0 of the PKTDMAs selected, thread 1 to thread 1 etc. For more on the packet streaming interface thread mapper register, see Section 3.1.

In general, the packet accelerator (PA2) and security accelerator (SA2) modules should communicate only through the local PKTDMA module. These modules should not communicate directly because the limited buffering in the system can degrade performance. Global PKTDMA should be reserved for Host-NetCP interaction.

2.4 Packet DMA Architecture

The global and local packet DMA controllers in the NETCP are responsible for transferring data between NETCP and the host (global) and between PA2-SA2 (local). Data transferred through global and local PKTDMA can be transmitted via the packet streaming switch to the receive ports of devices within the NETCP as listed in Table 2-2. For more information about packet DMA along with device specific TX queue ranges for Global and Local PKTDMA, see the *Multicore Navigator User's Guide* (SPRUGR9).

Below please find the TX thread allocation for both Local and Global PKTDMA. This relates to the queue range as in *Multicore Navigator User's Guide* (SPRUGR9).

PKTDMA TX Thread Allocation	
NetCP Component	**Global and Local TX Thread**
GbE Switch Host Port Priority 0	0
GbE Switch Host Port Priority 1	1
GbE Switch Host Port Priority 2	2
GbE Switch Host Port Priority 3	3
GbE Switch Host Port Priority 4	4
GbE Switch Host Port Priority 5	5
GbE Switch Host Port Priority 6	6
GbE Switch Host Port Priority 7	7
Ingress 0	8
Ingress 1	9
Ingress 2	10
Ingress 3	11
Ingress 4	12
Post-Processing	13
Egress 0	14
Egress 1	15
Egress 2	16
RA	17
SA Input 1	18
SA Input 2	19
Flexible Stats	20

2.5 Local Queue Manager Architecture

The local queue manager is an instance of the queue manager subsystem (QMSS) that manages the local PKTDMA. For more information about the local queue manager, see the *Multicore Navigator User's Guide* (SPRUGR9).

2.6 Reassembly Engine Architecture

The IP Reassembly Engine (RA) reassembles fragmented IPv4 and IPv6 packets. A packet or fragment is streamed in on the packet streaming interface (PSI) and buffered internally. Once the desired function is completed, the packet is forwarded out on the PSI streaming interface. The RA is designed to work in the context of the packet accelerator. It requires that packets be preclassified and that the metadata (i.e. information from the IPV4 or IPV6 header) is populated correctly. Specifically, the ingress0 block performs this operation. The RA then forwards the nonfragmented or fully reassembled packet to the ingress1 block for outer IP reassembly. RA also performs inner IP reassembly. This stage occurs after ingress3 processing which prepares the metadata for RA. Afterwards, RA will forward the reassembled packet to ingress4 for further processing. The RA supports 64 threads on ingress and 32 threads on egress. Configuration of the RA is performed via the PA firmware and drivers. Direct programming of the RA registers is not supported. See the MCSDK or PDK for programming information regarding the RA.

2.7 Distributed Interrupt Controller Architecture

The distributed interrupt controller in the NETCP has the ability to aggregate interrupts from several sources and combine these interrupts into one interrupt to the host.

2.8 Reset Considerations

The gigabit Ethernet (GbE) switch subsystem supports reset isolation. For more information on this functionality, see the *GbE Switch Subsystem User's Guide* (SPRUHZ3).

2.9 Initialization

This section describes how to initialize the network coprocessor (NETCP).

The NETCP relies on the queue manager subsystem (QMSS) and the packet DMA to communicate with the host, which requires that these two systems be set up before setting up the network coprocessor. After setting up the QMSS and the packet DMA, the user can configure the NETCP. The user should take care to program the packet streaming switch thread mapper configuration register so that it directs packets from the gigabit Ethernet (GbE) switch subsystem to the desired module.

However, this does not preclude the use of drivers to perform this operation. If using the packet accelerator (PA2) and security accelerator (SA2) together, the PA2 must be initialized before initializing the SA2. Otherwise, the PA2, SA2, and GbE switch subsystem can be initialized in any order.

Section 2.9.1 shows the network coprocessor initialization procedure:

2.9.1 Network Coprocessor Initialization Procedure

Step 1. Turn on the NETCP power domain.
Step 2. Ungate the clocks for all modules used.
Step 3. Configure the queue manager.
Step 4. Configure the local queue manager
Step 5. Configure the global and local packet DMA.
  (a) Configure the linking RAM.
  (b) Initialize descriptors.
  (c) Configure receive flows.
  (d) Enable transmit channels.
  (e) Enable receive channels.
Step 6. Configure the packet streaming switch thread mapper.
Step 7. Configure the GbE switch subsystem.
Step 8. Configure the PA2.
Step 9. Configure the SA2.

2.10 Interrupt Support

2.10.1 Interrupt Events and Requests

The NETCP supports interrupts from the gigabit Ethernet (GbE) switch subsystem and the packet accelerator version 2.0 (PA2). For more information about the interrupts generated by the GbE switch subsystem, see the *GbE Switch Subsystem for KeyStone Devices User's Guide* (SPRUHZ3). For more information about the interrupts generated by the PA2, see the *Packet Accelerator 2 (PA2) for K2E and K2L Devices User's Guide* (SPRUHZ2

).

2.10.2 Interrupt Multiplexing

Interrupt multiplexing is supported on the NETCP through the distributed interrupt controller. For more information, see the distributed interrupt controller section.

2.11 Power Management

The network coprocessor (NETCP) has power management capabilities for powering down the NETCP power domain. The power domain is powered on or powered off in its entirety. The NETCP power domain does not support the ability to power down the individual modules in the NETCP. By default, the NETCP power domain is powered off. To use the NETCP, the power domain must be powered on.

In addition to allowing the disabling of the NETCP power domain, NETCP also allows the clocks to the unused modules to be gated. The packet accelerator v2.0 (PA2), security accelerator v2.0 (SA2), and gigabit Ethernet (GbE) switch subsystem can each be clock-gated individually. This allows any unused modules in NETCP to be clock gated without affecting the other modules in the NETCP.

For more information, see the device-specific data manual.

NOTE: The local and global packet DMA controller and the packet streaming switch are included in the packet accelerator clock domain. This means that the packet accelerator clock domain must be enabled when using the security accelerator or the gigabit Ethernet switch subsystem.

Registers

This chapter describes the programmable register in the network coprocessor (NETCP).

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3.1 GbE Thread Map Register

This section details the GbE Thread Map Register as it relates to the connection of the GbE switch to the packet streaming interface (PSI). For an overview of its function, see Section Section 2.3. The offset is 0000:0500h.

Table 3-1. GBE Switch Thread Mapper Values

Thread (Programmed Register Value)	Target
0	Global PKTDMA
1	Local PKTDMA
2	Ingress 0
3	Ingress 1
4	Ingress 2
5	Ingress 3
6	Ingress 4
7	Post processing
8	Egress 0
9	Egress 1
10	Egress 2

Figure 3-1. GbE Thread Map Register

31 24	23 16	15 8	7 0
Thread *N**4+3	Thread *N**4+2	Thread *N**4+1	Thread *N**4
R/W -0x0	R/W -0x0	R/W -0x0	R/W -0x0

Legend: R/W = Read/Write; -n = value after reset

Table 3-2. GbE Thread Map Register Field Descriptions

Bit	Field	Description
31 - 24	Thread *N**4+3	Thread *N**4+3 from the gbe_switch TX will be mapped to this target based on Table 3-1. Only 0 through 10 are legal values. Attempting to write a value of 11 or greater will result in the field being unchanged.
23 - 16	Thread *N**4+2	Thread *N**4+2 from the gbe_switch TX will be mapped to this target based on Table 3-1. Only 0 through 10 are legal values. Attempting to write a value of 11 or greater will result in the field being unchanged.
15 - 8	Thread *N**4+1	Thread *N**4+1 from the gbe_switch TX will be mapped to this target based on Table 3-1. Only 0 through 10 are legal values. Attempting to write a value of 11 or greater will result in the field being unchanged.
7 - 0	Thread *N**4	Thread *N**4 from the gbe_switch TX will be mapped to this target based on Table 3-1. Only 0 through 10 are legal values. Attempting to write a value of 11 or greater will result in the field being unchanged.

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