Keystone II Architecture
DDR3 Memory Controller

User's Guide

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Preface

About This Manual

The DDR3 memory controller is used to interface with JESD79-3C standard compliant SDRAM devices. Memory types such as DDR1 SDRAM, DDR2 SDRAM, SDR SDRAM, SBSRAM, and asynchronous memories are not supported. The DDR3 memory controller SDRAM can be used for program and data storage.

Notational Conventions

This document uses the following conventions:

- Commands and keywords are in **boldface** font.
- Arguments for which you supply values are in *italic* font.
- Terminal sessions and information the system displays are in screen font.
- Information you must enter is in **boldface screen font**.
- Elements in square brackets ([ ]) are optional.

Notes use the following conventions:

NOTE: Means reader take note. Notes contain helpful suggestions or references to material not covered in the publication.

The information in a caution or a warning is provided for your protection. Please read each caution and warning carefully.

CAUTION

Indicates the possibility of service interruption if precautions are not taken.

WARNING

Indicates the possibility of damage to equipment if precautions are not taken.

Related Documentation from Texas Instruments

C66x CorePac User Guide	SPRUGW0
C66x CPU and Instruction Set Reference Guide	SPRUGH7
Enhanced Direct Memory Access 3 (EDMA3) for KeyStone Devices User Guide	SPRUGS5
External Memory Interface (EMIF16) for KeyStone Devices User Guide	SPRUGZ3
Interrupt Controller (INTC) for KeyStone Devices User Guide	SPRUGW4

Introduction

This document describes the operation of the DDR3 module in the KeyStone II devices. (Refer to the device-specific data manual for exact device applicability.) The DDR3 module is accessible across all the cores and all system masters that are not cores.

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1.1 Purpose of the Peripheral

The DDR3 memory controller is used to interface with JESD79-3E standard compliant SDRAM devices. Memory types such as DDR1 SDRAM, DDR2 SDRAM, SDR SDRAM, SBSRAM, and asynchronous memories are not supported. The DDR3 memory controller SDRAM can be used for program and data storage. The KeyStone II devices have one (DDR3A) or two (DDR3A and DDR3B) instances depending on the device variant. See the KeyStone II Data Manual. DDR3A is accessed via the MSMC module whereas DDR3B is connected directly to the TeraNet.

1.2 Features

The DDR3 controller supports the following features:

- Supports JEDEC standard JESD79-3E – DDR3 compliant devices
- 33-bit address for 8 GB of address space
- 16/32/64-bit data bus width support
- CAS latencies: 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15 and 16
- 1, 2, 4, and 8 internal banks
- Burst Length: 8
- Burst Type: sequential
- 8GB address space available over one or two chip selects
- Page sizes: 256, 512, 1024, and 2048-word
- SDRAM auto initialization from reset or configuration change
- Self-refresh mode
- Prioritized refresh scheduling
- Programmable SDRAM refresh rate and backlog counter
- Programmable SDRAM timing parameters
- Big and little endian modes
- ECC on SDRAM data bus (read-modify-write (RMW) ECC to support sub quanta accesses to ECC space (see the section on ECC for applicable device))
- 8-bit ECC per 64-bit data quanta without additional cycle latency
- Two latency classes supported
- UDIMM Address mirroring is supported
- RDIMM is not supported

1.3 Industry Standard(s) Compliance Statement

The DDR3 controller is compliant with the JESD79-3E DDR3 SDRAM standard.

Peripheral Architecture

The DDR3 controller interfaces with most standard DDR3 SDRAM devices. It supports self-refresh mode and prioritized refresh. In addition, it provides flexibility through programmable parameters such as the refresh rate, CAS latency, and many SDRAM timing parameters. The following sections describe the architecture of the DDR3 controller as well as how to interface and configure it to perform read and write operations to DDR3 SDRAM devices. Examples for interfacing the DDR3 controller to a common DDR3 SDRAM device are shown in Section 3.1.

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2.1 Clock Interface

There are two clocking schemes in the DDR3 controller - the clocking scheme used to drive the DDR3 controller and the clocking scheme used to drive the DDR3 I/O interface. The DDR3A controller is clocked by DSP/2 clock domain and the DDR3B controller is clocked by DSP/3 clock domain. The I/O interface is driven by the DDR3 A/B memory clock (half the data rate).

2.2 SDRAM Memory Map

On KeyStone II devices, both DDR3A and DDR3B have their own controller configuration space and PHY configuration space. For information describing the DDR3 A/B memory map, see the device-specific data manual.

2.3 Signal Descriptions

The DDR3 memory controller signals are shown in Figure 2-1 and described in Figure 2-1.

- The maximum data bus is 64-bits wide.
- The address bus is 33-bits wide.
- Two differential output clocks driven by internal clock sources.
- Command signals: Row and column address strobe, write enable strobe, data strobe, and data mask.
- Two chip selects and two clock enable signals.

Figure 2-1. DDR3 Memory Control Signals

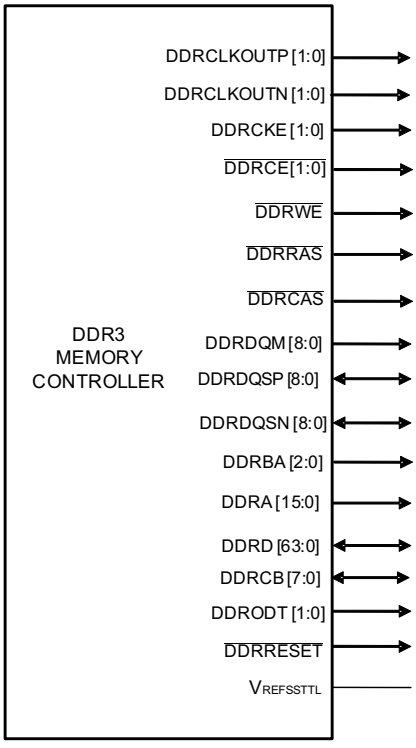


Table 2-1. DDR3 Memory Controller Signal Descriptions

Pin	Description
DDRD [63:0]	Bidirectional data bus. Input for data reads and output for data writes.
DDRCB [7:0]	Bidirectional data bus (check bits) for ECC byte lane. Input for data reads and output for data writes.
DDRA [15:0]	External address output.
DDRCE0	Active-low chip enable for memory space CE0. DDRCE0z is used to enable the DDR3 SDRAM memory device during external memory accesses.

Table 2-1. DDR3 Memory Controller Signal Descriptions (continued)

Pin	Description
$\overline{\text{DDRCE1}}$	Active-low chip enable for memory space CE1. DDRCE1z is used to enable the DDR3 SDRAM memory device during external memory accesses.
DDRDQM [8:0]	Active-high output data mask.
DDR3CLKOUTP [1:0]/ DDR3CLKOUTN [1:0]	Differential clock outputs.
DDRCKE [1:0]	Clock enable (used for self-refresh mode).
$\overline{\text{DDRCAS}}$	Active-low column address strobe.
$\overline{\text{DDRRAS}}$	Active-low row address strobe.
$\overline{\text{DDRWE}}$	Active-low write enable.
DDRDQSP [8:0]/ DDRDQSN [8:0]	Differential data strobe bidirectional signals.
DDRODT [1:0]	On-die termination signal(s) to external DDR3 SDRAM
DDRBA [2:0]	Bank-address control outputs
VREFSSTTL	DDR3 Memory Controller reference voltage. This voltage must be supplied externally. For more details, see the device-specific data manual.

2.4 Protocol Descriptions

The DDR3 memory controller supports the DDR3 SDRAM commands listed in Table 2-2.

Table 2-2. DDR3 SDRAM Commands

Command	Function
ACT	Activates the selected bank and row.
PREA	Precharge all command. Deactivates (precharges) all banks.
PRE	Precharge single command. Deactivates (precharges) a single bank.
DES	Device Deselect.
EMRS	Extended Mode Register set. Allows altering the contents of the mode register.
MRS	Mode register set. Allows altering the contents of the mode register.
NOP	No operation.
PDE	Power down entry
PDX	Power down exit
RD	Inputs the starting column address and begins the read operation.
REF	Autorefresh cycle
SRE	Self-refresh entry
SRX	Self-refresh exit
WR	Inputs the starting column address and begins the write operation.
ZQCS	ZQ Calibration short operation
ZQCL	ZQ Calibration long operation

Table 2-3 shows the signal truth table for the DDR3 SDRAM commands.

Table 2-3. Truth Table for DDR3 SDRAM Commands[1]

DDR3 SDRAM Signals	CKE		CS#	RAS#	CAS#	WE#	BA [2:0]	A [15:13]	A12	A10	A [9:0], A11
DDR3 Memory controller signals	DDRCKE		$\overline{DCE}$	$\overline{DDRRAS}$	$\overline{DDRCAS}$	$\overline{DDRWE}$	DDRBA [2:0]	DDRA [15:13]	DDRA [12]	DDRA [10]	DDRA [9:0],[11]
	Previous Cycle	Current Cycle									
ACT	H	H	L	L	H	H	BA	Row Address (RA)			
PREA	H	H	L	L	H	L	V	V	V	H	V
PRE	H	H	L	L	H	L	BA	V	V	L	V
MRS	H	H	L	L	L	L	BA	OP Code			
EMRS[2]	H	H	L	L	L	L	BA	OP Code			
RD (BL8)	H	H	L	H	L	H	BA	RFU	V	L	CA
WR (BL8)	H	H	L	H	L	L	BA	RFU	V	L	CA
REF	H	H	L	L	L	H	V	V	V	V	V
SRE[3]	H	L	L	L	L	H	V	V	V	V	V
SRX[3][4]	L	H	H	X	X	X	X	X	X	X	X
			L	H	H	H	V	X	V	V	V
NOP	H	H	L	H	H	H	V	V	V	V	V
DES[5]	H	H	H	X	X	X	X	X	X	X	X
PDE[6]	H	L	L	H	H	H	V	V	V	V	V
			X	X	X	X	X	X	X	X	X
PDX[6]	L	H	L	H	H	H	V	V	V	V	V
			X	X	X	X	X	X	X	X	X
ZQCL	H	H	L	H	H	L	X	X	X	H	X
ZQCS	H	H	L	H	H	L	X	X	X	L	X

(1) LEGEND: H = Logic High, L = Logic Low, X = Don't Care, RA = Row Address, CA = Column Address, RFU = Reserved for future use, V = Valid

(2) For extended mode register set (EMRS) command, bank address (BA) pins select an extended mode register (EMR).

(3) ODT function is not available during self-refresh.

(4) Self-refresh exit (SRE) is asynchronous.

(5) The Deselect (DES) command performs the same function as No Operation (NOP).

(6) The Power down mode does not perform any self-refresh operation.

2.4.1 Mode Register Set (MRS or EMRS)

DDR3 SDRAM contains mode and extended mode registers that configure the DDR3 memory for operation. These registers control burst type, burst length, CAS latency, DLL enable/disable, etc.

The DDR3 memory controller programs the mode and extended mode registers of the DDR3 memory by issuing MRS and EMRS commands. MRS and EMRS commands can be issued during DDR3 initialization as well as during normal operation as long as the external SDRAM is in idle state. When the MRS or EMRS command is executed, the value on DDRBA [1:0] selects the mode register to be written and the data on DDRA [12:0] is loaded into the register. DDRA [15:13] and DDRBA [2] are reserved and are programmed to 0 during MRS (or EMRS).

Each mode register allows programming of different sets of DDR3 SDRAM parameters. The DDR3 memory controller programs the mode registers in compliance with the JEDEC JESD79-3E spec. For more information about mode registers and how they are programmed, see the JEDEC spec.

2.4.2 Refresh Mode

The DDR3 memory controller issues refresh commands (REF) to the DDR3 SDRAM device. REF is automatically preceded by a Precharge-all (PREA) command, ensuring the deactivation of all CE spaces and banks selected.

Following the PREA command, the DDR3 memory controller begins performing refreshes at a rate defined by the refresh rate (REFRESH_RATE) field in the SDRAM refresh control register (SDRFC). In general, a refresh command needs to be issued to the DDR3 SDRAM regularly every tREFI interval. To allow for efficient operation, refresh commands can be postponed a maximum of 8 times. Also, at any given time a maximum of 16 refresh commands can issued within a 2 xtREFI interval. For more information on refresh command timing, see the JEDEC spec.

2.4.3 Activation

The ACTIVE command is used to open (or activate) a row in a specific bank for a subsequent access. DDRBA [2:0] select the bank, and the address provided on DDRA[15:0] selects the row. This row remains active (or open) for accesses until a precharge command is issued to that bank. A PRECHARGE command must be issued before opening a different row in the same bank.

When the DDR3 memory controller issues an ACT command, a delay of tRCD is incurred before a read or write command is issued. Reads or writes to the currently active row and bank of memory can achieve much higher throughput than reads or writes to random areas because every time a new row is accessed, the ACT command must be issued and a delay of tRCD incurred.

2.4.4 Deactivation

The precharge command is used to deactivate the open row in a particular bank (PRE) or the open row in all banks (PREA). The bank(s) will be available for a subsequent row activation a specified time (tRP) after the precharge command is issued, except in the case of concurrent auto precharge, where a read or write command to a different bank is allowed as along as it does not interrupt the data transfer in the current bank and does not violate any other timing parameters. A PRE command is allowed if there is no open row in that bank (idle state) or if the previously open row is already in the process of precharging. During a PREA command, DDRA [10] is driven high to ensure deactivation of all banks.

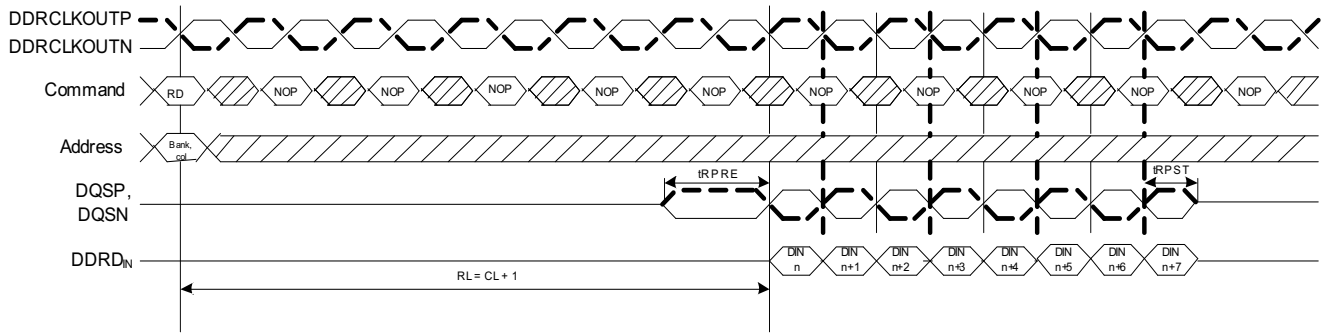
2.4.5 READ Command

Figure 2-2 shows the DDR3 memory controller performing a read burst from DDR3 SDRAM. The READ command initiates a burst read operation to an active row. The column address is driven on DDRA [15:0], and the bank address is driven on DDRBA [2:0].

The DDR3 memory controller uses a burst length of 8, and has a programmable CAS latency of 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15 or 16. The CAS latency is five cycles in Figure 2-2. In this figure it has been programmed to CL + 1. Because the default burst size is 8, the DDR3 memory controller returns 8 words of data for every read command. Word size is nothing but the DDR3 interface bus width.

If additional accesses are not pending to the DDR3 memory controller, the read burst completes and the unneeded data is disregarded. If additional accesses are pending, based on the arbitration result, the DDR3 memory controller can terminate the read burst and start a new read burst.

Figure 2-2. READ Command



NOP commands are shown for ease of illustration ; other commands may be valid at these times

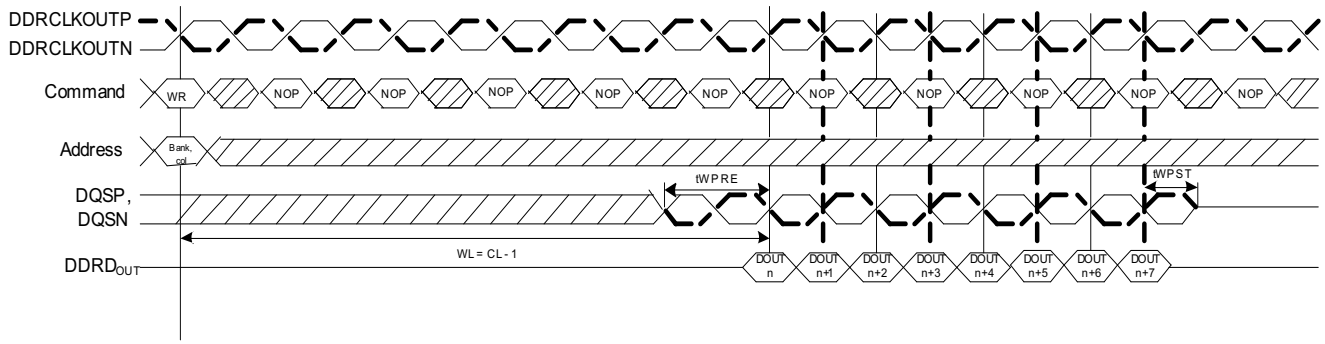
2.4.6 Write (WR) Command

Prior to a WRT command, the desired bank and row are activated by the ACT command. Following the WRT command, a write latency is incurred. Write latency is equal to CAS latency minus 1. All writes have a burst length of 8.

Figure 2-3 shows the timing for a write on the DDR3 memory controller. If the transfer request is for less than 8 words, depending on the scheduling result and the pending commands, the DDR3 memory controller can:

- Mask out the additional data using DDRDQM outputs
- Terminate the write burst and start a new write burst

Figure 2-3. WRITE Command



NOP commands are shown for ease of illustration; other commands may be valid at these times

2.5 Address Mapping

The DDR3 memory controller views external DDR3 SDRAM as one continuous block of memory across the two chip-selects. If smaller devices are used, the memory is seen to roll over. The DDR3 memory controller receives DDR3 memory access requests along with a 33-bit logical address from the rest of the system. The controller uses the logical address to generate a row/page, column, bank address, and chip selects for the DDR3 SDRAM. The number of bank and column address bits used is determined by the IBANK and PAGESIZE fields. The chip selection pins used are determined by the EBANK field (Table 2-4).

Table 2-4. Bank Configuration Register Fields for Address Mapping

Bit Field	Bit Value	Bit Description
IBANK		Defines the number of internal banks on external DDR3 memory
	0	1 bank
	1h	2 banks
	2h	4 banks
	3h	8 banks
PAGESIZE		Defines the page size of each page of the external DDR3 memory
	0	256 words (requires 8 column address bits)
	1h	512 words (requires 9 column address bits)
	2h	1024 words (requires 10 column address bits)
	3h	2048 words (requires 11 column address bits)
EBANK		External chip select setup. Defines whether SDRAM accesses use 1 or 2 chip select lines
	0	Use only chip enable 0 for all SDRAM accesses
	1	Use chip enables 0 and 1 for SDRAM accesses

NOTE: IBANK should always be programmed to 3h since DDR3 memory devices offer only 8-bank support unlike DDR2 with the option of 4-bank or 8-bank memory devices.

As the source address increments across SDRAM page boundaries, the DDR3 controller moves to the same page in the next bank on the current device (chip select).

After the page has been accessed in all banks of the current device, the same page is accessed in all banks in the next device. This is followed by accessing the next page in the first device and the process continues. To the DDR3 SDRAM, this process looks as shown on Figure 2-5. Thus, the DDR3 controller exploits this traversal across internal banks and chip selects while remaining on the same page to maximize the number of open SDRAM banks within the overall SDRAM space. See Figure 2-5.

Thus 16 banks (eight internal banks across two chip selects) can be kept open at a time, interleaving among all of them.

Table 2-5. Logical Address-to-SDRAM Address Mapping

Logical Address [32:N]							
Row Address		Chip Select		Bank Address[2:0]		Column Address	
ROW SIZE	nrb	EBANK	ncs	IBANK	nbb	PAGE SIZE	ncb
Don't care	16 bits	0	0 bits	0	0 bits	0	8 bits
		1	1 bit	1	1 bit	1	9 bits
				2	2 bits	2	10 bits
				3	3 bits	3	11 bits
Logical address mapping for row address		Logical address mapping for chip select		Logical address mapping for bank address[1:0]		Logical address mapping for column address	
MSB	LSB	MSB	LSB	MSB	LSB	MSB	LSB
M3+nrb-1	M3+1	M3=M2+ ncs-1	M2+1	M2=M1+ nbb-1	M1+1	M1=N+ ncb-1	N

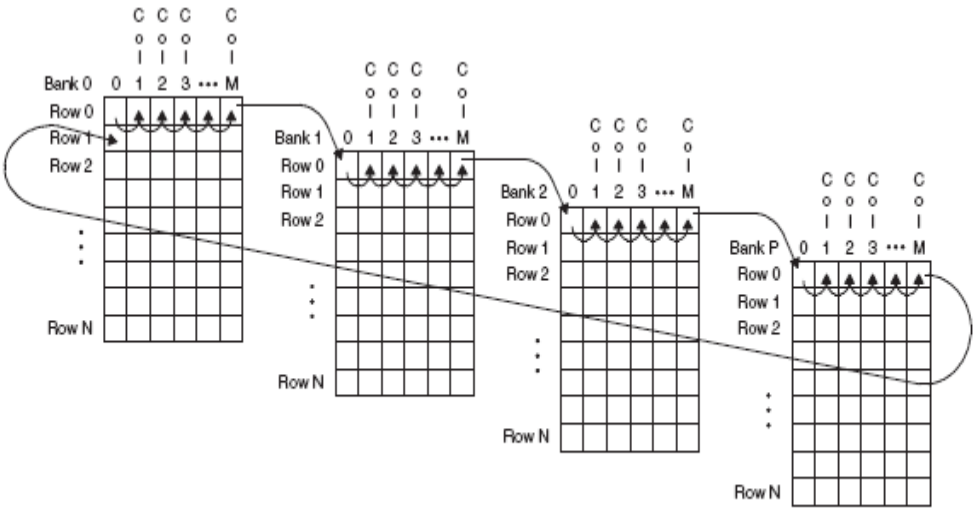
NOTE: N=1 for 16-bit SDRAM, N=2 for 32-bit SDRAM and N=3 for 64-bit SDRAM. ROWSIZE is kept for legacy reasons but is not used by the DDR3 controller. nrb = Number of row bits. ncs = Number of chip select bits. nbb = Number of bank select bits determined by bank address [2:0].

Figure 2-4. Logical Address-to-DDR3 SDRAM Address Map (EBANK=0)

Col. 0	Col. 1	Col. 2	Col. 3	Col. 4	• • •	Col. M–1	Col. M	
					• • •			Row 0, bank 0
					• • •			Row 0, bank 1
					• • •			Row 0, bank 2
•	•	•	•	•	• • •	•	•	•
•	•	•	•	•	• • •	•	•	•
•	•	•	•	•	• • •	•	•	•
					• • •			Row 0, bank P
					• • •			Row 1, bank 0
					• • •			Row 1, bank 1
					• • •			Row 1, bank 2
•	•	•	•	•	• • •	•	•	•
•	•	•	•	•	• • •	•	•	•
•	•	•	•	•	• • •	•	•	•
					• • •			Row 1, bank P
					• • •			•
					• • •			•
					• • •			•
					• • •			Row N, bank 0
					• • •			Row N, bank 1
					• • •			Row N, bank 2
•	•	•	•	•	• • •	•	•	•
•	•	•	•	•	• • •	•	•	•
•	•	•	•	•	• • •	•	•	•
					• • •			Row N, bank P

A M is number of columns (as determined by PAGESIZE) minus 1, P is number of banks (as determined by IBANK) minus 1, and N is number of rows (as determined by both PAGESIZE and IBANK) minus 1.

Figure 2-5. DDR3 SDRAM Column, Row, and Bank Access (EBANK=0)



A M is number of columns (as determined by PAGESIZE) minus 1, P is number of banks (as determined by IBANK) minus 1, and N is number of rows (as determined by both PAGESIZE and IBANK) minus 1.

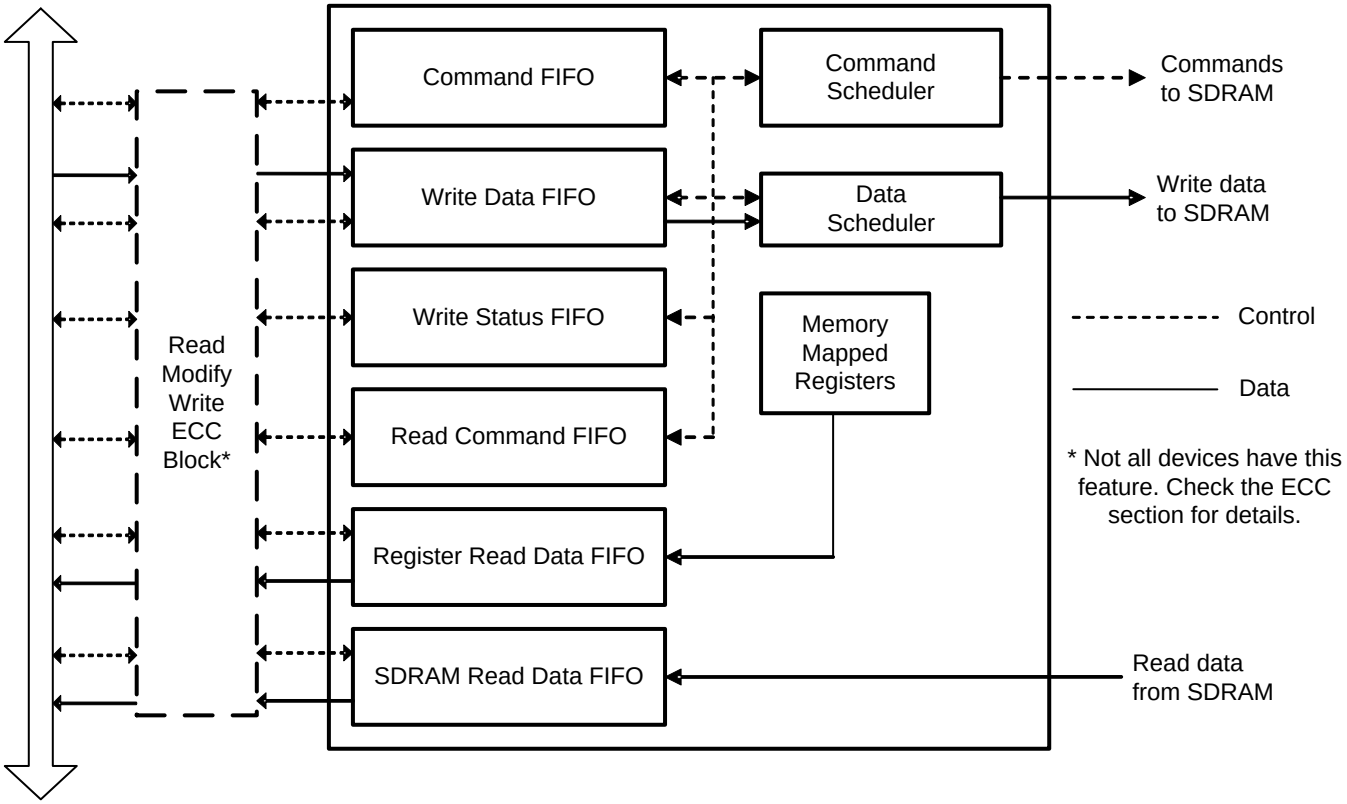
2.6 DDR3 Memory Controller Interface

To move data efficiently from on-chip resources to an external DDR3 SDRAM device, the DDR3 memory controller makes use of a Command FIFO, a Write Data FIFO, a Write Status FIFO, a Read Command FIFO, and two Read Data FIFOs and command and data schedulers. Table 2-6 describes the purpose of each FIFO. Figure 2-6 shows the block diagram of the DDR3 memory controller FIFOs. Commands, write data, and read data arrive at the DDR3 memory controller parallel to each other. The same peripheral bus is used to write and read data from external memory as well as internal memory-mapped registers (MMR).

Table 2-6. DDR3 Memory Controller FIFO Description

FIFO	Description	Depth
Command	Stores all commands coming from on-chip requestors	16
Write Data	Stores write data coming from on-chip requestors to memory	20 (512-bit wide)
Write Status	Stores the write status information for each write transaction	7
Read Command	Stores all read transactions that are to be issued to on-chip requestors	28
SDRAM Read Data	Stores read data coming from SDRAM memory to on-chip requestors	28 (256-bit wide)
Register Read Data	Stores read data coming from MMRs to on-chip requestors	2 (256-bit wide)

Figure 2-6. DDR3 Memory Controller FIFO Block Diagram



2.6.1 Arbitration

The DDR3 memory controller performs command reordering and scheduling in an attempt to achieve efficient transfers with maximum throughput. The goal is to maximize the utilization of the data, address, and command buses while hiding the overhead of opening and closing DDR3 SDRAM rows. Command reordering takes place within the command FIFO.

The DDR3 memory controller examines all the commands stored in the command FIFO to schedule commands to the external memory. For each master, the DDR3 memory controller reorders the commands based on the following rules:

- The DDR3 controller will advance a read command before an older write command from the same master if the read is to a different block address (2048 bytes) and the read priority is equal to or greater than the write priority.
- The DDR3 controller will block a read command, regardless of the master or priority if that read command is to the same block address (2048 bytes) as an older write command.

Thus, one pending read or write for a master might exist.

- Among all pending reads, the DDR3 controller selects all reads that have their corresponding SDRAM banks already open.
- Among all pending writes, the DDR3 controller selects all writes that have their corresponding SDRAM banks already open.

As a result of the above reordering, several pending reads and writes may exist that have their corresponding banks open. The highest priority read is selected from pending reads, and the highest priority write from pending writes. If two or more commands have the highest priority, the oldest command is selected. As a result, there might exist a final read and a final write command. Either the read or the write command will be selected depending on the value programmed in the Section 4.27.

The DDR3 controller supports interleaving of commands for maximum efficiency. In other words, the controller will partially execute one command and switch to executing another higher priority command before finishing the first command.

Apart from reads and writes the DDR3 controller also needs to open and close SDRAM banks, and maintain the refresh counts for an SDRAM. The priority of SDRAM commands with respect to refresh levels are as follows:

1. (Highest priority) SDRAM refresh request due to Refresh Must level of refresh urgency reached.
2. Read request without a higher priority write (from the reordering algorithm above)
3. Write request.
4. SDRAM Activate commands.
5. SDRAM Deactivate commands.
6. SDRAM Power-Down request.
7. SDRAM refresh request due to Refresh May or Release level of refresh urgency reached.
8. (Lowest priority) SDRAM self-refresh request.

2.6.2 Command Starvation

While running the scheduling algorithm described in Section 2.6.1, the DDR3 memory controller is subject to the following:

1. A continuous stream of high priority commands can block lower priority commands.
2. A continuous stream of SDRAM commands to a row in an open bank can block commands to another row in the same bank.

To avoid a continuous blocking effect, the priority of the oldest command is momentarily raised over all other commands when the latency counter for the oldest command expires. The latency counter for the oldest command (PR_OLD_COUNT) is configurable in the Latency Configuration Register. In addition to this, the order of command accesses can also be tailored by grouping commands into two categories or "classes" and assigning different latency expiration counters to each category. See Section 2.6.4 for more information.

On top of the above scheduling, the highest priority condition is a removal of hard or soft reset. If this occurs, the DDR3 controller abandons whatever it is currently doing and commences its startup sequence. In this case, commands and data stored in the FIFOs are lost. The startup sequence also commences whenever the SDRAM Config register is written and INITREF_DIS field in SDRAM Refresh Control register (SDRFC) is set to 0. In this case, commands and data stored in the FIFOs are not lost. The DDR3 controller will ensure that in-flight read or write transactions to the SDRAM are complete before starting the initialization sequence.

2.6.3 Possible Race Condition

A race condition may exist when certain masters write data to the DDR3 memory controller. For example, if master A passes a software message via a buffer in DDR3 memory and does not wait for indication that the write completes, when master B attempts to read the software message it may read stale data and therefore receive an incorrect message. In order to confirm that a write from master A has landed before a read from master B is performed, master A must wait for the write to complete before indicating to master B that the data is ready to be read. For example, an EDMA transfer controller should wait for the transfer completion event to occur before signaling a CorePac to read the message from DDR3.

If master A does not wait for indication that a write is complete, it must perform the following workaround:

1. Perform the required write.
2. Perform a dummy write to the DDR3 memory controller module ID and revision register.
3. Perform a dummy read to the DDR3 memory controller module ID and revision register.
4. Indicate to master B that the data is ready to be read after completion of the read in step 3. The completion of the read in step 3 ensures that the previous write was done.

2.6.4 Class of Service

The commands in the Command FIFO can be mapped to two classes of service: 1 and 2. The mapping of commands to a particular class of service can be done based on the priority or the master ID. The mapping based on priority can be done by setting the appropriate values in the Priority to Class of Service Mapping register. The mapping based on master ID can be done by setting the appropriate values of master ID and the masks in the Master ID to Class of Service Mapping registers.

There are three master ID and mask values that can be set for each class of service. In conjunction with the masks, each class of service can have a maximum of 144 master IDs mapped to it. For example, a master ID value of 0xFF along with a mask value of 0x3 will map all master IDs from 0xF8 to 0xFF to that particular class of service. By default all commands will be mapped to class of service 2.

Each class of service has an associated latency counter. The value of this counter can be set in the Latency Configuration register. When the latency counter for a command expires, i.e., reaches the value programmed for the class of service that the command belongs to, that command will be the one that is executed next. If there is more that one command that has expired latency counters, the command with the highest priority will be executed first. One exception to this rule is as follows: if any of the commands with the expired latency counters is also the oldest command in the queue, that command will be executed first irrespective of priority. This is done to prevent a continuous block effect as described in Section 2.6.1.

2.7 Refresh Scheduling

The DDR3 controller uses two counters to schedule AUTO REFRESH commands:

- a 13-bit decrementing refresh interval counter
- a four-bit refresh backlog counter

The interval counter is loaded with the REFRESH_RATE field value at reset. The interval counter decrements by one each cycle until it reaches zero at which point it reloads from REFRESH_RATE and restarts decrementing. The counter also reloads and restarts decrementing whenever the REFRESH_RATE field is updated.

The refresh backlog counter records the number of AUTO REFRESH commands that are currently outstanding. The backlog counter increments by one each time the interval counter reloads (unless it has reached its maximum value of 15). The backlog counter decrements by one each time the DDR3 controller issues an AUTO REFRESH command (unless it is already at zero). Following a refresh command, the DDR3 memory controller waits T_RFC cycles, defined in the SDRAM timing 3 register (SDTIM1), before rechecking the refresh urgency level.

For the range of values that the backlog counter can take, there are three levels of urgency with which the DDR3 controller should perform an auto refresh cycle (in which it issues AUTO REFRESH commands), as follows:

- Refresh May level is reached whenever the backlog count is greater than 0, to indicate that there is a refresh backlog, so if the DDR3 controller is not busy and none of the SDRAM banks are open, it should perform an auto refresh cycle.
- Refresh Release level is reached whenever the backlog count is greater than 4, to indicate that the refresh backlog is getting high, so if the DDR3 controller is not busy it should perform an auto refresh cycle even if any banks are open.
- Refresh Must level is reached whenever the backlog count is greater than 7, to indicate that the refresh backlog is getting excessive and the DDR3 controller should perform an auto refresh cycle before servicing any new memory access requests.

The DDR3 controller starts servicing new memory accesses after Refresh Release level is cleared. If any of the commands in the Command FIFO have class-of-service latency counters that are expired, the DDR3 controller will not wait for Refresh Release level to be cleared but will only perform one refresh command and exit the refresh state.

The refresh counters do not operate when SDRAM has been put into self-refresh mode. Also, the refresh counters start tracking the missed refreshes only after initialization is complete.

2.8 Self-Refresh Mode

The DDR3 memory controller supports self-refresh mode for low power. The controller maintains DDRCKE low to maintain the self-refresh state. In self-refresh, the memory maintains valid data while consuming a minimal amount of power.

Self-refresh mode is set by programming the LP_MODE in the Power Management Control register (PMCTL) to 2. The controller automatically puts the SDRAM into self-refresh after the controller is idle for SR_TIM DDR3CLKOUT cycles. (See Section 4.9 for more information.)

The memory is brought out of self-refresh under any of the following conditions:

- If the LP_MODE field is set not equal to 2
- A memory access is requested
- SR_TIM bit in PMCTL is cleared

In a situation where memory accesses and a self-refresh command are sent to the DDR3 memory controller, the controller always prioritizes the memory access. Thus, if a reset is triggered when memory accesses and a self-refresh command are queued in the controller, it is likely that self-refresh will not be entered.

The user must ensure that all memory accesses have been completed, and verify that self-refresh is set in the STATUS register before initiating a reset.

NOTE: The DDR3 memory controller completes all pending memory accesses and refreshes before it puts SDRAM into self-refresh. If a request for a memory access is received, the DDR3 memory controller services the memory access request then returns to the self-refresh state upon completion.

2.8.1 Extended Temperature Range

The normal operating temperature range for DDR3 SDRAMs is typically 0 to 85°C. When operating in self-refresh mode within the extended temperature range (85°C to 95°C), the memory device must be refreshed at 2× the normal refresh rate. For this purpose, either the auto self-refresh (ASR) or self-refresh temperature (SRT) feature should be used. Under normal operating conditions, both ASR and SRT should be disabled (equal to 0). When ASR is enabled, the internal refresh rate of the SDRAM automatically switches to 2× the refresh rate when the operating case temperature Tc is greater than 85°C when in Self-refresh mode. When SRT is enabled, the internal refresh rate of the SDRAM is forced to 2× the refresh rate regardless of Tc. Both SRT and ASR cannot be enabled at the same time. One must be disabled if the other is enabled.

NOTE: ASR and SRT are used only in self-refresh mode (LP_MODE=0×2). When operating in extended temperature range with LP_MODE = 0×0 (not in self-refresh), it is up to the user to program the manual refresh rate to 2× the normal refresh rate for proper operation. If it is guaranteed that Tc will exceed 85°C, it is recommended that SRT=1 to force the refresh rate to 2× regardless of operating temperature.

2.9 Reset Considerations

The DDR3 memory controller can be reset through a hard reset or a soft reset. A hard reset resets the state machine, the FIFOs, and the internal registers. A soft reset only resets the state machine and the FIFOs. A soft reset does not reset the internal registers except for the interrupt registers. Register accesses cannot be performed while either reset is asserted.

The DDR3 memory controller hard and soft reset are derived from device-level resets. Table 2-7 shows the relationship between the device-level resets and the DDR3 memory controller resets. For more information on the device-level resets, see the device-specific data manual.

Table 2-7. Device and DDR3 Memory Controller Reset Relationship

DDR3 Memory Controller	Reset Effect	Initiated by
Hard reset	Resets control logic and all DDR3 memory controller registers	• Please refer to the reset controller description in your device data manual
Soft reset	Resets control logic and interrupt registers	• Please refer to the reset controller description in your device data manual

2.10 Turnaround Time

Table 2-8 shows the turn around time that the DDR3 memory controller introduces on the data bus for various back-to-back accesses. Note that the DDR3 memory controller takes advantage of the CAS latencies and packs the commands as close as possible on the control bus to introduce the following turn around time on the data bus.

Table 2-8. Turnaround Time

Previous Access	Next Access	Turnaround Time (DDR3 memory clock cycles)
SDRAM Write	SDRAM Write to same chip select	0
SDRAM Write	SDRAM Write to different chip select	T CSTA + 1
SDRAM Read	SDRAM Read to same chip select	0
SDRAM Read	SDRAM Read to different chip select	T CSTA + 1
SDRAM Write	SDRAM Read	T WTR + 1 + CL
SDRAM Read	SDRAM Write	T_RTW + 1

2.11 DDR3 SDRAM Memory Initialization

DDR3 SDRAM initialization is achieved by programming memory mapped registers in the DDR3 controller configuration space and the DDR3 PHY configuration space in a specific sequence. The software programming sequence is described in the Keystone II DDR3 Initialization Application Note. This sequence of software programming steps, causes the controller to issue MRS and EMRS commands to program mode and extended mode registers in the SDRAM device. These registers control parameters such as burst type, burst length, and CAS latency. The sequence of commands during the initialization sequence described in Section 2.11.1. The initialization sequence performed by the DDR3 memory controller is compliant with the JESD79-3E specification.

The DDR3 memory controller performs the initialization sequence under the following conditions:

- Automatically following a hard or soft reset (see Section 2.11.1)
- Following a write to the SDRAM configuration register (SDCFG) (see Section 2.11.1)

At the end of the initialization sequence, the DDR3 memory controller performs an auto-refresh cycle, leaving the DDR3 memory controller in an idle state with all banks deactivated.

During the initialization sequence, the DDR3 memory controller issues MRS and EMRS commands that configure the DDR3 SDRAM mode registers with the values described in Table 2-9 and Table 2-10.

When a reset occurs, the DDR3 memory controller immediately begins the initialization sequence. Under this condition, commands and data stored in the DDR3 memory controller FIFOs will be lost. However, when the initialization sequence is initiated by a write to the SDCFG Register, data and commands stored in the DDR3 memory controller FIFOs will not be lost and the DDR3 memory controller will ensure read and write commands are completed before starting the initialization sequence.

As the default values of the Mode Register (MR) and extended mode registers 1, 2, 3 are not defined, contents of Mode/Extended Mode Registers must be fully initialized and/or reinitialized, i.e., written, after power up and/or reset for proper operation. Also the contents of the Mode/Extended Mode Registers can be altered by re-executing the MRS/EMRS command during normal operation. The mode/extended mode registers are selected by varying the bank address bits BA [1:0]. BA [2] and A [15:13] are reserved for future use and must be programmed to zero.

The extended mode register 3 is configured with a value of 0h.

Table 2-9. DDR3 SDRAM Extended Mode Register 2 Configuration(1)

Mode Register Bit	Mode Register Field	Init Value	Description
15-11	Reserved	0x0	Reserved
10-9	Rtt_WR	SDCFG.DYN _ODT and MR2.RTTWR	Dynamic ODT value from SDRAM Config Register and MR2.RTTWR (program both to same value)
8	Reserved	0x0	Reserved
7	SRT	MR2 .SRT	Self-Refresh temperature range from MR2 register
6	ASR	MR2 .ASR	Auto self-refresh enable from MR2 register
5-3	CWL	SDCFG.CWL	CAS write latency from SDRAM Config register
2-0	PASR	SDRCR.PASR	Partial array self-refresh from SDRAM Refresh Control register

(1) Bank Address bits to select EMR 2 are BA [1:0] = 0x2.

Table 2-10. DDR3 SDRAM Extended Mode Register 1 Configuration(1)

Mode Register Bit	Mode Register Field	Init Value	Description
12	Qoff	0x0	Output Buffer Enabled
11	TDQS	0x0	TDQS enable/disable
10	Reserved	0x0	Reserved
9	Rtt_nom	SDCFG.DDRTERM[2]	DDR3 termination resistor value from SDRAM Config register
8	Reserved	0x0	Reserved
7	Level	0x0	Write Leveling Disabled
6	Rtt_nom	SDCFG.DDRTERM[1]	DDR3 termination resistor value from SDRAM Config register
5	Output driver impedance	SDCFG.SDRAM _DRIVE[1]	SDRAM drive strength from SDRAM Config register
4-3	Additive Latency	0x0	Additive latency = 0
2	Rtt_nom	SDCFG.DDRTERM [0]	DDR3 termination resistor value from SDRAM Config register
1	Output driver impedance	SDCFG.SDRAM _DRIVE[0]	SDRAM drive strength from SDRAM Config register
0	DLL Enable	0x0	DLL enable/disable from SDRAM Config register

(1) Bank Address bits to select EMR 1 are BA [1:0] = 0x1.

Table 2-11. DDR3 SDRAM Mode Register 0 Configuration(1)

Mode Register Bit	Mode Register Field	Init Value	Description
12	DLL control for Precharge PD	0x0	Fast exit active powerdown exit time
11-9	Write Recovery	SDTIM1.T_WR	Write recovery for auto precharge from SDAM Timing 1 Register
8	DLL Reset	0x1	DLL Reset
7	Mode	0x0	Normal Mode from SDRAM Config Register
6-4	CAS Latency	SDCFG.CL[3:1]	CAS Latency from SDRAM Config Register
3	Read Burst Type	0x0	sequential/interleave burst type
2	CAS Latency	SDCFG.CL[0]	CAS Latency from SDRAM Config Register
1-0	Burst length	0x0	Burst length of 8

(1) Bank Address bits to select MR are BA [1:0] = 0x0.

2.11.1 DDR3 Initialization Sequence

On coming out of reset if the SDRAM_TYPE field in the SDRAM Config register is equal to 3 and the INITREF_DIS bit in the SDRAM Refresh Control register is set to 0, the DDR3 Controller performs a DDR3 SDRAM initialization sequence. The sequence follows the JEDEC standard. Please refer to the JEDEC spec for the initialization sequence.

The DDR3 memory controller also performs the initialization sequence whenever the SDRAM Config register is written. But in this case, the sequence starts at step 3. The DDR3 memory controller does not perform any transactions until the DDR3 initialization sequence is complete.

2.12 Leveling

The DDR3 controller supports leveling to compensate for the command and DQS skew as a result of the fly-by topology. Leveling compensates the skew for both reads and writes. Unlike Keystone I devices, the controller in Keystone II devices does not require the user to program initial leveling values (INIT_RATIOs) to establish the starting point of the search window before triggering hardware leveling. The logic inside the DDR PHY is able to automatically search for and determine the optimal starting point when leveling and training sequence is triggered by writing to the PHY Initialization Register (PIR). Please refer to the DDR3 initialization application note for software programming sequence to initialize DDR3 on Keystone II devices.

2.13 Interrupt Support

The DDR3 memory controller generates one error interrupt. Please check the section on interrupts in the device data manual for details on how the ECC error interrupt is routed. The source of the interrupt can be checked in the Interrupt Raw Status Register.

2.14 EDMA Event Support

The DDR3 memory controller is a DMA slave peripheral and therefore does not generate EDMA events. Data read and write requests may be made directly by masters including the EDMA controller.

2.15 Emulation Considerations

The DDR3 memory controller will remain fully functional during emulation halts to allow emulation access to external memory.

2.16 ECC

For data integrity, the DDR3 memory controller supports ECC on the data written to or read from the ECC protected address ranges in memory. The ECC algorithm is a single-error-correct-double-error-detect (SECDED) algorithm and uses the (72,64) Hamming code. Eight-bit ECC is calculated over 64-bit data quanta. ECC is enabled by setting ECC_EN = 1 in the ECC Control register and DXEN=1 in the DATX8 8 General configuration register (DX8GCR register). ECC is disabled by setting ECC_EN and DXEN=0. By default, ECC_EN=0 and DXEN=1. The address ranges can be programmed in the ECC Address Range 1 and 2 register. The system must ensure that any bursts accesses starting in the ECC protected region must not cross over into the unprotected region and vice-versa. The controller on some KeyStone II devices supports an additional read-modify-write (RMW) feature. This feature can be enabled by programming RMW_EN = 1 in the ECC Control register.

For memory controllers that do not support RMW, all accesses to ECC protected space must be 64-bit aligned and multiples of 64 bits.

For memory controllers that support RMW, ECC protected space can be used regardless of the alignment or quanta conditions, if RMW_EN=1. If RMW_EN=0, the controller will again assume the same 64-bit alignment and quanta conditions.

Silicon rev1.0 and 1.1 of K2K and K2H device family do not support RMW. Other K2K and K2H silicon revisions and all revisions in the K2E and K2L family support RMW.

NOTE: The ECC is stored inside the SDRAM during writes. After enabling ECC and before performing any functional reads or writes, all DDR3 memory space configured as ECC should be first written with known data that is 64-bit aligned and multiples of 64-bit. This is to ensure the correct ECC values are stored in the ECC SDRAM prior to functional use.

If the RMW ECC feature is not supported (or is disabled for the devices that do support it), a write access with byte count that is not a multiple of 64-bit quanta, or with a non-64-bit-aligned address performed within the address range protected by ECC, will result in a write ECC error interrupt. In this case, the DDR3 memory controller writes to the SDRAM. However, the ECC value written to the SDRAM will be corrupted. The controller will NOT trigger a write ECC error if a write access with a multiple of 64-bit quanta and with 64-bit aligned address but with partial byte enables set, is performed within the address range protected by ECC (this can be the case if the Multicore Navigator PktDMA writes to a descriptor placed in DDR3). The data and corrupted ECC value will be written to the SDRAM, but will go undetected and may be detected as 1-bit or 2-bit errors when read back.

When RMW is enabled (ECC_EN=1 and RMW_EN=1), the controller will perform a RMW operation if a write results in a sub-64-bit access. For details on how the RMW operations are performed, refer to Section 2.16.1.1.

The ECC is read and verified during reads if ECC_EN=1 and ECC_VERIFY_EN=1 in the ECC control register. Similar to RMW, K2K and K2H silicon revisions 1.0 and 1.1 do not support ECC_VERIFY_EN, but K2K and K2H revisions beyond rev1.1 and all K2E/K2L revisions support it. For the latter, ECC verification is disabled during reads if ECC_VERIFY_EN=0.

If there is a one-bit error, the DDR3 memory controller corrects the data and sends it on the read interface. For 2-bit errors, the DDR3 memory controller generates a read ECC error interrupt. Note that in both cases, the data in SDRAM is still corrupted. It is the responsibility of system software to go and correct the data in the SDRAM.

NOTE: The user should note that the single error correct, double error detect (SECDED) algorithm used by the ECC logic cannot detect more than 2-bit errors per 64-bit quanta. For these errors, the output of the algorithm is unknown i.e. it may erroneously detect as 1-bit, 2-bit or no errors. More than 2-bit errors are expected to be very rare in a well designed system.

See Section 4.24 through Section 4.26 for ECC-related registers.

NOTE: To disable ECC, program ECC_EN=0 in the ECC Control register (inside DDR3 controller) and DXEN=0 in the DATX8 8 General Configuration Register (see the DDR PHY registers) before triggering the leveling sequence in the PHY Initialization Register. By default, DXEN =1 so ECC byte lane will be enabled from the perspective of the PHY.

2.16.1 ECC Feature Enhancements

2.16.1.1 Read-modify-write

As seen in Figure 2-6, the Read-Modify-Write (RMW) module is placed prior to internal FIFO logic of the controller. The RMW module splits all writes to an SDRAM into a burst size of 64-bytes and converts any sub-quanta write into a RMW of aligned burst size (64 bytes). A quanta is defined as 8 bytes. Read bursts are not fragmented.

The RMW module has been designed such that normal aligned ECC block read or write bursts are unaffected. That is, they pass through without adding delay as well as maintaining all memory coherence. If RMW module detects write data that does not form a complete quanta, a read for that burst (64 bytes) is then issued by the controller. This return data burst is then merged with the sub-quanta write data and the modified 64-byte burst is then written to the SDRAM. For write commands with partial byte enables (such as those introduced by a Packet DMA peripheral), the active byte enables are passed through without any latency, but a write-read-modify-write (wRMW) is performed for the burst with partial byte enables.

The controller maintains coherence across all outstanding commands in the command FIFO whether or not they are affected by the RMW module and also follows the normal command arbitration outlined in section 2.6.1. The above RMW process for sub-quanta writes means the execution of the write command will be delayed compared to if the command was not sub-quanta and was 64-bit aligned.

2.16.1.2 Logging 1-bit ECC Error Address

For 1-bit ECC error, the controller logs the starting address of the SDRAM burst in an internal 2-deep address FIFO. This internal FIFO stores the first two 1-bit ECC errors. The 1-Bit ECC Error Address Log register will display the address on top of the internal FIFO. Software must write a 0x1 to the 1-bit ECC Address Log register to pop the FIFO and display the next address stored. The FIFO will be loaded with the address for the next 1-bit ECC error if it is not full. It must be noted that no address comparison will be performed, i.e., if a single address has ECC errors back-to-back, that address will be logged twice.

2.16.1.3 Counting the Number of 1-bit ECC Errors

The number of 1-bit ECC errors can be counted using the 1-Bit ECC Error Count register. The controller also supports programming a threshold and a window in the 1-Bit ECC Error Threshold register. The window is programmed in number of refresh periods. When the programmed window value is a 0, i.e., window is disabled, and the internal error count exceeds the programmed threshold, the controller will generate a 1-bit ECC error interrupt. When servicing the interrupt, software will need to set the error count with a value less than the threshold for the interrupt to be triggered again. When the programmed window value is non-zero, i.e., window is enabled, the controller will generate a 1-bit ECC error interrupt only if the internal error count exceeds the programmed threshold in that window. The internal error count is reset every time the window expires. Software can use this to gauge the degree of 1-bit ECC errors occurring in the system.

2.16.1.4 Diagnosing the Data bus bit on which 1-bit ECC Errors Occur

For diagnosis, the controller supports 1-Bit ECC Error Distribution register that represent whether an error has occurred in a given bit location on the data. This is advantageous to detect whether the errors are random or systemic. The distribution register will be overlay of all 1-bit ECC errors until the software clears the register. Therefore, multiple bits could be set as a result of multiple 1-bit ECC errors occurring over multiple read accesses.

For 2-bit ECC errors, the controller will generate a 2-bit ECC error interrupt. It must be noted that the controller will detect but not correct 2-bit ECC errors. The controller will generate an ECC error interrupt and send the resultant data from the ECC correction logic. The read data received from the memory may have further been corrupted by the ECC correction logic since it will have attempted to correct the read data but failed due to uncorrectable error.

2.16.1.5 Logging 2-bit ECC Error Address

For all uncorrectable ECC errors listed above, the controller will log the starting address of the SDRAM burst in the 2-Bit ECC Error Address Log register. The register will show the address of the first uncorrectable error. After the software clears the register, it will be loaded with the address for the next uncorrectable error.

Please check the section on interrupts in the device data manual for details on how the ECC error interrupt is routed. The source of the ECC error interrupt can be checked in the Interrupt Raw Status Register.

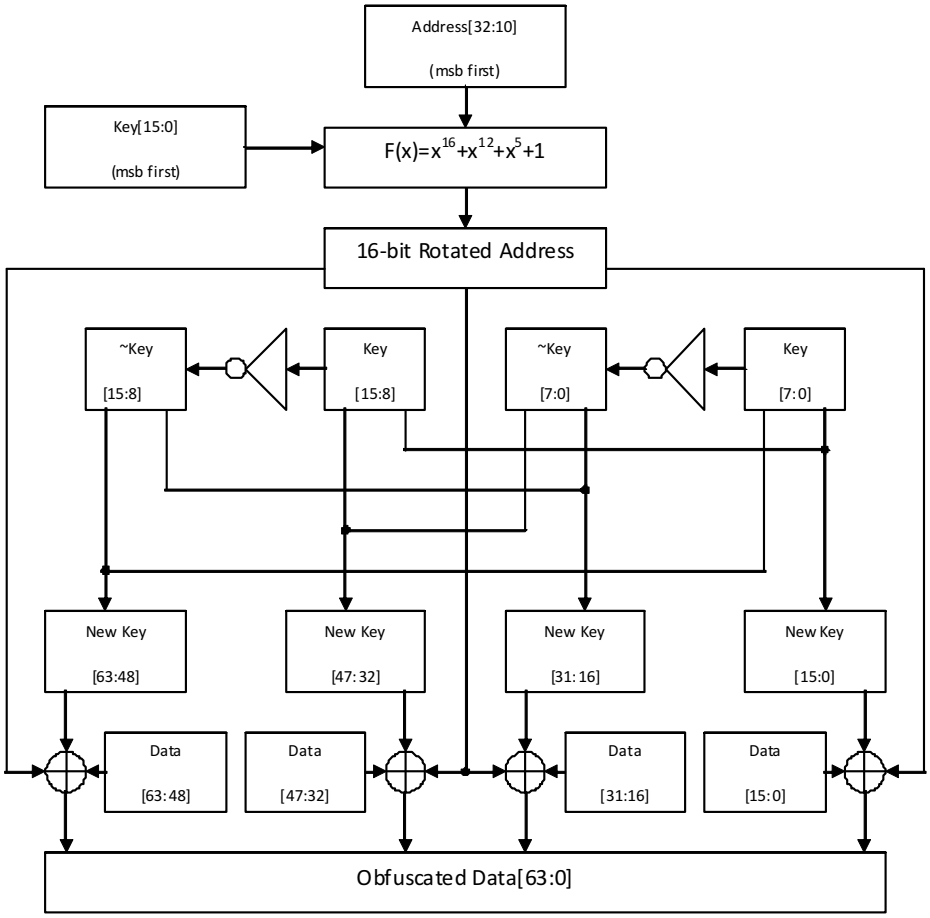
2.17 Data Bus Obfuscation

For security, the controller supports obfuscation for data written to the SDRAM. Data written to the memory mapped registers is not obfuscated.

NOTE: Obfuscation is available only on secure TI SoCs. For more information, contact a TI sales office for additional information.

The obfuscation scheme is shown in the figure below.

Figure 2-7. Data Bus Obfuscation



Obfuscation is enabled by setting the OBFUSCATION_ENABLE bit inside the Security Manager to 1. This causes the obfuscation key to be latched inside the controller. The 16-bit key should be programmed by software inside the Security Manager.

NOTE: Since the key is latched when obfuscation is enabled, the key should not be modified further.

The key is further modified to create a 64-bit new key. Data going out from the controller during writes will be obfuscated and data coming back during reads will be de-obfuscated. As seen from the figure, the obfuscation logic makes use of the upper address bits to ensure that obfuscation is different for different regions of memory.

Further, the data is also XOR'd with four copies of the 16-bit rotated address and the new key to ensure that obfuscation is also unique for each 1KB page of memory.

Enabling obfuscation does not increase the latency on command execution.

2.18 Power Management

2.18.1 SDRAM Self-Refresh Mode

(See Section 2.8.)

2.18.2 SDRAM Power-Down Mode

The DDR3 memory controller supports power-down mode. Automatic power-down is enabled by setting the LP_MODE field in the Power Management Control register (PMCTL) to 4. The memory is put into power-down after the controller is idle for PD_TIM number of DDR3CLKOUT cycles. In power-down mode, the DDR3 memory controller does not stop the clocks to the memory. The controller maintains DDRCKE low to maintain the power-down state. When the SDRAM is in power-down, the DDR3 memory controller services register accesses as normal.

The memory is brought out of power-down under any of the following conditions:

- If the LP_MODE field is set not equal to 4
- A memory access is requested
- Refresh Must level is reached

2.19 Performance Monitoring

The DDR3 controller provides a set of performance counter registers which can be used to monitor or calculate the bandwidth and efficiency of the DDR traffic. The counters can be configured to count events such as total number of SDAM accesses, SDRAM activates, reads, write and so on. The Performance Counter 1 and 2 Registers (PERF_CNT_1 and PERF_CNT_2) act as two 32-bit counters that are able to count events independent of each other. To provide more granularity the counters can also be configured to filter events originating from a particular master or address space. The events to be counted and filter enabled are programmed in the Performance Counter Config Register (PERF_CNT_CFG). The actual value of the filter is programmed in Performance Counter Master Region Select Register (PERF_CNT_SEL). The counters start counting the events independently when commands enter the Command FIFO.

The CNTRN_CFG (N=1,2) fields in the PERF_CNT_CFG register are used to select the event for the counter to count. The PERF_CNT_CFG also includes options to enable or disable the master (CNTRN_MSTID_EN) and address space (CNTRN_REGION_EN) filters for each counter. The filters are disabled by default. If the respective filters are enabled, the master ID value and region select options can be programmed in the PERF_CNT_SEL register. It should be noted that the master ID and region select filters apply only to a certain subset of events that can be counted. The table below shows the events for which the filters are applicable.

Table 2-12. Performance Counter Filter Configuration

PERF_CNT_CFG. [CNTR_CFG]	Event Selected for counting	PERF_CNT_CFG. [CTNR_REGION_EN]	PERF_CNT_CFG. [CNTR_MSTID_EN]
0x0	Total SDRAM accesses	NA	0 - Disable, 1 - Enable
0x1	Total SDRAM activates	NA	0 - Disable, 1 - Enable
0x2	Total Reads	0 - Disable, 1 - Enable	0 - Disable, 1 - Enable
0x3	Total Writes	0 - Disable, 1 - Enable	0 - Disable, 1 - Enable
0x4	Number of DDR/2 clock cycles Command FIFO is full	NA	NA
0x5	Number of DDR/2 clock cycles Write Data FIFO is full	NA	NA
0x6	Number of DDR/2 clock cycles Read Data FIFO is full	NA	NA
0x7	Number of DDR/2 clock cycles Write Status FIFO is full	NA	NA
0x8	Number of priority elevations	0 - Disable, 1 - Enable	0 - Disable, 1 - Enable
0x9	Number of DDR/2 clock cycles that a command was pending	NA	NA
0xA	Number of DDR/2 clock cycles for which DDR i/f was transferring data	NA	NA
0xB (only applies to devices that support RMW)	Number of SDRAM read bursts resulting from RMW and wRMW accesses	NA	NA
0xC (only applies to devices that support RMW)	Number of SDRAM write bursts resulting from RMW and wRMW accesses	NA	0 - Disable, 1 - Enable
0x D - 0XF	Reserved		

See Chapter 4 for details on Performance counter registers.

Using the DDR3 Memory Controller

The following sections show various ways to connect the DDR3 memory controller to DDR3 memory devices. The steps required to configure the DDR3 memory controller for external memory access are also described.

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3.1 Connecting the DDR3 Memory Controller to DDR3 SDRAM 38
3.2 Configuring DDR3 Memory Controller Registers to Meet DDR3 SDRAM Specifications 42

3.1 Connecting the DDR3 Memory Controller to DDR3 SDRAM

The following figures show high-level views of the three memory topologies:

- Figure 3-1
- Figure 3-2
- Figure 3-3

All DDR3 SDRAM devices must comply with the JESD79-3C standard.

Not all of the memory topologies shown may be supported by your device. For more information, see the device-specific data manual.

The printed-circuit-board (PCB) layout rules and connection requirements between the DSP and the memory device are described in a separate document. For more information, see the device-specific data manual.

Figure 3-1. Connecting Two 16 MB x 16 x 8 Banks (4Gb Total) Devices

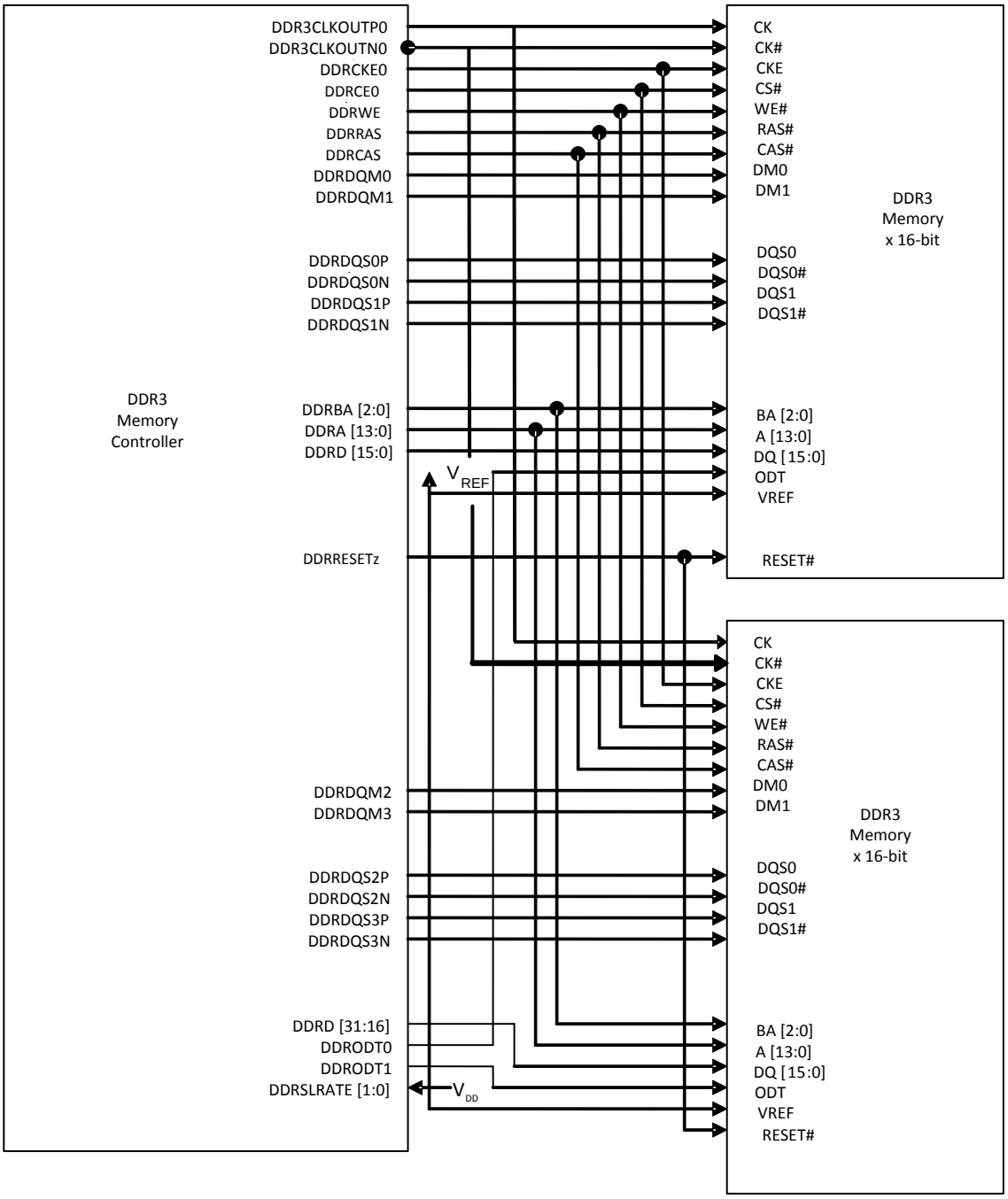


Figure 3-2. Connecting One 8 MB x 16 x 8 Banks (1Gb Total) Device

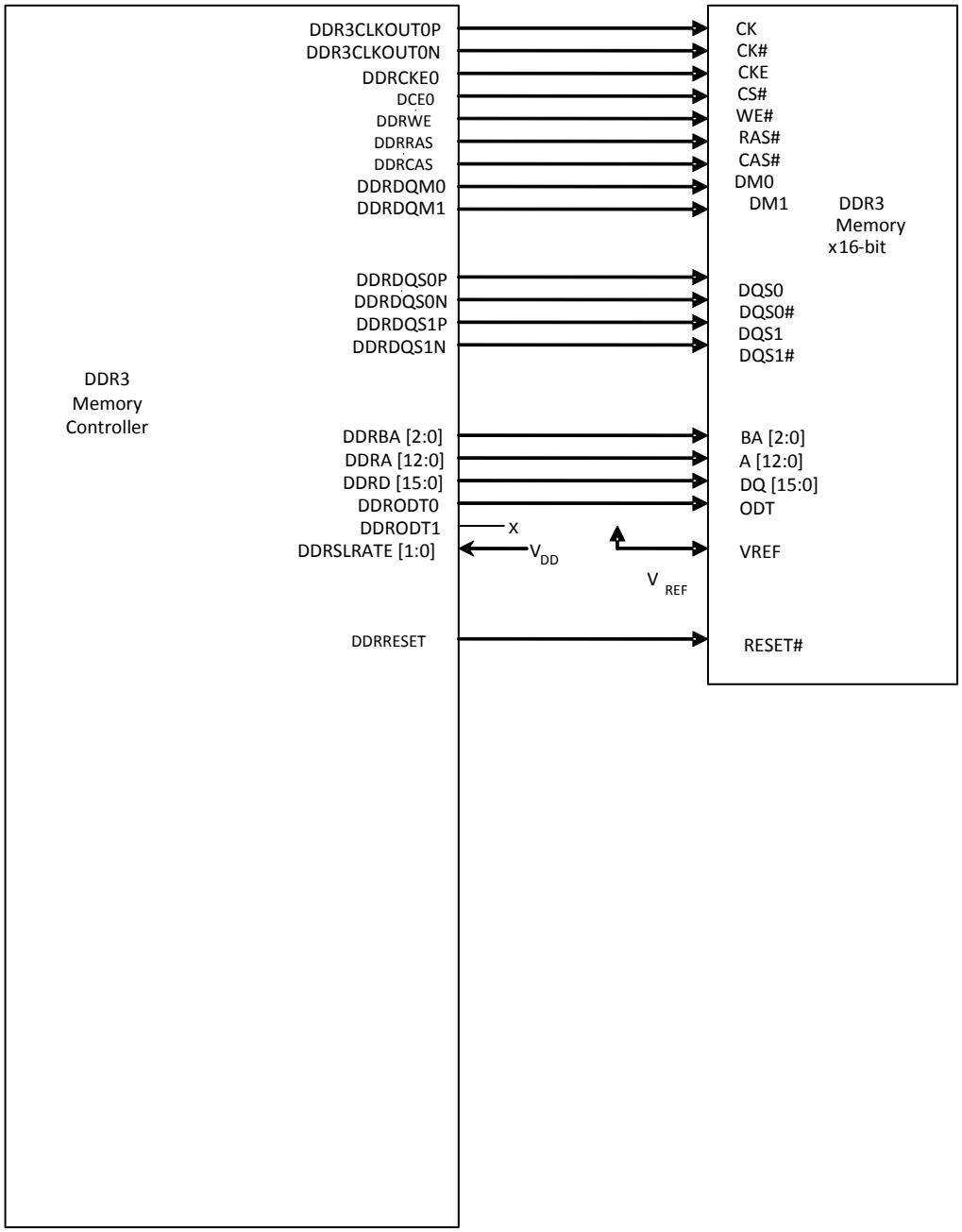
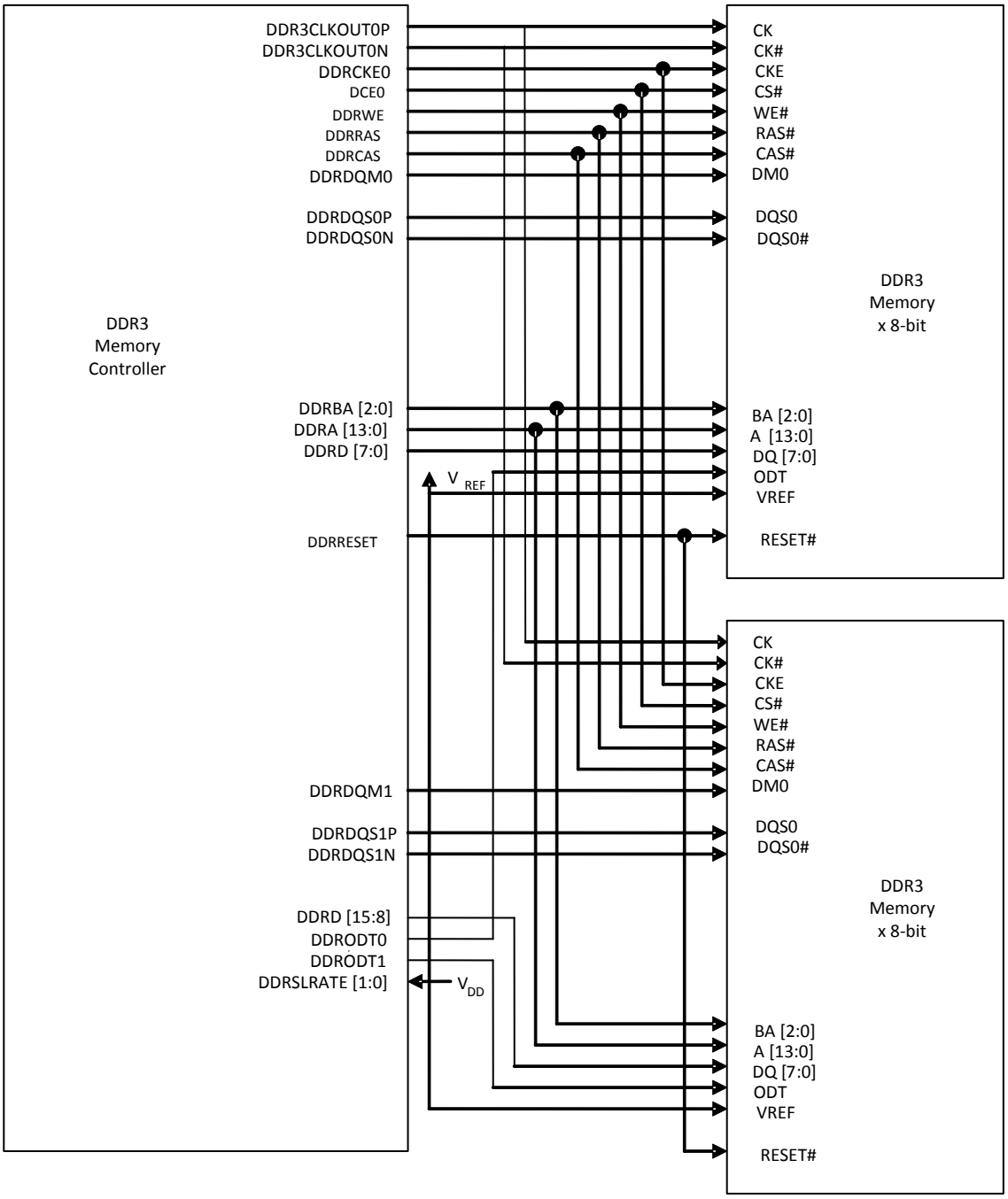


Figure 3-3. Connecting Two 16 MB x 8 x 8 Banks (2Gb Total) Devices



3.2 Configuring DDR3 Memory Controller Registers to Meet DDR3 SDRAM Specifications

The DDR3 memory controller allows a high degree of programmability for shaping DDR3 accesses. This provides the DDR3 memory controller with the flexibility to interface with a variety of DDR3 devices. By programming the SDRAM Configuration Register (SDCFG), SDRAM Refresh Control Register (SDRFC), SDRAM Timing 1 Register (SDTIM1), SDRAM Timing 2 Register (SDTIM2) , SDRAM Timing 3 Register (SDTIM3) and SDRAM Timing 4 Register (SDTIM4), the DDR3 memory controller can be configured to meet the data sheet specification for JESD79-3E compliant DDR3 SDRAM devices. The timing values also need to be programmed in the DRAM Timing Parameter Registers 0-2 inside the PHY block.

As an example, the following sections describe how to configure each of these registers for access to two 1 Gb, 16-bit wide DDR3 SDRAM devices connected as shown on Figure 3-2, where each device has the following configuration:

- Maximum data rate: 1333 MHz
- Number of banks: 8
- Page size: 1024 words
- CAS latency: 9

It is assumed that the frequency of the DDR3 memory controller clock (DDR3CLKOUT) is set to 666.5 MHz.

3.2.1 Programming the SDRAM Configuration Register (SDCFG)

The SDRAM configuration register (SDCFG) contains register fields that configure the DDR3 memory controller to match the data bus width, CAS latency, number of banks, and page size of the attached DDR3 memory.

Table 3-1 shows the resulting SDCFG configuration.

Table 3-1. SDCFG Configuration

Field	Value	Function Selection
SDRAM_TYPE	0x3h	SDRAM Type Select – DDR3
NM	1h	To configure the DDR3 memory controller for a 32-bit data bus width.
CL	10h	To select a CAS latency of 9.
IBANK	3h	To select 8 internal DDR3 banks.
EBANK	0	To select only DCE0z to be used.
PAGESIZE	2h	To select 1024-word page size.

3.2.2 Programming the SDRAM Refresh Control Register (SDRFC)

The SDRAM refresh control register (SDRFC) configures the DDR3 memory controller to meet the refresh requirements of the attached DDR3 device. SDRFC also allows the DDR3 memory controller to enter and exit self refresh.

The REFRESH_RATE field in SDRFC is defined as the rate at which the attached DDR3 device is refreshed in DDR3 cycles. The value of this field may be calculated using the following equation:

REFRESH_RATE = DDR3CLKOUT frequency × memory refresh period (1)

According to the DDR3 JEDEC standard, on reset de-assertion the DDRCKE pin must remain low for at least 500µs before becoming active during power-up initialization. This is achieved by programming a 500 µs refresh period in the SDRFC prior to initialization.

Table 3-2 shows the DDR3-1333 refresh rate specification.

Table 3-2. DDR3 Memory Refresh Specification

Symbol	Description	Value
t_{REFI}	Refresh interval to be programmed during power-up initialization	500 µs
t_{REFI}	Average Periodic Refresh Interval (after power-up initialization)	7.8 µs

The refresh rate of 500 µs to be programmed during power-up initialization should be calculated equal to a divide-by-16 value as follows. The DDR3 controller takes care of the divide-by-16 internal logic.

REFRESH_RATE = (666.5 MHz × 500 µs)/16 = 515Ch (2)

After power-up initialization, the refresh rate of 7.8 µs should be programmed as follows:

REFRESH_RATE = 666.5 MHz × 7.8 µs = 1450h (3)

NOTE: SRT and ASR should be programmed in the MR2 register inside the DDR PHY config space.

3.2.3 Configuring SDRAM Timing Registers (SDTIM1, SDTIM2, SDTIM3, SDTIM4)

The SDRAM timing 1 register (SDTIM1), SDRAM timing 2 register (SDTIM2), SDRAM timing 3 register (SDTIM3), SDRAM timing 4 register (SDTIM4) configure the DDR3 memory controller to meet the datasheet timing parameters of the attached DDR3 device. Each field in SDTIM1, SDTIM2, SDTIM3, SDTIM4 corresponds to a timing parameter in the DDR3 datasheet specification. Table 3-3, Table 3-4, and Table 3-5 show the register field name and corresponding DDR3 datasheet parameter name and value. These tables also provide a formula to calculate the register field value and show the resulting calculation. Each of the equations includes a minus 1 because the register fields are defined in terms of DDR3 clock cycles minus 1. (See Section 4.5- Section 4.8 for more information.). Some of these timing parameters will also have to be programmed in the DRAM Timing Parameter Registers (See Section 4.49 - Section 4.51)

The objective behind programming the timing values is to calculate them in terms of DRAM clock cycles and round off to the next highest integer value. For example, at 666.5 MHz, the clock period t_{CK} = 1.5 ns. So 13.5 ns will be programmed as (13.5/1.5)-1= 9 - 1 = 8 DDR3 clock cycles and 14ns will be 9 DDR3 clock cycles.

Table 3-3. See the register section for the SDTIM* register where the field exists

Register Field Name	DDR3 SDRAM Datasheet Parameter Name	Description	Datasheet Value (ns)	Formula (Register Field must be >=)	Field Value (h)
T_RP	t_{RP}	Precharge to Activate or Refresh command	13.5	(t_{RP}/t_{CK}) – 1	8
T_RCD	t_{RCD}	Activate command to Read/Write command	13.5	(t_{RCD}/t_{CK}) – 1	8
T_WR	t_{WR}	Write recovery time	6	(t_{WR}/t_{CK}) – 1	3
T_RAS	t_{RAS}	Active to precharge command	36	(t_{RAS}/t_{CK}) – 1	17
T_RC	t_{RC}	Activate to Activate command in same bank	49.5	(t_{RC}/t_{CK}) – 1	20
T_RRD	t_{RRD}	Activate to Activate in different bank	t_{FAW} = 30ns	($t_{FAW}/(4*t_{CK})$) – 1	4
T_WTR	t_{WTR}	Write to Read command delay	6	(t_{WTR}/t_{CK}) – 1	3

Table 3-4. See the register section for the SDTIM* register where the field exists

Register Field Name	DDR3 SDRAM Datasheet Parameter Name	Description	Datasheet Value (ns)	Formula (Register Field must be >=)	Field Value (h)
T_RTP	t_{RTP}	Read to precharge command delay	6	(t_{RTP}/t_{CK}) – 1	3
T_CKE	t_{CKE}	CKE minimum pulse width	3(t_{CK} cycles)	(t_{CKE}) – 1	2
T_XP	t_{XP}	Power-down exit to non-read command	5(t_{CK} cycles)	(t_{XP}) – 1	4

Table 3-5. See the register section for the SDTIM* register where the field exists

Register Field Name	DDR3 SDRAM Datasheet Parameter Name	Description	Datasheet Value (ns)	Formula (Register Field must be >=)	Field Value (h)
T_CSTA	DDR controller parameter	Refer to SDTIM 4 Register	—	—	5
T_RFC	t_{RFC}	Refresh cycle time	110	(t_{RFC}/t_{CK}) –1	49
T_ZQCS	t_{ZQcs}	ZQCS command time	64(t_{CK} cycles)	(t_{ZQcs}) –1	3F

DDR3 Memory Controller Registers

Table 4-1 lists the memory-mapped registers for the DDR3 memory controller. For the memory address of these registers, see the device-specific data manual.

Table 4-1. DDR3 Memory Controller Registers (See datasheet memory map for base address)

Offset	Acronym	Register Description	Section
000h	MIDR	Module ID and Revision Register	Section 4.1
004h	STATUS	DDR3 Memory Controller Status Register	Section 4.2
008h	SDCFG	SDRAM Configuration Register	Section 4.3
010h	SDRFC	SDRAM Refresh Control Register	Section 4.4
018h	SDTIM1	SDRAM Timing 1 Register	Section 4.5
01Ch	SDTIM2	SDRAM Timing 2 Register	Section 4.6
020h	SDTIM3	SDRAM Timing 3 Register	Section 4.7
028h	SDTIM4	SDRAM Timing 4 Register	Section 4.8
038h	PMCTL	Power Management Control Register	Section 4.9
0x54h	LAT_CONFIG	VBUSM Configuration Register	Section 4.10
0x80	PERF_CNT_1	Performance Counter 1 Register	Section 4.11
0x84	PERF_CNT_2	Performance Counter 2 Register	Section 4.12
0x88	PERF_CNT_CFG	Performance Counter Config Register	Section 4.13
0x8C	PERF_CNT_SEL	Performance Counter Master Region Select Register	Section 4.14
0x90	PERF_CNT_TIM	Performance Counter Time Register	Section 4.15
0A4h	IRQSTATUS_RAW_SYS	Interrupt Raw Status Register	Section 4.16
0ACh	IRQ_STATUS_SYS	Interrupt Status Register	Section 4.17
0B4h	IRQENABLE_SET_SYS	Interrupt Enable Set Register	Section 4.18
0BCh	IRQENABLE_CLR_SYS	Interrupt Enable Clear Register	Section 4.19
0C8h	ZQCONFIG	SDRAM Output Impedance Calibration Configuration Register	Section 4.20
100h	PRI_COS_MAP	Priority To Class-Of-Service Mapping Register	Section 4.21
104h	MSTID_COS_1_MAP	Master ID to Class-Of-Service 1 Mapping Register	Section 4.22
108h	MSTID_COS_2_MAP	Master ID to Class-Of-Service 2 Mapping Register	Section 4.23
110h	ECCCTL	ECC Control Register	Section 4.24
114h	ECCADDR1	ECC Address Range 1 Register	Section 4.25
118h	ECCADDR2	ECC Address Range 2 Register	Section 4.26
120h	RWTHRESH	Read Write Execution Threshold Register	Section 4.27
130h	ONE_BIT_ECC_ERR_CNT	1-Bit ECC Error Count Register	Section 4.28
134h	ONE_BIT_ECC_ERR_THRSH	1-Bit ECC Error Threshold Register	Section 4.29
138h	ONE_BIT_ECC_ERR_DST_1	1-Bit ECC Error Distribution 1 Register	Section 4.30
13Ch	ONE_BIT_ECC_ERR_ADDR_LOG_1	1-Bit ECC Error Address Log Register	Section 4.31
140h	TWO_BIT_ECC_ERR_ADDR_LOG_1	2-Bit ECC Error Address Log Register	Section 4.32
144h	ONE_BIT_ECC_ERR_DST_2	1-Bit ECC Error Distribution 2 Register	Section 4.33

Table 4-2. DDR3 PHY Registers (See device datasheet for base address)

Offset	Acronym	Register Description	Section
004h	PIR	PHY Initialization Register	Section 4.34
008h	PGCR0	PHY General Configuration Register 0	Section 4.35
00Ch	PGCR1	PHY General Configuration Register 1	Section 4.36
010h	PGSR0	PHY General Status Register 0	Section 4.38
014h	PGSR1	PHY General Status Register 1	Section 4.39
018h	PLLCR	PLL Control Register	Section 4.40
01Ch	PTR0	PHY Timing Register 0	Section 4.41
020h	PTR1	PHY Timing Register 1	Section 4.42
024h	PTR2	PHY Timing Register 2	Section 4.43
028h	PTR3	PHY Timing Register 3	Section 4.44
02Ch	PTR4	PHY Timing Register 4	Section 4.45
038h	ACIOCR	AC I/O Configuration Register	Section 4.46
03Ch	DXCCR	DATX8 Common Configuration Register	Section 4.47
044h	DCR	DRAM Configuration Register	Section 4.48
048h	DTPR0	DRAM Timing Parameters Register 0	Section 4.49
04Ch	DTPR1	DRAM Timing Parameters Register 1	Section 4.50
050h	DTPR2	DRAM Timing Parameters Register 2	Section 4.51
054h	MR0	Mode Register 0	Section 4.52
058	MR1	Mode Register 1	Section 4.53
05C	MR2	Mode Register 2	Section 4.54
060h	MR3	Mode Register 3	Section 4.55
064	ODTCR	ODT Configuration Register	Section 4.56
068	DTCR	Data Training Configuration Register	Section 4.57
08C	PGCR2	PHY General Configuration Register 2	Section 4.37
180h	ZQ0CR0	ZQ 0 Impedance Control Register 0	Section 4.58
184h	ZQ0CR1	ZQ 0 Impedance Control Register 1	Section 4.59
188h	ZQ0SR0	ZQ 0 Impedance Status Register 0	Section 4.60
18Ch	ZQ0SR1	ZQ 0 Impedance Status Register 1	Section 4.61
190h	ZQ1CR0	ZQ 1 Impedance Control Register 0	Section 4.58
194h	ZQ1CR1	ZQ 1 Impedance Control Register 1	Section 4.59
198h	ZQ1SR0	ZQ 1 Impedance Status Register 0	Section 4.60
19Ch	ZQ1SR1	ZQ 1 Impedance Status Register 1	Section 4.61
1A0h	ZQ2CR0	ZQ 2 Impedance Control Register 0	Section 4.58
1A4h	ZQ2CR1	ZQ 2 Impedance Control Register 1	Section 4.59
1A8h	ZQ2SR0	ZQ 2 Impedance Status Register 0	Section 4.60
1ACh	ZQ2SR1	ZQ 2 Impedance Status Register 1	Section 4.61
1B0h	ZQ3CR0	ZQ 3 Impedance Control Register 0	Section 4.58
1B4h	ZQ3CR1	ZQ 3 Impedance Control Register 1	Section 4.59
1B8h	ZQ3SR0	ZQ 3 Impedance Status Register 0	Section 4.60
1BCh	ZQ3SR1	ZQ 3 Impedance Status Register 1	Section 4.61
1C0h	DX0GCR	DATX8 0 General Configuration Register	Section 4.62
1C4h	DX0GSR0	DATX8 0 General Status Register 0	Section 4.63
1C8h	DX0GSR1	DATX8 0 General Status Register 1	Section 4.64
1E0h	DX0LCDLR0	DATX8 0 Local Calibrated Delay Line Register 0	Section 4.65
1E4h	DX0LCDLR1	DATX8 0 Local Calibrated Delay Line Register 1	Section 4.66
1E8h	DX0LCDLR2	DATX8 0 Local Calibrated Delay Line Register 2	Section 4.67
1ECh	DX0MDLR	DATX8 0 Master Delay Line Register	Section 4.68
1F0h	DX0GTR	DATX8 0 General Timing Register	Section 4.69

Table 4-2. DDR3 PHY Registers (See device datasheet for base address) (continued)

Offset	Acronym	Register Description	Section
1F4h	DX0GSR2	DATX8 0 General Status Register 2	Section 4.64
200h	DX1GCR	DATX8 1 General Configuration Register	Section 4.62
204h	DX1GSR0	DATX8 1 General Status Register 0	Section 4.63
208h	DX1GSR1	DATX8 1 General Status Register 1	Section 4.64
220h	DX1LCDLR0	DATX8 1 Local Calibrated Delay Line Register 0	Section 4.65
224h	DX1LCDLR1	DATX8 1 Local Calibrated Delay Line Register 1	Section 4.66
228h	DX1LCDLR2	DATX8 1 Local Calibrated Delay Line Register 2	Section 4.67
22Ch	DX1MDLR	DATX8 1 Master Delay Line Register	Section 4.68
230h	DX1GTR	DATX8 1 General Timing Register	Section 4.69
234h	DX1GSR2	DATX8 1 General Status Register 2	Section 4.64
240h	DX2GCR	DATX8 2 General Configuration Register	Section 4.62
244h	DX2GSR0	DATX8 2 General Status Register 0	Section 4.63
248h	DX2GSR1	DATX8 2 General Status Register 1	Section 4.64
260h	DX2LCDLR0	DATX8 2 Local Calibrated Delay Line Register 0	Section 4.65
264h	DX2LCDLR1	DATX8 2 Local Calibrated Delay Line Register 1	Section 4.66
268h	DX2LCDLR2	DATX8 2 Local Calibrated Delay Line Register 2	Section 4.67
26Ch	DX2MDLR	DATX8 2 Master Delay Line Register	Section 4.68
270h	DX2GTR	DATX8 2 General Timing Register	Section 4.69
274h	DX2GSR2	DATX8 2 General Status Register 2	Section 4.64
280h	DX3GCR	DATX8 3 General Configuration Register	Section 4.62
284h	DX3GSR0	DATX8 3 General Status Register 0	Section 4.63
288h	DX3GSR1	DATX8 3 General Status Register 1	Section 4.64
2A0h	DX3LCDLR0	DATX8 3 Local Calibrated Delay Line Register 0	Section 4.65
2A4h	DX3LCDLR1	DATX8 3 Local Calibrated Delay Line Register 1	Section 4.66
2A8h	DX3LCDLR2	DATX8 3 Local Calibrated Delay Line Register 2	Section 4.67
2ACh	DX3MDLR	DATX8 3 Master Delay Line Register	Section 4.68
2B0h	DX3GTR	DATX8 3 General Timing Register	Section 4.69
2B4h	DX3GSR2	DATX8 3 General Status Register 2	Section 4.64
2C0h	DX4GCR	DATX8 4 General Configuration Register	Section 4.62
2C4h	DX4GSR0	DATX8 4 General Status Register 0	Section 4.63
2C8h	DX4GSR1	DATX8 4 General Status Register 1	Section 4.64
2E0h	DX4LCDLR0	DATX8 4 Local Calibrated Delay Line Register 0	Section 4.65
2E4h	DX4LCDLR1	DATX8 4 Local Calibrated Delay Line Register 1	Section 4.66
2E8h	DX4LCDLR2	DATX8 4 Local Calibrated Delay Line Register 2	Section 4.67
2ECh	DX4MDLR	DATX8 4 Master Delay Line Register	Section 4.68
2F0h	DX4GTR	DATX8 4 General Timing Register	Section 4.69
2F4h	DX4GSR2	DATX8 4 General Status Register 2	Section 4.64
300h	DX5GCR	DATX8 5 General Configuration Register	Section 4.62
304h	DX5GSR0	DATX8 5 General Status Register 0	Section 4.63
308h	DX5GSR1	DATX8 5 General Status Register 1	Section 4.64
320h	DX5LCDLR0	DATX8 5 Local Calibrated Delay Line Register 0	Section 4.65
324h	DX5LCDLR1	DATX8 5 Local Calibrated Delay Line Register 1	Section 4.66
328h	DX5LCDLR2	DATX8 5 Local Calibrated Delay Line Register 2	Section 4.67
32Ch	DX5MDLR	DATX8 5 Master Delay Line Register	Section 4.68
330h	DX5GTR	DATX8 5 General Timing Register	Section 4.69
334h	DX5GSR2	DATX8 5 General Status Register 2	Section 4.64
340h	DX6GCR	DATX8 6 General Configuration Register	Section 4.62

Table 4-2. DDR3 PHY Registers (See device datasheet for base address) (continued)

Offset	Acronym	Register Description	Section
344h	DX6GSR0	DATX8 6 General Status Register 0	Section 4.63
348h	DX6GSR1	DATX8 6 General Status Register 1	Section 4.64
360h	DX6LCDLR0	DATX8 6 Local Calibrated Delay Line Register 0	Section 4.65
364h	DX6LCDLR1	DATX8 6 Local Calibrated Delay Line Register 1	Section 4.66
368h	DX6LCDLR2	DATX8 6 Local Calibrated Delay Line Register 2	Section 4.67
36Ch	DX6MDLR	DATX8 6 Master Delay Line Register	Section 4.68
370h	DX6GTR	DATX8 6 General Timing Register	Section 4.69
374h	DX6GSR2	DATX8 6 General Status Register 2	Section 4.64
380h	DX7GCR	DATX8 7 General Configuration Register	Section 4.62
384h	DX7GSR0	DATX8 7 General Status Register 0	Section 4.63
388h	DX7GSR1	DATX8 7 General Status Register 1	Section 4.64
3A0h	DX7LCDLR0	DATX8 7 Local Calibrated Delay Line Register 0	Section 4.65
3A4h	DX7LCDLR1	DATX8 7 Local Calibrated Delay Line Register 1	Section 4.66
3A8h	DX7LCDLR2	DATX8 7 Local Calibrated Delay Line Register 2	Section 4.67
3ACh	DX7MDLR	DATX8 7 Master Delay Line Register	Section 4.68
3B0h	DX7GTR	DATX8 7 General Timing Register	Section 4.69
3B4h	DX7GSR2	DATX8 7 General Status Register 2	Section 4.64
3C0h	DX8GCR	DATX8 8 General Configuration Register	Section 4.62
3C4h	DX8GSR0	DATX8 8 General Status Register 0	Section 4.63
3C8h	DX8GSR1	DATX8 8 General Status Register 1	Section 4.64
3E0h	DX8LCDLR0	DATX8 8 Local Calibrated Delay Line Register 0	Section 4.65
3E4h	DX8LCDLR1	DATX8 8 Local Calibrated Delay Line Register 1	Section 4.66
3E8h	DX8LCDLR2	DATX8 8 Local Calibrated Delay Line Register 2	Section 4.67
3ECh	DX8MDLR	DATX8 8 Master Delay Line Register	Section 4.68
3F0h	DX8GTR	DATX8 8 General Timing Register	Section 4.69
3F4h	DX8GSR2	DATX8 8 General Status Register 2	Section 4.64

4.1 Module ID and Revision Register (MIDR)

The Module ID and Revision register contains the revision number and identification data of the DDR3 peripheral, and is described in the following figure and table.

Figure 4-1. Module ID and Revision Register (MIDR)

31 30	29 28	27 16	15 11	10 8	7 6	5 0
REG_SCHEME	Reserved	MOD_ID	Reserved	MJ_REV	Reserved	MIN_REV
R=0x1	R=0x0	R=0x46	R=0x3 or 0x6	R=0x4	R=0x0	R=0x1 or 0x2

Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-3. Module ID and Revision Register (MIDR) Field Descriptions

Bit	Field	Attribute	Description
31:30	REG_SCHEME	R	Value=0x1. Used to distinguish between old and current revision schemes. 0 means old scheme. 1 means new scheme.
29-28	Reserved	R	Value = 0x0
27-16	MOD_ID	R	Value = 0x46 Module ID Bits
15-11	Reserved	R	Value = 0x3 or 0x6 Reserved. The reserved field always reads as 0x3 or 0x6. A value written to this field has no effect.
10-8	MJ_REV	R	Value = 0x4 Major Revision
7-6	Reserved	R	Value = 0x0 Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.
5-0	MIN_REV	R	Value = 0x1 or 0x2 Minor Revision

4.2 DDR3 Memory Controller Status Register (STATUS)

This register contains the status of the DDR3 module and is described in the following figure and table.

Figure 4-2. DDR3 Memory Controller Status Register (STATUS)

31	30	29	28	27	26	25	3	2	1	0
BE	Reserved		OBF_STAT	SELF_REF	PWRDN	Reserved		IFRDY	Reserved	
R=0	R=0		R=0R	R=0	R=0	R=0R		R=0R	R=0	

Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-4. DDR3 Memory Controller Status Register (STATUS) Field Descriptions

Bit	Field	Attribute	Description
31	BE	R	Big Endian. Reflects the value on the BIG_ENDIAN port that defines whether the EMIF is in big or little-endian mode
30-29	Reserved	R	Value = 0 This field is tied off to 0x1.
28	OBF_STAT	R	Obfuscation Status. • 0 = Obfuscation disabled. • 1 = Obfuscation enabled.
27	SELF_REF	R	Self refresh mode status. • 0 = SDRAM is not in self refresh mode. • 1 = SDRAM is in self refresh mode.
26	PWRDN	R	Power down status. • 0 = SDRAM is not in power down mode. • 1 = SDRAM is in power down mode.
25-3	Reserved	R	Reserved. A value written to this field has no effect
2	IFRDY	R	DDR3 memory controller interface logic ready bit. The interface logic controls the signals used to communicate with DDR3 SDRAM devices. This bit displays the status of the interface logic. • 0 = Interface logic is not ready; either powered down, not ready, or not locked. • 1 = Interface logic is powered up, locked and ready for operation.
1-0	Reserved	R	Value = 0 Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.

4.3 SDRAM Configuration Register (SDCFG)

The SDRAM Configuration Register (SDCFG) contains field that program the DDR3 memory controller to meet the specifications of the DDR3 memory. These fields configure the DDR3 memory controller to match the data bus width, CAS latency, number of internal banks, and page size of the external DDR3 memory. For more information on initializing the configuration registers of the DDR3 memory controller, see Section 3.2.

Figure 4-3. SDRAM Configuration Register (SDCFG)

31 29	28	27 25	24	23 22	21 17	16 14
SDRAM_TYPE	Reserved	DDR_TERM	Reserved	DYN_ODT	Reserved	CWL
RW=0x0	R=0x0	RW=0x0	R=0x0	RW=0x0	R=0x0	RW=0x0

13 12	11 8	7	6 5	4	3	2	1 0
NM	CL	Reserved	IBANK	Reserved	EBANK	Reserved	PAGESIZE
RW=0x0	RW=0x2	R=0x0	RW=0x0	R=0x0	RW=0x0	R=0x0	RW=0x0

Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-5. SDRAM Configuration Register (SDCFG) Field Descriptions

Bit	Field	Attribute	Description
31-29	SDRAM_TYPE	RW	Value = 3 SDRAM type selection. Set to 3 for DDR3. All other values reserved.
28	Reserved	R	Value = 0 Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.
27-25	DDR_TERM	RW	Defines termination resistor value. • 0 = Disables termination • 1 = RZQ/4 • 2 = RZQ/2 • 3 = RZQ/6 • 4 = RZQ/12 • 5 = RZQ/8
24	Reserved	R	Value = 0 Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.
23-22	DYN_ODT	RW	Dynamic On-Die Termination • 0 = Turn off dynamic ODT. • 1 = RZQ/4 • 2 = RZQ/2 All other values reserved.
21-17	Reserved	R	Value = 0 Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.
16-14	CWL	RW	CAS Write Latency. Lower value gives better performance. • 0 = CAS write latency of 5 • 1 = CAS write latency of 6 • 2 = CAS write latency of 7 • 3 = CAS write latency of 8 • 4 = CAS write latency of 9 • 5 = CAS write latency of 10 • 6 = CAS write latency of 11 • 7 = CAS write latency of 12

Table 4-5. SDRAM Configuration Register (SDCFG) Field Descriptions (continued)

Bit	Field	Attribute	Description
13-12	NM	RW	DDR3 data bus width. A write to this bit field will cause the memory controller to start SDRAM initialization sequence. • 0 = 64-bit bus width. • 1 = 32-bit bus width. • 2 = 16-bit bus width. All other values reserved.
11-8	CL	RW	CAS Latency. The value of this field defines the CAS latency, to be used when accessing connected SDRAM devices. A write to this field will cause the DDR3 memory controller to start the SDRAM initialization sequence. • 2 = CAS latency of 5. • 4 = CAS latency of 6. • 6 = CAS latency of 7. • 8 = CAS latency of 8. • 10 = CAS latency of 9. • 12 = CAS latency of 10. • 14 = CAS latency of 11. • 1 = CAS latency of 12. • 3 = CAS latency of 13. • 5 = CAS latency of 14. • 7 = CAS latency of 15. • 9 = CAS latency of 16. All other values are reserved.
7	Reserved	R	Value = 0 Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.
6- 5	IBANK	RW	Internal SDRAM bank setup bits. Defines number of banks inside connected SDRAM devices. A write to this bit will cause the DDR3 memory controller to start SDRAM initialization sequence. Values 4-7 are reserved for this field. A word is equal to the bus width of the individual SDRAM devices used (example, 1 byte for x8 and 2bytes for x16 devices) • 0 = One bank SDRAM devices. • 1 = Two bank SDRAM devices. • 2 = Four bank SDRAM devices. • 3 = Eight bank SDRAM devices.
4	Reserved	R	Value = 0 Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.
3	EBANK	RW	External chip select setup. Defines whether SDRAM accesses use 1 or 2 chip select lines as follows: • 0 = Use DCE0# for all SDRAM accesses. • 1 = Use DEC0# and DCE1# for SDRAM accesses.
2	Reserved	R	Value = 0 Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.
1-0	PAGESIZE	RW	Page size bits. Defines internal page size of the external DDR3 memory. A write to this bit will cause the DDR3 memory controller to start the SDRAM initialization sequence. Values 4-7 are reserved for this field. A word is equal to the bus width of the individual SDRAM devices used (example, 1 byte for x8 and 2bytes for x16 devices) • 0 = 256-word page requiring 8 column address bits. • 1 = 512-word page requiring 9 column address bits. • 2 = 1024-word page requiring 10 column address bits. • 3 = 2048-word page requiring 11 column address bits.

4.4 SDRAM Refresh Control Register (SDRFC)

The SDRAM Refresh Control Register (SDRFC) is used to configure the DDR3 memory controller to:

- Enter and Exit the self-refresh state.
- Meet the refresh requirements of the attached DDR3 device by programming a rate at which the DDR3 memory controller issues autorefresh commands.

The SDRFC register is described in the following figure and table.

Figure 4-4. SDRAM Refresh Control Register (SDRFC)

31	30 16	15 0
INITREF_DIS	Reserved	REFRESH_RATE
RW=0x1	R=0x0	RW=0x0

Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-6. SDRAM Refresh Control (SDRFC) Register Field Descriptions

Bit	Field	Attribute	Description
31	INITREF_DIS	RW	Initialization and Refresh Disable. • 0 = Normal operation • 1 = Disables SDRAM initialization and refreshes, but carries out SDRAM write/read transactions
30-16	Reserved	R	Reserved.
15-0	REFRESH_RATE	RW	The value in this field is used to define the rate at which connected SDRAM devices will be refreshed. REFRESH_RATE = Refresh period * DDR3 clock frequency.

4.5 SDRAM Timing 1 (SDTIM1) Register

SDRAM Timing 1 register (SDTIM1) configures the DDR3 memory controller to meet many of the AC timing specifications of the DDR3 memory. Note that DDR3CLKOUT is equal to the period of the DDR3CLKOUT signal. See the DDR3 memory datasheet for information on appropriate values to program each field. The SDTIM1 register is described in the following figure and table.

Figure 4-5. SDRAM Timing 1 (SDTIM1) Register

31 30	29 25	24 18	17 10	9 4	3 0
Reserved	T_WR	T_RAS	T_RC	T_RRD	T_WTR
R=0x0	RW=0x1F	RW=0x7F	RW=0xFF	RW=0x3F	RW=0xF

Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-7. SDRAM Timing 1 (SDTIM1) Register Field Descriptions

Bit	Field	Attribute	Description
31- 30	Reserved	R	Value = 0 Reserved. The reserved bit location is always read as 0. A value written to this field has no effect
29-25	T_WR	RW	These bits specify the minimum number of DDR3CLKOUT cycles from the last write transfer to a precharge command, minus 1. The value of this parameter can be derived from the t_{WR} AC timing parameter in the DDR3 memory data sheet. Calculate using the formula: $T\_WR = (t_{WR}/t_{CK}) - 1$
24-18	T_RAS	RW	These bits specify the minimum number of DDR3CLKOUT cycles from an activate command to precharge command, minus 1. The value of this parameter can be derived from the minimum value of the t_{RAS} AC timing parameter in the DDR3 memory data sheet. Calculate using the formula: $T\_RAS = (t_{RAS}/t_{CK}) - 1$
17-10	T_RC	RW	These bits specify the minimum number of DDR3CLKOUT cycles from an activate command to an activate command, minus 1. The value of this parameter can be derived from the t_{RC}AC timing parameter in the DDR3 memory data sheet. Calculate using the formula: $T\_RC = (t_{RC}/t_{CK}) - 1$
9-4	T_RRD	RW	These bits specify the minimum number of DDR3CLKOUT cycles from an activate to an activate in a different bank, minus 1. The value of this parameter can be derived from the t_{FAW} AC timing parameter in the DDR3 memory data sheet. Calculate using the formula: $T\_RRD = (t_{FAW}/(4*t_{CK})) - 1$
3 -0	T_WTR	RW	These bits specify the minimum number of DDR3CLKOUT cycles from the last write to a read command, minus 1. The value of this parameter can be derived from the t_{WTR} AC timing parameter in the DDR3 memory data sheet. Convert the t_{WTR} value from the memory datasheet into ns before using the formula below. Calculate using the formula: $T\_WTR = (t_{WTR}/t_{CK}) - 1$

4.6 SDRAM Timing 2 (SDTIM2) Register

Like the SDRAM Timing 1 register (SDTIM1), the SDRAM Timing 2 register (SDTIM2) also configures the DDR3 memory controller to meet many of the AC timing specifications of the DDR3 memory. See the DDR3 memory datasheet for information on appropriate values to program each field. The SDTIM2 register is described in the following figure and table.

Figure 4-6. SDRAM Timing 2 (SDTIM2) Register

31 13	12 10	9 5	4 0
Reserved	T_RTW	T_RP	T_RCD
R=0x0	RW=0x7	RW=0x1F	RW=0x1F

Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

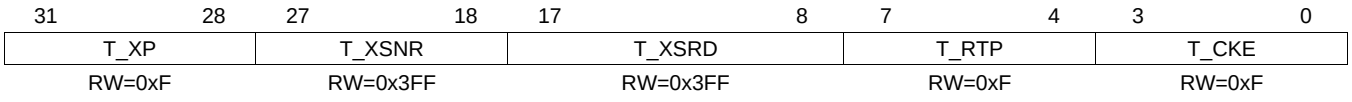
Table 4-8. SDRAM Timing 2 (SDTIM2) Register Field Descriptions

Bit	Field	Attribute	Description
31-13	Reserved	R	Value = 0 Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.
12-10	T_RTW	RW	Minimum number of DDR3CLKOUT cycles between read and write date phases, minus 1. This is not an SDRAM timing parameter. The value depends on the board topology supported. For single rank: reg_t_RTW= (((2*dqs_delay_for_cs0)+tDQSCK+ wr_leveling_tolerance)/clock_period)-1 For dual rank: reg_t_RTW= ((dqs_delay_for_cs0+dqs_delay_for_cs1+ absolute(command_delay_for_cs0-command_delay_for_cs1)+tDQSCK+ wr_leveling_tolerance)/clock_period)-1
9-5	T_RP	RW	These bits specify the minimum number of DDR3CLKOUT cycles from a precharge command to a refresh or activate command, minus 1. The value of this parameter can be derived from the t_{RP} AC timing parameter in the DDR3 memory data sheet. Calculate using the formula: T_RP = (t_{RP}/t_{CK}) – 1
4-0	T_RCD	RW	These bits specify the minimum number of DDR3CLKOUT cycles from an activate command to a read or write command, minus 1. The value of this parameter can be derived from the t_{RCD} AC timing parameter in the DDR3 memory data sheet. Calculate using the formula: T_RCD = (t_{RCD}/t_{CK}) – 1

4.7 SDRAM Timing 3 (SDTIM3) Register

Like the SDRAM Timing 1 and 2 registers (SDTIM1 & SDTIM2), the SDRAM Timing 3 register (SDTIM3) also configures the DDR3 memory controller to meet many of the AC timing specifications of the DDR3 memory. See the DDR3 memory datasheet for information on appropriate values to program each field. The SDTIM3 register is described in the following figure and table.

Figure 4-7. SDRAM Timing 3 (SDTIM3) Register



Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-9. SDRAM Timing 3 (SDTIM3) Register Field Descriptions

Bit	Field	Attribute	Description
31-28	T_XP	RW	These bits specify the minimum number of DDR3CLKOUT cycles from Power down exit to any command other than a read command, minus 1. The value of this parameter can be derived from the t_{XP} AC timing parameter in the DDR3 memory data sheet. Convert the t_{XP} datasheet parameter value into ns before using formula below. Calculate using the formula: $T\_XP = (t_{XP}/t_{CK}) - 1$
27-18	T_XSNR	RW	These bits specify the minimum number of DDR3CLKOUT cycles from a self-refresh exit to a command that does not require a locked DLL, minus 1. The value of this parameter can be derived from the t_{XS} AC timing parameter in the DDR3 memory data sheet. Calculate using the formula: $T\_XSNR = (t_{XS}/t_{CK}) - 1$
17-8	T_XSRD	RW	These bits specify the minimum number of DDR3CLKOUT cycles from a self-refresh exit to a command that requires a locked DLL, minus 1. The value of this parameter can be derived from the t_{XSDLL} AC timing parameter in the DDR3 memory data sheet. This parameter typically appears in the datasheet in terms of t_{CK} clock cycles. Calculate using the formula: $T\_XSRD = t_{XSDLL} - 1$
7-4	T_RTP	RW	These bits specify the minimum number of DDR3CLKOUT cycles from the last read to precharge command, minus 1. The value of this parameter can be derived from the t_{RTP} AC timing parameter in the DDR3 memory data sheet. Convert the t_{XP} datasheet parameter value into ns before using formula below. Calculate using the formula: $T\_RTP = (t_{RTP}/t_{CK}) - 1$
3-0	T_CKE	RW	These bits specify the minimum number of DDR3CLKOUT cycles between transitions on the DSDCKE pin, minus 1. The value of this parameter can be derived from the t_{CKE} AC timing parameter in the DDR3 memory data sheet. Calculate using the formula: $T\_CKE = (t_{CKE}/t_{CK}) - 1$

4.8 SDRAM Timing 4 (SDTIM4) Register

Like the SDRAM Timing 1, 2 and 3 registers, the SDRAM Timing 4 register (SDTIM4) also configures the DDR3 memory controller to meet many of the AC timing specifications of the DDR3 memory. See the DDR3 memory datasheet for information on appropriate values to program each field. The SDTIM4 register is described in the following figure and table.

Figure 4-8. SDRAM Timing 4 (SDTIM4) Register

31–28	27–24	23–16	15–14	13–4	3–0
T_CSTA	T_CKESR	ZQ_ZQCS	Reserved	T_RFC	T_RAS_MAX
RW=0xF	RW=0xF	RW=0xFF	R=0x0	RW=0x3FF	RW=0xF

Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-10. SDRAM Timing 4 (SDTIM4) Register Field Descriptions

Bit	Field	Attribute	Description
31-28	T_CSTA	RW	Minimum DDR3CLKOUT cycles between write-to-write or read-to-read data phases to different chip selects, minus 1.
27-24	T_CKESR	RW	Value = 0 Minimum DDR3CLKOUT cycles for which DDR3 should remain in self-refresh. This parameter typically appears as number of t_{CK} clock cycles. T_CKESR = (t_{CKESR}/t_{CK}) – 1
23-16	ZQ_ZQCS	RW	These bits specify the minimum number of DDR3CLKOUT cycles for a ZQCS command, minus 1. The value of this parameter can be derived from the t_{ZQCS} AC timing parameter in the DDR3 memory data sheet. This parameter typically appears as number of t_{CK} clock cycles. Calculate using the formula : ZQ_ZQCS = t_{ZQCS} – 1
15-14	Reserved	R	Value = 0 Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.
13-4	T_RFC	RW	These bits specify the minimum number of DDR3CLKOUT cycles from a refresh or load mode command to a refresh or activate command, minus 1. The value of this parameter can be derived from the t_{RFC} AC timing parameter in the DDR3 memory data sheet. Calculate using the formula: T_RFC = (t_{RFC}/t_{CK}) – 1
3-0	T_RAS_MAX	RW	This field must always be programmed to 0xF.

4.9 Power Management Control Register (PMCTL)

The PMCTL register is described in the following figure and table.

Figure 4-9. Power Management Control Register (PMCTL)

31 16	15 12	11	10 8	7 4	3 0
Reserved	PD_TIM	Reserved	LP_MODE	SR_TIM	Reserved
R=0x0	RW=0x0	R=0x0	RW=0x0	RW=0x0	R=0x0

Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-11. Power Management Control Register (PMCTL) Field Descriptions

Bit	Field	Attribute	Description
31-16	Reserved	R	Value = 0 Reserved. The reserved bit location is always read as 0. A value written to this field has no effect
15-12	PD_TIM	RW	Power Management timer for power-down. The DDR3 memory controller will put the SDRAM in power-down mode after the DDR3 controller is idle for PD_TIM number of DDR3CLKOUT cycles and if LP_MODE is set to 4. • 0 = Immediately enter power-down • 1 = Enter power-down after 16 clocks • 2 = Enter power-down after 32 clocks • 3 = Enter power-down after 64 clocks • 4 = Enter power-down after 128 clocks • 5 = Enter power-down after 256 clocks • 6 = Enter power-down after 512 clocks • 7 = Enter power-down after 1024 clocks • 8 = Enter power-down after 2048 clocks • 9 = Enter power-down after 4096 clocks • 10 = Enter power-down after 8912 clocks • 11 = Enter power-down after 16384 clocks • 12 = Enter power-down after 32768 clocks • 13 = Enter power-down after 65536 clocks • 14 = Enter power-down after 131072 clocks • 15 = Enter power-down after 262144 clocks
11	Reserved	R	Value = 0 Reserved. The reserved bit location is always read as 0. A value written to this field has no effect
10-8	LP_MODE	RW	Automatic power management enable. • 2 = Self-refresh mode • 4 = Power-down mode All other values will disable automatic power management.

Table 4-11. Power Management Control Register (PMCTL) Field Descriptions (continued)

Bit	Field	Attribute	Description
7-4	SR_TIM	RW	Power management timer for self-refresh. The DDR3 memory controller will put the external SDRAM in self-refresh mode after DDR3 controller has been idle for these number of DDR3CLKOUT cycles and LP_MODE is set to 2. • 0 = Immediately enter self-refresh • 1 = Enter self-refresh after 16 clocks • 2 = Enter self-refresh after 32 clocks • 3 = Enter self-refresh after 64 clocks • 4 = Enter self-refresh after 128 clocks • 5 = Enter self-refresh after 256 clocks • 6 = Enter self-refresh after 512 clocks • 7 = Enter self-refresh after 1024 clocks • 8 = Enter self-refresh after 2048 clocks • 9 = Enter self-refresh after 4096 clocks • 10 = Enter self-refresh after 8912 clocks • 11 = Enter self-refresh after 16384 clocks • 12 = Enter self-refresh after 32768 clocks • 13 = Enter self-refresh after 65536 clocks • 14 = Enter self-refresh after 131072 clocks • 15 = Enter self-refresh after 262144 clocks
3-0	Reserved	R	Reserved

4.10 VBUSM Configuration Register (VBUSM_CONFIG)

The VBUSM_CONFIG register is described in the following figure and table.

Figure 4-10. VBUSM Configuration Register (VBUSM_CONFIG)

31 24	23 16	15 8	7 0
Reserved	COS_COUNT_1	COS_COUNT_2	PR_OLD_COUNT
R=0x0	RW=0xFF	RW=0xFF	RW=0xFF

Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

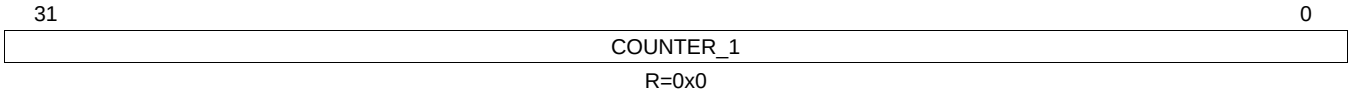
Table 4-12. VBUSM Configuration Register (VBUSM_CONFIG) Field Descriptions

Bit	Field	Attribute	Description
31-24	Reserved	R	Value = 0 Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.
23-16	COS_COUNT_1	RW	Value = 0xFF Priority raise counter for Class of Service 1. Number of DDR3CLKOUT cycles after which the DDR3 controller momentarily raises the priority of Class of Service 1 commands in Command FIFO. Number of clock cycles = COS_COUNT_1 x 16 clocks
15-8	COS_COUNT_2	RW	Value = 0xFF Priority raise counter for Class of Service 2. Number of DDR3CLKOUT cycles after which the DDR3 controller momentarily raises the priority of Class of Service 2 commands in Command FIFO. Number of clock cycles = COS_COUNT_2 x 16 clocks
7-0	PR_OLD_COUNT	RW	Value = 0xFF Priority raise old counter. Number of DDR3CLKOUT cycles after which DDR3 controller momentarily raises the priority of the oldest command in Command FIFO. Number of clock cycles = PR_OLD_COUNT_2 x 16 clocks

4.11 Performance Counter 1 Register (PERF_CNT_1)

The PERF_CNT_1 register is described in the following figure and table.

Figure 4-11. Performance Counter 1 Register (PERF_CNT_1)



Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

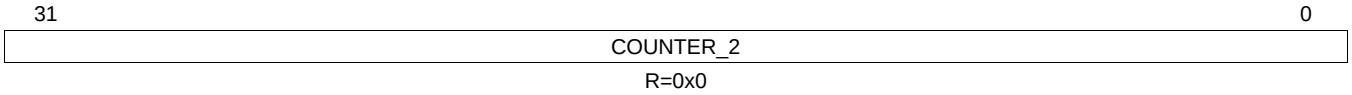
Table 4-13. Performance Counter 1 Register (PERF_CNT_1) Field Descriptions

Bit	Field	Attribute	Description
31-0	COUNTER_1	R	32-bit counter can be programmed as specified in the Performance Counter Config and Performance Counter Master Region Select registers.

4.12 Performance Counter 2 Register (PERF_CNT_2)

The PERF_CNT_2 register is described in the following figure and table.

Figure 4-12. Performance Counter 2 Register (PERF_CNT_2)



Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-14. Performance Counter 2 Register (PERF_CNT_2) Field Descriptions

Bit	Field	Attribute	Description
31-0	COUNTER_2	R	32-bit counter can be programmed as specified in the Performance Counter Config and Performance Counter Master Region Select registers.

4.13 Performance Counter Config Register (PERF_CNT_CFG)

The PERF_CNT_CFG register is described in the following figure and table.

Figure 4-13. Performance Counter Config Register (PERF_CNT_CFG)

31	30	29 20	19 16
CNTR2_MSTID_EN	CNTR2_REGION_EN	Reserved	CNTR2_CFG
RW=0x0	RW=0x0	R=0x0	RW=0x1
15	14	13 4	3 0
CNTR1_MSTID_EN	CNTR1_REGION_EN	Reserved	CNTR1_CFG
RW=0x0	RW=0x0	R=0x0	RW=0x0

Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-15. Performance Counter Config Register (PERF_CNT_CFG) Field Descriptions

Bit	Field	Attribute	Description
31	CNTR2_MSTID_EN	RW	Master ID filter enable for Performance Counter 2 Register. Set to 1 to enable filtering of events for counter 2 by Master ID. Refer to your device data manual for the master IDs of various masters.
30	CNTR2_REGION_EN	RW	Memory space region enable for Performance Counter 2 Register. Set to 1 to enable filtering of events for counter 2 by the accessed memory region.
29-20	Reserved	R	Value = 0x0 Reserved
19-16	CNTR2_CFG	RW	Filter configuration selected for Performance Counter 2. This field selects the type of event to count for Counter 2. Refer to Table 2-12 for various configuration options.
15	CNTR1_MSTID_EN	RW	Master ID filter enable for Performance Counter 1 Register. Set to 1 to enable filtering of events for counter 1 by Master ID. Refer to your device data manual for the master IDs of various masters.
14	CNTR1_REGION_EN	RW	Memory space region enable for Performance Counter 1 Register. Set to 1 to enable filtering of events for counter 1 by the accessed memory region.
13-4	Reserved	R	Value = 0x0 Reserved
3-0	CNTR1_CFG	RW	Filter configuration selected for Performance Counter 1. This field selects the type of event to count for Counter 1. Refer to Table 2-12 for various configuration options.

4.14 Performance Counter Master Region Select Register (PERF_CNT_SEL)

For events that can be configured to enable master ID and/or memory region filters, the value of the master ID and the region select options for the counters are programmed in the PERF_CNT_SEL register. The PERF_CNT_SEL register is described in the following figure and table.

Figure 4-14. Performance Counter Master Region Select Register (PERF_CNT_SEL)

31 24	23 20	19 16	15 8	7 4	3 0
MSTID2	Reserved	REGION_SEL2	MSTID1	Reserved	REGION_SEL1
RW=0x0	R=0x0	RW=0x0	RW=0x0	R=0x0	RW=0x0

Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

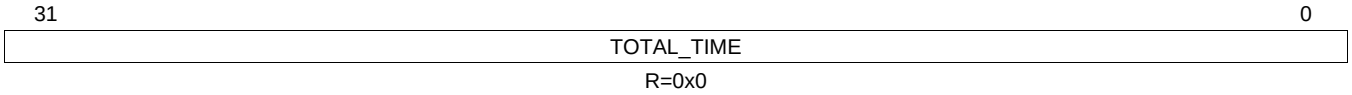
Table 4-16. Performance Counter Master Region Select Register (PERF_CNT_SEL) Field Descriptions

Bit	Field	Attribute	Description
31-24	MSTID2	RW	Master ID for Performance Counter 2 Register. Refer to your device data manual for the master IDs of various masters.
23-20	Reserved	R	Value = 0x0 Reserved
19-16	REGION_SEL2	RW	Region select for Performance Counter 2. • 0x0 - DDR3 memory space • 0x7 - DDR3 controller memory mapped registers All other values are reserved.
15-8	MSTID1	RW	Master ID for Performance Counter 1 Register. Refer to your device data manual for the master IDs of various masters.
7-4	Reserved	R	Value = 0x0 Reserved
3-0	REGION_SEL1	RW	Region select for Performance Counter 1. • 0x0 - DDR3 memory space • 0x7 - DDR3 controller memory mapped registers All other values are reserved.

4.15 Performance Counter Time Register (PERF_CNT_TIM)

The PERF_CNT_TIM register is described in the following figure and table.

Figure 4-15. Performance Counter Time Register (PERF_CNT_TIM)



Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-17. Performance Counter Time Register (PERF_CNT_TIM) Field Descriptions

Bit	Field	Attribute	Description
31-0	TOTAL_TIME	R	32-bit counter continuously counts number of DDR/2 clock cycles elapsed after the controller is brought out of reset.

4.16 Interrupt Raw Status Register (IRQSTATUS_RAW_SYS)

The IRQSTATUS_RAW_SYS register is described in the following figure and table.

Figure 4-16. Interrupt Raw Status Register (IRQSTATUS_RAW_SYS)

31 6	5	4	3	2 1	0
Reserved	1B_ECC_ERR_SYS	2B_ECC_ERR_SYS	WR_ECC_ERR_SYS	Reserved	ERR_SYS
R=0x0	WOS=0x0	WOS=0x0	WOS=0x0	R=0x0	WOS=0x0

Legend: R = Read only; WOS = Write one to set ;- *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-18. Interrupt Raw Status Register (IRQSTATUS_RAW_SYS) Field Descriptions

Bit	Field	Attribute	Description
31- 6	Reserved	R	Value = 0x0 Reserved
5	1B_ECC_ERR_SYS	WOS	Value = 0x0 Raw status of 1-bit ECC error interrupt. Writing a 1 sets the raw status. Writing a 0 has no effect.
4	2B_ECC_ERR_SYS	WOS	Value = 0x0 Raw status of 2-bit ECC error interrupt. Writing a 1 sets the raw status. Writing a 0 has no effect.
3	WR_ECC_ERR_SYS	WOS	Value = 0x0 Raw status of write ECC error interrupt. Writing a 1 sets the raw status. Writing a 0 has no effect.
2-1	Reserved	R	Value = 0x0 Reserved
0	ERR_SYS	WOS	Value = 0x0 Raw status of system VBUSM interrupt for command or address error. Writing a 1 sets the raw status. Writing a 0 has no effect.

4.17 Interrupt Status Register (IRQSTATUS_ SYS)

The IRQSTATUS_SYS register is described in the following figure and table.

Figure 4-17. Interrupt Status Register (IRQSTATUS_ SYS)

31 6	5	4	3	2 1	0
Reserved	1B_ECC_ERR_SYS	2B_ECC_ERR_SYS	WR_ECC_ERR_SYS	Reserved	ERR_SYS
R	WOC	WOC	WOC	R	WOC

Legend: R = Read only; WOC = write one to clear; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-19. Interrupt Status Register (IRQSTATUS_SYS) Field Descriptions

Bit	Field	Attribute	Description
31- 6	Reserved	R	Value = 0x0 Reserved.
5	1B_ECC_ERR_SYS	WOC	Value = 0x0 Enabled status of 1-bit ECC error interrupt. Writing a 1 clears the status as well the raw status. Writing a 0 has no effect.
4	2B_ECC_ERR_SYS	WOC	Value = 0x0 Enabled status of 2-bit ECC error interrupt. Writing a 1 clears the status as well the raw status. Writing a 0 has no effect.
3	WR_ECC_ERR_SYS	WOC	Value = 0x0 Enabled status of write ECC error interrupt. Writing a 1 clears the status as well the raw status. Writing a 0 has no effect.
2-1	Reserved	R	Value = 0x0 Reserved.
0	ERR_SYS	WOC	Value = 0x0 Enabled status of system VBUSM interrupt for command or address error. Writing a 1 clears the status as well the raw status. Writing a 0 has no effect.

4.18 Interrupt Enable Set Register (IRQSTATUS_ SET_SYS)

The IRQSTATUS_SET_SYS register is described in the following figure and table.

Figure 4-18. Interrupt Enable Set Register (IRQSTATUS_ SET_SYS)

31 6	5	4	3	2 1	0
Reserved	1B_ECC_ERR_SYS	2B_ECC_ERR_SYS	WR_ECC_ERR_SYS	Reserved	ERR_SYS
R=0x0	WOS=0x0	WOS=0x0	WOS=0x0	R=0x0	WOS=0x0

Legend: R = Read only; WOS = Write one to set; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-20. Interrupt Enable Set Register (IRQSTATUS_ SET_SYS) Field Descriptions

Bit	Field	Attribute	Description
31- 6	Reserved	R	Value = 0x0 Reserved.
5	1B_ECC_ERR_SYS	WOS	Value = 0x0 Enabled set for 1-bit ECC error interrupt. Writing a 1 will enable the read ECC error interrupt, set this bit as well as the bit in Interrupt Enable Clear Register. Writing a 0 has no effect.
4	2B_ECC_ERR_SYS	WOS	Value = 0x0 Enabled set for 2-bit ECC error interrupt. Writing a 1 will enable the read ECC error interrupt, set this bit as well as the bit in Interrupt Enable Clear Register. Writing a 0 has no effect.
3	WR_ECC_ERR_SYS	WOS	Value = 0x0 Enabled set for write ECC error interrupt. Writing a 1 will enable the write ECC error interrupt, set this bit as well as the bit in Interrupt Enable Clear Register. Writing a 0 has no effect.
2-1	Reserved	R	Value = 0x0 Reserved.
0	ERR_SYS	WOS	Value = 0x0 Enable set for system VBUSM interrupt for command or address error. Writing a 1 will enable the interrupt, and set this bit as well as the corresponding Interrupt Enable Clear Register. Writing a 0 has no effect.

4.19 Interrupt Enable Clear Register (IRQSTATUS_ CLR_SYS)

The IRQSTATUS_CLR_SYS register is described in the following figure and table.

Figure 4-19. Interrupt Enable Clear Register (IRQSTATUS_ CLR_SYS)

31 6	5	4	3	2 1	0
Reserved	1B_ECC_ERR_SYS	2B_ECC_ERR_SYS	WR_ECC_ERR_SYS	Reserved	ERR_SYS
R	WOC=0x0	WOC=0x0	WOC=0x0	R	WOC=0x0

Legend: R = Read only; WOC = Write one to clear; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-21. Interrupt Enable Clear Register (IRQSTATUS_ CLR_SYS) Field Descriptions

Bit	Field	Attribute	Description
31- 6	Reserved	R	Value = 0x0 Reserved.
5	1B_ECC_ERR_SYS	WOC	Value = 0x0 Enabled clear for 1-bit ECC error interrupt. Writing a 1 will disable the read ECC error interrupt, clear this bit as well as the bit in Interrupt Enable Clear Register. Writing a 0 has no effect.
4	2B_ECC_ERR_SYS	WOC	Value = 0x0 Enabled clear for 2-bit ECC error interrupt. Writing a 1 will disable the read ECC error interrupt, clear this bit as well as the bit in Interrupt Enable Clear Register. Writing a 0 has no effect.
3	WR_ECC_ERR_SYS	WOC	Value = 0x0 Enabled clear for write ECC error interrupt. Writing a 1 will disable the write ECC error interrupt, clear this bit as well as the bit in Interrupt Enable Clear Register. Writing a 0 has no effect.
2-1	Reserved	R	Value = 0x0 Reserved.
0	ERR_SYS	WOC	Value = 0x0 Enable clear for system VBUSM interrupt for command or address error. Writing a 1 will disable the interrupt, and clear this bit as well as the corresponding Interrupt Enable Set Register. Writing a 0 has no effect.

4.20 SDRAM Output Impedance Calibration Configuration Register (ZQCFG)

The ZQCFG register is described in the following figure and table.

Figure 4-20. SDRAM Output Impedance Calibration Configuration Register (ZQCFG)

31	30	29	28
ZQ_CS1EN	ZQ_CS0EN	ZQ_DUALCALEN	ZQ_SFEXITEN
RW=0x0	RW=0x0	RW=0x0	RW=0x0

27 19	18 16	15 0
Reserved	ZQ_ZQCL_MULT	ZQ_REFINTERVAL
R=0x0	RW=0x0	RW=0x0

Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-22. SDRAM Output Impedance Calibration Configuration Register (ZQCFG) Field Descriptions

Bit	Field	Attribute	Description
31	ZQ_CS1EN	RW	ZQ calibration for CS1 • 0 = Disable ZQ calibration for CS1 • 1 = Enable ZQ calibration for CS1
30	ZQ_CS0EN	RW	ZQ calibration for CS0 • 0 = Disable ZQ calibration for CS0 • 1 = Enable ZQ calibration for CS0
29	ZQ_DUALCALEN	RW	ZQ Dual Calibration enable. Allows both ranks to be calibrated simultaneously. • 0 = Dual ZQ calibration disable • 1 = Both chip selects have a separate calibration resistor per device. .
28	ZQ_SFEXITEN	RW	ZQCL on Self-refresh, Active power-down and precharge power-down exit enable. • 0 = Disable ZQCL on Self-refresh, Active power-down and precharge power-down exit enable • 1 = Enable ZQCL on Self-refresh, Active power-down and precharge power-down exit enable. Set this value to 1 to issue a ZQCL command upon self-refresh exit.
27- 19	Reserved	R	Value = 0 Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.
18-16	ZQ_ZQCL_MULT	RW	Number of ZQCS intervals that make up a ZQCL interval, minus one. ZQCS interval is defined by ZQ_ZQCS field in SDRAM Timing 3 (SDTIM3) register. The value of this parameter can be derived using the formula: T_ZQ_ZQCL_MULT = ($t_{ZQoper}/t_{ZQCS} - 1$)
15-0	ZQ_REFINTERVAL	RW	Number of refresh periods between ZQCS commands, minus one. This field supports between one refresh period to 256 ms between ZQCS calibration commands. Refresh period is defined by REFRESH_RATE field in SDRAM Refresh control (SDRFC) register. ZQ_REFINTERVAL = number of refresh periods between ZQCS commands. The interval is calculated as = 0.5% / [(Tsens x Tdriftrate) + (Vsens x Vdriftrate)]. Tsens = max (dRTTdT, dRONdTM) from the memory device datasheet. Vsens = max(dRTTdV, dRONdVM) from the memory device datasheet Tdriftrate = drift rate in ° C/second. This is the temperature drift rate that the SDRAM is subject to in the application. Vdriftrate = drift rate in mV/second. This is the voltage drift rate that the SDRAM is subject to in the application. Example: If Tsens= 1.5%/ ° C, Vsens = 0.15%/mV, Tdriftrate = 1.2 ° C/second and Vdriftrate = 10mV/second, Interval = 0.5/[(1.5 x 1.2) + (0.15 x 10)] = 152ms. Since refresh interval = 7.8µs, ZQ_REFINTERVAL = 152ms/7.8µs = 0x4C1F

4.21 Priority to Class-Of-Service Mapping Register (PRI_COS_MAP)

The PRI_COS_MAP register is described in the following figure and table.

Figure 4-21. Priority to Class-Of-Service Mapping Register (PRI_COS_MAP)

31	30 16	15 14	13 12	11 10
PRI_COS_MAP_EN	Reserved	PRI_7_COS	PRI_6_COS	PRI_5_COS
RW=0x0	R=0x0	RW=0x0	RW=0x0	RW=0x0

9 8	7 6	5 4	3 2	1 0
PRI_4_COS	PRI_3_COS	PRI_2_COS	PRI_1_COS	PRI_0_COS
RW=0x0	RW=0x0	RW=0x0	RW=0x0	RW=0x0

Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-23. Priority to Class-Of-Service Mapping Register (PRICOSMAP) Field Descriptions

Bit	Field	Description
31	PRI_COS_MAP_EN	Value = 0x0 Priority to Class-of-service mapping • 0 = Disable Priority to Class-of-service mapping • 1 = Enable Priority to Class-of-service mapping
30-16	Reserved	Value = 0 Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.
15-14	PRI_7_COS	Class-of-service for commands with priority of 7 (lowest priority). • 1= Map to Class-of-service 1 • 2= Map to Class-of-service 2 • 0 or 3 will not assign any class of service.
13-12	PRI_6_COS	Class-of-service for commands with priority of 6. • 1= Map to Class-of-service 1 • 2= Map to Class-of-service 2 • 0 or 3 will not assign any class of service.
11-10	PRI_5_COS	Class-of-service for commands with priority of 5. • 1= Map to Class-of-service 1 • 2= Map to Class-of-service 2 • 0 or 3 will not assign any class of service.
9-8	PRI_4_COS	Class-of-service for commands with priority of 4. • 1= Map to Class-of-service 1 • 2= Map to Class-of-service 2 • 0 or 3 will not assign any class of service.
7-6	PRI_3_COS	Class-of-service for commands with priority of 3. • 1= Map to Class-of-service 1 • 2= Map to Class-of-service 2 • 0 or 3 will not assign any class of service.
5-4	PRI_2_COS	Class-of-service for commands with priority of 2. • 1= Map to Class-of-service 1 • 2= Map to Class-of-service 2 • 0 or 3 will not assign any class of service.
3-2	PRI_1_COS	Class-of-service for commands with priority of 1. • 1= Map to Class-of-service 1 • 2= Map to Class-of-service 2 • 0 or 3 will not assign any class of service.
1-0	PRI_0_COS	Class-of-service for commands with priority of 0 (highest priority). • 1= Map to Class-of-service 1 • 2= Map to Class-of-service 2 • 0 or 3 will not assign any class of service.

4.22 Master ID to Class-Of-Service 1 Mapping Register (MSTID_COS_1_MAP)

The MSTID_COS_1_MAP register is described in the following figure and table.

Figure 4-22. Master ID to Class-Of-Service 1 Mapping Register (MSTID_COS_1_MAP)

31	30 23	22 20
MSTID_COS_1_MAP_EN	MSTID_1_COS_1	MSK_1_COS_1
RW=0x0	RW=0x0	RW=0x0

19 12	11 10	9 2	1 0
MSTID_2_COS_1	MSK_2_COS_1	MSTID_3_COS_1	MSK_3_COS_1
RW=0x0	RW=0x0	RW=0x0	RW=0x0

Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-24. Master ID to Class-Of-Service Mapping 1 Register (MSTID_COS_1_MAP) Field Descriptions

Bit	Field	Description
31	MSTID_COS_1_MAP_EN	Master ID to Class-of-service 1 mapping. • 0 = Disable Master ID to Class-of-service 1 mapping • 1 = Enable Master ID to Class-of-service 1 mapping
30-23	MSTID_1_COS_1	Value = 0x0 Master ID value 1 for Class-of-service 1.
22-20	MSK_1_COS_1	Mask for master ID value 1 for Class-of-service 1. • 0 = Disable masking • 1 = Mask master ID bit 0 • 2 = Mask master ID bits 1-0 • 3 = Mask master ID bits 2-0
19-12	MSTID_2_COS_1	Value = 0x0 Master ID value 2 for Class-of-service 1.
11-10	MSK_2_COS_1	Mask for master ID value 2 for Class-of-service 1. • 0 = Disable masking • 1 = Mask master ID bit 0 • 2 = Mask master ID bits 1-0 • 3 = Mask master ID bits 2-0
9-2	MSTID_3_COS_1	Value = 0x0 Master ID value 3 for Class-of-service 1.
1-0	MSK_3_COS_1	Mask for master ID value 3 for Class-of-service 1. • 0 = Disable masking • 1 = Mask master ID bit 0 • 2 = Mask master ID bits 1-0 • 3 = Mask master ID bits 2-0

4.23 Master ID to Class-Of-Service 2 Mapping Register (MSTID_COS_2_MAP)

The MSTID_COS_2_MAP register is described in the following figure and table.

Figure 4-23. Master ID to Class-Of-Service 2 Mapping Register (MSTID_COS_2_MAP)

31	30 23	22 20	19 12	11 10	9 2	1 0
MSTID_COS_2_MAP_EN	MSTID_1_COS_2	MSK_1_COS_2	MSTID_2_COS_2	MSK_2_COS_2	MSTID_3_COS_2	MSK_3_COS_2
RW=0x0	RW=0x0	RW=0x0	RW=0x0	RW=0x0	RW=0x0	RW=0x0

Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-25. Master ID to Class-Of-Service Mapping 2 Register (MSTID_COS_2_MAP) Field Descriptions

Bit	Field	Description
31	MSTID_COS_2_MAP_EN	Master ID to Class-of-service 2 mapping. • 0 = Disable Master ID to Class-of-service 2 mapping • 1 = Enable Master ID to Class-of-service 2 mapping
30-23	MSTID_1_COS_2	Value = 0x0 Master ID value 1 for Class-of-service 2.
22-20	MSK_1_COS_2	Mask for master ID value 1 for Class-of-service 2. • 0 = Disable masking • 1 = Mask master ID bit 0 • 2 = Mask master ID bits 1-0 • 3 = Mask master ID bits 2-0
19-12	MSTID_2_COS_2	Value = 0x0 Master ID value 2 for Class-of-service 2.
11-10	MSK_2_COS_2	Mask for master ID value 2 for Class-of-service 2. • 0 = Disable masking • 1 = Mask master ID bit 0 • 2 = Mask master ID bits 1-0 • 3 = Mask master ID bits 2-0
9-2	MSTID_3_COS_2	Value = 0x0 Master ID value 3 for Class-of-service 2.
1-0	MSK_3_COS_2	Mask for master ID value 3 for Class-of-service 2. • 0 - Disable masking • 1 = Mask master ID bit 0 • 2 = Mask master ID bits 1-0 • 3 = Mask master ID bits 2-0

4.24 ECC Control Register (ECCCTL)

The ECCCTL register is described in the following figure and table.

Figure 4-24. ECC Control Register (ECCCTL)

31	30	29	28
ECC_EN	ECC_ADDR_RNG_PROT	ECC_VERIFY_EN	RMW_EN
RW=0x0	RW=0x0	RW=0x0	RW=0x0

27	2	1	0
Reserved		ECC_ADDR_RNG_2_EN	ECC_ADDR_RNG_1_EN
R=0x0		RW=0x0	RW=0x0

Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

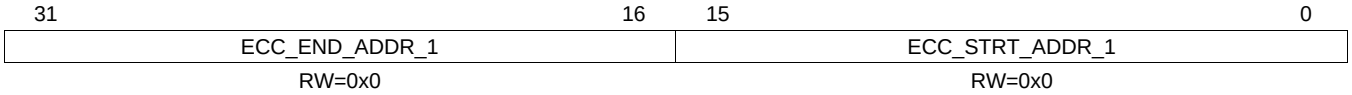
Table 4-26. ECC Control Register (ECCCTL) Field Descriptions

Bit	Field	Description
31	ECC_EN	ECC enable. Enabling ECC will cause the DDR3 controller to start the SDRAM initialization sequence. • 0 = Disable ECC • 1 = Enable ECC
30	ECC_ADDR_RNG_PROT	This bit is used to determine whether ECC calculation is allowed within address ranges described by ECC Address Range 1 and 2 Registers, provided ECC_EN is set to enable ECC. • 0 = Disable ECC calculation within address ranges defined in ECC Address Range 1 and 2 registers and enable calculation for accesses outside of these address ranges • 1 = Enable ECC calculation within address ranges defined in ECC Address Range 1 and 2 registers and disable calculation for accesses outside of these address ranges
29	ECC_VERIFY_EN	• 0 - Disable ECC verification for read accesses when ECC_EN=1. • 1- Enable ECC verification for read accesses when ECC_EN=1. This field is ignored if ECC_EN=0. Note that this field is available only on K2K and K2H silicon revisions above 1.1. It is available on all revisions of the K2E and K2L families.
28	RMW_EN	• 0 - Disable read-modify-write functionality for sub-quanta accesses when ECC_EN=1. • 1 - Enable read-modify-write functionality for sub-quanta accesses when ECC_EN=1. This field is ignored if ECC_EN=0. Note that this field is available only on K2K and K2H silicon revisions above 1.1. It is available on all revisions of the K2E and K2L families.
27-2	Reserved	Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.
1	ECC_ADDR_RNG_2_EN	ECC Address Range 2 enable. • 0 = Disable ECC Address Range 2 • 1 = Enable ECC Address Range 2
0	ECC_ADDR_RNG_1_EN	ECC Address Range 1 enable. • 0 = Disable ECC Address Range 1 • 1 = Enable ECC Address Range 1

4.25 ECC Address Range 1 Register (ECCADDR1)

The ECCADDR1 register is described in the following figure and table.

Figure 4-25. ECC Address Range 1 Register (ECCADDR1)



Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-27. ECC Address Range 1 Register Field Descriptions

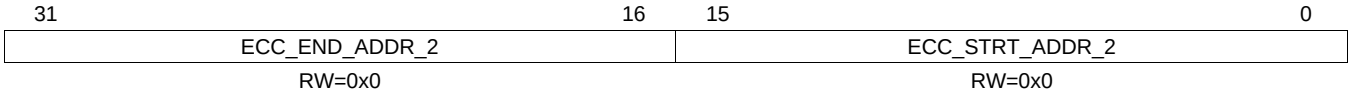
Bit	Field	Description
31-16	ECC_END_ADDR_1	End address [32-17] of 33-bit address for ECC address range 1
15-0	ECC_STRT_ADDR_1	Start address [32-17] of 33-bit address for ECC address range 1

NOTE: The range is inclusive of start and end addresses.

4.26 ECC Address Range 2 Register (ECCADDR2)

The ECCADDR2 register is described in the following figure and table.

Figure 4-26. ECC Address Range 2Register (ECCADDR2)



Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-28. ECC Address Range 2 Register Field Descriptions

Bit	Field	Description
31-16	ECC_END_ADDR_2	End address [32-17] of 33-bit address for ECC address range 2
15-0	ECC_STRT_ADDR_2	Start address [32-17] of 33-bit address for ECC address range 2

NOTE: The range is inclusive of start and end addresses.

4.27 Read Write Execution Threshold Register (RWTHRESH)

The RWTHRESH register is described in the following figure and table.

Figure 4-27. Read Write Execution Threshold Register (RWTHRESH)

31	13	12	8	7	5	4	0
Reserved		WR_THRSH		Reserved		RD_THRSH	
R=0x0		RW=0x3		R=0x0		RW=0x5	

Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

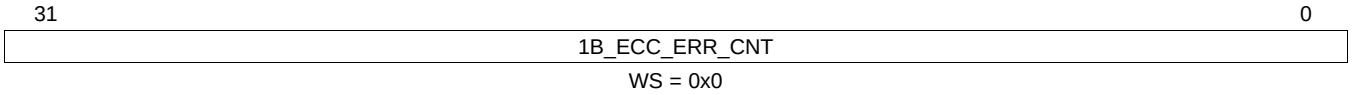
Table 4-29. Read Write Execution Threshold Register (RWTHRESH) Field Descriptions

Bit	Field	Description
31-13	Reserved	Value = 0x0 Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.
12-8	WR_THRSH	Write Threshold. Number of SDRAM write bursts after which the arbitration will switch to executing read commands. The value programmed is always minus 1 the required number.
7-5	Reserved	Value = 0x0 Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.
4-0	RD_THRSH	Read Threshold. Number of SDRAM read bursts after which the arbitration will switch to executing write commands. The value programmed is always minus 1 the required number.

4.28 1-Bit ECC Error Count Register (ONE_BIT_ECC_ERR_CNT)

The ONE_BIT_ECC_ERR_CNT register is described in the following figure and table.

Figure 4-28. 1-Bit ECC Error Count Register (ONE_BIT_ECC_ERR_CNT)



Legend: R = Read only; WS = write to subtract; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-30. 1-Bit ECC Error Count Register Field Descriptions

Bit	Field	Attribute	Description
31-0	1B_ECC_ERR_CNT	WS	32-bit counter that displays the number of 1-bit ECC errors. Writing a value will decrement the count by that value.

4.29 1-Bit ECC Error Threshold Register (ONE_BIT_ECC_ERR_THRSH)

The ONE_BIT_ECC_ERR_THRSH register is described in the following figure and table.

Figure 4-29. 1-Bit ECC Error Threshold Register (ONE_BIT_ECC_ERR_THRSH)

31	24	23	16	15	0
1B_ECC_ERR_THRSH		Reserved		1B_ECC_ERR_WIN	
RW=0x0		R=0x0		RW=0x0	

Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-31. 1-Bit ECC Error Threshold Register (ONE_BIT_ECC_ERR_THRSH) Field Descriptions

Bit	Field	Attribute	Description
31-24	1B_ECC_ERR_THRSH	RW	1-bit ECC error threshold. The DDR3 controller will generate an interrupt when the 1-bit ECC error count is greater than this threshold. A value of 0 will disable the generation of interrupt.
23-16	Reserved	R	Reserved for future use
15-0	1B_ECC_ERR_WIN	RW	1-bit ECC error window in number of refresh periods. The controller will generate an interrupt when the 1-bit ECC error count is equal to or greater than the threshold within this window. A value of 0 will disable the window. Refresh period is defined by REFRESH_RATE in SDRAM Refresh Control register.

4.30 1-Bit ECC Error Distribution 1 Register (ONE_BIT_ECC_ERR_DIST_1)

The ONE_BIT_ECC_ERR_DIST_1 register is described in the following figure and table.

Figure 4-30. 1-Bit ECC Error Distribution 1 Register (ONE_BIT_ECC_ERR_DIST_1)

31	0
1B_ECC_ERR_DST_1	
WOC=0x0	

Legend: R = Read only; WOC = Write one to clear; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

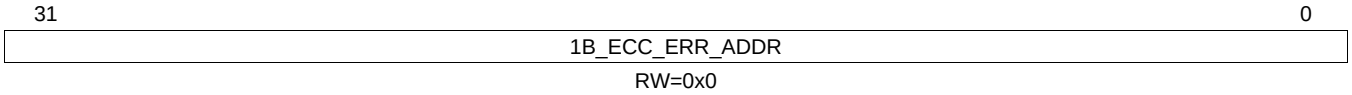
Table 4-32. 1-Bit ECC Error Distribution 1 Register (ONE_BIT_ECC_ERR_DIST_1) Field Descriptions

Bit	Field	Attribute	Description
31-0	1B_ECC_ERR_DST_1	WOC	1-bit ECC error distribution over data bus bits 31:0. A value of 1 on a bit indicates 1-bit error on the corresponding bit on the data bus. Writing a 1 to any bit will clear that bit. Writing a 0 has no effect.

4.31 1-Bit ECC Error Address Log Register (ONE_BIT_ECC_ERR_ADDR_LOG)

The ONE_BIT_ECC_ERR_ADDR_LOG register is described in the following figure and table.

Figure 4-31. 1-Bit ECC Error Address Log Register (ONE_BIT_ECC_ERR_ADDR_LOG)



Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

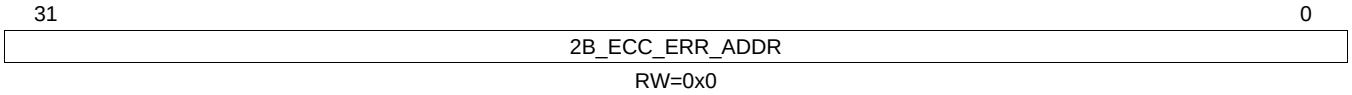
Table 4-33. 1-Bit ECC Error Address Log Register (ONE_BIT_ECC_ERR_ADDR_LOG) Field Descriptions

Bit	Field	Attribute	Description
31-0	1B_ECC_ERR_ADDR	RW	1-bit ECC error address. Most significant bits of the starting address of the first two SDRAM bursts that had the 1-bit ECC error. This field displays the first address logged in the 2 deep address logging FIFO. Writing a 0x1 will pop one element of the FIFO. Writing a 0x2 will pop both the elements of the FIFO. Writing any other value has no effect..

4.32 2-Bit ECC Error Address Log Register (TWO_BIT_ECC_ERR_ADDR_LOG)

The TWO_BIT_ECC_ERR_ADDR_LOG register is show in the figure and table below.

Figure 4-32. 2-Bit ECC Error Address Log Register (TWO_BIT_ECC_ERR_ADDR_LOG)



Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

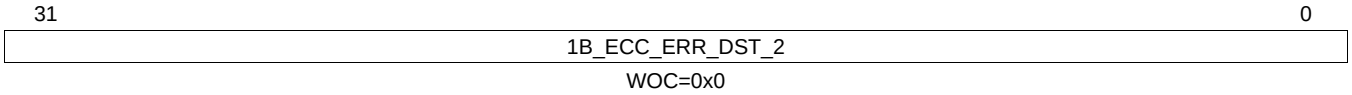
Table 4-34. 2-Bit ECC Error Address Log Register (TWO_BIT_ECC_ERR_ADDR_LOG) Field Descriptions

Bit	Field	Attribute	Description
31-0	2B_ECC_ERR_ADDR	RW	2-bit ECC error address. Most significant bits of the starting address of the first SDRAM burst that had the 2-bit ECC error. Writing a 0x1 will clear this field. Writing any other value has no effect..

4.33 1-Bit ECC Error Distribution 2 Register (ONE_BIT_ECC_ERR_DIST_2)

The ONE_BIT_ECC_ERR_DIST_2 register is described in the figure and table below.

Figure 4-33. 1-Bit ECC Error Distribution 2 Register (ONE_BIT_ECC_ERR_DIST_2)



Legend: R = Read only; WOC = Write one to clear; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-35. 1-Bit ECC Error Distribution 2 register (ONE_BIT_ECC_ERR_DIST_2) Field Descriptions

Bit	Field	Attribute	Description
31-0	1B_ECC_ERR_DST_2	WOC	1-bit ECC error distribution over data bus bits 63:32. A value of 1 on a bit indicates 1-bit error on the corresponding bit on the data bus. Writing a 1 to any bit will clear that bit. Writing a 0 has no effect.

4.34 PHY Initialization Register (PIR)

The PHY Initialization register is used to configure and control initialization of the DDR3 PHY. This includes the triggering of certain initialization routines, as well as reset of the PHY and/or the PLLs used in the PHY. Any PIR register bit used to trigger an initialization routine (bits 0 to 15) is self clearing and is set to 0 once the initialization is done. Any configuration register write that sets the PIR[INIT] register bit triggers initialization as selected by the other PIR register bits. The completion status of this initialization can be checked by polling the PHY General Status Register 0.

Figure 4-34. PHY Initialization Register (PIR)

31	30	29	28	27	26 20	19	18
INITBYP	ZCALBYP	DCALBYP	LOCKBYP	CLRSR	Reserved	Reserved	CTLDINIT
RW=0x0	RW=0x0	RW=0x0	RW=0x0	RW=0x0	R=0x0	RW=0x0	RW=0x0

17	16	15	14	13	12	11	10	9
PLLBYP	ICPC	WREYE	RDEYE	WRDSKW	RDDSKW	WLADJ	QSGATE	WL
RW=0x0	RW=0 x0	RW=0x0	RW=0x0	RW=0x0	RW=0x0	RW=0x0	RW=0x0	RW=0 x0

8	7	6	5	4	3 2	1	0
DRAMINIT	DRAMRST	PHYRST	DCAL	PLLINIT	Reserved	ZCAL	INIT
RW=0x0	RW=0x0	RW=0x0	RW=0x0	RW=0x0	R=0x0	RW=0x0	RW=0x0

Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-36. PHY Initialization Register (PIR) Field Descriptions

Bits	Name	Description
31	INITBYP	Reset = 0x0 Initialization Bypass: Bypasses or stops, if set, all initialization routines currently running, including PHY initialization, DRAM initialization, and PHY training. Initialization may be triggered manually using INIT and the other relevant bits of the PIR register. This bit is self-clearing.
30	ZCALBYP	Reset = 0x0 Impedance Calibration Bypass: Bypasses or stops, if set, impedance calibration of all ZQ control blocks that automatically triggers after reset. Impedance calibration may be triggered manually using INIT and ZCAL bits of the PIR register. This bit is self-clearing.
29	DCALBYP	Reset = 0x0 Digital Delay Line (DDL) Calibration Bypass: Bypasses or stops, if set, DDL calibration that automatically triggers after reset. DDL calibration may be triggered manually using INIT and DCAL bits of the PIR register. This bit is self-clearing.
28	LOCKBYP	Reset = 0x0 PLL Lock Bypass: Bypasses or stops, if set, the waiting of PLLs to lock. PLL lock wait is automatically triggered after reset. PLL lock wait may be triggered manually using INIT and PLLLOCK bits of the PIR register. This bit is self-clearing.
27	CLRSR	Reset = 0x0 Clear Status Registers: A write of '1' to this bit will clear (reset to ‘0’) all status registers, including PGSR and DXnGSR. The clear status register bit is self-clearing. Note, this bit does not clear the PGSR.IDONE bit. If the IDONE bit is set it remains at 1’b1 to indicate the PUB has competed its task. This bit is primarily for debug purposes and is typically not needed during normal functional operation. It can be used when PGSR.IDONE=1, to manually clear the PGSR status bits, although starting a new init process will automatically clear the PGSR status bits. Or it can be used to manually clear the DXnGSR status bits, although starting a new data training process will automatically clear the DXnGSR status bits.
26-19	Reserved	Reset = 0x0 Returns zeros on reads.
18	CTLDINIT	Reset = 0x0 Controller DRAM Initialization: Indicates if set that DRAM initialization will be performed by the controller. Otherwise if not set it indicates that DRAM initialization will be performed using the built-in initialization sequence or using software through the configuration port.
17	PLLBYP	Reset = 0x0 PLL Bypass: A setting of 1 on this bit will put all PHY PLLs in bypass mode.

Table 4-36. PHY Initialization Register (PIR) Field Descriptions (continued)

Bits	Name	Description
16	ICPC	Reset = 0x0 Initialization Complete Pin Configuration: Specifies how the DFI initialization complete output pin (dfi_init_complete) should be used to indicate the status of initialization. Valid value are: • 0 = Asserted after PHY initialization (DLL locking and impedance calibration) is complete. • 1 = Asserted after PHY initialization is complete and the triggered the PUB initialization (DRAM initialization, data training, or initialization trigger with no selected initialization) is complete.
15	WREYE	Reset = 0x0 Write Data Eye Training: Executes a PUB training routine to maximize the write data eye.
14	RDEYE	Reset = 0x0 Read Data Eye Training: Executes a PUB training routine to maximize the read data eye.
13	WRDSKW	Reset = 0x0 Write Data Bit Deskew: Executes a PUB training routine to deskew the DQ bits during write
12	RDDSKW	Reset = 0x0 Read Data Bit Deskew: Executes a PUB training routine to deskew the DQ bits during read
11	WLADJ	Reset = 0x0 Write Leveling Adjust (DDR3 Only): Executes a PUB training routine that readjusts the write latency used during write in case the write leveling routine changed the expected latency.
10	QSGATE	Reset = 0x0 Read DQS Gate Training: Executes a PUB training routine to determine the optimum position of the read data DQS strobe for maximum system timing margins
9	WL	Reset = 0x0 Write Leveling (DDR3 Only): Executes a PUB write leveling routine.
8	DRAMINIT	Reset = 0x0 DRAM Initialization: Executes the DRAM initialization sequence
7	DRAMRST	Reset = 0x0 DRAM Reset: Issues a reset to the DRAM (by driving the DRAM reset pin low) and wait 200us. This can be triggered in isolation or with the full DRAM initialization (DRAMINIT). For the later case, the reset is issued and 200us is waited before starting the full initialization sequence.
6	PHYRST	Reset = 0x0 PHY Reset: Resets the AC and DATX8 modules by asserting the AC/DATX8 reset pin.
5	DCAL	Reset = 0x0 Digital Delay Line (DDL) Calibration: Performs PHY delay line calibration.
4	PLLINIT	Reset = 0x0 PLL Initialization: Executes the PLL initialization sequence which includes correct driving of PLL power-down, reset and gear shift pins, and then waiting for the PHY PLLs to lock.
3-2	Reserved	Reset = 0x0 Returns zeros on reads
1	ZCAL	Reset = 0x0 Impedance Calibration: Performs PHY impedance calibration. When set the impedance calibration will be performed in parallel with PHY initialization (PLL initialization + DDL calibration + PHY reset).
0	INIT	Reset = 0x0 Initialization Trigger: A write of '1' to this bit triggers the DDR system initialization, including PHY initialization, DRAM initialization, and PHY training. The exact initialization steps to be executed are specified in bits 1 to 15 of this register. A bit setting of 1 means the step will be executed as part of the initialization sequence, while a setting of ‘0’ means the step will be bypassed. The initialization trigger bit is self-clearing.

4.35 PHY General Configuration Register 0 (PGCR0)

PGCR0-2 are used for miscellaneous PHY configurations such as enabling VT drift compensation and setting up write-leveling.

Figure 4-35. PHY General Configuration Register 0 (PGCR0)

31 26	25 19	18 14	13 12	11 9	8	7
CKEN	Reserved	DTOSEL	OSCWDL	OSCDIV	OSCEN	DLTST
RW=0x2A	R=0x0	RW=0x0	RW=0x3	RW=0x7	RW=0x0	RW=0x0
6	5	4	3	2	1	0
DLTMODE	RDBVT	WDBVT	RGLVT	RDLVT	WDLVT	WLLVT
RW=0x0	RW=0x1	RW=0x1	RW=0x1	RW=0x1	RW=0x1	RW=0x1

Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-37. PHY General Configuration Register 0 (PGCR0) Field Descriptions

Bits	Name	Description
31-26	CKEN	Reset = 101010b CK Enable: Controls whether the CK going to the SDRAM is enabled (toggling) or disabled (static value) and whether the CK is inverted. Two bits for each of the up to three CK pairs. Valid values for the two bits are: • 00 = CK disabled (Driven to constant 0) • 01 = CK toggling with inverted polarity • 10 = CK toggling with normal polarity (This should be the default setting) • 11 = CK disabled (Driven to constant 1) TI recommends that this field be always programmed to 101010b.
25-19	Reserved	Reset = 0x0 Returns zeros on reads.
18-14	DTOSEL	Reset = 0x0 Digital Test Output Select: Selects the PHY digital test output that should be driven onto PHY digital test output (phy_dto) pin: Valid values are: • 00000 = DATX8 0 PLL digital test output • 00001 = DATX8 1 PLL digital test output • 00010 = DATX8 2 PLL digital test output • 00011 = DATX8 3 PLL digital test output • 00100 = DATX8 4 PLL digital test output • 00101 = DATX8 5 PLL digital test output • 00110 = DATX8 6 PLL digital test output • 00111 = DATX8 7 PLL digital test output • 01000 = DATX8 8 PLL digital test output • 01001 = AC PLL digital test output • 01010 – 01111 = Reserved • 10000 = DATX8 0 delay line digital test output • 10001 = DATX8 1 delay line digital test output • 10010 = DATX8 2 delay line digital test output • 10011 = DATX8 3 delay line digital test output • 10100 = DATX8 4 delay line digital test output • 10101 = DATX8 5 delay line digital test output • 10110 = DATX8 6 delay line digital test output • 10111 = DATX8 7 delay line digital test output • 11000 = DATX8 8 delay line digital test output • 11001 = AC delay line digital test output • 11010 – 11111 = Reserved

Table 4-37. PHY General Configuration Register 0 (PGCR0) Field Descriptions (continued)

Bits	Name	Description
13-12	OSCWDL	Reset = 0x3 Oscillator Mode Write-Leveling Delay Line Select: Selects which of the two write leveling LCDLs is active. The delay select value of the inactive LCDL is set to zero while the delay select value of the active LCDL can be varied by the input write leveling delay select pin. Valid values are: • 00 = No WL LCDL is active • 01 = DDR WL LCDL is active • 10 = SDR WL LCDL is active • 11 = Both LCDLs are active
11-9	OSCDIV	Reset = 0x7 Oscillator Mode Division: Specifies the factor by which the delay line oscillator mode output is divided down before it is output on the delay line digital test output pin dl_dto. Valid values are: • 000 = Divide by 1 • 001 = Divide by 256 • 010 = Divide by 512 • 011 = Divide by 1024 • 100 = Divide by 2048 • 101 = Divide by 4096 • 110 = Divide by 8192 • 111 = Divide by 65536
8	OSCEN	Reset = 0x0 Oscillator Enable: Enables, if set, the delay line oscillation.
7	DLTST	Reset = 0x0 Delay Line Test Start: A write of '1' to this bit will trigger delay line oscillator mode period measurement. This bit is not self clearing and needs to be reset to '0' before the measurement can be re-triggered.
6	DLTMODE	Reset = 0x0 Delay Line Test Mode: Selects, if set, the delay line oscillator test mode.
5	RDBVT	Reset = 0x1 Read Data BDL VT Compensation: Enables, if set the VT drift compensation of the read data bit delay lines
4	WDBVT	Reset = 0x1 Write Data BDL VT Compensation: Enables, if set the VT drift compensation of the write data bit delay lines.
3	RGLVT	Reset = 0x1 Read DQS Gating LCDL Delay VT Compensation: Enables, if set the VT drift compensation of the read DQS gating LCDL
2	RDLVT	Reset = 0x1 Read DQS LCDL Delay VT Compensation: Enables, if set the VT drift compensation of the read DQS LCDL.
1	WDLVT	Reset = 0x1 Write DQ LCDL Delay VT Compensation: Enables, if set the VT drift compensation of the write DQ LCDL.
0	WLLVT	Reset = 0x1 Write Leveling LCDL Delay VT Compensation: Enables, if set, the VT drift compensation of the write leveling LCDL

4.36 PHY General Configuration Register 1 (PGCR1)

PGCR0-2 are used for miscellaneous PHY configurations such as enabling VT drift compensation and setting up write-leveling.

Figure 4-36. PHY General Configuration Register 1 (PGCR1)

31	30	29	28	27	26	25
LBMODE	LBGDQS		LBDQSS	IOLB	INHVT	PHYHRST
RW=0x0	RW=0x0		RW=0x0	RW=0x0	RW=0x0	RW=0x1

24	23	22	15	14	13	12	11	10	9
ZCKSEL		DLDLMT		FDEPTH		LPFDEPTH		LPFEN	MDLEN
RW=0x2		RW=0x1		RW=0x2		RW=0x0		RW=0x1	RW=0x0

8	7	6	5	3	2	1	0
IODDRM		WLSELT	Reserved		WLSTEP	WLMODE	PDDISDX
RW=0x0		RW=0x1	R=0x4		RW=0x0	RW=0x0	RW=0x1

Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-38. PHY General Configuration Register 1 (PGCR1) Field Descriptions

Bits	Name	Description
31	LBMODE	Reset = 0x0 Loopback Mode: Indicates, if set, that the PHY/PUB is in loopback mode
30-29	LBGDQS	Reset = 0x0 Loopback DQS Gating: Selects the DQS gating mode that should be used when the PHY is in loopback mode, including BIST loopback mode. Valid values are: • 00 = DQS gate is always on • 01 = DQS gate training will be triggered on the PUB • 10 = DQS gate is set manually using software • 11 = Reserved
28	LBDQSS	Reset = 0x0 Loopback DQS Shift: Selects how the read DQS is shifted during loopback to ensure that the read DQS is centered into the read data eye. Valid values are: • 0 = PUB sets the read DQS LCDL to 0; DQS is already shifted 90 degrees by write path • 1 = The read DQS shift is set manually through software
27	IOLB	Reset = 0x0 I/O Loop-Back Select: Selects where inside the I/O the loop-back of signals happens. Valid values are: • 0 = Loopback is after output buffer; output enable must be asserted • 1 = Loopback is before output buffer; output enable is don't care
26	INHVT	Reset = 0x0 VT Calculation Inhibit: Inhibits calculation of the next VT compensated delay line values. A value of 1 will inhibit the VT calculation. This bit should be set to 1 during writes to the delay line registers. This bit should NOT be set to 1 until after PHY initialization completes
25	PHYHRST	Reset = 0x0 PHY High-Speed Reset: A write of '0' to this bit resets the AC and DATX8 macros without resetting PUB RTL logic. This bit is not self-clearing and a '1' must be written to de-assert the reset
24-23	ZCKSEL	Reset = 0x2 Impedance Clock Divider Select: Selects the divide ratio for the clock used by the impedance control logic relative to the clock used by the memory controller and SDRAM. Valid values are: • 00 = Divide by 2 • 01 = Divide by 8 • 10 = Divide by 32 • 11 = Divide by 64 TI recommends that this field be always programmed to 01b.

Table 4-38. PHY General Configuration Register 1 (PGCR1) Field Descriptions (continued)

Bits	Name	Description
22-15	DLDLMT	Reset = 0x1 Delay Line VT Drift Limit: Specifies the minimum change in the delay line VT drift in one direction which should result in the assertion of the delay line VT drift status signal (vt_drift). The limit is specified in terms of delay select values. A value of 0 disables the assertion of delay line VT drift status signal.
14-13	FDEPTH	Reset = 0x2 Filter Depth: Specifies the number of measurements over which all AC and DATX8 initial period measurements, that happen after reset or when calibration is manually triggered, are averaged. Valid values are: • 00 = 2 • 01 = 4 • 10 = 8 • 11 = 16
12-11	LPFDEPTH	Reset = 0x0 Low-Pass Filter Depth: Specifies the number of measurements over which MDL period measurements are filtered. This determines the time constant of the low pass filter. Valid values are: • 00 = 2 • 01 = 4 • 10 = 8 • 11 = 16
10	LPFEN	Reset = 0x1 Low-Pass Filter Enable: Enables, if set, the low pass filtering of MDL period measurements.
9	MDLEN	Reset = 0x0 Master Delay Line Enable: Enables, if set, the AC master delay line calibration to perform subsequent period measurements following the initial period measurements that are performed after reset or on when calibration is manually triggered. These additional measurements are accumulated and filtered as long as this bit remains high.
8-7	IODDRM	Reset = 0x0 This field should be programmed to 0x1 if using DDR3 and 0x2 if using DDR3L. • 1 = DDR3 • 2 = DDR3L
6	WLSELT	Reset = 0x0 Write Leveling Select Type: Selects the encoding type for the write leveling select signal depending on the desired setup/hold margins for the internal pipelines. Valid values are: • 0 = Setup margin of 90 degrees and hold margin of 90 degrees • 1 = Setup margin of 135 degrees and hold margin of 45 degrees
5-3	Reserved	Reset = 0x0 Return zeros on reads.
2	WLSTEP	Reset = 0x0 Write Leveling Step: Specifies the number of delay step-size increments during each step of write leveling. Valid values are: • 0 = 32 step sizes • 1 = 1 step size
1	WLMODE	Reset = 0x1 Write Leveling (Software) Mode: Indicates if set that the PHY is in software write leveling mode in which software executes single steps of DQS pulsing by writing '1' to PIR.WL. The write leveling DQ status from the DRAM is captured in DXnGSR0.WLDQ
0	PDDISDX	Reset = 0x1 Power Down Disabled Byte: Indicates if set that the PLL and I/Os of a disabled byte should be powered down

4.37 PHY General Configuration Register 2 (PGCR2)

PGCR0-2 are used for miscellaneous PHY configurations such as enabling VT drift compensation and setting up write-leveling.

Figure 4-37. PHY General Configuration Register 2 (PGCR2)

31	30 28	27 20	19	18	17 0
DYNACPDD	Reserved	DTPMXTMR	FXDLAT	NOBUB	tREFPRD
RW=0x0	R=0x0	RW=0xF	RW=0x0	RW=0x0	RW=0x12480

Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-39. PHY General Configuration Register 2 (PGCR2) Field Descriptions

Bits	Name	Description
31	DYNACPDD	Dynamic AC Power Down Driver: Powers down, when set, the output driver on I/O for the address and bank address lines
30-28	Reserved	Reset = 0x0 These bits should be always programmed to 0.
27-20	DTPMXTMR	Reset = 0x0F Data Training PUB Mode Timer Exit: Specifies the number of controller clocks to wait when entering and exiting pub mode data training. The default value ensures controller refreshes do not cause memory model errors when entering and exiting data training. The value should be increased if controller initiated SDRAM ZQ short or long operation may occur just before or just after the execution of data training.
19	FXDLAT	Reset = 0x0 Fixed Latency: Specified whether all reads should be returned to the controller with a fixed read latency. Enabling fixed read latency increases the read latency. Valid values are: • 0 = Disable fixed read latency • 1 = Enable fixed read latency Fixed read latency is calculated as (12 + (maximum DXnGTR.RxDGSL)/2) half data rate clock cycles.
18	NOBUB	Reset = 0x0 No Bubbles: Specified whether reads should be returned to the controller with no bubbles. Enabling no-bubble reads increases the read latency. Valid values are: • 0 = Bubbles are allowed during reads • 1 = Bubbles are not allowed during reads
17-0	tREFPRD	Reset = 0x12480 Refresh Period: Indicates the period in clock cycles after which the PUB has to issue a refresh command to the SDRAM. This is derived from the maximum refresh interval from the datasheet, tRFC(max) or REFI, divided by the clock cycle time. A further 400 clocks must be subtracted from the derived number to account for command flow and missed slots of refreshes in the internal PUB blocks. The default corresponds to DDR3 9*7.8us at 1066MHz (DDR3-2133) when a burst of 9 refreshes are issued at every refresh interval. TI recommends tREFPRD be programmed to 5*tREFI.

4.38 PHY General Status Register 0 (PGSR0)

PGSR0-1 are general status registers for the PHY. They indicate, among other things, whether initialization, write leveling or period measurement calibrations are done.

Figure 4-38. PHY General Status Register 0 (PGSR0)

31	30 28	27	26	25	24	23	22
APLOCK	Reserved	WEERR	REERR	WDERR	RDERR	WLAERR	QSGERR
R=0x0	R=0x0	R=0x0	R=0x0	R=0x0	R=0x0	R=0x0	R=0x0
21	20	19 12	11	10	9	8	
WLERR	ZCERR	Reserved	WEDONE	REDONE	WDDONE	RDDONE	
R=0x0	R=0x0	R=0x0	R=0x0	R=0x0	R=0x0	R=0x0	
7	6	5	4	3	2	1	0
WLADONE	QSGDONE	WLDONE	DIDONE	ZCDONE	DCDONE	PLDONE	IDONE
R=0x0	R=0x0	R=0x0	R=0x0	R=0x0	R=0x0	R=0x0	R=0x0

Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-40. PHY General Status Register 0 (PGSR0) Field Descriptions

Bits	Name	Description
31	APLOCK	Reset = 0x0 AC PLL Lock: Indicates, if set, that AC PLL has locked. This is a direct status of the AC PLL lock pin
30-28	Reserved	Reset = 0x0 Returns zeros on reads.
27	WEERR	Reset = 0x0 Write Eye Training Error: Indicates if set that there is an error in write eye training.
26	REERR	Reset = 0x0 Read Eye Training Error: Indicates if set that there is an error in read eye training
25	WDERR	Reset = 0x0 Write Bit Deskew Error: Indicates if set that there is an error in write bit deskew
24	RDERR	Reset = 0x0 Read Bit Deskew Error: Indicates if set that there is an error in read bit deskew
23	WLAERR	Reset = 0x0 Write Leveling Adjustment Error: Indicates if set that there is an error in write leveling adjustment
22	QSGERR	Reset = 0x0 DQS Gate Training Error: Indicates if set that there is an error in DQS gate training.
21	WLERR	Reset = 0x0 Write Leveling Error: Indicates if set that there is an error in write leveling.
20	ZCERR	Reset = 0x0 Impedance Calibration Error: Indicates if set that there is an error in impedance calibration.
19-12	Reserved	Reset = 0x0 Returns zeros on reads.
11	WEDONE	Reset = 0x0 Write Eye Training Done: Indicates if set that write eye training has completed
10	REDONE	Reset = 0x0 Read Eye Training Done: Indicates if set that read eye training has completed
9	WDDONE	Reset = 0x0 Write Bit Deskew Done: Indicates if set that write bit deskew has completed.
8	RDDONE	Reset = 0x0 Read Bit Deskew Done: Indicates if set that read bit deskew has completed
7	WLADONE	Reset = 0x0 Write Leveling Adjustment Done: Indicates if set that write leveling adjustment has completed
6	QSGDONE	Reset = 0x0 DQS Gate Training Done: Indicates if set that DQS gate training has completed.

Table 4-40. PHY General Status Register 0 (PGSR0) Field Descriptions (continued)

Bits	Name	Description
5	WLDONE	Reset = 0x0 Write Leveling Done: Indicates if set that write leveling has completed.
4	DIDONE	Reset = 0x0 DRAM Initialization Done: Indicates if set that DRAM initialization has completed
3	ZCDONE	Reset = 0x0 Impedance Calibration Done: Indicates if set that impedance calibration has completed
2	DCDONE	Reset = 0x0 Digital Delay Line (DDL) Calibration Done: Indicates if set that DDL calibration has completed
1	PLDONE	Reset = 0x0 PLL Lock Done: Indicates if set that PLL locking has completed.
0	IDONE	Reset = 0x0 Initialization Done: Indicates if set that the DDR system initialization has completed. This bit is set after all the selected initialization routines in PIR register have completed.

4.39 PHY General Status Register 1 (PGSR1)

PGSR0-1 are general status registers for the PHY. They indicate, among other things, whether initialization, write leveling or period measurement calibrations are done.

Figure 4-39. PHY General Status Register 1 (PGSR1)

31	30	29 25	24 1	0
Reserved	VTSTOP	Reserved	DLTCODE	DLTDONE
R=0x0	R=0x0	R=0x0	R=0x0	R=0x0

Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-41. PHY General Status Register 1 (PGSR1) Field Descriptions

Bits	Name	Description
31	Reserved	Reset = 0x0 Returns zeros on reads.
30	VTSTOP	Reset = 0x0 VT Stop: Indicates if set that the VT calculation logic has stopped computing the next values for the VT compensated delay line values. After assertion of the PGCR.INHVT, the VTSTOP bit should be read to ensure all VT compensation logic has stopped computations before writing to the delay line registers
29-25	Reserved	Reset = 0x0 Returns zeros on reads.
24-1	DLTCODE	Reset = 0x0 Delay Line Test Code: Returns the code measured by the PHY control block that corresponds to the period of the AC delay line digital test output.
0	DLTDONE	Reset = 0x0 Delay Line Test Done: Indicates, if set, that the PHY control block has finished doing period measurement of the AC delay line digital test output

4.40 PLL Control Register (PLLCR)

The PLLCR register provides miscellaneous controls of the PLLs used in the AC and DATX8 macros, including PLL test modes and PLL bypass.

Figure 4-40. PLL Control Register (PLLCR)

31	30	29	28 20	19 18	17	16 13	12 11	9 0
BYP	PLLRST	PLLPD	Reserved	FRQSEL	QPMODE	CPPC	CPIC	Reserved
RW=0x0	RW=0x0	RW=0x0	R=0x0	RW=0x0	RW=0x0	RW=0xE	RW=0x0	R=0x0

Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-42. PLL Control Register (PLLCR) Field Descriptions

Bits	Name	Description
31	BYP	Reset = 0x0 PLL Bypass: Bypasses the PLL if set to 1.
30	PLLRST	Reset = 0x0 PLL Rest: Resets the PLLs by driving the PLL reset pin. This bit is not self-clearing and a '0' must be written to de-assert the reset.
29	PLLPD	Reset = 0x0 PLL Power Down: Puts the PLLs in power down mode by driving the PLL power down pin. This bit is not self-clearing and a '0' must be written to de-assert the power-down
28-20	Reserved	Reset = 0x0 Returns zeros on reads.
19-18	FRQSEL	Reset = 0x0 PHY PLL reference frequency select: Selects the operating range of the PHY PLL. Valid values are: • 00 = PHY PLL reference clock ranges from 335 MHz to 533 MHz • 01 = PHY PLL reference clock ranges from 225 MHz to 385 MHz • 10 = Reserved • 11 = PHY PLL reference clock ranges from 166 MHz to 275 MHz
17	QPMODE	Reset = 0x0 PLL Quadrature Phase Mode: Enables, if set, the quadrature phase clock outputs. This mode is not used in this version of the PHY
16-13	CPPC	Reset = 0xE Charge Pump Proportional Current Control
12-11	CPIC	Reset = 0x0 Charge Pump Integrating Current Control
10	GSHIFT	Gear Shift: Enables, if set, rapid locking mode.
9-0	Reserved	Reset = 0x0 Reads return zeros

4.41 PHY Timing Register 0 (PTR0)

PHY Timing Registers are used to program different timing parameters used by the PHY logic. All the default values shown in these tables are in decimal format and correspond to the DDR3-2133N speed grade. This corresponds to DRAM bit rate of 2133Mbps, DRAM clock frequency of 1066MHz, controller clock frequency of 533MHz, and configuration clock frequency of 533MHz. Configure these parameters assuming controller and configuration clocks of 533MHz. The clocks in which the timing numbers are measured are specified in the description of each parameter.

Figure 4-41. PHY Timing Register 0 (PTR0)

31 21	20 6	5 0
tPLLPD	tPHYRST	tPHYRST
RW=0x216	RW=0x856	RW=0x10

Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-43. PHY Timing Register 0 (PTR0) Field Descriptions

Bits	Name	Description
31-21	tPLLPD	Reset = 0x216 PLL Power-Down Time: Number of configuration clock cycles that the PLL must remain in power-down mode, i.e. number of clock cycles from when PLL power-down pin is asserted to when PLL power-down pin is de-asserted. This must correspond to a value that is equal to or more than 1us. Default value corresponds to 1us.
20-6	tPLLGS	Reset = 0x856 PLL Gear Shift Time: Number of configuration clock cycles from when the PLL reset pin is de-asserted to when the PLL gear shift pin is de-asserted. This must correspond to a value that is equal to or more than 4us. Default value corresponds to 4us.
5-0	tPHYRST	Reset = 0xF PHY Reset Time: Number of configuration clock cycles that the PHY reset must remain asserted after PHY calibration is done before the reset to the PHY is de-asserted. This is used to extend the reset to the PHY so that the reset is asserted for some clock cycles after the clocks are stable. TI recommends setting this to 15.

4.42 PHY Timing Register 1 (PTR1)

PHY Timing Registers are used to program different timing parameters used by the PHY logic. All the default values shown in these tables are in decimal format and correspond to the highest speed the PHY can be compiled for, i.e. JEDEC DDR3-2133N speed grade. This corresponds to DRAM bit rate of 2133Mbps, DRAM clock frequency of 1066MHz, controller clock frequency of 533MHz, and configuration clock frequency of 533MHz. Configure these parameters assuming controller and configuration clocks of 533MHz. The clocks in which the timing numbers are measured are specified in the description of each parameter.

Figure 4-42. PHY Timing Register 1 (PTR1)

31 16	15 13	12 0
tPLLLOCK	Reserved	tPLLRST
RW=0xD056	R=0x0	RW=0x12C0

Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-44. PHY Timing Register 1 (PTR1) Field Descriptions

Bits	Name	Description
31-16	tPLLLOCK	Reset = 0xD056 PLL Lock Time: Number of configuration clock cycles for the PLL to stabilize and lock, i.e., number of clock cycles from when the PLL reset pin is de-asserted to when the PLL has lock and is ready for use. This must correspond to a value that is equal to or more than 100us. Default value corresponds to 100us
15-13	Reserved	Reset = 0x0 Reads return zeros.
12-0	tPLLRST	Reset = 0x12C0 PLL Reset Time: Number of configuration clock cycles that the PLL must remain in reset mode, i.e. , number of clock cycles from when PLL power-down pin is de-asserted and PLL reset pin is asserted to when PLL reset pin is de-asserted. This must correspond to a value that is equal to or more than 9 us. Default value corresponds to 9 us.

4.43 PHY Timing Register 2 (PTR2)

PHY Timing Registers are used to program different timing parameters used by the PHY logic. All the default values shown in these tables are in decimal format and correspond to the highest speed the PHY can be compiled for, i.e. JEDEC DDR3-2133N speed grade. This corresponds to DRAM bit rate of 2133Mbps, DRAM clock frequency of 1066MHz, controller clock frequency of 533MHz, and configuration clock frequency of 533MHz. Configure these parameters assuming controller and configuration clocks of 533MHz. The clocks in which the timing numbers are measured are specified in the description of each parameter.

Figure 4-43. PHY Timing Register 2 (PTR2)

31 20	19 15	14 10	9 5	4 0
Reserved	tWLDLYS	tCALH	tCALS	tCALON
RW=0x0	RW=0x10	RW=0xF	RW=0xF	RW=0xF

Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-45. PHY Timing Register 2 (PTR2) Field Descriptions

Bits	Name	Description
31-20	Reserved	Reset = 0x0 Reads return zeros.
19-15	tWLDLYS	Reset = 0x10 Write Leveling Delay Settling Time: Number of controller clock cycles from when a new value of the write leveling delay is applies to the LCDL to when to DQS high is driven high. This allows the delay to settle
14-10	tCALH	Reset = 0xF Calibration Hold Time: Number of controller clock cycles from when the clock was disabled (cal_clk_en deasserted) to when calibration is enable (cal_en asserted).
9-5	tCALS	Reset = 0xF Calibration Setup Time: Number of controller clock cycles from when calibration is enabled (cal_en asserted) to when the calibration clock is asserted again (cal_clk_en asserted).
4-0	tCALON	Reset = 0xF Calibration On Time: Number of controller clock cycles that the calibration clock is enabled (cal_clk_en asserted).

4.44 PHY Timing Register 3 (PTR3)

PHY Timing Registers are used to program different timing parameters used by the PHY logic. All the default values shown in these tables are in decimal format and correspond to the highest speed the PHY can be compiled for, i.e. JEDEC DDR3-2133N speed grade. This corresponds to DRAM bit rate of 2133Mbps, DRAM clock frequency of 1066MHz, controller clock frequency of 533MHz, and configuration clock frequency of 533MHz. Configure these parameters assuming controller and configuration clocks of 533MHz. The clocks in which the timing numbers are measured are specified in the description of each parameter.

Figure 4-44. PHY Timing Register 3 (PTR3)

31 29	28 20	19 0
Reserved	tDINIT1	tDINIT0
R=0x0	RW=0x180	RW=0xD056

Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-46. PHY Timing Register 3 (PTR3) Field Descriptions

Bits	Name	Description
31-29	Reserved	Reset = 0x0 Reads return zeros.
28-20	tDINIT1	Reset = 0x180 DRAM Initialization Time 1: DRAM initialization time in DRAM clock cycles corresponding to the following: DDR3 = CKE high time to first command (tRFC + 10 ns or 5 tCK, whichever is bigger) Default value corresponds to DDR3 tRFC of 360ns at 1066 MHz tDINIT1 = (tCKE/tCK)-1
19-0	tDINIT0	Reset = 0x82536 DRAM Initialization Time 0: DRAM initialization time in DRAM clock cycles corresponding to the following: DDR3 = CKE low time with power and clock stable (500 us)

4.45 PHY Timing Register 4 (PTR4)

PHY Timing Registers are used to program different timing parameters used by the PHY logic. All the default values shown in these tables are in decimal format and correspond to the highest speed the PHY can be compiled for, i.e. JEDEC DDR3-2133N speed grade. This corresponds to DRAM bit rate of 2133Mbps, DRAM clock frequency of 1066MHz, controller clock frequency of 533MHz, and configuration clock frequency of 533MHz. Configure these parameters assuming controller and configuration clocks of 533MHz. The clocks in which the timing numbers are measured are specified in the description of each parameter.

Figure 4-45. PHY Timing Register 4 (PTR4)

31 28	27 18	17 0
Reserved	tDINIT3	tDINIT2
R=0x0	RW=0x2AB	RW=0x34156

Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-47. PHY Timing Register 4 (PTR4) Field Descriptions

Bits	Name	Description
31-28	Reserved	Reset = 0x0 Reads return zeros.
27-18	tDINIT3	Reset = 0x2AB DRAM Initialization Time 3: DRAM initialization time in DRAM clock cycles corresponding to the following: DDR3 = Time from ZQ initialization command to first command (1 us) Default value corresponds to the DDR3 640ns at 1066 MHz.
17-0	tDINIT2	Reset = 0x34156 DRAM Initialization Time 2: DRAM initialization time in DRAM clock cycles corresponding to the following: DDR3 = Reset low time (200 us on power-up or 100 ns after power-up) Default value corresponds to DDR3 200 us at 1066 MHz.

4.46 AC I/O Configuration Register (ACIOCR)

The AC I/O Configuration Register is used to control the slew rate on the address/command lines.

Figure 4-46. AC I/O Configuration Register (ACIOCR)

31	30	29	0
ACSR		Reserved	
RW=0x0		R=0x33C03812	

Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-48. AC I/O Configuration Register (ACIOCR) Field Descriptions

Bits	Name	Description
31-30	ACSR	Reset = 0x0 Address/Command Slew Rate: Selects slew rate of the I/O for all address and command pins. 00 = very fast (use as default for DDR3 and DDR3L) 01 = fast 10 = medium 11 = slow
29-0	Reserved	Reset = 0x33C03812 Reserved.

4.47 DATX8 Common Configuration Register (DXCCR)

The DATX8 Common Configuration Register is used to control features that affect all DATX8 macros. These include on-die termination enables and power-down enables for SSTL I/Os for all SDRAM data, data mask and data strobe signals.

Figure 4-47. DATX8 Common Configuration Register (DXCCR)

31 28	27 24	23	22	21	20	19
DDPDRCDO	DDPDDCDO	DYNDXPDR	DYNDXPDD	UDQIOM	UDQPDR	UDQPDD
RW=0x4	RW=0x4	RW=0x0	RW=0x0	RW=0x0	RW=0x1	RW=0x1

18	17 15	14 13	12 9	8 5	4	3	2	1	0
UDQODT	MSBUDQ	DXSR	DQSNRES	DQSRES	DXPDR	DXPDD	MDLEN	DXIOM	DXODT
RW=0x0	RW=0x0	RW=0x0	RW=0xC	RW=0x4	RW=0x0	RW=0x0	RW=0x1	RW=0x0	RW=0x0

Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-49. DATX8 Common Configuration Register (DXCCR) Field Descriptions

Bits	Name	Description
31-28	DDPDRCDO	Reset = 0x4 Dynamic Data Power Down Receiver Count Down Offset: Offset applied in calculating window of time where receiver is powered up
27-24	DDPDDCDO	Reset = 0x4 Dynamic Data Power Down Driver Count Down Offset: Offset applied in calculating window of time where driver is powered up
23	DYNDXPDR	Reset = 0x0 Data Power Down Receiver: Dynamically powers down, when set, the input receiver on I/O for the DQ pins of the active DATX8 macros. Applies only when DXPDR and DXnGCR.DXPDR are not set to 1.
22	DYNDXPDD	Reset = 0x0 Dynamic Data Power Down Driver: Dynamically powers down, when set, the output driver on I/O for the DQ pins of the active DATX8 macros. Applies only when DXPDD and DXnGCR.DXPDD are not set to 1.
21	UDQIOM	Reset = 0x0 Unused DQ I/O Mode: Selects SSTL mode (when set to 0) or CMOS mode (when set to 1) of the I/O for unused DQ pins.
20	UDQPDR	Reset = 0x1 Unused DQ Power Down Receiver: Powers down, when set, the input receiver on the I/O for unused DQ pins.
19	UDQPDD	Reset = 0x1 Unused DQ Power Down Driver: Powers down, when set, the output driver on the I/O for unused DQ pins.
18	UDQODT	Reset = 0x0 Unused DQ On-Die Termination: Enables, when set, the on-die termination on the I/O for unused DQ pins.
17-15	MSBUDQ	Reset = 0x0 Most Significant Byte Unused DQs: Specifies the number of DQ bits that are not used in the most significant byte. The used (valid) bits for this byte are [8-MSBDQ- 1:0]. To disable the whole byte, use the DXnGCR.DXEN register.
14-13	DXSR	Reset = 0x0 Data Slew Rate: Selects slew rate of the I/O for DQ, DM, and DQS/DQS# pins of all DATX8 macros. 00 = very fast (use as default for DDR3 and DDR3L) 01 = fast 10 = medium 11 = slow
12-9	DQSNRES	Reset = 0xC DQS# Resistor: Selects the on-die pull-up/pull-down resistor for DQS# pins. Same encoding as DQSRES.

Table 4-49. DATX8 Common Configuration Register (DXCCR) Field Descriptions (continued)

Bits	Name	Description
8-5	DQSRES	Reset = 0x4 DQS Resistor: Selects the on-die pull-down/pull-up resistor for DQS pins. DQSRES[3] selects pull-down (when set to 0) or pull-up (when set to 1). DQSRES[2:0] selects the resistor value as follows: 000 = Open: On-die resistor disconnected (use external resistor) 001 = 688 ohms 010 = 611 ohms 011 = 550 ohms 100 = 500 ohms 101 = 458 ohms 110 = 393 ohms 111 = 344 ohms
4	DXPDR	Reset = 0x0 Data Power Down Receiver: Powers down, when set, the input receiver on I/O for DQ, DM, and DQS/DQS# pins of all DATX8 macros. This bit is ORed with the PDR configuration bit of the individual DATX8.
3	DXPDD	Reset = 0x0 Data Power Down Driver: Powers down, when set, the output driver on I/O for DQ,DM, and DQS/DQS# pins of all DATX8 macros. This bit is ORed with the PDD configuration bit of the individual DATX8.
2	MDLEN	Reset = 0x1 Master Delay Line Enable: Enables, if set, all DATX8 master delay line calibration to perform subsequent period measurements following the initial period measurements that are performed after reset or on when calibration is manually triggered. These additional measurements are accumulated and filtered as long as this bit remains high. This bit is ANDed with the MDLEN bit in the individual DATX8
1	DXIOM	Reset = 0x0 Data I/O Mode: Selects SSTL mode (when set to 0) or CMOS mode (when set to 1) of the I/O for DQ, DM, and DQS/DQS# pins of all DATX8 macros. This bit is ORed with the IOM configuration bit of the individual DATX8.
0	DXODT	Reset = 0x0 Data On-Die Termination: Enables, when set, the on-die termination on the I/O for DQ, DM, and DQS/DQS# pins of all DATX8 macros. This bit is ORed with the ODT configuration bit of the individual DATX8

4.48 DRAM Configuration Register (DCR)

The DCR register is used to configure the DRAM system, and is described in the figure and table below.

Figure 4-48. DRAM Configuration Register (DCR)

31 30	29	28	27	26 18	17 10
Reserved	UDIMM	Reserved	NOSRA	Reserved	BYTEMASK
R=0x0	RW=0x0	R=0x0	RW=0x0	R=0x0	RW=0x1

9 8	7	6 4	3	2 0
Reserved	MPRDQ	PDQ	DDR8BNK	DDRMD
R=0x0	RW=0x0	RW=0x0	RW=0x1	RW=0x3

Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-50. DRAM Configuration Register (DCR) Field Descriptions

Bits	Name	Description
31-30	Reserved	Reset = 0x0 Reads return zeros.
29	UDIMM	Reset = 0x0 Un-buffered DIMM Address Mirroring: Indicates if set that there is address mirroring on the second rank of an un-buffered DIMM (the rank connected to CS1). DCR[NOSRA] must be set if address mirroring is enabled.
28	Reserved	Reset = 0x0 Reads return zeros.
27	NOSRA	Reset = 0x0 No Simultaneous Rank Access: Specifies if set that simultaneous rank access on the same clock cycle is not allowed. This means that multiple chip select signals will not be asserted at the same time. This bit must be set if address mirroring is enabled in DCR[UDIMM]. NOSRA should be set to 0 if address mirroring is enabled (for example, DCR[UDIMM]=1).
26-18	Reserved	Reset = 0x0 Reads return zeros.
17-10	BYTEMASK	Reset = 0x1 Byte Mask: Mask applied to all beats of read data on all bytes lanes during read DQS gate training. This allows training to be conducted based on selected bit(s) from the byte lanes. Valid values for each bit are: • 0 = Disable compare for that bit • 1 = Enable compare for that bit Note that this mask in DDR3 MPR operation mode as well and must be in keeping with the PDQ field setting. TI recommends that this field be always programmed to 0000 0001b.
9-8	Reserved	Reset = 0x0 Reads return zeros.
7	MPRDQ	Reset = 0x0 Multi-Purpose Register (MPR) DQ (DDR3 Only): Specifies the value that is driven on non-primary DQ pins during MPR reads. Valid values are: • 0 = Primary DQ drives out the data from MPR (0-1-0-1); non-primary DQs drive ‘0’ • 1 = Primary DQ and non-primary DQs all drive the same data from MPR (0-1-0-1) TI recommends that this bit be always programmed to 0.
6-4	PDQ	Reset = 0x0 Primary DQ (DDR3 Only): Specifies the DQ pin in a byte that is designated as a primary pin for Multi-Purpose Register (MPR) reads. Valid values are 0 to 7 for DQ[0] to DQ[7], respectively. TI recommends that this field be always programmed to 000b.
3	DDR8BNK	Reset = 0x1 DDR 8-Bank: Indicates if set that the SDRAM used has 8 banks.
2-0	DDRMD	Reset = 0x3 DDR Mode: Set to 0x3 for DDR3 mode.

4.49 DRAM Timing Parameters Register 0 (DTPR0)

DTPR0-2 are used to program timing parameters for different DDR3 speed grades. These timing parameters are in DRAM clock cycles and are derived from corresponding parameters in the SDRAM datasheet divided by the DRAM clock cycle time. Non-integer values should be rounded up to the next integer. All the default values correspond to the DDR3-2133 speed grade.

Figure 4-49. DRAM Timing Parameters Register 0 (DTPR0)

31 26	25 22	21 16	15 12	11 8	7 4	3 0
tRC	tRRD	tRAS	tRCD	tRP	tWTR	tRTP
RW=0x32	RW=0x7	RW=0x24	RW=0xE	RW=0xE	RW=0x8	RW=0x8

Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-51. DRAM Timing Parameters Register 0 (DTPR0) Field Descriptions

Bits	Name	Description
31-26	tRC	Reset = 0x32 Activate to activate command delay (same bank). Valid values are 2 to 63
25-22	tRRD	Reset = 0x7 Activate to activate command delay (different banks). Valid values are 1 to 15.
21-16	tRAS	Reset = 0x24 Activate to precharge command delay. Valid values are 2 to 63
15-12	tRCD	Reset = 0xE Activate to read or write delay. Minimum time from when an activate command is issued to when a read or write to the activated row can be issued. Valid values are 2 to 15.
11-8	tRP	Reset = 0xE Precharge command period: The minimum time between a precharge command and any other command. Valid values are 2 to 15.
7-4	tWTR	Reset = 0x8 Internal write to read command delay. Valid values are 1 to 15.
3-0	tRTP	Reset = 0x8 Internal read to precharge command delay. Valid values are 2 to 15.

4.50 DRAM Timing Parameters Register 1 (DTPR1)

DTPR0-2 are used to program timing parameters for different DDR3 speed grades. These timing parameters are in DRAM clock cycles and are derived from corresponding parameters in the SDRAM datasheet divided by the DRAM clock cycle time. Non-integer values should be rounded up to the next integer. All the default values correspond to the DDR3-2133 speed grade.

Figure 4-50. DRAM Timing Parameters Register 1 (DTPR1)

31 30	29 26	25 20	19 11	10 5	4 2	1 0
Reserved	tWLO	tWLMRD	tRFC	tFAW	tMOD	tMRD
R=0x0	RW=0x8	RW=0x28	RW=0x176	RW=0x26	RW=0x4	RW=0x2

Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-52. DRAM Timing Parameters Register 1 (DTPR1) Field Descriptions

Bits	Name	Description
31-30	Reserved	Reset = 0x0
29-26	tWLO	Reset = 0x8 Write leveling output delay: Number of clock cycles from when write leveling DQS is driven high by the PHY to when the results from the SDRAM on DQ is sampled by the PHY. This must include the SDRAM tWLO timing parameter plus the round trip delay from the DUT to SDRAM back to the DUT. TI recommends that this field always be programmed to 12 decimal.
25-20	tWLMRD	Reset = 0x28 Minimum delay from when write leveling mode is programmed to the first DQS/DQS# rising edge
19-11	tRFC	Reset = 0x176 Refresh-to-Refresh: Indicates the minimum time, in clock cycles, between two refresh commands or between a refresh and an active command. This is derived from the minimum refresh interval from the datasheet, tRFC(min), divided by the clock cycle time.
10-5	tFAW	Reset = 0x26 4-bank activate period. No more than 4-bank activate commands may be issued in a given tFAW period. Valid values are 2 to 63.
4-2	tMOD	Reset = 0x4 Load mode update delay. The minimum time between a load mode register command and a non-load mode register command. Valid values are: • 000 = 12 • 001 = 13 • 010 = 14 • 011 = 15 • 100 = 16 • 101 = 17 • 110 – 111 = Reserved
1-0	tMRD	Reset = 0x2 Load mode cycle time: The minimum time between a load mode register command and any other command. For DDR3 this is the minimum time between two load mode register commands. the value used for tMRD is 4 plus the value programmed in these bits, i.e. tMRD ranges from 4 to 7.

4.51 DRAM Timing Parameters Register 2 (DTPR2)

DTPR0-2 are used to program timing parameters for different DDR3 speed grades. These timing parameters are in DRAM clock cycles and are derived from corresponding parameters in the SDRAM datasheet divided by the DRAM clock cycle time. Non-integer values should be rounded up to the next integer. All the default values correspond to the DDR3-2133 speed grade.

Figure 4-51. DRAM Timing Parameters Register 2 (DTPR2)

31	30	29	28 19	18 15	14 10	9 0
tCCD	tRTW	tRTODT	tDLLK	tCKE	tXP	tXS
RW=0x0	RW=0x0	RW=0x0	RW=0x200	RW=0x6	RW=0x1A	RW=0x200

Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-53. DRAM Timing Parameters Register 2 (DTPR2) Field Descriptions

Bits	Name	Description
31	tCCD	Reset = 0x0 Read to read and write to write command delay. Valid values are: • 0 = 4 DRAM clock cycles • 1 = 5 DRAM clock cycles
30	tRTW	Reset = 0x0 Read to Write command delay. This parameter is only used when the PHY issues commands during initialization and leveling. During normal operation, the controller issues commands to the SDRAM and uses the timing parameters programmed in the controller. TI recommends that this bit be always set to 1 to provide additional margin during PHY initiated initialization/leveling.
29	tRTODT	Reset = 0x0 Read to ODT delay. This parameter is only used when the PHY issues commands during initialization and leveling. During normal operation, the controller issues commands to the SDRAM and uses the timing parameters programmed in the controller. TI recommends that this bit be always set to 0.
28-19	tDLLK	Reset = 0x200 DLL locking time. Valid values are 2 to 1023.
18-15	tCKE	Reset = 0x6 CKE minimum pulse width. Also specifies the minimum time that the SDRAM must remain in power down or self refresh mode. This parameter must be set to the value of tCKESR which is usually bigger than the value of tCKE. Valid values are 2 to 15.
14-10	tXP	Reset = 0x1A Power down exit delay. The minimum time between a power down exit command and any other command. This parameter must be set to the maximum of the various minimum power down exit delay parameters specified in the SDRAM datasheet, i.e. max(tXP, tXPDLL). Valid values are 2 to 31.
9-0	tXS	Reset = 0x200 Self refresh exit delay. The minimum time between a self refresh exit command and any other command. This parameter must be set to the maximum of the various minimum self refresh exit delay parameters specified in the SDRAM datasheet, i.e. (tXS, tXSDLL) for DDR3. Valid values are 2 to 1023.

4.52 Mode Register 0 (MR0)

SDRAM definitions controlled by the Mode Register 0 (MR0) include, among other things, burst length, burst type, CAS latency, operating mode, DLL reset, write recovery and power-down modes.

Figure 4-52. Mode Register 0 (MR0)

31	13	12	11	9	8
Reserved		PD	WR		DR
R=0x0		RW=0x0	RW=0x5		RW=0x0

7	6	4	3	2	1	0
TM	CL		BT	CL	BL	
RW=0x0	RW=0x5		RW=0x0	RW=0x5	RW=0x3	

Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-54. Mode Register 0 (MR0) Field Descriptions

Bits	Name	Description
31-16	Reserved	Reset = 0x0 Returns zeros on reads.
15-13	Reserved	Reset = 0x0 These are JEDEC reserved bits and are recommended by JEDEC to be programmed to ‘0’.
12	PD	Reset = 0x0 Power-Down Control: Controls the exit time for power-down modes. This must always be set to 1.
11-9	WR	Reset = 0x5 Write Recovery: This is the value of the write recovery in clock cycles. It is calculated by dividing the datasheet write recovery time, tWR (ns) by the datasheet clock cycle time, tCK (ns) and rounding up a non-integer value to the next integer. Valid values are: • 001 = 5 • 010 = 6 • 011 = 7 • 100 = 8 • 101 = 10 • 110 = 12 • 111 = 14 • 000 = 16 All other settings are reserved and should not be used.
8	DR	Reset = 0x0 DLL Reset: Writing a ‘1’ to this bit will reset the SDRAM DLL. This bit is self-clearing, i.e. it returns back to ‘0’ after the DLL reset has been issued.
7	TM	Reset = 0x0 Operating Mode: Always set to 0 for normal operating mode.
6-4,2	CL	Reset = 0xA CAS Latency: The delay, in clock cycles, between when the SDRAM registers a read command to when data is available. Valid values are: • 0010 = 5 • 0100 = 6 • 0110 = 7 • 1000 = 8 • 1010 = 9 • 1100 = 10 • 1110 = 11 • 0001 = 12 • 0011 = 13 • 0101 = 14 All other settings are reserved and should not be used.

Table 4-54. Mode Register 0 (MR0) Field Descriptions (continued)

Bits	Name	Description
3	BT	Reset = 0x0 Burst type: Set to 0 for sequential burst (interleaved burst is not supported)
1-0	BL	Reset = 0x0 Burst Length: Determines the maximum number of column locations that can be accessed during a given read or write command. Set to 0 for a fixed burst length of 8 (other burst lengths are not supported)

4.53 Mode Register 1 (MR1)

SDRAM definitions controlled by the Mode register 1 (MR1) include, among other things, DLL enable/disable, drive strength, on-die termination (ODT) resistance, CAS additive latency, off-chip driver (OCD) impedance calibration and output enable.

Figure 4-53. Mode Register 1 (MR1)

31	13	12	11	10	9	8	7
Reserved		QOFF	TDQS	Reserved	RTT	Reserved	LEVEL
R=0x0		RW=0x0	RW=0x0	R=0x0	RW=0x0	R=0x0	RW=0x0

6	5	4	3	2	1	0
RTT	DIC	AL		RTT	DIC	DE
RW=0x0	RW=0x0	RW=0x0		RW=0x0	RW=0x0	RW=0x0

Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-55. Mode Register 1 (MR1) Field Descriptions

Bits	Name	Description
31-16	Reserved	Reset = 0x0 Returns zeros on reads.
15-13	Reserved	Reset = 0x0 These are JEDEC reserved bits and are recommended by JEDEC to be programmed to ‘0’.
12	QOFF	Reset = 0x0 Output Enable/Disable: Program to ‘0’ for all outputs to function as normal.
11	TDQS	Reset = 0x0 Termination Data Strobe: This must always be set to 0.
10	Reserved	Reset = 0x0 Reserved. This is a JEDEC reserved bit for DDR3 and is recommended by JEDEC to be programmed to ‘0’.
9	RTT	Reset = 0x0 On Die Termination: Selects the effective resistance for SDRAM on die termination. Valid values are: • 000 = ODT disabled • 001 = RZQ/4 • 010 = RZQ/2 • 011 = RZQ/6 • 100 = RZQ/12 • 101 = RZQ/8 All other settings are reserved and should not be used
8	Reserved	Reset = 0x0 Reserved. This is a JEDEC reserved bit for DDR3 and is recommended by JEDEC to be programmed to ‘0’.
7	LEVEL	Reset = 0x0 Write Leveling Enable: Enables write-leveling when set.
6	RTT	Reset = 0x0 On Die Termination: Selects the effective resistance for SDRAM on die termination. Valid values are: • 000 = ODT disabled • 001 = RZQ/4 • 010 = RZQ/2 • 011 = RZQ/6 • 100 = RZQ/12 • 101 = RZQ/8 All other settings are reserved and should not be used
5	DIC	Reset = 0x0 Output Driver Impedance Control: Controls the output drive strength. Valid values are: • 00 = Reserved for RZQ/6 • 01 = RZQ7 • 10 = Reserved • 11 = Reserved

Table 4-55. Mode Register 1 (MR1) Field Descriptions (continued)

Bits	Name	Description
4-3	AL	Reset = 0x0 Posted CAS Additive Latency: the controller does not support this feature. This must always be set to 0.
2	RTT	Reset = 0x0 On Die Termination: Selects the effective resistance for SDRAM on die termination. Valid values are: • 000 = ODT disabled • 001 = RZQ/4 • 010 = RZQ/2 • 011 = RZQ/6 • 100 = RZQ/12 • 101 = RZQ/8 All other settings are reserved and should not be used
1	DIC	Reset = 0x0 Output Driver Impedance Control: Controls the output drive strength. Valid values are: • 00 = Reserved for RZQ/6 • 01 = RZQ7 • 10 = Reserved • 11 = Reserved
0	DE	Reset = 0x0 DLL Enable/Disable: Enable (0) or disable (1) the DLL. DLL must be enabled for normal operation.

4.54 Mode Register 2 (MR2)

Mode Register 2 controls (among other things) refresh related features of SDRAMs, and is described in the figure and table below.

Figure 4-54. Mode Register 2 (MR2)

31 11	10 9	8	7	6	5 3	2 0
Reserved	RTTWR	Reserved	SRT	ASR	CWL	PASR
R=0x0	RW=0x0	R=0x0	RW=0x0	RW=0x0	RW=0x0	RW=0x0

Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-56. Mode Register 2 (MR2) Field Descriptions

Bits	Name	Description
31-16	Reserved	Reset = 0x0 Returns zeros on reads.
15-11	Reserved	Reset = 0x0 These are JEDEC reserved bits and are recommended by JEDEC to be programmed to ‘0’.
10-9	RTTWR	Reset = 0x0 Dynamic ODT: Selects RTT for dynamic ODT. Valid values are: • 00 = Dynamic ODT off • 01 = RZQ/4 • 10 = RZQ/2 • 11 = Reserved
8	Reserved	Reset = 0x0 These are JEDEC reserved bits and are recommended by JEDEC to be programmed to ‘0’.
7	SRT	Reset = 0x0 Self-Refresh Temperature Range: Selects either normal (‘0’) or extended (‘1’) operating temperature range during self-refresh.
6	ASR	Reset = 0x0 Auto Self-Refresh: When enabled (‘1’), SDRAM automatically provides self-refresh power management functions for all supported operating temperature values. Otherwise the SRT bit must be programmed to indicate the temperature range.
5-3	CWL	Reset = 0x0 CAS Write Latency: The delay, in clock cycles, between when the SDRAM registers a write command to when write data is available. Valid values are: • 000 = 5 (tCK > 2.5ns) • 001 = 6 (2.5ns > tCK > 1.875ns) • 010 = 7 (1.875ns > tCK> 1.5ns) • 011 = 8 (1.5ns > tCK > 1.25ns) • 100 = 9 (1.25ns > tCK > 1.07ns) • 101 = 10 (1.07ns > tCK > 0.935ns) • 110 = 11 (0.935ns > tCK > 0.833ns) • 111 = 12 (0.833ns > tCK > 0.75ns) All other settings are reserved and should not be used
2-0	PASR	Reset = 0x0 Partial Array Self Refresh: Specifies that data located in areas of the array beyond the specified location will be lost if self refresh is entered. • 000 = Full Array • 001 = Half Array (BA[2:0] = 000, 001, 010 & 011) • 010 = Quarter Array (BA[2:0] = 000, 001) • 011 = 1/8 Array (BA[2:0] = 000) • 100 = 3/4 Array (BA[2:0] = 010, 011, 100, 101, 110 & 111) • 101 = Half Array (BA[2:0] = 100, 101, 110 & 111) • 110 = Quarter Array (BA[2:0] = 110 & 111) • 111 = 1/8 Array (BA[2:0] 111)

4.55 Mode Register 3 (MR3)

Mode Register 3 controls (among other things) the multi-purpose register, and is described in the figure and table below.

Figure 4-55. Mode Register 3 (MR3)

31	3	2	1	0
Reserved		MPR	MPRLOC	
R=0x0		RW=0x0	RW=0x0	

Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-57. Mode Register 3 (MR3) Field Descriptions

Bits	Name	Description
31-16	Reserved	Reset = 0x0 Returns zeros on reads.
15-3	Reserved	Reset = 0x0 These are JEDEC reserved bits and are recommended by JEDEC to be programmed to '0'.
2	MPR	Reset = 0x0 Multi-Purpose Register Enable: Enables, if set, that read data should come from the Multi-Purpose Register. Otherwise read data come from the DRAM array.
1-0	MPRLOC	Reset = 0x0 Multi-Purpose Register (MPR) Location: Selects MPR data location: Valid value are: • 00 = Predefined pattern for system calibration • All other settings are reserved and should not be used.

4.56 ODT Configuration Register (ODTCR)

This register configures how ODT should be controlled on the different ranks when writing or reading a particular rank. This provides full flexibility on how the overall termination of the SDRAM system is set depending on how many ranks are used and whether the DIMM slots are occupied or not.

For example, assume the system is a 2-rank configuration and during Read commands the user wishes to always enable the ODT on the SDRAM which is not providing the Read data. In this case, the user would write “0010” to RDODT0 and “0001” to RDODT1.

Figure 4-56. ODT Configuration Register (ODTCR)

31 28	27 24	23 20	19 16	15 12	11 8	7 4	3 0
WRODT3	WRODT2	WRODT1	WRODT0	RDODT3	RDODT2	RDODT1	RDODT0
RW=0x8	RW=0x4	RW=0x2	RW=0x1	RW=0x0	RW=0x0	RW=0x0	RW=0x0

Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-58. ODT Configuration Register (ODTCR) Field Descriptions

Bits	Name	Description
31-28	WRODT3	Reset = 0x8, 0x4, 0x2, 0x1 (WRODT3 - 0) Write ODT: Specifies whether ODT should be enabled (‘1’) or disabled (‘0’) on each of the up to four ranks when a write command is sent to rank n. WRODT0, WRODT1, WRODT2, and WRODT3 specify ODT settings when a write is to rank 0, rank 1, rank 2, and rank 3, respectively. The four bits of each field each represent a rank, the LSB being rank 0 and the MSB being rank 3. Default is to enable ODT only on rank being written to
27-4	WRODT2	See description for WRODT3.
23-20	WRODT1	See description for WRODT3.
19-16	WRODT0	See description for WRODT3.
15-12	RDODT3	Reset = All are 0x0 Read ODT: Specifies whether ODT should be enabled (‘1’) or disabled (‘0’) on each of the up to four ranks when a read command is sent to rank n. RDODT0, RDODT1, RDODT2, and RDODT3 specify ODT settings when a read is to rank 0, rank 1, rank 2, and rank 3, respectively. The four bits of each field each represent a rank, the LSB being rank 0 and the MSB being rank 3. Default is to disable ODT during reads.
11-8	RDODT2	See description for RDODT3.
7-4	RDODT1	See description for RDODT3.
3-0	RDODT0	See description for RDODT3.

4.57 Data Training Configuration Register (DTCR)

The DTCR register is used to set various configurations for data training, and is described in the figure and register below.

Figure 4-57. Data Training Configuration Register (DTCR)

31 28	27 24	23	22	21	20	19 16	15 14
RFSHDT	RANKEN	Reserved	DTEXD	DTDSTP	DTDEN	DTDBS	Reserved
RW=0x9	RW=0xF	R=0x0	RW=0x0	RW=0x0	RW=0x0	RW=0x0	R=0x0
13	12	11 8	7	6	5 4	3 0	
DTBDC	DTWBDDM	DTWDQM	DTCMPD	DTMPR	DTRANK	DTRPTN	
RW=0x1	RW=0x1	RW=0x5	RW=0x1	RW=0x0	RW=0x0	RW=0x7	

Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-59. Data Training Configuration Register (DTCR) Field Descriptions

Bits	Name	Description
31-28	RFSHDT	Reset = 0x9 Refresh During Training: A non-zero value specifies that a burst of refreshes equal to the number specified in this field should be sent to the SDRAM after training each rank except the last rank
27-24	RANKEN	Reset = 0xF Rank Enable: Specifies the ranks that are enabled for data-training. Bit 0 controls rank 0, bit 1 controls rank 1, bit 2 controls rank 2, and bit 3 controls rank 3. Setting the bit to '1' enables the rank, and setting it to '0' disables the rank.
23	Reserved	Reset = 0x0
22	DTEXD	Reset = 0x0 Data Training Extended Write DQS: Enables, if set, an extended write DQS whereby two additional pulses of DQS are added as post-amble to a burst of writes. Generally this should only be enabled when running read bit deskew with the intention of performing read eye deskew prior to running write leveling adjustment
21	DTDSTP	Reset = 0x0 Data Training Debug Step: A write of 1 to this bit steps the data training algorithm through a single step. This bit is self-clearing
20	DTDEN	Reset = 0x0 Data Training Debug Enable: Enables, if set, the data training debug mode
19-16	DTDBS	Reset = 0x0 Data Training Debug Byte Select: Selects the byte during data training debug mod
15-14	Reserved	Reset = 0x0 Returns zeros on reads.
13	DTBDC	Reset = 0x1 Data Training Bit Deskew Centering: Enables, if set, eye centering capability during write and read bit deskew training.
12	DTWBDDM	Reset = 0x1 Data Training Write Bit Deskew Data Mask. If set it enables write bit deskew of the data mask
11-8	DTWDQM	Reset = 0x5 Training WDQ Margin: Defines how close to 0 or how close to 2*(wdq calibration_value) the WDQ lcdl can be moved during training. Basically defines how much timing margin.
7	DTCMPD	Reset = 0x1 Data Training Compare Data: Specifies, if set, that DQS gate training should also check if the returning read data is correct. Otherwise data-training only checks if the correct number of DQS edges were returned.
6	DTMPR	Reset = 0x0 Data Training Using MPR (DDR3 Only): Specifies, if set, that DQS gate training should use the SDRAM Multi-Purpose Register (MPR) register. Otherwise data training is performed by first writing to some locations in the SDRAM and then reading them back.
5-4	DTRANK	Reset = 0x0 Data Training Rank: Selects the SDRAM rank to be used during data bit deskew and eye centering
3-0	DTRPTN	Reset = 0x7 Data Training Repeat Number: Repeat number used to confirm stability of DDR write or read

4.58 Impedance Control Register 0 (ZQnCR0)

ZQnCR0-1 (n=0 to 3) registers are used for impedance control and calibration to enable the programmable and PVTcompensated on-die termination (ODT) and output impedance of the functional SSTL cells. The following figure and table describe the bits of the ZQnCR0 register.

Figure 4-58. Impedance Control Register 0 (ZQnCR0)

31	30	29	28	27 0
ZQPD	ZCALEN	ZCALBYP	ZDEN	ZDATA
RW=0x0	RW=0x1	RW=0x0	RW=0x0	RW=0x014A

Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-60. Impedance Control Register 0 (ZQnCR0) Field Descriptions

Bits	Name	Description
31	ZQPD	Reset = 0x0 ZQ Power Down: Powers down, if set, the impedance control block.
30	ZCALEN	Reset = 0x1 Impedance Calibration Enable: Enables if set the impedance calibration of the ZQn control block when impedance calibration is triggered using either the ZCAL bit of PIR register or the DFI update interface.
29	ZCALBYP	Reset = 0x0 Impedance Calibration Bypass: Bypasses, if set, impedance calibration of the ZQn control block when impedance calibration is already in progress. Impedance calibration can be disabled prior to trigger by using the ZCALEN bit.
28	ZDEN	Reset = 0x0 Impedance Over-ride Enable: When this bit is set, it allows users to directly drive the impedance control using the data programmed in the ZDATA field. Otherwise, the control is generated automatically by the impedance control logic
27-0	ZDATA	Reset = 0x014A Impedance Over-Ride Data: Data used to directly drive the impedance control. ZDATA field mapping is as follows: • ZDATA[27:21] is used to select the pull-up on-die termination impedance • ZDATA[20:14] is used to select the pull-down on-die termination impedance • ZDATA[13:7] is used to select the pull-up output impedance • ZDATA[6:0] is used to select the pull-down output impedance

4.59 Impedance Control Register 1 (ZQnCR1)

ZQnCR0-1 (n=0 to 3) registers are used for impedance control and calibration to enable the programmable and PVTcompensated on-die termination (ODT) and output impedance of the functional SSTL cells. The following figure and table describe the bits of the ZQnCR1 register.

Figure 4-59. Impedance Control Register 1 (ZQnCR1)

31	17	16	15	8	7	0
Reserved		DFIPU0	Reserved		ZPROG	
R=0x0 00010		R=0x0	R=0x0 00010		RW=0 x7B	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-61. Impedance Control Register 1 (ZQnCR1) Field Descriptions

Bits	Name	Description
31-17	Reserved	Reset = 0x0 Returns zeros on reads.
16	DFIPU0	Impedance Calibration Enable: Setting to 1 enables the PHY to request periodic updates to compensate for VT drifts that might result in decreased timing margin. TI recommends this be set to 1. Note that this bit is supported only on K2H Rev2.0, K2K Rev 2.0 and all revisions of K2E and K2L families. It is not supported on K2H Rev 1.x or K2K Rev1.x.
15-8	Reserved	Reset = 0x0 Returns zeros on reads.
7-0	ZPROG	Reset = 0x7B Impedance Divide Ratio: Selects the external resistor divide ratio to be used to set the output impedance and the on-die termination as follows: • ZPROG[7:4] = On-die termination divide select. Available values are: – 2 decimal – 120 ohms – 5 decimal – 60 ohms – 8 decimal – 40 ohms • ZPROG[3:0] = Output impedance divide select. Available values are: – 11 decimal – 40 ohms – 13 decimal – 34 ohms

4.60 Impedance Status Register 0 (ZQnSR0)

ZQnSR0-1 (n=0 to 3) registers are used to provide the status for impedance control and calibration to enable the programmable and PVT-compensated on-die termination (ODT) and output impedance of the functional SSTL cells. The following figure and table describe the bits of the ZQnSR0 register.

Figure 4-60. Impedance Status Register 0 (ZQnSR0)

31	30	29 28	27 0
ZDONE	ZERR	Reserved	ZCTRL
R=0x0	R=0x0	R=0x0	R=0x000014A

Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-62. Impedance Status Register 0 (ZQnSR0) Field Descriptions

Bits	Name	Description
31	ZDONE	Reset = 0x0 Impedance Calibration Done: Indicates that impedance calibration has completed.
30	ZERR	Reset = 0x0 Impedance Calibration Error: If set, indicates that there was an error during impedance calibration.
29-28	Reserved	Reset = 0x0 Returns zeros on reads.
27-0	ZCTRL	Reset = 0x000014A Impedance Control: Current value of impedance control. ZCTRL field mapping is as follows: • ZCTRL[27:21] is used to select the pull-up on-die termination impedance • ZCTRL[20:14] is used to select the pull-down on-die termination impedance • ZCTRL[13:7] is used to select the pull-up output impedance • ZCTRL[6:0] is used to select the pull-down output impedance

4.61 Impedance Status Register 1 (ZQnSR1)

ZQnSR0-1 (n=0 to 3) registers are used to provide the status for impedance control and calibration to enable the programmable and PVT-compensated on-die termination (ODT) and output impedance of the functional SSTL cells. The following figure and table describe the bits of the ZQnSR1 register.

Figure 4-61. Impedance Status Register 1 (ZQnSR1)

31 8	7 6	5 4	3 2	1 0
Reserved	OPU	OPD	ZPU	ZPD
R=0x0	R=0x0	R=0x0	R=0x0	R=0x0

Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-63. Impedance Status Register 1 (ZQnSR1) Field Descriptions

Bits	Name	Description
31-8	Reserved	Reset = 0x0 Returns zeros on reads.
7-6	OPU	Reset = 0x0 On-die termination (ODT) pull-up calibration status. Similar status encodings as ZPD.
5-4	OPD	Reset = 0x0 On-die termination (ODT) pull-down calibration status. Similar status encodings as ZPD.
3-2	ZPU	Reset = 0x0 Output impedance pull-up calibration status. Similar status encodings as ZPD.
1-0	ZPD	Reset = 0x0 Output impedance pull-down calibration status. Valid status encodings are: • 00 = Completed with no errors • 01 = Overflow error • 10 = Underflow error • 11 = Calibration in progress

4.62 DATX8 General Configuration Register (DXnGCR)

This register is used for miscellaneous configurations specific to a particular instantiation of the DATX8 macro (n=0 to 8).

Figure 4-62. DATX8 General Configuration Register (DXnGCR)

31	30	29 26	25 20	19	18
CALBYP	MDLEN	WLRNKEN	Reserved	PLLBYP	GSHIFT
RW=0x0	RW=0x1	RW=0xF	R=0x0	RW=0x0	RW=0x0

17	16	15 14	13	12 11	10	9
PLLPD	PLLRST	DXOEO	RTTOAL	RTTOH	DQRTT	DQSRTT
RW=0x0	RW=0x0	RW=0x0	RW=0x0	RW=0x1	RW=0x1	RW=0x1

8 7	6 5	4	3	2	1	0
DSEN	DQSRPD	DXPDR	DXPDD	DXIOM	DQODT	DQSODT	DXEN
RW=0x1	RW=0x0	RW=0x0	RW=0x0	RW=0x0	RW=0x0	RW=0x0	RW=0x1

Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-64. DATX8 General Configuration Register (DXnGCR) Field Descriptions

Bits	Name	Description
31	CALBYP	Reset = 0x0 Calibration Bypass: Prevents, if set, period measurement calibration from automatically triggering after PHY initialization.
30	MDLEN	Reset = 0x1 Master Delay Line Enable: Enables, if set, the DATX8 master delay line calibration to perform subsequent period measurements following the initial period measurements that are performed after reset or when calibration is manually triggered. These additional measurements are accumulated and filtered as long as this bit remains high. This bit is ANDed with the common DATX8 MDL enable bit.
29-26	WLRNKEN	Reset = 0xF Write Level Rank Enable: Specifies the ranks that should be write leveled for this byte. Write leveling responses from ranks that are not enabled for write leveling for a particular byte are ignored and write leveling is flagged as done for these ranks. WLRKEN[0] enables rank 0, [1] enables rank 1, [2] enables rank 2, and [3] enables rank 3.
25-20	Reserved	Reset = 0x0 Reads return zeros
19	PLLBYP	Reset = 0x0 PLL Bypass: Puts the byte PLL in bypass mode by driving the PLL bypass pin. This bit is not self-clearing and a '0' must be written to de-assert the bypass. This bit is ORed with the global BYP configuration bit in PLLCR
18	GSHIFT	Reset = 0x0 Gear Shift: Enables, if set, rapid locking mode on the byte PLL
17	PLLPD	Reset = 0x0 PLL Power Down: Puts the byte PLL in power down mode by driving the PLL power down pin. This bit is not self-clearing and a '0' must be written to de-assert the power-down. This bit is ORed with the global PLLPD configuration bit in PLLCR
16	PLLRST	Reset = 0x0 PLL Rest: Resets the byte PLL by driving the PLL reset pin. This bit is not selfclearing and a '0' must be written to de-assert the reset. This bit is ORed with the global PLLRST configuration bit in PLLCR
15-14	DXOEO	Reset = 0x0 Data Byte Output Enable Override: Specifies whether the output I/O output enable for the byte lane should be set to a fixed value. Valid values are: • 00 = No override. Output enable is controlled by DFI transactions • 01 = Ouput enable is asserted (I/O is forced to output mode). • 10 = Output enable is de-asserted (I/O is forced to input mode) • 11 = Reserved
13	RTTOAL	Reset = 0x0 RTT On Additive Latency: Indicates when the ODT control of DQ/DQS SSTL I/Os is set to the value in DQODT/DQSODT during read cycles. Valid values are: • 0 = ODT control is set to DQSODT/DQODT almost two cycles before read data preamble • 1 = ODT control is set to DQSODT/DQODT almost one cycle before read data preamble

Table 4-64. DATX8 General Configuration Register (DXnGCR) Field Descriptions (continued)

Bits	Name	Description
12-11	RTTOH	Reset = 0x1 RTT Output Hold: Indicates the number of clock cycles (from 0 to 3) after the read data postamble for which ODT control should remain set to DQSODT for DQS or DQODT for DQ/DM before disabling it (setting it to '0') when using dynamic ODT control. ODT is disabled almost RTTOH clock cycles after the read postamble
10	DQRTT	Reset = 0x1 DQ Dynamic RTT Control: Indicates, if set, that the ODT control of DQ/DM SSTL I/Os be dynamically controlled by setting it to the value in DQODT during reads and disabling it (setting it to '0') during any other cycle. If this bit is not set, then the ODT control of DQ SSTL I/Os is always set to the value in DQODT.
9	DQSRTT	Reset = 0x1 DQS Dynamic RTT Control: Indicates, if set, that the ODT control of DQS SSTL I/Os be dynamically controlled by setting it to the value in DQSODT during reads and disabling it (setting it to '0') during any other cycle. If this bit is not set, then the ODT control of DQS SSTL I/Os is always set to the value in DQSODT field
8-7	DSEN	Reset = 0x1 Write DQS Enable: Controls whether the write DQS going to the SDRAM is enabled (toggling) or disabled (static value) and whether the DQS is inverted. DQS# is always the inversion of DQS. These values are valid only when DQS/DQS# output enable is on, otherwise the DQS/DQS# is tri-stated. Valid settings are: • 00 = DQS disabled (Driven to constant 0) • 01 = DQS toggling with normal polarity (This should be the default setting) • 10 = DQS toggling with inverted polarity • 11 = DQS disabled (Driven to constant 1)
6	DQSRPD	Reset = 0x0 DQSR Power Down: Powers down, if set, the PDQSR cell.
5	DXPDR	Reset = 0x0 Data Power Down Receiver: Powers down, when set, the input receiver on I/O for DQ, DM, and DQS/DQS# pins of the byte.
4	DXPDD	Reset = 0x0 Data Power Down Driver: Powers down, when set, the output driver on I/O for DQ, DM, and DQS/DQS# pins of the byte.
3	DXIOM	Reset = 0x0 Data I/O Mode: Selects SSTL mode (when set to 0) or CMOS mode (when set to 1) of the I/O for DQ, DM, and DQS/DQS# pins of the byte.
2	DQODT	Reset = 0x0 Data On-Die Termination: Enables, when set, the on-die termination on the I/O for DQ and DM pins of the byte.
1	DQSODT	Reset = 0x0 DQS On-Die Termination: Enables, when set, the on-die termination on the I/O for DQS/DQS# pin of the byte
0	DXEN	Reset = 0x1 Data Byte Enable: Enables if set the data byte. Setting this bit to '0' disables the byte, i.e. the byte is not used in PHY initialization or training and is ignored during SDRAM read/write operations. Note: Software-initiated PHY initialization and leveling is only required after ECC has been enabled in the PHY by writing to DX8GCR.DXEN. Once ECC is enabled in the PHY and the PHY is initialized and leveled, the ECC enable bit in the controller (ECCCTL.ECC_EN) can be enabled or disabled without re-triggering PHY initialization and leveling.

4.63 DATX8 General Status Register 0 (DXnGSR0)

DXnGSR0-2 are general status registers for the DATX8 (n=0 to 8). They indicate among other things whether write leveling or period measurement calibration is done. Note that WDQCAL, RDQSCAL, RDQSNCAL, GDQSCAL, and WLCAL are calibration measurement-done flags that should be used for debug purposes if the global calibration done flag (PGSR0[CAL]) is not asserted. These flags will typically assert for a minimum of two configuration clock cycles and then de-assert when all measurement done flags are asserted.

Figure 4-63. DATX8 General Status Register 0 (DXnGSR0)

31 29	28	27 24	23 16	15
Reserved	WLDQ	QSGERR	GDQSPRD	DPLOCK
R=0x0	R=0x0	R=0x0	R=0x0	R=0x0

14 7	6	5	4	3	2	1	0
WLPRD	WLERR	WLDONE	WLCAL	GDQSCAL	RDQSNCAL	RDQSCAL	WDQCAL
R=0x0	R=0x0	R=0x0	R=0x0	R=0x0	R=0x0	R=0x0	R=0x0

Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-65. DATX8 General Status Register 0 (DXnGSR0) Field Descriptions

Bits	Name	Description
31-29	Reserved	Reset = 0x0 Reads return zeros.
28	WLDQ	Reset = 0x0 Write Leveling DQ Status: Captures the write leveling DQ status from the DRAM during software write leveling
27-24	QSGERR	Reset = 0x0 DQS Gate Training Error: Indicates if set that there is an error in DQS gate training. One bit for each of the up to 4 ranks
23-16	GDQSPRD	Reset = 0x0 Read DQS gating Period: Returns the DDR clock period measured by the read DQS gating LCDL during calibration. This value is PVT compensated
15	DPLOCK	Reset = 0x0 DATX8 PLL Lock: Indicates, if set, that the DATX8 PLL has locked.
14-7	WLPRD	Reset = 0x0 Write Leveling Period: Returns the DDR clock period measured by the write leveling LCDL during calibration. The measured period is used to generate the control of the write leveling pipeline which is a function of the write-leveling delay and the clock period. This value is PVT compensated
6	WLERR	Reset = 0x0 Write Leveling Error: Indicates, if set, that there is a write leveling error in the DATX8.
5	WLDONE	Reset = 0x0 Write Leveling Done: Indicates, if set, that the DATX8 has completed write leveling.
4	WLCAL	Reset = 0x0 Write Leveling Calibration: Indicates, if set, that the DATX8 has finished doing period measurement calibration for the write leveling slave delay line
3	GDQSCAL	Reset = 0x0 Read DQS gating Calibration: Indicates, if set, that the DATX8 has finished doing period measurement calibration for the read DQS gating LCDL.
2	RDQSNCAL	Reset = 0x0 Read DQS# Calibration (Type B/B1 PHY Only): Indicates, if set, that the DATX8 has finished doing period measurement calibration for the read DQS# LCDL
1	RDQSCAL	Reset = 0x0 Read DQS Calibration: Indicates, if set, that the DATX8 has finished doing period measurement calibration for the read DQS LCDL.
0	WDQCAL	Reset = 0x0 Write DQ Calibration: Indicates, if set, that the DATX8 has finished doing period measurement calibration for the write DQ LCDL.

4.64 DATX8 General Status Register 2 (DXnGSR2)

DXnGSR0-2 are general status registers for the DATX8 (n=0 to 8). They indicate among other things whether write leveling or period measurement calibration is done. Note that WDQCAL, RDQSCAL, RDQSNCAL, GDQSCAL, and WLCAL are calibration measurement-done flags that should be used for debug purposes if the global calibration done flag (PGSR0[CAL]) is not asserted. These flags will typically assert for a minimum of two configuration clock cycles and then de-assert when all measurement done flags are asserted.

Figure 4-64. DATX8 General Status Register 2 (DXnGSR2)

31 12	11 8	7	6	5
Reserved	ESTAT	WEWN	WEERR	REWN
R=0x0	R=0x0	R=0x0	R=0x0	R=0x0
4	3	2	1	0
REERR	WDWN	WDERR	RDWN	RDERR
R=0x0	R=0x0	R=0x0	R=0x0	R=0x0

Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-66. DATX8 General Status Register 2 (DXnGSR2) Field Descriptions

Bits	Name	Description
31-12	Reserved	Reset = 0x0 Reads return zeros.
11-8	ESTAT	Reset = 0x0 Error Status: If an error occurred for this lane as indicated by RDERR, WDERR, REERR or WEERR the error status code can provide additional information regard when the error occurred during the algorithm execution.
7	WEWN	Reset = 0x0 Write Eye Centering Warning: Indicates, if set, that the byte lane *n* has encountered a warning during execution of the write eye centering training.
6	WEERR	Reset = 0x0 Write Eye Centering Error: Indicates, if set, that the byte lane *n* has encountered an error during execution of the write eye centering training.
5	REWN	Reset = 0x0 Read Eye Centering Warning: Indicates, if set, that the byte lane *n* has encountered a warning during execution of the read eye centering training.
4	REERR	Reset = 0x0 Read Eye Centering Error: Indicates, if set, that the byte lane *n* has encountered an error during execution of the read eye centering training.
3	WDWN	Reset = 0x0 Write Bit Deskew Warning: Indicates, if set, that the byte lane *n* has encountered a warning during execution of the write bit deskew training.
2	WDERR	Reset = 0x0 Write Bit Deskew Error: Indicates, if set, that the byte lane *n* has encountered an error during execution of the write bit deskew training.
1	RDWN	Reset = 0x0 Read Bit Deskew Warning: Indicates, if set, that the byte lane *n* has encountered a warning during execution of the read bit deskew training.
0	RDERR	Reset = 0x0 Read Bit Deskew Error: Indicates, if set, that the byte lane *n* has encountered an error during execution of the read bit deskew training.

4.65 DATX8 Local Calibrated Delay Line Register 0 (DXnLCDLR0)

The DATX8 local calibrated delay line registers 0-2 (n=0 to 8) are used to select the delay value on the LCDLs used in the DATX8 macros. A single LCDL field in the LCDLR register connects to a corresponding LCDL. The following tables describe the bits of the DATX8 LCDLR registers. The write data delay (WDQD) and the read DQS delay (RDQSD) are automatically derived from the measured period during calibration. WDQD and RDQSD correspond to a 90 degrees phase shift for DQ during writes and DQS during reads, respectively. The 90 degrees phase shift is used to centre DQS into the write and read data eyes. A 90 degrees phase shift is equivalent to half the DDR clock period. After calibration WDQD and RDQSD fields will contain a value that corresponds to half the DDR clock period (or a quarter of the SDRAM clock period). The write leveling delay (RnWLD) and read DQS gating delay DQSGD are derived from the write leveling and DQS training algorithms. These are normally run automatically by the PHY control block or they can be executed in software by the user. After calibration RnWLD field will contain a value that corresponds to the DDR clock period (or half of the SDRAM clock period), while RnDQSGD field will contain a value that corresponds to half the DDR clock period (or a quarter of the SDRAM clock period).

After the initial setting, all LCDL register fields are automatically updated by the VT compensation logic to track drifts due to voltage and temperature. The user can however override these values by writing to the respective fields of the register and/or optionally disabling the automatic drift compensation.

Figure 4-65. DATX8 Local Calibrated Delay Line Register 0 (DXnLCDLR0)

31 24	23 16	15 8	7 0
R3WLD	R2WLD	R1WLD	R0WLD
RW=0x0	RW=0x0	RW=0x0	RW=0x0

Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-67. DATX8 Local Calibrated Delay Line Register 0 (DXnLCDLR0) Field Descriptions

Bits	Name	Description
31-24	R3WLD	Reset = 0x0 Rank 3 Write Leveling Delay: Rank 3 delay select for the write leveling (WL) LCDL
23-16	R2WLD	Reset = 0x0 Rank 2 Write Leveling Delay: Rank 2 delay select for the write leveling (WL) LCDL
15-8	R1WLD	Reset = 0x0 Rank 1 Write Leveling Delay: Rank 1 delay select for the write leveling (WL) LCDL
7-0	R0WLD	Reset = 0x0 Rank 0 Write Leveling Delay: Rank 0 delay select for the write leveling (WL) LCDL

4.66 DATX8 Local Calibrated Delay Line Register 1 (DXnLCDLR1)

The DXnLCDLR1 register is described in the figure and table below.

Figure 4-66. DATX8 Local Calibrated Delay Line Register 1 (DXnLCDLR1)

31 24	23 16	15 8	7 0
Reserved	RDQSND	RDQSD	WDQD
R=0x0	RW=0x0	RW=0x0	RW=0x0

Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-68. DATX8 Local Calibrated Delay Line Register 1 (DXnLCDLR1) Field Descriptions

Bits	Name	Description
31-24	Reserved	Reset = 0x0 Reads return zeros
23-16	RDQSND	Reset = 0x0 Read DQSN Delay: Delay select for the read DQSN (RDQS) LCDL
15-8	RDQSD	Reset = 0x0 Read DQS Delay: Delay select for the read DQS (RDQS) LCDL
7-0	WDQD	Reset = 0x0 Write Data Delay: Delay select for the write data (WDQ) LCDL.

4.67 DATX8 Local Calibrated Delay Line Register 2 (DXnLCDLR2)

The DXnLCDLR2 register is described in the figure and table below.

Figure 4-67. DATX8 Local Calibrated Delay Line Register 2 (DXnLCDLR2)

31 24	23 16	15 8	7 0
R3DQSGD	R2DQSGD	R1DQSGD	R0DQSGD
RW=0x0	RW=0x0	RW=0x0	RW=0x0

Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

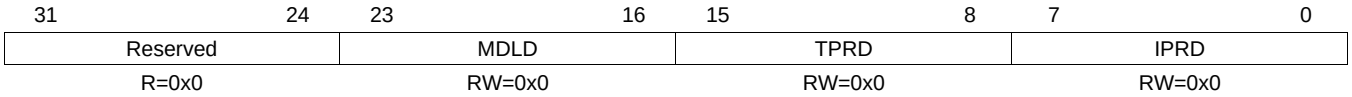
Table 4-69. DATX8 Local Calibrated Delay Line Register 2 (DXnLCDLR2) Field Descriptions

Bits	Name	Description
31-24	R3DQSGD	Reset = 0x0 Rank 3 Read DQS Gating Delay: Rank 3 delay select for the read DQS gating (DQSG) LCDL.
23-16	R2DQSGD	Reset = 0x0 Rank 2 Read DQS Gating Delay: Rank 2 delay select for the read DQS gating (DQSG) LCDL.
15-8	R1DQSGD	Reset = 0x0 Rank 1 Read DQS Gating Delay: Rank 1 delay select for the read DQS gating (DQSG) LCDL.
7-0	R0DQSGD	Reset = 0x0 Rank 0 Read DQS Gating Delay: Rank 0 delay select for the read DQS gating (DQSG) LCDL.

4.68 DATX8 Master Delay Line Register (DXnMDLR)

The DATX8 Master Delay Line Registers return different period values measured by the master delay lines in the DATX8 macros. In the default normal operating conditions, the value of the DXnMDLR registers change based on ongoing calibration and measurements.

Figure 4-68. DATX8 Master Delay Line Register (DXnMDLR)



Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-70. DATX8 Master Delay Line Register (DXnMDLR) Field Descriptions

Bits	Name	Description
31-24	Reserved	Reset = 0x0 Reads return zeros
23-16	MDLD	Reset = 0x0 MDL Delay: Delay select for the LCDL for the Master Delay Line.
15-8	TPRD	Reset = 0x0 Target Period: Target period measured by the master delay line calibration for VT drift compensation. This is the current measured value of the period and is continuously updated if the MDL is enabled to do so.
7-0	IPRD	Reset = 0x0 Initial Period: Initial period measured by the master delay line calibration for VT drift compensation. This value is used as the denominator when calculating the ratios of updates during VT compensation.

4.69 DATX8 General Timing Register (DXnGTR)

This register is used to control various timing settings of the byte lane, including DQS gating system latency and write leveling system latency.

Figure 4-69. DATX8 General Timing Register (DXnGTR)

31 20	19 18	17 16	15 14	13 12
Reserved	R3WLSL	R2WLSL	R1WLSL	R0WLSL
R=0x0	RW=0x1	RW=0x1	RW=0x1	RW=0x1

11 9	8 6	5 3	2 0
R3DGSL	R2DGSL	R1DGSL	R0DGSL
RW=0x0	RW=0x0	RW=0x0	RW=0x0

Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-71. DATX8 General Timing Register (DXnGTR) Field Descriptions

Bits	Name	Description
31-20	Reserved	Reset = 0x0 Reads return zeros
19-18	R3WLSL	Reset = All 0x1 Rank n Write Leveling System Latency: This is used to adjust the write latency after write leveling. Power-up default is 01 (i.e. no extra clock cycles required). The SL fields are initially set by the PUB during automatic write leveling but these values can be overwritten by a direct write to this register. Every two bits of this register control the latency of each of the (up to) four ranks. R0WLSL controls the latency of rank 0, R1WLSL controls rank 1, and so on. Valid values: • 00 = Write latency = WL - 1 • 01 = Write latency = WL • 10 = Write latency = WL + 1 • 11 = Reserved
17-16	R2WLSL	See description for R3WLSL.
15-14	R1WLSL	See description for R3WLSL.
13-12	R0WLSL	See description for R3WLSL.
11-9	R3DGSL	Reset = All 0x0 Rank n DQS Gating System Latency: This is used to increase the number of clock cycles needed to expect valid DDR read data by up to seven extra clock cycles. This is used to compensate for board delays and other system delays. Power-up default is 000 (i.e. no extra clock cycles required). The SL fields are initially set by the PHY during automatic DQS data training but these values can be overwritten by a direct write to this register. Every three bits of this register control the latency of each of the (up to) four ranks. R0DGSL controls the latency of rank 0, R1DGSL controls rank 1, and so on. Valid values are 0 to 7:
8-6	R2DGSL	See description for R3DGSL.
5-3	R1DGSL	See description for R3DGSL.
2-0	R0DGSL	See description for R3DGSL.

Revision History

Changes from January 21, 2015 to March 27, 2015 **Page**

- Added RDIMM is not supported to Features. 12
- Changed RDIMMINIT bit in PHY Initialization Register to Reserved. 85
- Changed PARERR bit in PHY General Status Register to Reserved. 94

(From Revision B to C)

Revision History

Changes from A Revision (May 2014) to B Revision **Page**

- Updated Self-Refresh Mode section. 26
- Changed SDTIM2 offset from 18h to 1Ch. 46
- Updated SDRAM Timing 3 (SDTIM3) Register. 57
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