TMS320C5515/05/VC05 DSP
Liquid Crystal Display Controller (LCDC)

User's Guide

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Read This First

About This Manual

This document describes the liquid crystal display controller (LCDC) on the TMS320C5515/05/VC05 digital signal processor (DSP).

Notational Conventions

This document uses the following conventions.

- Hexadecimal numbers are shown with the suffix h. For example, the following number is 40 hexadecimal (decimal 64): 40h.
- Registers in this document are shown in figures and described in tables.
  - Each register figure shows a rectangle divided into fields that represent the fields of the register. Each field is labeled with its bit name, its beginning and ending bit numbers above, and its read/write properties below. A legend explains the notation used for the properties.
  - Reserved bits in a register figure designate a bit that is used for future device expansion.

Related Documentation From Texas Instruments

The following documents describe the TMS320C5515/14/05/04 Digital Signal Processor (DSP) Digital Signal Processor (DSP). Copies of these documents are available on the internet at http://www.ti.com.

SWPU073 — TMS320C55x 3.0 CPU Reference Guide. This manual describes the architecture, registers, and operation of the fixed-point TMS320C55x digital signal processor (DSP) CPU.

SPRU652 — TMS320C55x DSP CPU Programmer's Reference Supplement. This document describes functional exceptions to the CPU behavior.

SPRUFO0 — TMS320VC5505/5504 Digital Signal Processor (DSP) Universal Serial Bus 2.0 (USB) User's Guide. This document describes the universal serial bus 2.0 (USB) in the TMS320VC5505/5504 Digital Signal Processor (DSP). The USB controller supports data throughput rates up to 480 Mbps. It provides a mechanism for data transfer between USB devices.

SPRUFO1 — TMS320C5515/14/05/04/VC05/VC04 Digital Signal Processor (DSP) Inter-Integrated Circuit (I2C) Peripheral User's Guide. This document describes the inter-integrated circuit (I2C) peripheral in the TMS320VC5505/5504 Digital Signal Processor (DSP) device. The I2C peripheral provides an interface between the device and other devices compliant with Phillips Semiconductors Inter-IC bus (I2C-bus) specification version 2.1 and connected by way of an I2C-bus. This document assumes the reader is familiar with the I2C-bus specification.

SPRUFO2 — TMS320C5515/14/05/04/VC05/VC04 Digital Signal Processor (DSP) Timer/Watchdog Timer User's Guide. This document provides an overview of the three 32-bit timers in the TMS320VC5505/5504 Digital Signal Processor (DSP) device. The 32-bit timers of the device are software programmable timers that can be configured as general-purpose (GP) timers. Timer 2 can be configured as a GP, a Watchdog (WD), or both simultaneously.

SPRUFO3 — TMS320C5515/14/05/04/VC05/VC04 Digital Signal Processor (DSP) Serial Peripheral Interface (SPI) User's Guide. This document describes the serial peripheral interface (SPI) in the TMS320VC5505/5504 Digital Signal Processor (DSP) device. The SPI is a high-speed synchronous serial input/output port that allows a serial bit stream of programmed length (1 to 32 bits) to be shifted into and out of the device at a programmed bit-transfer rate. The SPI supports multi-chip operation of up to four SPI slave devices. The SPI can operate as a master device only.

SPRUFO4 — TMS320C5515/14/05/04/VC05/VC04 Digital Signal Processor (DSP) General-Purpose Input/Output (GPIO) User's Guide. This document describes the general-purpose input/output (GPIO) on the TMS320VC5505/5504 digital signal processor (DSP). The GPIO peripheral provides dedicated general-purpose pins that can be configured as either inputs or outputs. When configured as an input, you can detect the state of an internal register. When configured as an output you can write to an internal register to control the state driven on the output pin.

SPRUFO5 — TMS320C5515/14/05/04/VC05/VC04 Digital Signal Processor (DSP) Universal Asynchronous Receiver/Transmitter (UART) User's Guide. This document describes the universal asynchronous receiver/transmitter (UART) peripheral in the TMS320VC5505/5504 Digital Signal Processor (DSP) device. The UART performs serial-to-parallel conversions on data received from a peripheral device and parallel-to-serial conversion on data received from the CPU.

SPRUFO6 — TMS320C5515/14/05/04/VC05/VC04 Digital Signal Processor (DSP) Multimedia Card (MMC)/Secure Digital (SD) Card Controller User's Guide. This document describes the Multimedia Card (MMC)/Secure Digital (SD) Card Controller on the TMS320VC5505/5504 Digital Signal Processor (DSP) device. The multimedia card (MMC)/secure digital (SD) card is used in a number of applications to provide removable data storage. The MMC/SD card controller provides an interface to external MMC and SD cards.

SPRUF07 — TMS320VC5505/5504 Digital Signal Processor (DSP) Real-Time Clock (RTC) User's Guide. This document describes the operation of the Real-Time Clock (RTC) module in the TMS320VC5505/5504 Digital Signal Processor (DSP) device. The RTC also has the capability to wake-up the power management and apply power to the rest of the device through an alarm, periodic interrupt, or external WAKEUP signal.

SPRUFO8 — TMS320C5515/14/05/04/VC05/VC04 Digital Signal Processor (DSP) External Memory Interface (EMIF) User's Guide. This document describes the operation of the external memory interface (EMIF) in the TMS320VC5505/5504 Digital Signal Processor (DSP) device. The purpose of the EMIF is to provide a means to connect to a variety of external devices.

SPRUFO9 — TMS320VC5505/5504 Digital Signal Processor (DSP) Direct Memory Access (DMA) Controller User's Guide. This document describes the features and operation of the DMA controller that is available on the TMS320VC5505/5504 Digital Signal Processor (DSP) device. The DMA controller is used to move data among internal memory, external memory, and peripherals without intervention from the CPU and in the background of CPU operation.

SPRUFP0 — TMS320VC5505 Digital Signal Processor (DSP) System User's Guide. This document describes various aspects of the TMS320VC5505/5504 digital signal processor (DSP) including: system memory, device clocking options and operation of the DSP clock generator, power management features, interrupts, and system control.

SPRUGL6 — TMS320VC5504 Digital Signal Processor (DSP) System User's Guide. This document describes various aspects of the TMS320VC5505/5504 digital signal processor (DSP) including: system memory, device clocking options and operation of the DSP clock generator, power management features, interrupts, and system control.

SPRUFP1 — TMS320C5515/05/VC05 Digital Signal Processor (DSP) Successive Approximation (SAR) Analog to Digital Converter (ADC) User's Guide. This document provides an overview of the Successive Approximation (SAR) Analog to Digital Converter (ADC) on the TMS320VC5505/5504 Digital Signal Processor (DSP). The SAR is a 10-bit ADC using a switched capacitor architecture which converts an analog input signal to a digital value.

SPRUFP3 — TMS320C5515/05/VC05 Digital Signal Processor (DSP) Liquid Crystal Display Controller (LCDC) User's Guide. This document describes the liquid crystal display controller (LCDC) in the TMS320VC5505/5504 Digital Signal Processor (DSP) device. The LCD controller includes a LCD Interface Display Driver (LIDD) controller.

SPRUFP4 — TMS320VC5505/5504 Digital Signal Processor (DSP) Inter-IC Sound (I2S) Bus User's Guide. This document describes the features and operation of Inter-IC Sound (I2S) Bus in the TMS320VC5505/5504 Digital Signal Processor (DSP) device. This peripheral allows serial transfer of full duplex streaming data, usually streaming audio, between DSP and an external I2S peripheral device such as an audio codec.

Liquid Crystal Display Controller (LCDC)

1 Introduction

The liquid crystal display controller (LCDC) supports asynchronous (memory-mapped) LCD interfaces.

1.1 Purpose of the Peripheral

The LCD controller consists of two independent controllers, the Raster Controller and the LCD Interface Display Driver (LIDD) controller. Each controller operates independently from the other and only one of them is active at any given time. The Raster Controller is currently not supported and is only for feature enhancement for the future.

The LIDD Controller supports the asynchronous LCD interface. It provides full-timing programmability of control signals and output data.

Figure 1 shows internal blocks of the LCD controller. Please note that Figure 1 shows LIDD controller and Raster controller as well but the blocks in gray belong to Raster Controller and are not supported. The solid, thick lines in Figure 1 indicate the data path. The LIDD controllers are responsible for generating the correct external timing. The DMA engine provides a constant flow of data from the frame buffer(s) to the external LCD panel via the LIDD Controllers. In addition, CPU access is provided to read and write registers.

The blocks in gray belong to the Raster Controller that is not supported.

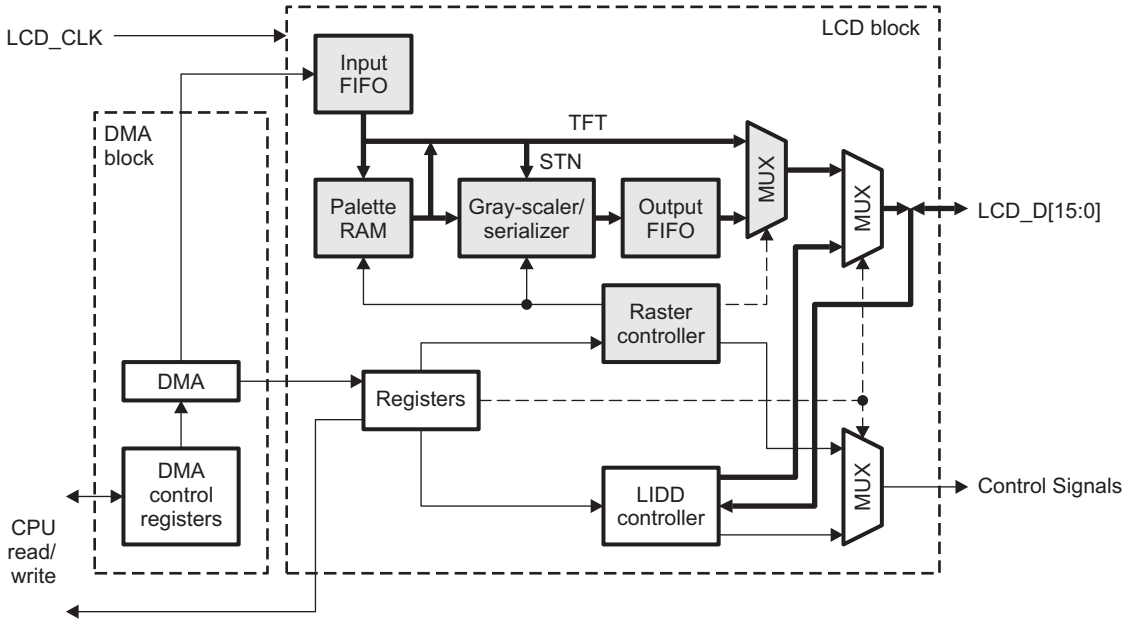


Figure 1. LCD Controller

1.2 Terminology Used in this Document

Term	Meaning
RDB	Read Strobe
WRB	Write Strobe
RS	Register Select
CS	Chip select
OE	Output enable
WE	Write enable

1.2.1 LCD Clock

The LCD controller has an internal clock (LCD_CLK) which is derived from system clock. The LCD_CLK determines the minimum cycle of configuration of the control signals .

$$\text{LCD\_CLK} = \text{SYSTEM\_CLK} \text{ when CLK\_DIV} = 0$$

$$\frac{\text{LCD\_CLK} = \text{SYSTEM\_CLK}}{\text{LCK\_DIV}} \text{ when } 0 < \text{CLK\_DIV} < 256$$

1.3 LCD External I/O Signals

Table 1 shows the details of the LCD controller external signals.

Table 1. LCD External I/O Signals

Signal	Type	Description
LCD_RS	OUT	HD44780U mode: Register Select (RS)
		MPU6800 Sync mode: Command/Data Select (C/D)
		MPU6800 Async mode: Command/Data Select (C/D)
		MPU80 Sync mode: Command/Data Select (C/D)
		MPU80 Async mode: Command/Data Select (C/D)
LCD_RW_WRB	OUT	HD44780U mode: Read/Write Select (R/W)
		MPU6800 Sync mode: Read/Write Select (R/W)
		MPU6800 Async mode: Read/Write Select (R/W)
		MPU80 Sync mode: Write Strobe (WRB)
		MPU80 Async mode: Write Strobe (WRB)
LCD_EN_RDB	OUT	HD44780U mode: not used
		MPU6800 Sync mode: Read or Write Enable (EN)
		MPU6800 Async mode: Read or Write Enable (EN)
		MPU80 Sync mode: Read Strobe (RDB)
		MPU80 Async mode: Read Strobe (RDB)
LCD_CS0_E0	OUT	HD44780U mode: Start Data Read/Write (E0)
		MPU6800 Sync mode: Primary Chip Select (CS0)
		MPU6800 Async mode: Primary Chip Select (CS0)
		MPU80 Sync mode: Primary Chip Select (CS0)
		MPU80 Async mode: Primary Chip Select (CS0)

Table 1. LCD External I/O Signals (continued)

Signal	Type	Description
LCD_CS1_E1	OUT	HD44780U mode: Start Data Read/Write (E1)
		MPU6800 Sync mode: LCD_CLK output
		MPU6800 Async mode: Secondary Chip Select (CS1)
		MPU80 Sync mode: LCD_CLK output
		MPU80 Async mode: Secondary Chip Select (CS1)
LCD_D[15:0]	LIDD: OUT/IN	HD44780U mode: Read and write the command and Data
		MPU6800 Sync mode: Read and write command and data
		MPU6800 Async mode: Read and write command and data
		MPU80 Sync mode: Read and write command and data
		MPU80 Async mode: Read and write command and data

1.4 LCD Interface Display Driver Details (LIDD) Controller

The LIDD Controller is designed to support LCD panels with a memory-mapped interface. The types of displays range from low-end character monochrome LCD panels to high-end TFT smart LCD panels.

LIDD mode (and the use of this logic) is enabled by clearing the MODESEL bit in the LCD control register (LCD_CTRL).

LIDD Controller operation is summarized as follows:

- During initialization, the LCD LIDD CS0/CS1 configuration registers (LIDD_CS0_CONF and LIDD_CS1_CONF) are configured to match the requirements of the LCD panel being used.
- During normal operation, the CPU writes display data to the LCD data registers (LIDD_CS0_DATA and LIDD_CS1_DATA). The LIDD interface converts the CPU write into the proper signal transition sequence for the display, as programmed earlier. Note that the first CPU write should send the beginning address of the update to the LCD panel and the subsequent writes update data at display locations starting from the first address and continuing sequentially. Note that DMA may be used instead of CPU.
- The LIDD Controller is also capable of reading back status or data from the LCD panel, if the latter has this capability. This is set up and activated in a similar manner to the write function described above.

NOTE: If an LCD panel is not used, this interface can be used to control any MCU-like peripheral.

Table 2 describes how the signals are used to interface external LCD modules, which are configured by the LIDD_CTRL register.

Table 2. LIDD I/O Name Map

Display Type	Interface Type	Data Bits	LIDD_CTRL [2:0]	I/O Name	Display I/O Name	Comment
Character Display	HD44780 Type	4	100	LCD_D[7:4]	DATA[7:4]	Data Bus (length defined by Instruction)
				LCD_CS0_E1	E0	Enable Strobe (first display)
				LCD_RW_WRB	R/$\overline{W}$	Read/$\overline{Write}$
				LCD_RS	RS	Register Select (Data/not Instruction)
				LCD_CS1_E1	E1	Enable Strobe (second display optional)

Table 2. LIDD I/O Name Map (continued)

Display Type	Interface Type	Data Bits	LIDD_CTRL [2:0]	I/O Name	Display I/O Name	Comment
Character Display	HD44780 Type	8	100	LCD_D[7:0]	DATA[7:0]	Data Bus (length defined by Instruction)
				LCD_CS0_E0	E0	Enable Strobe (first display)
				LCD_RW_WRB	R/$\overline{W}$	Read/$\overline{Write}$
				LCD_RS	RS	Register Select (Data/not Instruction)
				LCD_CS1_E1	E1	Enable Strobe (second display optional)
Micro Interface Graphic Display	6800 Family	Up To 16	001	LCD_D[7:0]	DATA[7:0]	Data Bus
				LCD_EN_RDB	E	Enable Clock
				LCD_RW_WRB	R/$\overline{W}$	Read/$\overline{Write}$
				LCD_RS	A0	Address/Data Select
				LCD_CS0_E0	CS (or CS0)	Chip Select (first display)
				LCD_CS1_E1	CS1	Chip Select (second display optional)
			000	LCD_CS1_E1	LCD_CLK	LCD_CLK Output for Synchronous Clock
Micro Interface Graphic Display	8080 Family	Up To 16	011	LCD_D[7:0]	DATA[7:0]	Data Bus
				LCD_EN_RDB	RD	Read Strobe
				LCD_RW_WRB	WR	Write Strobe
				LCD_RS	A0	Address/Data Select
				LCD_CS1_E0	CS (or CS0)	Chip Select (first display)
				LCD_CS1_E1	CS1	Chip Select (second display optional)
			010	LCD_CLK	LCD_CLK	LCD_CLK Output for Synchronous Clock

The timing parameters are defined by the LIDD_CS0_CONF and LIDD_CS1_CONF registers.

The timing configuration is based on an internal reference clock, LCD_CLK. LCD_CLK is generated out of System Clock , which is determined by the CLKDIV bit in the LCD_CTRL register.

$$\text{LCD\_CLK} = \text{SYSTEM\_CLK when CLK\_DIV} = 0$$

$$\frac{\text{LCD\_CLK} = \text{SYSTEM\_CLK}}{\text{LCK\_DIV}} \text{ when } 0 < \text{CLK\_DIV} < 256$$

1.5 LIDD Controller Timing

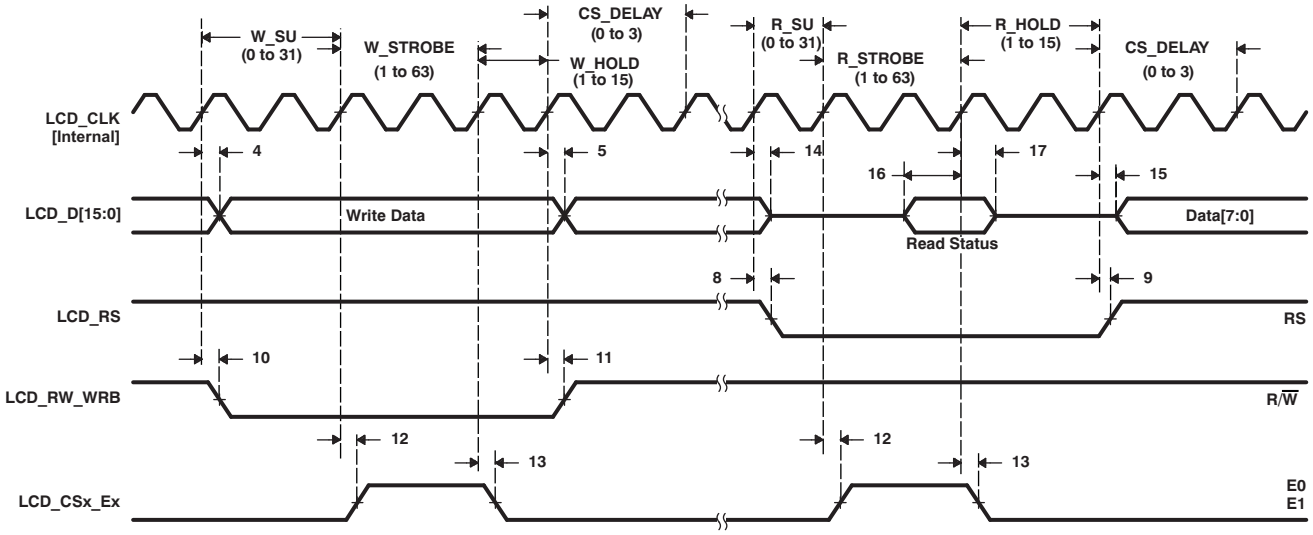
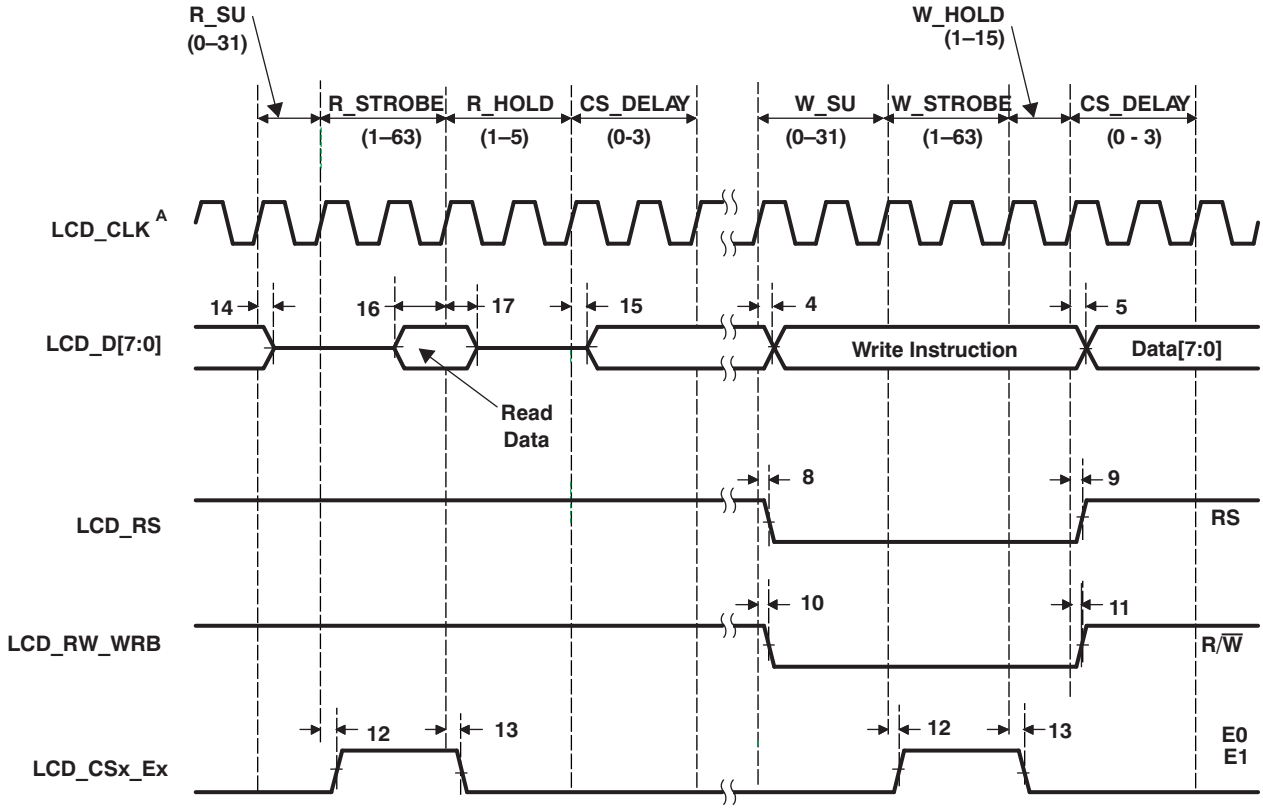
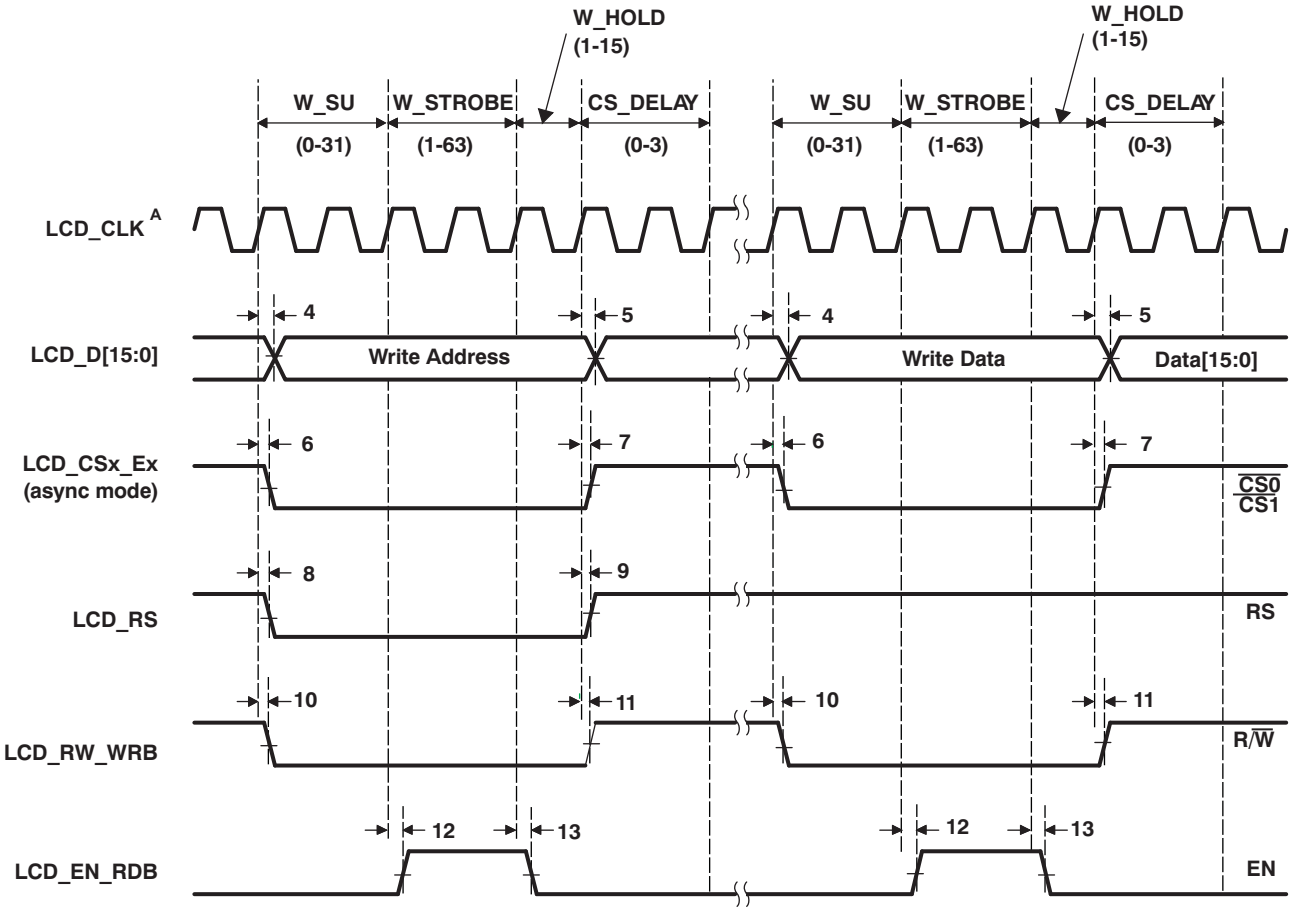


Figure 2. LIDD Mode HD44780 Write Timing Diagram



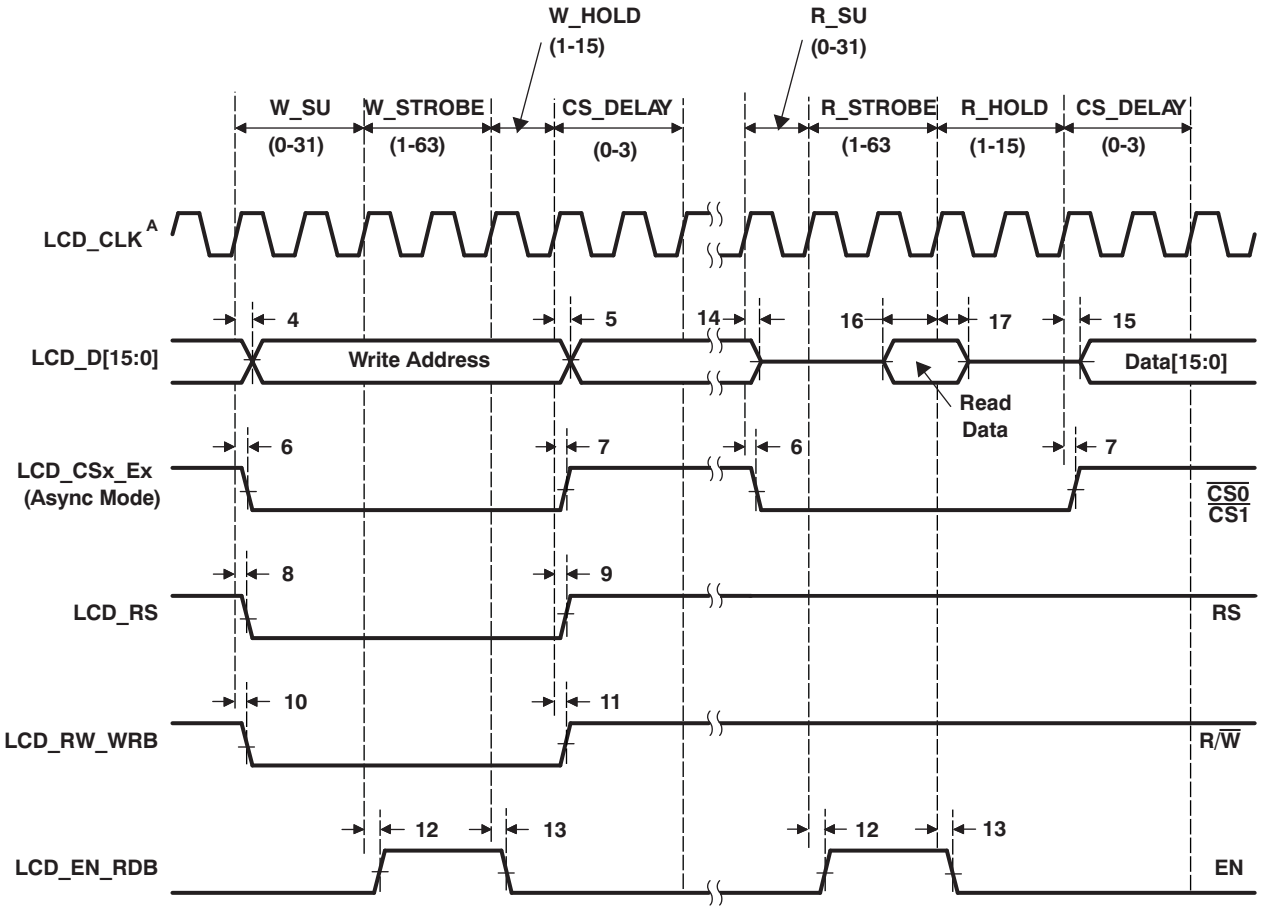
A In 6800 Async mode, LCD_CLK is internal
In 6800 Sync mode, LCD_CLK is output via LCD_CS1_E1

Figure 3. LIDD Mode HD44780 Read Timing Diagram



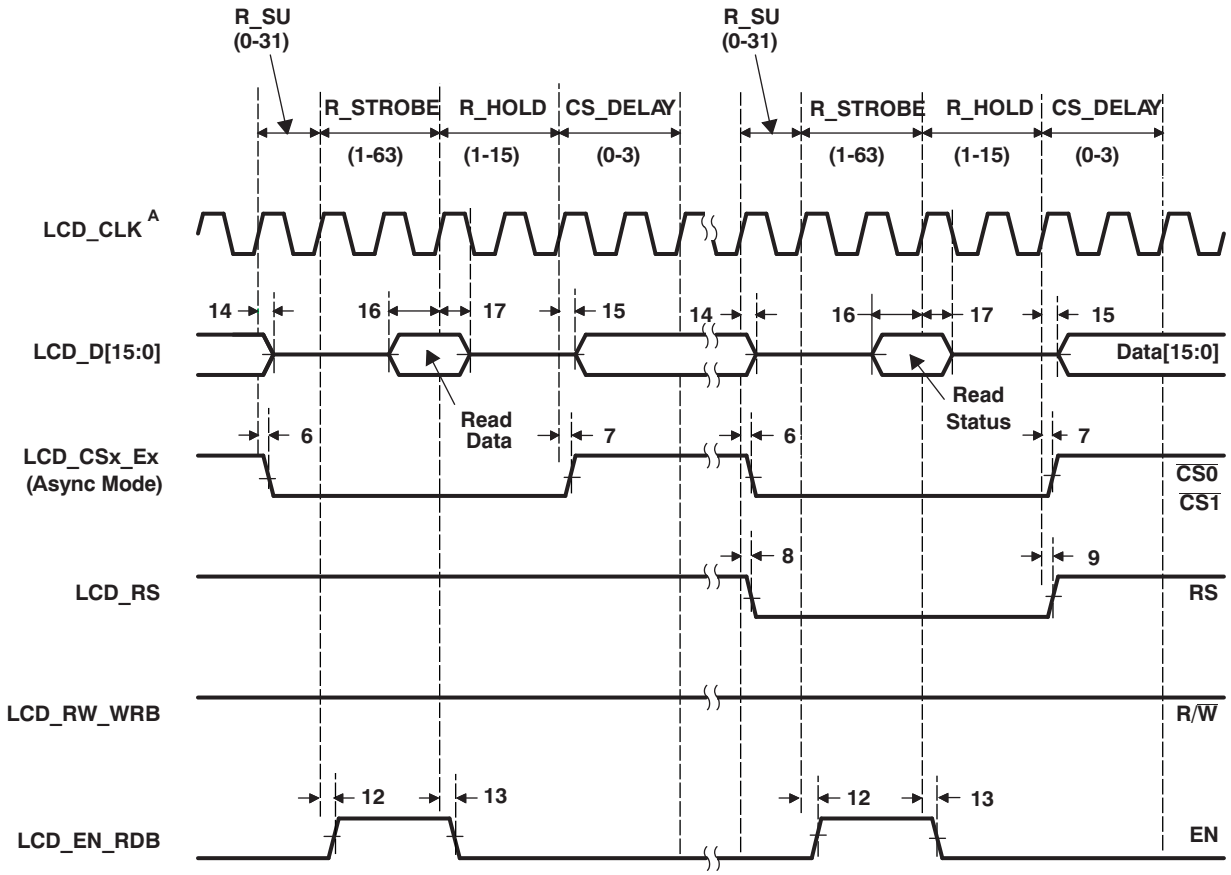
A In 6800 Async mode, LCD_CLK is internal
In 6800 Sync mode, LCD_CLK is output via LCD_CS1_E1

Figure 4. LIDD Mode 6800 Write Timing Diagram



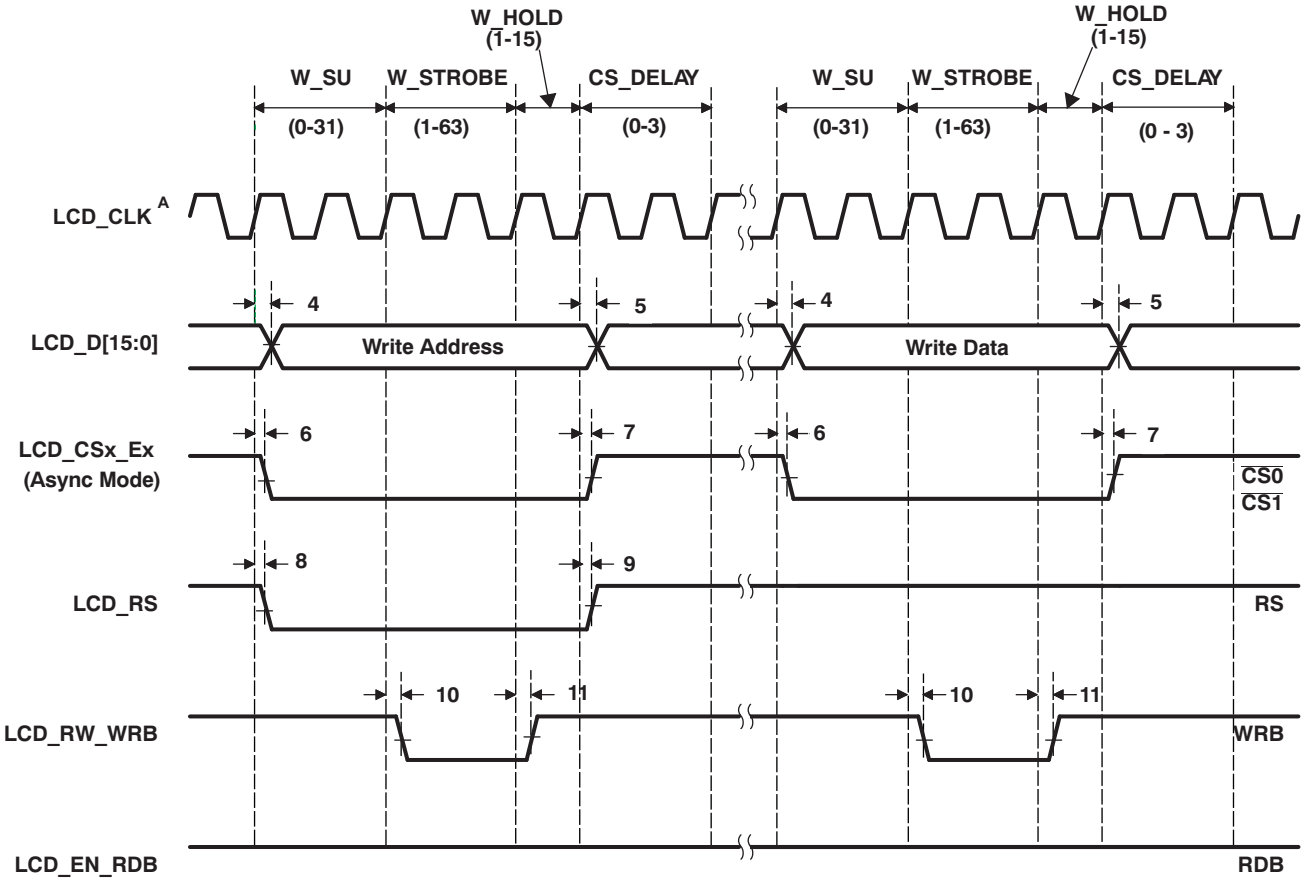
A In 6800 Async mode, LCD_CLK is internal
In 6800 Sync mode, LCD_CLK is output via LCD_CS1_E1

Figure 5. LIDD Mode 6800 Read Timing Diagram



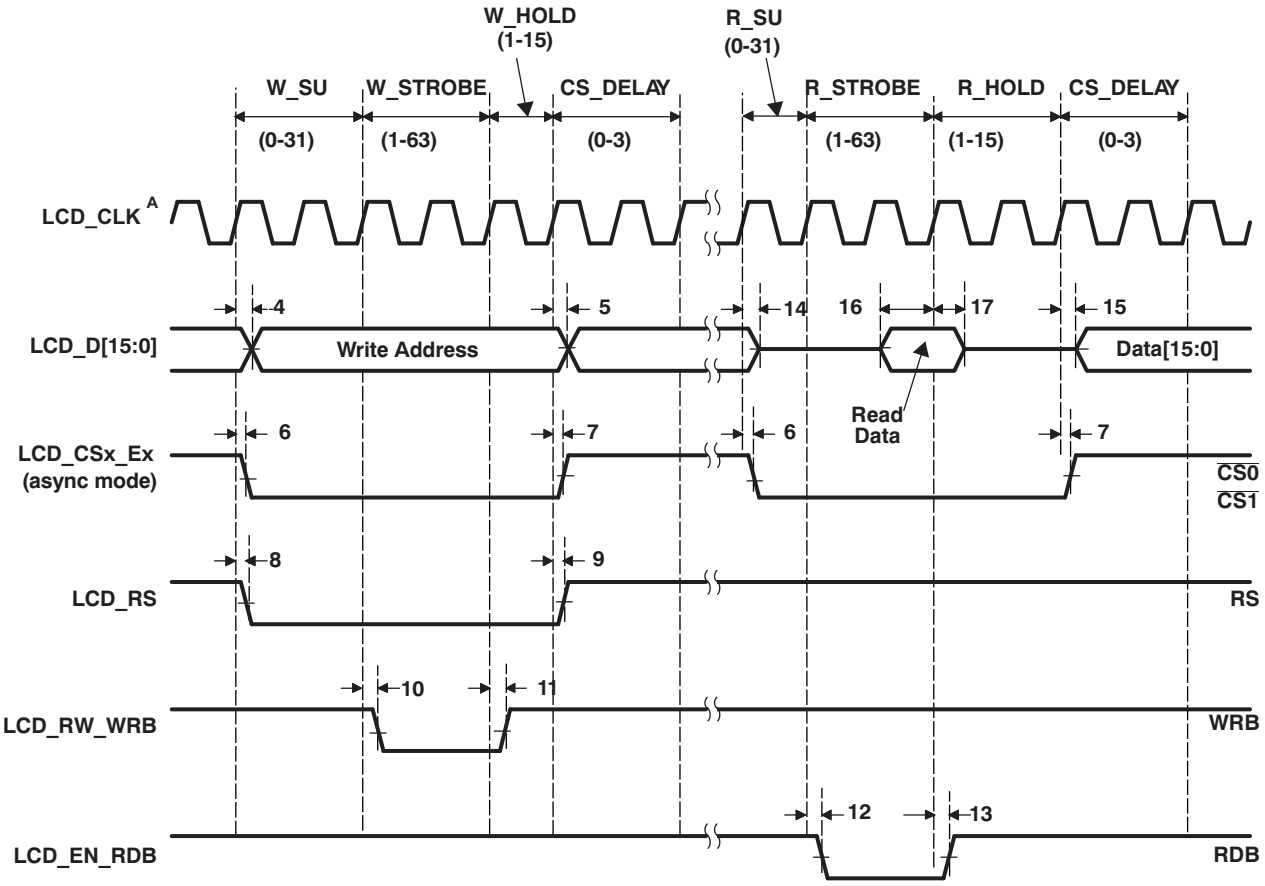
A In 6800 Async mode, LCD_CLK is internal
In 6800 Sync mode, LCD_CLK is output via LCD_CS1_E1

Figure 6. LIDD Mode 6800 Status Timing Diagram



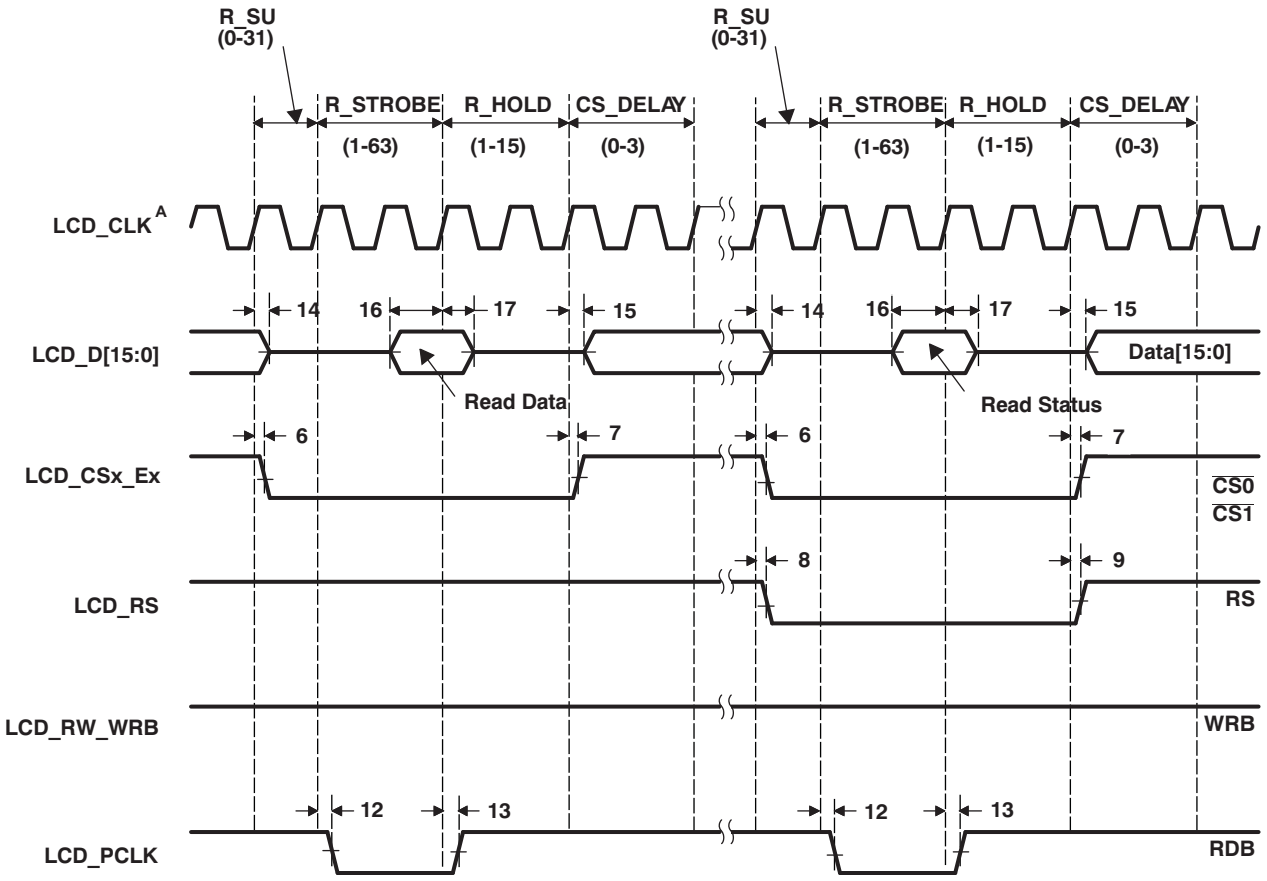
A In 8080 Async mode, LCD_CLK is internal
In 8080 Sync mode, LCD_CLK is output via LCD_CS1_E1

Figure 7. LIDD Mode 8080 Write Timing Diagram



A In 8080 Async mode, LCD_CLK is internal
In 8080 Sync mode, LCD_CLK is output via LCD_CS1_E1

Figure 8. LIDD Mode 8080 Read Timing Diagram



A In 8080 Async mode, LCD_CLK is internal
In 8080 Sync mode, LCD_CLK is output via LCD_CS1_E1

Figure 9. LIDD Mode 8080 Status Timing Diagram

1.6 DMA Engine

The DMA engine provides the capability to output data constantly, without burdening the CPU, via interrupts or a firmware timer. It operates on one or two frame buffers, which are set up during initialization. Using two frame buffers (ping-pong buffers) enables the simultaneous operation of outputting the current video frame to the external display and updating the next video frame. The ping-pong buffering approach is preferred in most applications.

The DMA engine accesses the LIDD Controller's address and/or data registers.

To program DMA engine, configure the following registers, as shown in Table 3.

Table 3. Register Configuration for DMA Engine Programming

Register	Configuration
LCDDMA_CTRL	Configure DMA data format
LCDDMA_FB0_BASE LCDDMA_FB0_CEILING	Configure frame buffer 0
LCDDMA_FB1_BASE LCDDMA_FB1_CEILING	Configure frame buffer 1 (If only one frame buffer is used, these two registers will not be used.)

In addition, the LIDD_CTRL register (for LIDD Controller) should also be configured appropriately, along with all the timing registers.

To enable DMA transfers, the LIDD_DMA_EN bit (in the LIDD_CTRL register) should be written with 1.

1.6.1 Interrupts

Interrupts in this LCD module are related to DMA engine operation. Two registers are closely related to this subject:

- The LIDD_CTRL enables or disables .
- The LCD_STAT register collects all the interrupt status information.

The DMA engine generates one interrupt signal every time the specified frame buffer has been transferred completely.

- The DONE_INT_EN bit in the LIDD_CTRL register specifies if the interrupt signal is delivered to the system interrupt controller, which in turn may or may not generate an interrupt to CPU.
- The EOF1, EOF0, and DONE bits in the LCD_STAT register reflect the interrupt signal, regardless of being delivered to the system interrupt controller or not.

1.6.1.1 Interrupt Handling

Refer the device-specific data manual for information about LCD interrupt number to CPU .The interrupt service routine needs to determine the interrupt source by examining the LCD_STAT register and clearing the interrupt properly.

2 LCD Port Mapping

The VC5505 DSP uses pin multiplexing to accommodate a larger number of peripheral functions in the smallest possible package, providing the ultimate flexibility for end applications. The external bus selection register (EBSR) controls all the pin multiplexing functions on the device. LCD ports can be 8-bit LCD ports, 16-bit LCD ports, or disabled via the EBSR register. For more details on the EBSR register, see the *TMS320VC5505 Digital Signal Processor (DSP) System User's Guide* (SPRUFP0).

3 Registers

Table 4 lists the memory-mapped registers for the LCD Controller (LCDC). See the device-specific data manual for the memory address of these registers.

Table 4. LCD Controller (LCDC) Registers

CPU Word Address	Acronym	Register Description	Section
2E00h	LCDREVMIN	LCD Minor Revision Register	Section 3.1
2E01h	LCDREVMAJ	LCD Major Revision Register	Section 3.2
2E04h	LCDCR	LCD Control Register	Section 3.3
2E08h	LCDSR	LCD Status Register	Section 3.4
2E0Ch	LCDLIDDCR	LCD LIDD Control Register	Section 3.5
2E10h	LCDLIDDCS0CONFIG0	LCD LIDD CS0 Configuration Register 0	Section 3.6
2E11hh	LCDLIDDCS0CONFIG1	LCD LIDD CS0 Configuration Register 1	Section 3.7
2E14h	LCDLIDDCS0ADDR	LCD LIDD CS0 Address Read/Write Register	Section 3.8
2E18h	LCDLIDDCS0DATA	LCD LIDD CS0 Data Read/Write Register	Section 3.9
2E1Ch	LCDLIDDCS1CONFIG0	LCD LIDD CS1 Configuration Register 0	Section 3.6
2E1Dh	LCDLIDDCS1CONFIG1	LCD LIDD CS1 Configuration Register 1	Section 3.7
2E20h	LCDLIDDCS1ADDR	LCD LIDD CS1 Address Read/Write Register	Section 3.8
2E24h	LCDLIDDCS1DATA	LCD LIDD CS1 Data Read/Write Register	Section 3.9
2E28h – 2E3Ah	-	Reserved	-
2E40h	LCDDMACR	LCD DMA Control Register	Section 3.10
2E44h	LCDDMAFB0BAR0	LCD DMA Frame Buffer 0 Base Address Register 0	Section 3.11
2E45h	LCDDMAFB0BAR1	LCD DMA Frame Buffer 0 Base Address Register 1	Section 3.12
2E48h	LCDDMAFB0CAR0	LCD DMA Frame Buffer 0 Ceiling Address Register 0	Section 3.13
2E49h	LCDDMAFB0CAR1	LCD DMA Frame Buffer 0 Ceiling Address Register 1	Section 3.14
2E4Ch	LCDDMAFB1BAR0	LCD DMA Frame Buffer 1 Base Address Register 0	Section 3.15
2E4Dh	LCDDMAFB1BAR1	LCD DMA Frame Buffer 1 Base Address Register 1	Section 3.16
2E50h	LCDDMAFB1CAR0	LCD DMA Frame Buffer 1 Ceiling Address Register 0	Section 3.17
2E51h	LCDDMAFB1CAR1	LCD DMA Frame Buffer 1 Ceiling Address Register 1	Section 3.18

3.1 LCD Minor Revision Register (LCDREVMIN)

The LCD minor revision register (LCDREVMIN) is shown in Figure 10 and described in Table 5.

Figure 10. LCD Minor Revision Register (LCDREVMIN)

15	0
REVMIN	
R- 0000h	

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 5. LCD Minor Revision Register (LCDREVMIN) Field Descriptions

Bit	Field	Value	Description
15-0	REVMIN	0000h	Minor Revision.

3.2 LCD Major Revision Register (LCDREVMAJ)

The LCD major revision register (LCDREVMAJ) is shown in Table 6 and described in Table 6.

Figure 11. LCD Major Revision Register (LCDREVMAJ)

15	0
REVMAJ	
R-0001h	

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 6. LCD Major Revision Register (LCDREVMAJ) Field Descriptions

Bit	Field	Value	Description
15-0	REVMAJ	0001h	Major Revision.

3.3 LCD Control Register (LCDCR)

The LCD control register (LCDCR) is shown in Figure 12 and described in Table 7.

Figure 12. LCD Control Register (LCDCR)

15	8	7	1	0
CLKDIV		Reserved		MODESEL
RW-0		R-0		RW-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 7. LCD Control Register (LCDCR) Field Descriptions

Bit	Field	Value	Description
15-8	CLKDIV	0-FFh	Clock Divisor Value (from 0–255) is used to specify the frequency of LCD_CLK .
7-1	Reserved	0	Reserved.
0	MODESEL		LCD Mode Select. MODESEL should be set to 0 (default) all the time. Raster mode is not supported.
		0	LCD Controller in LIDD mode.
		1	LCD Controller in Raster mode (not supported).

The 8-bit clock divider (CLKDIV) field is used to select the frequency LCD_CLK.

$$\text{LCD\_CLK} = \text{SYSTEM\_CLK} \text{ when } \text{CLK\_DIV} = 0$$

$$\text{LCD\_CLK} = \frac{\text{SYSTEM\_CLK}}{\text{CLK\_DIV}} \text{ when } 0 < \text{CLK\_DIV} < 256$$

3.4 LCD Status Register (LCDSR)

The LCD status register (LCD_STAT) contains bits that signal status to the processor. Each of the LCD status bits signals an interrupt request as long as the bit is set AND the interrupt enable for that bit is also set (see the LCD DMA control register for these enables). Writing a 1 to each bit clears it; once the bit is cleared, the interrupt is cleared.

The LCD status register (LCDSR) is shown in Figure 13 and described in Table 8.

Figure 13. LCD Status Register (LCDSR)

15	10	9	8
Reserved		EOF1	EOF0
R-0		RW-0	RW-0

7	1	0
Reserved		DONE
R-0		RW-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 8. LCD Status Register (LCDSR) Field Descriptions

Bit	Field	Value	Description
15-10	Reserved	0	Reserved.
9	EOF1		End of Frame 1
		0	No end of frame 1 detected
		1	End of frame 1 detected.
8	EOF0		End of Frame 0
		0	No end of frame 0 detected.
		1	End of frame 0 detected.
7-1	Reserved	0	Reserved.
0	DONE		LIDD Frame Done.
		0	Raster engine enabled.
		1	Raster engine disabled.

3.5 LCD LIDD Control Register (LCDLIDDCR)

The LCD LIDD control register (LIDD_CTRL) contains the polarity controls for LIDD output signals (to account for variety in the external LCD display/peripheral signal requirements), and the LIDD type select bits.

NOTE: To activate DMA to drive LIDD interface, all other control bit-fields must be programmed before setting LIDD_DMA_EN = 1 and must also disable LIDD_DMA_EN bit when changing the state of any control bit within the LCD controller.

The LCD LIDD control register (LCDLIDDCR) is shown in Figure 14 and described in Table 9.

Figure 14. LCD LIDD Control Register (LCDLIDDCR)

15					11	10	9	8
Reserved						DONE_INT_EN	DMA_CS0_CS1	LIDD_DMA_EN
R-0						RW-0	RW-0	RW-0
7	6	5	4	3	2			0
CS1_E1_POL	CS0_E0_POL	WS_DIR_POL	RS_EN_POL	RSPOL	LIDD_MODE_SEL			
RW-0	RW-0	RW-0	RW-0	RW-0	RW-0			

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 9. LCD LIDD Control Register (LCDLIDDCR) Field Descriptions

Bit	Field	Value	Description
15-11	Reserved	0	Reserved
10	DONE_INT_EN		LIDD Frame Done Interrupt Enable
		0	Disable LIDD Frame Done interrupt.
		1	Enable LIDD Frame Done interrupt (seen on LCD Status Reg bit 0).
9	DMA_CS0_CS1		CS0/CS1 Select for LIDD DMA writes
		0	DMA writes to LIDD CS0.
		1	DMA writes to LIDD CS1.
8	LIDD_DMA_EN		LIDD DMA Enable
		0	Deactivate DMA control of LIDD interface; DMA control is released upon completion of transfer of the currentframe of data (LIDD Frame Done) after this bit is cleared. The MPU has direct read/write access to the panel in this mode .
		1	Activate DMA to drive LIDD interface to support streaming data to "smart" panels. The MPU cannot access the panel directly in this mode.
7	CS1_E1_POL		Chip Select 1/Enable 1 (Secondary) Polarity Control.
		0	Do Not Invert Chip Select 1/Enable 1
		1	Invert Chip Select 1/Enable 1 Chip Select 1 is active low by default; Enable 1 is active high by default.
6	CS0_E0_POL		Chip Select 0/Enable 0 (Primary) Polarity Control.
		0	Do Not Invert Chip Select 0/Enable 0
		1	Invert Chip Select 0/Enable 0 Chip Select 0 is active low by default; Enable 0 is active high by default.
5	WS_DIR_POL		Write Strobe/Direction Polarity Control
		0	Do Not Invert Write Strobe/Direction
		1	Invert Write Strobe/Direction Write Strobe/Direction is active low/write low by default.
4	RS_EN_POL		Read Strobe/Enable Polarity Control
		0	Do Not Invert Read Strobe/Enable
		1	IInvert Read Strobe/Enable Read Strobe is active low by default; Enable is active high by default
3	RSPOL		Register Select Polarity Control
		0	Do not invert RS
		1	Invert RS. RS is active low by default

Table 9. LCD LIDD Control Register (LCDLIDDCR) Field Descriptions (continued)

<table>
<tr><th>Bit</th><th>Field</th><th>Value</th><th>Description</th></tr>
<tr><td>2-0</td><td>LIDD_MODE_SEL</td><td>0-7h</td><td>LIDD Mode Select. Selects type of LCD interface for the LIDD to drive. LIDD_MODE_SEL defines the function of LCD external pins as follows:
<table>
<tr><th>Pin</th><th>000b</th><th>001b</th><th>010b</th><th>011b</th><th>100b</th></tr>
<tr><td>LCD_EN_RDB</td><td>EN</td><td>EN</td><td>RDB</td><td>RDB</td><td>N/A</td></tr>
<tr><td>LCD_RW_WRB</td><td>R/W</td><td>R/W</td><td>WRB</td><td>WRB</td><td>R/W</td></tr>
<tr><td>LCD_RS</td><td>D/C(RS)</td><td>D/C (RS)</td><td>D/C (RS)</td><td>D/C (RS)</td><td>RS</td></tr>
<tr><td>LCD_CS0_E0</td><td>CS0</td><td>CS0</td><td>CS0</td><td>CS0</td><td>E0</td></tr>
<tr><td>LCD_CS1_E1</td><td>LCD_CLK</td><td>CS1</td><td>LCD_CLK</td><td>CS1</td><td>E1</td></tr>
</table>
0 MPU6800 Sync mode
1h MPU 6800 Async mode
2h MPU80 Sync mode
3h MPU80 Async mode
4h Hitachi Async (HD44780)mode</td></tr>
</table>

3.6 LCD LIDD CS0 and CS1 Configuration Register 0 (LCDLIDDCS0CONFIG0 and LCDLIDDCS1CONFIG0)

The LCD LIDD CS0 and CS1 Configuration Register 0 (LCDLIDDCS0CONFIG0 and LCDLIDDCS1CONFIG0) provides the capability to configure write and read strobe timing parameters to meet a variety of interface timing requirements for the chip select 0 (primary) device and chip select 1 (secondary) device, respectively. These values are in LCD_CLK cycles; LCD_CLK is divided down from system clock as defined by the CLKDIV field in the LCD control register.

The LLCD LIDD CS0 and CS1 Configuration Register 0 (LCDLIDDCS0CONFIG0 and LCDLIDDCS1CONFIG0) is shown in Figure 15 and described in Table 10.

Figure 15. LCD LIDD CS0 and CS1 Configuration Register 0 (LCDLIDDCS0CONFIG0 and LCDLIDDCS1CONFIG0)

15 12	11 6	5 2	1 0
R_SU0	R_STROBE	R_HOLD	TA
RW-0	RW-1	RW-1	RW-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 10. LCD LIDD CS0 and CS1 Configuration Register 0 (LCDLIDDCS0CONFIG0 and LCDLIDDCS1CONFIG0) Field Descriptions

Bit	Field	Value	Description
15-12	R_SU0	0-Fh	Read Strobe Set-Up cycles (lower 4 bits upper bit is in LIDD CSO config reg 1 at bit-0) Field value defines number of LCD_CLK cycles after Data Bus/Pad Output Enable, ALE, Direction bit and Chip Select 0 have been set-up before the Read Strobe is asserted when performing a read access.
11-6	R_STROBE	0-3Fh	Read Strobe Duration cycles Field value defines number of LCD_CLK cycles for which the Read Strobe is held active when performing a read access.
5-2	R_HOLD	0-Fh	Read Strobe Hold cycles Field value defines number of LCD_CLK cycles for which Data Bus/Pad Output Enable, ALE, Direction bit and Chip Select 0 are held after the Read Strobe is deasserted when performing a read access.
1-0	TA	0-3h	Field value defines number of LCD_CLK cycles between the end of one CS0 device access and the start of another CS0 device access unless the two accesses are both reads, in which case this delay is not incurred.

3.7 LCD LIDD CS0 and CS1 Configuration Register 1 (LCDLIDDCS0CONFIG1 and LCDLIDDCS1CONFIG1)

The LCD LIDD CS0 and CS1 Configuration Register 1 (LCDLIDDCS0CONFIG1 and LCDLIDDCS1CONFIG1) provides the capability to configure write and read strobe timing parameters to meet a variety of interface timing requirements for the chip select 0 (primary) device and chip select 1 (secondary) device, respectively. These values are in LCD_CLK cycles; LCD_CLK is divided down from system clock as defined by the CLKDIV field in the LCD control register.

The LCD LIDD CS0 and CS1 Configuration Register 1 (LCDLIDDCS0CONFIG1 and LCDLIDDCS1CONFIG1) is shown in Figure 16 and described in Table 11.

Figure 16. LCD LIDD CS0 and CS1 Configuration Register 1 (LClidd_cs1_1DLIDDCS0CONFIG1 and LCDLIDDCS1CONFIG1)

15 11	10 5	4 1	0
W_SU	W_STROBE	W_HOLD	R_SU1
RW-0	RW-1	RW-1	RW-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 11. LCD LIDD CS0 and CS1 Configuration Register 1 (LCDLIDDCS0CONFIG1 and LCDLIDDCS1CONFIG1) Field Descriptions

Bit	Field	Value	Description
15-11	W_SU	0-1Fh	Write Strobe Set-Up cycles Field value defines number of LCD_CLK cycles after Data Bus/Pad Output Enable, ALE, Direction bit and Chip Select 0 have been set-up before the Write Strobe is asserted when performing a write access.
10-5	W_STROBE	0-3Fh	Write Strobe Duration cycles Field value defines number of LCD_CLK cycles for which the Write Strobe is held active when performing a write access.
4-1	W_HOLD	0-Fh	Write Strobe Hold cycles Field value defines number of LCD_CLK cycles for which Data Bus/Pad Output Enable, ALE, Direction bit and Chip Select 0 are held after the Write Strobe is deasserted when performing a write access.
0	R_SU1	1-0	Most Significant Bit for Read Strobe Set-Up cycles (upper bit. The lower 4 bits are located in LIDD CSO confir reg 0) Field value defines number of LCD_CLK cycles after Data Bus/Pad Output Enable, ALE, Direction bit and Chip Select 0 have been set-up before the Read Strobe is asserted when performing a read access.

3.8 LCD LIDD CS0 and CS1 Address Read/Write Register (LCDLIDDCS0ADDR and LCDLIDDCS1ADDR)

The LCD LIDD CS0 and SC1 Address Read/Write Register (LCDLIDDCS0ADDR and LCDLIDDCS1ADDR) are accessed by the processor to perform the address/index read or write operations on the CS0 and CS1 device respectively. Writing to LCDLIDDCS0ADDR asserts CS0 and Address Latch Enable, which loads the ADR_INDX field of this register into the address generator of the peripheral device. Likewise, reading from LCDLIDDCS0ADDR asserts CS0 and Address Latch Enable, which loads status information from the peripheral device into the ADR_INDX field of this register. Similarly writing to LCDLIDDCS1ADDR asserts CS1 and Address Latch Enable, which loads the ADR_INDX field of this register into the address generator of the peripheral device. Likewise, reading from LCDLIDDCS1ADDR asserts CS1 and Address Latch Enable, which loads status information from the peripheral device into the ADR_INDX field of this register.

The LCD LIDD CS0 and SC1 Address Read/Write Register (LCDLIDDCS0ADDR and LCDLIDDCS1ADDR) is shown in Figure 17 and described in Table 12.

Figure 17. LCD LIDD CS0 and CS1 Address Read/Write Register (LCDLIDDCS0ADDR and LCDLIDDCS1ADDR)

15	0
ADR_INDX	
RW-0	

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 12. LCD LIDD CS0 and CS1 Address Read/Write Register (LCDLIDDCS0ADDR and LCDLIDDCS1ADDR) Field Descriptions

Bit	Field	Value	Description
15-0	ADR_INDX	0-FFFFh	Peripheral Device Address/Index value. On writes, this field is loaded into the CSn peripheral device's address generator. On reads, this field contains the CSn peripheral device's status

3.9 LCD LIDD CS0 and CS1 Data Read/Write Register (LCDLIDDCS0DATA and LCDLIDDCS1DATA)

The LCD LIDD CS0 and CS1 Data Read/Write Register (LCDLIDDCS0DATA and LCDLIDDCS1DATA) are accessed by the processor to perform the data read or write operations on the CS0 and CS1 device respectively . Writing to LCDLIDDCS0DATA asserts CS0 and deasserts Address Latch Enable, which loads the DATA field of this register into the peripheral device. Likewise, reading from this register asserts CS0 and deasserts Address Latch Enable, which loads data from the peripheral device into the DATA field of this register. Similarly writing to LCDLIDDCS1DATA asserts CS1 and deasserts Address Latch Enable, which loads the DATA field of this register into the peripheral device. Likewise, reading from LCDLIDDCS1DATA asserts CS1 and deasserts Address Latch Enable, which loads data from the peripheral device into the DATA field of this register.

The LCD LIDD CS0 and CS1 Data Read/Write Register (LCDLIDDCS0DATA and LCDLIDDCS1DATA) is shown in Figure 18 and described in Table 13.

Figure 18. LCD LIDD CS0 and CS1 Data Read/Write Register (LCDLIDDCS0DATA and LCDLIDDCS1DATA)

15	0
DATA	
RW-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 13. LCD LIDD CS0 and CS1 Data Read/Write Register (LCDLIDDCS0DATA and LCDLIDDCS1DATA) Field Descriptions

Bit	Field	Value	Description
15-0	DATA	0-FFFFh	Peripheral Device Data value. On writes, this field is loaded into the CSn peripheral device. On reads, this field contains the CSn peripheral device's data.

3.10 LCD DMA Control Register (LCDDMACR)

The LCD DMA control register (LCDDMACR) is shown in Figure 19 and described in Table 14.

Figure 19. LCD DMA Control Register (LCDDMACR)

15						8
Reserved						
R-0						

7	6	4	3	2	1	0
Reserved	BURST_SIZE		Reserved	EOF_INTEN	BIGENDIAN	FRAME_MODE
R-0	RW-0		R-0	RW-0	RW-0	RW-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 14. LCD DMA Control Register (LCDDMACR) Field Descriptions

Bit	Field	Value	Description
15-7	Reserved	0	Reserved.
6-4	BURST_SIZE		Burst Size setting for DMA transfers (all DMA transfers are 32 bits wide).
		0	Burst size of 1
		1	Burst size of 2
		2h	Burst size of 4
		3h	Burst size of 8
		4h	Burst size of 16
		5h-7h	Reserved.
3	Reserved	0	Reserved.
2	EOF_INTEN		End of Frame interrupt enable Setting this bit allows the End of Frame 0 or 1 Status bits in the LCD Status Register to trigger an interrupt 0: End of Frame 0/1Interrupt disabled 1: End of Frame 0/1Interrupt enabled.
		0	EoF Interrupt disabled.
		1	EoF Interrupt enabled.
1	BIGENDIAN		Big Endian enable Use this bit when the processor is operating in Big Endian mode and writes to the frame buffer(s) are less than 32 bits wide; only in this scenario we need to change the byte alignment for data coming into the FIFO from the frame buffer(s) 0: Big Endian data reordering disabled 1: Big Endian data reordering enabled.
		0	Big Endian disabled.
		1	Big Endian enabled.
0	FRAME_MODE		Frame Mode 0: one frame buffer (FB0 only) used 1: two frame buffers used; DMA ping-pongs between FB0 and FB1 in this mode
		0	One Frame buffer used
		1	Two frame buffers used.

3.11 LCD DMA Frame Buffer 0 Base Address Register 0 (LCDDMAFB0BAR0)

The LCD DMA frame buffer 0 base address register 0 is shown in Figure 20 and described in Table 15.

Figure 20. LCD DMA Frame Buffer 0 Base Address Register 0 (LCDDMAFB0BAR0)

15	0
FB0_BASE0	
RW-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 15. LCD DMA Frame Buffer 0 Base Address Register 0 (LCDDMAFB0BAR0) Field Descriptions

Bit	Field	Value	Description
15-0	FB0_BASE0	0-FFFFh	Frame Buffer 0 Base Address pointer LSW; 2 LSBs are hardwired to be 00.

3.12 LCD DMA Frame Buffer 0 Base Address Register 1 (LCDDMAFB0BAR1)

The LCD DMA frame buffer 0 base address register 1 is shown in Figure 21 and described in Table 16.

Figure 21. LCD DMA Frame Buffer 0 Base Address Register 1 (LCDDMAFB0BAR1)

15	0
FB0_BASE1	
RW-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 16. LCD DMA Frame Buffer 0 Base Address Register 1 (LCDDMAFB0BAR1) Field Descriptions

Bit	Field	Value	Description
15-0	FB0_BASE1	0-FFFFh	Frame Buffer 0 Base Address pointer MSW.

3.13 LCD DMA Frame Buffer 0 Ceiling Address Register 0 (LCDDMAFB0CAR0)

The LCD DMA frame buffer 0 ceiling address register 0 is shown in Figure 22 and described in Table 17.

Figure 22. LCD DMA Frame Buffer 0 Ceiling Address Register 0 (LCDDMAFB0CAR0)

15	0
FB0_CEIL0	
RW-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 17. LCD DMA Frame Buffer 0 Ceiling Address Register 0 (LCDDMAFB0CAR0) Field Descriptions

Bit	Field	Value	Description
15-0	FB0_CEIL0	0-FFFFh	Frame Buffer 0 Ceiling Address pointer LSW; 2 LSBs are hardwired to be 00.

3.14 LCD DMA Frame Buffer 0 Ceiling Address Register 1 (LCDDMAFB0CAR1)

The LCD DMA frame buffer 0 ceiling address register 1 is shown in Figure 23 and described in Table 18.

Figure 23. LCD DMA Frame Buffer 0 Ceiling Address Register 1 (LCDDMAFB0CAR1)

15	0
FB0_CEIL1	
RW-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

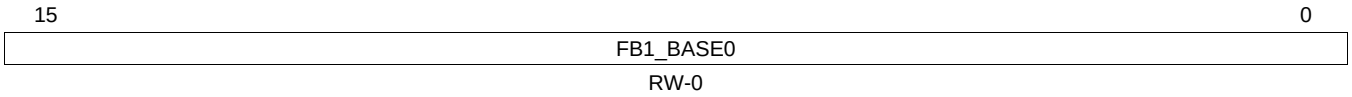
Table 18. LCD DMA Frame Buffer 0 Ceiling Address Register 1 (LCDDMAFB0CAR1) Field Descriptions

Bit	Field	Value	Description
15-0	FB0_CEIL1	0-FFFFh	Frame Buffer 0 Ceiling Address pointer MSW.

3.15 LCD DMA Frame Buffer 1 Base Address Register 0 (LCDDMAFB1BAR0)

The LCD DMA frame buffer 1 base address register 0 is shown in Figure 24 and described in Table 19.

Figure 24. LCD DMA Frame Buffer 1 Base Address Register 0 (LCDDMAFB1BAR0)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

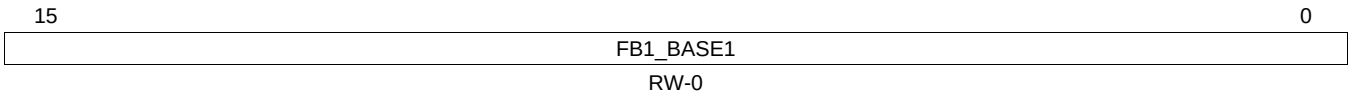
Table 19. LCD DMA Frame Buffer 1 Base Address Register 0 (LCDDMAFB1BAR0) Field Descriptions

Bit	Field	Value	Description
15-0	FB1_BASE0	0-FFFFh	Frame Buffer 1 Base Address pointer LSW; 2 LSBs are hardwired to be 00.

3.16 LCD DMA Frame Buffer 1 Base Address Register 1 (LCDDMAFB1BAR1)

The LCD DMA frame buffer 1 base address register 1 is shown in Figure 25 and described in Table 20.

Figure 25. LCD DMA Frame Buffer 1 Base Address Register 1 (LCDDMAFB1BAR1)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 20. LCD DMA Frame Buffer 1 Base Address Register 1 (LCDDMAFB1BAR1) Field Descriptions

Bit	Field	Value	Description
15-0	FB1_BASE1	0-FFFFh	Frame Buffer 1 Base Address pointer MSW.

3.17 LCD DMA Frame Buffer 1 Ceiling Address Register 0 (LCDDMAFB1CAR0)

The LCD DMA frame buffer 1 ceiling address register 0 is shown in Figure 26 and described in Table 21.

Figure 26. LCD DMA Frame Buffer 1 Ceiling Address Register 0 (LCDDMAFB1CAR0)

15	0
FB1_CEIL0	
RW-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 21. LCD DMA Frame Buffer 1 Ceiling Address Register 0 (LCDDMAFB1CAR0) Field Descriptions

Bit	Field	Value	Description
15-0	FB1_CEIL0	0-FFFFh	Frame Buffer 1 Ceiling Address pointer LSW; 2 LSBs are hardwired to be 00.

3.18 LCD DMA Frame Buffer 1 Ceiling Address Register 1 (LCDDMAFB1CAR1)

The LCD DMA frame buffer 1 ceiling address register 1 is shown in Figure 27 and described in Table 22.

Figure 27. LCD DMA Frame Buffer 1 Ceiling Address Register 1 (LCDDMAFB1CAR1)

15	0
FB1_CEIL1	
RW-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 22. LCD DMA Frame Buffer 1 Ceiling Address Register 1 (LCDDMAFB1CAR1) Field Descriptions

Bit	Field	Value	Description
15-0	FB1_CEIL1	0-FFFFh	Frame Buffer 1 Ceiling Address pointer MSW.

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