TMS320DM36x Digital Media System-on-Chip (DMSoC)
Video Processing Back End (VPBE)

User's Guide

Literature Number: SPRUFG9C
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About This Manual

Describes the operation of the Video Processing Back End in the TMS320DM36x Digital Media System-on-Chip (DMSoC).

Notational Conventions

This document uses the following conventions.

- Hexadecimal numbers are shown with the suffix h. For example, the following number is 40 hexadecimal (decimal 64): 40h.
- Registers in this document are shown in figures and described in tables.
  - Each register figure shows a rectangle divided into fields that represent the fields of the register. Each field is labeled with its bit name, its beginning and ending bit numbers above, and its read/write properties below. A legend explains the notation used for the properties.
  - Reserved bits in a register figure designate a bit that is used for future device expansion.

Related Documentation From Texas Instruments

The following documents describe the TMS320DM36x Digital Media System-on-Chip (DMSoC). Copies of these documents are available on the internet at www.ti.com.

SPRUFG5 — ***TMS320DM365 Digital Media System-on-Chip (DMSoC) ARM Subsystem Reference Guide*** This document describes the ARM Subsystem in the TMS320DM36x Digital Media System-on-Chip (DMSoC). The ARM subsystem is designed to give the ARM926EJ-S (ARM9) master control of the device. In general, the ARM is responsible for configuration and control of the device; including the components of the ARM Subsystem, the peripherals, and the external memories.

SPRUFG8 — ***TMS320DM36x Digital Media System-on-Chip (DMSoC) Video Processing Front End (VPFE) Users Guide*** This document describes the Video Processing Front End (VPFE) in the TMS320DM36x Digital Media System-on-Chip (DMSoC).

SPRUFG9 — ***TMS320DM36x Digital Media System-on-Chip (DMSoC) Video Processing Back End (VPBE) Users Guide*** This document describes the Video Processing Back End (VPBE) in the TMS320DM36x Digital Media System-on-Chip (DMSoC).

SPRUFH0 — ***TMS320DM36x Digital Media System-on-Chip (DMSoC) 64-bit Timer Users Guide*** This document describes the operation of the software-programmable 64-bit timers in the TMS320DM36x Digital Media System-on-Chip (DMSoC).

SPRUFH1 — ***TMS320DM36x Digital Media System-on-Chip (DMSoC) Serial Peripheral Interface (SPI) Users Guide*** This document describes the serial peripheral interface (SPI) in the TMS320DM36x Digital Media System-on-Chip (DMSoC). The SPI is a high-speed synchronous serial input/output port that allows a serial bit stream of programmed length (1 to 16 bits) to be shifted into and out of the device at a programmed bit-transfer rate. The SPI is normally used for communication between the DMSoC and external peripherals. Typical applications include an interface to external I/O or peripheral expansion via devices such as shift registers, display drivers, SPI EPROMs and analog-to-digital converters.

SPRUFH2 — ***TMS320DM36x Digital Media System-on-Chip (DMSoC) Universal Asynchronous Receiver/Transmitter (UART) Users Guide*** This document describes the universal asynchronous receiver/transmitter (UART) peripheral in the TMS320DM36x Digital Media System-on-Chip (DMSoC). The UART peripheral performs serial-to-parallel conversion on data received from a peripheral device, and parallel-to-serial conversion on data received from the CPU.

SPRUFH3 — ***TMS320DM36x Digital Media System-on-Chip (DMSoC) Inter-Integrated Circuit (I2C) Peripheral Users Guide*** This document describes the inter-integrated circuit (I2C) peripheral in the TMS320DM36x Digital Media System-on-Chip (DMSoC). The I2C peripheral provides an interface between the DMSoC and other devices compliant with the I2C-bus specification and connected by way of an I2C-bus.

SPRUFH5 — ***TMS320DM36x Digital Media System-on-Chip (DMSoC) Multimedia Card (MMC)/Secure Digital (SD) Card Controller Users Guide*** This document describes the multimedia card (MMC)/secure digital (SD) card controller in the TMS320DM36x Digital Media System-on-Chip (DMSoC).

SPRUFH6 — ***TMS320DM36x Digital Media System-on-Chip (DMSoC) Pulse-Width Modulator (PWM) Users Guide*** This document describes the pulse-width modulator (PWM) peripheral in the TMS320DM36x Digital Media System-on-Chip (DMSoC).

SPRUFH7 — ***TMS320DM36x Digital Media System-on-Chip (DMSoC) Real-Time Out (RTO) Controller Users Guide*** This document describes the Real Time Out (RTO) controller in the TMS320DM36x Digital Media System-on-Chip (DMSoC).

SPRUFH8 — ***TMS320DM36x Digital Media System-on-Chip (DMSoC) General-Purpose Input/Output (GPIO) Users Guide*** This document describes the general-purpose input/output (GPIO) peripheral in the TMS320DM36x Digital Media System-on-Chip (DMSoC). The GPIO peripheral provides dedicated general-purpose pins that can be configured as either inputs or outputs.

SPRUFH9 — ***TMS320DM36x Digital Media System-on-Chip (DMSoC) Universal Serial Bus (USB) Controller Users Guide*** This document describes the universal serial bus (USB) controller in the TMS320DM36x Digital Media System-on-Chip (DMSoC). The USB controller supports data throughput rates up to 480 Mbps. It provides a mechanism for data transfer between USB devices and also supports host negotiation.

SPRUFI0 — ***TMS320DM36x Digital Media System-on-Chip (DMSoC) Enhanced Direct Memory Access (EDMA) Controller Users Guide*** This document describes the operation of the enhanced direct memory access (EDMA3) controller in the TMS320DM36x Digital Media System-on-Chip (DMSoC). The EDMA controller's primary purpose is to service user-programmed data transfers between two memory-mapped slave endpoints on the DMSoC.

SPRUFI1 — ***TMS320DM36x Digital Media System-on-Chip (DMSoC) Asynchronous External Memory Interface (EMIF) Users Guide*** This document describes the asynchronous external memory interface (EMIF) in the TMS320DM36x Digital Media System-on-Chip (DMSoC). The EMIF supports a glueless interface to a variety of external devices.

SPRUFI2 — ***TMS320DM36x Digital Media System-on-Chip (DMSoC) DDR2/Mobile DDR (DDR2/mDDR) Memory Controller Users Guide*** This document describes the DDR2/mDDR memory controller in the TMS320DM36x Digital Media System-on-Chip (DMSoC). The DDR2/mDDR memory controller is used to interface with JESD79-2A standard compliant DDR2 SDRAM and mobile DDR devices.

SPRUFI3 — ***TMS320DM36x Digital Media System-on-Chip (DMSoC) Multibuffered Serial Port Interface (McBSP) User's Guide*** This document describes the operation of the multibuffered serial host port interface in the TMS320DM36x Digital Media System-on-Chip (DMSoC). The primary audio modes that are supported by the McBSP are the AC97 and IIS modes. In addition to the primary audio modes, the McBSP supports general serial port receive and transmit operation.

SPRUFI4 — ***TMS320DM36x Digital Media System-on-Chip (DMSoC) Universal Host Port Interface (UHPI) User's Guide*** This document describes the operation of the universal host port interface in the TMS320DM36x Digital Media System-on-Chip (DMSoC).

SPRUFI5 — ***TMS320DM36x Digital Media System-on-Chip (DMSoC) Ethernet Media Access Controller (EMAC) User's Guide*** This document describes the operation of the ethernet media access controller face in the TMS320DM36x Digital Media System-on-Chip (DMSoC).

SPRUFI7 — ***TMS320DM36x Digital Media System-on-Chip (DMSoC) Analog to Digital Converter (ADC) User's Guide*** This document describes the operation of the analog to digital conversion in the TMS320DM36x Digital Media System-on-Chip (DMSoC).

SPRUFI8 — ***TMS320DM36x Digital Media System-on-Chip (DMSoC) Key Scan User's Guide*** This document describes the key scan peripheral in the TMS320DM36x Digital Media System-on-Chip (DMSoC).

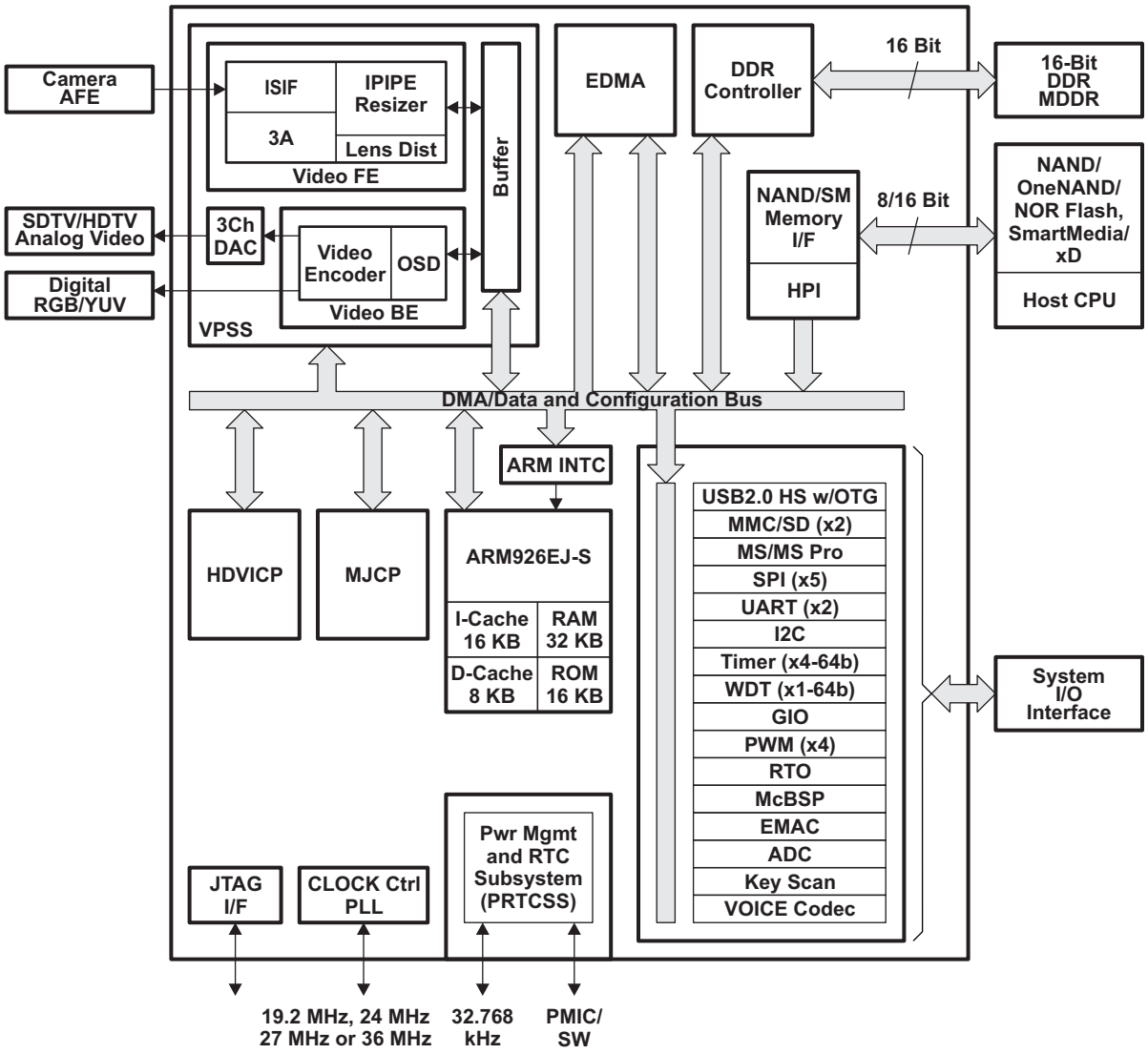
SPRUFI9 — ***TMS320DM36x Digital Media System-on-Chip (DMSoC) Voice Codec User's Guide*** This document describes the voice codec peripheral in the TMS320DM36x Digital Media System-on-Chip (DMSoC). This module can access ADC/DAC data with internal FIFO (Read FIFO/Write FIFO). The CPU communicates to the voice codec module using 32-bit-wide control registers accessible via the internal peripheral bus.

SPRUFJ0 — ***TMS320DM36x Digital Media System-on-Chip (DMSoC) Power Management and Real-Time Clock Subsystem (PRTCSS) User's Guide*** This document provides a functional description of the Power Management and Real-Time Clock Subsystem (PRTCSS) in the TMS320DM36x Digital Media System-on-Chip (DMSoC) and PRTC interface (PRTCIF).

Video Processing Back End

TMS320DM36x is a highly integrated, programmable platform for digital still/video cameras and other mobile imaging devices. Designed to offer camera manufacturers the ability to produce affordable DSC products with high picture quality, the device combines programmable image processing capability with a highly integrated imaging peripheral set. The device contains an ARM9 RISC CPU, a proprietary DSP-based imaging co-processor subsystem, and a powerful video processing subsystem. Together, they enable device manufacturers to implement high-speed hardware enabled image pipelines as well as their own proprietary image processing algorithms in software. The device also enables seamless interface to many external display devices required for a complete digital camera digital implementation via the Video Processing Back End Subsystem or VPBE. The interface is flexible enough to support various types of digital as well as analog (NTSC/PAL) displays. A block diagram is shown in Figure 1.

Figure 1. Functional Block Diagram

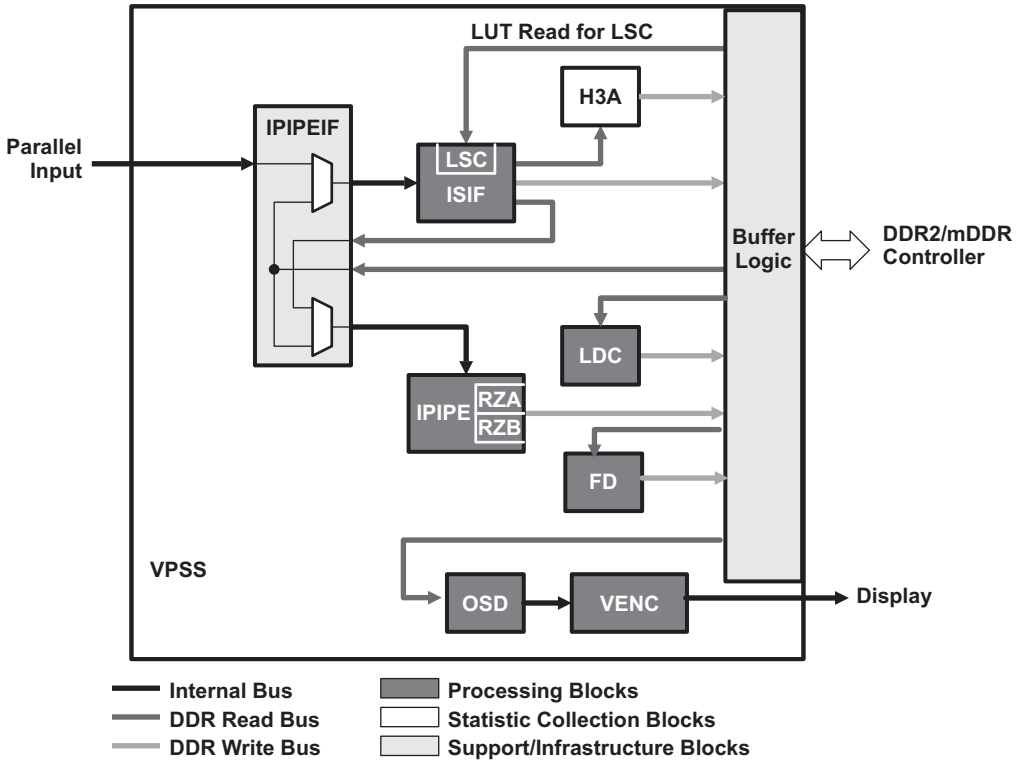


1 Purpose of the Video Processing Back End

The device contains a video processing subsystem (VPSS) that provides an input interface (video processing front end or VPFE) for external imaging peripherals such as image sensors, video decoders, etc., and an output interface, Video Processing Back End (VPBE) for display devices, such as analog SDTV displays, digital LCD panels, HDTV video encoders, etc.

In addition to these peripherals, there is a set of common buffer logic/memory and DMA control to ensure efficient use of the DDR2/mDDR burst bandwidth. The shared buffer logic/memory is a unique block that is tailored for seamlessly integrating the VPSS into an image/video processing system. It acts as the primary source or sink to all the VPFE and VPBE modules that are either requesting or transferring data from/to DDR2/mDDR. In order to efficiently utilize the external DDR2/mDDR bandwidth, the shared buffer logic/memory interfaces with the DMA system via a high bandwidth bus (64-bit wide). The shared buffer logic/memory also interfaces with all the VPFE and VPBE modules via a 128-bit wide bus. It is imperative that the VPSS utilize DDR2/mDDR bandwidth efficiently due to both its large bandwidth requirements and the real-time requirements of the VPSS modules.

Figure 2. Video Processing Subsystem Block Diagram



1.1 Features

The video processing back-end (VPBE) block is comprised of the on-screen display (OSD) and the video encoder (VENC) modules. Together, these modules provide the device with a powerful and flexible back-end display interface. These are described below:

- The on-screen display (OSD) graphic accelerator manages display data in various formats for several types of hardware display windows and handles the blending of the display windows into a single display frame, which is then output by the video encoder module.
- The video encoder (VENC) takes the display frame from the OSD and formats it into the desired output format and output signals, including data, clocks, sync, etc. required to interface to display devices. The VENC consists of three primary sub-blocks:
  - The analog video encoder generates the signaling, including video D/A conversion, to interface to NTSC/PAL television displays.
  - The digital LCD controller supports interfaces to various digital LCD display formats as well as standard digital YUV outputs to interface to HD video encoders and/or DVI/HDMI interface devices.
  - The timing generator to generate the specific timing required for analog video output as well as various digital video output modes.

1.1.1 On-Screen Display (OSD) Features

The primary function of the OSD module is to gather and blend video data and bitmap data and pass it to the video encoder (VENC) in YCbCr format. The video and bitmap data is read from external DDR2/mDDR memory. The OSD is programmed via control and parameter registers. Following are the primary features that are supported by the OSD:

- Support two video windows and two OSD bitmapped windows that can be displayed simultaneously (VIDWIN0,VIDWIN1 and OSDWIN0,OSDWIN1)
- Video windows support YCbCr data in 422 and 420 format from external memory, with the ability to interchange the order of the CbCr component in the 32-bit word
- OSD bitmap windows support ½/4/8 bit width index data of color palette

- In addition, one OSD bitmap window at a time can be configured to one of the following:
  - YUV422 (same as video data)
  - RGB format data in 16-bit mode (R=5bit, G=6bit, B=5bit)
  - 24-bit mode (each R/G/B=8bit) with pixel level blending with video windows
- Programmable color palette with the ability to select between a RAM and ROM table with support for 256 colors.
- Support for two ROM tables, one of which can be selected at a given time
- Separate enable/disable control for each window
- Programmable width, height, and base starting coordinates for each window
- External memory address and offset registers for each window
- Support for x2 and x4 zoom in both the horizontal and vertical direction
- Pixel-level blending/transparency/blinking attributes can be defined for OSDWIN0 when OSDWIN1 is configured as an attribute window for OSDWIN0
- Support for blinking intervals to the attribute window
- Ability to select either field or frame mode for the windows (interlaced/progressive)
- An eight-step blending process between the bitmap and video windows
- Transparency support for the bitmap and video data (when a bitmap pixel is zero, there will be no blending for that corresponding video pixel)
- Ability to resize from VGA to NTSC/PAL (640x480 to 720x576) for both the OSD and video windows
- Horizontal rescaling x1.5 is supported
- Support for a rectangular cursor window and a programmable background color selection
- The width, height, and color of the cursor is selectable
- The display priority is: Rectangular-Cursor > OSDWIN1 > OSDWIN0 > VIDWIN1 > VIDWIN0 > background color
- Support for attenuation of the YCbCr values for the REC601 standard.

The following restrictions exist in the OSD module:

- If the vertical resize filter is enabled for either of the video windows, the maximum horizontal window dimension cannot be greater than 1024 currently. This is due to the limitation in the size of the line memory.
- It is not possible to use both of the CLUT ROMs at the same time. However, a window can use RAM while another uses ROM.

1.1.2 Video Encoder (VENC) Features

The VENC/DLCD consists of three major blocks: a) the video encoder that generates analog video output, b) the digital LCD controller that generates digital RGB/YCbCr data output and timing signals, and c) the timing generator.

The analog video encoder features are described below

- Master clock Input-27MHz for NTSC/PAL/525p/625p
- Master clock Input-74.25MHz for 720p/1080i
- SDTV Support
  - Composite NTSC-M, PAL-B/D/G/H/I
  - S-Video (Y/C)
  - Component YPbPr (SMPTE/EBU N10, Betacam, MII)
  - RGB
  - Non-Interlace
  - CGMS/WSS attribute insertion
  - Line 21 Closed caption data encoding
  - Chroma low-pass filter 1.5 MHz/3 MHz
  - Programmable SC-H phase
- HDTV Support

  - Progressive Output (525p/625p/720p) and Interlaced Output for 1080i
  - HD Output 1080i (SMPTE-274M)and 720p (SMPTE-296M)
  - Component YPbPr
  - RGB
  - CGMS/WSS attribute insertion
- Three 10-bit D/A converters (27 MHz)
- Optional 7.5% pedestal
- 16-235/0-255 input amplitude selectable
- Programmable luma delay
- Master/slave operation
- Internal color bar generation (100%/75%)

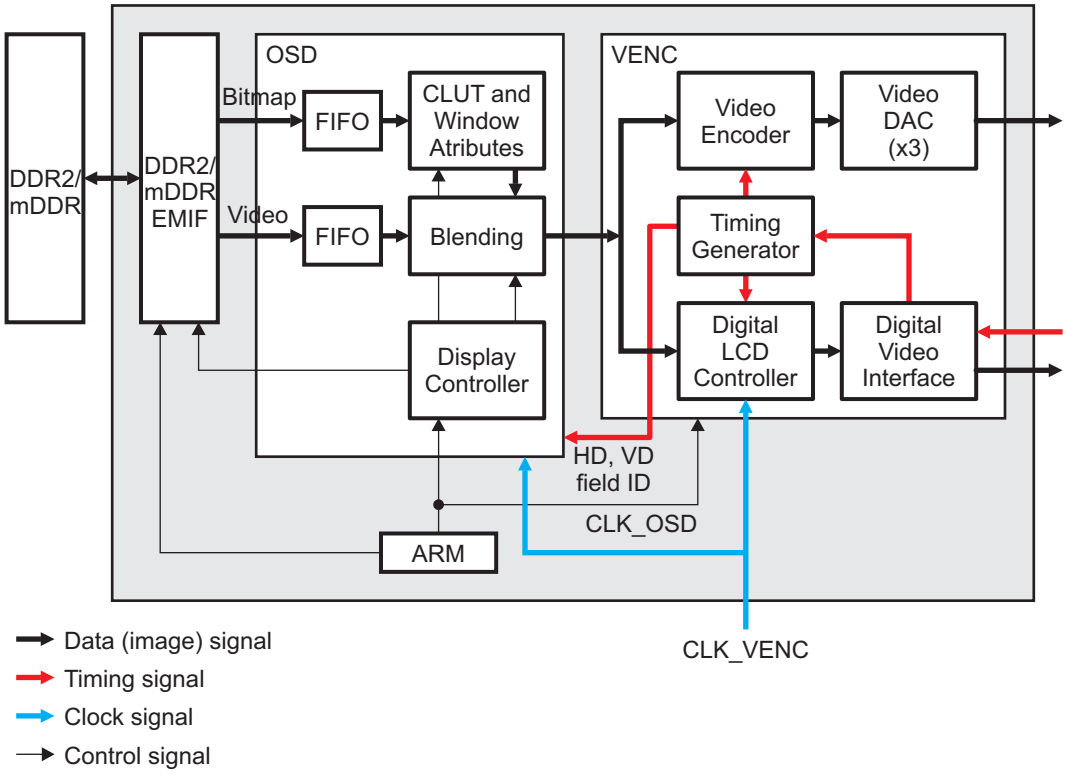
The digital LCD interface features are described below

- Programmable DCLK
- Various output formats
  - YCbCr 16-bit
  - YCbCr 8-bit
  - ITU-R BT. 656
  - Parallel RGB (24 bit)
  - Serial RGB
- Low-pass filter for digital RGB output
- Programmable timing generator
- Master/slave operation
- Internal color bar generation (100%/75%)
- 8-bit programable gamma correction

1.2 Functional Block Diagram

Figure 3 shows a high-level functional block diagram of the VPBE functional blocks, along with the different data flow paths.

Figure 3. Video Processing Back End Block Diagram



1.3 Supported Use Case Statement

The VPBE supports image (2-D window) compositing and blending from data stored in DDR2/mDDR memory in various display formats by the OSD module and then data formatting and conversion for display to analog SDTV/HDTV displays and to digital display devices various modes/formats by the VENC module. YUV output modes have minimal data processing applied and can be passed through directly from YUV input sources to VPFE. Digital RGB and LCD display formats are generated from the OSD's YUV422 output format, as are the analog outputs. The analog DAC outputs supports SDTV/HDTV with composite output format only.

1.4 Industry Standard(s) Compliance Statement

Analog television standards supported:

- SDTV
  - 525-line / 60 Hz (NTSC-M) or
  - 625-line / 50 Hz (PAL-B/D/G/H/I)
- HDTV
  - 525p
  - 625p
  - 720p (SMPTE-296M)
  - 1080i (SMPTE-274M)

2 Display Subsystem Environment

The VPBE signals are shown in Table 1 below. Note that these signals can take on different meanings

depending on the specific interface chosen. In addition, some of these signals are multiplexed with other SoC functions (GIO, PWM, etc.). Pin multiplexing is controlled via the PINMUX1 and PINMUX4 registers from the DM36x system module described in the *TMS320DM365 Digital Media System-on-Chip (DMSoC) ARM Subsystem Reference Guide* (SPRUFG5). The following sections will describe each of the scenarios supported.

Table 1. Interface Signals for Video Processing Back End

Name	Type	PU PD	Reset State	Description	Mux Control
VPBE Digital Signals					
YOUT7(R7)	out		in	Digital Video Out: VENC settings determine function	
YOUT6(R6)	out		in	Digital Video Out: VENC settings determine function	
YOUT5(R5)	out		in	Digital Video Out: VENC settings determine function	
YOUT4(R4)	out		in	Digital Video Out: VENC settings determine function	
YOUT3(R3)	out		in	Digital Video Out: VENC settings determine function	
YOUT2(G7)	out		in	Digital Video Out: VENC settings determine function	
YOUT1(G6)	out		in	Digital Video Out: VENC settings determine function	
YOUT0(G5)	out		in	Digital Video Out: VENC settings determine function	
COUT7(G4) / GIO092 / PWM0	inout		in	Digital Video Out: VENC settings determine function GIO: GIO[092], PWM0	PINMUX1[1:0].COUT_7
COUT6(G3) / GIO091 / PWM1	inout		in	Digital Video Out: VENC settings determine function GIO: GIO[091], PWM1	PINMUX1[3:2].COUT_6
COUT5(G2) / GIO090 / PWM2A / RTO0	inout		in	Digital Video Out: VENC settings determine function GIO: GIO[090], PWM2A, RTO0	PINMUX1[5:4].COUT_5
COUT4(B7) / GIO089 / PWM2B / RTO1	inout		in	Digital Video Out: VENC settings determine function GIO: GIO[089], PWM2B, RTO1	PINMUX1[7:6].COUT_4
COUT3(B6) / GIO088 / PWM2C / RTO2	inout		in	Digital Video Out: VENC settings determine function GIO: GIO[088], PWM2C, RTO2	PINMUX1[9:8].COUT_3
COUT2(B5) / GIO087 / PWM2D / RTO3	inout		in	Digital Video Out: VENC settings determine function GIO: GIO[087], PWM2D, RTO3	PINMUX1[11:10].COUT_2
COUT1(B4) / GIO086 / PWM3A / STTRIG	inout		in	Digital Video Out: VENC settings determine function GIO: GIO[086], PWM3A, STTRIG	PINMUX1[13:12].COUT_1
COUT0(B3) / GIO085 / PWM3B	inout		in	Digital Video Out: VENC settings determine function GIO: GIO[085], PWM3B	PINMUX1[15:14].COUT_0
HSYNC / GIO083	inout	PD	in	Video Encoder: Horizontal Sync GIO: GIO[083]	PINMUX1[16].HVSYNC
VSYNC / GIO084	inout	PD	in	Video Encoder: Vertical Sync GIO: GIO[084]	PINMUX1[16].HVSYNC

Table 1. Interface Signals for Video Processing Back End (continued)

Name	Type	PU PD	Reset State	Description	Mux Control
LCD_OE / GIO082	inout		in	Video Encoder: Signals valid Video Encoder output GIO: GIO[082]	PINMUX1[17].LCD_OE
LCD_FIELD / GIO081 / R2 / PWM3C	inout		in	Video Encoder: Field identifier for interlaced display formats GIO: GIO[070] Digital Video Out: R2 PWM3C	PINMUX1[19:18].LCD_FIELD
EXTCLK / GIO080 / B2 / PWM3D	inout	PD	in	Video Encoder: External clock input GIO: GIO[080] Digital Video Out: B2 PWM3D	PINMUX1[21:20].EXTCLK
GIO0033 / R1 / USBDRVVBUS /SPI2_SCS[0]	inout	PD	in	Video Encoder: General I/O GIO: GIO[033] Digital Video Out: R1 USBDRVVBUS SPI2_SCS[1]	PINMUX4[13:12].GIO33
GIO0032 / R0 / Rsvd/ SPI2_CLKS	inout	PD	in	Video Encoder: General I/O GIO: GIO[032] Digital Video Out: R0 Rsvd SPI2_CLKS	PINMUX4[11:10].GIO32
GIO0030 / G1 / Rsvd / SDI2_SIMO	inout	PD	in	Video Encoder: General I/O GIO: GIO[030] Digital Video Out: G1 Rsvd SDI2_SIMO	PINMUX4[7:6].GIO30
GIO0029 / G0 / Rsvd/ SPI1_SCS[0]	inout	PD	in	Video Encoder: General I/O GIO: GIO[029] Digital Video Out: G0 Rsvd SPI2_SCS[0]	PINMUX4[5:4].GIO29
GIO0028 / B1 / Rsvd/ SPI1_CLKS	inout	PD	in	Video Encoder: General I/O GIO: GIO[028] Digital Video Out: B1 Rsvd SPI1_CLKS	PINMUX4[3:2].GIO28
GIO0027 /B0 /SPI1_SCS[1] /SPI1_SOMI	inout	PD	in	Video Encoder: General I/O GIO: GIO[027] Digital Video Out: B0 SPI1_SCS[1] SPI1_SOMI	PINMUX4[1:0].GIO27
VPBE Analog Signals					
VREF	A inout			Video DAC: Reference voltage output (0.5 V, 0.1 μF to gnd)	
IREF	A inout			Video DAC: Reference current output (2400 Ω to gnd)	
IDACOUT	A inout			Video DAC: Current source input from DAC (2100 Ω to VFB)	
VFB	A inout			Video DAC: Amplifier feedback node. (2100 Ω to IDACOUT, 2150 Ω to TVOUT)	
TVOUT	A inout			Video DAC: DAC1 video output (2150 Ω to VFB, Output of 75 Ω driver, AC couple to TV)	
COMPY	A out			Video DAC: Analog video signal component output Y	
COMPPB	A out			Video DAC: Analog video signal component output Pb	
COMPPR	A out			Video DAC: Analog video signal component output Pr	

Table 1. Interface Signals for Video Processing Back End (continued)

Name	Type	PU PD	Reset State	Description	Mux Control
V_{DDA18_DAC}	PWR			Video DAC: Analog 1.8-V power	
V_{DDA12_DAC}	PWR			Video DAC: Analog 1.2-V power	
V_{SSA18_DAC}	GND			Video DAC: Analog 1.8-V ground	
V_{SSA12_DAC}	GND			Video DAC: Analog 1.2-V ground	

2.1 Analog Display Interface

The analog interface is used for driving NTSC/PAL/HDTV compatible television displays, video decoders, and other devices with NTSC/PAL/HDTV compatible display interfaces

2.1.1 Analog Display Signal Interface

Table 24 shows the VPBE analog display signals. For more details about the analog display signal interface, refer to the *TMS320DM365 Digital Media System-on-Chip (DMSoC) Data Manual* (SPRS457).

2.1.2 Analog Display Signal Interface Timing

This section describes master mode timings. For slave mode timings, please refer to Section 4.5.4.3.

2.1.2.1 Horizontal Timing

The timings, such as location of horizontal sync pulses, color burst position and active video position, are automatically calculated by hardware. Figure 4 shows horizontal timing characteristics. Table 3 shows the parameters of the timing chart. Each parameter is set to conform to standard but can be adjusted by user registers. Independent timing configurations can be available for CVBS and component/RGB output.

Figure 4. Horizontal Timing (SDTV/Progressive)

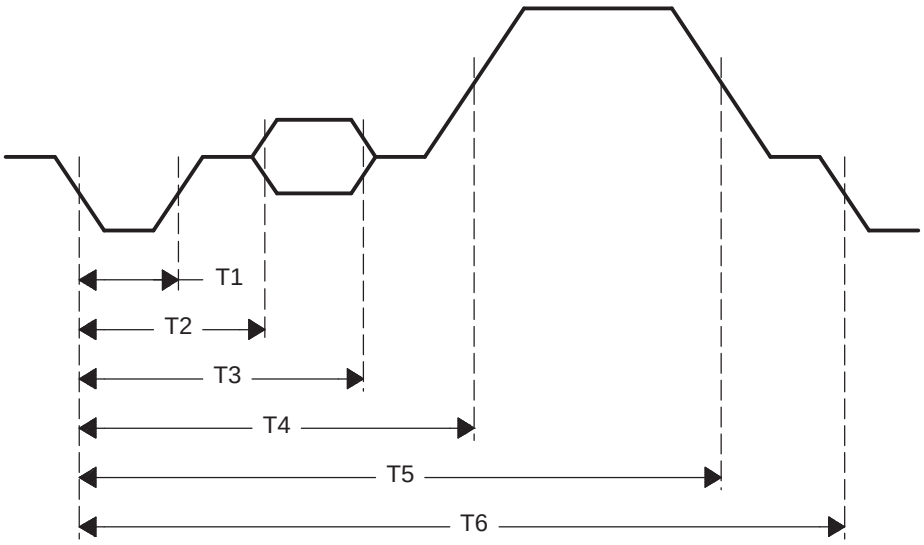


Table 2. Horizontal Timing Parameters (SDTV)

Parameter	Item	NTSC (1)	PAL (1)	CVBS Adjust	Comp. Adjust
T1	Horizontal sync pulse width	127	127	ETMG0.CLSW	ETMG2.MLSW
T2	H ref to burst start	141	151	ETMG1.CBST	N/A
T3	H ref to burst end	210	212	ETMG1.CBSE	N/A
T4	H ref to H blanking end	243	263	ETMG1.CLBI	ETMG3.MLBI

(1) Units are in ENC clocks.

Table 2. Horizontal Timing Parameters (SDTV) (continued)

Parameter	Item	NTSC (1)	PAL (1)	CVBS Adjust	Comp. Adjust
T5	H ref to H blanking start	1683	1703	ETMG1.CFPW	ETMG3.MFPW
T6	1H	1716	1728	-	-

Table 3. Horizontal Timing Parameters (Progressive)

Parameter	Item	525P (1)	625P (1)	CVBS Adjust	Comp. Adjust
T1	Horizontal sync pulse width	127	127	N/A	ETMG2.MLSW
T4	H ref to H blanking end	243	243	N/A	ETMG3.MLBI
T5	H ref to H blanking start	1683	1683	N/A	ETMG3.MFPW
T6	1H	858	864	-	-

(1) Units are in ENC clocks.

Figure 5. Horizontal Timing (1080I/720P)

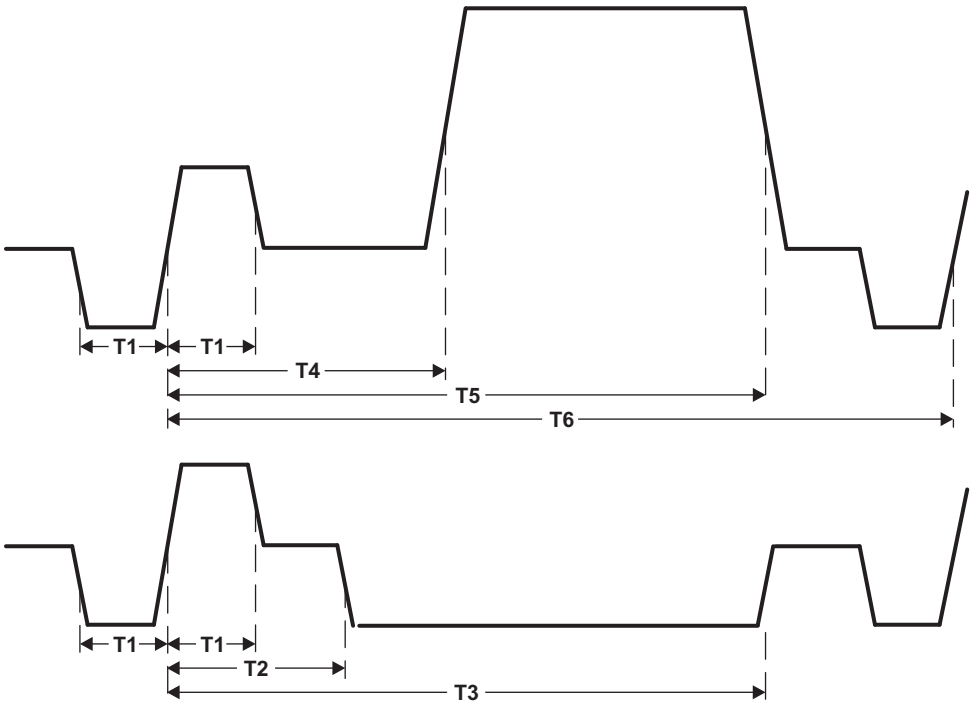


Table 4. Horizontal Timing Parameters (1080I/720P)

Parameter	Item	1080I (1)	720P (1)	CVBS Adjust	Comp. Adjust
T1	Horizontal sync pulse width	44	40	N/A	ETMG2.MLSW
T2	H ref to broad pulse start (vertical sync)	132	260	N/A	ETMG2.MEPW
T3	H ref to broad pulse end (vertical sync)	1012	1540	N/A	ETMG2.MFSW
T4	H ref to H blanking end	192	260	N/A	ETMG3.MLBI
T5	H ref to H blanking start	2112	1540	N/A	ETMG3.MFPW
T6	1H	2200+XH	1650+XH	-	-

(1) Units are in ENC clocks.

Table 5. HD Frame Rate

Format	Original H Interval	XH	Updated H Interval	Frame Rate
1080i	2200	0	2200	30 Hz
		440	2640	25 Hz
720p	1650	0	1650	60 Hz
		330	1980	50 Hz
		1650	3300	30 Hz
		2310	3960	25 Hz
		2475	4125	24 Hz

2.1.2.2 Horizontal Blanking Timing

Some pixels around the horizontal video blanking edge are clipped so that the output video has the proper blanking transition.

This feature is enabled by default but can be disabled by setting the parameter CVBS.CBLS to 1. Figure 6 shows the waveforms when blanking edge shaping is enabled and disabled. Table 6 shows the difference of T4 and T5 (see Figure 4 for T4 and T5).

Figure 6. Horizontal Blanking Shaping

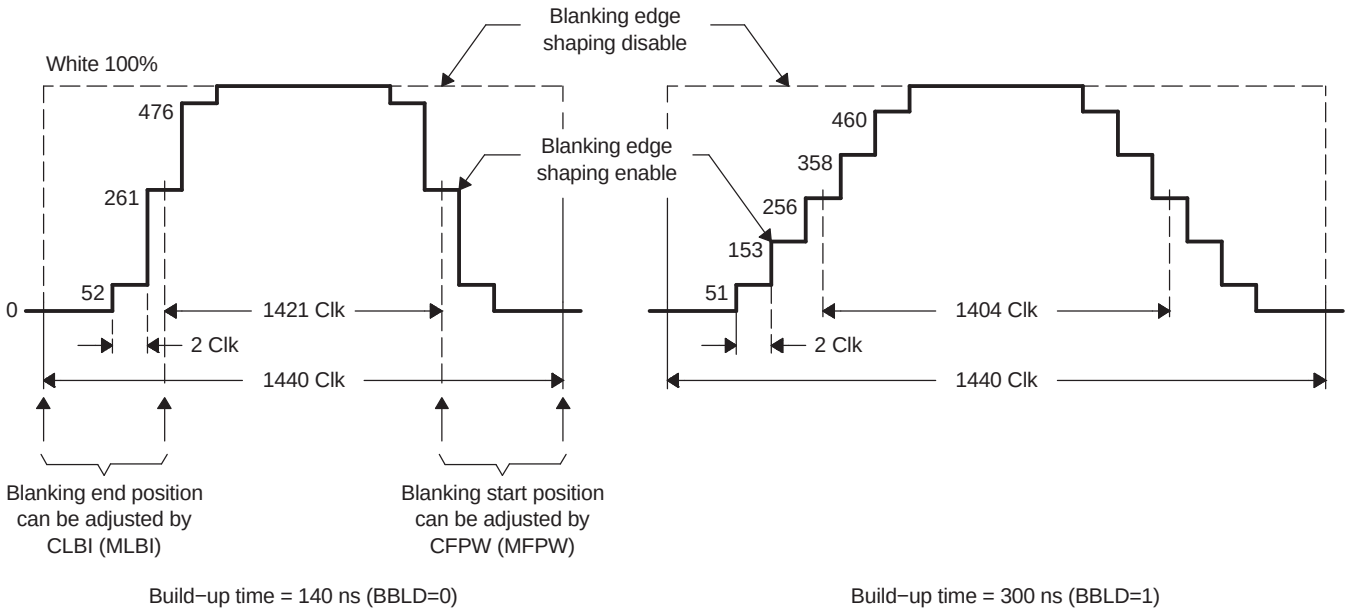


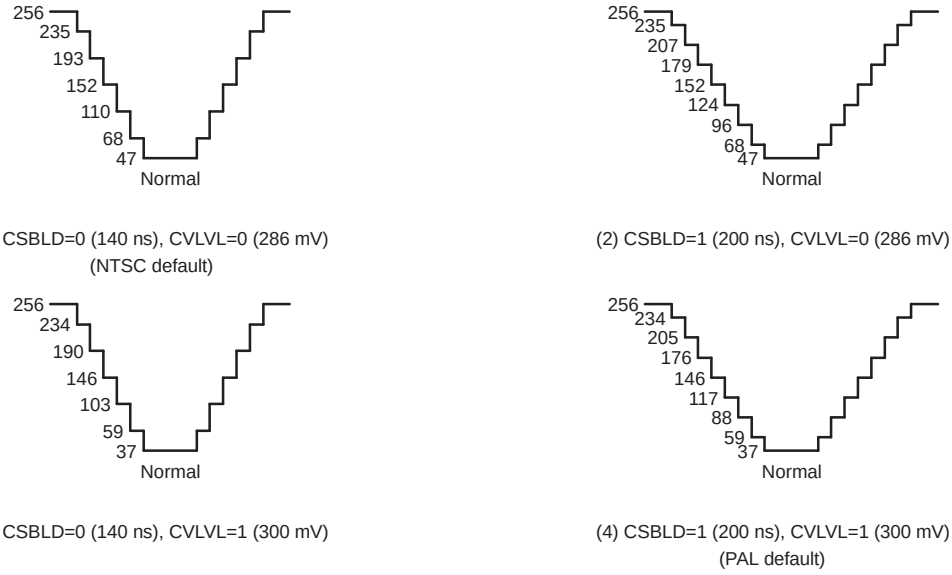
Table 6. Blanking Shaping On/Off

Parameter	NTSC		PAL	
	CVBS.CBLS = 0	CVBS.CBLS = 1	CVBS.CBLS = 0	CVBS.CBLS = 1
T4	252	243	282	263
T5	1673	1683	1686	1703

2.1.2.3 Horizontal Sync Timing

The detail waveform of horizontal sync pulse to be inserted on the luma signal is shown inFigure 7. The levels in Figure 7 are the internal digital values. The duration of each step is one ENC clock period. The register name in this figure is for CVBS output.

Figure 7. Sync Signal Detail Waveform (SDTV)



(1) CSBLD=0 (140 ns), CVLVL=0 (286 mV) (NTSC default)

(2) CSBLD=1 (200 ns), CVLVL=0 (286 mV)

(3) CSBLD=0 (140 ns), CVLVL=1 (300 mV)

(4) CSBLD=1 (200 ns), CVLVL=1 (300 mV) (PAL default)

2.1.2.4 Vertical Timing

The vertical timing is also controlled by hardware automatically for each mode (NTSC or PAL). Serration and equalization pulses are generated for appropriate lines. The color burst is automatically disabled on appropriate lines.

Figure 8 and Figure 9 show the vertical timing characteristics of NTSC and PAL.

Figure 10 and Figure 11 show the non-interlaced mode for NTSC and PAL. The non-interlaced mode is activated when VMOD.ITLC = 1. The line number in a field can be selected by VMOD.ITLCL, as shown in Table 7.

Table 7. Number of Lines for Each Scan Mode

VMOD.ITLC	VMOD.ITLCL	Line	
		NTSC	PAL
0	-	262.5	312.5
1	0	262	312
	1	263	313

In these figures, the color burst is denoted as |, ↑ or ↓ marks. For NTSC, | denotes the color burst position. For PAL, ↑ means +135°, while ↓ means -135° relative to U. For interlaced NTSC, the video encoder operation starts with the field I in master mode. For interlaced PAL, it starts with the field II.

Figure 8. NTSC Vertical Timing

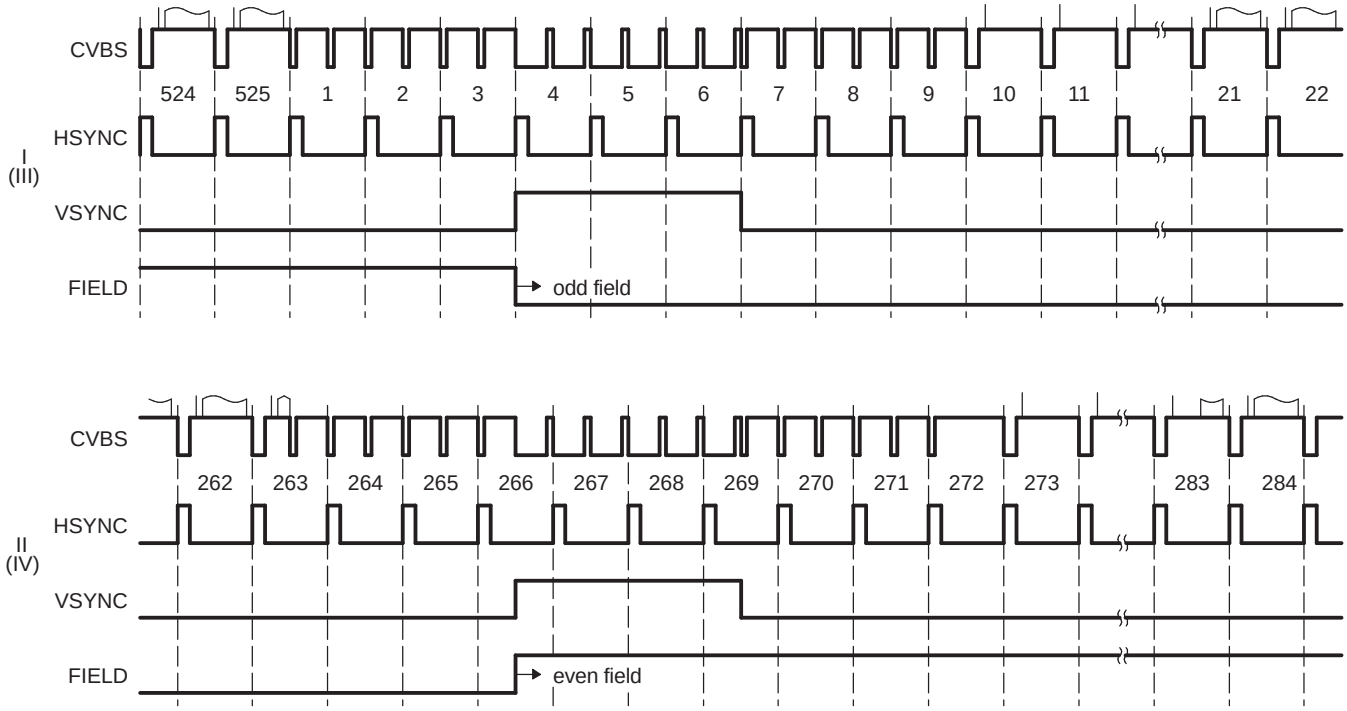


Figure 9. PAL Vertical Timing

Figure 10. Non-Interlaced NTSC (ITLC = 1, ITLCL = 0) Vertical Timing

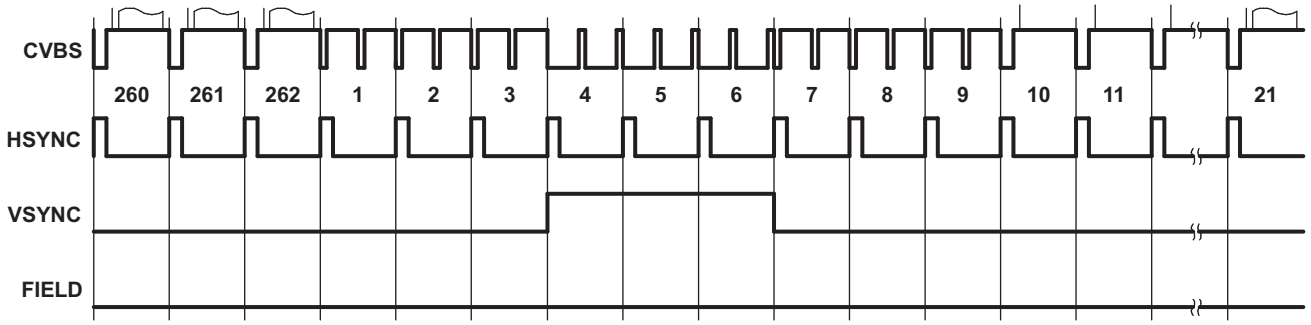


Figure 11. Non-Interlaced PAL (ITLC = 1, ITLCL = 0) Vertical Timing

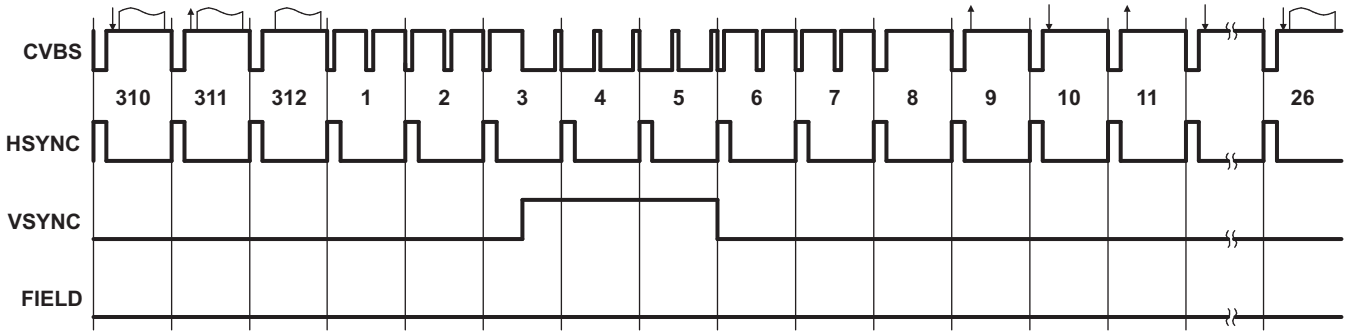


Figure 12. 525P Vertical Timing

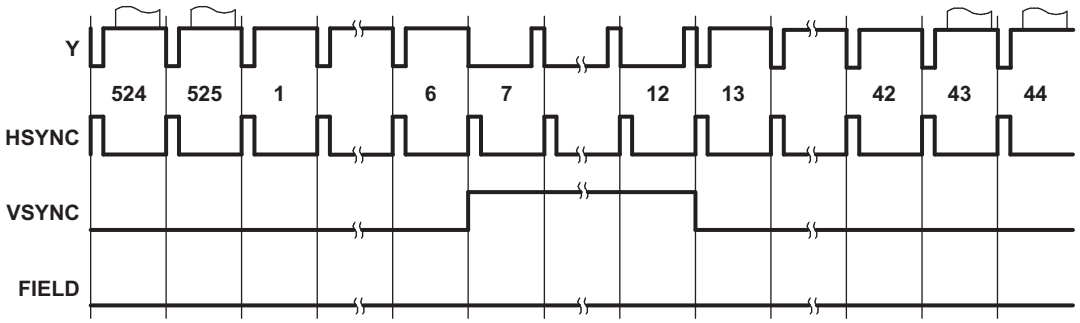


Figure 13. 625P Vertical Timing

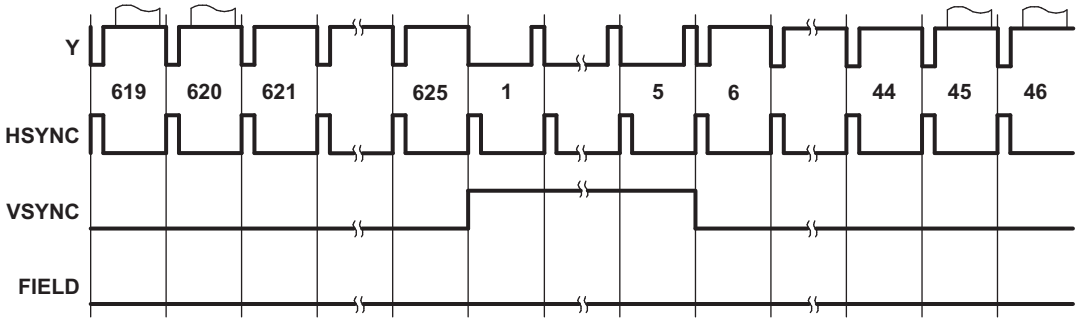


Figure 14. 1080I Vertical Timing

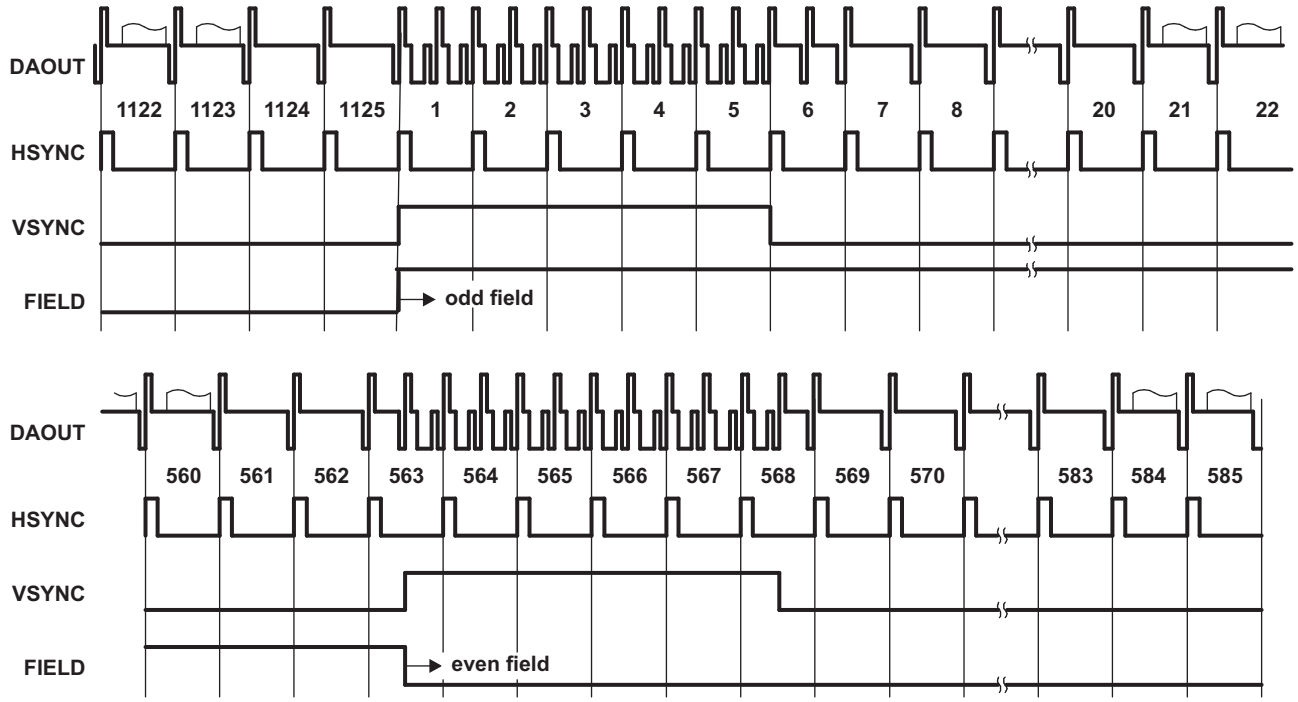
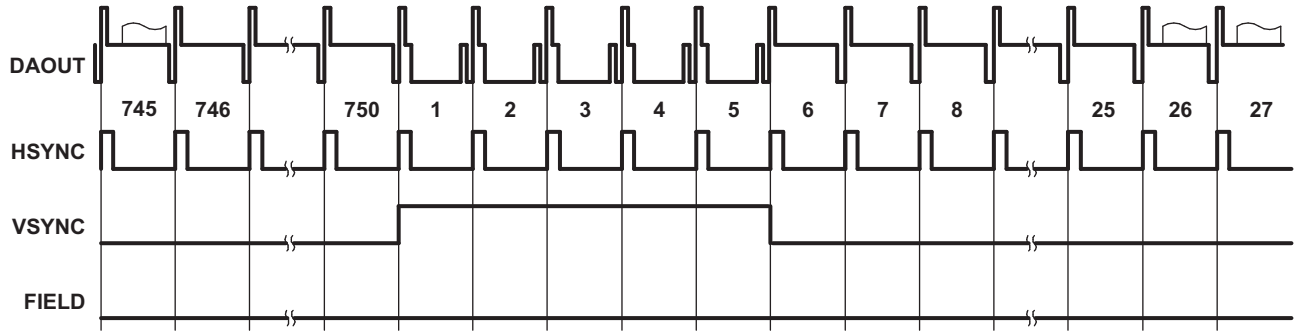


Figure 15. 720P Verical Timing



2.1.2.5 Internal Color Bar Output Level

The NTSC/PAL encoder can internally generate color bars. Setting VDPRO.CBMD = 1 enables the internal color bar generator. The VDPRO.CBTYP field switches the saturation of the color bar; 0 for 75%, 1 for 100%. Figure 16 and Figure 17 show the digital level of the video encoder when the internal color bar is enabled for each mode.

Figure 16. 100% Color Bar Output Level

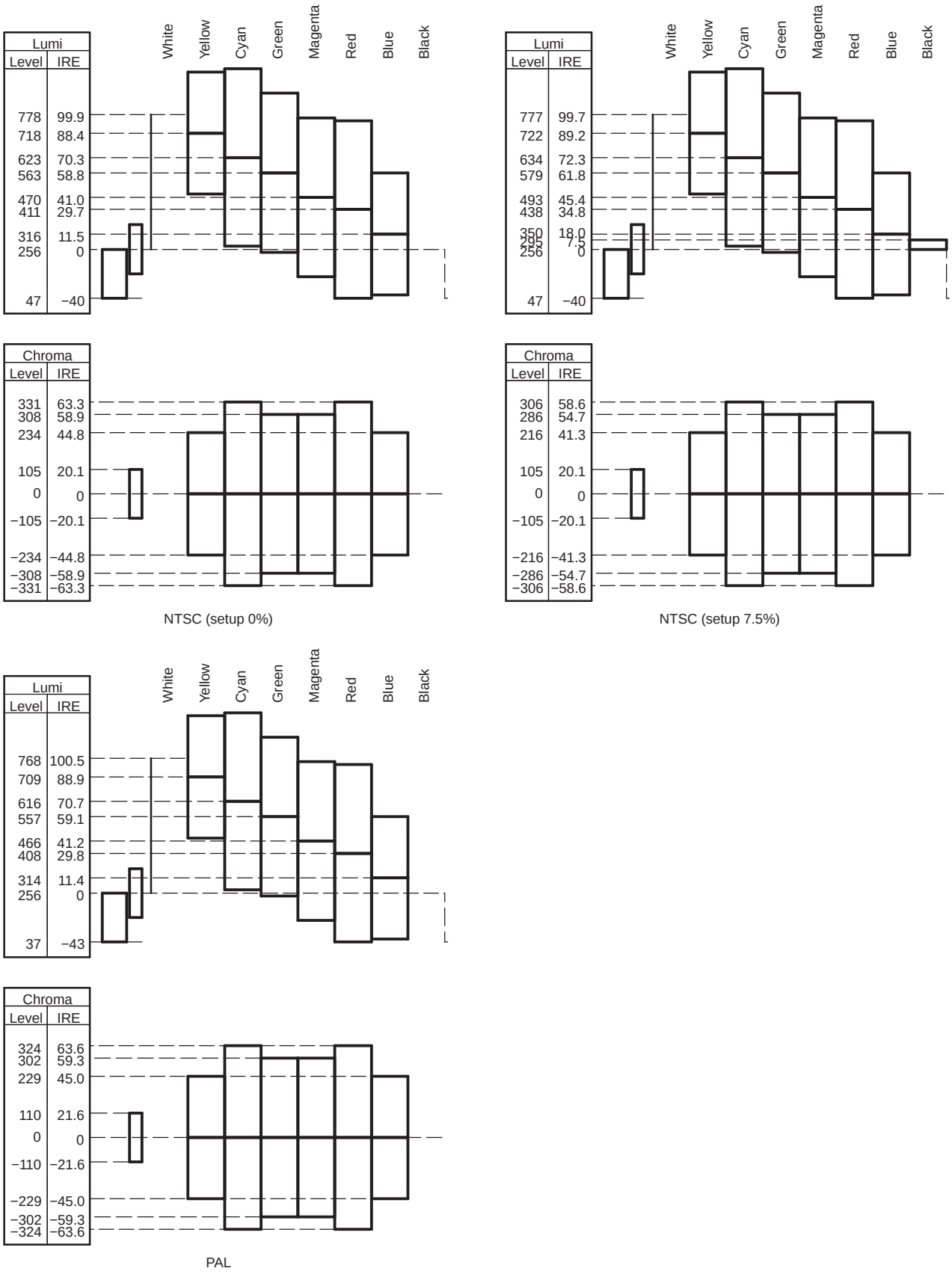
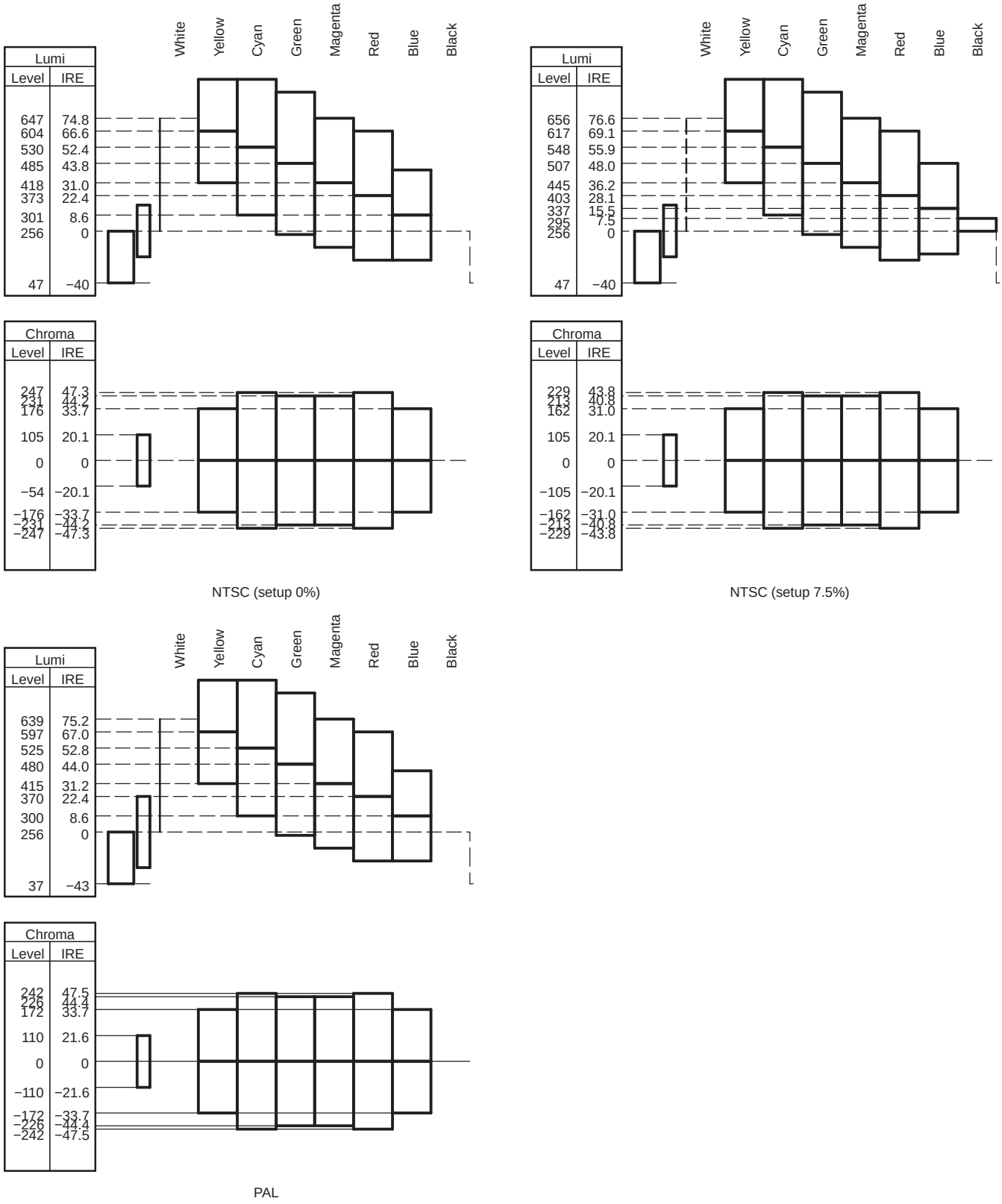


Figure 17. 75% Color Bar Output Level



2.2 Digital Display Interface

The digital display interface is used for driving various types of digital display devices.

Table 8. Digital Display Modes

VDMD	Mode	Description
0	YCC16	16-bit YCbCr output mode. Y and C are output separately on 16bit bus.
1	YCC8	8-bit YCbCr output mode. 422 YCbCr is time-multiplexed on the 8bit bus. Optionally supports ITU-R BT.656 output.
2	PRGB	Parallel RGB mode to output RGB separately. Optionally supports embedded sync output.
3	SRGB	Serial RGB mode to output RGB sequentially.

The digital image data output signals support multiple functions / interfaces, depending on the display mode selected. Table 9 describes these modes. Note that Parallel RGB mode with more than 16-bit RGB565 signals requires enabling pin multiplexing to support (i.e., for RGB888 mode).

Table 9. Signals for VPBE Digital Display Modes

Pin Name	YCC16	YCC8 / REC656	PRGB	SRGB
HSYNC GIO083	HSYNC	HSYNC	HSYNC	HSYNC
VSYNC GIO084	VSYNC	VSYNC	VSYNC	VSYNC
LCD_OE GIO082	As needed	As needed	As needed	As needed
LCD_FIELD GIO081, R2, PWM3C	As needed	As needed	As needed	As needed
EXTCLK GIO080, B2, PWM3D	As needed	As needed	As needed	As needed
VCLK GIO079	VCLK	VCLK	VCLK	VCLK
YOUT7(R7)	Y7	Y7, Cb7, Cr7	R7	DATA 7
YOUT6(R6)	Y6	Y6, Cb6, Cr6	R6	DATA 6
YOUT5(R5)	Y5	Y5, Cb5, Cr5	R5	DATA 5
YOUT4(R4)	Y4	Y4, Cb4, Cr4	R4	DATA 4
YOUT3(R3)	Y3	Y3, Cb3, Cr3	R3	DATA 3
YOUT2(G7)	Y2	Y2, Cb2, Cr2	G7	DATA 2
YOUT1(G6)	Y1	Y1, Cb1, Cr1	G6	DATA 1
YOUT0(G5)	Y0	Y0, Cb0, Cr0	G5	DATA 0
COUT7(G4) GIO092, PWM0	C7	LCD_AC	G4	LCD_AC
COUT6(G3) GIO091, PWM1	C6	LCD_OE	G3	LCD_OE
COUT5(G2) GIO090, PWM2A, RTO0	C5	BRIGHT	G2	BRIGHT
COUT4(B7) GIO089, PWM2B, RTO1	C4	PWM	B7	PWM
COUT3(B6) GIO088, PWM2C, RTO2	C3	CSYNC	B6	CSYNC

Table 9. Signals for VPBE Digital Display Modes (continued)

Pin Name	YCC16	YCC8 / REC656	PRGB	SRGB
COUT2(B5) GIO087, PWM2D, RTO3	C2	0	B5	-
COUT1(B4) GIO086, PWM3A, STTRIG	C1	0	B4	-
COUT0(B3) GIO085, PWM3B	C0	0	B3	DATA_8
GIO0033, R1	-	-	R1	-
GIO0032, R0	-	-	R0	-
GIO0030, G1	-	-	G1	-
GIO0029, G0	-	-	G0	-
GIO0028, B1	-	-	B1	-
GIO0027, B0	-	-	B0	-

2.2.1 YCC16 Signal Interface

In YCC16 mode, the Y (luma) signal is output to YOUT[7:0] at every VCLK rising edge, while Cb and Cr (chroma) are alternately multiplexed onto COUT[7:0]. The order of chroma output is controlled by YCCCTL.YCP. Data is only output when the LCD_OE signal is asserted. Otherwise the output signals are held low. Table 10 shows the interface connections for the YCC16 digital display interface.

Table 10. Interface Signals For YCC16 Digital Displays

Name	TYPE	PU PD	Reset State	Description	Fuction Control / Mux Control
YOUT7(R7)	inout		in	YOUT7 signal	VMOD.VDMD = 0
YOUT6(R6)	inout		in	YOUT6 signal	VMOD.VDMD = 0
YOUT5(R5)	inout		in	YOUT5 signal	VMOD.VDMD = 0
YOUT4(R4)	inout		in	YOUT4 signal	VMOD.VDMD = 0
YOUT3(R3)	inout		in	YOUT3 signal	VMOD.VDMD = 0
YOUT2(G7)	inout		in	YOUT2 signal	VMOD.VDMD = 0
YOUT1(G6)	inout		in	YOUT1 signal	VMOD.VDMD = 0
YOUT0(G5)	inout		in	YOUT0 signal	VMOD.VDMD = 0
COUT7(G4) / GIO092 / PWM0	inout		in	COUT7 signal	VMOD.VDMD = 0 PINMUX1[1:0], COUT_7 = 1
COUT6(G3) / GIO091 / PWM1	inout		in	COUT6 signal	VMOD.VDMD = 0 PINMUX1[3:2], COUT_6 = 1
COUT5(G2) / GIO090 / PWM2A / RTO0	inout		in	COUT5 signal	VMOD.VDMD = 0 PINMUX1[5:4], COUT_5 = 1
COUT4(B7) / GIO089 / PWM2B / RTO1	inout		in	COUT4 signal	VMOD.VDMD = 0 PINMUX1[7:6], COUT_4 = 1
COUT3(B6) / GIO088 / PWM2C / RTO2	inout		in	COUT3 signal	VMOD.VDMD = 0 PINMUX1[9:8], COUT_3 = 1

Table 10. Interface Signals For YCC16 Digital Displays (continued)

Name	TYPE	PU PD	Reset State	Description	Fuction Control / Mux Control
COUT2(B5) / GIO087 / PWM2D / RTO3	inout		in	COUT2 signal	VMOD.VDMD = 0 PINMUX1[11:10], COUT_2 = 1
COUT1(B4) / GIO086 / PWM3A STTRIG	inout		in	COUT1 signal	VMOD.VDMD = 0 PINMUX1[13:12], COUT_1 = 1
COUT0(B3) / GIO085 / PWM3B	inout		in	COUT0 signal	VMOD.VDMD = 0 PINMUX1[15:14], COUT_0 = 1
HSYNC / GIO083	inout	PD	in	Video encoder: Horizontal SYNC GIO: GIO[083]	PINMUX1[16], HVSYNC = 0
VSYNC / GIO084	inout	PD	in	Video encoder: Vertical SYNC GIO: GIO[084]	PINMUX1[16], HVSYNC = 0
LCD_OE / GIO082	inout		in	Video encoder: Signals valid Video Encoder output GIO: GIO[082]	PINMUX1[17], LCD_OE = 0 (if needed)
LCD_FIELD / GIO081 / R2 / PWM3C	inout		in	Video encoder: Field identifier for interlaced display formats GIO: GIO[081], Digital Video Out: R2, PWM3C	PINMUX1[19:18], LCD_FIELD = 1 (if needed)
EXTCLK / GIO080 / B2 / PWM3D	inout	PD	in	Video encoder: External clock input. GIO: GIO[080], Digital Video Out: B2, PWM3D	PINMUX1[21:20], EXTCLK = 1 (if needed)
VCLK / GIO079	inout		out L	Video encoder: Video output clock GIO: GIO[079]	PINMUX1[22], VCLK = 0

2.2.1.1 YCC16 Signal Interface Description

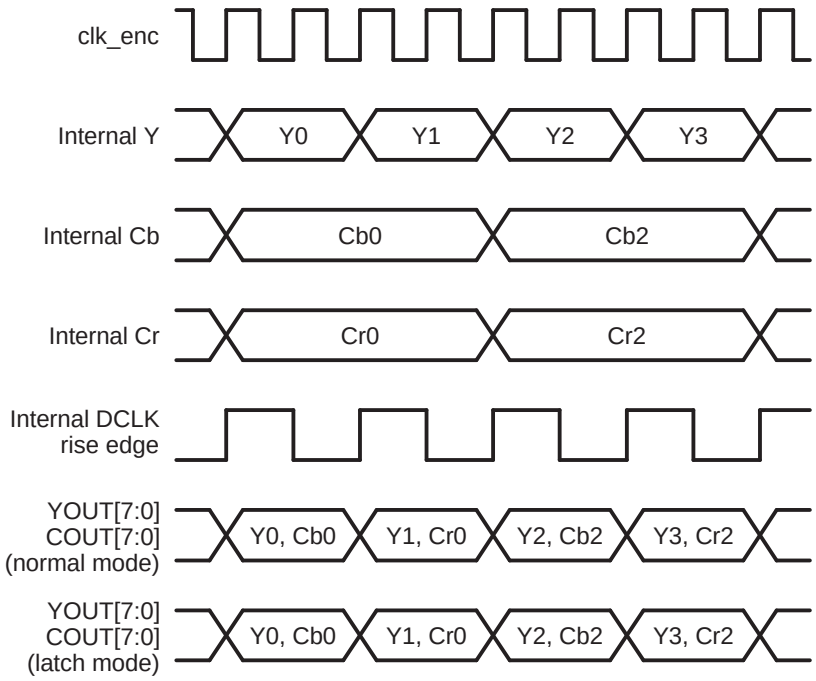
The YCC16 interface includes the 8-bit YOUT[7:0] and COUT[7:0] signals, along with the HSYNC, VSYNC, and VCLK signals. An optional EXTCLK input clock can be used if the internally generated VPBE clock is not fast enough.

Note that the YOUT/COUT busses can be swapped via the VIOCTL.YCSWAP register setting.

2.2.1.2 YCC16 Protocol and Data Formats

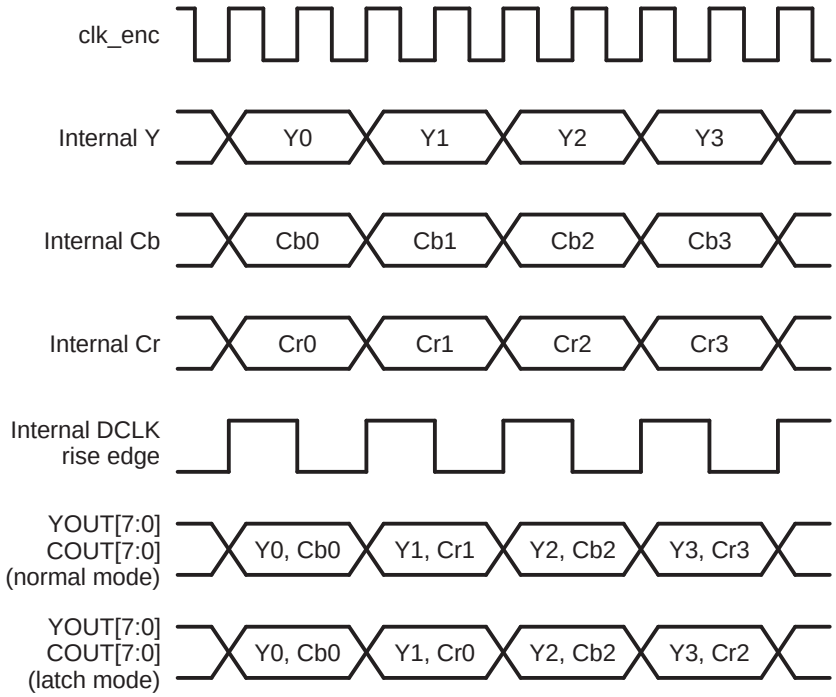
Figure 18 shows the output data sampling of the input YUV422 resolution signal from the OSD module for video windows. Video window input data is YUV422 format natively and RGB888 input data is chroma sub-sampled via boxcar averaging to YUV422 resolution.

Figure 18. YCC16 Output for Normal OSD Operation



The OSD also includes support for window data in bitmap format, either 1,2,4, or 8-bit resolution via a YUV Color Look Up Table (CLUT) or via RGB565 bitmap format. Data corresponding to bitmap pixels is in full YUV444 resolution and is overlaid onto the YUV422 resolution video window pixel output. In this case, chroma blurring can occur at the edge between bitmap windows and the rest of the OSD image. In normal operation, the chroma value output from VENC is the immediate value at the sampling time. However, to alleviate this chroma blurring, a “latch” mode is provided where the chroma output for the second pixel in a UV pair can be the data latched at the first pixel. The latch mode is enabled by setting YCCCTL.CHM to 1.

Figure 19. YCC16 Output When OSD Window in RGB565



Embedded Sync Insertion like ITU-R BT.656 is optionally available in YCC16 mode. Setting YCCCTL.R656 bit to 1 activates this mode. Figure 20 and Figure 21 show the horizontal and vertical timing in R656 mode respectively. The position that SAV/EAV code is inserted is determined by HSTART and HVALID registers. The V code toggles corresponding to VSTART and VVALID registers. The F code toggle position in even field of interlaced mode can be chosen from 0.5H ahead of VSYNC or 0.5H behind of VSYNC by YCCCTL.FID656 register bit field.

Figure 20. BT.656 Mode Horizontal Timing

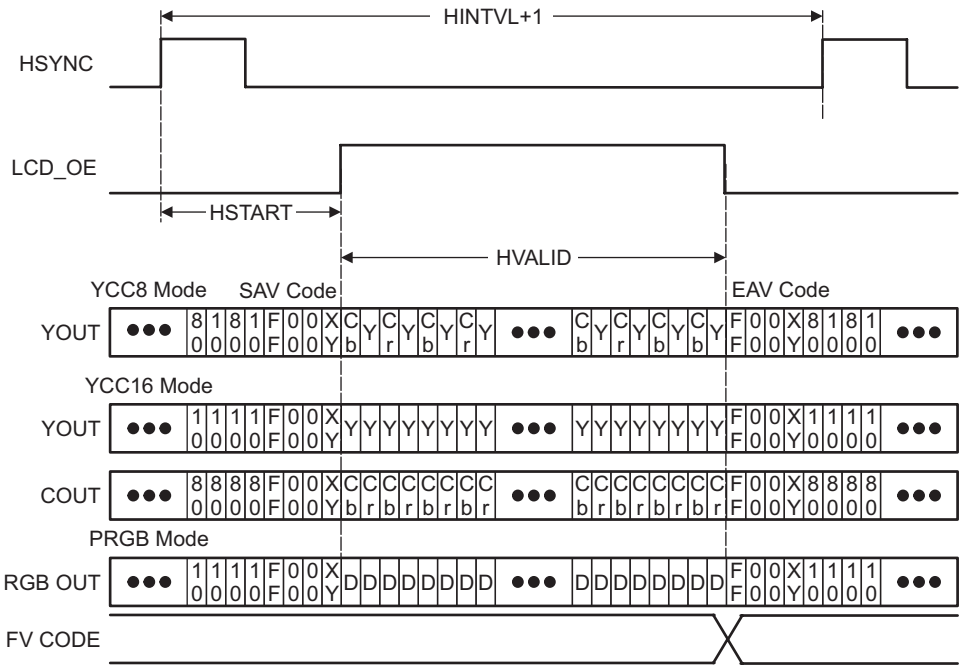
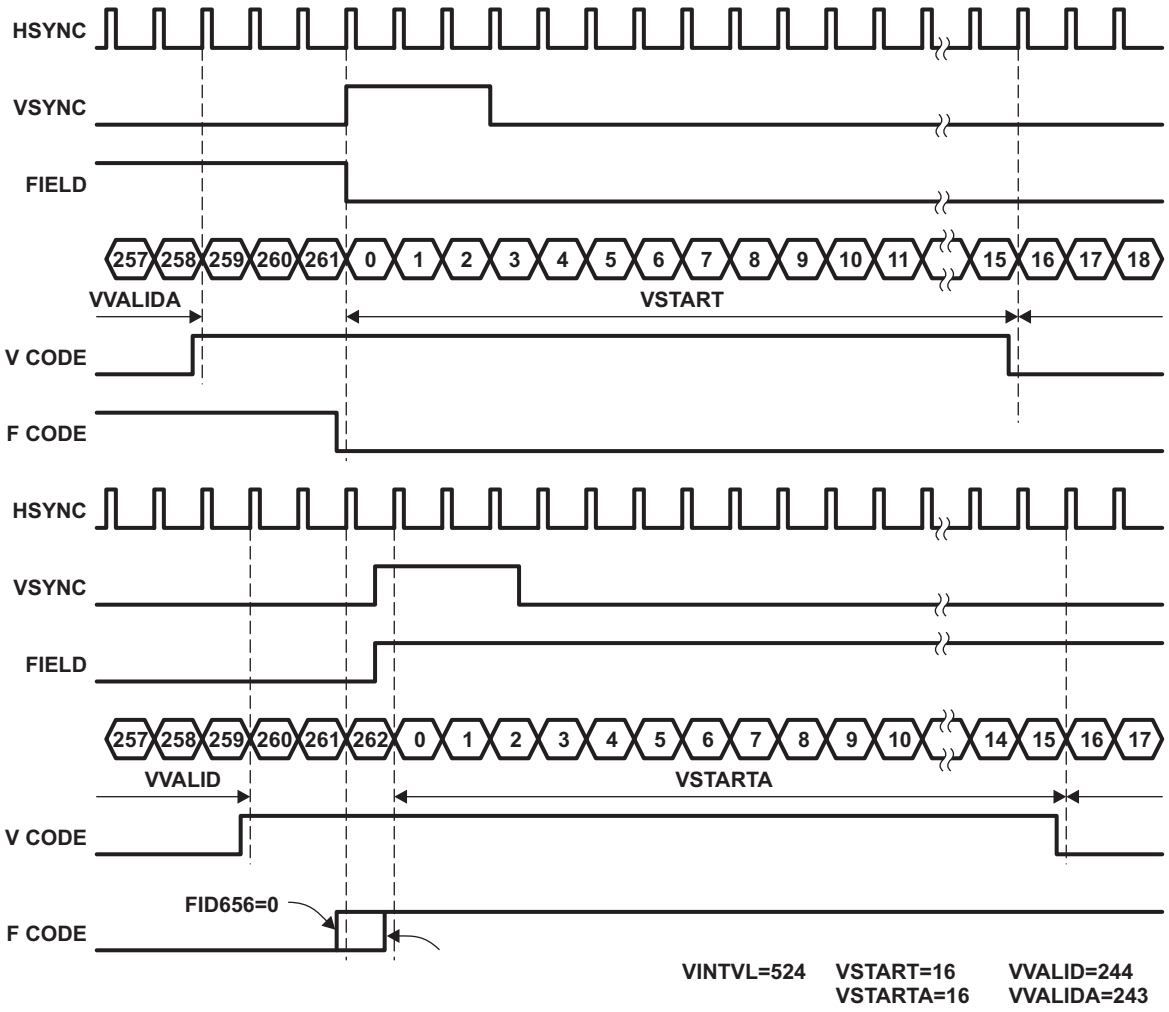


Figure 21. BT.656 Mode Vertical Timing



2.2.2 YCC8 Signal Interface, Including ITU-R-BT.656

In YCC8 mode, each component of the OSD YCbCr signal is alternately output from YOUT[7:0]. The default output order is Cb-Y-Cr-Y but this can be modified by YCCCTL.YCP. Table 11 shows the interface connections for the YCC8 digital display interface.

Table 11. Interface Signals For YCC8 Digital Displays

Name	TYPE	PU PD	Reset State	Description	Fuction Control / Mux Control
YOUT7(R7)	inout		in	YOUT7/COUT7 signal	VMOD.VDMD = 1 Use YOUT[7:0] for VENC.VIOCTL.YCSWAP = 0 Use COUT[7:0] for VENC.VIOCTL.YCSWAP = 1
YOUT6(R6)	inout		in	YOUT6/COUT6 signal	
YOUT5(R5)	inout		in	YOUT5/COUT5 signal	
YOUT4(R4)	inout		in	YOUT4/COUT4 signal	
YOUT3(R3)	inout		in	YOUT3/COUT3 signal	
YOUT2(G7)	inout		in	YOUT2/COUT2 signal	
YOUT1(G6)	inout		in	YOUT1/COUT1 signal	
YOUT0(G5)	inout		in	YOUT0/COUT0 signal	
COUT7(G4) / GIO92 / PWM0	inout		in	LCD_AC signal	VMOD.VDMD = 1 PINMUX1[1:0]. COUT_7 = 1 PINMUX1[3:2]. COUT_6 = 1 PINMUX1[5:4].COUT_5 = 1 PINMUX1[7:6]. COUT_4 = 1 PINMUX1[9:8]. COUT_3 = 1 PINMUX1[11:10]. COUT_2 = 1 PINMUX1[13:12]. COUT_1 = 1 PINMUX1[15:14]. COUT_0 = 1
COUT6(G3) / GIO91 / PWM1	inout		in	LCD_OE signal	
COUT5(G2) / GIO90 / PWM2A / RTO0	inout		in	BRIGHT signal	
COUT4(B7) / GIO89 / PWM2B / RTO1	inout		in	PWM signal	
COUT3(B6) / GIO88 / PWM2C / RTO2	inout		in	CSYNC signal	
COUT2(B5) / GIO87 / PWM2D / RTO3	inout		in	0	
COUT1(B4) / GIO86 / PWM3A STTRIG	inout		in	0	
COUT0(B3) / GIO85 / PWM3B	inout		in	0	
HSYNC / GIO083	inout	PD	in	Video encoder: Horizontal Sync GIO: GIO[083]	PINMUX1[16]. HVSYNC = 0
VSYNC / GIO084	inout	PD	in	Video encoder: Vertical Sync GIO: GIO[084]	PINMUX1[16]. HVSYNC = 0
LCD_OE / GIO082	inout		in	Video Encoder: Signals valid video encoder output GIO: GIO[082]	PINMUX1[17]. LCD_OE = 0 (if needed)

Table 11. Interface Signals For YCC8 Digital Displays (continued)

Name	TYPE	PU PD	Reset State	Description	Fuction Control / Mux Control
LCD_FIELD/ GIO081 / R2 / PWM3C	inout		in	Video encoder: Field identifier for interlaced display formats GIO: GIO[081], Digital video out: R2, PWM3C	PINMUX1[19:18]. LCD_FIELD = 1 (if needed)
EXTCLK / GIO080 / B2 / PWM3D	inout	PD	in	Video encoder: External clock input, used if clock rates > 27MHz are needed, e.g., 74.25 MHz for HDTV digital output. GIO: GIO[080], Digital video out: B2, PWM3D	PINMUX1[21:20]. EXTCLK = 1 (if needed)
VCLK / GIO079	inout		out L	Video encoder: Video output clock GIO: GIO[079]	PINMUX1[22], VCLK = 0

2.2.2.1 YCC8 Signal Interface Description

The YCC8 interface includes the 8-bit YOUT[7:0] or the 8-bit COUT[7:0] signals, along with the HSYNC, VSYNC, and VCLK signals. An optional EXTCLK input clock can be used if the internally generated VPBE clock is not fast enough .

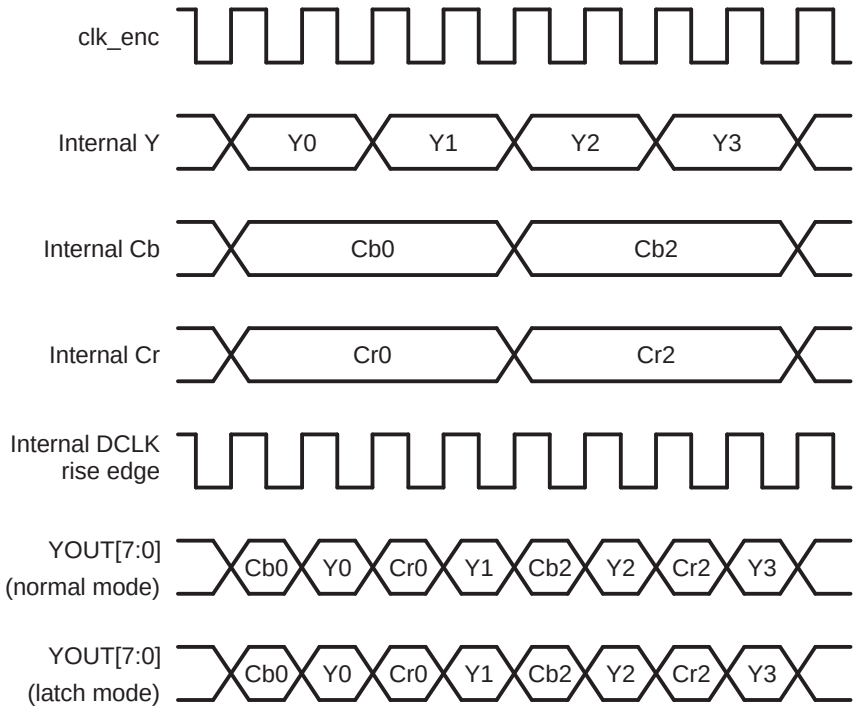
Note that in YCC8 mode, data is normally output on the YOUT bus. However, the YOUT/COUT busses can be swapped via the VIOCTL.YCSWAP register setting to output the YCC8 data on the COUT bus.

ITU-R BT.656 format output is optionally available in YCC8 mode and is enabled via YCCCTL.R656. In this mode, the YCbCr output timing and output order is fixed by hardware in order to conform to the standard and they cannot be altered by the user. To use BT656 mode, the VENC must operate in the standard mode (VMOD.VMD=0). Note that this mode operates correctly only when the pixel clock frequency is half of the VENC clock. In this mode, the sync signals are embedded within the data stream and HSYNC/VSYNC are inactive.

2.2.2.2 YCC8 Protocol and Data Formats

Figure 22 shows the output data sampling of the input YUV422 resolution signal from the OSD module for video windows. Video window input data is YUV422 format natively and RGB888 input data is chroma sub-sampled via boxcar averaging to YUV422 resolution.

Figure 22. YCC8 Output for Normal OSD Operation



The OSD also includes support for window data in bitmap format, either 1,2,4, or 8-bit resolution via a YUV Color Look Up Table (CLUT) or via RGB565 format. Data corresponding to bitmap pixels is in full YUV444 resolution and is overlaid onto the YUV422 resolution video window pixel output. In this case, chroma blurring can occur at the edge between bitmap windows and the rest of the OSD image. In normal operation, the chroma value output from VENC is the immediate value at the sampling time. However, to alleviate this chroma blurring, a “latch” mode is provided where the chroma output for the second pixel in a UV pair can be the data latched at the first pixel. The latch mode is enabled by setting YCCCTL.CHM to 1.

Figure 23. YCC8 Output When OSD Window in RGB565

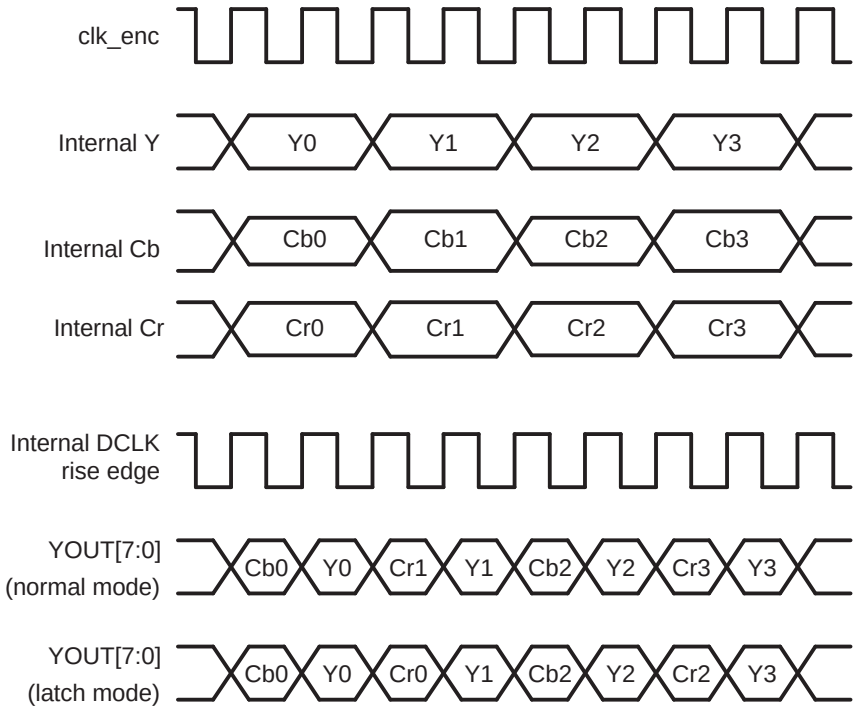


Figure 20 and Figure 21 how the timing marker inserted horizontally and vertically in BT.656 mode. The timing registers such as HSTART, HVALID, VSTART and VSTARTA that specify LCD_OE timing affect the embedded sync insertion position as well in the in the non-standard mode (VMOD.VMD = 1). The field toggle position can be adjusted by YCCCTL.FID656 register bit field. when in the standard mode (VMOD.VMD = 0), the position is fixed as defined in each standard irrespective of the timing registers.

2.2.3 Parallel RGB Signal Interface

For parallel RGB modes, up to 18-bit RGB display data is output in parallel. The upper bits of the RGB samples are multiplexed onto the YOUT and COUT pins, with the lower bits assigned to GIO pins. Output data is sub-sampled at the DCLK rising edge when the data valid signal (LCD_OE) is asserted and output signals are held low when LCD_OE is de-asserted.

Table 12. Interface Signals For Parallel RGB Digital Displays

Name	TYPE	PU PD	Reset State	Description	Fuction Control / Mux Control
VPBE Digital Signals					
YOUT7(R7)	inout		in	R7 signal	VMOD.VDMD = 2
YOUT6(R6)	inout		in	R6 signal	
YOUT5(R5)	inout		in	R5 signal	
YOUT4(R4)	inout		in	R4 signal	
YOUT3(R3)	inout		in	R3 signal	
YOUT2(G7)	inout		in	G7 signal	
YOUT1(G6)	inout		in	G6 signal	
YOUT0(G5)	inout		in	G5 signal	

Table 12. Interface Signals For Parallel RGB Digital Displays (continued)

Name	TYPE	PU PD	Reset State	Description	Fuction Control / Mux Control
VPBE Digital Signals					
COUT7(G4) / GIO092 / PWM0	inout		in	G4 signal	VMOD.VDMD = 2 PINMUX1[1:0]. COUT_7 = 1 PINMUX1[3:2]. COUT_6 = 1 PINMUX1[5:4]. COUT_5 = 1 PINMUX1[7:6]. COUT_4 = 1 PINMUX1[9:8]. COUT_3 = 1 PINMUX1[11:10]. COUT_2 = 1 PINMUX1[13:12]. COUT_1 = 1 PINMUX1[15:14]. COUT_0 = 1
COUT6(G3) / GIO091 / PWM1	inout		in	G3 signal	
COUT5(G2) / GIO090 / PWM2A / RTO0	inout		in	G2 signal	
COUT4(B7) / GIO089 / PWM2B / RTO1	inout		in	B7 signal	
COUT3(B6) / GIO088 / PWM2C / RTO2	inout		in	B6 signal	
COUT2(B5) / GIO087 / PWM2D / RTO3	inout		in	B5 signal	
COUT1(B4) / GIO086 / PWM3A STTRIG	inout		in	B4 signal	
COUT0(B3) / GIO085 / PWM3B	inout		in	B3 signal	
HSYNC / GIO083	inout	PD	in	Video encoder: Horizontal Sync GIO: GIO[083]	PINMUX1[16]. HVSYNC = 0
VSYNC / GIO084	inout	PD	in	Video encoder: Vertical Sync GIO: GIO[084]	PINMUX1[16]. HVSYNC = 0
LCD_OE / GIO082	inout		in	Video encoder: Signals valid video encoder output GIO: GIO[082]	PINMUX1[17]. LCD_OE = 0 (if needed)
LCD_FIELD / GIO081 / R2 / PWM3C	inout		in	Video encoder: Field identifier for interlaced display formats GIO: GIO[081], Digital video out: R2, PWM3C	PINMUX1[19:18], LCD_FIELD = 1 or PINXMUX1[19:18].LCD_FIELD = 2 (if needed)
EXTCLK / GIO080 / B2 / PWM3D	inout	PD	in	Video encoder: External clock input GIO: GIO[080], Digital video out: B2, PWM3D	PINMUX1[21:20], EXTCLK = 1 or PINMUX1[21:20], EXTCLK = 2 (if needed)
VCLK / GIO079	inout		out L	Video encoder: Video output clock GIO: GIO[079]	PINMUX1[22], VCLK = 0
GIO0033 / R1	inout	-	in	GIO: GIO[033] R1 signal	PINMUX4[13:12].GIO33 = 3 (if RGB888 needed)
GIO0032 / R0	inout	-	in	GIO: GIO[032] R0 signal	PINMUX4[11:10].GIO32 = 3 (if RGB888 needed)
GIO0030 / G1	inout	-	in	GIO: GIO[030] G1 signal	PINMUX4[7:6].GIO30 = 3 (if RGB888 needed)
GIO0029 / G0	inout	-	in	GIO: GIO[029] G0 signal	PINMUX4[5:4].GIO29 = 3 (if RGB888 needed)
GIO0028 / B1	inout	-	in	GIO: GIO[028] B1 signal	PINMUX4[3:2].GIO28 = 3 (if RGB888 needed)
GIO0027 / B0	inout	-	in	GIO: GIO[027] B0 signal	PINMUX4[1:0].GIO27 = 3 (if RGB888 needed)

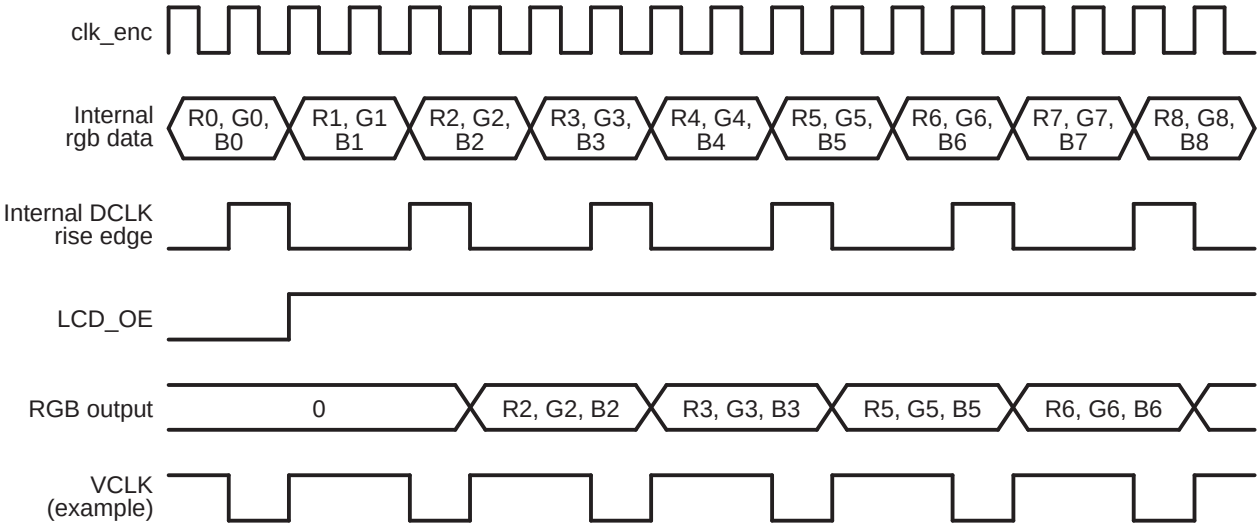
2.2.3.1 Parallel RGB Signal Interface Description

In parallel RGB mode, an RGB565 interface (5-bits Red, 6-bits Green, 5-bits Blue) can be supported via the normal YOUT/COUT signals without requiring additional GIO signals. In addition to this, RGB888 mode can be supported by assigning additional GIO pins to the display interface. Note that RGB888 mode precludes use of the EXTCLK and FIELD signals since the multiplexed functions overlap with the same GIO signals. This assignment is done via the pin multiplexing and is controlled from the DM36x system module described in the *TMS320DM365 Digital Media System-on-Chip (DMSoC) ARM Subsystem Reference Guide* (SPRUFG5). In addition to these signals, the HSYNC, VSYNC, and VCLK signals are also output. An optional EXTCLK input clock can also be used in RGB565 mode.

2.2.3.2 Parallel RGB Protocol and Data Formats

Figure 24 shows the output data sampling of the input YUV422 signal from the OSD module converted by the VENC to parallel RGB format. In this diagram, the values R0, G0, B0, etc. refer to pixel locations.

Figure 24. RGB Output in Parallel RGB Mode



Embedded sync insertion like ITR-R BT.656 is optionally available in PRGB mode. Setting YCCCTL.R656 bit to 1 activates this mode. See Figure22 for the timing.

2.2.4 Serial RGB Signal Interface

For serial RGB modes, the RGB data samples are output serially, multiplexed onto the 8-bit YOUT bus. Output data is sub-sampled at DCLK rising edge when data valid signal (LCD_OE) is asserted and output signals are held low when LCD_OE is de-asserted.

Table 13. Interface Signals For Serial RGB Digital Displays

Name	TYPE	PU PD	Reset State	Description	Function Control / Mux Control
VPBE Digital Signals					
YOUT7(R7)	inout		in	Data7 signal	VMOD.VDMD = 3
YOUT6(R6)	inout		in	Data6 signal	
YOUT5(R5)	inout		in	Data5 signal	
YOUT4(R4)	inout		in	Data4 signal	
YOUT3(R3)	inout		in	Data3 signal	
YOUT2(G7)	inout		in	Data2 signal	
YOUT1(G6)	inout		in	Data1 signal	
YOUT0(G5)	inout		in	Data0 signal	

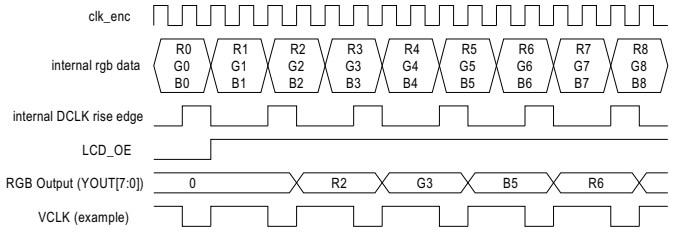
Table 13. Interface Signals For Serial RGB Digital Displays (continued)

Name	TYPE	PU PD	Reset State	Description	Function Control / Mux Control
VPBE Digital Signals					
COUT7(G4) / GIO092 / PWM0	inout		in	LCD_AC	VENC.LCDOUT.ACE = 1 PINMUX1[1:0].COUT_7 = 1
COUT6(G3) / GIO091 / PWM1	inout		in	LCD_OE	VENC.LCDOUT.OEE = 1 PINMUX1[3:2].COUT_6 = 1
COUT5(G2) / GIO090 / PWM2A / RTO0	inout		in	BRIGHT	VENC.LCDOUTBRE = 1 PINMUX1[5:4].COUT_5 = 1
COUT4(B7) / GIO089 / PWM2B / RTO1	inout		in	PWM	VENC.LCDOUT.PWME = 1 PINMUX1[7:6].COUT_4 = 1
COUT3(B6) / GIO088 / PWM2C / RTO2	inout		in	CSYNC	PINMUX1[9:8].COUT_3 = 1
COUT2(B5) / GIO087 / PWM2D / RTO3	inout		in	0	PINMUX1[11:10].COUT_2 = 1
COUT1(B4) / GIO086 / PWM3A STTRIG	inout		in	0	PINMUX1[13:12].COUT_1 = 1
COUT0(B3) / GIO085 / PWM3B	inout		in	Data8 signal	PINMUX1[15:14].COUT_0 = 1
HSYNC / GIO083	inout	PD	in	Video encoder: Horizontal SYNC GIO: GIO[083]	PINMUX1[16] .HVSYNC = 0
VSYNC / GIO084	inout	PD	in	Video encoder: Vertical SYNC GIO: GIO[084]	PINMUX1[16]. HVSYNC = 0
LCD_OE / GIO082	inout		in	Video encoder: Signals valid video encoder output GIO: GIO[082]	PINMUX1[17]. LCD_OE = 0 (if needed)
LCD_FIELD / GIO081 / R2 / PWM3C	inout		in	Video encoder: Field identifier for interlaced display formats GIO: GIO[081], Digital video out: R2, PWM3C	PINMUX1[19:18]. LCD_FIELD = 1 (if needed)
EXTCLK / GIO080 / B2 / PWM3D	inout	PD	in	Video encoder: External clock input, used if clock rates > 27MHz are needed (e.g., 74.25 MHz for HDTV digital output). GIO: GIO[080], Digital video out: B2, PWM3D	PINMUX1[21:20]. EXTCLK = 1 (if needed)
VCLK / GIO079	inout		out L	Video encoder: Video output clock GIO: GIO[079]	PINMUX1[22], VCLK = 0

2.2.4.1 Serial RGB Signal Interface Description

In Serial RGB mode, each component of RGB is output from YOUT[7:0] in rotation. The rotation order can be specified by the RGBOF or RGBEF fields in RGBCTL and different orders can be set for two different line IDs. RGBOF is for odd fields (line ID=0) while RGBEF is for even fields (Line ID=1). The order is reset at HSYNC and rotated at the internal DCLK rising edge on valid data duration (LCD_OE=1). While LCD_OE is de-asserted, the output data is tied to zero (seeFigure 25).

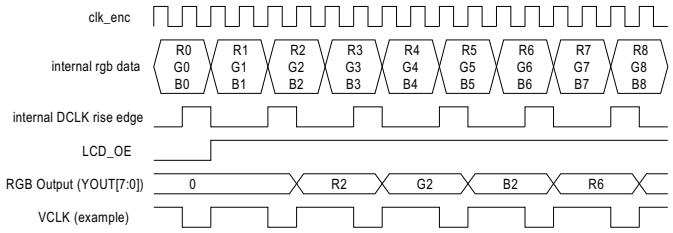
Figure 25. RGB Sampling Rotation in Serial RGB Mode



2.2.4.1.1 Serial RGB Protocol and Data Formats

Figure 26 shows the output data sampling of the input YUV422 signal from the OSD module converted by the VENC to RGB format.

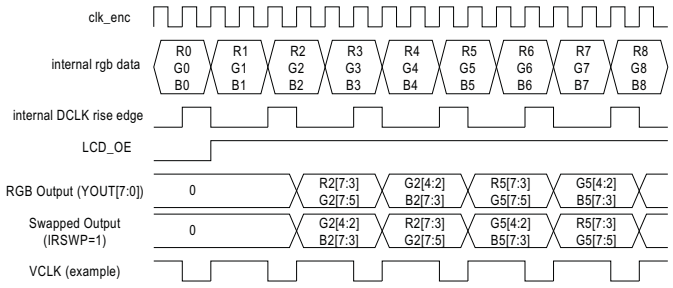
Figure 26. RGB Output in Latch Mode



2.2.4.1.2 IronMan Mode

Optionally, IronMan-type rotation is provided. Setting RGBCTL.IRONM to 1 activates IronMan mode. In this mode, R[7:3], G[7:2] and B[7:3] are concatenated into a 16-bit bus signal, then output in a time-multiplexed fashion as shown in Figure 27. The time-multiplexed order can be swapped by setting RGBCTL.IRSWP to 1.

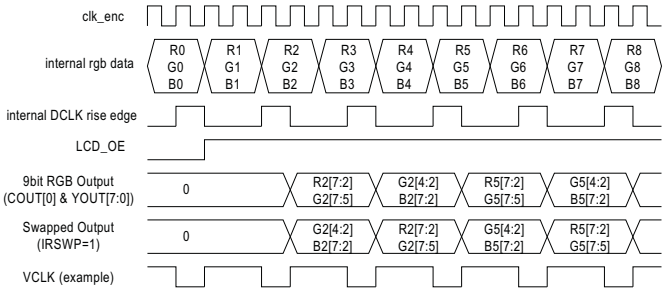
Figure 27. IronMan Serial RGB Output Mode



2.2.4.1.3 9-Bit IronMan Mode

The 9-bit IronMan mode is enabled when RGBCTL.IRONM and RGBCTL.IR9 are set to 1. In this mode, R[7:2], G[7:2] and B[7:2] are concatenated into a 18-bit bus then output as shown in Figure 28. The MSB is assigned to COUT0(B3). As in 8-bit IronMan mode, the order can be swapped by RGBCTL.IRSWP.

Figure 28. 9-Bit IronMan Serial RGB Output Mode



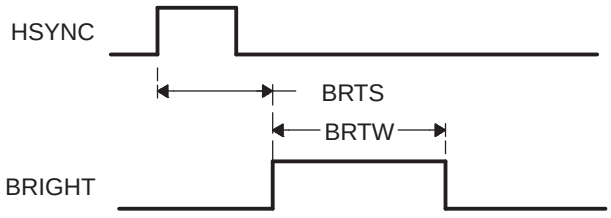
2.2.5 Other Digital LCD Interface Signals

The following LCD signals can be optionally generated. Utilize them as appropriate. See Table 9 for the signal availability in each mode.

2.2.5.1 Bright

- Polarity can be inverted via LCDOUT.BRP.
- When using the BRIGHT signal, set LCDOUT.BRE to 1.
- The units of BRTS and BRTW are in ENC CLK periods.

Figure 29. Bright Signal Timing

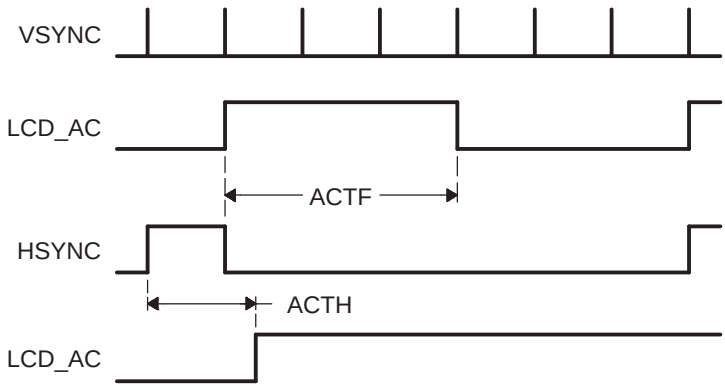


2.2.5.2 LCD_AC

When using the LCD_AC signal, set LCDOUT.ACE to 1.

The units of ACCTL.ACTH and ACCTL.ACTF are ENC CLK and line, respectively.

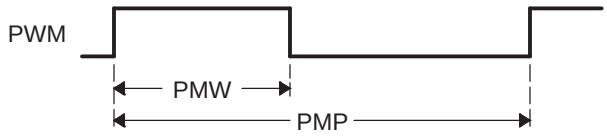
Figure 30. LCD_AC Signal Timing



2.2.5.3 Pulse Width Modulation (PWM) Signal

To use the PWM signal, set LCDOUT.PWME to 1. Polarity can be inverted by LCDOUT.PWMP. This is a free-run signal and not synchronized to any sync signals. The unit is ENC CLK.

Figure 31. PWM Signal Timing



2.3 VPBE Display Subsystem I/O Multiplexing

The various VPBE digital display modes have unique pin multiplexing options as shown in Table 14. Some of these settings are controlled in the System Module, described in PINMUX1 and PINMUX4 registers in detail in the *TMS320DM365 Digital Media System-on-Chip (DMSoC) ARM Subsystem Reference Guide* (SPRUFG5). The remaining settings are controlled via the mode in which the controller is placed.

Table 14. Signals for VPBE Digital Display Modes

Pin Name	YCC16	YCC8/REC656	PRGB	SRGB
HSYNC GIO083	HSYNC	HSYNC	HSYNC	HSYNC
VSYNC GIO084	VSYNC	VSYNC	VSYNC	VSYNC
LCD_OE GIO082	As needed	As needed	As needed	As needed
LCD_FIELD GIO081, R2, PWM3C	As needed	As needed	As needed	As needed
EXTCLK GIO080, B2, PWM3D	As needed	As needed	As needed	As needed
GIO0033 R1	-	-	R1	-
GIO0032 R0	-	-	R0	-
GIO0030 G1	-	-	G1	-
GIO0029 G0	-	-	G0	-
GIO0028 B1	-	-	B1	-
GIO0027 B0	-	-	B0	-
VCLK GIO079	VCLK	VCLK	VCLK	VCLK
YOUT7(R7)	Y7	Y7,Cb7,Cr7	R7	Data7
YOUT6(R6)	Y6	Y6,Cb6,Cr6	R6	Data6
YOUT5(R5)	Y5	Y5,Cb5,Cr5	R5	Data5
YOUT4(R4)	Y4	Y4,Cb4,Cr4	R4	Data4
YOUT3(R3)	Y3	Y3,Cb3,Cr3	R3	Data3
YOUT2(G7)	Y2	Y2,Cb2,Cr2	G7	Data2
YOUT1(G6)	Y1	Y1,Cb1,Cr1	G6	Data1
YOUT0(G5)	Y0	Y0,Cb0,Cr0	G5	Data0
COUT7(G4) GIO092, PWM0	C7	LCD_AC	G4	LCD_AC
COUT6(G3) GIO091, PWM1	C6	LCD_OE	G3	LCD_OE
COUT5(G2) GIO090, PWM2A, RTO0	C5	BRIGHT	G2	BRIGHT
COUT4(B7) GIO089, PWM2B, RTO1	C4	PWM	B7	PWM

Table 14. Signals for VPBE Digital Display Modes (continued)

Pin Name	YCC16	YCC8/REC656	PRGB	SRGB
COUT3(B6) GIO088, PWM2C, RTO2	C3	CSYNC	B6	CSYNC
COUT2(B5) GIO087, PWM2D, RTO3	C2	optional	B5	-
COUT1(B4) GIO086, PWM3A, STTRIG	C1	optional	B4	-
COUT0(B3) GIO085, PWM3B	C0	optional	B3	Data8

2.3.1 RGB888 Output Mode Pin Muxing

Allocation of GIO signals for the RGB888 mode of the parallel RGB video out is done in the system module via the PINMUX1 and PINMUX4 registers as shown in Table 15 and Table 16. Enabling PWM3x or PEXTCLK/FIELD options usurps the B2 or R2 pin, respectively, and prevents proper RGB888 operation.

Proper RGB888 operation requires setting PINMUX1.EXTCLK to 10, PINMUX1.FIELD to 10, and PINMUX4.GIO33, PINMUX4.GIO32, PINMUX4.GIO30, PINMUX4.GIO29, PINMUX4.GIO28, and PINMUX4.GIO27 to 11.

Table 15. RGB888 Output Mode Pin Multiplexing (PINMUX1)

PINMUX1.EXTCLK	PINMUX1.FIELD	EXTCLK / GIO[80] / B2 / PWM3D	FIELD / GIO[81] / R2 / PWM3C
00	x	GIO[80]	x
01	x	EXTCLK	x
10	x	B2	x
11	x	PWM3D	x
x	00	x	GIO[81]
x	01	x	FIELD
x	10	x	R2
x	11	x	PWM3C

Table 16. RGB888 Output Mode Pin Multiplexing (PINMUX4)

Register	Selection
PINMUX4[13:12]	00: GIO0033 01: SPI2_SCS[0] 10: USBDRVVBUS **11: R1**
PINMUX4[11:10]	00: GIO0032 01: SPI2_CLKS 10: Reserved **11: R0**
PINMUX4[7:6]	00: GIO0030 01: SDI2_SIMO 10: Reserved **11: G1**
PINMUX[5:4]	00: GIO0029 01: SPI2_SCS[0] 10: Reserved **11: G0**
PINMUX[3:2]	00: GIO0028 01: SPI1_CLKS 10: Reserved **11: B1**

Table 16. RGB888 Output Mode Pin Multiplexing (PINMUX4) (continued)

Register	Selection
PINMUX[1:0]	00: GIO0027 01: SPI1_SOMI 10: SPI2_SCS[1] **11: B0**

2.3.2 CCD and LCD Control Signal Multiplexing

The LCD controller in the VPBE requires additional control signals for certain modes of operation multiplexed to some of the COUT signals. Each of these signals has a separate enable bit in the VENC.LCDOUT register which selects between the control signal function and other VPBE functions. Note that for these controls to be effective, the signals must first be configured to be VPBE pins via the PINMUX1 register.

2.3.3 Pin Multiplexing Control Registers

2.3.3.1 PINMUX1 Register

The PINMUX1 register is shown in Figure 32 and described in Table 17. The address for this register is 0x01C4:0004.

Figure 32. PINMUX1 Register

31	23	22	21	20	19	18	17	16
Reserved		VCLK	EXTCLK		FIELD		VVALID	HVSYNC
R-0		R/W-0	R/W-0		R/W-0		R/W-0	R/W-0

15	14	13	12	11	10	9	8
COUT_0		COUT_1		COUT_2		COUT_3	
R/W-0		R/W-0		R/W-0		R/W-0	

7	6	5	4	3	2	1	0
COUT_4		COUT_5		COUT_6		COUT_7	
R/W-0		R/W-0		R/W-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

Table 17. PINMUX1 Register Field Descriptions

Bit	Field	Value	Description
31-23	Reserved		Reserved. Must be set to zero.
22	VCLK		Enable VCLK
		0	VCLK
		1	GIO[79]
21-20	EXTCLK		Enable EXTCLK (Video Out pin mux)
		0	GIO[80]
		1h	EXTCLK
		2h	B2
		3h	PWM3
19-18	LCD_FIELD		Enable LCD_FIELD (Video Out pin mux)
		0	GIO[81]
		1h	LCD_FIELD
		2h	R2
		3h	PWM3

Table 17. PINMUX1 Register Field Descriptions (continued)

Bit	Field	Value	Description
17	LCD_OE		Enable LCD_OE signal output (Video Out pin mux)
		0	LCD_OE
		1	GIO[82]
16	HVSYNC		Enable HVSYNC (Video Out pin mux)
		0	HVSYNC and VSYNC
		1	GIO[84:83]
15-14	COUT_0		Enable COUT[0] (Video Out pin mux)
		0	GIO[85]
		1h	COUT[0]
		2h	PWM3
13-12	COUT_1		Enable COUT[1] (Video Out pin mux)
		0	GIO[86]
		1h	COUT[1]
		2h	PWM3
		3h	STTRIG
11-10	COUT_2		Enable COUT[2] (Video Out pin mux)
		0	GIO[87]
		1h	COUT[2]
		2h	PWM2
		3h	RTO3
9-8	COUT_3		Enable COUT[3] (Video Out pin mux)
		0	GIO[88]
		1h	COUT[3]
		2h	PWM2
		3h	RTO2
7-6	COUT_4		Enable COUT[4] (Video Out pin mux)
		0	GIO[89]
		1h	COUT[4]
		2h	PWM2
		3h	RTO1
5-4	COUT_5		Enable COUT[5] (Video Out pin mux)
		0	GIO[90]
		1h	COUT[5]
		2h	PWM2
		3h	RTO0
3-2	COUT_6		Enable COUT[6] (Video Out pin mux)
		0	GIO[91]
		1h	COUT[6]
		2h	PWM1
		3h	Reserved
1-0	COUT_7		Enable COUT[7] (Video Out pin mux)
		0	GIO[92]
		1h	COUT[7]
		2h	PWM0
		3h	Reserved

2.3.3.2 Pin Mux 4 (PINMUX4) Register

The pin mux 4 (PINMUX4) register is shown in Figure 33 and described in Table 18. This register controls pin multiplexing for SPI0 and MMC/SD0.

Figure 33. Pin Mux 4 (PINMUX4) Register

31	30	29	28	27	26	25	24
GIO42		GIO41		GIO40		GIO39	
R/W-0		R/W-0		R/W-0		R/W-0	
23	22	21	20	19	18	17	16
GIO38		GIO37		GIO36		GIO35	
R/W-0		R/W-0		R/W-0		R/W-0	
15	14	13	12	11	10	9	8
GIO34		GIO33		GIO32		GIO31	
						R/W-0	
7	6	5	4	3	2	1	0
GIO30		GIO29		GIO28		GIO27	
R/W-0		R/W-0		R/W-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 18. Pin Mux 4 (PINMUX4) Register Field Descriptions

Bit	Field	Value	Description
31-30	GIO42		Enable GIO[42] (GPIO Pin Mux)
		0	GIO42
		1	MMCSD1_CMD
		2	EM_A19
		3	Reserved
29-28	GIO41		Enable GIO[41] (GPIO Pin Mux)
		0	GIO41
		1	MMCSD1_DATA3
		2	EM_A18
		3	Reserved
27-26	GIO40		Enable GIO[40] (GPIO Pin Mux)
		0	GIO40
		1	MMCSD1_DATA2
		2	EM_A17
		3	Reserved
25-24	GIO39		Enable GIO[39] (GPIO Pin Mux)
		0	GIO39
		1	MMCSD1_DATA1
		2	EM_A16
		3	Reserved
23-22	GIO38		Enable GIO[38] (GPIO Pin Mux)
		0	GIO38
		1	MMCSD1_DATA0
		2	EM_A15
		3	Reserved

Table 18. Pin Mux 4 (PINMUX4) Register Field Descriptions (continued)

Bit	Field	Value	Description
21-20	GIO37		Enable GIO[37] (GPIO Pin Mux)
		0	GIO37
		1	SPI4_SCS[0]
		2	McBSP_CLKS
		3	CLKOUT0
19-18	GIO36		Enable GIO[36] (GPIO Pin Mux)
		0	GIO36
		1	SPI4_CLKS
		2	EM_A21
		3	EM_A14
17-16	GIO35		Enable GIO[35] (GPIO Pin Mux)
		0	GIO35
		1	SPI4_SOMI
		2	SPI4_SCS[1]
		3	CLKOUT1
15-14	GIO34		Enable GIO[34] (GPIO Pin Mux)
		0	GIO34
		1	SPI4_SIMO
		2	SPI4_SOMI
		3	UART1_RXD
13-12	GIO33		Enable GIO[33] (GPIO Pin Mux)
		0	GIO33
		1	SPI2_SCS[0]
		2	USBDRVVBUS
		3	R1
11-10	GIO32		Enable GIO[32] (GPIO Pin Mux)
		0	GIO32
		1	SPI2_CLKS
		2	Reserved
		3	R0
9-8	GIO31		Enable GIO[31] (GPIO Pin Mux)
		0	GIO31
		1	SPI2_SOMI
		2	SPI2_SCS[1]
		3	CLKOUT2
7-6	GIO30		Enable GIO[30] (GPIO Pin Mux)
		0	GIO30
		1	SPI2_SIMO
		2	Reserved
		3	G1
5-4	GIO29		Enable GIO[29] (GPIO Pin Mux)
		0	GIO29
		1	SPI1_SCS[0]
		2	Reserved
		3	G0

Table 18. Pin Mux 4 (PINMUX4) Register Field Descriptions (continued)

Bit	Field	Value	Description
3-2	GIO28		Enable GIO[28] (GPIO Pin Mux)
		0	GIO28
		1	SPI1_CLKS
		2	Reserved
		3	B1
1-0	GIO27		Enable GIO[27] (GPIO Pin Mux)
		0	GIO27
		1	SPI1_SOMI
		2	SPI1_SCS[1]
		3	B0

3 VPBE Integration

This section describes how the VPBE subsystem is integrated into the DMSoC.

3.1 Clocking, Reset, and Power Management Scheme

3.1.1 Clocks

3.1.1.1 DAC and External Clock

The DAC will be attached to the VENC module that is inside the video processing back end (VPBE). The data flow between the VPBE and DACs is synchronous. Figure 34 shows the possible clocking modes.

The VPBE must interface with a variety of LCDs (which require many different and specific frequencies), as well as the 4-channel DAC module. The range of frequencies that the pin interface needs to run is 6.25MHz – 75MHz.

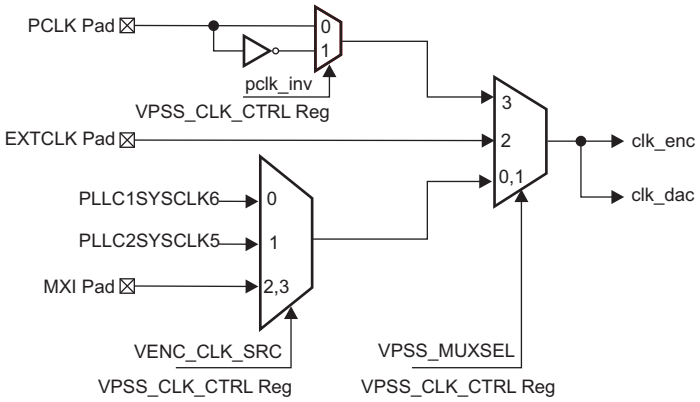
There are two synchronous clock domains in the VPBE -- the external clock domain (6.25 MHz to 75 MHz), and the internal (system) clock domain, which is at the PLLC1SYSCLK6 / PLLC2SYSCLK5 clock rate.

The VENC clock domain can get its clock from four sources:

- MXI (27 MHz) crystal input
- EXTCLK input pin
- VPFE pixel clock input (PCLK)
- PLLC1SYSCLK6 / PLLC2SYSCLK5

The DACs can also have their clocks independently gated off when the DACs are not being used.

Figure 34. VPBE/DAC Clocking Options



The VPBE clock control is in the System module in the VPSS_CLK_CTRL register. The various modes shown in Figure 34 are described here.

- **VPSS_MUXSEL = 0 or 1:** Both the VENC and DAC get their clock from one of the following three sources: PLLC1SYSCLK6 clock, PLLC2SYSCLK5 clock, or MXI crystal input.
- **VPSS_MUXSEL = 2:** EXTCLK mode - Both the DAC and VENC receive the external input clock via the EXTCLK port.
- **VPSS_MUXSEL = 3:** PCLK mode - Both the DAC and VENC receive the PCLK. When PCLK frequency is 27 MHz or 74.25 MHz, the DAC clock can be enabled to get SDTV, HDTV video output. PCLK can be inverted for negative edge support, selectable by the PCLK_INV bit of VPSS_CLK_CTRL register.

3.1.1.2 VPSS Clock Mux Control Register (VPSS_CLK_CTRL)

The VPSS clock mux control register (VPSS_CLK_CTRL) is shown in Figure 35 and described in Table 19. The address for this register is 0x01C4:0044.

Figure 35. VPSS Clock Mux Control Register (VPSS_CLK_CTRL)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
R-0															

15	14	13	12	11	10	9	8
Reserved							
R-0							

7	6	5	4	3	2	1	0
VPSS_CLKMD	VENC_CLK_SRC		DACCLKEN	VENCLKEN	PCLKINV	MUXSEL	
R/W-0	R/W-0		R/W-0	R/W-0	R/W-0	R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 19. VPSS Clock Mux Control Register (VPSS_CLK_CTRL) Field Descriptions

Bit	Field	Value	Description
31-8	Reserved	0	Reserved
7	VPSS_CLKMD		Config/DMA bus clock versus VPSS clock ratio
		0	1:2
		1	1:1
6-5	VENC_CLK_SRC		27/74.25 MHz input source
		0	PLLC1SYSCLK6
		1	PLLC2SYSCLK5
		2h	MXI Oscillator
		3h	MXI Oscillator
4	DACCLKEN		Video DAC clock enable
		0	Disabled
		1	Enabled
3	VENCCLKEN		VPBE/Video encoder clock enable
		0	Disabled
		1	Enabled
2	PCLK_INV		Invert VPFE pixel clock (PCLK)
		0	Diable VENC clock mux and receive normal PCLK
		1	Enable VENC clock mux and receive inverted PCLK
1-0	VPSS_MUXSEL	0-3h	VPSS clock selection
		0	Use input set by VENC_CLK_SRC
		1h	Use input set by VENC_CLK_SRC
		2h	EXTCLK mode. Use external VPBE clock input
		3h	PCLK mode. Use PCLK (or ~PCLK) from VPFE

3.1.2 Resets

The module resets are tied to the device reset signals.

The VPBE is a subset of the VPSS module and has two module domains, the VPSS Master processing domain and the VPSS Slave register interface. Thus, resetting either of these will affect the VPFE as well.

CAUTION

Do not use the SyncReset or SwRstDisable states of the PSC for either the VPSS Master or VPSS Slave modules.

3.1.3 Power Domain and Power Management

The device VPBE module resides in the “Always On” power domain, along with the ARM core and most other peripherals. When enabled, the VPFE modules utilize auto clock gating on a clock-by-clock basis to conserve dynamic power during periods of inactivity. Active power consumption can also be managed proactively via numerous clock enable/disable controls.

3.1.3.1 Minimize Active Power

To completely disable the VPSS module and all logic gated by external clocks:

- Disable the VPSS master module in the PSC (use Disable only; not SwRstDisable). This will disable the clock to the VPSS logic and the VPSS shared DMA logic and memory buffers. Note that this also disables the VPFE logic.
- Disable the VPSS slave module in the PSC (useDisable only; not SwRstDisable). This will disable the clock to the VPSS register interface. Note that this also disables the register interface for the VPFE modules.

To disable any other clocks to the VPBE:

- Disable any external imaging device driving the VPFE pixel clock (PCLK) to avoid clocking any input logic and any of the VPBE logic via pass-through.
- Disable any external EXTCLK source to avoid clocking any output logic.
- Stop the DAC clock directly via SYSTEM.VPSS_CLK_CTRL.DACCLKEN = 0.
- Stop Gamma table, digital LCD, and analog video encoder clocks via VENC.CLKCTL.

3.1.3.2 Minimize Active Power When only VPBE is Used (VPFE is Disabled)

VPBE-only mode

Clock gate VPFE only, but keep VPBE active:

-
- Disable the clocks to the VPFE modules via VPSSCLK.CLKCTRL (i.e., CCDC_CLK, IPIPE_CLK, H3A_CLK).
- Disable any external imaging device driving the VPFE pixel clock (PCLK) to avoid clocking any input logic and any of the VPBE logic via pass-through.

VPBE digital-only mode

Clock gate video DAC:

- Stop the DAC clock directly via SYSTEM.VPSS_CLK_CTRL.DACCLKEN = 0.
- Stop analog video encoder clock via VENC.CLKCTL.
- Stop gamma table clock via VENC.CLKCTL, if not used.

NOTE: When PCLK is used for VPBE (CLK_VENC), the DAC clock is automatically disabled: SYSTEM.VPSS_CLK_CTRL.VPSS_MUXSEL = 3.

3.1.3.3 Minimize Active Power When Only VPFE is Used (VPBE is Disabled)

VPFE-only mode

Clock gate VPBE only, but keep VPFE active:

- Gate CLK_VENC by stopping it at the source (at the clock input pin or via SYSTEM.VPSS_CLK_CTRL.VENCCLKEN = 0).
- Gate CLK_DAC by stopping it at the source (at the clock input pin or via SYSTEM.VPSS_CLK_CTRL.DACCLKEN = 0).

VPFE-only mode

Other options:

- Gate all VPBE clocks off via VPBE_CLK_CTRL.VPBE_CLK_ENABLE = 0.
- Disable the video encoder (VENC) operation via VMOD.VENC = 0.

3.2 Hardware Requests

3.2.1 Interrupt Requests

The device OSD and VENC can generate interrupts to the ARM as shown in Table 20. This indicates an end-of-frame event, i.e., processing has completed for a frame.

Table 20. ARM Interrupts - VPBE

INT Number	Acronym	Source	VPBE Options
0 - 8	VPSSINT0 - 8	VPSS, configurable via the ISP.INTSEL[1:3] register	OSDINT, VENCINT

3.2.2 EDMA Requests

The OSD and VENC interrupt events can also be used to trigger EDMA as shown in Table 21. This indicates an end-of-frame event, i.e., processing has completed for a frame.

Table 21. EDMA Interrupts

EVT Number	Acronym	Source	VPBE Options
4 - 7	VPSSEVT1 - 4	VPSS, configurable via register: ISP.EVTSEL	OSDINT, VENCINT

3.3 Video DAC Configuration

The video DACs can be configured via the VDAC_CONFIG register. For more details on video DAC configuration register, refer to *TMS320DM365 Digital Media System-on-Chip (DMSoC) ARM Subsystem Reference Guide* (SPRUFG5).

3.3.1 Video DAC Configuration (VDAC_CONFIG) Register

The video DAC configuration (VDAC_CONFIG) register is shown in Figure 36and described in Table 22.

Figure 36. Video Dac Configuration (VDAC_CONFIG) Register

31	30	29	24
TVSHORT	TVINT	Reserved	
R-0	R-0	R-0	

23	20	19	18	16
Reserved		PDTVSHORTZ	Reserved	
R-0		R/W-0	R-0	

15	8
Reserved	
R-0	

7	6	5	4	3	2	1	0
Reserved		XDMODE	PWDNZ_TVDETECT	PWDNBUFZ	PWD_C	PWD_B	PWD_A
R-0		R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 22. Video Dac Configuration (VDAC_CONFIG) Register Field Descriptions

Bit	Field	Value	Description
31	TVSHORT		TVSHORT performs short detection for the video output. When the output of either channel is shorted to ground, the signal TVSHORT turns to logic high.

Table 22. Video Dac Configuration (VDAC_CONFIG) Register Field Descriptions (continued)

Bit	Field	Value	Description
30	TVINT		TVINT performs detection of connection and disconnection of video signal. Reading '1" shows the connection of video signal.
29-20	Reserved	0x101	Reserved
19	PDTVSHORTZ		Output interrupt signal when TVOUT shorts to ground. Active high.
18-6	Reserved	0x907	Reserved
5	XDMODE		Select HD DAC mode / SD Video Buffer mode for DAC CH-C.
		0	SD Video buffer mode
		1	HD DAC mode
4	PWDNZ_TVDETECT		TVINT circuit enable signal.
		0	Disable
		1	Enable
3	PWDNBUFZ		Power down control for SD Video Buffer.
		0	Power down
		1	Normal
2	PWD_C		Power down mode control for CH-C
		0	Power down
		1	Normal
1	PWD_B		Power down mode control for CH-B
		0	Power down
		1	Normal
0	PWD_A		Power down mode control for CH-A
		0	Power down
		1	Normal

3.4 VPBE Top-Level Register Mapping Summary

The VPBE module memory map is described in Table 23.

Table 23. VPBE Module Register Map

Address	Peripheral	Description
0x01C4:0044	VPSS_CLK_CTRL	VPSS Clock Control
0x01C7:1C00	OSD	VPBE On-Screen Display
0x01C7:1E00	VENC	VPBE Video Encoder

4 VPBE Functional Description

4.1 Block Diagram

The VPSS block diagram is shown in Figure 37. Additional detailed block diagrams are shown in the Interface and Image Processing subsections.

Figure 37. Video Processing Subsystem Block Diagram

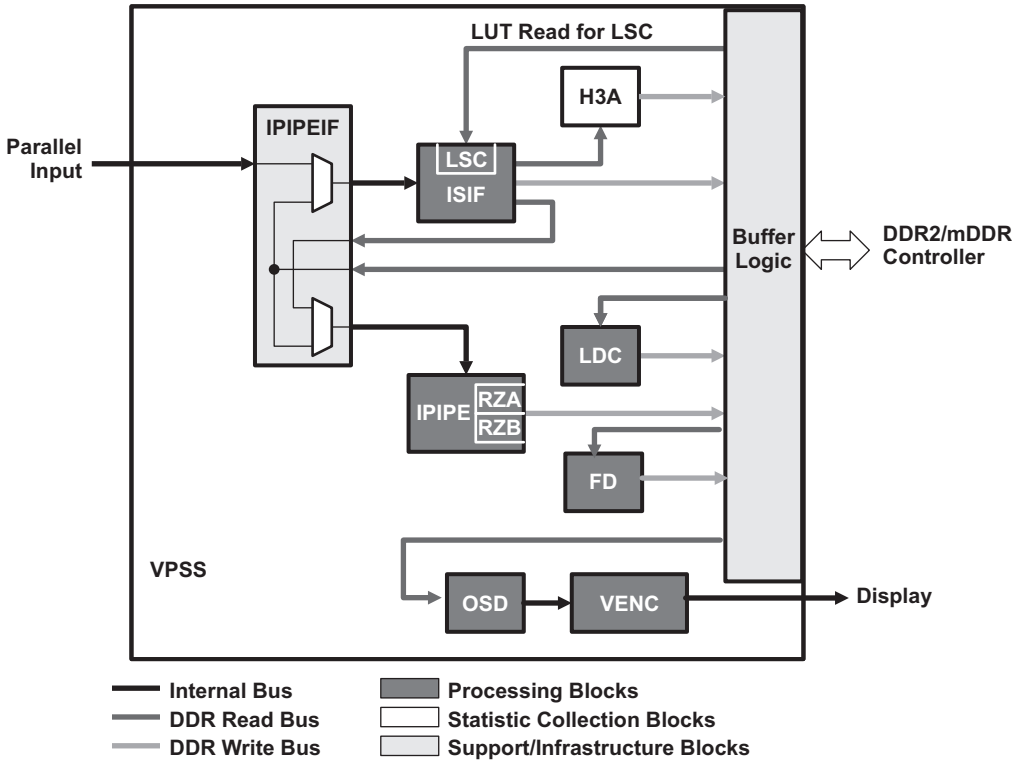
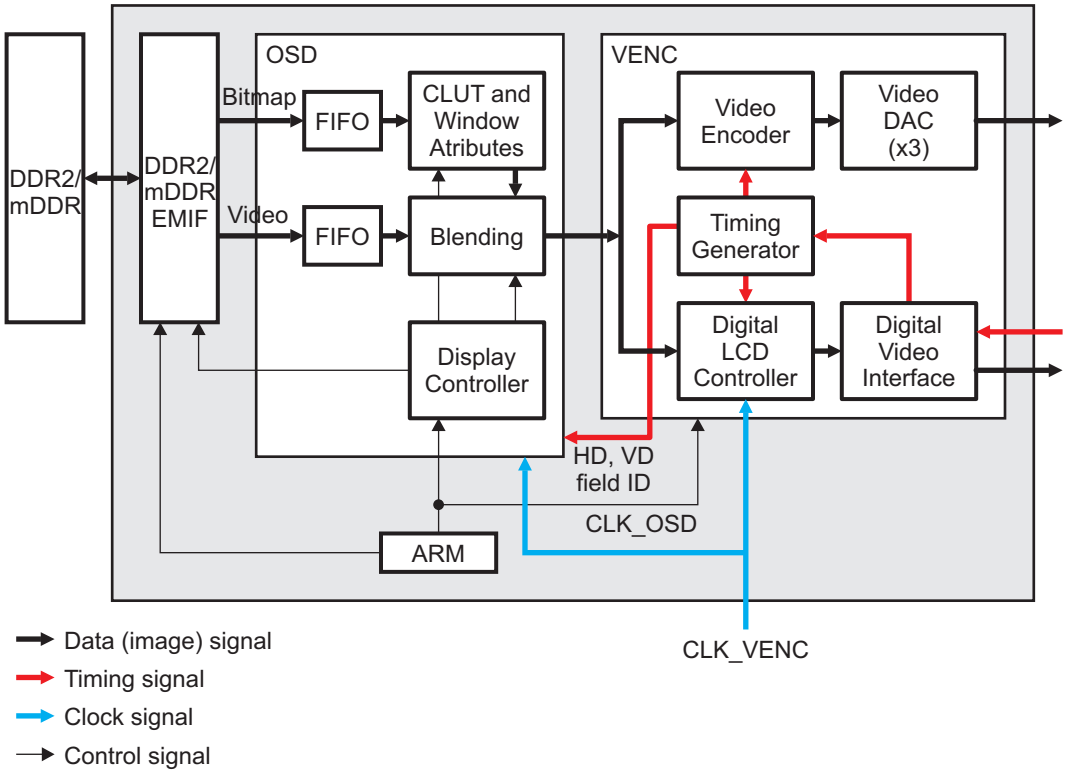


Figure 38. Video Processing Back End Block Diagram



4.2 Interfacing with Displays

The VENC/digital LCD controller supports several display/output interfaces described in the following sections. For further details on configuring the VENC for operation in the various modes, see Section 5.

4.2.1 Analog Display Interface

The analog display interface uses these DAC signals as described below.

Table 24. Analog Display Interface Signals

Name	I/O	Function
VREF	A inout	Video DAC: Reference voltage output (0.5 V, 0.1 μF to gnd)
IREF	A inout	Video DAC: Reference current output inout (2400 Ω to gnd)
IDACOUT	A inout	Video DAC: Current source input from DAC (2100 Ω to VFB)
VFB	A inout	Video DAC: Amplifier feedback node (2100 Ω to IDACOUT, 2150 Ω to TVOUT
TVOUT	A inout	Video DAC: DAC1 video output (2150 Ω to VFB, Output of 75 Ω driver, AC couple to TV)
COMPY	A out	Video DAC: Analog video signal component output Y
COMPPB	A out	Video DAC: Analog video signal component output Pb
COMPPR	A out	Video DAC: Analog video signal component output Pr
V_{DDA18_DAC}	PWR	Video DAC:Analog 1.8 V power
V_{DDA12_DAC}	PWR	Video DAC:Analog 1.2 V power

Table 24. Analog Display Interface Signals (continued)

Name	I/O	Function
V_{SSA18_DAC}	GND	Video DAC:Analog 1.8 V ground
V_{SSA12_DAC}	GND	Video DAC:Analog 1.2 V ground

4.2.2 YCC16 Digital Display Interface

The YCC16 interface includes the signals described in Table 25.

Table 25. YCC16 Digital Display Interface Signals

Name	I/O	Function
YOUT[7:0] COUT[7:0]	O	Image Data - mode set by VMOD.VDMD • Busses can be swapped via VIOCTL.YCSWAP • Cb, Cr order controlled by YCCCTL.YCP
VSYNC	I/O	VSYNC-vertical sync signal • This signal can be configured as an input or an output (VMOD.SLAVE) • When configured as an output, the OSD/VENC supplies the VD signal • When configured as an input, the Display supplies the VD signal
HSYNC	I/O	HSYNC - horizontal sync signal • This signal can be configured as an input or an output (SLAVE bit in VMOD) • When configured as an output, the OSD/VENC supplies the HD signal • When configured as an input, the Display supplies the HD signal
LCD_OE	O	LCD output enable signal • This signal indicates when the VENC/DLCD outputs valid data
VCLK	O	Video pixel clock • This signal is the pixel clock used to indicate valid display data
EXTCLK	I	VPBE pixel clock (SYSTEM.VPSS_CLK_CTRL.VPSS_MUXSEL) • This signal is the optional input pixel clock

4.2.3 YCC8 Digital Display Interface

The YCC8/REC656 interface includes the signals described in Table 26.

Table 26. YCC8 Digital Display Interface Signals

Name	I/O	Function
YOUT[7:0] or COUT[7:0]	O	Image Data - mode set by the VMOD.VDMD; REC656 mode set by YCCCTL.R656 • Buses can be selected via VIOCTL.YCSWAP • Y, Cb, Cr order controlled by the YCCCTL.YCP
VSYNC	I/O	VSYNC-vertical sync signal • This signal can be configured as an input or an output (VMOD.SLAVE) • When configured as an output, the OSD/VENC supplies the VD signal • When configured as an input, the Display supplies the VD signal
HSYNC	I/O	HSYNC - horizontal sync signal • This signal can be configured as an input or an output (VMOD.SLAVE) • When configured as an output, the OSD/VENC supplies the HD signal • When configured as an input, the Display supplies the HD signal
LCD_OE	O	LCD output enable signal • This signal indicates when the VENC/DLCD outputs valid data
VCLK	O	Video pixel clock • This signal is the pixel clock used to indicate valid display data
EXTCLK	I	VPBE pixel clock (SYSTEM.VPSS_CLKCTL.MUXSEL) • This signal is the optional input pixel clock

4.2.4 Parallel RGB Digital Display Interface

The parallel RGB interface includes the signals described in Table 27.

Table 27. Parallel RGB Digital Display Interface Signals

Name	I/O	Function
R[7:3], G[7: 2], B[7:3]	O	Image Data - mode set by the VMOD.VDMD • Default is RGB565 • Use system register PINMUX1.EXTCLK, PINMUX1.LCD_FIELD, PINMUX4.GIO33-32, PINMUX4.GIO30-27 to set up RGB888 mode
VSYNC	I/O	VSYNC-vertical sync signal • This signal can be configured as an input or an output (VMOD.SLAVE) • When configured as an output, the OSD/VENC supplies the VD signal • When configured as an input, the Display supplies the VD signal
HSYNC	I/O	HSYNC - horizontal sync signal • This signal can be configured as an input or an output (VMOD.SLAVE) • When configured as an output, the OSD/VENC supplies the HD signal • When configured as an input, the Display supplies the HD signal
LCD_OE	O	LCD output enable signal • This signal indicates when the VENC/DLCD outputs valid data
VCLK	O	Video pixel clock • This signal is the pixel clock used to indicate valid display data
EXTCLK	I	VPBE pixel clock (SYSTEM.VPSS_CLK_CTRL.VPSS_MUXSEL) • This signal is the optional input pixel clock; cannot be used in RGB888 mode

4.2.5 Serial RGB Digital Display Interface

The serial RGB interface includes the signals described in Table 28.

Table 28. Serial RGB Digital Display Interface Signals

Name	I/O	Function
Data[7:0]	O	Image Data - mode set by the VDMD bit in VDMD.
VSYNC	I/O	VSYNC-vertical sync signal • This signal can be configured as an input or an output (VMOD.SLAVE) • When configured as an output, the OSD/VENC supplies the VD signal • When configured as an input, the Display supplies the VD signal
HSYNC	I/O	HSYNC - horizontal sync signal • This signal can be configured as an input or an output (VMOD.SLAVE) • When configured as an output, the OSD/VENC supplies the HD signal • When configured as an input, the Display supplies the HD signal
LCD_OE	O	LCD output enable signal • This signal indicates when the VENC/DLCD outputs valid data
VCLK	O	Video pixel clock • This signal is the pixel clock used to indicate valid display data
EXTCLK	I	VPBE pixel clock (SYSTEM.VPSS_CLK_CTRL.VPSS_MUXSEL) • This signal is the optional input pixel clock
LCD_AC	I	LCD_AC signal
BRIGHT	I	BRIGHT signal
PWM	I	PWM signal
CSYNC	I	CSYNC signal

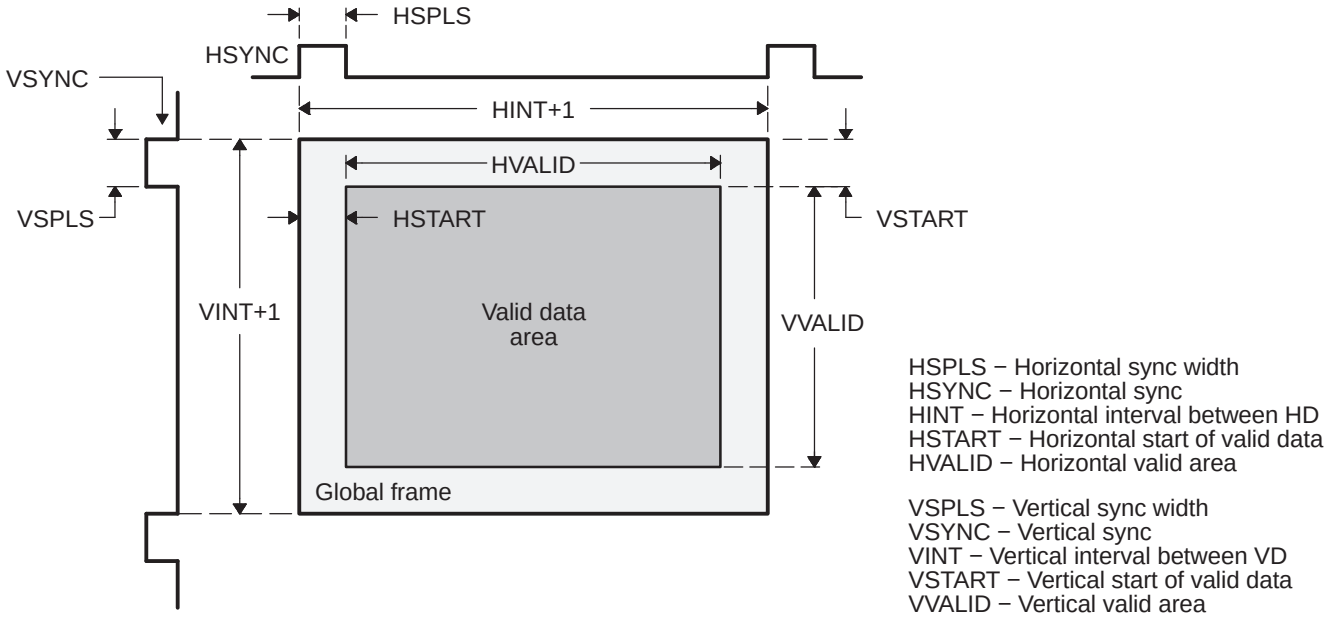
4.3 Master/Slave Mode Interface

The device can be separately configured to either source or sink the VSYNC/HSYNC signals. If master mode is set via VMOD.SLAVE=0, the VIOCTL.SYDIR=0 must be set to output the sync signals. In addition, the registers listed in Table 29 must be set to define the output frame (Figure 39).

Table 29. Master Mode Configuration Registers

Acronym	Register
HSPLS	Horizontal sync pulse width
VSPLS	Vertical sync pulse width
HINTVL	Horizontal interval
HSTART	Horizontal valid data start position
HVALID	Horizontal data valid range
VINT	Vertical interval
VSTART	Vertical valid data start position
VVALID	Vertical data valid range
HSDLY	Horizontal sync delay
VSDLY	Vertical sync delay

Figure 39. Video Encoder Display Frame and Control Signal Definitions



NOTE: HINT + 1 must be even when OSD clock is 1/2 VENC clock.

4.4 On-Screen Display (OSD) Module

The on-screen display (OSD) module reads data in various window formats from DDR2/mDDR and converts them into YUV display data, blends the various windows using the fixed display priority and any optional blending and transparency rules and sends the combined display image to the VENC for conditioning and output. The OSD windows (Table 30 and Figure 40) show the display priority, window type, and data types supported by each window.

Table 30. OSD Windows

Window	Priority	Type	Data Types	Control Register	Description
CURSOR	1	Rectangular outline w/transparent center	NA	RECTCUR	Controls the size and on/off control of rectangular cursor window
OSD1	2	Bitmap (or Attribute)	Bitmap, RGB565, RGB888+blend YUV422 or Attribute (blend+blink)	OSDWIN1MD	Controls the display, zoom blending, and on/off control of OSD window 1
OSD0	3	Bitmap	Bitmap, RGB565, RGB888+blend YUV422	OSDWIN0MD /OSDATRMD	Controls the display, zoom on/off control of OSD window 0.If attribute mode is enabled,OSDATRMD controls blend + blink of OSD Window 0
VID1	4	Video	YUV422,YUV420	VIDWINMD	Controls the display, zoom on/off control of Video Windows
VID0	5	Video	YUV422,YUV420	VIDWINMD	Controls the display, zoom and on/off control of Video windows

Figure 40. OSD Window Display Priorities

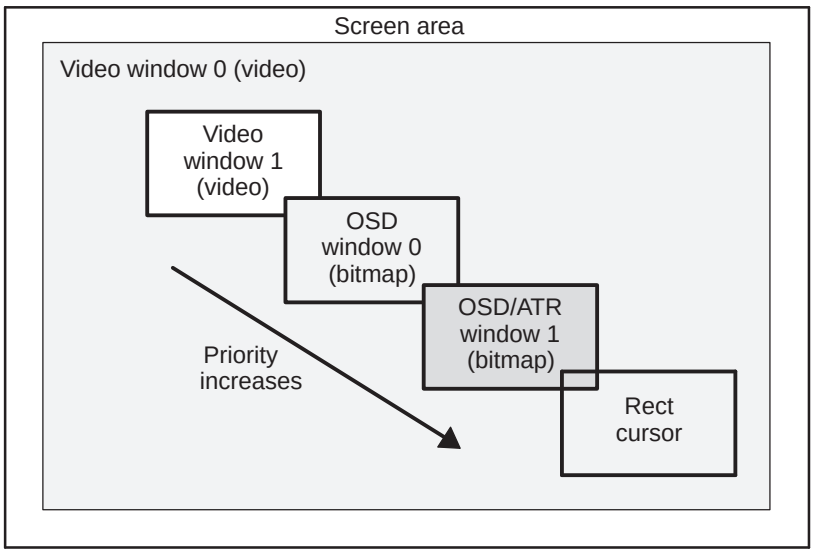


Table 31. Functional Description of the OSD Windows

Function	Video0	Video1	Bitmap0	Bitmap1	H/W Cursor
Blend with 8 steps	√ (Higher one of video windows)		√ (Higher one of bitmap windows)		x (paste only)
Independent display	√	√	√	√	√
Duplicational display	x	x	x	√	√
Color look-up table ROM and RAM	x	x	√	√	√
Blinking with programmable interval	x	x	√ (with attribute mode of bitmap window 1)		x
Pixel level blending factor	x	x	√ (with attribute mode of bitmap window 1)		x
RGB565 and RGB888 mode support	x	x	√	√	x
1/2/4/8-bit/pixel bitmap support	x	x	√	√	8-bit supported
Rescaling on horizontal x2/x4	√	√	√	√	x
Rescaling on vertical x2/x4	√	√	√	√	x
Rescaling on horizontal x1. 125/1.5	√ (Higher one of video windows)		√ (Higher one of bitmap windows)		x
Rescaling on vertical x1.2	√ (Higher one of video windows)		√ (Higher one of bitmap windows)		

4.4.1 Video Window Constraints

- Video Window 0 : Use video window 0 for HD display
- Video Window 1 : Depending on the application, video window 1 may need to be turned off due to probable bandwidth constraint.

4.4.2 OSD Configuration and Control

Many of the OSD registers contain bits that are latched by the VD signal, which is the vertical sync pulse generated by the device's Video Encoder module. Data written to a latched bit does not take affect until the VD pulse is received. This allows registers that control the OSD, such as the SDRAM data address, display window size, display zoom configuration, etc., to be changed between successive VD pulses without corrupting the current display. In the OSD register descriptions, bit fields marked with (*) are latched by the VD signal.

4.4.2.1 DDR Addresses

The location of data stored in DDR is defined by several memory-mapped registers. The DDR addresses are specified as an offset for the start of DDR in units of 32-byte burst.

Table 32. OSD SDRAM Address Registers

SDRAM Address Register	Window
VIDWIN0ADL	Video window 0 address (low 16 bits)
VIDWIN1ADL	Video window 1 address (low 16 bits)
VIDWINADH	Video window addresses (upper bits)
OSDWIN0ADL	OSD bitmap window 0 address (low 16 bits)
OSDWIN1ADL	OSD bitmap window 1/attribute window address (low 16 bits)
OSDWINADH	OSD bitmap window addresses (upper bits)

4.4.2.2 DDR Offsets

The offset registers specify the address offset between each horizontal line of display data. Since this is independent of the window display size, this allows a subset of an image to be displayed. The offset is in units of 32 bytes. Thus, the width of each line of data stored in DDR must be a multiple of 32 bytes. If the width of data is not a multiple of 32 bytes, then it must be padded when stored in DDR.

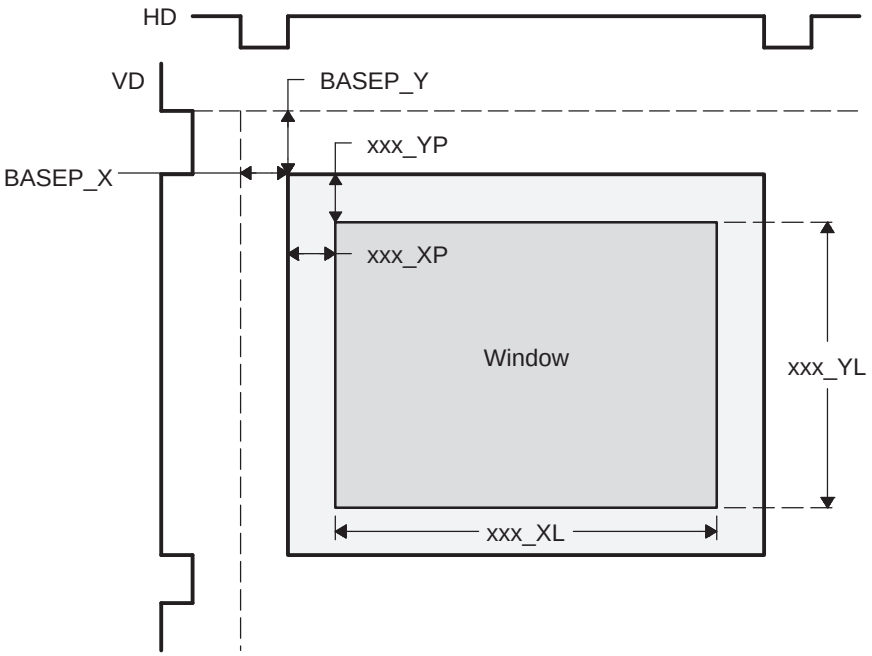
Table 33. OSD SDRAM Offset Registers

SDRAM Address Register	Window
VIDWIN0OFST	Video Window 0 SDRAM offset register
VIDWIN1OFST	Video Window 1 SDRAM offset register
OSDWIN0OFST	OSD Bitmap Window 0 SDRAM offset register
OSDWIN1OFST	OSD Bitmap Window 1/Attribute Window SDRAM offset register

4.4.2.3 Window Positioning

All windows use a common reference pixel (base pixel). The position of this pixel is determined from the beginning of the video encoder HD and the beginning of the video encoder VD signal. For each window (video, bitmap, and cursor), the location of the upper left corner is specified, along with the horizontal and vertical display sizes. The relationship of the display positions of each window is shown in Figure 41.

Figure 41. OSD Window Positioning



Window start position is specified with respect to the BASEP_X and BASEP_Y position. Window start position in X-direction and window width is specified in units of pixels. Window start position in Y-direction and window height is specified in units of lines. When the VENC is in interlaced mode, window vertical position and height (*YP and *YL registers) are defined in terms of display lines in each field. When the VENC is in progressive mode, window vertical position and height (*YP and *YL) registers are defined in terms of display lines in the progressive frame. Table 34 shows the register used for window position and size.

Table 34. OSD Window Positioning Registers

Window Positioning Registers	Window
VIDWIN0XP VIDWIN0YP VIDWIN0XL VIDWIN0YL	Video Window 0 start position and size registers
VIDWIN1XP VIDWIN1YP VIDWIN1XL VIDWIN1YL	Video Window 1 start position and size registers
OSDWIN0XP OSDWIN0YP OSDWIN0XL OSDWIN0YL	OSD Bitmap Window 0 start position and size registers
OSDWIN1XP OSDWIN1YP OSDWIN1XL OSDWIN1YL	OSD Bitmap Window 1/Attribute Window start position and size registers
CURXP CURYP CURXL CURYL	Hardware cursor start position and size registers

4.4.2.4 Window Mode - Field/Frame

Each video and bitmap window has two display modes: field mode and frame mode (VIDWINMD.VFF*n*, OSDWINnMD.OFF*n*). Table 35 shows the registers used for the window modes. The field/frame mode setting describes how the display data is organized in and read from DRAM, as shown in Table 36.

Table 35. OSD Field/Frame Mode Registers

Register.Field	Description
VIDWINMD.VFF0	Video Window 0 Field/Frame specification
VIDWINMD.VFF1	Video Window 1 Field/Frame specification
OSDWIN0MD.OFF0	OSD Bitmap Window 0 Field/Frame specification
OSDWIN1MD.OFF1	OSD Bitmap Window 1 Field/Frame specification
OSDATRMD.OFFA	OSD Attribute Window Field/Frame specification (same address/offset as for OSD Bitmap Window 1)

Table 36. Window Mode Description

Window Mode	Display Field	Initial Data	Line Increment	VENC Mode	Window Height Register	Display Usage
Frame	Top	Start Address	2 × Offset	Interlaced	Field Height (1/2 display height)	Progressive data to interlaced display device
	Bottom	Start Address + Offset	2 × Offset			
Field		Start Address	Offset	Interlaced	Field Height (1/2 display height)	Field data is line doubled
Field		Start Address	Offset	Interlaced	Field Height (full display height)	Progressive frame to progressive display

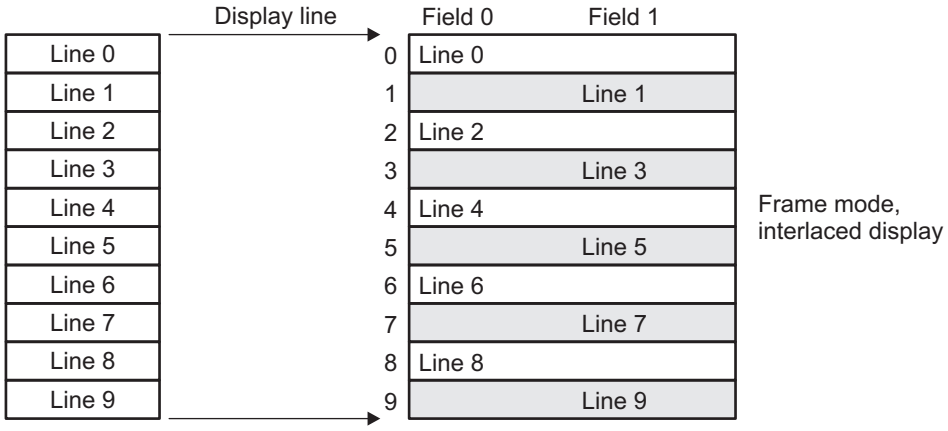
4.4.2.4.1 Frame Mode

Frame mode (Figure 42) allows a progressive frame of data (full vertical resolution) stored in DRAM and data is read sequentially, beginning from the start address and skipping every other line by incrementing by 2× the offset each line.

The readout for the second field is started at an offset of 1 line from the start address.

If the VENC is in interlaced mode (standard TV out mode), different data is read for each field and the full progressive frame is output on each even/odd field pair. In this case, the window height registers are programmed to the number of lines in each field; that is, the number of lines the VENC reads for each VSYNC (field) = 1/2 the display height.

Figure 42. OSD Window Frame Mode



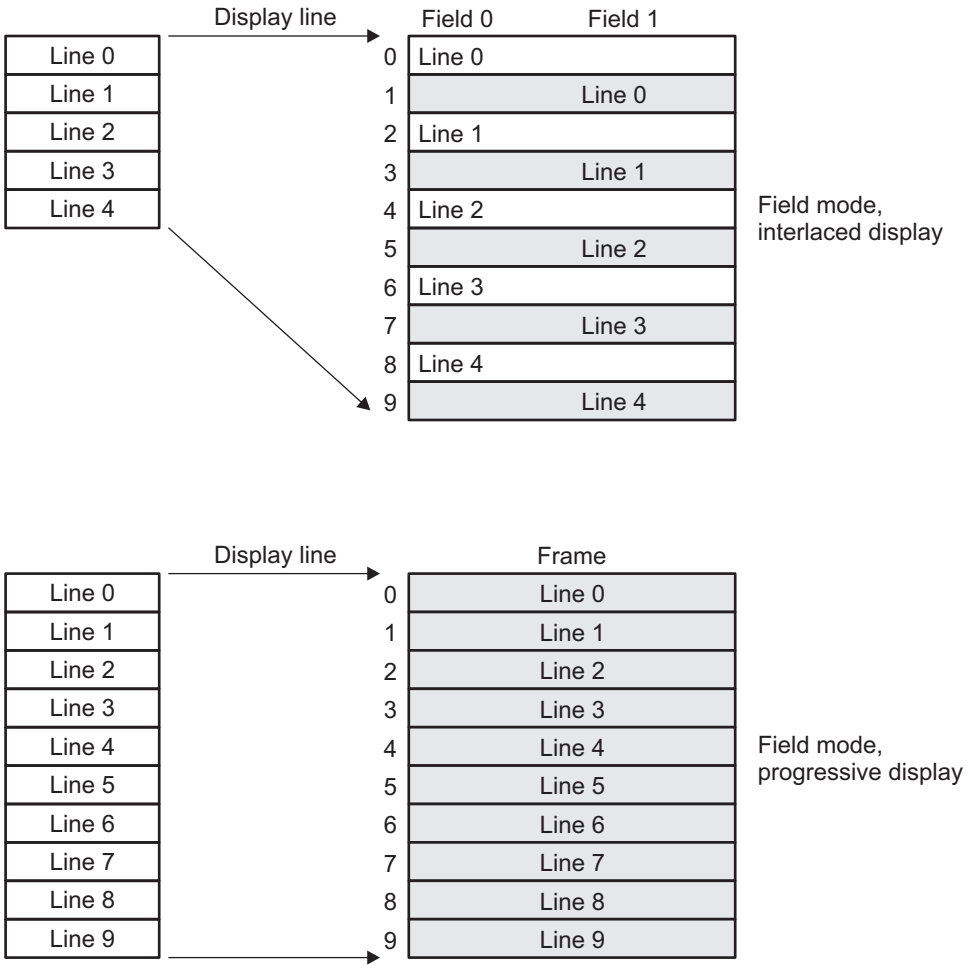
4.4.2.4.2 Field Mode

Field mode (Figure 43) assumes a single display field is stored in DRAM and data lines are read sequentially, beginning from the start address, and incrementing by the offset each line, and repeating for each field (or frame).

If the VENC is in interlaced mode (standard TV out mode), the same data is read twice for each field. This results in each line being displayed twice, once for each field (line-doubled). In this case, the window height registers are programmed to the number of lines in each field (i.e., the number of lines the VENC reads for each VSYNC (field) = 1/2 the display height). Alternately, if interlaced video frames are to be displayed, for instance from a video decode operation, the start address can be altered at each VSYNC to ping-pong between the two actual video fields and output the interlaced data to the interlaced display output.

If the VENC is in progressive mode, then field mode should be used so that all data is read from DRAM progressively so that each line is displayed once per progressive frame. In this case, window height registers are programmed to the number of lines in each progressive frame (i.e., the number of lines the VENC reads for each VSYNC (frame) = full display height).

Figure 43. OSD Window Field Mode



4.4.2.5 Window Scaling

The OSD has two rescaling methods. Window zooming is based on pure pixel/line copy for x2 and x4 rescaling. Zooming can be applied to each window independently. The other scaling method is based on linear interpolation between pixels for x9/8 and x3/2 in horizontal direction and x6/5 in vertical direction.

Horizontal x9/8 rescaling is provided for up-sampling of VGA (640) sized windows to 720 pixels for NTSC/PAL analog displays, which shrink the effective display by 8/9 when displayed on a TV. The horizontal rescaling function of x3/2 is provided for specific LCD panels displaying 960 pixels horizontal.

Vertical x6/5 rescaling is provided for up-sampling of VGA/NTSC-sized windows (480 lines) to 576 lines for usage of PAL-based TV displaying. Notice that these scaling functions are applied to a window type (i.e., both video or both bitmap windows) and the user cannot configure different rescaling ratios for each window of the same type (video and bitmap window rescaling can be configured to be different from each other). Also, a combination of rescaling and zoom methods (x9/8, x3/2 horizontal rescaling / x6/5 vertical rescaling / x2 and x4 horizontal and vertical zoom) is possible.

The combined usage of the scaling / zoom function is described by taking actual usage that can be expected with common sense. The usage matrix of scaling and zoom function is shown in Table 37. The relationship between the source picture size and displayed picture size has some limitations as mentioned here.

Table 37. Functional Matrix of Scaling and Zoom

Output Source	960(h) x 480(v)	960(h) x 576(v)	720(h) x 480(v)	720(h) x 576(v)
VGA (640(h) x 480(v))	√ (x1.5(h))	√ (x1.5(h)x1.2(v))	√ (x1.125(h))	√ (x1.125(h)x1.2(v))
NTSC D1(720(h) x 480(v))	x	x	√	√ (x1.2(v)
PAL D1(720(h) x 480(v))	x	x	x	√
3/4 VGA (480(h) x 480(v))	√ (x2(h))	√ (x2(h)x1.2(v))	√ (x1.5(h))	√ (x1.5(h)x1.2(v))
1/2 VGA (320(h) x 480(v))	√ (x2(h)x1.5(h))	√ (x2(h)x1.5(h)x1.2(v))	√ (x2(h)x1.125(h))	√ (x2(h)x1.125(h)x1.2(v))
1/4 VGA (320(h) x 240(v))	√ (x2(h)x1.5(h)x2(v)x2(v))	√ (x2(h)x1.5(h)x2(v)x1.2(v))	√ (x2(h)x1.125(h)x2(v))	√ (x2(h)x1.125(h)x2(v)x1.2(v))
1/2 QVGA (160(h) x 240(v))	√ (x4(h)x1.5(h)x2(v))	√ (x4(h)x1.5(h)x2(v)x1.2(v))	√ (x4(h)x1.125(h)x2(v))	√ (x4(h)x1.125(h)x2(v)x1.2(v))
1/4 QVGA (160(h) x 120(v))	√ (x4(h)x1.5(h)x4(v))	√ (x4(h)x1.5(h)x4(v)x1.2(v))	√ (x4(h)x1.125(h)x4(v))	√ (x4(h)x1.125(h)x4(v)x1.2(v))
3/4 D1 (544(h) x 480(v))	x	x	x	x
1/2 D1 (352(h) x 480(v))	x	x	x	x
1/4 D1 (352(h) x 240(v))	x	x	x	x

4.4.2.5.1 Window Zooming

The video windows and OSD bitmap windows can be zoomed along their horizontal and vertical directions by a factor of 2 or 4. Figure 44 shows the zoom process and the parameters that must be set up to execute a zoom. All of the registers used in the zoom process (Table 38) are latched by the VD signal so they can be safely updated any time.

- Set the starting DDR address of the area desired to be magnified, offset, zoom factor and the display window size. The OSD will take data, starting from the start address, to generate a magnified image that fits into the display window.
- Set the display position to the desired position of the window. Set the display height and display width to the desired magnified height and width.
- When zoom is enabled (VIDWINMD.VVZ*n*, VIDWINMD.VHZ*n*, OSDWIN*n*MD.OVZ*n*, OSDWIN*n*MD.OHZ*n*), data starting from the DDR start position will be magnified to fit into the display area specified by the display height and display width. For example, if the horizontal and vertical directions are set to 2× zoom and the display width and height are set to 640 × 480, then a 320 × 240 block of data starting from the DDR start position will be magnified to 640 × 480 in the display window.

Figure 44. OSD Window Zoom Process

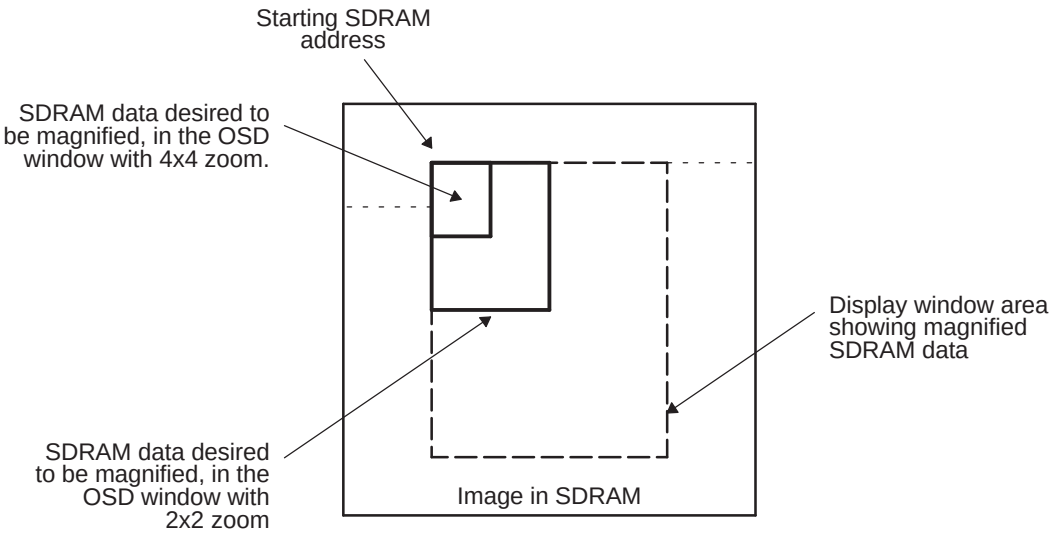


Table 38. OSD Window Zoom Registers

Register.Field	Description
VIDWINMD.VHZ0	Video Window 0 Horizontal Zoom
VIDWINMD.VVZ0	Video Window 0 Vertical Zoom
VIDWINMD.VHZ1	Video Window 1 Horizontal Zoom
VIDWINMD.VVZ1	Video Window 1 Vertical Zoom
OSDWIN0MD.OHZ0	Bitmap Window 0 Horizontal Zoom
OSDWIN0MD.OVZ0	Bitmap Window 0 Vertical Zoom
OSDWIN1MD.OHZ1	Bitmap Window 1 Horizontal Zoom
OSDWIN1MD.OVZ1	Bitmap Window 1 Vertical Zoom

4.4.2.5.2 Window Scaling - Square Pixels for NTSC/PAL Analog Output or Display Matching

The analog NTSC/PAL output video signals are spatially compressed. As a result, the OSD has an option to horizontally and vertically expand the video and bitmaps windows to counteract the spatial compression in the video signal. In addition, there are options to smooth the expanded video window data. Table 39 shows the registers used for window expansion.

- NTSC analog output is compressed 8/9 horizontally
  - 720 × 480 input appears as 640 × 480 (6:4 aspect ratio source data appears as 4:3)

  - Solution (example)-Use 640 × 480 source material with 9/8 horizontal expansion (MODE.VHRSZ and MODE.OHRSZ) and window display size set to 720 × 480, which will appear as 640 × 480.
  - If EXTMODE.EXPMDSEL = 1, then use EXTMODE.SCRNHEXP (applies to all windows).
- PAL analog output is compressed 8/9 horizontally and 5/6 vertically
  - 720 × 576 input appears as 640 × 480
  - Solution (example)-Use 640 × 480 source material with 9/8 horizontal expansion (MODE.VHRSZ and/or MODE.OHRSZ) and 6/5 vertical expansion (MODE.VVRSZ and/or MODE.OVRSZ) and window display size set to 720 × 576, which will appear as 640 × 480.
  - If EXTMODE.EXPMDSEL = 1, then use EXTMODE.SCRNVEXP (applies to all windows).
- Display scaling to 960 wide LCD
  - Must set: MODE.VHRSZ and/or MODE.OHRSZ to 0
  - Must set: EXTMODE.EXPMDSEL = 0
  - Then enable with EXTMODE.VIDHRSZ and EXTMODE.OSDHRSZ

Table 39. Normal OSD Window Expansion Registers

Register.Field	Description
MODE.VHRSZ	Video Window Horizontal 9/8 Expansion
MODE.VVRSZ	Video Window Vertical 6/5 Expansion
MODE.V0EFC	Video Window 0 smoothing filter enable (with MODE.EF)
MODE.V1EFC	Video Window 1 smoothing filter enable (with MODE.EF)
MODE.EF	Video Window smoothing filter (maximum line width is 720)
MODE.OHRSZ	Video Window Horizontal 9/8 Expansion
MODE.OVRSZ	Video Window Vertical 6/5 Expansion

Table 40. Extended OSD Window Expansion Registers

Register.Field	Description
EXTMODE.EXPMDSEL	Sets filtering mode before expansion
EXTMODE.SCRNHEXP	Global H expansion on all windows
EXTMODE.SCRNVEXP	Global V expansion for all windows
EXTMODE.OSDHRSZ15	Bitmap window 1.5x expansion if normal filtering done
EXTMODE.VIDHRAZ15	Video window 1.5x expansion if normal filtering done

4.4.2.5.3 Zoom and Expansion Filter Usage

Table 41 shows the usage of the zoom and expansion filters. Note that the vertical expansion filter has a higher priority than the vertical zoom filter. If you configure both the zoom and expansion filters tobe active, the OSD module can perform only the expansion filter for the vertical direction due to limitations in the design.

Additionally, if you configure EXTMODE.EXPMDSEL = 1 (post-blend mode), you can perform only the expansion filter (no zoom filter). This fact means that only screen-level filtering is valid in post-blend mode. Window-level filtering is impossible in post-blend mode.

Table 41. Zoom and Expansion Filter Usage

Performance Expand Filter (MODE.EF)	Description of Detailed Performance
ON (MODE.EF = 1)	All interpolation filters perform in both horizontal and vertical direction. (Also both of zoom (x2/x4) and expansion (x9/8h, x3/2h, x6/5v). Additionally; H(On, On) and V(On, On)) In combined performance of vertical zoom and vertical expansion, filter is active for expansion only.

Table 41. Zoom and Expansion Filter Usage (continued)

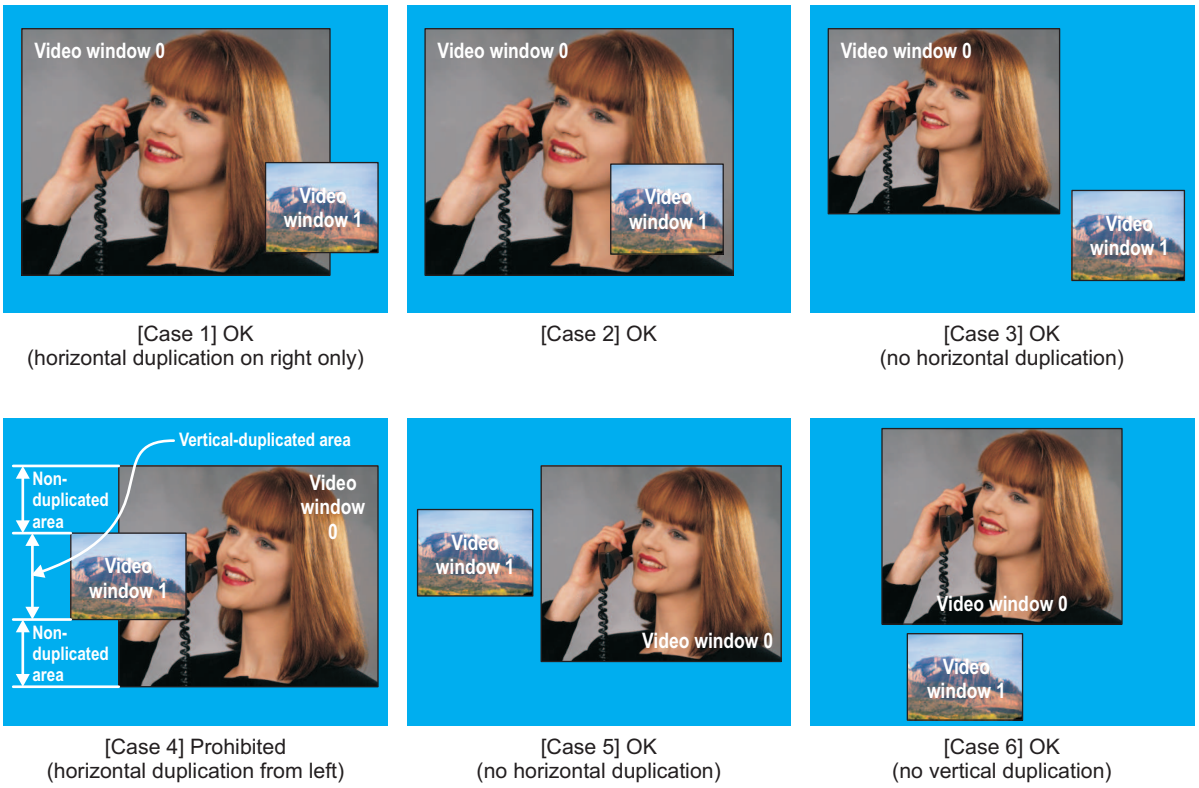
Performance Expand Filter (MODE.EF)	Description of Detailed Performance			
OFF (MODE.EF = 0)	Filter SW (H) (EXTMODE.EXPFILVEN)	ON	zoom_SW(h) ON EXTMODE.ZMFILV1HEN EXTMODE.ZMFILV0HEN	Interpolation filter is active in zoom function. Also, expansion filter is active (source is result of zoom function).
			zoom_SW(h) OFF EXTMODE.ZMFILV1HEN EXTMODE.ZMFILV0HEN	No interpolation (only pixel copy) is executed in zoom function. Expansion filter is active (source is result of zoom function).
		OFF	zoom_SW(h) ON EXTMODE.ZMFILV1HEN EXTMODE.ZMFILV0HEN	Interpolation filter is active in zoom function. Expansion filter is inactive; just pixel copy is executed (source is result of zoom function).
			zoom_SW(h) OFF EXTMODE.ZMFILV1HEN EXTMODE.ZMFILV0HEN	No interpolation (only pixel copy) is executed in zoom function. Expansion filter is inactive, just pixel copy is executed (source is result of zoom function).
	FILTER SW (V) (EXTMODE.EXPFILHEN)	ON	zoom_SW(v) ON EXTMODE.ZMFILV1VEN EXTMODE.ZMFILV0VEN	No interpolation (only pixel copy) is executed in zoom function. Expansion filter is active (source is result of zoom function).
			zoom_SW(v) OFF EXTMODE.ZMFILV1VEN EXTMODE.ZMFILV0VEN	
		OFF	zoom_SW(V) ON EXTMODE.ZMFILV1VEN EXTMODE.ZMFILV0VEN	Interpolation filter is active in zoom function. Expansion filter is inactive, just pixel copy is executed. (source is result of zoom function)
			zoom_SW(v) OFF EXTMODE.ZMFILV1VEN EXTMODE.ZMFILV0VEN	No interpolation filter (only pixel copy) is executed in zoom function. Expansion filter is inactive, just pixel copy is executed. (source is result of zoom function).

4.4.2.5.4 Window Positioning Limits for When Using Horizontal Expansion

When using horizontal expansion (x9/8 or x3/2), there are some limitations on window positioning and layout. Figure 45 describes the limitation on the location and layout of each window when horizontal expansion is used. These limitations apply only between windows of the same type (Video Window 0 and Video Window 1, or Bitmap Window 0 and Bitmap Window 1).

Windows of the same type can be located independently if there is no overlap / duplication or if Window 1 is fully contained within Window 0. Window 1 can overlap on the right side of Window 0. However, Window 1 cannot overlap the left side of Window 0. This limitation is only present when horizontal expansion (x9/8 and x3/2) is used.

Figure 45. OSD Window Zoom Process



4.4.2.5.5 Vertical Boundary Processing

When using vertical expansion (x6/5) with filtering, filtering is not applied at the lower boundary line of Window 1 in cases 1, 2, and 4 in Table 42. This is because the expansion method used in each window is different (start line is different) and the line is repetitively read from different positions and, as a result, the lower boundary between the windows will appear improper. In this case, the user can prevent or control filtering on the edge of the window.

Table 42. Vertical Boundary Filtering Control Registers

Register Field	Description
VBNDRY. VBNDRYPRCSEN	Enables video boundary processing
VBNDRY. VFILINCMD	Turn ON to have vertical filtering increment past the end of the vertical display area. In this case, additional data to be processed for vertical filtering should be stored in SDRAM, immediately following the display data. Turn OFF to have vertical filtering stop incrementing when it reaches the last display line. This is the DM320 equivalent mode.

4.4.2.6 OSD Background Color

The background color can be specified in terms of the color lookup tables. This color is displayed in regions of the combined OSD display area that do not have an overlapping window. Table 43 shows the registers used for OSD background color.

Table 43. OSD Background Color Registers

Register.Field	Description
MODE.BCLUT	Selects the color lookup table to be used (ROM or RAM). Note that there are two ROM tables and the selection for the other windows also applies here (MISCCTL.RSEL).
MODE.CABG	Background color. 8-bit offset into color lookup table.

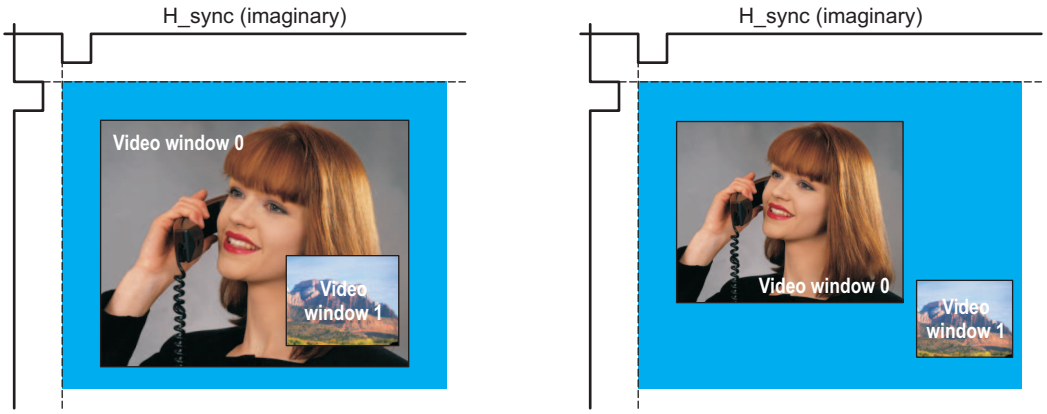
4.4.3 Video Windows

The device supports two video windows (VIDWIN0 and VIDWIN1) that can be displayed simultaneously. Data referenced by each Video window is read from external memory and displayed within the two windows.

Note that both picture-in-picture (PIP) and independent displays are supported.

Note also that blending on video window 1 (VIDWIN1) and video window 0 (VIDWIN0) is not supported.

Figure 46. Video Window Display Options



DM36x OSD Video window supports YUV420 format in addition to conventional YUV422 format. YUV420 format is selected by setting YC420 of MISSCTL register to 1. Both non-interlaced and interlaced data formats are supported. Figure 48 describes the 422 and 420 data formats in external memory.

Note that since each horizontal line of window data must be a multiple of 32-bytes, video windows data must contain a multiple of 32-bytes /pixel = 32-pixels per horizontal line.

For YC420, even if the display data is single video/image, both VIDWIN0 and VIDWIN1 parameters must be used. The start address of Y data plane and C data plane is configured in VIDEOWIN0ADH/L and VIDEOWIN1ADH/L respectively. The following parameters should be same value.

VIDWIN0XP = VIDWIN1XP

VIDWIN0YP = VIDWIN1YP

VIDWIN0XL = VIDWIN1XL

VIDWIN0YL = VIDWIN1YL

VIDWIN0OFST = VIDWIN1OFST

VIDWINMD [9:8] = VIDWINMD [1:0]

Note that any zoom function is not supported for YC420 format.

OSD window data is always packed into 32-bit words and left-justified. Starting from the upper left corner of the OSD window, all data will be packed into adjacent 32-bit words. Figure 47 shows data format window data in SDRAM.

Figure 47. Pixel Arrangement in the Display

Left, Top

P0	P1	P2	P3	P4	P5	P6	P7 ...

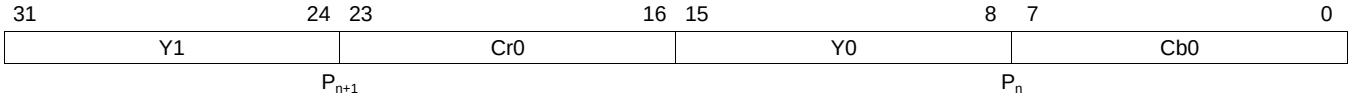
4.4.3.1 Video Window Data - YUV422 Format

OSD video window data is in YCbCr 4:2:2 or 4:2:0 format. Note that the order of the Cb and Cr data is dependent on MODE.CS (chroma swap). Figure 48 describes the default case of Cb/Cr order.

Since each horizontal line of window data must be a multiple of 32 bytes, video window data must contain a multiple of 32 bytes/2 bytes/pixel = 16 pixels per horizontal line.

Figure 48. Video Data Format - YUV422

(a) 16-bits per pixel, 32-bit pixel pair with combined Chroma



(b) SDRAM format

Address	31	16	15	0
N	P1		P0	
N + 1	P3		P2	
N + 2	P5		P4	
...	...		...	

4.4.3.2 Expansion and Anti-Flicker Filter for Video Window

The OSD module has a two-tap linear filter for the video window. This is useful when using horizontal and vertical expansion for reduction of flicker noise due to display rate conversion such as 60i display from 30 Hz frame data that are field-based. This section also describes configuration options of this filtering function.

Table 44. Expansion and Anti-Flicker Filter for Video Window

Register.Field	Description
MODE.EF	Expansion filter enable. Only use when EXTMODE.EXPMDSEL = 0
WIDWINMD.VFINV	Inverts application of the two sets of expansion filter coefficients between field 0 and field 1.
WIDWINMD.VnEFC	Enables different anti-flicker coefficients for each field
EXTMODE.EXPMDSEL	Extended mode expansion filtering mode select
EXTMODE.ZMFILVnVEN	Extended mode - video window n vertical zoom filter type (x6/5)
EXTMODE.ZMFILVnHEN	Extended mode - video window n horizontal zoom filter type
EXTMODE.EXPFILHEN	Extended mode - video window horizontal expansion filter enable (x9/8, x1/5)
EXTMODE.EXPFILVEN	Extended mode - video window vertical expansion filter enable (x6/5)

4.4.3.2.1 Video Window Filtering - Horizontal Direction

In the horizontal direction, this filter operates only if x2/x4 zoom-up function or x1.5/x9/8 rescaling functions are enabled. Configuration and processing details are described in this section.

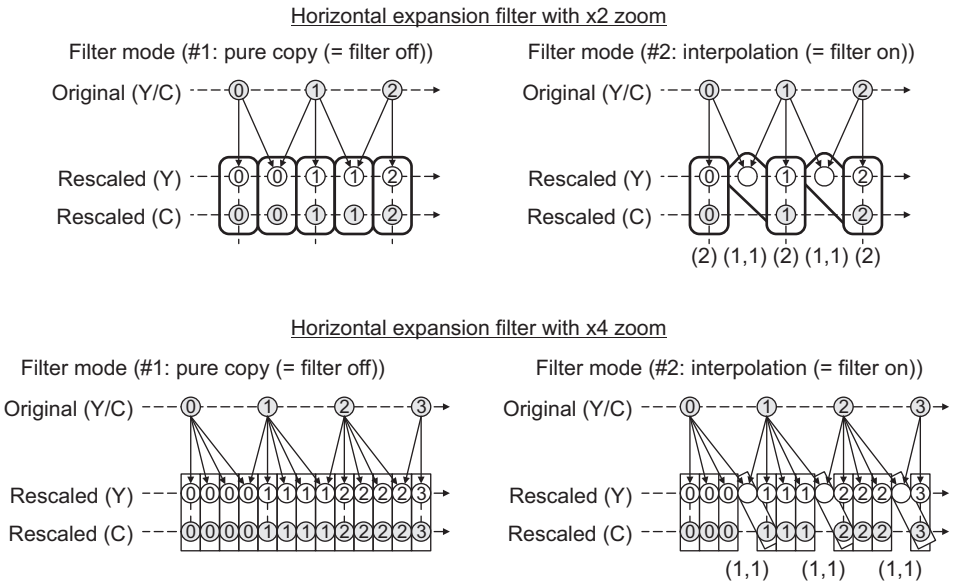
4.4.3.2.1.1 Horizontal x2/x4 Zoom-Up Filter

In this case, the filtering function is only interpolating a pixel value for the new pixel at the boundary of the resized pixels. All other pixels are duplicated.

Table 45. Filtering Configuration for Horizontal x2/x4 Zoom

Filter Mode #1		Filter Mode #2	
Normal			
Register. Field	**Value**	**Register. Field**	**Value**
MODE.EF	0	MODE.EF	1
Extended			
Register. Field	**Value**	**Register. Field**	**Value**
MODE.EF	0	MODE.EF	0
EXTMODE.ZMFILVnHEN	0	EXTMODE.ZMFILVnHEN	1

Figure 49. Filtering Method for Horizontal x2/x4 Zoom



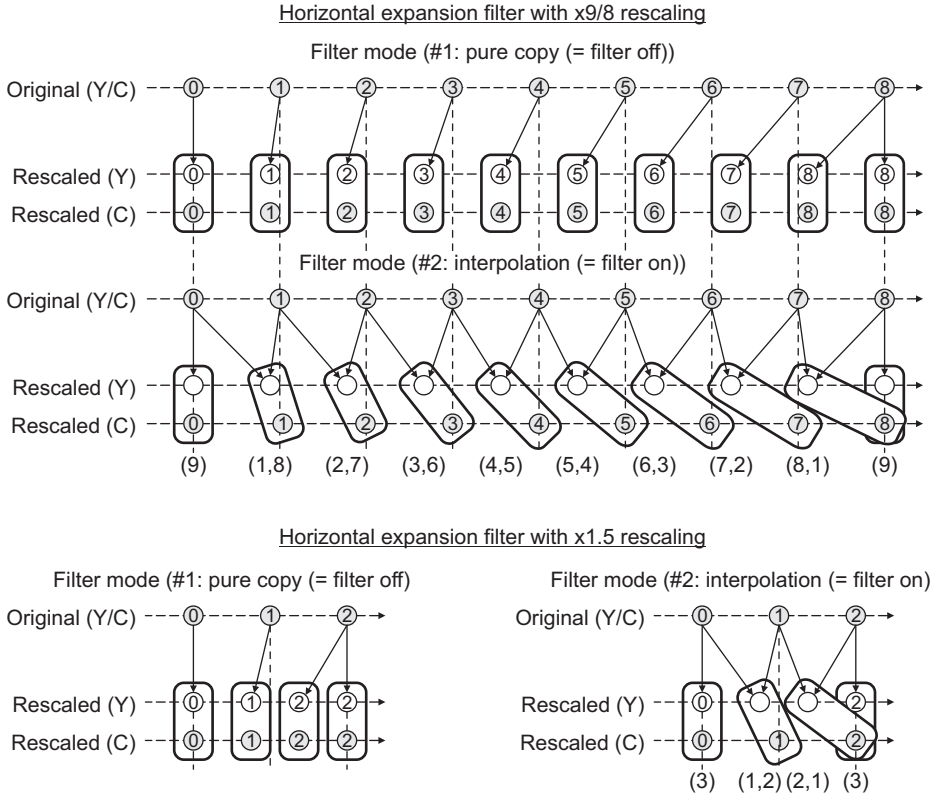
4.4.3.2.1.2 Horizontal x1.5 (3/2)/x1.125 (9/8) Rescaling Filter

In this case, the filtering function is a linear interpolation.

Table 46. Filtering Configuration for Horizontal x1.5/x1.125 Expansion

Filter Mode #1		Filter Mode #2	
Normal			
Register. Field	**Value**	**Register. Field**	**Value**
MODE.EF	0	MODE.EF	1
Extended			
Register. Field	**Value**	**Register. Field**	**Value**
MODE.EF	0	MODE.EF	0
EXTMODE.ZMFILVnHEN	0	EXTMODE.ZMFILVnHEN	1

Figure 50. Filtering Method for Horizontal x1.5/x1.125 Zoom



4.4.3.2.2 Video Window Filtering - Vertical Direction

In the vertical direction, this filter operates only when x1/x2/x4 zoom or x1.5(x6/5) scaling is active (x1 zoom-up is only for field rate conversion).

4.4.3.2.2.1 Vertical x1 Anti-Flicker (Expansion) Filter (Field Rate Conversion)

This case applies when a field-based image is displayed as 60i image (i.e., data for each 60i field is the same). In this case, the filtering function is effective to reduce flicker noise.

Table 47. Table 37. Vertical x1 Anti-Flicker Filter Control Registers

Register Field	Value			
WIDWINMD.FSINV or WIDWINMD.VFINV	1			
WIDWINMD.VnEFC	0 or 1			

Figure 51. Filtering Method for Vertical x1 Expansion (Same Data Each Field)

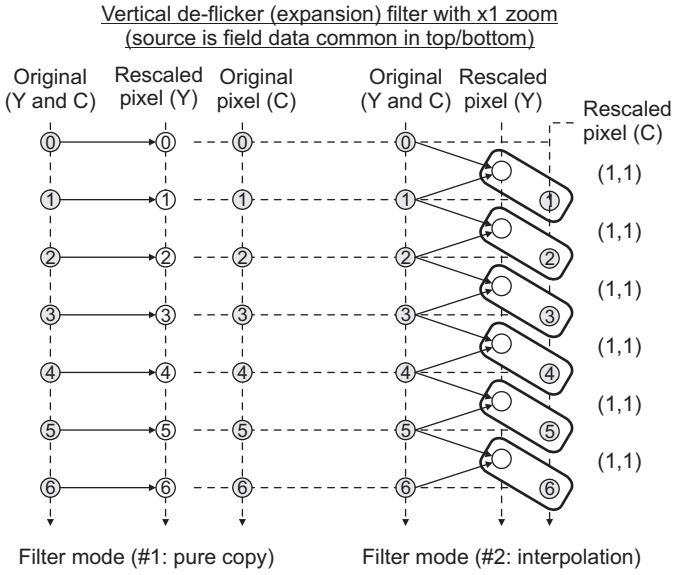


Table 48. Operation of Vertical x1 Anti-Flicker Filter Control Registers

Invert bit (VIDWINMD.VFINF or MODE.FSINV) Expand Filter (V)	0		1	
Coefficient bit (VIDWINMD.VnEFC)	Different (due to same field source)			
ON	FID = 0	1	FID = 0	2
	FID = 1	2	FID = 1	1
OFF	FID = 0	1	FID = 0	1
	FID = 1	1	FID = 1	1

4.4.3.2.2.2 Vertical x1 Anti-Flicker (Expansion) Filter (Without Field Rate Conversion)

This case applies when source image top and bottom are stored in SDRAM and displayed as a 60i image (i.e., data for each 60i field is unique). In this case, the filtering function is not applied.

Table 49. Operation of Vertical x1 Anti-Flicker Filter Control Registers

Invert bit (VIDWINMD.VFINF or MODE.FSINV) Expand Filter (V)	0		1	
Coefficient Bit (VIDWINMD.VnEFC)	Same (due to different field source)			
ON	FID = 0	1	FID = 0	1
	FID = 1	1	FID = 1	1
OFF	FID = 0	1	FID = 0	1
	FID = 1	1	FID = 1	1

4.4.3.2.2.3 Vertical x1 Anti-Flicker (Expansion) Filter (Frame Source Data Case)

This case applies when any frame-based image is displayed. In this case, the filtering function is not applied

Figure 52. Filtering Method for Vertical x1 Expansion (Frame Data)

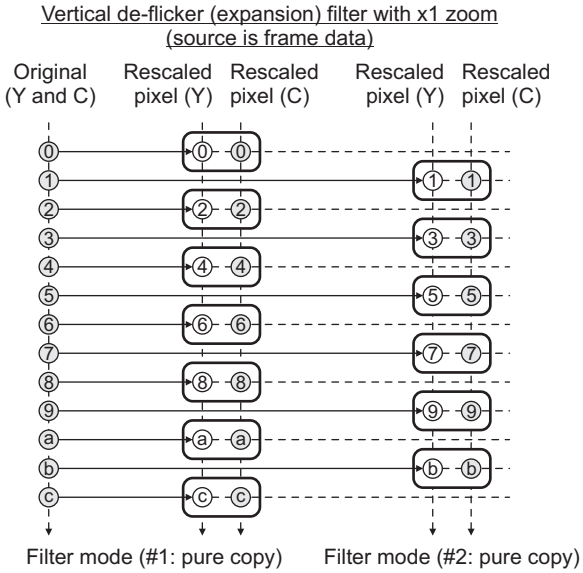


Table 50. Operation of Vertical x1 Anti-Flicker Filter for Frame Mode

Invert bit (VIDWINMD.VFINF or MODE.FSINV) Expand Filter (V)	0		1	
Coefficient bit (VIDWINMD.VnEFC)	Different (due to same field source)			
ON	FID = 0	1	FID = 0	2
	FID = 1	2	FID = 1	1
OFF	FID = 0	1	FID = 0	2
	FID = 1	2	FID = 1	1

4.4.3.2.2.4 Vertical x2 Zoom-Up Filter (Including Field Rate Conversion)

This case applies when a field-based image is displayed as 60i image (i.e., data for each 60i field is the same) with x2 vertical zoom. In this case, the filtering function is effective to reduce flicker noise.

Figure 53. Filtering Method for Vertical x2 Expansion (Same Data Each Field)

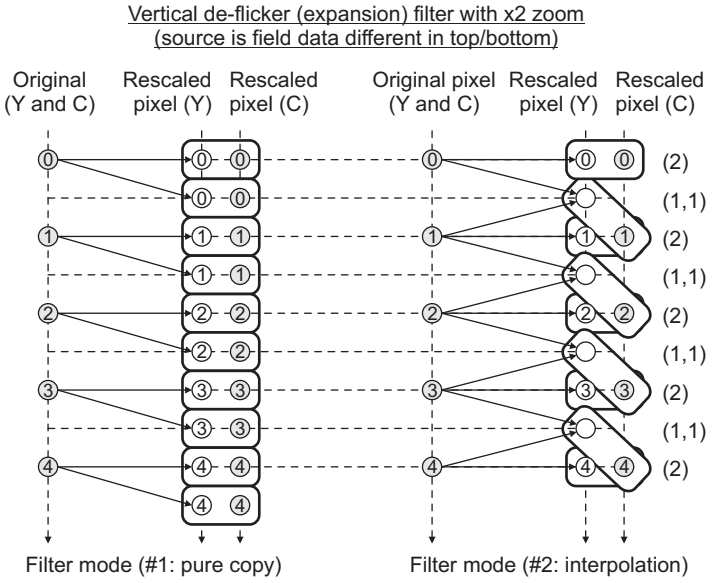


Table 51. Operation of Vertical x2 Anti-Flicker Filter for Field Mode

Invert bit (VIDWINMD.VFINF or MODE.FSINV) Expand Filter (V)	0		1	
Coefficient Bit (VIDWINMD.VnEFC)	Different (due to same field source)			
ON	FID = 0	1	FID = 0	2
	FID = 1	2	FID = 1	1
OFF	FID = 0	1	FID = 0	1
	FID = 1	1	FID = 1	1

4.4.3.2.2.5 Vertical x2 Zoom-Up Filter (Without Field Rate Conversion)

This case applies when source image top and bottom are stored in SDRAM and displayed as a 60i image (i.e., data for each 60i field is unique) and x2 zoom is applied. In this case, the filtering function is not applied.

Figure 54. Filtering Method for Vertical x2 Expansion (No Field Rate Conversion)

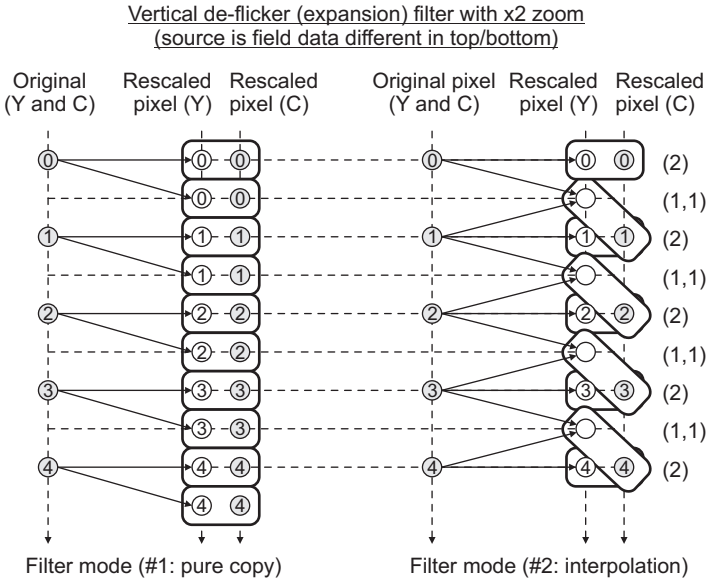


Table 52. Operation of Vertical x2 Anti-Flicker Filter (No Field Rate Conversion)

Invert bit (VIDWINMD.VFINF or MODE.FSINV) Expand Filter (V)	0		1	
Coefficient bit (VIDWINMD.VnEFC)	Same (due to different field source)			
ON	FID = 0	2	FID = 0	2
	FID = 1	2	FID = 1	2
OFF	FID = 0	1	FID = 0	1
	FID = 1	1	FID = 1	1

4.4.3.2.2.6 Vertical x2 Zoom-Up Filter (Frame Source Data Case)

This case applies when any frame-based image is displayed with x2 zoom. In this case, the filtering function is not applied. The interpolated value for filter mode #2 is derived from the average value between two pixels that surround the interpolated pixel data.

Figure 55. Filtering Method for Vertical x2 Expansion (Frame Data)

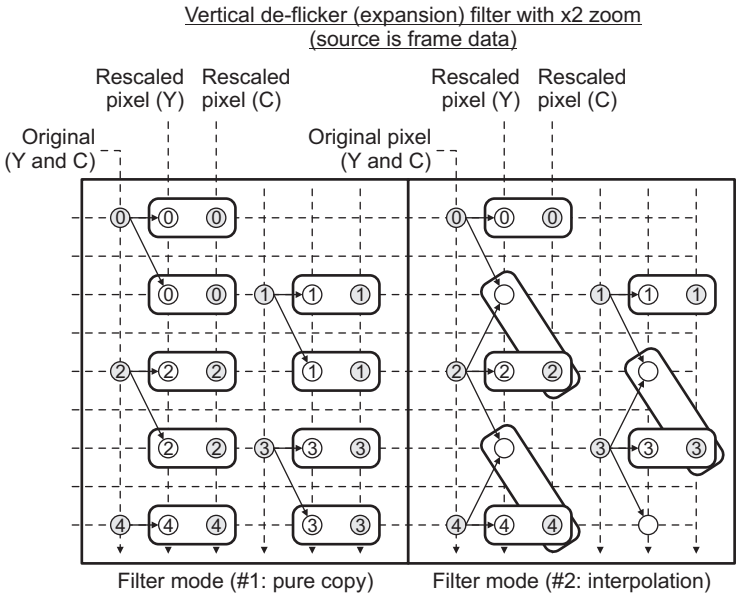


Table 53. Operation of Vertical x2 Anti-Flicker Filter for Frame Mode

Invert bit (VIDWINMD.VFINF or MODE.FSINV) Expand Filter (V)	0		1	
Coefficient bit (VIDWINMD.VnEFC)	Same (due to frame source)			
ON	FID = 0	1	FID = 0	2
	FID = 1	2	FID = 1	1
OFF	FID = 0	1	FID = 0	1
	FID = 1	1	FID = 1	1

4.4.3.2.2.7 Vertical x4 Zoom-Up Filter (Including Field Rate Conversion)

This case applies when a field based image is displayed as 60i image (i.e., data for each 60i field is the same) with x4 vertical zoom. In this case, the filtering function is effective to reduce flicker noise. Filter processing and configuration is described in this section.

Figure 56. Filtering Method for Vertical x4 Expansion (Same Data Each Field)

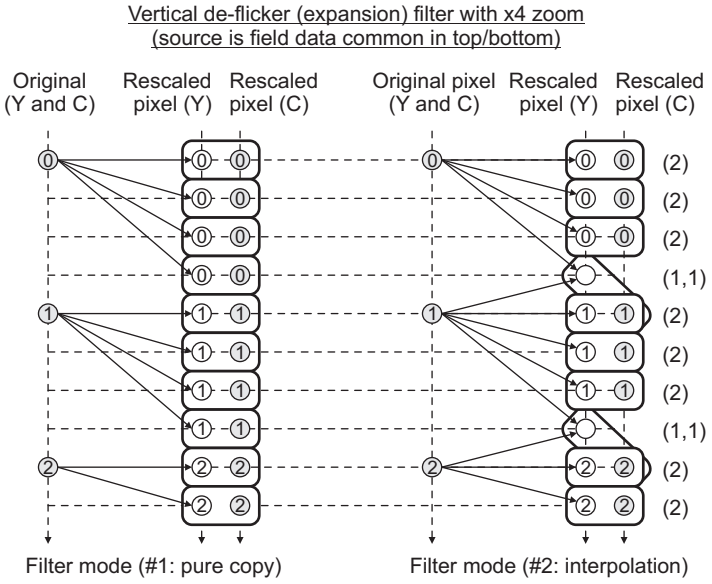


Table 54. Operation of Vertical x4 Anti-Flicker Filter for Field Mode

Invert bit (VIDWINMD.VFINF or MODE.FSINV) Expand Filter (V)	0		1	
Coefficient bit (VIDWINMD.VnEFC)	Different (due to same field source)			
ON	FID = 0	1	FID = 0	2
	FID = 1	2	FID = 1	1
OFF	FID = 0	1	FID = 0	1
	FID = 1	1	FID = 1	1

4.4.3.2.2.8 Vertical x4 Zoom-Up Filter (Without Field Rate Conversion)

This case applies when source image top and bottom are stored in SDRAM and displayed as a 60i image (i.e., data for each 60i field is unique) and x4 zoom is applied. In this case, the filtering function is not applied.

Figure 57. Filtering Method for Vertical x4 Expansion (No Field Rate Conversion)

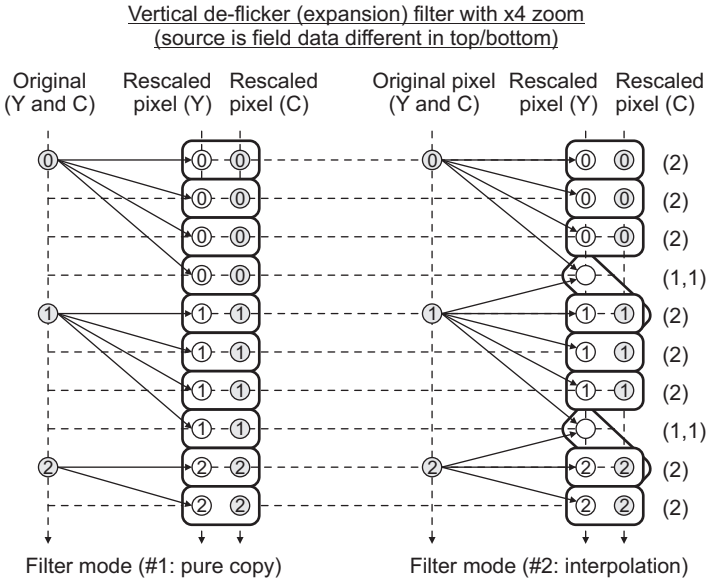


Table 55. Operation of Vertical x4 Anti-Flicker Filter (No Field Rate Conversion)

Invert bit (VIDWINMD.VFINF or MODE.FSINV) Expand Filter (V)	0		1	
Coefficient bit (VIDWINMD.VnEFC)	Same (due to different field source)			
ON	FID = 0	2	FID = 0	2
	FID = 1	2	FID = 1	2
OFF	FID = 0	1	FID = 0	1
	FID = 1	1	FID = 1	1

4.4.3.2.2.9 Vertical x4 Zoom-Up Filter (Frame Source Data Case)

This case applies when any frame based image is displayed with x4 zoom. In this case, the filtering function is not applied. The interpolated value for filter mode #2 is derived from the average value between two pixels that surround the interpolated pixel data.

Figure 58. Filtering Method for Vertical x4 Expansion (Frame Data)

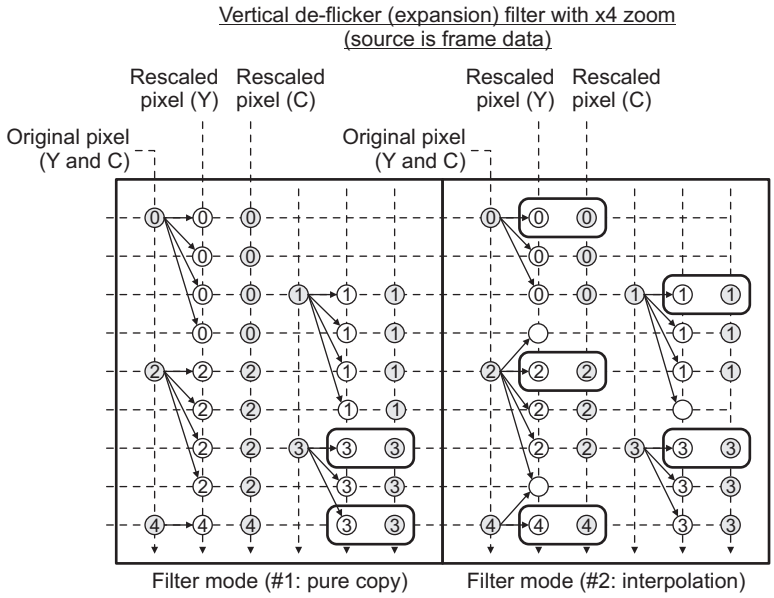


Table 56. Vertical x4 Anti-Flicker Filter for Frame Mode

Invert bit (VIDWINMD.VFINF or MODE.FSINV) Expand Filter (V)	0		1	
Coefficient bit (VIDWINMD.VnEFC)	Same (due to frame source)			
ON	FID = 0	2	FID = 0	2
	FID = 1	2	FID = 1	2
OFF	FID = 0	1	FID = 0	1
	FID = 1	1	FID = 1	1

4.4.3.2.2.10 Vertical x6/5 Anti-Flicker (Expansion) Filter

If the user configures vertical x1.2 expansion, this case is available. The user can select filter type with the configuration of the register based on the type of source data stored in SDRAM. The recommended type for each stored type of source data is:

- If source data is a field-based image and the source image of each field is the same, select only “different coefficient mode” so that the filter coefficients of top field processing are different from those used for bottom field processing.
- If source data is a field-based image and the source image of each field is stored in SDRAM, user can select either “same coefficient mode” or “different coefficient mode.” Because source data for top field is different from bottom field, the same filter coefficient can provide sufficient quality.
- If source data is a frame-based image, user can select either “same coefficient mode” and “different coefficient mode”. Because source data for top field is different from bottom field, the same filter coefficient can provide sufficient quality.

Figure 59. Filtering Method for Vertical x1.2 Expansion with No Zoom

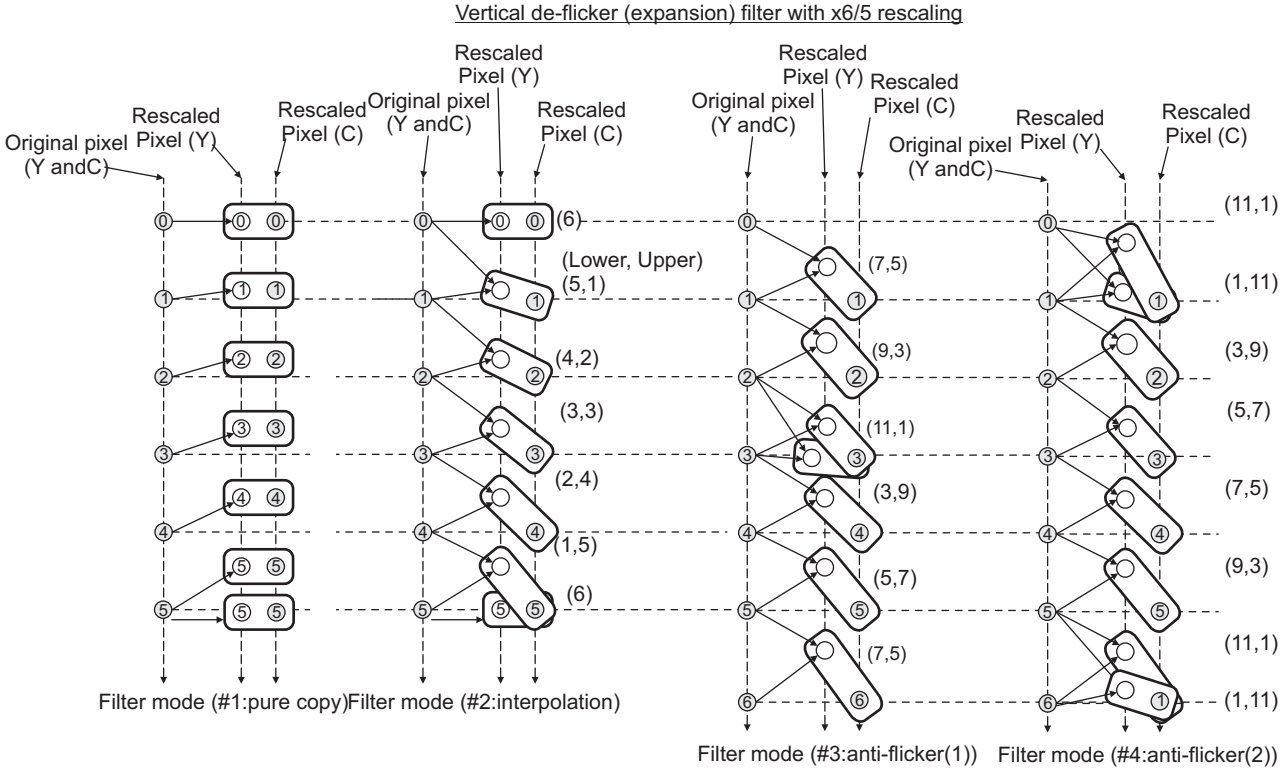


Table 57. Filtering Method for Vertical x1.2 Expansion with No Zoom

Invert bit Expand Filter (V)	0				1				0				1			
SDRAM Stored Mode	Field								Frame							
Coefficient Bit	Same		Different		Same		Different		Same		Different		Same		Different	
ON	FID = 0	2	FID = 0	2	FID = 0	2	FID = 0	3	FID = 0	2	FID = 0	2	FID = 0	2	FID = 0	4
	FID = 1	2	FID = 1	3	FID = 1	2	FID = 1	2	FID = 1	2	FID = 1	4	FID = 1	2	FID = 1	2
OFF	FID = 0	1	FID = 0	1	FID = 0	1	FID = 0	1	FID = 0	1	FID = 0	1	FID = 0	1	FID = 0	1
	FID = 1	1	FID = 1	1	FID = 1	1	FID = 1	1	FID = 1	1	FID = 1	1	FID = 1	1	FID = 1	1

The 1.2x vertical rescaling function can be also used with combination of x2/x4 zoom functions. Notice that the register configuration is the same as for x1.2 rescaling, only without zoom.

Figure 60. Filtering Method for Vertical x1.2 Expansion with 2x Zoom

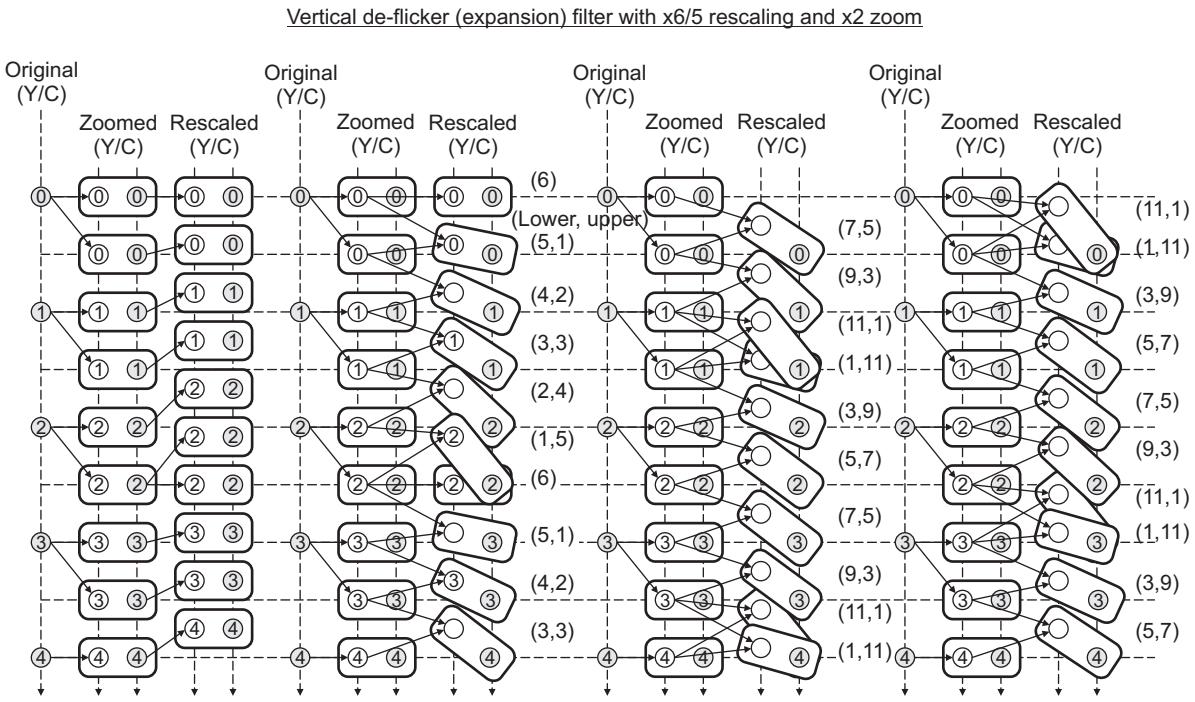
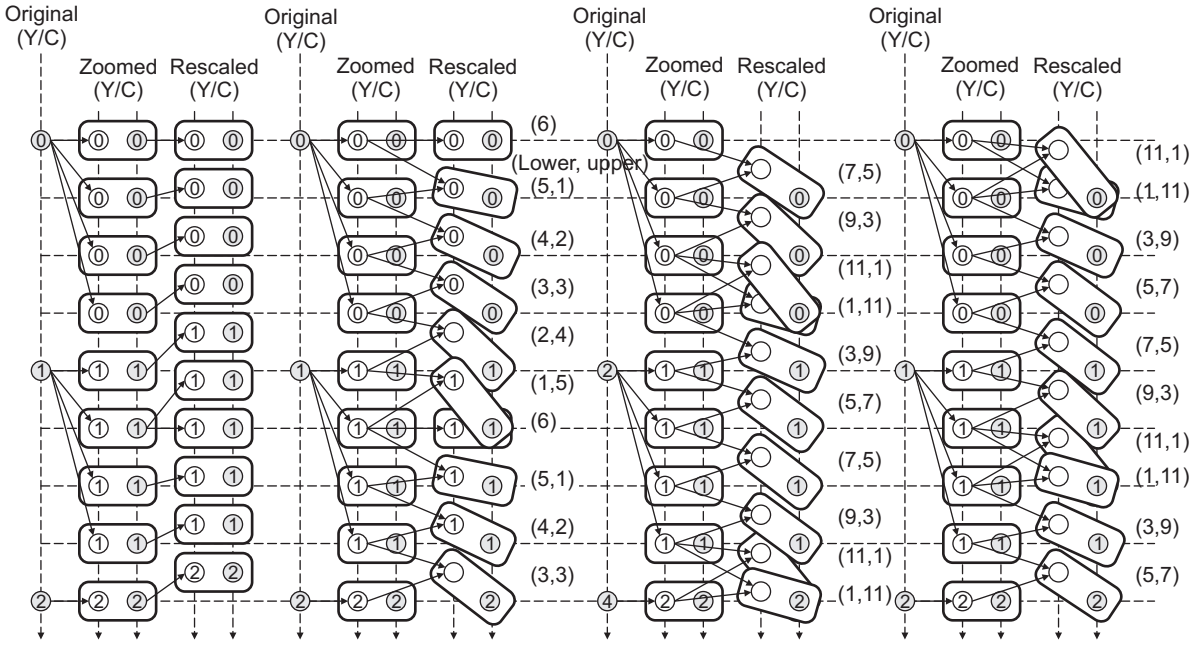


Figure 61. Filtering Method for Vertical x1.2 Expansion with 4x Zoom

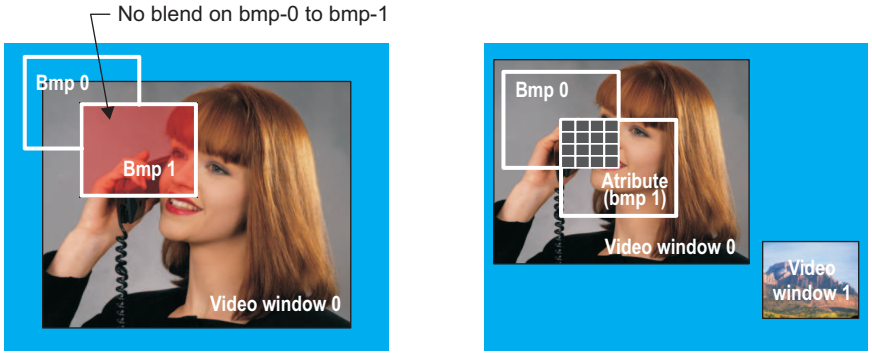


4.4.4 Bitmap Windows

The device supports two bitmap windows (OSDWIN0 and OSDWIN1) that can be displayed simultaneously. Data referenced by each bitmap window is read from external memory and displayed within the two windows.

Bitmap windows allow the user to display graphics and icons on the display unit. In typical usage, the source data is an index into a color lookup table (CLUT), either in ROM or RAM, to determine the actual display color for a given bitmap pixel value. A total of 256 CLUT entries, in 24-bit YUV color space, are available. The maximum width of a bitmap pixel is thus 8-bits. However, 1, 2, and 4-bit bitmap color depths are also supported.

Figure 62. Bitmap + Video Window Display Examples



Bitmap window 1 can be defined as an attribute window, whose data pixels modify the display attributes of the underlying Bitmap window 0.

In addition to displaying bitmap data, the OSD bitmap windows support displaying RGB data in either 16-bit RGB565 format; i.e., each R and B pixel is 5 bits and the G pixel is 6 bits or 24-bit format. The RGB data from external memory is converted into YCbCr data within the OSD module using the following equations to calculate YCrCb.

$Y = (0.2990 \times R) + (0.5870 \times G) + (0.1140 \times B)$

$Cb = (-0.1687 \times R) - (0.3313 \times G) + (0.5000 \times B) + 128$

$Cr = (0.5000 \times R) - (0.4187 \times G) - (0.0813 \times B) + 128$

The OSD bitmap windows can also display YUV422 data used by the video windows.

4.4.4.1 Color Look-Up Tables

There are three possible color look-up tables (CLUTs). Two of these are fixed-ROM CLUTs and one is a user-configurable RAM CLUT. Each of the windows uses either the RAM or ROM CLUT and you must select which of the two ROM CLUTs to use for all OSD options that use the ROM CLUT (MISCCTL.RSEL). Table 58 shows the registers used for the color look-up tables.

In addition to the bitmap windows, the overall OSD background color (the color displayed in areas where no windows are displayed) is set to a specific CLUT entry and the cursor color is selected from one of the CLUT tables/values.

The RAM CLUT must be initialized before it can be used. To set up the OSD RAM CLUT, the following steps are required:

1. Wait for the CPBSY bit of the MISCCTL register to be cleared to 0.
2. Write the luma and chroma Cb values into the CLUTRAMYCB register.
3. Write the chroma Cr value and the CLUT address into the CLUTRAMCR register. The address is the offset address into the CLUT RAM table for the Y, Cb and Cr values.
4. Repeat the previous steps until the RAM table is loaded completely.

Table 58. OSD Color Look-Up Table Registers

	Register.Field	Description
ROM color look-up table selection	MISCCTL.RSEL	Selects the ROM color look-p table to use for all options that select the ROM table (0=DM270, 1=DM320)
Background color selection	MODE.BCLUT	Background CLUT selection (ROM or RAM)
	MODE.CABG	Background CLUT selection (offset into 256-bit table)
Cursor CLUT selection	RECTCUR.CLUTSR	Cursor CLUT selection (ROM or RAM)
	RECTCUR.RCAD	Rectangular Cursor color address within CLUT (offset into 256-bit table)
Bitmap window CLUT selections	OSDWIN0MD.CLUTS0	Window 0 CLUT selection (ROM or RAM)
	OSDWIN1MD.CLUTS1	Window 1 CLUT selection (ROM or RAM)
RAM CLUT Setup/Write	CLUTRAMYCB.Y	CLUTRAM Y (luma) value
	CLUTRAMYCB.CB	CLUTRAM CB (chroma) value
	CLUTRAMCR.CR	CLUTRAM CR (chroma) value
	CLUTRAMCR.CADDR	CLUTRAM address offset (writes all values)
	MISCCTL.CPBUSY	Indicates if busy when writing to CLUT RAM

The RGB equivalent CLUT values are shown in Section 4.4.4.1.1 as converted with the inverse of the OSD's RGB-to-YUV conversion matrix for RGB888 and RGB565 window data shown below.

$R = (1.00000 \times Y) + (0.00000 \times (Cb - 128)) + (1.40200 \times (Cr - 128))$

$G = (1.00000 \times Y) - (0.34414 \times (Cb - 128)) - (0.71444 \times (Cr - 128))$

$B = (1.00000 \times Y) + (1.72200 \times (Cb - 128)) + (0.00000 \times (Cr - 128))$

Note: The default YUV-to-RGB conversion matrix values in the VENC module shown below are different and thus the output colors may not exactly match those shown here.

$R = (1.00000 \times Y) + (0.00000 \times (Cb - 128)) + (1.37110 \times (Cr - 128))$

$G = (1.00000 \times Y) - (0.33690 \times (Cb - 128)) - (0.69820 \times (Cr - 128))$

$B = (1.00000 \times Y) + (1.73240 \times (Cb - 128)) + (0.00000 \times (Cr - 128))$

The YUV output of each bitmap window can be attenuated to reduce the dynamic range of the YUV signals (see Table 59). Luma values are attenuated to a range between 16-235 and chroma values are attenuated to a range between 16-240.

Table 59. OSD Bitmap Window YUV Output Attenuation Registers

Register.Field	Description
EXTMODE.ATNOSD0EN	Enable YUV attenuation for Bitmap Window 0
EXTMODE.ATNOSD1EN	Enable YUV attenuation for Bitmap Window 1

4.4.4.1.1 ROM0 Color Look-Up Tables

Table 60. ROM0 Color Look-Up Table (YUV Values)

ndx	value	ndx	value	ndx	value	ndx	value	ndx	value	ndx	value	ndx	value	ndx	value
0	00 80 80	32	59 71 A2	64	72 1E F5	96	D2 08 95	128	63 46 46	160	3F 93 72	192	52 D3 4F	224	54 A7 76
1	26 5A DA	33	6E 6C AE	65	5B 6F 88	97	92 1F 93	129	17 71 71	161	26 93 72	193	8A 9B 71	225	AE 87 7F
2	4B 35 35	34	66 6C AE	66	18 68 89	98	B7 00 9F	130	4D 4B 4B	162	51 E4 37	194	48 9B 71	226	9D 88 7F
3	71 0F 8F	35	60 6A B4	67	49 4F 91	99	BD 00 A1	131	1B 6D 6D	163	58 EE 30	195	43 D1 55	227	6C 87 7F
4	0F F1 71	36	68 62 C5	68	41 4F 91	100	B5 00 A1	132	3B 55 55	164	EE 89 79	196	4A EB 46	228	64 87 7F
5	35 CB CB	37	40 40 FF	69	30 60 89	101	C4 00 A3	133	29 6F 67	165	DB 94 73	197	4A EB 46	229	53 87 7F
6	5A A6 26	38	53 5E C1	70	6E 1A 9E	102	D2 00 A5	134	8A 82 7A	166	D1 9E 6C	198	3B E1 4D	230	5B 88 7F
7	C0 80 80	39	2D 5B C6	71	50 59 8A	103	CA 10 94	135	48 82 7A	167	B9 9D 6C	199	BB 9B 72	231	4B 87 7F
8	D0 70 70	40	48 40 F5	72	48 59 8A	104	A8 32 64	136	2F 82 7A	168	A8 9E 6C	200	58 9B 72	232	43 87 7F
9	C4 AC 62	41	65 65 AF	73	77 32 95	105	AD 3E 67	137	27 82 7A	169	28 89 79	201	50 9B 72	233	6D 8E 7E
10	FB 80 80	42	4C 65 AF	74	6E 2A 96	106	A5 2D 5F	138	1E 83 7A	170	96 A7 65	202	37 9B 72	234	65 8E 7E
11	08 80 80	43	51 47 E4	75	5E 32 95	107	A6 34 5E	139	5F 8C 73	171	6E 9E 6C	203	47 AC 6A	235	22 87 7F
12	10 80 80	44	23 65 AF	76	27 59 8A	108	9A 30 59	140	8E C0 3C	172	86 A7 65	204	5E C7 5B	236	4D 96 7D
13	18 80 80	45	3B 4D D9	77	46 3A 94	109	8F 33 54	141	9B CC 2F	173	A5 B1 5F	205	E6 91 78	237	19 88 7F
14	21 80 80	46	43 45 EA	78	BE 04 A0	110	8C 2D 4E	142	BC A2 60	174	95 B1 5E	206	83 91 78	238	11 87 7F
15	29 80 80	47	1D 63 B5	79	35 4B 8D	111	84 2D 4E	143	81 DD 28	175	8C B1 5F	207	58 AC 6A	239	45 85 85
16	31 80 80	48	8B 68 AA	80	76 43 8E	112	88 29 4A	144	A8 B6 53	176	65 A7 65	208	59 A2 71	240	1C 85 85
17	4A 80 80	49	5A 4F D3	81	BE 1C 98	113	7D 24 45	145	98 B6 53	177	74 B1 5E	209	59 A2 71	241	74 87 90
18	5A 80 80	50	5D 3B F1	82	55 43 8E	114	72 50 60	146	78 D6 39	178	9A C4 51	210	51 A2 71	242	50 82 8A
19	73 80 80	51	18 68 AA	83	9C 0D 99	115	22 66 6E	147	74 E2 2D	179	62 EC 36	211	49 A2 70	243	58 82 8B
20	7B 80 80	52	45 53 C7	84	7C 1C 98	116	72 26 3F	148	62 EC 26	180	69 CC 50	212	41 A2 70	244	73 80 91
21	94 80 80	53	53 2D FF	85	B2 00 A4	117	6A 26 3F	149	C7 A0 66	181	7F AE 64	213	1F B3 69	245	00 80 80
22	A5 80 80	54	7F 5B B6	86	8A 06 9B	118	5E 5B 64	150	9C AA 5F	182	85 B8 5E	214	1F C4 61	246	FB 75 84
23	BD 80 80	55	2D 5B B6	87	AA 00 A4	119	9C 57 5F	151	5C EA 2C	183	74 B9 5E	215	B5 91 78	247	A0 84 80
24	44 7E 86	56	33 5D B0	88	B0 00 A6	120	73 2E 3E	152	AD A9 5F	184	5E AE 64	216	94 91 78	248	80 80 80
25	70 7B 8B	57	7B 4F C2	89	C4 06 9A	121	63 35 3E	153	AB B3 59	185	61 DC 48	217	7B 91 78	249	4C 34 FF
26	68 7B 8B	58	71 40 D5	90	B2 00 9C	122	2E 7B 7B	154	9B B3 58	186	B1 A5 6B	218	39 91 78	250	96 00 00
27	57 7B 8C	59	65 23 F9	91	BA 00 9C	123	31 67 67	155	A1 BD 52	187	A1 A5 6B	219	31 91 78	251	E2 00 9D
28	85 76 97	60	5F 21 FF	92	C1 00 9D	124	54 55 55	156	65 F1 2B	188	90 A5 6B	220	28 BB 68	252	1D FF 63
29	6D 76 97	61	2E 62 A4	93	B0 00 9E	125	78 41 41	157	C3 93 72	189	80 A5 6B	221	18 AA 70	253	69 FF FF
30	64 76 97	62	25 63 A5	94	98 00 9D	126	70 41 41	158	A2 93 72	190	46 A5 6B	222	63 98 77	254	B3 CC 00
31	5E 74 9D	63	6B 25 F3	95	3D 43 8D	127	4C 55 55	159	60 93 72	191	4C C0 5D	223	52 99 78	255	FF 80 80

Figure 63. ROM0 Color Look-Up Table (Equivalent RGB)

ndx	color	ndx	color	ndx	color	ndx	color	ndx	color	ndx	Color	ndx	color	ndx	color
0		224		64		96		128		160		192		224	
1		225		65		97		129		161		193		225	
2		226		66		98		130		162		194		226	
3		227		67		99		131		163		195		227	
4		228		68		100		132		164		196		228	
5		229		69		101		133		165		197		229	
6		230		70		102		134		166		198		230	
7		231		71		103		135		167		199		231	
8		232		72		104		136		168		200		232	
9		233		73		105		137		169		201		233	
10		234		74		106		138		170		202		234	
11		235		75		107		139		171		203		235	
12		236		76		108		140		172		204		236	
13		237		77		109		141		173		205		237	
14		238		78		110		142		174		206		238	
15		239		79		111		143		175		207		239	
16		240		80		112		144		176		208		240	
17		241		81		113		145		177		209		241	
18		242		82		114		146		178		210		242	
19		243		83		115		147		179		211		243	
20		244		84		116		148		180		212		244	
21		245		85		117		149		181		213		245	
22		246		86		118		150		182		214		246	
23		247		87		119		151		183		215		247	
24		248		88		120		152		184		216		248	
25		249		89		121		153		185		217		249	
26		250		90		122		154		186		218		250	
27		251		91		123		155		187		219		251	
28		252		92		124		156		188		220		252	
29		253		93		125		157		189		221		253	
30		254		94		126		158		190		222		254	
31		255		95		127		159		191		223		255	

4.4.4.1.2 ROM1 Color Look-Up Tables

Table 61. ROM1 Color Look-Up Table (YUV Values)

ndx	value	ndx	value	ndx	value	ndx	value	ndx	value	ndx	value	ndx	value	ndx	value
0	FF 80 80	32	5E A1 F3	64	61 66 CC	96	69 D5 A2	128	6C 9A 7C	160	6F 5E 55	192	77 CD 2B	224	05 7D 88
1	F9 66 84	33	58 88 F7	65	5B 4D D1	97	63 BB A7	129	66 80 80	161	69 45 59	193	71 B3 2F	225	8C 31 1C
2	F3 4D 88	34	52 6E FB	66	5A DD D1	98	5D A2 AB	130	60 66 84	162	68 D5 5A	194	6B 9A 34	226	82 37 23
3	EE 34 8C	35	4C 55 FF	67	54 C4 D5	99	57 88 AF	131	5A 4D 88	163	62 BC 5E	195	65 80 38	227	6E 42 32
4	E8 1A 91	36	F0 89 66	68	4E AA DA	100	51 6F B3	132	5A DD 89	164	5D A2 62	196	60 67 3C	228	64 48 39
5	E2 00 95	37	EA 6F 6B	69	49 91 DE	101	4C 55 B7	133	54 C4 8D	165	57 89 66	197	5A 4D 40	229	50 53 47
6	E1 91 95	38	E4 56 6F	70	43 77 E2	102	4B E6 B8	134	4E AA 91	166	51 6F 6B	198	59 DE 41	230	46 59 4E
7	DB 77 9A	39	DE 3C 73	71	3D 5E E6	103	45 CC BC	135	48 91 95	167	4B 56 6F	199	53 C4 45	231	32 64 5C
8	D5 5E 9E	40	D8 23 77	72	E1 91 4D	104	3F B3 C0	136	42 77 9A	168	4A E6 6F	200	4D AB 49	232	28 69 64
9	D0 44 A2	41	D3 09 7B	73	DB 78 51	105	39 99 C4	137	3C 5E 9E	169	44 CC 74	201	48 91 4D	233	14 75 72
10	CA 2B A6	42	D2 9A 7C	74	D5 5E 55	106	34 80 C8	138	3C EE 9E	170	3F B3 78	202	42 78 51	234	0A 7A 79
11	C4 11 AA	43	CC 80 80	75	CF 45 59	107	34 80 C8	139	36 D5 A2	171	39 9A 7C	203	3C 5E 55	235	1B F7 6D
12	C3 A2 AB	44	C6 66 84	76	C9 2B 5E	108	D1 9A 34	140	30 BB A7	172	33 80 80	204	3B EF 56	236	19 EE 6E
13	BD 88 AF	45	C0 4D 88	77	C3 12 62	109	CB 80 38	141	2A A2 AB	173	2D 66 84	205	35 D5 5A	237	15 DE 71
14	B7 6F B3	46	BB 34 8C	78	C3 A2 62	110	C6 67 3C	142	24 88 AF	174	2C F7 85	206	2F BC 5E	238	13 D5 72
15	B2 55 B7	47	B5 1A 91	79	BD 89 66	111	C0 4D 40	143	1E 6F B3	175	27 DD 89	207	2A A2 62	239	10 C4 75
16	AC 3C BB	48	B4 AA 91	80	B7 6F 6B	112	BA 34 44	144	C2 A2 1A	176	21 C4 8D	208	24 89 66	240	0E BC 76
17	A6 22 BF	49	AE 91 95	81	B1 56 6F	113	B4 1A 48	145	BC 89 1E	177	1B AA 91	209	1E 6F 6B	241	0A AA 79
18	A5 B3 C0	50	A8 77 9A	82	AB 3C 73	114	B3 AB 49	146	B6 6F 22	178	15 91 95	210	1D FF 6B	242	08 A2 7A
19	9F 99 C4	51	A2 5E 9E	83	A5 23 77	115	AE 91 4D	147	B1 56 26	179	0F 77 9A	211	17 E6 6F	243	04 91 7D
20	9A 80 C8	52	9D 44 A2	84	A5 B3 78	116	A8 78 51	148	AB 3C 2B	180	B3 AB 00	212	11 CC 74	244	02 88 7F
21	94 66 CC	53	97 2B A6	85	9F 9A 7C	117	A2 5E 55	149	A5 23 2F	181	AD 92 05	213	0C B3 78	245	EE 80 80
22	8E 4D D1	54	96 BB A7	86	99 80 80	118	9C 45 59	150	A4 B3 2F	182	A7 78 09	214	06 9A 7C	246	DD 80 80
23	88 33 D5	55	90 A2 AB	87	93 66 84	119	96 2B 5E	151	9E 9A 34	183	A1 5F 0D	215	47 58 F7	247	BB 80 80
24	87 C4 D5	56	8A 88 AF	88	8D 4D 88	120	95 BC 5E	152	98 80 38	184	9B 45 11	216	42 5B EE	248	AA 80 80
25	81 AA DA	57	84 6F B3	89	88 34 8C	121	90 A2 62	153	93 67 3C	185	96 2C 15	217	38 60 DE	249	88 80 80
26	7C 91 DE	58	7F 55 B7	90	87 C4 8D	122	8A 89 66	154	8D 4D 40	186	95 BC 16	218	33 63 D5	250	77 80 80
27	76 77 E2	59	79 3C BB	91	81 AA 91	123	84 6F 6B	155	87 34 44	187	8F A2 1A	219	29 69 C4	251	55 80 80
28	70 5E E6	60	78 CC BC	92	7B 91 95	124	7E 56 6F	156	87 34 44	188	89 89 1E	220	24 6C BC	252	44 80 80
29	6A 44 EA	61	72 B3 C0	93	75 77 9A	125	78 3C 73	157	80 AB 49	189	83 6F 22	221	19 72 AA	253	22 80 80
30	69 D4 EB	62	6C 99 C4	94	6F 5E 9E	126	77 CC 74	158	7B 91 4D	190	7E 56 26	222	14 75 A2	254	11 80 80
31	64 BB EF	63	67 80 C8	95	6F 5E 9E	127	72 B3 78	159	75 78 51	191	78 3C 2B	223	0A 7A 91	255	00 80 80

Table 62. ROM1 Color Look-Up Table (Equivalent RGB Values)

ndx	value	ndx	value	ndx	value	ndx	value	ndx	value	ndx	value	ndx	value	ndx	value
0	FF FF FF	32	FF 00 98	64	CB 33 32	96	98 33 FF	128	66 65 9A	160	32 99 32	192	00 99 FF	224	10 00 00
1	FE FF CA	33	FE 00 66	65	CC 32 00	97	99 32 CB	129	66 66 66	161	32 99 00	193	00 99 CB	225	00 EE 00
2	FE FE 98	34	FE 00 32	66	CB 00 FE	98	99 32 99	130	65 66 31	162	32 65 FE	194	00 98 99	226	00 DD 00
3	FE FF 67	35	FE 00 00	67	CB 00 CC	99	98 32 65	131	65 65 00	163	32 65 CC	195	00 98 65	227	00 BB 00
4	FF FE 33	36	CB FF FF	68	CC 00 98	100	98 32 32	132	66 33 FE	164	32 66 99	196	00 99 33	228	00 A9 00
5	FF FF 00	37	CC FE CB	69	CC 00 67	101	99 33 00	133	66 33 CC	165	32 66 66	197	00 99 00	229	00 88 00
6	FE CC FF	38	CC FE 99	70	CC 00 33	102	99 00 FF	134	65 33 98	166	33 65 32	198	00 65 FF	230	00 77 00
7	FF CB CB	39	CB FE 65	71	CC 00 00	103	99 00 CB	135	65 33 66	167	33 65 00	199	00 65 CB	231	00 55 00
8	FF CB 98	40	CB FE 33	72	99 FF FF	104	98 00 99	136	66 32 32	168	32 33 FE	200	00 65 99	232	00 43 00
9	FF CC 65	41	CB FF 00	73	99 FF CC	105	98 00 65	137	66 32 00	169	33 32 CA	201	00 66 66	233	00 21 00
10	FF CC 33	42	CC CB FF	74	98 FF 98	106	98 00 34	138	66 00 FE	170	33 33 99	202	00 66 33	234	00 11 00
11	FE CC 00	43	CC CC CC	75	98 FF 66	107	98 00 00	139	65 00 CC	171	33 32 67	203	00 66 00	235	00 00 ED
12	FF 98 FF	44	CB CC 97	76	99 FE 32	108	66 FE FF	140	66 00 98	172	33 33 33	204	00 32 FF	236	00 00 DB
13	FE 98 CB	45	CB CB 65	77	98 FE 00	109	66 FE CB	141	66 00 66	173	32 33 00	205	00 32 CB	237	00 00 BB
14	FE 98 98	46	CB CC 34	78	98 CC FF	110	66 FF 99	142	65 00 32	174	33 00 FE	206	00 32 99	238	00 00 A9
15	FF 99 65	47	CC CB 00	79	98 CC CC	111	66 FF 65	143	65 00 00	175	33 00 CB	207	00 33 66	239	00 00 88
16	FE 99 33	48	CB 99 FE	80	99 CB 98	112	65 FF 33	144	32 FF FE	176	33 00 99	208	00 33 33	240	00 00 78
17	FE 99 00	49	CB 99 CC	81	99 CB 66	113	65 FF 00	145	32 FE CB	177	32 00 65	209	00 32 00	241	00 00 54
18	FE 65 FF	50	CC 98 98	82	98 CB 32	114	65 CB FF	146	32 FE 97	178	32 00 33	210	00 00 FE	242	00 00 44
19	FE 65 CB	51	CC 98 65	83	98 CB 00	115	66 CC CC	147	32 FF 66	179	33 00 00	211	00 00 CB	243	00 00 22
20	FE 66 9A	52	CC 99 32	84	99 99 FF	116	66 CC 99	148	33 FF 32	180	00 FF FF	212	00 00 97	244	00 00 10
21	FE 66 65	53	CC 99 00	85	99 98 CD	117	65 CC 65	149	33 FE 00	181	00 FE CC	213	00 00 66	245	EE EE EE
22	FF 65 33	54	CC 65 FE	86	99 99 99	118	65 CC 33	150	32 CC FE	182	00 FE 98	214	00 00 34	246	DD DD DD
23	FF 65 00	55	CC 65 CC	87	98 99 64	119	66 CB 00	151	33 CB CC	183	00 FE 66	215	ED 00 00	247	BB BB BB
24	FE 32 FF	56	CB 65 98	88	98 98 32	120	65 98 FF	152	33 CB 98	184	00 FE 32	216	DC 00 00	248	AA AA AA
25	FF 32 CB	57	CB 65 65	89	98 99 01	121	65 99 CC	153	33 CC 66	185	00 FF 01	217	BB 00 00	249	88 88 88
26	FF 33 9A	58	CC 66 32	90	99 66 FF	122	65 99 99	154	33 CC 32	186	00 CC FF	218	AA 00 00	250	77 77 77
27	FF 33 66	59	CB 66 00	91	98 66 CB	123	66 98 65	155	32 CC 00	187	00 CC CB	219	88 00 00	251	55 55 55
28	FF 32 33	60	CC 32 FE	92	98 66 99	124	66 98 33	156	33 98 FE	188	00 CB 98	220	78 00 00	252	44 44 44
29	FE 32 00	61	CB 32 CC	93	99 65 65	125	65 98 00	157	32 98 CC	189	00 CB 64	221	53 00 00	253	22 22 22
30	FF 00 FD	62	CB 32 98	94	99 65 32	126	66 65 FD	158	33 99 99	190	00 CC 33	222	43 00 00	254	11 11 11
31	FF 00 CC	63	CB 33 67	95	99 66 00	127	66 66 CC	159	33 99 66	191	00 CC 00	223	21 00 00	255	00 00 00

Figure 64. ROM1 Color Look-Up Table (Equivalent RGB)

ndx	Color	ndx	color	ndx	color	ndx	color	ndx	color	ndx	color	ndx	color	ndx	color
0		32		64		96		128		160		192		224	
1		33		65		97		129		161		193		225	
2		34		66		98		130		162		194		226	
3		35		67		99		131		163		195		227	
4		36		68		100		132		164		196		228	
5		37		69		101		133		165		197		229	
6		38		70		102		134		166		198		230	
7		39		71		103		135		167		199		231	
8		40		72		104		136		168		200		232	
9		41		73		105		137		169		201		233	
10		42		74		106		138		170		202		234	
11		43		75		107		139		171		203		235	
12		44		76		108		140		172		204		236	
13		45		77		109		141		173		205		237	
14		46		78		110		142		174		206		238	
15		47		79		111		143		175		207		239	
16		48		80		112		144		176		208		240	
17		49		81		113		145		177		209		241	
18		50		82		114		146		178		210		242	
19		51		83		115		147		179		211		243	
20		52		84		116		148		180		212		244	
21		53		85		117		149		181		213		245	
22		54		86		118		150		182		214		246	
23		55		87		119		151		183		215		247	
24		56		88		120		152		184		216		248	
25		57		89		121		153		185		217		249	
26		58		90		122		154		186		218		250	
27		59		91		123		155		187		219		251	
28		60		92		124		156		188		220		252	
29		61		93		125		157		189		221		253	
30		62		94		126		158		190		222		254	
31		63		95		127		159		191		223		255	

4.4.4.2 Bitmap Indexing Into Color Look-Up Tables

When the bitmap color depth is 8 bits (OSDWIN0MD.BMW0, OSDWIN1MD.BMW1), each 8-bit pixel value in SDRAM is a direct index into the color lookup table (CLUT). However, when the bitmap color depth is 1, 2, or 4 bits, the W*n*BMP01-W*n*BMPEF registers must be used to map the pixel values into the CLUT. Any of the 256 colors in the table can be used. For example, given 1-bit bitmap data, any of the 256 colors in the CLUT can be mapped to bit value 0 and any of the 256 colors can be mapped to bit value 1. This mapping is specified separately for each OSD bitmap window. Table 63 shows the registers which can be used to select the color for a bitmap value.

Table 63. CLUT Mapping for 1-Bit, 2-Bit, or 4-Bit Bitmaps

Register.Field (n = 0 or 1 for OSD Bitmap Window 0 or 1, respectively)	Color Corresponding to Bitmap Value		
	4-Bit Bitmap	2-Bit Bitmap	1-Bit Bitmap
WnBMP01.PAL00	0	0	0
WnBMP01.PAL01	1	-	-
WnBMP23.PAL02	2	-	-
WnBMP23.PAL03	3	-	-
WnBMP45.PAL04	4	-	-
WnBMP45.PAL05	5	1	-
WnBMP67.PAL06	6	-	-
WnBMP67.PAL07	7	-	-
WnBMP89.PAL08	8	-	-
WnBMP89.PAL09	9	-	-
WnBMPAB.PAL10	10	2	-
WnBMPAB.PAL11	11	-	-
WnBMPCD.PAL12	12	-	-
WnBMPCD.PAL13	13	-	-
WnBMPEF.PAL14	14	-	-
WnBMPEF.PAL15	15	3	1

4.4.4.3 Bitmap Window Blending and Transparency

The OSD also supports pixel blending for the bitmap windows only. If blending is enabled, the amount of blending (relative amount of video data versus bitmap data) at each pixel is determined by the blending factor.

The OSD also supports transparency blending mode. If transparency is enabled, any pixel on the bitmap display that has a value equal to that of the transparent value for that window as defined in TRANSPBMPIDX.BMPn will be transparent (only partially transparent) and allow the underlying video pixel to be displayed based on the blending factor.

Blend factor through mode is also supported (only for RGB mode). In this mode the blending factor for the OSD window is set to 1. Blending factor and transparency are configured using OSDWIN0MD and OSDWIN1MD registers for OSD bitmap window 0 and 1 respectively. Blend factor through mode is configured by setting bit BBF_TH of MISCCTL register to 1.

Table 64. Bitmap Transparency and Blending Settings

Transparency OSDWINnMD.TEn	Blending Factor OSDWINnMD.BLNDn	OSD Window Contribution	Video Contribution
OFF	0	0	1
	1	1/8	7/8
	2	2/8	6/8
	3	3/8	5/8
	4	4/8	4/8
	5	5/8	3/8
	6	6/8	2/8
	7	1	0
ON		If pixel value is equal to TRANSBMPIDX.BMPn:	
	0	0	1
	1	1/8	7/8
	2	2/8	6/8
	3	3/8	5/8
	4	4/8	4/8
	5	5/8	3/8
	6	6/8	2/8
	7	1	0
		If pixel value is not equal to TRANSBMPIDX.BMPn:	
	X	1	0

4.4.4.4 Attenuation in Bitmap Window (RGB Mode Only)

The OSD module has an attenuation function for use when displaying RGB data in a bitmap window. Because RGB data is displayed by converting to YC format, the converted result values may not fall into appropriate ranges for digital video. This function is useful if the video output module does not have any attenuation function (this is regulated by CCIR Rec.601 and Rec.656).

Luminance data is scaled down to 16~235 and chrominance data is scaled down to 16~240 using linear interpolation. This function is performed after conversion from RGB to YC format.

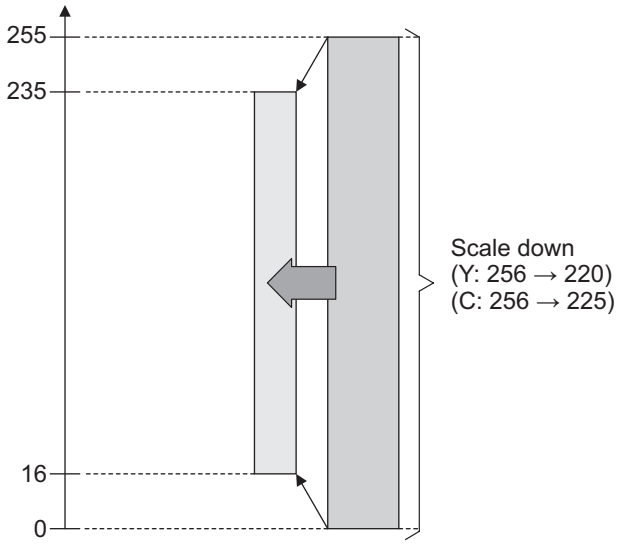
Table 65. Expansion and Anti-Flicker Filters for Video Window Registers

Register.Field	Description
EXTMODE.ATNOSD0EN	Bitmap Window 0 RGB attenuation enable
EXTMODE.ATNOSD1EN	Bitmap Window 1 RGB attenuation enable

This conversion is not performed unless the data source is RGB, even if it is enabled.

NOTE: For Digital RGB output, the matrix values converting from YC to RGB in the video encoder are set for the Rec.601 attenuation at the default setting.

Figure 65. Concept of Attenuation for RGB Bitmap Data



4.4.4.5 Bitmap Window Data Formats

The bitmap data formats are shown in Figure 66. Bitmap data is interpreted in bytes, with the pixels read in order from the most significant portion of the byte. Note that since each horizontal line of window data must be a multiple of 32-bytes:

- 8-bit bitmap windows must contain a multiple of 32 bytes/1 bytes/pixel = 32 pixels per horizontal line.
- 4-bit bitmap windows must contain a multiple of 32 bytes/1/2 bytes/pixel = 64 pixels per horizontal line.
- 2-bit bitmap windows must contain a multiple of 32 bytes/1/4 bytes/pixel = 128 pixels per horizontal line.
- 1-bit bitmap windows must contain a multiple of 32 bytes/1/8 bytes/pixel = 256 pixels per horizontal line.

Figure 66. Bitmap Data Formats

8−bits per pixel within 32−bit word

31 28	27 24	23 20	19 16	15 12	11 8	7 4	3 0
P3		P2		P1		P0	

8−bits per pixel SDRAM format

Addr	31 24	23 16	15 8	7 0
N	P3	P2	P1	P0
N+1	P7	P6	P5	P4
N+2	P11	P10	P9	P8

4−bits per pixel within 32−bit word

31 28	27 24	23 20	19 16	15 12	11 8	7 4	3 0
P6	P7	P4	P5	P2	P3	P0	P1

4−bits per pixel SDRAM format

Addr	31 28	27 24	23 20	19 16	15 12	11 8	7 4	3 0
N	P6	P7	P4	P5	P2	P3	P0	P1
N+1	P14	P15	P12	P13	P10	P11	P8	P9
N+2	P22	P23	P20	P21	P18	P19	P16	P17

2−bits per pixel within 32−bit word

31 30	29 28	27 26	25 24	23 22	21 20	19 18	17 16	15 14	13 12	11 10	9 8	7 6	5 4	3 2	1 0
P12	P13	P14	P15	P8	P9	P10	P11	P4	P5	P6	P7	P0	P1	P2	P3

2−bits per pixel SDRAM format

Addr	31 30	29 28	27 26	25 24	23 22	21 20	19 18	17 16	15 14	13 12	11 10	9 8	7 6	5 4	3 2	1 0
N	P12	P13	P14	P15	P8	P9	P10	P11	P4	P5	P6	P7	P0	P1	P2	P3
N+1	P28	P29	P30	P31	P24	P25	P26	P27	P20	P21	P22	P23	P16	P17	P18	P19
N+2	P44	P45	P46	P47	P40	P41	P42	P43	P36	P37	P38	P39	P32	P33	P34	P35

1−bit per pixel within 32−bit word

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P24	P25	P26	P27	P28	P29	P30	P31	P16	P17	P18	P19	P20	P21	P22	P23	P8	P9	P10	P11	P12	P13	P14	P15	P0	P1	P2	P3	P4	P5	P6	P7

1−bit per pixel SDRAM format

Addr	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
N	P24	P25	P26	P27	P28	P29	P30	P31	P16	P17	P18	P19	P20	P21	P22	P23	P8	P9	P10	P11	P12	P13	P14	P15	P0	P1	P2	P3	P4	P5	P6	P7
N+1	P56	P57	P58	P59	P60	P61	P62	P63	P48	P49	P50	P51	P52	P53	P54	P55	P40	P41	P42	P43	P44	P45	P46	P47	P32	P33	P34	P35	P36	P37	P38	P39
N+2	P88	P89	P90	P91	P92	P93	P94	P95	P80	P81	P82	P83	P84	P85	P86	P87	P72	P73	P74	P75	P76	P77	P78	P79	P64	P65	P66	P67	P68	P69	P70	P71

4.4.4.6 Bitmap Window Data — RGB Formats

OSD bitmap windows also support the display of 16-bit and 24-bit RGB source data. This data in internally converted to YUV422 prior to entering the OSD module for blending. The RGB data from external memory is converted into YCbCr data within the OSD module using the following equations to calculate YCrCb.

Y = 0.2990*R + 0.5870*G + 0.1140*B

Cb = -0.1687*R - 0.3313*G + 0.5000*B + 128

Cr = 0.5000*R - 0.4187*G - 0.0813*B + 128

While there is no restriction on bitmap data formats (both bitmap windows can be RGB16 or RGB25 or one of each), only one transparency color key setting is provided.

Table 66. RGB Control Registers

Control Register	Window
OSDWIN0MD.BMP0MD	Defines data source format for Bitmap Window 0
OSDWIN1MD.BMP1MD	Defines data source format for Bitmap Window 1
TRANSPVALL.RGBL	Transparency value (RGB565) for RGB565 data, or lower 16-bit of transparency value (GB) for RGB888.
TRANSPVALU.RGBU	Transparency value upper byte (R) for RGB888.

The 16-bit RGB565 data is stored in DDR2/mDDR in 16-bit words. Within each 16-bit element, the red value is least significant, followed by the green, then blue, as shown in Figure 68.

The DDR format for RGB565 data is shown below.

Figure 67. Data Format - RGB565

(a) RGB565 pixels within 32-bit word

31 27	26 21	20 16	15 11	10 5	4 0
R1	G1	B1	R0	G0	B0

(b) RGB565 SDRAM format

Address	31 27	26 21	20 16	15 11	10 5	4 0
N	R1	G1	B1	R0	G0	B0
N + 1	R3	G3	B3	R2	G2	B2
N + 2	R5	G5	B5	R4	G4	B4
...	...					

Note that since each horizontal line of window data must be a multiple of 32-bytes, the RGB565 windows must contain a multiple of 32-bytes / 2 byte/pixel = 16 pixels per horizontal line.

The 24-bit RGB888 data is stored in DDR2/mDDR in 32-bit words. Within each 24-bit element, the red value in the least significant byte, followed by the green, then the blue byte, as shown in Figure 68. The three lower bits of the MSByte are interpreted as pixel-level blending bits.

Figure 68. Bitmap Data Format - RGB888

(a) RGB565 pixels within 32-bit word

31 27	26 24	23 16	15 8	7 0
n/a	Blend0	RO	G0	R0

(b) SDRAM format

Address	31 27	26 24	23 16	15 8	7 0
N	n/a	Blend0	R0	G0	B0
N + 1	n/a	Blend1	R1	G1	B1
N + 2	n/a	Blend2	R2	G2	B2

4.4.4.7 OSD Bitmap Window —YUV422 Format

The OSD windows can also display YUV422 data. See the Video Window descriptions for the data formats.

4.4.4.8 OSD Attribute Window

OSD bitmap window 1 can be configured as an attribute window (OSDWIN1MD.OASW and OSDATRMD.OASW) instead of a bitmap window, see Figure 69. In this mode, the attribute window allows blending and blinking on a pixel-by-pixel basis in bitmap window 0. In particular, the attribute window provides a means to:

- Set the blending level (3 bits, 8 levels) of individual pixels in OSD window 0
- Set individual pixels in OSD window 0 to blink, if blinking is enabled

Figure 69. OSD Attribute Window

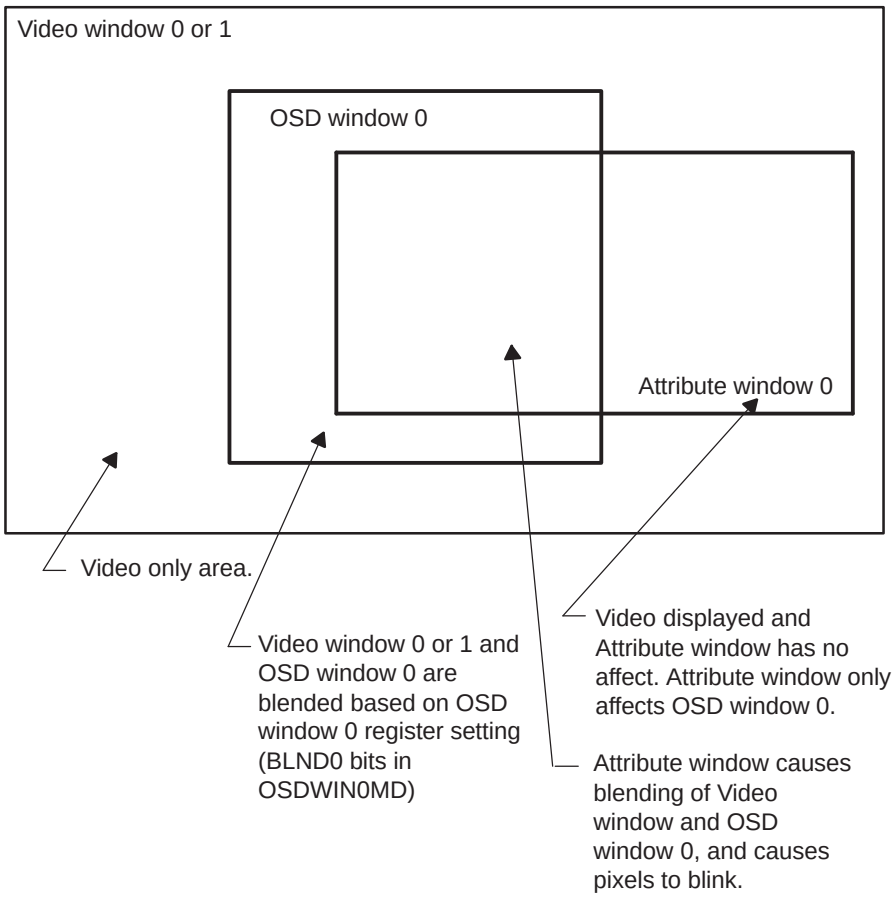


Table 67. OSD Blink Attribute Control Registers

Control Register.Field	Description
OSDATRMD.BLNK	Enable blinking defined by attribute window
OSDATRMD.BLNKINT	Set the blink interval

The SDRAM data format follows that for 4-bit bitmap windows (see Figure 66). Note that since each horizontal line of window data must be a multiple of 32 bytes, the attribute windows must contain a multiple of 32 bytes/ 1/2 byte/pixel = 64 pixels per horizontal line.

4.4.5 OSD - Cursor Window

The rectangular hardware cursor always appears on top of all other OSD windows. The cursor size, color, horizontal and vertical thickness can be specified (see Table 68). This cursor can also be configured to use the ROM or RAM CLUT.

Figure 70 shows an example usage of the rectangle cursor. The outline shows the rectangle cursor and the ICON 1-4 windows are displayed by using OSD window 0 or 1.

Table 68. OSD Cursor Window Control Registers

Control Register	Description
RECTCUR.RCAD	Cursor color address (offset into CLUT)
RECTCUR.CLUTSR	Cursor CLUT selection (RAM or ROM)
RECTCUR.RCHW	Rectangular Cursor Horizontal Width
RECTCUR.RCVW	Rectangular Cursor Vertical Width

Figure 70. Cursor Window Example

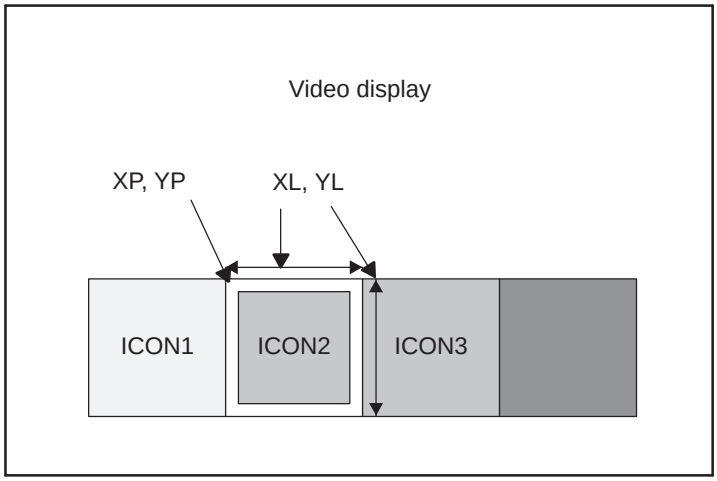
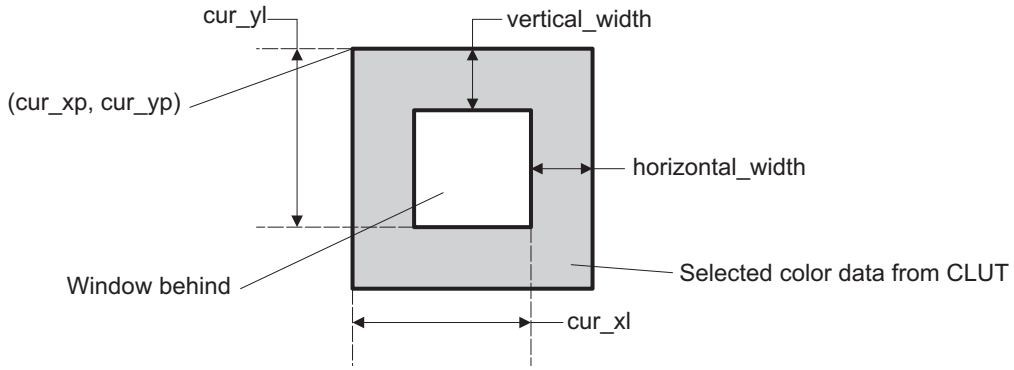


Figure 71. Cursor Window Configuration



4.5 Video Encoder Module

The video encoder (VENC) module consists of two main sub-modules, and an analog NTSC/PAL/HDTV video encoder with integrated 3-channel HD video DAC with 1-channel SD video buffer and a digital LCD/video controller.

4.5.1 Video Timing Mode

The VENC module supports two timing modes: standard NTSC/PAL/HDTV and non-standard mode (user-defined).

4.5.1.1 Standard Mode

In this mode, the timing generator operates in the standard format. The support formats are 525/60 Hz (NTSC-M) or 625/50 Hz (PAL-B/D/G/H/I) for SDTV and 525p/625p/720p/1080i for HDTV. The digital output from the LCD interface is also available simultaneously. Note, however, this is limited to LCDs that support NTSC/PAL/HDTV timing and the output will mirror the analog output display.

4.5.1.2 Nonstandard Mode

This mode is provided to configure the user-defined generic timing. The VENC module operates at any given timing defined by the module's register settings. In this mode, the video encoder sub-module of VENC is automatically disabled. To select non-standard mode, set VMOD.VMD to 1.

4.5.2 Synchronous Mode

The VENC module supports two synchronous modes: master and slave. Each mode can be used in either of the two video timing modes (standard NTSC/PAL/HDTV and non-standard).

4.5.2.1 Master Mode

This mode operates in synchronization with horizontal/vertical sync signals generated by the timing generator in the VENC module.

4.5.2.2 Slave Mode

This mode operates in synchronization with sync signals input from an external source. To configure the video encoder as a slave device, set VMOD.SLAVE to 1.

1. When SYNCCTL.EXSYNC is cleared to 0, the external inputs from the HSYNC/VSYNC/LCD_FIELD pins are used as the external sync signals. It is also required to set VIOCTL.SYDIR to 1 to configure the HSYNC/VSYNC/LCD_FIELD pins as input.
2. When SYNCCTL.EXSYNC is set to 1, the sync signals from the CCD controller (see the device VPFE Programmer's Guide) are used as external sync signals. This provides synchronization between the CCD timing and video timing. It is possible to invert the timing signals by setting the EXHIV, EXVIV, and EXFIV fields in the SYNCCTL register.

4.5.3 Analog NTSC/PAL Video Encoder

The NTSC/PAL encoder (Figure 72) takes video data from the OSD module and generates the necessary signaling and formatting to display the video/image data onto an NTSC/PAL display. The TVTYP field of the VMOD register (see Table 69) specifies the video formats.

Table 69. Supported TV Formats

VMD	TVTYP	ITLC	ITLCL	NSIT	Video Format
0	0	0	-	-	NTSC
0	0	1	0	-	Non-interlace 262 line/field
0	0	1	1	-	Non-interlace 263 line/field

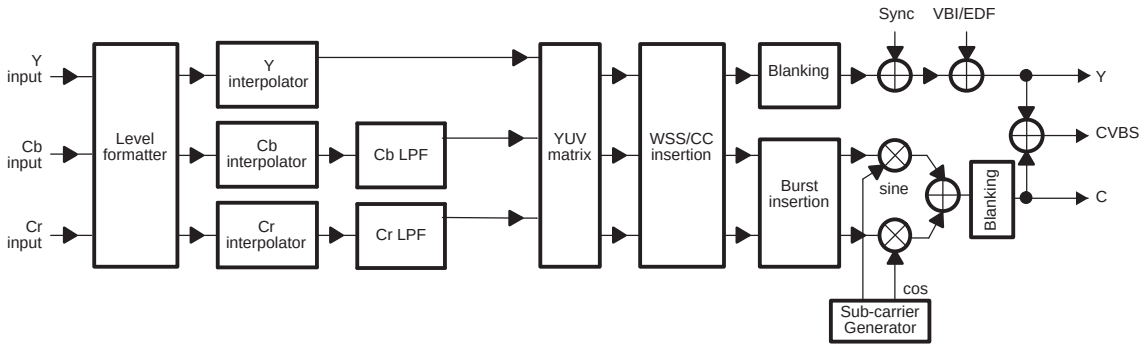
Table 69. Supported TV Formats (continued)

VMD	TVTYP	ITLC	ITLCL	NSIT	Video Format
0	1	0	-	-	PAL
0	1	1	0	-	Non-interlace 312 line/field
0	1	1	1	-	Non-interlace 313 line/field
1	-	-	-	0	Progressive
1	-	0	-	1	Interlace
1	-	1	-	1	Interlace (FIELD low fix)

Other composite DAC/timing settings are made via fields in the CVBS and ETMG0/1 registers.

The BLNK field in the VMOD register is the blanking enable. When this field is set to 1, the CVBS and/or component output is blanked without regard to the input video signals.

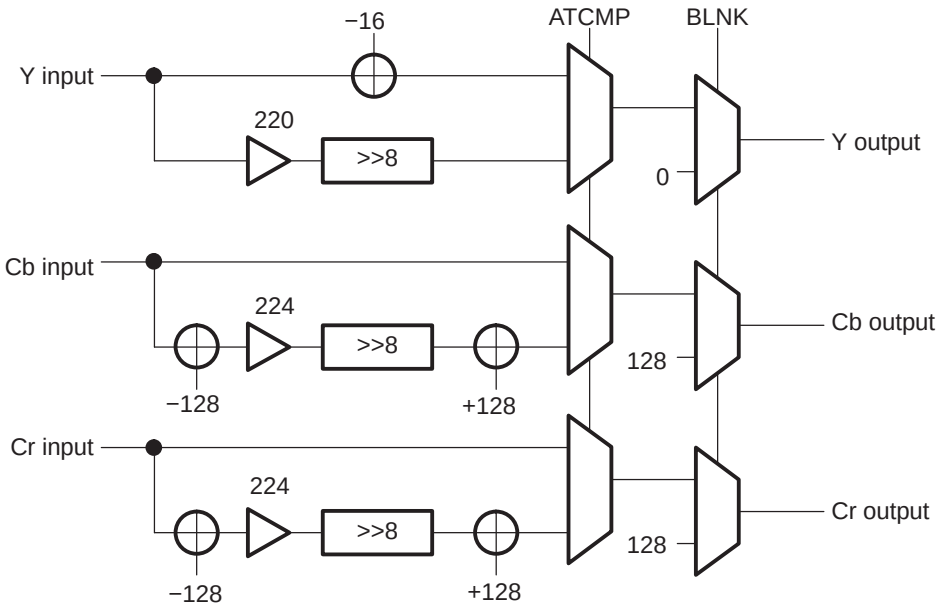
Figure 72. NTSC/PAL Video Encoder Block Diagram



4.5.3.1 Level Formatter

The front-end of the video encoder receives the YCbCr pixel data from the OSD module and converts it into the digital YCbCr, YUV, and RGB representations. The level formatter has the role to compress the signal level with 0-255 into the ITU-R BT.601 specified level (Y:16-235, C:16-240). The user can choose whether or not to apply the attenuation independently for each data path using the ATCOM, ATYCC, and the ATRGB fields in the VDPRO register. Figure 73 shows the block diagram for the level formatter.

Figure 73. Level Formatter Block Diagram



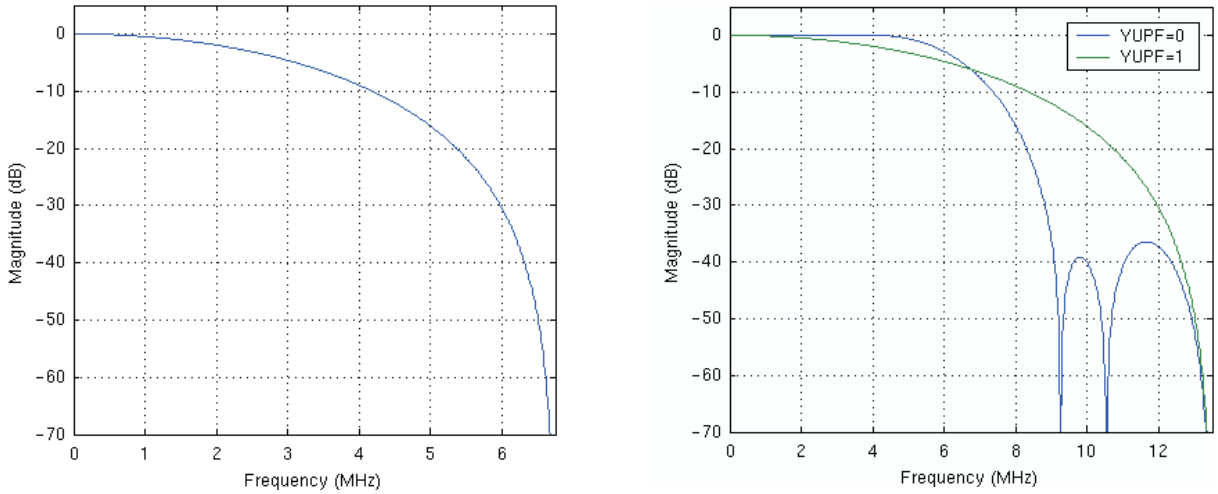
4.5.3.2 Luma Signal Processing

The luma signal from the level formatter can be processed by a 2× interpolation with a filter. The interpolation filter has 11 taps with a transfer function of:

$[3 - 10z^{-2} + 39z^{-4} + 64z^{-5} + 39z^{-6} - 10z^{-8} + 3z^{-10}]/64$

The interpolation is disabled by default and can be enabled by setting VDPRO.YUPS = 1. When in progressive mode, the interpolation should be disabled since the pixel rate is already 27 MHZ. The frequency response of the luma interpolation filter is shown in Figure 74. A low-pass filter follows the interpolation filter. The LPF is provided only for compatibility with previous devices for test purposes. It is disabled by default and is not supported.

Figure 74. Luma LPF (left) and Luma Interpolation Filter (right)



4.5.3.3 Chroma Signal Processing

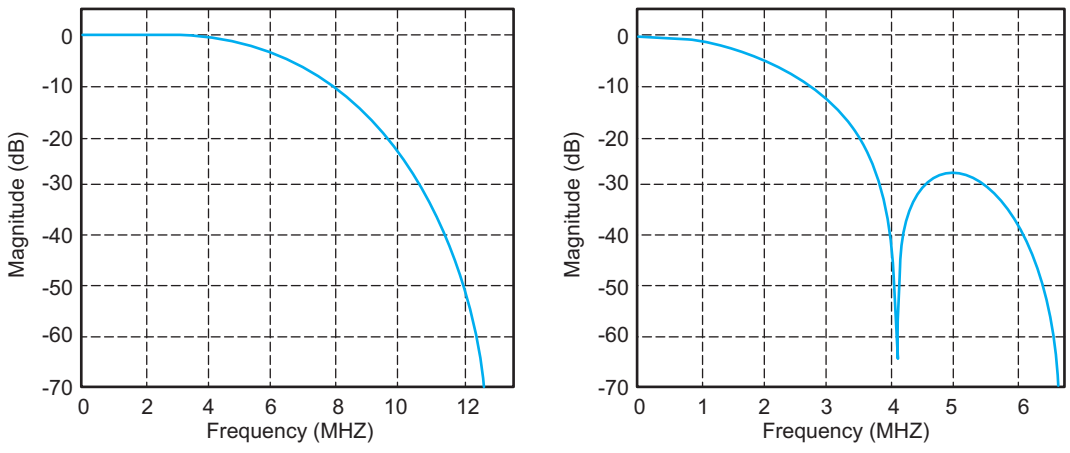
The chroma signal from the level formatter can also be processed by a 2× interpolation with a filter. Two cut-off frequencies, 1.5 MHz or 3.0 MHz can be selected by CVBS.CRCUT. The transfer functions are:

$[3 + 8z^{-1} + 10z^{-2} + 8z^{-3} + 3z^{-4}]/32$ for CRCUT=0 and

$(-1+8z^{-1}+18z^{-2}+8z^{-3}-1z^{-4})/32$ for CRCUT=1

The interpolation is disabled by default and can be enabled by setting VDPRO.CUPS = 1. The sampling rate of the LPF is 1/2 VENC clock (13.5 MHz). There are two outputs of this LPF block, composite and component. Low-pass filtering is only processed for composite output. No filtering is applied to the component output. The frequency response of the chroma interpolation filter is shown in Figure 75.

Figure 75. Chroma Interpolation Filter (left) and Chroma LPF (right)



4.5.3.4 CVBS Output

4.5.3.4.1 YUV Conversion

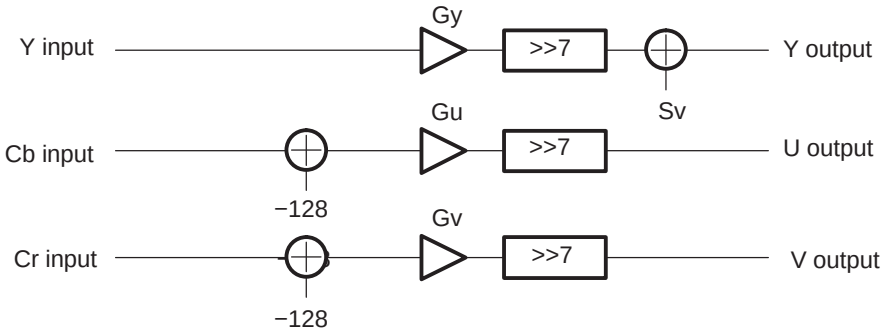
The interpolated and low pass filter YCbCr data are applied the proper gain and are then converted to YUV signals for CVBS generation. Table 70 shows the gain applied for each mode.

Table 70. Gains Used in YUV Conversion

CVBS.CVLVL	CVBS.CSTUP	Gy	Gu	Gv	Sv
0	0	305	315	444	0
	1	282	291	411	39
1	0	299	309	435	0
	1	277	285	403	38

The processing is done by subtracting 128 for the chroma (not for the luminance), then multiplying the gain and shifting right by 7. Figure 76 shows the block diagram for YCbCr to YUV conversion. When the CVBS.CSTUP = 1, then 7.5% setup is added for the output. The setting CSTUP is effective for both NTSC or PAL. However, note that for PAL mode, setting CSTUP = 1 causes an illegal output level.

Figure 76. YUV Conversion Block Diagram



4.5.3.4.2 CVBS Output Generation

The scaled luma then has the WSS and closed caption signals inserted and then is applied to the video edge controller. The video edge controller clips the video level of a few pixels around the horizontal blanking edge so that the output video has the proper blanking transition. This feature is enabled by default and can be disabled by CVBS.CBLS. Please refer to Section 2.1.2.2 for details of blanking edge shaping. Horizontal blanking start/end position can be adjusted by the CFPW and CLBI fields in the ETMG1 register. Following the edge shaping, the sync pulse are inserted. The horizontal sync pulse duration can be adjusted by the CEPW and CFSW fields in the ETMG0 register.

The scaled chroma signals (U and V) are modulated onto the sub-carrier following color burst insertion. The SC-H (sub-carrier to horizontal) phase can be controlled by the user. The SCSD field in the SCPROG register automatically updates the sub-carrier phases. The update occurs at line 9 in the color field 1 for both NTSC and PAL. By default, the values shown in Table 71 are applied. These values are chosen so that the SC-H phase is close to 0.

Table 71. Sub-Carrier Initial Phase Default Value

Mode	Preset Value
NTSC	378
PAL	356

Color burst insertion horizontal position can be controlled by the CBST and CBSE fields in the ETMG1 register. The modulated chroma signal is also applied to blanking edge shaping. Chroma blanking shaping can also be disabled by CBLS and blanking horizontal position is also adjusted by CFPW and CLBI.

The resulting Y and C are mixed together to get composite video output. Separated Y and C are also available for S-Video output. The offset 512 is added to the separated C to have the blanking level at the center of the DAC range. You can also control the blanking build-up time (Table 72) and the sync build-up time (Table 73).

Table 72. CVBS Blanking Build-Up Time

CVBS.CBBLD	Time
0	140 ns
1	300 ns

Table 73. CVBS Sync Build-Up Time

CVBS.CSBLD	Time
0	140 ns
1	200 ns

4.5.3.5 DAC Output

4.5.3.5.1 DAC Output Level

The video encoder has a 10-bit digital output to the DAC input. It is designed so that the full-scale digital output (7FFh = 1023) is expected to be converted to 1400 mV. In consideration of this, the user needs to take care of the DAC termination. It is convenient to utilize DAC DC output mode described in Section 4.5.3.5.3 to adjust the video output level.

The DAC output mode can be optionally amplified so that it can do full-swing (0-1023). GAMCTL.DAFUL register bit field enables this mode for each DAC independently. Gain and offset can be programmed by DACAMP.DAGA bit field and DACAMP.DAOF bit field respectively. The conversion can be represented by the following equation.

DAC_output_code = floor (DAGA/512 * (DAC_original_code) + 0.5) – DAOF

The gain and offset should be chosen so that the entire DAC output code does the full-swing between 0 and 1023.

DAGA = floor(1023/Peak-Sync)*512 + 0.5)

DAOF = floor(DAGA/512 * Sync + 0.5)

Table 74 shows the peak and sync value for each mode and the corresponding setting of DAGA and DAOF.

Table 74. Example of DAGA and DAOF

CYLVL	CSTUP	Peak	Sync	DAGA	DAOF
0	0	953	47	578	53
	1	940	47	587	54
1	0	940	37	580	42
	1	927	37	589	43

4.5.3.5.2 DAC Output Disable/Power Down

Setting VMOD.VIE to ‘0’ will force the analog output of the three DACs to a low voltage level regardless of the video signal. DAC power down can be enabled by DACTST.DAPD0-2 register bit fields. 3 DACs can be power down independently. By default, these registers are set to 1, so user must set them to 0 before using analog output

4.5.3.5.3 DAC DC Output Mode

The DACs support outputting a DC output instead of an analog output from the DAC pins. Setting the DADC bit in DACTST to 1 switches DAC digital input from normal video signal to the digital signal level, as specified in DACTST.DALVL.

4.5.3.5.4 DAC Output Configuration

Output video signal assignments to three DACs can be configurable by corresponding DA0S-DA2S registers (DACSEL). For component output, setting CMPNT.MRGB bit replaces YPbPr component output by RGB output. Table 75 shows the configuration of DAC output selection.

Table 75. DAC Output Select

DAxS	MRGB	DAC Output
0	-	CVBS
1	-	S-Video Y
2	-	S-video C
3	0	Y
	1	G

Table 75. DAC Output Select (continued)

DAxS	MRGB	DAC Output
4	0	Pb
	1	B
5	0	PR
	1	R
6-15	-	Reserved

4.5.3.5.5 DAC Output Inverse

Setting DACINV register allows you to invert the DAC output mode.

4.5.3.5.6 Y/C Delay

Y signal delay can be adjusted by register setting. Different delays can be applied to CVBS and component. The CVBS.CYDLY can adjust the Y delay for CVBS output, while CMPNT.MYDLY take effects on the component Y delay. The adjustable range is from -4 to 3 ENC clock for each.

4.5.3.5.7 Video Attribute Insertion

The video encoder has the capability to insert video information into the vertical blanking period. For example, the video encoder can insert a video attribute which indicates the proper aspect ratio to the video receiver. For NTSC mode, the video encoder can insert 14-bit video information on line 20 and line 283 to conform to the EIAJ CPR-1024 Video Aspect Ratio ID specification. Attribute information should be set using the ATR1 and ATR0 registers. The ATR2 register should be set with the 6-bit CRC data that is calculated by the following equation:

$G(x) = x^6 + x + 1$, where x^6 and x are preset to 1.

Bit 7 of ATR2 enables attribute insertion.

For PAL mode, the video encoder can insert 14-bit video information (WSS) on line 23 of every frame to conform to the ITU-R BT.1119-2 (ETSI EN 300 294) Wide Screen Signaling specification. Attribute information should be set in ATR1 register and ATR2 bits 5-0. Bit 7 of ATR2 enables attribute insertion.

In NTSC and PAL encoding modes, data in the ATR1 and ATR0 registers are transferred to internal circuitry when ATR2 is set. For this reason, ATR2 should be set last.

The video encoder also supports video ID insertion for progressive. EIAJ CPR-1204-1 for 525p and IEC 62375 for 625p and EIAJ CPR-1204-2 for 720p/1080i. Usage of ATR0-ATR2 registers is same as in SDTV (NTSC for 525p, PAL for 625p).

CEA-805 A standard defines two packet type. Type A and Type B. Type A packet format is same as the one defined in EIAJ standards. Type B packet is supported in DM36x VENC. BATR0-8 registers are used to transmit Type B packet.

4.5.3.5.8 Closed-Captioning

The video encoder supports closed-caption encoding. Closed-caption data is transmitted on line 21 of the odd field and line 284 of the even field in NTSC. It is possible to specify the fields on which closed-captioning is enabled by CAPCTL.CAPF.

The data should be written to the CAPDO or CAPDE registers for odd or even fields, respectively. It is required to load the data at least 1 line early. When data is written to CAPDO/CAPDE, VSTAT.CAOST/VSTAT.CAEST) is changed to 1. This bit is automatically cleared to 0 when caption data transmission is completed on line 21 in the odd field or line 284 in the even field.

When the caption data register (CAPDO or CAPDE) is not updated before the caption data transmission timing for the corresponding field, the ASCII code specified by CAPCTL.CADF is automatically transmitted for closed caption data.

The width of every data register is 7 bits and the parity bit is automatically calculated by hardware.

4.5.3.5.9 Sub-Carrier Generation

The video encoder generates the sub-carrier by internal direct digital synthesizer (DDS). The phase resolution of DDS is (1/1024) × 360°.

Sub-carrier to Horizontal (SC-H) phase can be controlled by the user. Writing SCPROG.SCSD automatically updates the sub-carrier phase as the specified value. Update occurs at line 9 in color field 1 for both NTSC and PAL. By default, preset values shown in Table 76 are applied. These values are chosen so that SC-H phase close to 0°.

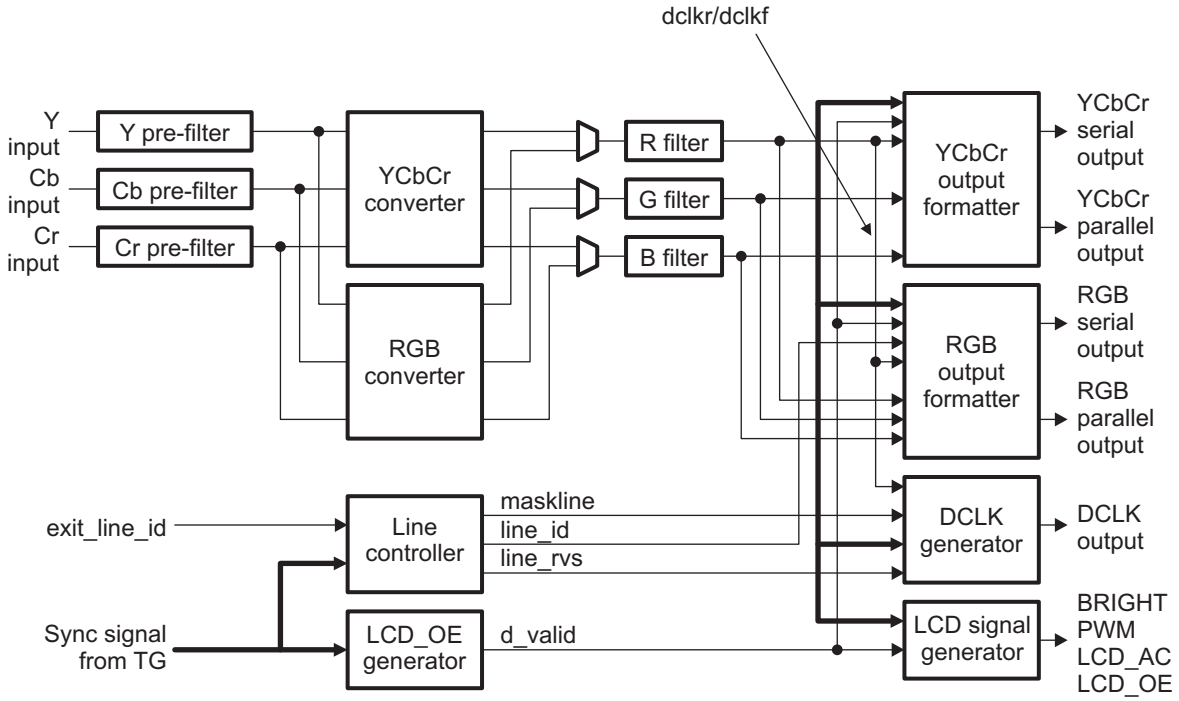
Table 76. Sub-Carrier Initial Phase Default Values

Mode	Preset Value
NTSC	378
PAL	356

4.5.4 Digital LCD Controller

The digital LCD controller is shown in Figure 77.

Figure 77. Digital LCD Controller Block Diagram



4.5.4.1 Digital Video Output Mode

The digital LCD controller supports four digital output modes. The mode can be selected by VMOD.VDMD and are shown in Table 77.

Table 77. Digital Video Output Modes

VDMD	Mode	Description
0	YCC16	16-bit YCbCr output mode. Y and C are output separately on 16-bit bus. Optionally supports embedded sync output.
1	YCC8	8-bit YCbCr output mode. 422 YCbCr is time-multiplexed on the 8-bit bus. Optionally supports embedded sync output (ITU BT.656 mode).
2	PRGB	Parallel RGB mode to output RGB separately. Optionally supports embedded sync output.
3	SRGB	Serial RGB mode to output RGB sequentially.

4.5.4.2 Timings

The timing parameter control registers are shown in Table 78. Figure 78 to Figure 80 show the timing charts for HSYNC, VSYNC, LCD_FIELD and LCD_OE. For interlaced operation when VMOD.NSIT is 1, the vertical interval and pulse width is counted by half line (0.5H).

Table 78. Timing Control Registers

Register	Description	Unit (1)
HSPLS	HSYNC pulse width	CLK
VSPLS	VSYNC pulse width	H (0.5H)
HINT	HSYNC interval (HINT + 1). Must be even when OSD clock is 1/2 VENC clock (standard timing)	CLK
HSTART	Horizontal data valid start position	CLK
HVALID	Horizontal data valid duration	CLK
VINT	VSYNC interval (VINT + 1)	H (0.5H)
VSTART	Vertical data valid start position	H
VSTARTA	Vertical data valid start position for even field. available only when VSTF = 1.	H
VVALID	Vertical data valid duration	H
VVALIDA	Vertical data valid duration for even field. available only when VVLDF = 1.	H
HSDLY	HSYNC delay	CLK
VSDLY	VSYNC delay	CLK

(1) Value in brackets apply to interlace (NSIT = 1)

Figure 78. Horizontal Timing

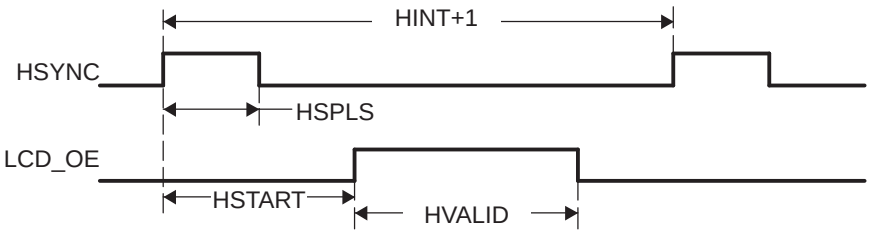
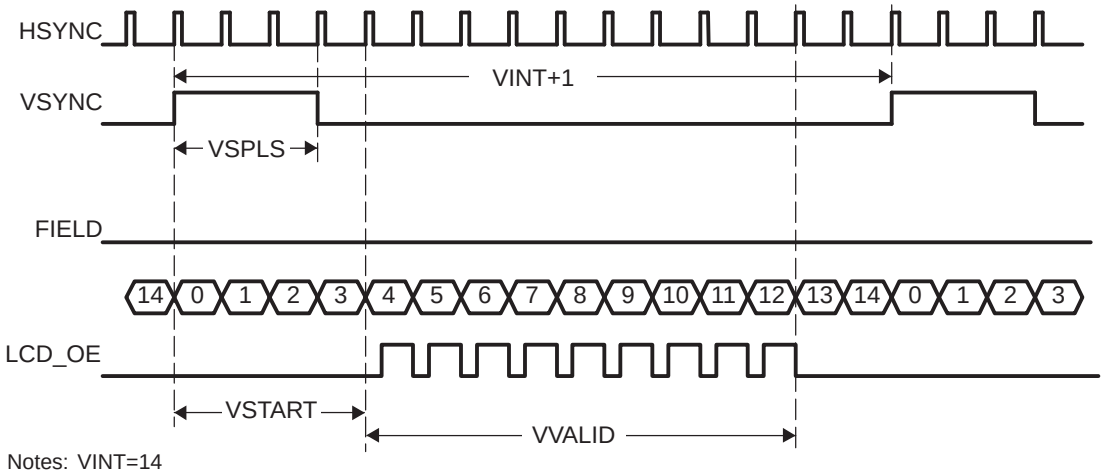
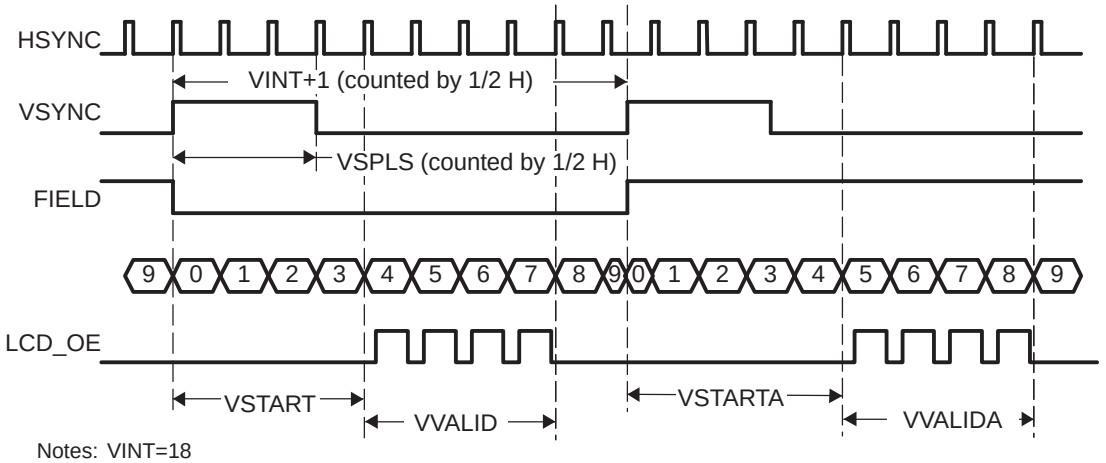


Figure 79. Vertical Timing (Progressive)



Notes: VINT=14
VSTART=4
VSPLS=3
VVALID=9

Figure 80. Vertical Timing (Interlaced)



Notes: VINT=18
VSTART=4
VSPLS=6
VVALIDA=4
VSTARTA=5

When in interlaced mode (VMOD.NSIT = 1 or NTSC/PAL), different VSTART positions and VVALID duration can be specified for odd and even fields. VSTART and VVALID are for odd fields and VSTARTA and VVALIDA are for even fields. VSTARTA is available only when LINECTL.VSTF is 1 and VVALIDA is available only when LINECTL.VVLDF is set to 1.

The HSYNC and VSYNC outputs can be delayed via HSDLY and VSDLY registers, respectively, without affecting the timing of the internal sync signals. The LCD_FIELD output is also delayed by VSDLY. The delays unit is CLK.

In standard mode operation (VMOD.VMD = 0), horizontal and vertical pulse width and interval timings are fixed by hardware to conform to the video standard regardless of the HSPLS, VSPLS, HINT, and VINT registers. Regarding pulse width, the optional sync pulse width processing mode is provided to program standard mode sync pulse width by the HSPLS and VSPLS registers. This mode is enabled when SYNCTL.SYSW is 1. When interlaced (VMOD.HDMD = 0), VSYNC pulse width is counted in 0.5H (half lines). The parameters are shown in Table 79.

Table 79. Standard Video Timing

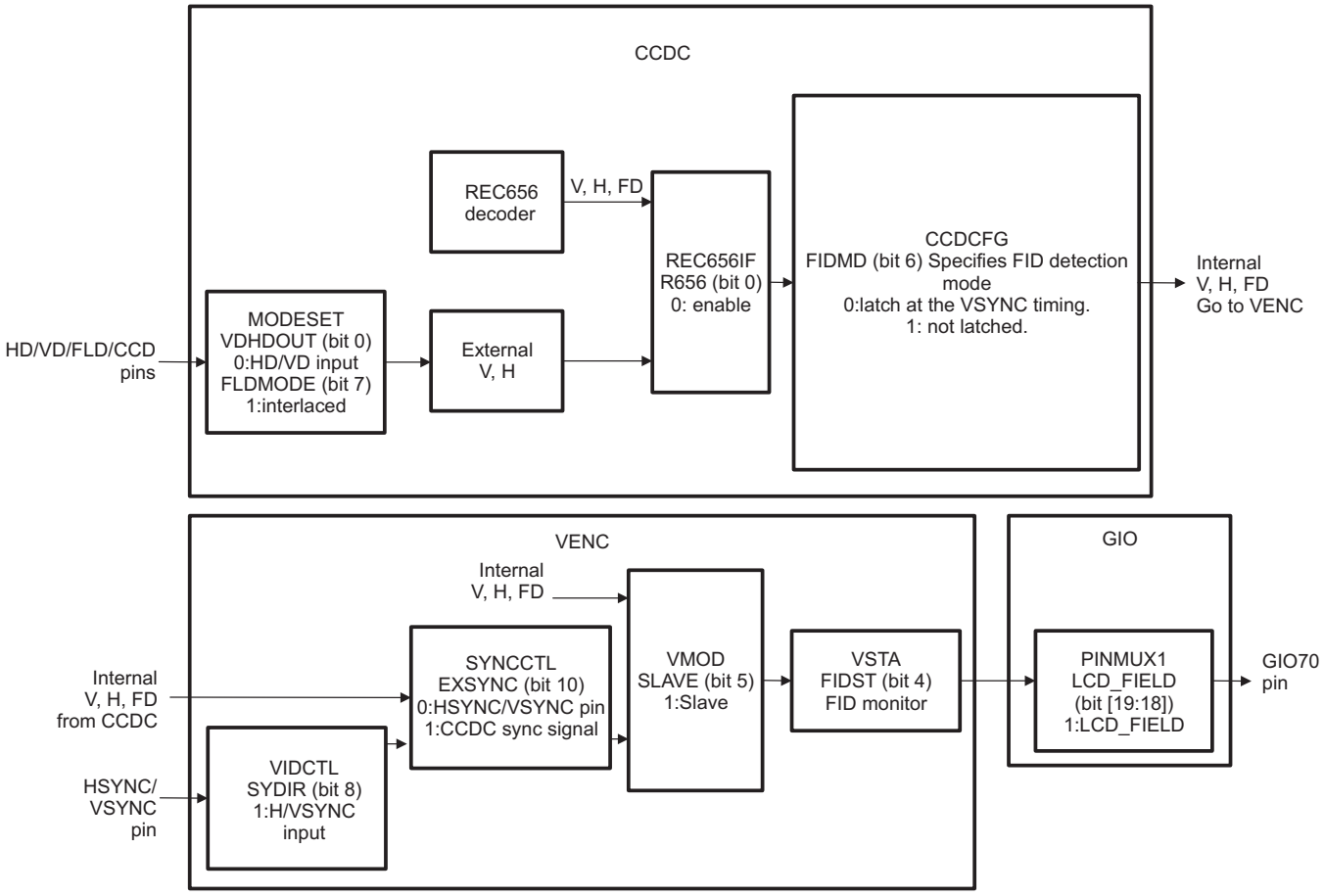
	SDTV (HDMD = 0)		HDTV (HDMD=1)				
Parameter	**NTSC (TVTYP = 0)**	**PAL (TVTYP = 1)**	**525p (TVTYP = 0)**	**625p (TVTYP = 1)**	**1080i (TVTYP = 2)**	**720p (TVTYP = 3)**	**Unit**
HSYNC pulse width	127	127	63	63	63	63	CLK
VSYNC pulse width	6	5	6	5	5	5	H
Horizontal interval	1716	1724	858	864	2200	1650	CLK
Vertical interval	262.5	312.5	525	625	562.5	750	H

4.5.4.3 Slave Mode Timings

4.5.4.3.1 Slave Mode Sync Path Using VPFE

Figure 81 illustrates how to set the VENC slave mode.

Figure 81. Slave Mode Sync Path

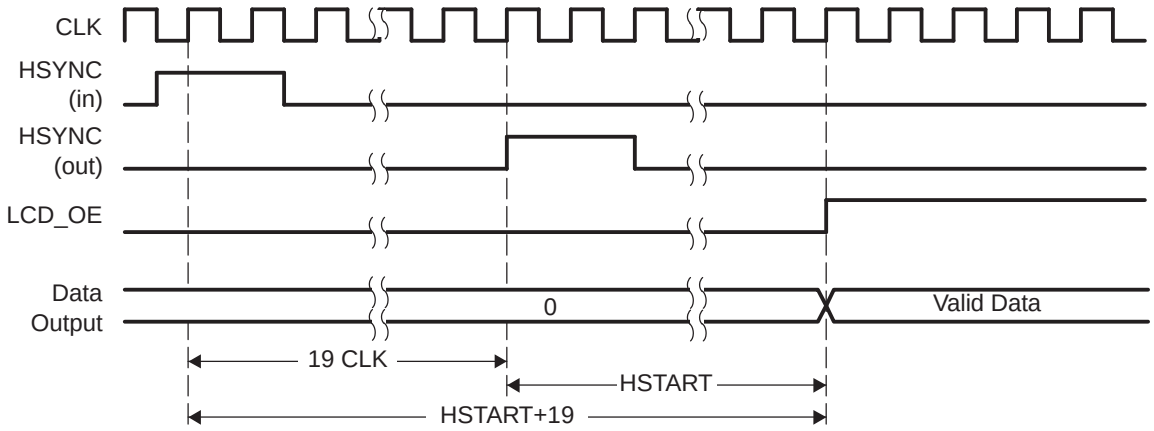


4.5.4.3.2 Horizontal Timing

Figure 82 shows the slave mode horizontal timing chart. It takes 19 CLKs for HSYNC output to be asserted after the external HSYNC input is latched. The data start position from HSYNC output is not different from master mode. However, HSYNC output cannot be seen from the outside chip because HSYNC pin is shared with input for slave and output for master. The HSYNC output timing in Figure 82 is for reference.

This horizontal timing is always applied, regardless of video timing mode (VMOD.VMD).

Figure 82. Horizontal Timing Chart



4.5.4.3.3 Vertical Timings

Figure 84 shows the vertical timing chart of NTSC slave mode. Vertical timing is reset when VSYNC rise transition is detected at HSYNC rising edge or the center of line (0.5H). Figure 85 indicates the PAL slave mode. Please note that the field is oppositely detected in PAL. In vertical timing chart of slave mode, output timings of HSYNC, VSYNC and VSYNC pins are denoted but these cannot be seen from outside the chip because they are used as input in slave mode.

If VSYNC is behind HSYNC assertion, vertical reset is suspended until the next HSYNC rise edge. Figure 83 shows various VSYNC detection timings.

Figure 83. VSYNC Input Latch Timing

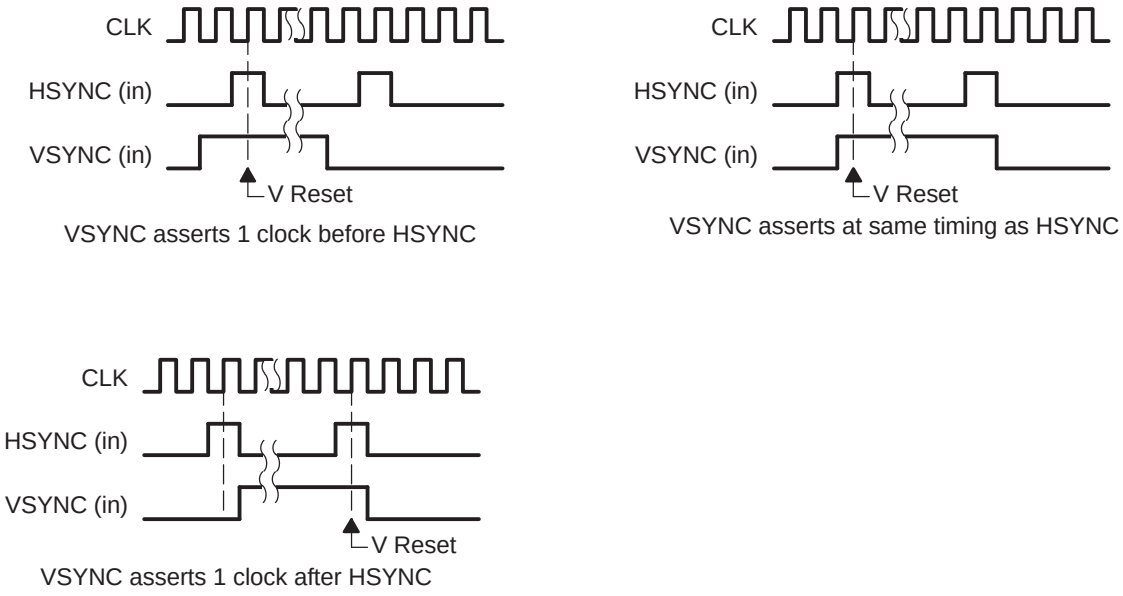


Figure 84. Vertical Timing Chart (NTSC)

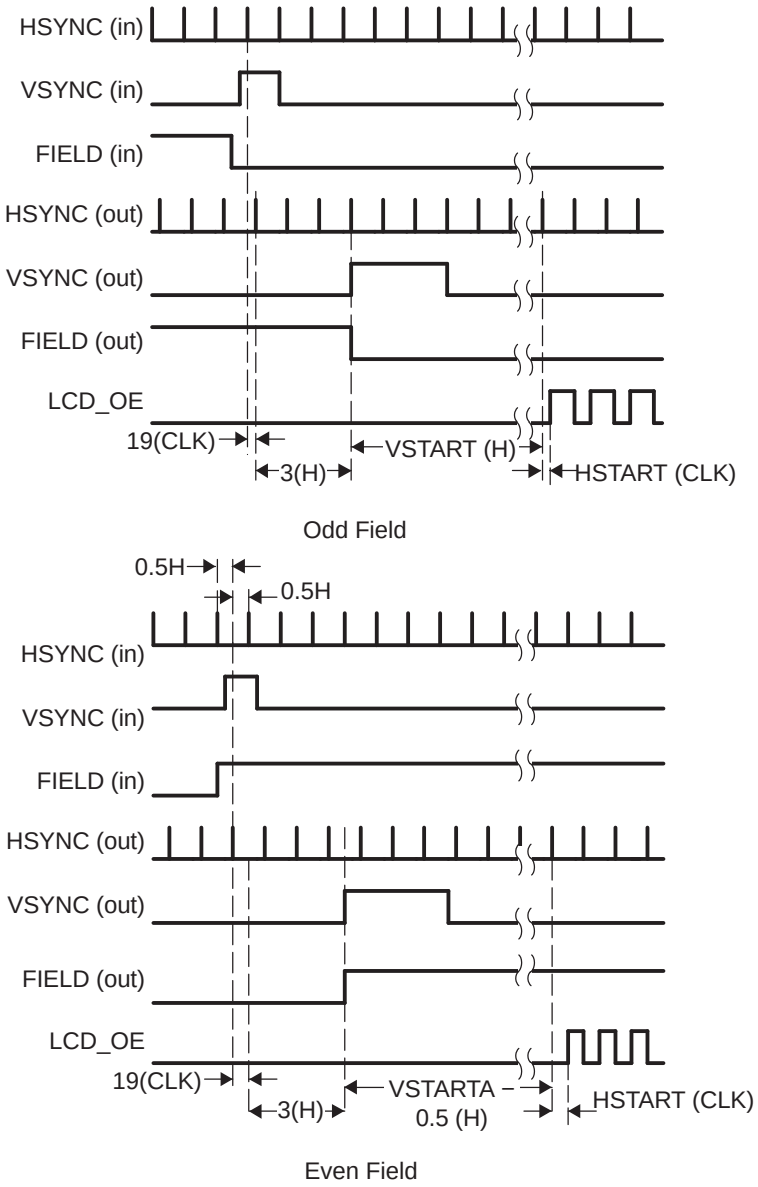


Figure 85. Vertical Timing Chart (PAL)

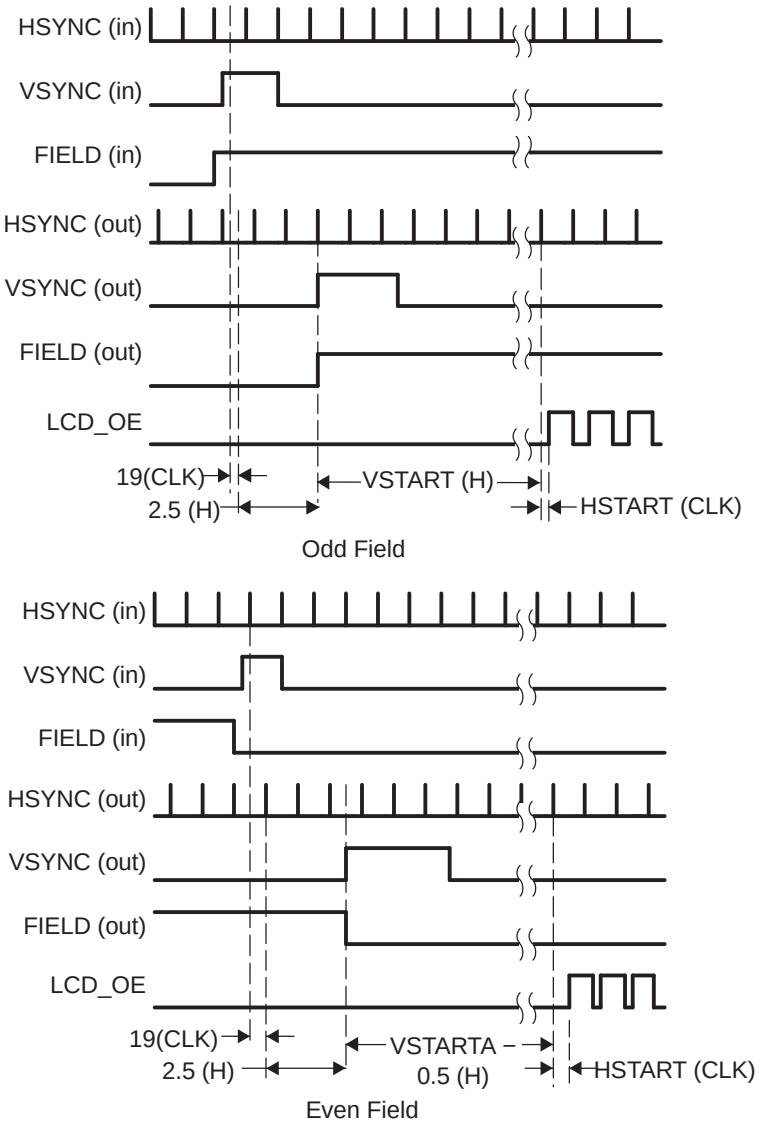


Figure 86 shows the vertical timing char of slave non-standard progressive mode (VMD=1, NSIT=0). Figure 87 indicates the nonstandard interlace timing (VMD=1, NSIT=1). Vertical timing is reset when VSYNC rise transition is detected at HSYNC rising edge. Please note that interlace mode vertical timing is reset only when VSYNC rise transition is detected at HSYNC rising edge (not at the center of line (0.5H) as in NTSC/PAL).

Figure 86. Vertical Timing Chart (Nonstandard/Progressive)

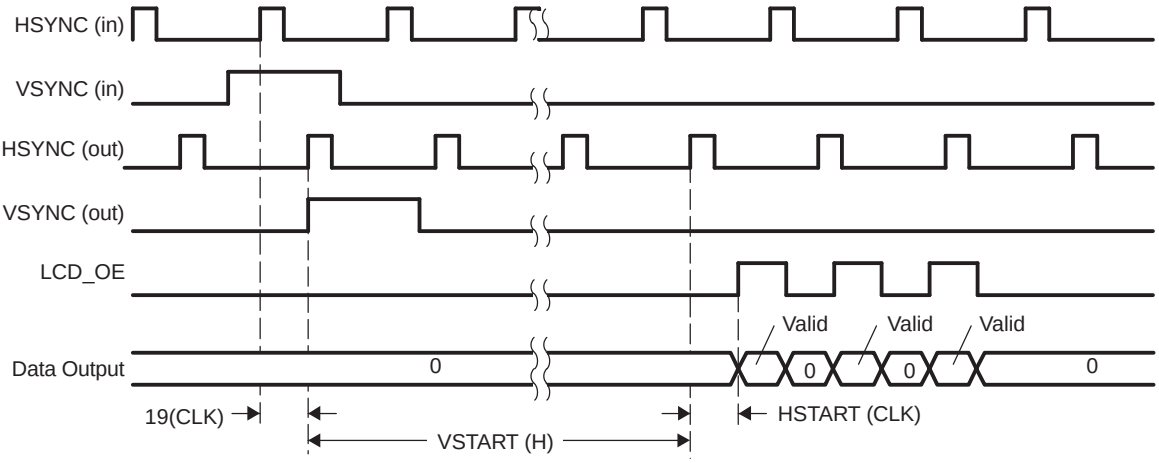
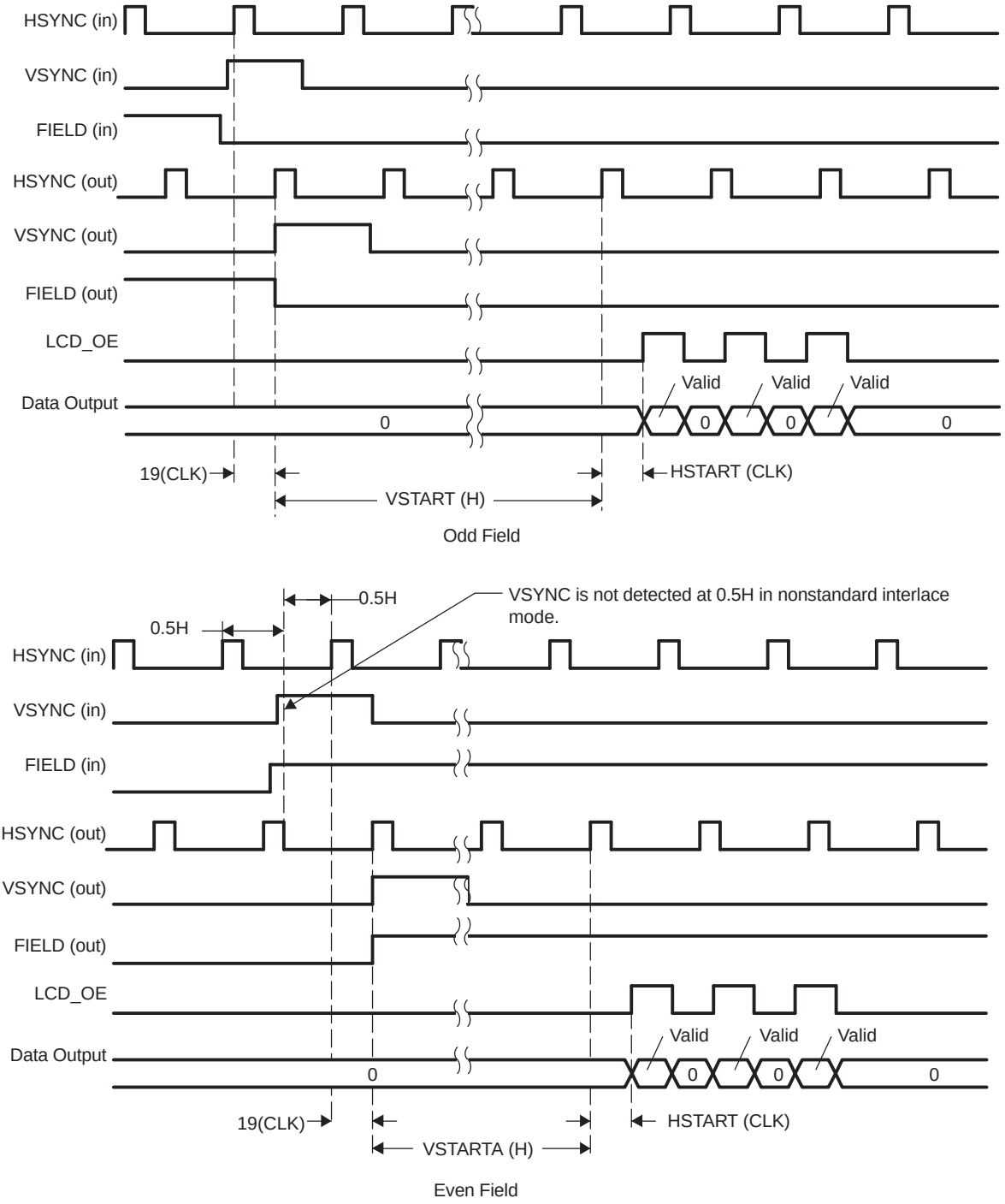


Figure 87. Vertical Timing Chart (Nonstandard/Interlace)



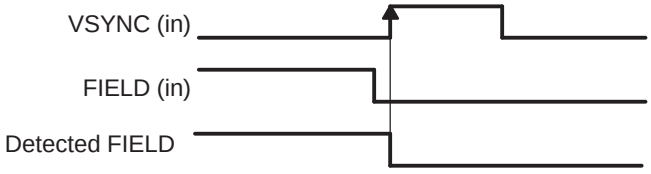
4.5.4.3.4 Slave Mode Field Detection

For slave interlace mode, namely when NTSC/PAL (VMOD.VMD = 0 and VMOD.HDMD = 0) or non-standard interlace (VMOD.VMD = 1 and VMOD.NSIT = 1), external field ID is detected. There are four field detection modes:

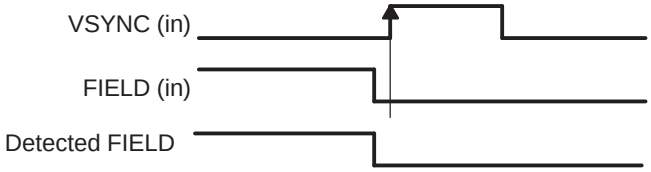
- Latch FIELD input at VSYNC rise edge
- Use raw FIELD input
- Use VSYNC input as FIELD
- Detect VSYNC phase

These four modes can be selected by SYNCCTL.EXFMD. Figure 88 shows the timing of each mode.

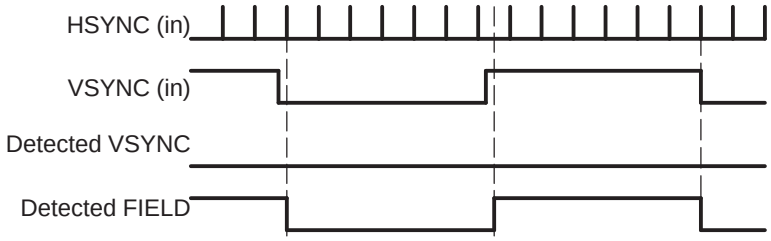
Figure 88. Field Detection Mode



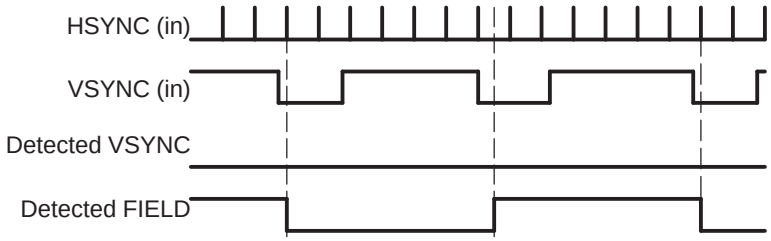
(1) Latch FIELD input at VSYNC rise edge



(2) Use raw FIELD input



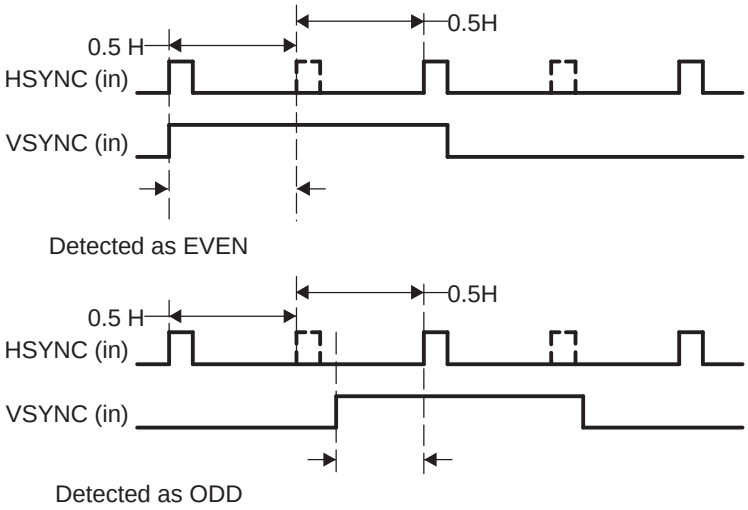
(3) Use VSYNC input as FIELD



(4) Detect VSYNC phase

In the option 4 (Detect VSYNC phase), the timing generator detects VSYNC assertion position in a line. When VSYNC is in the first half of a line, the field is detected as even. When VSYNC is the second half of a line, the field is detected as odd. Figure 89 shows this detection scheme. This mode is only available for NTSC/PAL. When in non-standard mode, Field_id is always detected as odd in option 4.

Figure 89. Field Detection by VSYNC Phase



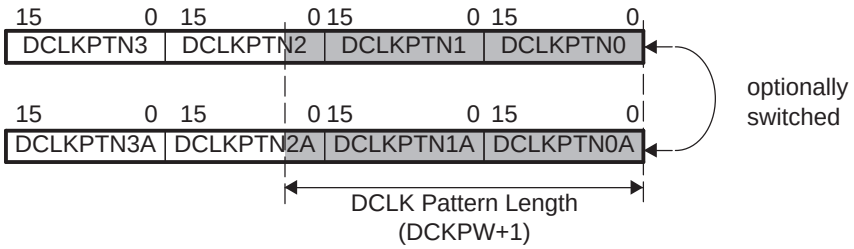
4.5.4.4 DCLK Generator

The LCD controller can generate a dot clock, called DCLK, that is fed to LCD panels. The generated DCLK is output from the VCLK pin. Frequency, waveform, and valid duration of the DCLK is programmed by register settings with various options. The digital data is output synchronized to the rising edge of DCLK.

4.5.4.4.1 Pattern Register

The DCLKPTN register is provided for DCLK waveform configuration. The user can configure various waveforms for DCLK within and up to a 64-cycle period. The register is 64 bits in length, mapped onto four 16-bit registers (DCLKPTN0-3). The effective pattern length can be specified in DCLKCTL.DCKPW. Moreover, another set of pattern registers with same structure (DCLKPTN0-3A) is optionally provided. This enables the user to switch the waveform on certain lines. Figure 90 shows the DCLK pattern register configuration scheme.

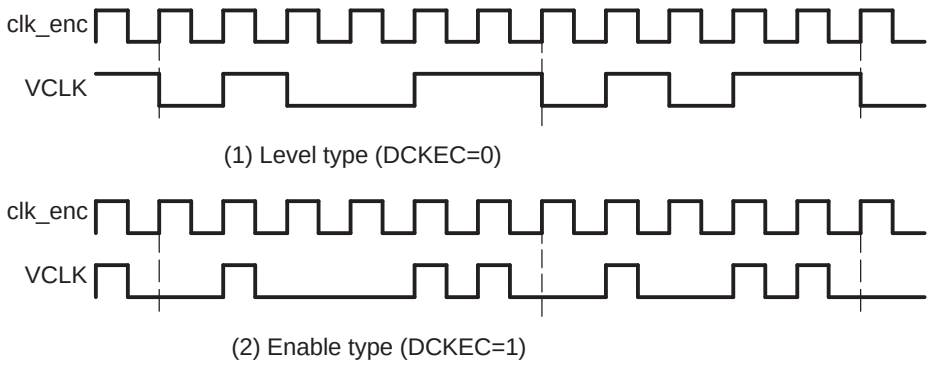
Figure 90. Pattern Register Configuration



There are two types of clock waveform configurations. They can be selected by DCLKCTL.DCKEC. For an example, see Figure 91.

- When DCKEC = 0, the pattern register becomes the clock level pattern of DCLK itself (Level mode).
- When DCKEC = 1, the pattern register works as the clock enable of the ENC clock (Enable mode).

Figure 91. DCLK Pattern Mode



Notes: DCKPW=5
DCLKPTN0=0013h

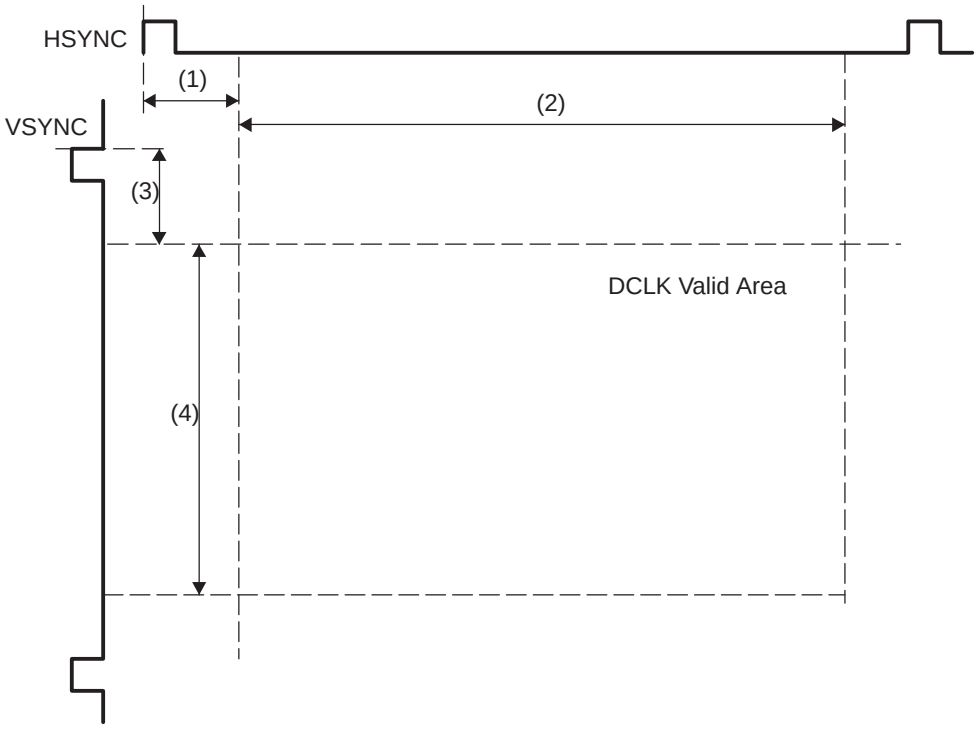
4.5.4.4.2 Masking

It is possible to mask the DCLK signal in horizontal and vertical directions. The registers listed in Table 80 allow you to set when DCLK is valid in the horizontal and vertical start positions of LCD display data. As shown in Figure 92, the valid start position in the horizontal direction is set relative to HSYNC, and the length of valid data in the horizontal position is set relative to the horizontal start position of valid data. The horizontal resolution is in ENC clocks. Figure 92 shows that valid data in the vertical direction is configured similar to valid data in the horizontal direction. DCLKCTL.DCKME can activate DCLK masking. Regarding horizontal start position, two sets of registers are provided as well as a pattern register.

Table 80. DCLK Masking Registers

Mark	Register	Description	Unit
1	DCLKHSTT.DHS DCLKHSA.DCHS	Horizontal DCLK mask start position.	CLK
2	DCLKHR.DCHR	Horizontal DCLK mask range.	CLK
3	DCLKVSTT.DVS	Vertical DCLK mask start position.	H
4	DCLKVVLD.DVV	Vertical DCLK mask range.	H

Figure 92. DCLK Masking



4.5.4.4.3 Half-Rate Mode

It is possible to divide the DCLK by two. The dividing can be applied to the internal DCLK or the output DCLK. When DCLKCTL.DCKOH is 1, only the DCLK output is divided by two. Since the internal DCLK is not divided, the RGB data rate is not changed. Therefore, this mode can be used to connect to the LCD that captures the data using both edges of DCLK. On the other hand, when DCLKCTL.DCKIH is 1, the internal DCLK is divided by two. When output dividing is not enabled, two clocks can be output per one data sample. Therefore, this mode can be used to connect to the LCD that requires data at a rate of double the clock frequency.

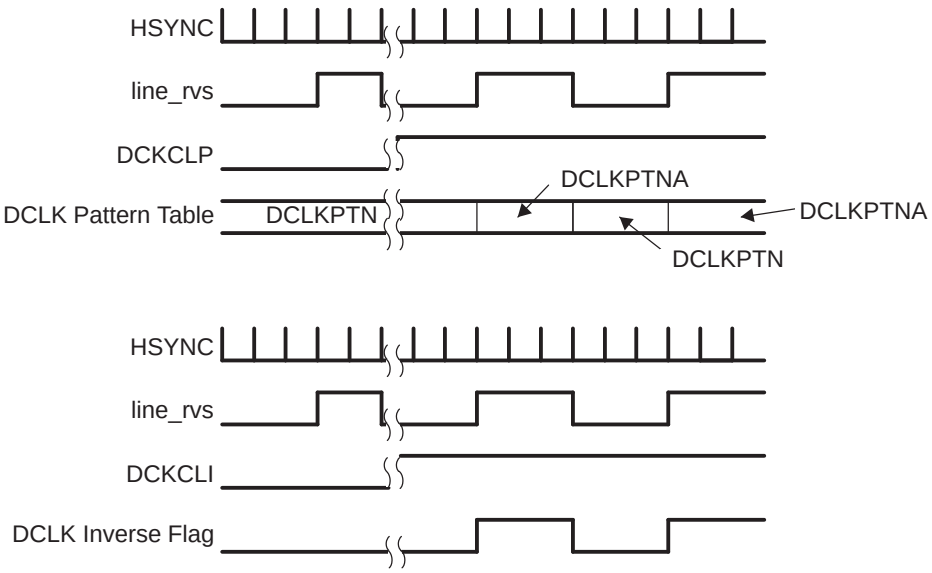
4.5.4.4.4 Line Control

The DCLK controller provides two kinds of DCLK waveform alteration by line. The culling line ID that controls RGB data output sequence also affects DCLK waveform alteration. Figure 93 shows this functionality.

- DCLK Pattern Switching. When LINECTL.DCKCLP = 1, DCLK pattern can be switched according to the culling line ID. The DCLK pattern on each line is specified by the DCLKPTN and DCLKPTNA registers.
- DCLK Polarity Inversion. When LINECTL.DCKCLI = 1, DCLK polarity is inverted on the line whose line ID is the culling line ID set by the CULLLINE register.

Both DCKCLP and DCKCLI can be set to 1, simultaneously.

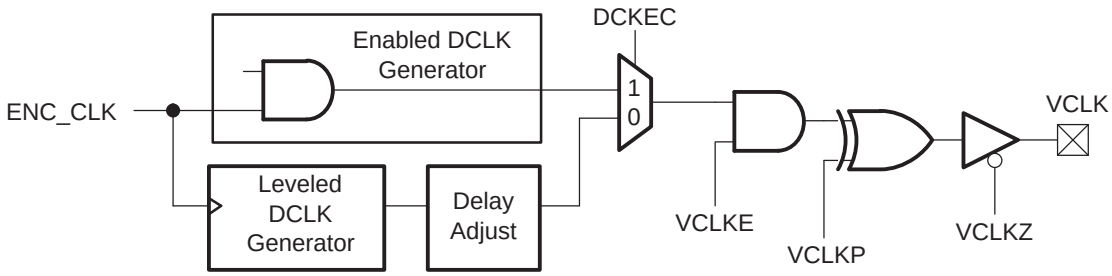
Figure 93. DCLK Pattern Switch/Inversion by Line



4.5.4.4.5 DCLK Output

VCLK output attributes, such as output enable, polarity and clock output on/off, can be controlled by registers in VIOCTL. Moreover, the level type DCLK output can have the offset of-0.5, 0.5 or 1.0 ENC CLK as set by DCLKCTL.DOFST. Figure 94 shows the DCLK output block diagram.

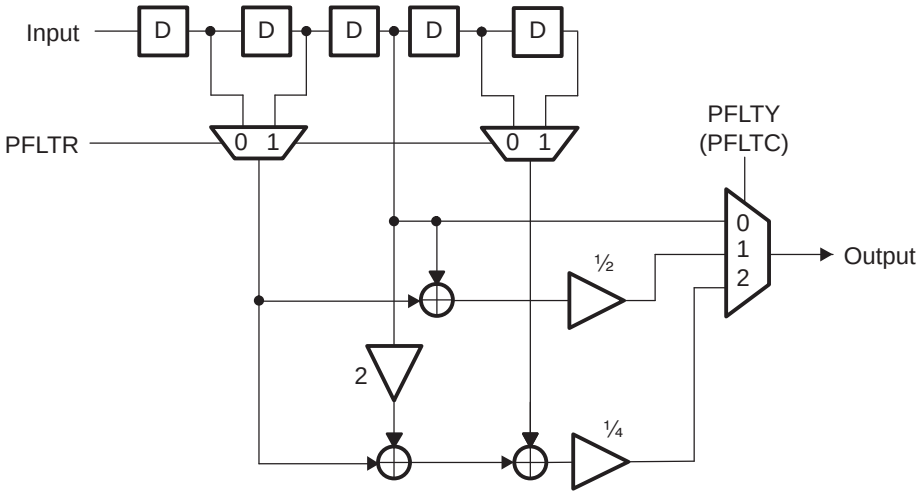
Figure 94. DCLK Output



4.5.4.5 YCbCr Pre-Filter

The video encoder inputs data from the OSD module in YCbCr format. A YCbCr filter (Figure 95) resides in the beginning of the data path. Each component (Y, Cb and Cr) has its own filter. The filter length can be programmed to 2 or 3 taps by PFLTY/PFLTC for Y/C, respectively, in the VDPRO register. The pre-filter sampling rate can be chosen to be either VENC clock or 1/2 VENC clock by VDPRO.PFLTR.

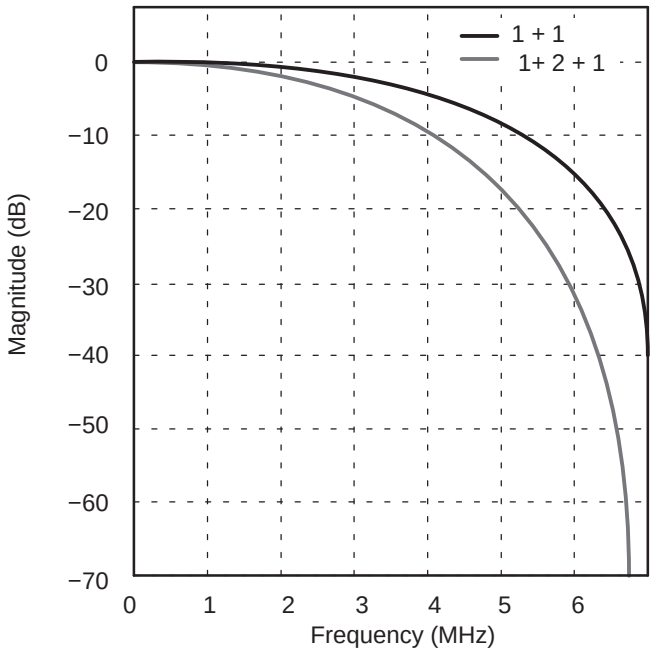
Figure 95. YCbCr Pre-Filter



The pre-filter frequency response with the sampling rate of 13.5 MHZ is shown in Figure 96.

The group delay of the filter is 1 when PFLTY/PFLTC = 0 or 2, and 0.5 for PFLTY/PFLTC = 1. Do not set PFLTY and PFLTC to different values or Y and C will not be aligned.

Figure 96. Frequency Response of the Pre-Filter



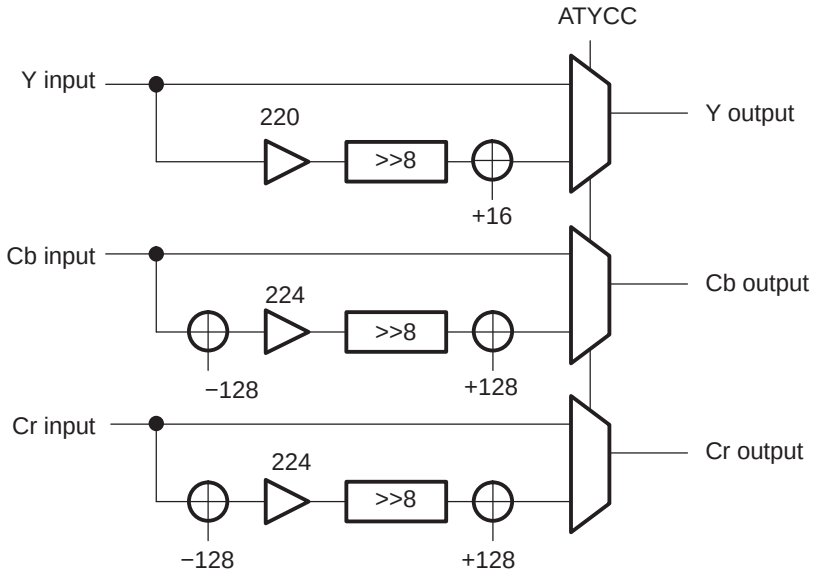
4.5.4.6 YCbCr Output Formatter

The YCbCr Output Formatter manages YCbCr data output in YUV16 and YUV8 modes.

4.5.4.6.1 YCbCr Conversion

YCbCr data processed by the pre-filter is then input to the YCbCr converter (Figure 97). This converter can attenuate the data with full range (0-255) levels to ITU-R BT.601 compliant levels (Y:16-235, C:16-240). The attenuation is enabled by setting VDPRO.ATYCC to 1.

Figure 97. YCbCr Conversion Block Diagram



4.5.4.6.2 16-Bit YCbCr Output Mode (YCC16)

In YCC16 mode, the Y (luma) signal is output to YOUT[7:0] at every VCLK rising edge, while Cb and Cr (chroma) are alternately multiplexed onto COUT[7:0]. For details of this output mode and the optional controls, see Section 2.2.1.

4.5.4.6.3 8-Bit YCbCr Output Mode (YCC8)

In YCC8 mode, each component of the OSD YCbCr signal is alternately output from YOUT[7:0]. For details of this output mode and the optional controls, see Section 2.2.2.

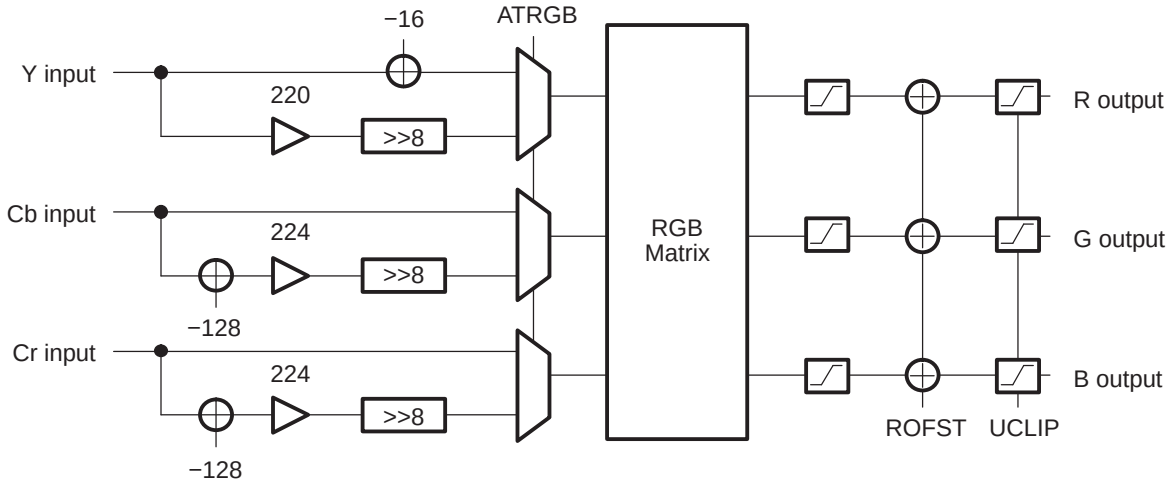
4.5.4.7 RGB Output Formatter

The RGB output formatter manages RGB data output in RGB parallel and serial modes.

4.5.4.7.1 RGB Conversion

Figure 98 shows the block diagram of the YCbCr to RGB converter. At the first stage, YCbCr input ranging from 0-255 can be attenuated to ITU-R BT601 levels (Y:0-219, C:-128-128). This is enabled by setting VDPRO.ATRGB = 1.

Figure 98. RGB Conversion Block Diagram



The formatted YCbCr data is then converted to RGB according to the following equation:

$$\begin{bmatrix} R \\ G \\ B \end{bmatrix} = \frac{1}{1024} \begin{bmatrix} GY & 0 & RV \\ GY & -GU & -GV \\ GY & BU & 0 \end{bmatrix} \begin{bmatrix} Y-16 \\ Cb-128 \\ Cr-128 \end{bmatrix}$$

The coefficients of the matrix can be programmed by setting the DRGBX0-DRGBX4 registers with the appropriate coefficients. By default, these values are set to the ITU-R BT601 RGB conversion matrix. RGB ranging from 0 to 219 is possible from the REC.601 formatted signal (Y:16-235, C:16-240). Since the converted RGB may become negative due to finite precision arithmetic, zero level clipping is applied.

Then the offset specified by RGBCLP.OFST is added followed by upper level clipping. The clip level is set by RGBCLP.UCLIP. The output RGB samples are limited to 8-bit resolution.

4.5.4.7.2 RGB Filter

A low-pass filter can then be applied to the converted RGB data. There is a separate LPF module for each color component, each with 8-bit inputs and outputs. For each component, either a 3-tap or a 7-tap LPF can be selected via RGBCTL.DFLTS. The sampling clock can also be chosen from the VENC clock or its divided clock by RGBCTL.DFLTR. Even though there are separate filters that operate in parallel, the user does not have individual control so these settings apply to all components.

NOTE: When YCbCr output is selected VMOD.VDMD = 0 or 1, (YCC16 or YCC8 modes), the RGB filters should be disabled (DFLTS = 0).

4.5.4.7.3 Parallel RGB Mode (PRGB)

In parallel RGB mode, up to 18-bit resolution data (6-bits each for RGB) can be output. By default, RGB565 can be output using the dedicated YOUT[7:0]/COUT[7:0] signals. For additional details, see Section 2.2.3. RGB888 and RGB565 output modes can also be supported by assigning additional GPIO pins to the display interface. This assignment, done via the pin multiplexing, is controlled from the System module, described in Section 2.3.

4.5.4.7.4 Serial RGB Mode (SRGB)

For Serial RGB modes, the RGB data samples are output serially, multiplexed onto the YOUT bus. Output data is sub-sampled at DCLK rising edge when data valid signal (LCD_OE) is asserted, and output signals are held low when LCD_OE is deasserted. See Section 2.2.4 for additional details and options, including the IronMan interface protocol.

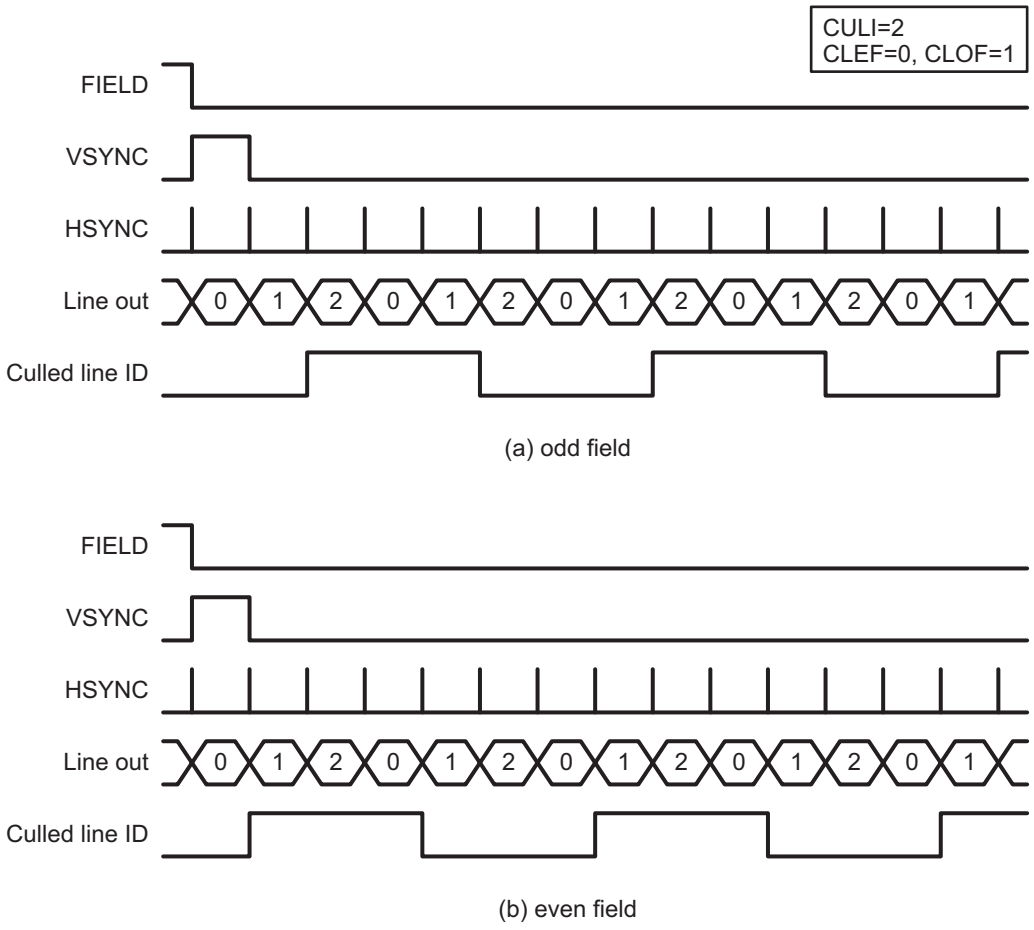
4.5.4.8 Line ID Control

Line ID is the line identification flag altered at HSYNC and reset by VSYNC. This flag is used for the RGB rotation order selector or DCLK waveform alteration. Normally, line ID is toggled at every HSYNC. In addition to this normal behavior, the LCD controller provides a culling line ID feature. This feature enables the use of the line ID toggled by a specified line interval. You can also set the line ID toggle position within the interval for even and odd field, respectively.

The generated culled line ID in Figure 99 affects the RGB rotation order when LINECTL.RGBCL = 1. In this mode, the XORed signal of the actual line ID and the culled line ID operates as the ID for the RGB rotation order.

In addition to RGB order, the DCLK waveform can be controlled by the culled line ID. When LINECTL.DCKCLP = 1, the effective DCLK pattern register (DCLKPTN) is switched by the culled line ID. The DCLKPTN is selected for culled line ID = 0 and DCLKPTNA for 1. As well as pattern switching, a DCLK inversion feature is also provided when LINECTL.DCKCLI = 1. In this mode, the created DCLK waveform is inverted for the culled line ID = 1.

Figure 99. Culled Line ID

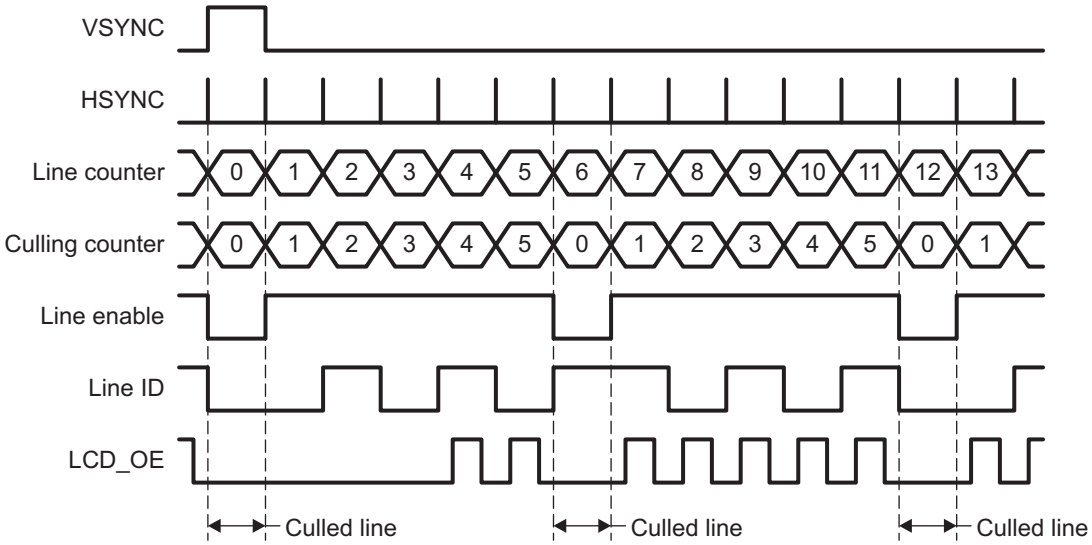


For PAL, the field is identified as odd when FIELD = 1.

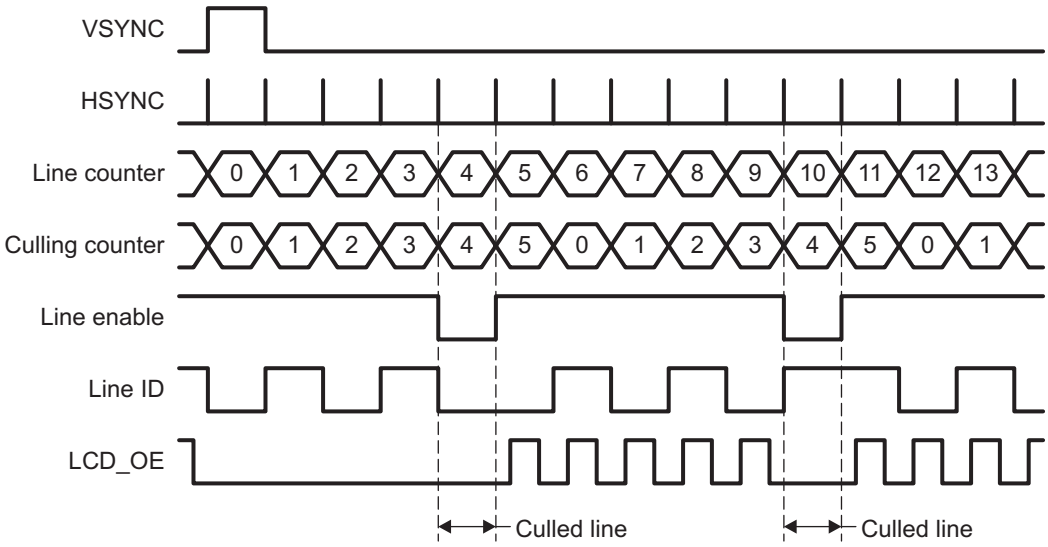
4.5.4.9 5/6 Line Culling

The digital video output can be vertically culled of 5/6. Setting LINECTL.VCL56 to 1 activates the culling. When in this mode, one line of video output is discarded every six lines. The VENC asserts the sync for the OSD and reads data from the OSD, but ignores it for output for the culled line. HSYNC output and LCD_OE assertion are also disabled in the culled line. The line position to be culled can be controlled by the VCLRD and VCLID bits in LINECTL. See Figure 100 and Figure 101 for details of the operation. Culling is enabled on the line where the internal culling counter (remove_counter) value is equal to the VCLID bit value. The internal culling counter is incremented at hsync and reset at vsync. The reset value can be 0 or a pseudo-random value that can be selected by the VCLRD bit.

Figure 100. 5/6 Line Culling Mode

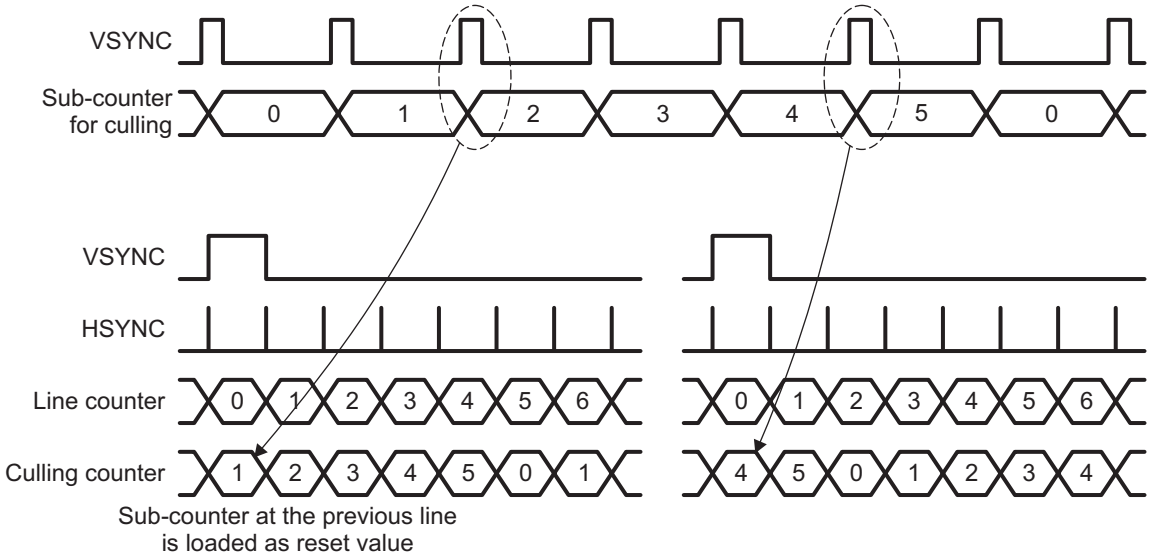


(1) VCLRD=0, VCLID=0, V_VALID=4



(2) VCLRD=0, VCLID=4, V_VALID=4

Figure 101. Random Reset of Vertical Culling Counter



4.5.4.10 Output Hold

The LCD controller provides a video output hold function. The controller can stop the operation of the timing generator when the current line or field transmission is completed. During the hold mode, reading data from the OSD is suspended and the output of the sync signals and video data is also suspended. The hold function is available only for digital video output in non-standard mode.

Setting the LINECTL.HLDL to 1 brings the controller into the line hold mode (Figure 102). Once HLDL is set, the controller automatically turns into the hold mode when the current line transmission is completed. Similarly, setting LINECTL.HLDF to 1 activates the field hold mode (Figure 103). After HLDF is set, the timing generator is suspended when the current field transmission is completed. Clearing these bits to 0 restarts the timing generator.

Figure 102. Output Line Hold Mode

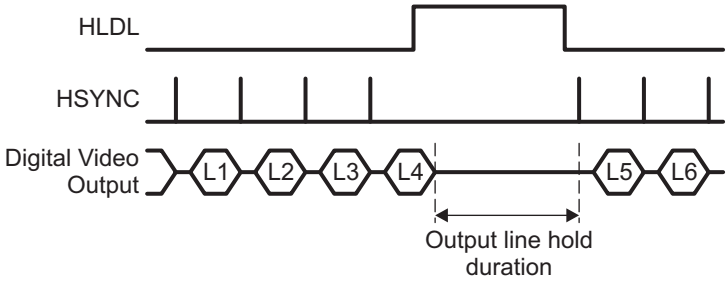
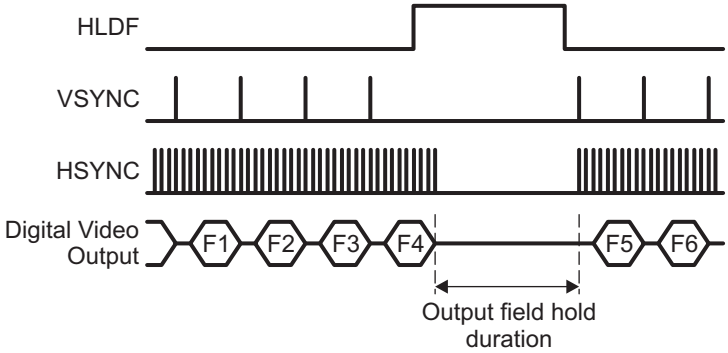


Figure 103. Output Field Hold Mode



4.5.4.11 LCD_OE Horizontal Culling

LCD_OE can be horizontally culled when HVLDCL0.HCM is 1. When in this mode, you can specify the culling period and valid pattern by HVLDCL0.HCPW and HVLDCL1.HCPT, respectively. Figure 104 shows the register usage for LCD_OE culling. Figure 105 shows an example of LCD_OE horizontal culling timing. In Figure 105, DCLK is set to be the same as CLK. Every third data is thrown away. Zero is transmitted during LCD_OE = 0.

Figure 104. LCD_OE Horizontal Culling Register

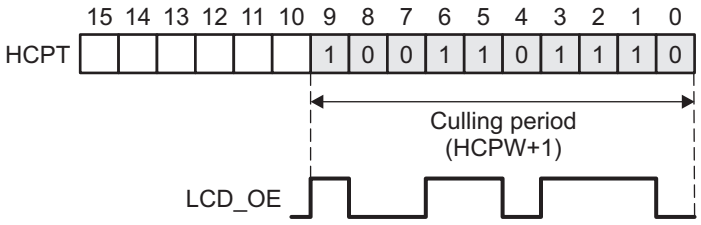
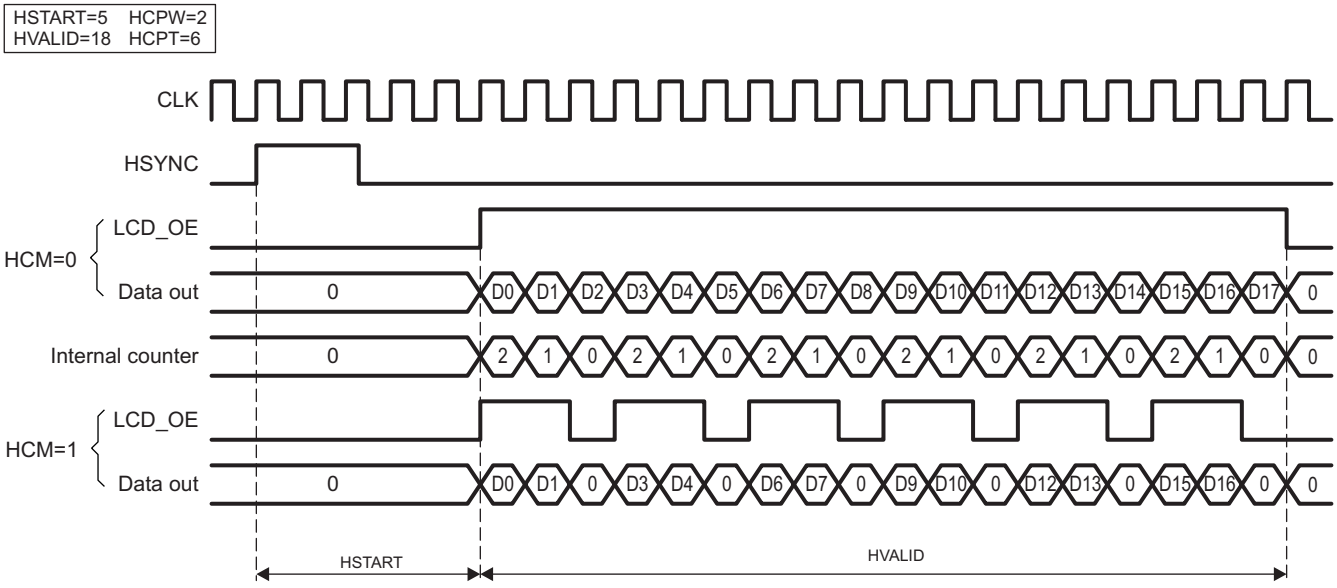


Figure 105. LCD_OE Horizontal Culling Timing Chart



4.5.5 Other Video Encoder Features

4.5.5.1 Internal Color Bar

The VENC can internally generate the color bar by itself. Setting VDPRO.CBAE = 1 enables the internal color bar generator. VDPRO.CBTY switches the saturation of the color bar (0 = 75%, 1 = 100%).

Table 81. Digital Output Value of Color Bar Generator

	100% (VDPRO.CBTYP = 1)			75% (VDPRO.CBTYP = 0)		
Color	**Y**	**Cb**	**Cr**	**Y**	**Cb**	**Cr**
Black	16	128	128	16	128	128
Blue	41	240	110	35	212	114
Red	81	90	240	65	100	212
Magenta	106	202	222	84	184	198
Green	145	54	34	112	72	58
Cyan	170	166	16	131	156	44

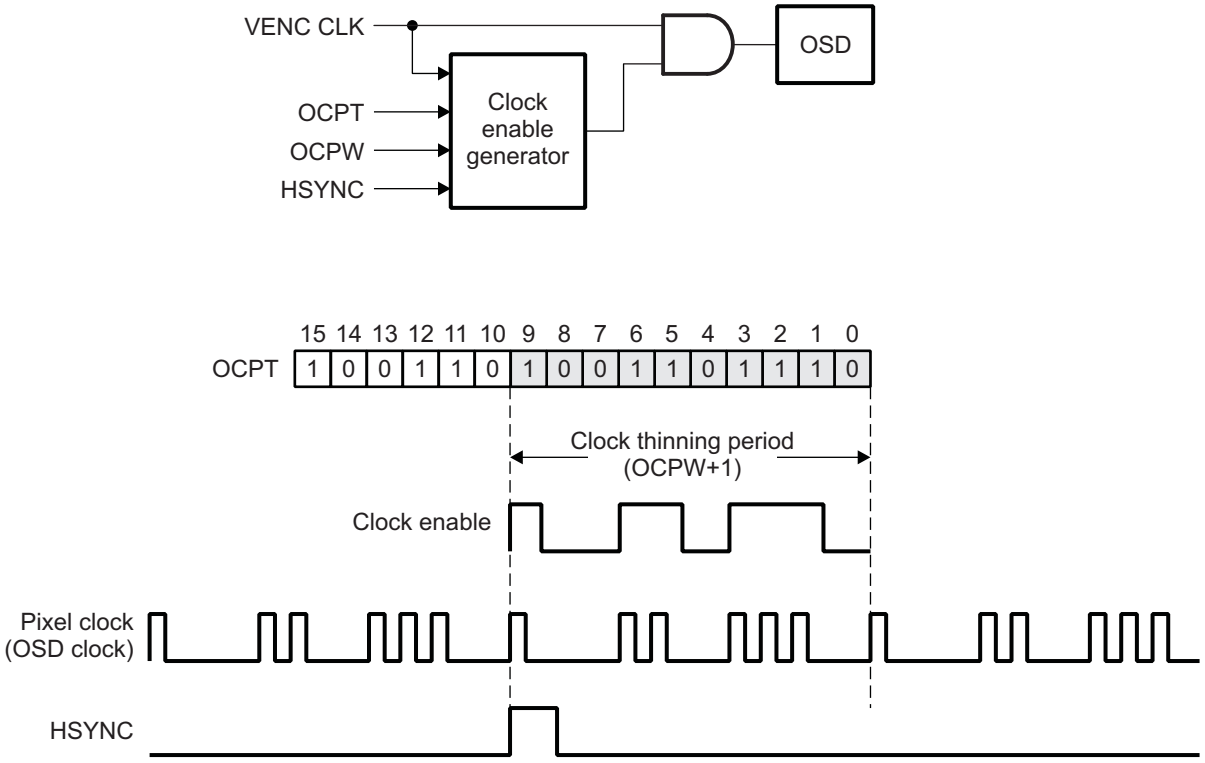
Table 81. Digital Output Value of Color Bar Generator (continued)

	100% (VDPRO.CBTYP = 1)			75% (VDPRO.CBTYP = 0)		
Color	**Y**	**Cb**	**Cr**	**Y**	**Cb**	**Cr**
Yellow	210	16	146	162	44	142
White	235	128	128	180	128	128

4.5.5.2 Pixel Clock Programming

You can arbitrarily thin out the pixel clock, which is the main clock used in the OSD module. Thinning out is processed periodically in the horizontal direction. During this period, you can freely program the active clock position. The period is specified by the OCPW bit in the OSD clock control 0 register (OSDCLK0) and the clock enable pattern is specified by the OCPT bit in the OSD clock control 1 register (OSDCLK1). The period of the clock gating pattern is started at HSYNC. Figure 106 shows the pixel clock thin out processing scheme.

Figure 106. Thinning Out Pixel Clock



After a reset, the OCPW bit is set to 1 and the OCPT bit is set to 2h so that the resulting pixel clock becomes half of VENC CLK (when VENC CLK is 27 MHz, the pixel clock becomes 13.5 MHz). For NTSC/PAL use, there is no change of these registers from the default value. It is required to clear the OCPW bit to 0 and set the OCPT bit to 1 for progressive scan output.

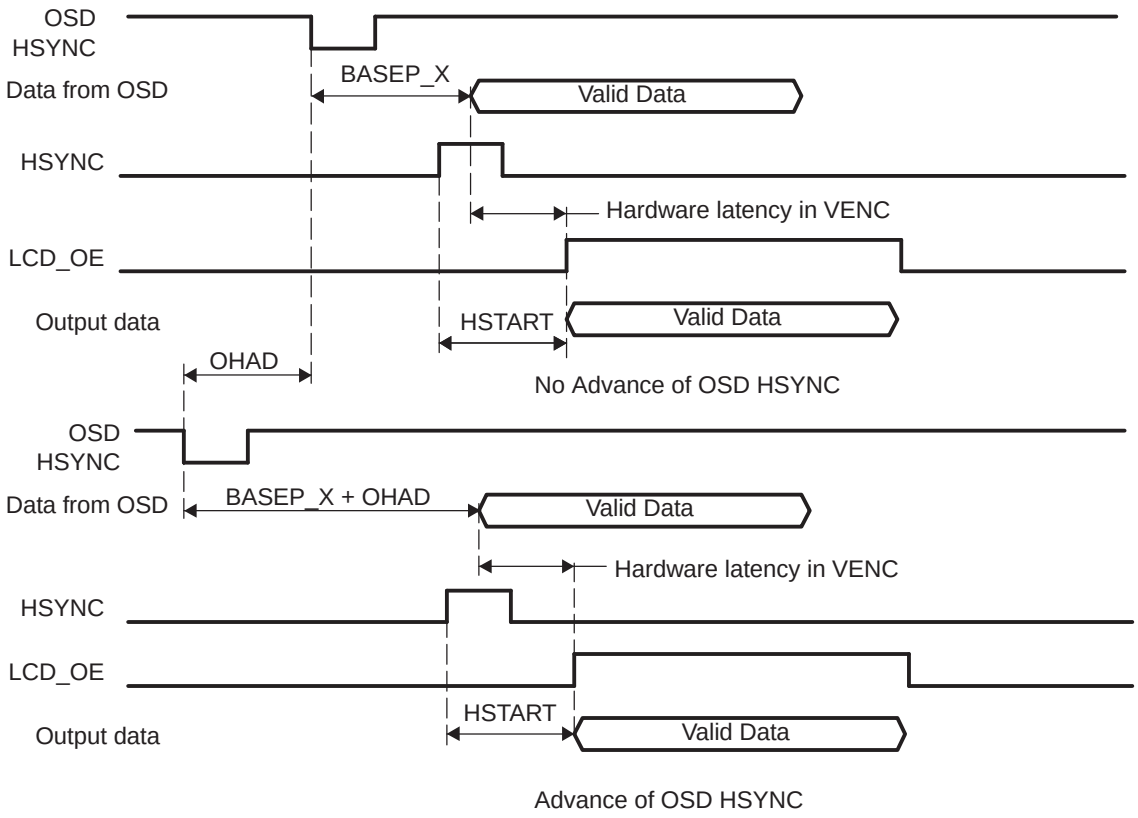
4.5.5.3 OSD Sync Control

4.5.5.3.1 Advanced Horizontal Sync

The VENC provides the sync signals to the OSD module. The horizontal sync timing is controlled by the VENC hardware so that the horizontal data start position is aligned between VENC and OSD when HSTART and BASEP_X (OSD register) have the same value (when OSD CLK is set to VENC CLK itself without gating). This horizontal sync timing can be advanced by OSDHADV.OHAD. The assertion timing can be 0 to 127 VENC CLK ahead of the original timing. This feature is useful when OSD does not have enough margin to prepare the first data in specified BASEP_X value due to SDRAM bandwidth limitation. In such a case, if the user advances the OSD horizontal sync, it will relax the latency for OSD to prepare the first data. Figure 107 shows the OSD horizontal sync advanced feature.

Note that OSD sync signals are low active.

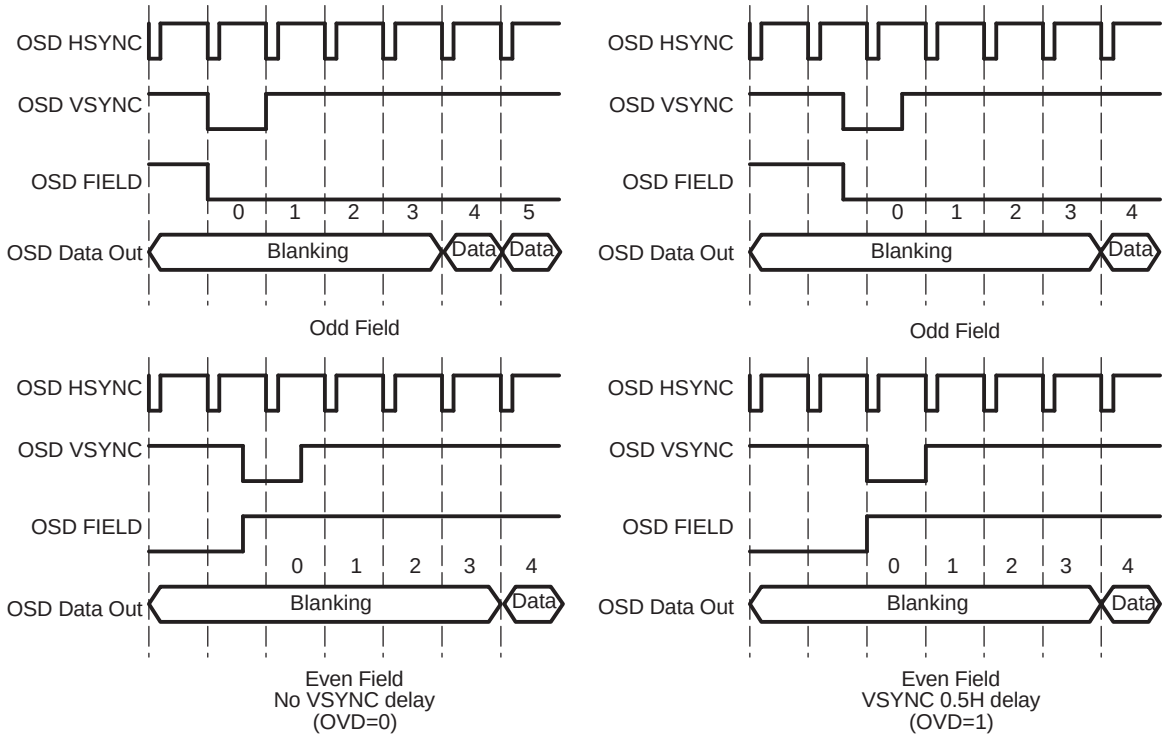
Figure 107. Advanced OSD HSYNC



4.5.5.3.2 0.5H Delay Vertical Sync

The vertical sync assertion for OSD can be delayed 0.5H by setting SYNCCTL.OVD to 1. This can modify the OSD data start line in odd field. The difference is shown in Figure 108. For PAL, OVD is automatically set to 1.

Figure 108. OSD VSYNC 0.5H Delay



4.5.5.4 Field ID Monitor

The current field ID status can be read from VSTAT.FIDST. The field status that can be seen from this bit is the field ID provided to the OSD module.

4.5.5.5 Interrupt

VENC asserts an interrupt at every VSYNC assertion. When the OSD module receives a vertical sync pulse from VENC, it updates its internal configuration registers. The interrupt assertion immediately follows this register update.

4.5.5.6 I/O Control

When VIOCTL.YCDC is 1, the specified level in YLVL, CLVL in the register, YCOLVL can be directly output onto YOUT and COUT pins. It is necessary to set the direction of YOUT and COUT to output by setting VIOCTL.YCDIR. YCDIR affects YOUT and COUT.

The direction of sync signals is controlled by SYNCCTL.SYDIR. This bit affects HSYNC, VSYNC and LCD_FIELD (if GIOx is configured as LCD_FIELD).

4.5.5.7 Gamma Correction RAM Table

The LCD controller has 128 x 16 bits of RAM. This RAM is used for the gamma correction of the digital LCD output. The RAM can be easily accessed through the ARM register, RAMADR(0x3145E) and

RAMPORT(0x31460). You specify the target RAM address (0-63) to the RAMADR register, then access the RAMPORT register. Reading it returns the contents of the specified RAM address. Writing to it overwrites the specified RAM address with the written data. Since the RAMADR is automatically incremented by accessing the RAMPORT, you do not have to update the address for every access. The RAM contents are initialized to 0 at the reset.

The RAM acts as the lookup table which has 256 words of 8-bit data. Gamma correction is enabled by setting GAMON (bit 0, GAMCTL) to 1. The basic operation is that 8-bit RGB data is replaced with the 8-bit RGB data by the lookup table and all RGB components share one lookup table.

You may use a unique table for each RGB component. When GAMUQ (bit 1, GAMBTL) is 1, the lookup table is split into four regions which have 64 words, respectively, and the upper 6 bits of each RGB component is independently applied to its own lookup table. Since the input precision is reduced to 6 bits, this mode should be used in the application that only needs 6 bits of output precision even though the lookup table output is still 8 bits.

4.5.5.8 Clock Control

Individual clock enable/disable is provided for the gamma table, digital LCD controller, and analog video encoder in the CLKCTL register.

5 Programming Model

5.1 Setup for Typical Configuration

A typical configuration of the VPBE would be standard mode timing in master mode, which would support analog NTSC/PAL SDTV output via the integrated video DACs and also could support digital LCD display devices if they, in turn, supported standard mode timing.

5.2 Resetting the VPBE Subsystem

The entire VPSS subsystem (VPFE and VPBE) can be reset via the Power and Sleep Controller (PSC).

CAUTION

Do not reset the entire VPSS Master or VPSS Slave subsystem (VPFE and VPBE), via the Power Sleep Controller.

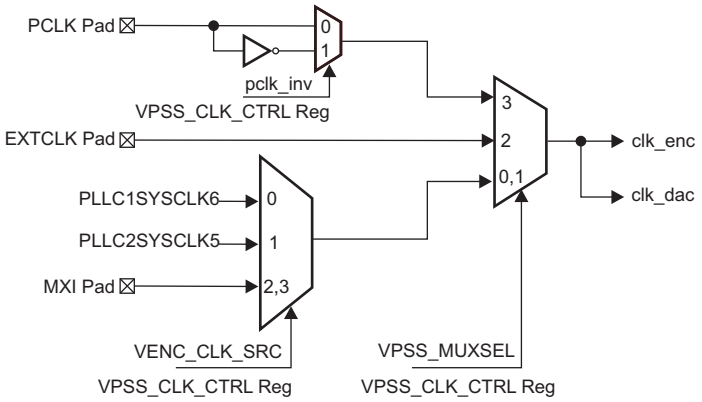
5.3 Configuring the Clocks and Control Signals

The VPBE/VENC clock must be configured for proper operation of the desired display mode. For more information, see Section 3.1.1.

5.3.1 VPBE Clock Source Selection

The VBPE clock can be selected from five different sources. Note that MXI2 is powered off by default.

Figure 109. VPBE/DAC Clocking Options



5.4 Programming the On-Screen Display (OSD)

This section discusses issues related to the software control of the on-screen display (OSD) module. It lists registers that are required to be programmed in different modes and how to enable and disable OSD window displays. Additionally, it discusses the different register access types, and enumerates several programming constraints.

5.4.1 Hardware Setup/Initialization

This section discusses how the OSD must be configured before the module can be used. Also, note that the VENC module must also be configured before any display output is produced by the device.

5.4.1.1 Reset Behavior

Upon hardware reset of the VPSS, all of the registers in the OSD are initialized to their reset values. However, since the OSD RAM CLUT is stored in internal RAM, its content does not have reset values. After reset, the contents of these tables are unknown.

5.4.1.2 Hardware Setup

Prior to enabling the OSD, the hardware must be properly configured via register writes. Table 82 identifies the register parameters that must be programmed before enabling the OSD. Note that the default settings may be appropriate values so explicit register write may not be needed to all indicated registers/fields.

Table 82. OSD Hardware Setup

Function	Configuration Required	Description
Global Configuration	MODE.CS	CB/CY order
	MODE.FSINV	Field signal inverse
	MODE.VVRSZ	Video window vertical 6/5 resize
	MODE.VHRSZ	Video window horizontal 9/8 resize
	MODE.OVRSZ	Bitmap window vertical 6/5 resize
	MODE.OHRSZ	Bitmap window horizontal 9/8 resize
Background color	MODE.BCLUT	Background CLUT (ROM/RAM)
	MODE.CABG	Background color
OSD display frame	BASEPX	Base pixel X
	BASEPY	Base pixel Y
ROM CLUT	MISCCTL.RSEL	ROM CLUT selection

Table 82. OSD Hardware Setup (continued)

Function	Configuration Required	Description
Transparency	TRANSPVALL.RGBL	RGB Transparency value (Low 16)
	TRANSPVALU.RGBU	RGB Transparency value (High 8)
	TRANSPVALU.Y	Luma Transparency
	TRANSPBMPIDX.BMP0	Bitmap Transparency (Window 0)
	TRANSPBMPIDX.BMP1	Bitmap Transparency (Window 1)

5.4.2 Color LookUp Table Setup

The user-defined RAM Color Look-Up Table (CLUT) must be programmed before it can be used. For additional details, see Section 4.4.4.1.

5.4.2.1 Window Setup

Before an individual window can be displayed, appropriate data must be made available in DDR2/mDDR, along with the appropriate window settings. The data formats are described above and the window configuration settings are described in Table 83.

Table 83. OSD Window Configuration

Function	Configuration Options
All Windows	Position offset relative to BASEPX/Y
	Window display size
	DDR2/mDDR data pointer
	DDR2/mDDR Offset (size in 32-byte increments of each data line)
	Field/Frame settings
	Horizontal/vertical Zoom factor
Video Windows	Expansion filter coefficient settings
Bitmap Windows	YUV attenuation enable
	RGB565 display mode (one window only)
	CLUT selection (ROM/RAM)
	Bitmap data width (1, 2, 4, or 8)
	CLUT mapping if bit depth < 8-bits
	Blend factor
	Transparency enable
	Transparent color value (global for RGB and YUV)
Attribute Window	Blinking (ON/OFF)
	Blink Rate
Cursor Window	Size
	Thickness
	Color

5.4.3 Enable/Disable Hardware

The OSD has no separate hardware enable/disable but each window has a separate display enable/disable (see Table 84).

Table 84. OSD Window Enable/Disable

Window	Display Enable
Video Window 0	VIDWINMD.ACT0
Video Window 0	VIDWINMD.ACT1
Bitmap Window 0	OSDWIN0MD.OACT0

Table 84. OSD Window Enable/Disable (continued)

Window	Display Enable
Bitmap Window 1	OSDWIN1MD.OACT1
Attribute Window	None - always active when in attribute mode
Cursor Window	RECTCUR.RCACT

5.4.4 Events and Status Checking

The VPBE generates a frame sync interrupt. This can be used as a trigger to update any frame-dependent registers. The OSD generates no events or status other than the indicator that a CLUT write is pending.

5.4.5 Register Accessibility During Frame Display

Some registers/fields are shadowed during the frame display time and any writes to these locations are not applied until the next frame field. These are highlighted in Table 85.

Table 85. OSD Window Registers/Field Shadowing

Register.Field	Description
MODE.CS	Cb/Cr or Cr/Cb Format
MODE.OVRSZ	OSD Window Vertical Expansion Enable
MODE.OHRSZ	OSD Window Horizontal Expansion Enable
MODE.EF(1)	Expansion Filter Enable
MODE.VVRSZ(1)	Video Window Vertical Expansion Enable
MODE.VHRSZ(1)	Video Window Horizontal Expansion Enable
MODE.FSINV(1)	Field Signal Inversion
MODE.BCLUT(1)	Background CLUT Selection
MODE.CABG	Background Color CLUT
VIDWINMD.VFINV	Video Window 0/1 Expansion Filter Coefficient Inverse
VIDWINMD.V1EFC	Video Window 1 Expansion Filter Coefficient
VIDWINMD.VHZ1(1)	Video Window 1 Horizontal Direction Zoom
VIDWINMD.VVZ1(1)	Video Window 1 Vertical Direction Zoom
VIDWINMD.VFF1(1)	Video Window 1 Display Mode
VIDWINMD.ACT1(1)	Sets Image Display On/Off Video Window 1
VIDWINMD.V0EFC	Video Window 0 Expansion Filter Coefficient
VIDWINMD.VHZ0(1)	Video Window 0 Horizontal Direction Zoom
VIDWINMD.VVZ0(1)	Video Window 0 Vertical Direction Zoom
VIDWINMD.VFF0(1)	Video Window 0 Display Mode
VIDWINMD.ACT0(1)	Sets Image Display On/Off Video Window 0
OSDWINOMD.BMPOMD	Bitmap Input Mode
OSDWIN0MD.CLUTS0(1)	CLUT Select for OSD Window 0
OSDWIN0MD.OHZ0(1)	OSD Window 0 Horizontal Zoom
OSDWIN0MD.OVZ0(1)	OSD Window 0 Vertical Zoom
OSDWIN0MD.BMW0(1)	Bitmap Bit Width for OSD Window 0
OSDWIN0MD.BLND0(1)	Blending Ratio for OSD Window 0
OSDWIN0MD.TE0(1)	Transparency Enable for OSD Window 0
OSDWIN0MD.OFF0(1)	OSD Window 0 Display Mode
OSDWIN0MD.OACT0(1)	OSD Window 0 Active (displayed)
OSDWIN1MD.OASW(1)	OSD Window 1 Attribute Mode Enable
OSDWIN1MD.BMP1MD	Bitmap Input Mode

(1) This register/field is shadowed during the frame display time and any writes to this location is not applied until the next frame field.

Table 85. OSD Window Registers/Field Shadowing (continued)

Register.Field	Description
OSDWIN1MD.CLUTS1	CLUT Select for OSD Window 1
OSDWIN1MD.OHZ1[1]	OSD Window 1 Horizontal Zoom
OSDWIN1MD.OVZ1[1]	OSD Window 1 Vertical Zoom
OSDWIN1MD.BMW1[1]	Bitmap Bit Width for OSD Window 1
OSDWIN1MD.BLND1[1]	Blending Ratio for OSD Window 1
OSDWIN1MD.TE1[1]	Transparency Enable for OSD Window 1
OSDWIN1MD.OFF1[1]	OSD Window 1 Display Mode
OSDWIN1MD.OACT1[1]	OSD Window 1 Active (displayed)
OSDATRMD.OASW[1]	OSD Window 1 Attribute Mode Enable
OSDATRMD.OHZA[1]	OSD Attribute Window Horizontal Zoom
OSDATRMD.OVZA[1]	OSD Attribute Window Vertical Zoom
OSDATRMD.BLNKINT[1]	Blinking Interval
OSDATRMD.OFFA[1]	OSD Attribute Window Display Mode
OSDATRMD.BLNK[1]	OSD Attribute Window Blink Enable
RECTCUR.RCAD	Rectangular Cursor Color Palette Address
RECTCUR.CLUTSR[2]	CLUT Select
RECTCUR.RCHW[2]	Rectangular Cursor Horizontal Line Width
RECTCUR.RCVW[2]	Rectangular Cursor Vertical Line Width
RECTCUR.RCACT[2]	Rectangular Cursor Active (displayed)
VIDWIN0OFST.V0LO[2]	Video Window 0 Line Offset
VIDWIN1OFST.V1LO[2]	Video Window 1 Line Offset
OSDWIN0OFST.O0LO[2]	OSD Window 0 Line Offset
OSDWIN1OFST.O1LO[2]	OSD Window 1 Line Offset
VIDWINADH.V1AH[2]	Video Window 1 SDRAM Source Address (High)
VIDWINADH.V0AH[2]	Video Window 0 SDRAM Source Address (High)
VIDWIN0ADL.VIDWIN0ADL[2]	Video Window 0 SDRAM Source Address (Low)
VIDWIN1ADL.VIDWIN1ADL[2]	Video Window 1 SDRAM Source Address (Low)
OSDWINADH.O1AH[2]	OSD Window 0 SDRAM Source Address (High)
OSDWINADH.O0AH[2]	OSD Window 1 SDRAM Source Address (High)
OSDWIN0ADL.OSDWIN0ADL[2]	OSD Window 0 SDRAM Source Address (Low)
OSDWIN1ADL.OSDWIN1ADL[2]	OSD Window 1 SDRAM Source Address (Low)
BASEPX.BPX[2]	Base Pixel in X
BASEPY.BPY[2]	Base Pixel(Line) in Y
VIDWIN0XP.V0X[2]	Video Window 0 X-Position
VIDWIN0YP.V0Y[2]	Video Window 0 Y-Position
VIDWIN0XL.V0W[2]	Video Window 0 X-Width
VIDWIN0YL.V0H[2]	Video Window 0 Y-Height
VIDWIN1XP.V1X[2]	Video Window 1 X-Position
VIDWIN1YP.V1Y[2]	Video Window 1 Y-Position
VIDWIN1XL.V1W[2]	Video Window 1 X-Width
VIDWIN1YL.V1H[2]	Video Window 1 Y-Height
OSDWIN0XP.W0X[2]	OSD Window 0 X-Position
OSDWIN0YP.W0Y[2]	OSD Window 0 Y-Position
OSDWIN0XL.W0W[2]	OSD Window 0 X-Width
OSDWIN0YL.W0H[2]	OSD Window 0 Y-Height
OSDWIN1XP.W1X[2]	OSD Window 1 X-Position

[2] This register/field is shadowed during the frame display time and any writes to this location is not applied until the next frame field.

Table 85. OSD Window Registers/Field Shadowing (continued)

Register.Field	Description
OSDWIN1YP.W1Y[2]	OSD Window 1 Y-Position
OSDWIN1XL.W1W[2]	OSD Window 1 X-Width
OSDWIN1YL.W1H[2]	OSD Window 1 Y-Height
CURXP.RCSX[2]	Rectangular Cursor Window X-Position
CURYP.RCSY[2]	Rectangular Cursor Window Y-Position
CURXL.RCSW[2]	Rectangular Cursor Window X-Width
CURYL.RCSH[2]	Rectangular Cursor Window Y-Height
W0BMP01.PAL01	Palette Address for Bitmap Value [1,x,x]-OSD Window 0
W0BMP01.PAL00	Palette Address for Bitmap Value [0,0,0]-OSD Window 0
W0BMP23.PAL03	Palette Address for Bitmap Value [3,x,x]-OSD Window 0
W0BMP23.PAL02	Palette Address for Bitmap Value [2,x,x]-OSD Window 0
W0BMP45.PAL05	Palette Address for Bitmap Value [5,1,x]-OSD Window 0
W0BMP45.PAL04	Palette Address for Bitmap Value [4,x,x]-OSD Window 0
W0BMP67.PAL07	Palette Address for Bitmap Value [7,x,x]-OSD Window 0
W0BMP67.PAL06	Palette Address for Bitmap Value [6,x,x]-OSD Window 0
W0BMP89.PAL09	Palette Address for Bitmap Value [9,x,x]-OSD Window 0
W0BMP89.PAL08	Palette Address for Bitmap Value [8,x,x]-OSD Window 0
W0BMPAB.PAL11	Palette Address for Bitmap Value [B,x,x]-OSD Window 0
W0BMPAB.PAL10	Palette Address for Bitmap Value [A,2,x]-OSD Window 0
W0BMPCD.PAL13	Palette Address for Bitmap Value [D,x,x]-OSD Window 0
W0BMPCD.PAL12	Palette Address for Bitmap Value [C,x,x]-OSD Window 0
W0BMPEF.PAL15	Palette Address for Bitmap Value [F,3,1]-OSD Window 0
W0BMPEF.PAL14	Palette Address for Bitmap Value [E,x,x]-OSD Window 0
W1BMP01.PAL01	Palette Address for Bitmap Value [1,x,x]-OSD Window 1
W1BMP01.PAL00	Palette Address for Bitmap Value [0,0,0]-OSD Window 1
W1BMP23.PAL03	Palette Address for Bitmap Value [3,x,x]-OSD Window 1
W1BMP23.PAL02	Palette Address for Bitmap Value [2,x,x]-OSD Window 1
W1BMP45.PAL05	Palette Address for Bitmap Value [5,1,x]-OSD Window 1
W1BMP45.PAL04	Palette Address for Bitmap Value [4,x,x]-OSD Window 1
W1BMP67.PAL07	Palette Address for Bitmap Value [7,x,x]-OSD Window 1
W1BMP67.PAL06	Palette Address for Bitmap Value [6,x,x]-OSD Window 1
W1BMP89.PAL09	Palette Address for Bitmap Value [9,x,x]-OSD Window 1
W1BMP89.PAL08	Palette Address for Bitmap Value [8,x,x]-OSD Window 1
W1BMPAB.PAL11	Palette Address for Bitmap Value [B,x,x]-OSD Window 1
W1BMPAB.PAL10	Palette Address for Bitmap Value [A,2,x]-OSD Window 1
W1BMPCD.PAL13	Palette Address for Bitmap Value [D,x,x]-OSD Window 1
W1BMPCD.PAL12	Palette Address for Bitmap Value [C,x,x]-OSD Window 1
W1BMPEF.PAL15	Palette Address for Bitmap Value [F,3,1]-OSD Window 1
W1BMPEF.PAL14	Palette Address for Bitmap Value [E,x,x]-OSD Window 1
VBNDRY.VFILINCMD	Vertical Filter Increment Mode
VBNDRY.VDNDRYPRCSEN	Video Boundary Processing Enable
EXTMODE.EXPMDSEL	Expansion Filtering Mode Select
EXTMODE.SCRNHEXP	Horizontal Expansion Mode
EXTMODE.SCRNVEXP	Vertical Expansion Mode
EXTMODE.OSD1BLDCHR	OSD Bitmap1 Blend Characteristics
EXTMODE.OSD0BLDCHR	OSD Bitmap0 Blend Characteristics
EXTMODE.ATNOSD1EN	Attenuation Enable for REC601 for OSD Bitmap 1

Table 85. OSD Window Registers/Field Shadowing (continued)

Register.Field	Description
EXTMODE.ATNOSD0EN	Attenuation Enable for REC601 for OSD Bitmap 0
EXTMODE.OSDHRSZ15	OSD Bitmap Window Horizontal 1.5x Expansion
EXTMODE.VIDHRSZ15	OSD Video Window Horizontal 1.5x Expansion
EXTMODE.ZMFILV1HEN	Video Window 1 Horizontal Zoom Filter
EXTMODE.ZMFILV1VEN	Video Window 1 Vertical Zoom Filter
EXTMODE.ZMFILV0HEN	Video Window 0 Horizontal Zoom Filter
EXTMODE.ZMFILV0VEN	Video Window 0 Vertical Zoom Filter
EXTMODE.EXPFILHEN	Horizontal Expansion Filter Enable
EXTMODE.EXPFILVEN	Vertical Expansion Filter Enable
MISCCTL.FIELD_ID	Indicates field being processed
MISCCTL.DMANG	DMA Status
MISCCTL.RSEL	CLUT ROM Selection
MISCCTL.CPBSY	CLUT Write Busy
RSV5.RSV5	Reserved
CLUTRAMYCB.Y	Write Data (Y) Into Built-In CLUT RAM
CLUTRAMYCB.CB	Write Data (Cb) Into Built-In CLUT RAM
CLUTRAMCR.CR	Write Data (Cr) Into Built-In CLUT RAM
CLUTRAMCR.CADDR	CLUT Write Pallette Address
TRANSPVALL.RGBL	RGB Transparency Value (Low)
TRANSPVALU.Y	Luma Transparency Value
TRANSPVALU.RGBH	RGB Transparency Value (High)
TRANSPBMPIDX.BMP1	OSD Bitmap Window 1 Transparent Value
TRANSPBMPIDX.BMP0	OSD Bitmap Window 0 Transparent Value

5.4.6 Summary of Constraints

The following restrictions exist in the OSD module.

- If the vertical resize filter is enabled for either of the video windows, the maximum horizontal window dimension cannot be greater than 1024 currently. This is due to the limitation in the size of the line memory.
- It is not possible to use both of the CLUT ROMs at the same time. However, a window can use RAM while another chooses ROM.

5.5 Programming the VENC

This section discusses issues related to the software control of the Video Encoder/Digital LCD Controller module (VENC). It lists registers that are required to be programmed in different modes and how to enable and disable the VENC. It also discusses the different register access types and enumerates several programming constraints.

5.5.1 Hardware Setup/Initialization

This section discusses the configuration of the VENC required before the module can be used. Also, the OSD module must be configured before any display output is produced by the device.

5.5.1.1 Reset Behavior

Upon hardware reset of the VPSS, all of the registers in the VENC are returned to their reset values and all the memory values in the internal RAM of gamma correction table are zero (reset value is zero). If the reset is a chip-level power-on reset (reset after power is applied), then the contents of this table is returned to zero. Same way, if the reset is a VPSS module reset (when power remains active) then the contents of the Gamma RAM Table cleared to zero.

5.5.1.2 Hardware Setup

Prior to enabling the VENC, the hardware must be properly configured via register writes. Essentially all of the VENC programming is related to hardware setup and little to no interaction is required once the desired display operating condition is set. Table 86 shows which register/field affects the available display modes.

The analog output is only available in standard (NTSC/PAL/525p/625p/720p/1080i) timing mode, but the digital outputs are available in either mode. Therefore, if the digital display device supports standard mode timing, the analog and digital outputs can be available simultaneously, if desired.

Table 86. VPBE Global Registers for Hardware Setup[1]

Register.Field	Description	Analog TV	YCC16	YCC8	Parallel RGB	Serial RGB
VMOD.VDMD	Digital Video Output Mode	Sets mode				
VMOD.ITLCL	Non-Interlace Line Number Select	O	O	O	O	O
VMOD.ITLC	Interlaced Scan Mode Enable	O	O	O	O	O
VMOD.NSIT	Nonstandard Interlace Mode		O	O	O	O
VMOD.TVTYP	TV Format Type Select	Sets mode				
VMOD.SLAVE	Master-Slave Select					
VMOD.VMD	Video Timing	Standard	Standard or Non-Standard			
VMOD.BLNK	Blanking Enable	O				
VMOD.VIE	Composite Analog Output Enable	O				
VMOD.VENC	Video Encoder Enable	R				
VIOCTL.VCLKP	VCLK Output Polarity		O	O	O	O
VIOCTL.VCLKE	VCLK Output Enable		R	R	R	R
VIOCTL.VCLKZ	VCLK Pin Output Enable		R	R	R	R
VIOCTL.SYDIR	Horizontal/Vertical Sync Pin I/O Control		Enable in Master mode			
VIOCTL.DOMD	Digital Data Output Mode		R	R	R	R
VIOCTL.YCSWAP	Swaps YOUT/COUT Pins		O	O		
VIOCTL.YCOL	YOUT/COUT Pin Output Level		O	O		
VIOCTL.YCOMD	YOUT/COUT Pin Output Mode (N/A)		N/A	N/A		
VIOCTL.YCDIR	YOUT/COUT Pin Direction (N/Z)		N/A	N/A		
VDPRO.PFLTC	C Prefilter Select		O	O		
VDPRO.PFLTY	Y Prefilter Select		O	O		
VDPRO.PFLTR	Prefilter Sampling Frequency		O	O		
VDPRO.CBTYP	Color Bar Type	O				
VDPRO.CBMD	Color Bar Mode	O				
VDPRO.ATRGB	Input Video Attenuation Control for RGB				O	O
VDPRO.ATYCC	Input Video Attenuation Control for YCbCr		O	O		
VDPRO.ATCOM	Input Video Attenuation Control for Composite	O				
VDPRO.CUPS	C Signal Up-Sampling Enable	O				
VDPRO.YUPS	Y Signal Up-Sampling Enable	O				
SYNCCTL.OVD	OSD Vsync Delay	O				
SYNCCTL.EXFMD	External Field Detection Mode		SL	SL	SL	SL
SYNCCTL.EXFIV	External Field Input Inversion		SL	SL	SL	SL
SYNCCTL.EXSYNC	External Sync Select		SL	SL	SL	SL
SYNCCTL.EXVIV	External Vertical Sync Input Polarity		SL	SL	SL	SL
SYNCCTL.EXHIV	External Horizontal Sync Input Polarity		SL	SL	SL	SL
SYNCCTL.CSP	Composite Signal Output Polarity		SL	SL	SL	SL
SYNCCTL.CSE	Composite Signal Output Enable		SL	SL	SL	SL
SYNCCTL.SYSW	Output Sync Select		SL	SL	SL	SL
SYNCCTL.VSYNCS	Vertical Sync Output Signal		SL	SL	SL	SL
SYNCCTL.VPL	Vertical Sync Output Polarity		SL	SL	SL	SL
SYNCCTL.HPL	Horizontal Sync Output Polarity		SL	SL	SL	SL
SYNCCTL.SYEV	Vertical Sync Output Enable		SL	SL	SL	SL
SYNCCTL.SYEH	Horizontal Sync Output Enable		SL	SL	SL	SL
HSPLS.HSPLS	Horizontal Sync Pulse Width (number of ENC clocks)	M	M	M	M	M

(1) R = Required, O = Optional, M = Master Mode, SL = Slave Mode, r = Read-Only Status

Table 86. VPBE Global Registers for Hardware Setup[(1)] (continued)

Register.Field	Description	Analog TV	YCC16	YCC8	Parallel RGB	Serial RGB
VSPLS.VSPLS	Vertical Sync Pulse Width (number of ENC clocks)	M	M	M	M	M
HINT.HINT	Horizontal Interval (number of ENC clocks)	M	M	M	M	M
HSTART.HSTART	Horizontal Valid Data Start Position	M	M	M	M	M
HVALID.HVALID	Horizontal Data Valid Range	M	M	M	M	M
VINTVL.VINT	Vertical Interval (number of lines)	M	M	M	M	M
VSTART.VSTART	Vertical Valid Data Start Position	M	M	M	M	M
VVALID.VVALID	Vertical Data Valid Range	M	M	M	M	M
HSDLY.HSDLY	Output Delay of Horizontal Sync Signal	M	M	M	M	M
VSDLY.VSDLY	Output Delay of Vertical Sync Signal	M	M	M	M	M
YCCCTL.CHM	Chroma Output Mode		O	O		
YCCCTL.YCP	YC Output Order		O	O		
YCCCTL.R656	REC656 Mode (Standard Mode timing only)			O		
RGBCTL.RGBLAT	RGB Latch Setting				O	O
RGBCTL.IRSWP	Swap Order of data output in IronMan mode					O
RGBCTL.IR9	IronMan 9-bit mode					O
RGBCTL.IRONM	IronMan Type RGB output					O
RGBCTL.DFLTR	RGB LPF Sampling Frequency				O	O
RGBCTL.DFLTS	RGB LPF Select				O	O
RGBCTL.RGBEF	RGB Output Order (Line id=1)					O
RGBCTL.RGBOF	RGB Output Order (Line id=0)					O
RGBCLP.UCLIP	Upper Clip Level for RGB Output				O	O
RGBCLP.OFST	Offset Level for RGB Output				O	O
LINECTL.VSTF	Vertical Data Valid Start Position Field Mode					
LINECTL.VCLID	Vertical Culling Line Position					
LINECTL.VCLRD	Vertical Culling Counter Reset Mode					
LINECTL.VCL56	Digital Output Vertical Culling					
LINECTL.HLDF	Digital Output Field Hold					
LINECTL.HLDL	Digital Output Line Hold					
LINECTL.LINID	Start Line ID Control in Even Field					
LINECTL.DCKCLP	DCLK Pattern Switching by Culling Line ID					
LINECTL.DCKCLI	DCLK Polarity Inversion by Culling Line ID					
LINECTL.RGBCL	RGB Output Order Switching by Culling Line ID					
CULLLINE.CLOF	Culling Line ID Toggle Position (Odd field)					
CULLLINE.CLEF	Culling Line ID Toggle Position (Even field)					
CULLLINE.CULI	Culling Line ID Inversion Interval					
LCDOUT.OES	Output Enable Signal Selection				O	O
LCDOUT.FIDP	Field ID Output Polarity				O	O
LCDOUT.PWMP	PWM Output Pulse Polarity				O	O
LCDOUT.PWME	PWM Output Control				O	O
LCDOUT.ACE	LCD_AC Output Control				O	O
LCDOUT.BRP	BRIGHT Output Polarity				O	O
LCDOUT.BRE	BRIGHT Output Control				O	O
LCDOUT.OEP	LCD_OE Output Polarity		O	O	O	O
LCDOUT.OEE	LCD_OE Output Control		O	O	O	O

Table 86. VPBE Global Registers for Hardware Setup[(1)] (continued)

Register.Field	Description	Analog TV	YCC16	YCC8	Parallel RGB	Serial RGB
BRTS.BRTS	BRIGHT Pulse Start Position				O	O
BRTW.BRTW	BRIGHT Pulse Width				O	O
ACCTL.ACTF	LCD_AC Toggle Interval				O	O
ACCTL.ACTH	LCD_AC Toggle Horizontal Position				O	O
PWMP.PWMP	PWM Output Period				O	O
PWMW.PWMW	PWM Output Pulse Width				O	O
DCLKCTL.DCKIM	DCLK Internal Mode					
DCLKCTL.DOFST	DCLK Output Offset					
DCLKCTL.DCKEC	DCLK Pattern Mode				R	R
DCLKCTL.DCKME	DCLK Mask Control					
DCLKCTL.DCKOH	DCLK Output Divide					
DCLKCTL.DCKIH	Internal DCLK Output Divide					
DCLKCTL.DCKPW	DCLK Pattern Valid Bit Width				R	R
DCLKPTN0.DCPTN0	DCLK Pattern				R	R
DCLKPTN1.DCPTN1	DCLK Pattern				R	R
DCLKPTN2.DCPTN2	DCLK Pattern				R	R
DCLKPTN3.DCPTN3	DCLK Pattern				R	R
DCLKPTN0A.DCPTN0A	DCLK Pattern (auxiliary)					
DCLKPTN1A.DCPTN1A	DCLK Pattern (auxiliary)					
DCLKPTN2A.DCPTN2A	DCLK Pattern (auxiliary)					
DCLKPTN3A.DCPTN3A	DCLK Pattern (auxiliary)					
DCLKHS.DCHS	Horizontal DCLK Mask Start Position					
DCLKHSA.DCHS	Horizontal DCLK (auxiliary) Mask Start Position					
DCLKHR.DCHR	Horizontal DCLK Mask Range					
DCLKVS.DCVS	DCLK Vertical Mask Start Position					
DCLKVR.DCVR	DCLK Vertical Mask Range					
CAPCTL.CADF	Closed Caption Default Data Register	O				
CAPCTL.CAPF	Closed Caption Field Select	O				
CAPDO.CADO0	Closed Caption Default Data0 (odd field)	O				
CAPDO.CADO1	Closed Caption Default Data1 (odd field)	O				
CAPDE.CADE0	Closed Caption Default Data0 (even field)	O				
CAPDE.CADE1	Closed Caption Default Data1 (even field)	O				
ATR0.ATR0	Video Attribute Data Register 0	O				
ATR1.ATR1	Video Attribute Data Register 1	O				
ATR2.ATR2	Video Attribute Data Register 2	O				
VSTAT.CAEST	Closed Caption Status (even field)	r				
VSTAT.CAOST	Closed Caption Status (odd field)	r				
VSTAT.FIDST	Field ID Monitor	r	r	r	r	r
RAMADR.RAMADR	Gamma Correction Table RAM address					
RAMPORT.RAMPORT	RAM Data Port					
DACTST.DAPD0	DAC0 Power-Down	O				
DACTST.DACDC	DC Output mode	O				
DACTST.DALVL	DC DC Level control	O				
YCOLVL.YLVL	YOUT DC Level		O	O		
YCOLVL.CLVL	COUT DC Level		O	O		
SCPROG.SCSD	Sub-Carrier Initial Phase Value	O				

Table 86. VPBE Global Registers for Hardware Setup[1] (continued)

Register.Field	Description	Analog TV	YCC16	YCC8	Parallel RGB	Serial RGB
CVBS.YCDLY	Delay Adjustment of Y Signal in Composite Signal	O				
CVBS.CVLVL	Composite Video Level (sync/white)	O				
CVBS.CSTUP	Setup Level at NTSC Output	O				
CVBS.CBLS	Blanking Shape Disable	O				
CVBS.CBBLD	Blanking Build-Up Time for Composite Output	O				
CVBS.CSBLD	Sync Build-Up Time for Composite Output	O				
ETMG0.CEPW	Equalizing Pulse Width Offset for Composite	O				
ETMG0.CFSW	Field Sync Pulse Width Offset for Composite	O				
ETMG0.CLSW	Line Sync Pulse Width Offset for Composite	O				
ETMG1.CBSE	Burst End Position Offset for Composite	O				
ETMG1.CBST	Burst Start Position Offset for Composite	O				
ETMG1.CFPW	Front Porch Position Offset for Composite	O				
ETMG1.CLBI	Line Blanking End Pos. offset for composite	O				
DRGBX0.DGY	YCbCr→RGB Coefficient GY for Digital RGB				R	R
DRGBX1.DRV	YCbCr→RGB Coefficient RV for Digital RGB				R	R
DRGBX2.DGU	YCbCr→RGB Coefficient GU for Digital RGB				R	R
DRGBX3.DGV	YCbCr→RGB Cefficient GV for Digital RGB				R	R
DRGBX4.DBU	YCbCr→RGB Coefficient BU for Digital RGB				R	R
VSTARTA.VSTARTA	Vertical Data Valid Start Position for Even Field					
OSDCLK0.OCPW	OSD Clock Pattern Bit Width					
OSDCLK1.OCPT	OSD Clock Pattern					
HVLDCL0.HCM	Horizontal Valid Culling Mode					
HVLDCL0.HCPW	Horizontal Valid Culling Pattern Bit Width					
HVLDCL1.HCPT	Horizontal Culling Pattern					
OSDHADV.OHAD	OSD Horizontal Sync Advance					
CLKCTL.CLKGAM	Clock Enable for Gamma Correction Table					
CLKCTL.CLKDIG	Clock Enable for Digital LCD Controller					
CLKCTL.CLKENC	Clock Enable for Video Encoder					
CLKCTL.GAMON	Enable Gamma Correction					

5.5.1.3 *Gamma Table Setup*

The user-defined Gamma RAM table must be programmed before it can be used.

5.5.2 Enable/Disable Hardware

The VENC has several module enables as described in Table 87.

Table 87. OSD Window Enable/Disable

Module	Display Enable
VPBE	VPBE.CLK_OFF
VENC	VMOD.VIE
Composite Analog Out	VMOD.VIE, CLKCTL.CLKENC
Digital Output	VIOCTL.DOMD, CLKCTL.CLKDIG

5.5.3 Events and Status Checking

The VENC frame sync generates an interrupt. This is useful primarily for OSD operation.

6 VPBE Registers

The following sub-modules below are associated with the VPBE subsystem. Few common registers between VPBE and VPFE are explained in the VPFE user guide. For details of these registers refer to *TMS320DM36x Digital Media System-on-Chip (DMSoC) Video Processing Front End (VPFE) Users Guide* (SPRUFG8) .

Table 88. VPBE Module Register Map

Address	Peripheral	Description
0x01C7:0200	VPBE_CLK_CTRL	VPBE Clock Control
0x01C7:1C00	OSD	VPBE On-Screen Display
0x01C7:1E00	VENC	VPBE Video Encoder

6.1 VPBE Clock Control Register

For details of VPBE Clock Control Register refer to *TMS320DM36x Digital Media System-on-Chip (DMSoC) Video Processing Front End (VPFE) Users Guide* (SPRUFG8) .

6.2 On-Screen Display (OSD) Registers

Table 89 lists the memory-mapped registers for the on-screen display (OSD). For the memory address of these registers, see the device-specific data manual.

Table 89. On-Screen Display (OSD) Registers

Offset	Acronym	Register Description	Section
0h	MODE	OSD Mode Setup	Section 6.2.1
4h	VIDWINMD	Video Window Mode Setup	Section 6.2.2
8h	OSDWIN0MD	Bitmap Window 0 Mode Setup	Section 6.2.3
Ch	OSDWIN1MD	OSD Window 1 Mode Setup (when used as a second OSD window)	Section 6.2.4
Ch	OSDATRMD	OSD Attribute Window Mode Setup (when used as an attribute window)	Section 6.2.5
10h	RECTCUR	Rectangular Cursor Setup	Section 6.2.6
14h	RSV0	Reserved	Section 6.2.7
18h	VIDWIN0OFST	Video Window 0 Offset	Section 6.2.8
1Ch	VIDWIN1OFST	Video Window 1 Offset	Section 6.2.9
20h	OSDWIN0OFST	Bitmap Window 0 Offset	Section 6.2.10
24h	OSDWIN1OFST	Bitmap Window 1/Attribute Window Offset	Section 6.2.11
28h	VIDWINADH	Video Window 0/1 Address - High	Section 6.2.12
2Ch	VIDWIN0ADL	Video Window 0 Address - Low	Section 6.2.13
30h	VIDWIN1ADL	Video Window 1 Address - Low	Section 6.2.14
34h	OSDWINADH	BMP Window 0/1 Address - High	Section 6.2.15
38h	OSDWIN0ADL	BMP Window 0 Address - Low	Section 6.2.16
3Ch	OSDWIN1ADL	Bitmap Window 1/Attribute Address - Low	Section 6.2.17
40h	BASEPX	Base Pixel X	Section 6.2.18
44h	BASEPY	Base Pixel Y	Section 6.2.19
48h	VIDWIN0XP	Video Window 0 X-Position	Section 6.2.20
4Ch	VIDWIN0YP	Video Window 0 Y-Position	Section 6.2.21
50h	VIDWIN0XL	Video Window 0 X-Size	Section 6.2.22
54h	VIDWIN0YL	Video Window 0 Y-Size	Section 6.2.23
58h	VIDWIN1XP	Video Window 1 X-Position	Section 6.2.24
5Ch	VIDWIN1YP	Video Window 1 Y-Position	Section 6.2.25
60h	VIDWIN1XL	Video Window 1 X-Size	Section 6.2.26
64h	VIDWIN1YL	Video Window 1 Y-Size	Section 6.2.27
68h	OSDWIN0XP	Bitmap Window 0 X-Position	Section 6.2.28
6Ch	OSDWIN0YP	Bitmap Window 0 Y-Position	Section 6.2.29
70h	OSDWIN0XL	Bitmap Window 0 X-Size	Section 6.2.30
74h	OSDWIN0YL	Bitmap Window 0 Y-Size	Section 6.2.31
78h	OSDWIN1XP	Bitmap Window 1 X-Position	Section 6.2.32
7Ch	OSDWIN1YP	Bitmap Window 1 Y-Position	Section 6.2.33
80h	OSDWIN1XL	Bitmap Window 1 X-Size	Section 6.2.34
84h	OSDWIN1YL	Bitmap Window 1 Y-Size	Section 6.2.35
88h	CURXP	Rectangular Cursor Window X-Position	Section 6.2.36
8Ch	CURYP	Rectangular Cursor Window Y-Position	Section 6.2.37
90h	CURXL	Rectangular Cursor Window X-Size	Section 6.2.38
94h	CURYL	Rectangular Cursor Window Y-Size	Section 6.2.39
98h	RSV1	Reserved	Section 6.2.40
9Ch	RSV2	Reserved	Section 6.2.41
A0h	W0BMP01	Window 0 Bitmap Value to Palette Map 0/1	Section 6.2.42

Table 89. On-Screen Display (OSD) Registers (continued)

Offset	Acronym	Register Description	Section
A4h	W0BMP23	Window 0 Bitmap Value to Palette Map 2/3	Section 6.2.43
A8h	W0BMP45	Window 0 Bitmap Value to Palette Map 4/5	Section 6.2.44
ACh	W0BMP67	Window 0 Bitmap Value to Palette Map 6/7	Section 6.2.45
B0h	W0BMP89	Window 0 Bitmap Value to Palette Map 8/9	Section 6.2.46
B4h	W0BMPAB	Window 0 Bitmap Value to Palette Map A/B	Section 6.2.47
B8h	W0BMPCD	Window 0 Bitmap Value to Palette Map C/D	Section 6.2.48
BCh	W0BMPEF	Window 0 Bitmap Value to Palette Map E/F	Section 6.2.49
C0h	W1BMP01	Window 1 Bitmap Value to Palette Map 0/1	Section 6.2.50
C4h	W1BMP23	Window 1 Bitmap Value to Palette Map 2/3	Section 6.2.51
C8h	W1BMP45	Window 1 Bitmap Value to Palette Map 4/5	Section 6.2.52
CCh	W1BMP67	Window 1 Bitmap Value to Palette Map 6/7	Section 6.2.53
D0h	W1BMP89	Window 1 Bitmap Value to Palette Map 8/9	Section 6.2.54
D4h	W1BMPAB	Window 1 Bitmap Value to Palette Map A/B	Section 6.2.55
D8h	W1BMPCD	Window 1 Bitmap Value to Palette Map C/D	Section 6.2.56
DCh	W1BMPEF	Window 1 Bitmap Value to Palette Map E/F	Section 6.2.57
E0h	VBNDRY	Test Mode	Section 6.2.58
E4h	EXTMODE	Extended Mode	Section 6.2.59
E8h	MISCCTL	Miscellaneous Control	Section 6.2.60
ECh	CLUTRAMYCB	CLUT RAM Y/Cb Setup	Section 6.2.61
F0h	CLUTRAMCR	CLUT RAM Cr/Mapping Setup	Section 6.2.62
F4h	TRANSPVALL	Transparent Color Code - Lower	Section 6.2.63
F8h	TRANSPVALU	Transparent Color Code - Upper	Section 6.2.64
FCh	TRANSPBMPIDX	Transparent Index Code for Bitmaps	Section 6.2.65

6.2.1 OSD Mode Setup (MODE)

The OSD mode setup register is shown in Figure 110 and described in Table 90.

Figure 110. OSD Mode Setup (MODE)

31															16
Reserved															
R-0															
15	14	13	12	11	10	9	8	7							0
CS	OVRSZ	OHRSZ	EF	VVRSZ	VHRSZ	FSINV	BCLUT	CABG							
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0							

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 90. OSD Mode Setup (MODE) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved
15	CS		Cb/Cr or Cr/Cb format.
		0	Cb/Cr
		1	Cr/Cb
14	OVRSZ		OSD window vertical expansion enable. When enabled, the bitmap window images are stretched by a factor of 6/5 in the vertical direction. Results in proper vertical sizing to display a normal VGA (640x480) image on a PAL television (720x576); i.e., 480 x 6/5=576 Note: This expansion only duplicates one line out of every 5 lines. Note: This setting is effective only when EXTMODE.EXPMDSEL = 0.
		0	x 1
		1	x 6/5
13	OHRSZ		OSD window horizontal expansion enable. When enabled, the bitmap window images are stretched by a factor of 9/8 in the horizontal direction. Results in proper horizontal sizing to display a normal VGA (640x480) image on a PAL/NTSC television (720); i.e., 640 x 9/8=720 Note: This expansion only merely duplicates one pixel of every 8 pixels. Note: This setting is effective only when EXTMODE.EXPMDSEL = 0.
		0	x 1
		1	x 9/8
12	EF		Expansion filter enable. When either VVRSZ (x6/5 vertical expansion) or VHRSZ (9/8 horizontal expansion) are enabled, this will enable different filter coefficients in place of the normal bilinear expansion coefficients to reduce flicker between fields. Otherwise, an anti-flicker filter is applied regardless of the vertical and horizontal zoom settings in VIDWINMD.VHZn and VIDWINMD.VHZn (i.e., even at x1 zoom). Note: If EXTMODE.EXPMDSEL = 1, then this bit must = 0 (disabled). This bit is latched by VD.
		0	Off
		1	On
11	VVRSZ		Video window vertical expansion enable. When enabled, the video window images are stretched by a factor of 6/5 in the vertical direction. Results in proper vertical sizing to display a normal VGA (640x480) image on a PAL television (720x576); i.e., 480 x 6/5=576 Note: Simple bilinear interpolation of luma is performed if MODE.EF = 1. Note: This setting is effective only when EXTMODE.EXPMDSEL = 0. This bit is latched by VD.
		0	x 1
		1	x 6/5
10	VHRSZ		Video window horizontal expansion enable. When enabled, the video window images are stretched by a factor of 9/8 in the horizontal direction. Results in proper horizontal sizing to display a normal VGA (640x480) image on an NTSC/PAL television (720x576); i.e., 640 x 9/8 = 720 Note: Simple bilinear interpolation of luma is performed if MODE.EF = 1 Note: This setting is effective only when EXTMODE.EXPMDSEL = 0. This bit is latched by VD.
		0	x 1
		1	x 9/8

Table 90. OSD Mode Setup (MODE) Field Descriptions (continued)

Bit	Field	Value	Description
9	FSINV		Field signal inversion. Controls polarity of the field ID signal from the video encoder. This bit is latched by VD.
		0	Un-inverted
		1	Inverted
8	BCLUT		Background CLUT selection. Selects color look-up table for background color display. This bit is latched by VD.
		0	ROM
		1	RAM
7-0	CABG	0-FFh	Background color (CLUT index). Specifies image display background color by CLUT address. This color is displayed in any part of the display region where a window is not displayed.

6.2.2 Video Window Mode Setup (VIDWINMD)

The video window mode setup register is shown in Figure 111 and described in Table 91.

Figure 111. Video Window Mode Setup (VIDWINMD)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
R-0															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VFINV	V1EFC	VHZ1		VVZ1		VFF1	ACT1	Rsvd	V0EFC	VHZ0		VVZ0		VFF0	ACT0
R/W-0	R/W-0	R/W-0		R/W-0		R/W-0	R/W-0	R-0	R/W-0	R/W-0		R/W-0		R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 91. Video Window Mode Setup (VIDWINMD) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved
15	VFINV		Video window 0/1 expansion filter coefficient invert. Inverts application of the two sets of expansion filter coefficients between field 0 and field 1. Note: Valid on Video Windows when VnEFC is set.
		0	Normal
		1	Inversed
14	V1EFC		Video window 1 expansion filter coefficient selection. Enables different anti-flicker coefficients for each field. Note: Valid when MODE.EF = 1.
		0	Same co-efficient for field-0 and field-1
		1	Different co-efficient for field-0 and field-1
13-12	VHZ1		Video window 1 horizontal zoom. This bit is latched by VD.
		0	x1
		1	x2
		2	x4
		3	Reserved (same as '00')
11-10	VVZ1		Video window 1 vertical zoom. This bit is latched by VD.
		0	x1
		1	x2
		2	x4
		3	Reserved (same as '00')
9	VFF1		Video window 1 display mode. Field Mode: Data in display memory is field data, or 1/2 the vertical height of the eventual window display. Each line is output twice (line doubled). Frame Mode: Data in display memory is frame data, or full vertical height of the eventual window display. Each line is output once. When Video Encoder set to Interlaced: ((VENC:VMOD.VMD = 0 AND VENC:VMOD.ITLC = 0) OR (VENC:VMOD.VMD = 1 AND VENC:VMOD.NSIT = 1)). Window Height: VIDWINnYL = 1/2 window height or the number of lines per field in the window. Field Mode: Display data is read twice, once for each field. Frame Mode: Every other line is read and output for each field. When Video Encoder set to Progressive: ((VENC:VMOD.VMD = 1 AND VENC:VMOD.ITLC = 1) OR (VENC:VMOD.VMD = 0 AND VENC:VMOD.NSIT = 0)). Window Height: VIDWINnYL = Full window height. Field Mode: Each line is read and output twice. Frame Mode: Each lie is read and output once. This bit is latched by VD.
		0	Field mode
		1	Frame mode
8	ACT1		Activates Display of Video Window 1. This bit is latched by VD.
		0	Off
		1	On

Table 91. Video Window Mode Setup (VIDWINMD) Field Descriptions (continued)

Bit	Field	Value	Description
7	Reserved	0	Reserved
6	V0EFC		Video window 1 expansion filter coefficient selection. Enables different anti-flicker coefficients for each field. Note: Valid when MODE.EF = 1.
		0	Same co-efficient for field-0 and field-1
		1	Different co-efficient for field-0 and field-1
5-4	VHZ0		Video window 0 horizontal zoom. This bit is latched by VD.
		0	x1
		1	x2
		2	x4
		3	Reserved (same as '00')
3-2	VVZ0		Video window 0 vertical zoom. This bit is latched by VD.
		0	x1
		1	x2
		2	x4
		3	Reserved (same as '00')
1	VFF0		Video window 0 display mode. Field Mode: Data in display memory is field data, or 1/2 the vertical height of the eventual window display. Each line is output twice (line doubled). Frame Mode: Data in display memory is frame data, or full vertical height of the eventual window display. Each line is output once. When Video Encoder set to Interlaced: ((VENC:VMOD.VMD = 0 AND VENC:VMOD.ITLC = 0) OR (VENC:VMOD.VMD = 1 AND VENC:VMOD.NSIT = 1)). Window Height: VIDWINnYL = 1/2 window height or the number of lines per field in the window. Field Mode: Display data is read twice, once for each field. Frame Mode: Every other line is read and output for each field. When Video Encoder set to Progressive: ((VENC:VMOD.VMD = 1 AND VENC:VMOD.ITLC = 1) OR (VENC:VMOD.VMD = 0 AND VENC:VMOD.NSIT = 0)). Window Height: VIDWINnYL = Full window height. Field Mode: Each line is read and output twice. Frame Mode: Each lie is read and output once. This bit is latched by VD
		0	Field mode
		1	Frame mode
0	ACT0		Activates display of video window 0. This bit is latched by VD.
		0	Off
		1	On

6.2.3 Bitmap Window 0 Mode Setup (OSDWIN0MD)

The bitmap window 0 mode setup register is shown in Figure 112 and described in Table 92.

Figure 112. Bitmap Window 0 Mode Setup (OSDWIN0MD)

31	16
Reserved	
R-0	

15	14 13	12	11 10	9 8	7 6	5 3	2	1	0
BMPMDE	BMP0MD	CLUTS0	OHZ0	OVZ0	BMW0	BLND0	TE0	OFF0	OACT0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 92. Bitmap Window 0 Mode Setup (OSDWIN0MD) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved
15	BMPMDE		Bitmap window mode enable. This register controls bitmap window to share bitmap window 1.
		0	Window 0 and window 1
		1	Window 0
14-13	BMP0MD		Bitmap input mode. YCbCr is calculated from the following equation when RGB data is input: Y = 0.2990*R + 0.5870*G + 0.1140*B Cb = -0.1687*R - 0.3313*G + 0.5000*B + Offset(128) Cr = 0.5000*R - 0.4187*G - 0.0813*B + Offset(128)
		00	Bitmap data input mode
		01	RGB data - 16 bit/pixel, RGB565 input mode
		10	RGB data - 24 bit/pixel, RGB888 + 8bpp extension data input mode
		11	YC data - YCbYCr, Video Window data input mode
12	CLUTS0		CLUT select. This bit is latched by VD.
		0	ROM-look-up table
		1	RAM-look-up table
11-10	OHZ0		OSD window 0 horizontal zoom. This bit is latched by VD.
		0	x1
		1	x2
		2	x4
		3	Reserved (same as '00')
9-8	OVZ0		OSD window 0 vertical zoom. This bit is latched by VD.
		0	x1
		1	x2
		2	x4
		3	Reserved (same as '00')
7-6	BMW0		Bitmap bit width for OSD window 0. This bit is latched by VD. Valid for bitmap input mode.
		0	1
		1	2
		2	4
		3	8

Table 92. Bitmap Window 0 Mode Setup (OSDWIN0MD) Field Descriptions (continued)

Bit	Field	Value	Description
5-3	BLND0		Blending ratio between OSD window 0 and video window(s). TE0 controls which pixels are blended. This bit is latched by VD.
		0	0 1
		1	1/8 7/8
		2	2/8 6/8
		3	3/8 5/8
		4	4/8 4/8
		5	5/8 3/8
		6	6/8 2/8
		7	1 0
2	TE0		Transparency enable for OSD window 0. Controls which pixels are blended according to TE0. When disabled, all pixels are blended. When enabled, blending is only performed for pixels whose value matches the transparency value specified below: • (BMP0MD = 00): TRANSPBMPIDX.BMP0 • (BMP0MD = 01): TRANSPVALL.RGBL • (BMP0MD = 10): TRANSPVALL.RGBL & TRANSPVALU.RGBU • (BMP0MD = 11): TRANSPVALL.Y (only luma value examined) The blending is done as per the BLND0 register configuration. This bit is latched by VD.
		0	Disable
		1	Enable
1	OFF0		OSD window 0 display mode. Field Mode: Data in display memory is field data, or 1/2 the vertical height of the eventual window display. Each line is output twice (line doubled). Frame Mode: Data in display memory is frame data, or full vertical height of the eventual window display. Each line is output once. When Video Encoder set to Interlaced: ((VENC:VMOD.VMD = 0 AND VENC:VMOD.ITLC = 0) OR (VENC:VMOD.VMD = 1 AND VENC:VMOD.NSIT = 1)). Window Height: OSDWINnYL = 1/2 window height or the number of lines per field in the window. Field Mode: Display data is read twice, once for each field. Frame Mode: Every other line is read and output for each field. When Video Encoder set to Progressive: ((VENC:VMOD.VMD = 1 AND VENC:VMOD.ITLC = 1) OR (VENC:VMOD.VMD = 0 AND VENC:VMOD.NSIT = 0)). Window Height: OSDWINnYL = Full window height. Field Mode: Each line is read and output twice. Frame Mode: Each lie is read and output once. This bit is latched by VD
		0	Field mode
		1	Frame mode
0	OACT0		OSD Window0 Active (displayed). This bit is latched by VD
		0	Off
		1	On

6.2.4 Bitmap Window 1 Mode Setup (OSDWIN1MD)

The bitmap window 1 mode setup register is shown in Figure 113 and described in Table 93.

Figure 113. Bitmap Window 1 Mode Setup (OSDWIN1MD)

31	16
Reserved	
R-0	

15	14	13	12	11	10	9	8	7	6	5	3	2	1	0
OASW	BMP1MD		CLUTS1	OHZ1		OVZ1		BMW1		BLND1		TE1	OFF1	OACT1
R/W-0	R/W-0		R/W-0	R/W-0		R/W-0		R/W-0		R/W-0		R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 93. Bitmap Window 1 Mode Setup (OSDWIN1MD) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	ny writes to these bit(s) must always have a value of 0.
15	OASW		OSD window 1 attribute mode enable. This bit is latched by VD.
		0	OSD window 1
		1	Attribute window
14-13	BMP1MD		Bitmap input mode. YCbCr is calculated from the following equation when RGB data is input: Y = 0.2990*R + 0.5870*G + 0.1140*B Cb = -0.1687*R - 0.3313*G + 0.5000*B + Offset(128) Cr = 0.5000*R - 0.4187*G - 0.0813*B + Offset(128).
		00	Bitmap data input mode
		01	RGB data - 16 bit/pixel, RGB565 input mode
		10	RGB data - 24 bit/pixel, RGB888 + 8bpp extension data input mode
		11	YC data - YCbYCr, Video Window data input mode
12	CLUTS1		CLUT select. This bit is latched by VD.
		0	ROM-look-up table
		1	RAM-look-up table
11-10	OHZ1		OSD window 1 horizontal zoom. This bit is latched by VD.
		0	x1
		1	x2
		2	x4
		3	Reserved
9-8	OVZ1		OSD window1 vertical zoom. This bit is latched by VD.
		0	x1
		1	x2
		2	x4
		3	Reserved
7-6	BMW1		Bitmap bit width for OSD window 1. This bit is latched by VD. Valid for bitmap input mode.
		0	1-bit
		1	2-bits
		2	4-bits
		3	8-bits

Table 93. Bitmap Window 1 Mode Setup (OSDWIN1MD) Field Descriptions (continued)

Bit	Field	Value	Description
5-3	BLND1		Blending ratio between OSD window 1 and video window(s). TE0 controls which pixels are blended. This bit is latched by VD.
		0	0 1
		1	1/8 7/8
		2	2/8 6/8
		3	3/8 5/8
		4	4/8 4/8
		5	5/8 3/8
		6	6/8 2/8
		7	1 0
2	TE1		Transparency enable for OSD window 1. Controls which pixels are blended according to TE0. When disabled, all pixels are blended When enabled, blending is only performed for pixels whose value matches the transparency value specified below: • (BMP1MD = 00): TRANSPBMPIDX.BMP1 • (BMP1MD = 01): TRANSPVALL.RGBL • (BMP1MD = 10): TRANSPVALL.RGBL & TRANSPVALU.RGBU • (BMP1MD = 11): TRANSPVALL.Y (only luma value examined) The blending is done as per the BLND0 register configuration. This bit is latched by VD.
		0	Disable
		1	Enable
1	OFF1		OSD window 1 display mode. Field Mode: Data in display memory is field data, or 1/2 the vertical height of the eventual window display. Each line is output twice (line doubled). Frame Mode: Data in display memory is frame data, or full vertical height of the eventual window display. Each line is output once. When Video Encoder set to Interlaced: ((VENC:VMOD.VMD = 0 AND VENC:VMOD.ITLC = 0) OR (VENC:VMOD.VMD = 1 AND VENC:VMOD.NSIT = 1)). Window Height: OSDWINnYL = 1/2 window height or the number of lines per field in the window. Field Mode: Display data is read twice, once for each field. Frame Mode: Every other line is read and output for each field. When Video Encoder set to Progressive: ((VENC:VMOD.VMD = 1 AND VENC:VMOD.ITLC = 1) OR (VENC:VMOD.VMD = 0 AND VENC:VMOD.NSIT = 0)). Window Height: OSDWINnYL = Full window height. Field Mode: Each line is read and output twice. Frame Mode: Each lie is read and output once. This bit is latched by VD.
		0	Field mode
		1	Frame mode
0	OACT1		OSD window 1 active (displayed). This bit is latched by VD.
		0	Off
		1	On

6.2.5 OSD Attribute Window Mode Setup Register (OSDATRMD)

The OSD attribute window mode setup register (OSDATRMD) is shown in Figure 114 and described in Table 94.

Figure 114. OSD Attribute Window Mode Setup Register (OSDATRMD)

15	14 12	11 10	9 8	7 6	5 2	1	0
OASW	Reserved	OHZA	OVZA	BLNKINT	Reserved	OFFA	BLNK
R/W-0	R-0	R/W-0	R/W-0	R/W-0	R-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

Table 94. OSD Attribute Window Mode Setup Register (OSDATRMD) Field Descriptions

Bit	Field	Value	Description
15	OASW		OSD window 1 attribute mode enable. This bit enables attribute mode for OSD window 0. VD latches this bit.
		0	OSD window 0
		1	Attribute window
14-12	Reserved	0	Reserved
11-10	OHZA	0-3h	OSD attribute window horizontal zoom (when OASW = 1). VD latches this bit.
		0	× 1
		1h	× 2
		2h	× 4
		3h	Reserved (same as 0)
9-8	OVZA	0-3h	OSD attribute window vertical zoom (when OASW = 1). VD latches this bit.
		0	× 1
		1h	× 2
		2h	× 4
		3h	Reserved (same as 0)
7-6	BLNKINT	0-3h	Blinking interval (when OASW = 1). Specifies the blinking interval of the attribute window in units of 8 VD pulses. VD latches this bit.
		0	1 unit
		1h	2 units
		2h	3 units
		3h	4 units
5-2	Reserved	0	Reserved
1	OFFA		OSD attribute window display mode VD latches this bit.
		0	Field mode
		1	Frame mode
0	BLNK		OSD attribute window blink enable (when OASW = 1). VD latches this bit.
		0	Disable
		1	Enable

6.2.6 Rectangular Cursor Setup (RECTCUR)

The rectangular cursor setup register is shown in Figure 115 and described in Table 95.

Figure 115. Rectangular Cursor Setup (RECTCUR)

31	16
Reserved	
R-0	

15	8	7	6	4	3	1	0
RCAD		CLUTSR	RCHW		RCVW		RCACT
R/W-0		R/W-0	R/W-0		R/W-0		R/W-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 95. RECTCUR - Rectangular Cursor Setup(RECTCUR) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15-8	RCAD	0-FFh	Rectangular cursor color palette address.
7	CLUTSR		CLUT select. This bit is latched by VD.
		0	ROM-look-up table
		1	RAM-look-up table
6-4	RCHW	0-7h	Rectangular cursor horizontal line width. Width is 4xRCHW, with 0 interpreted as 1 pixel. Range is: 1, 4, 8, 16, 20, 24, 28 pixels. This bit is latched by VD.
3-1	RCVW	0-7h	Rectangular cursor vertical line width. Width is 2xRCVW, with 0 interpreted as 1 line. Range is: 1, 2, 4, 6, 8, 10, 12, 14 lines. This bit is latched by VD.
0	RCACT		Rectangular cursor active (displayed). This bit is latched by VD.
		0	Off
		1	On

6.2.7 Reserved 0 (RSV0)

The reserved 0 register is shown in Figure 116 and described in Table 96.

Figure 116. Reserved 0 (RSV0)

31	16
Reserved	
R-0	
15	0
RSV0	
-	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

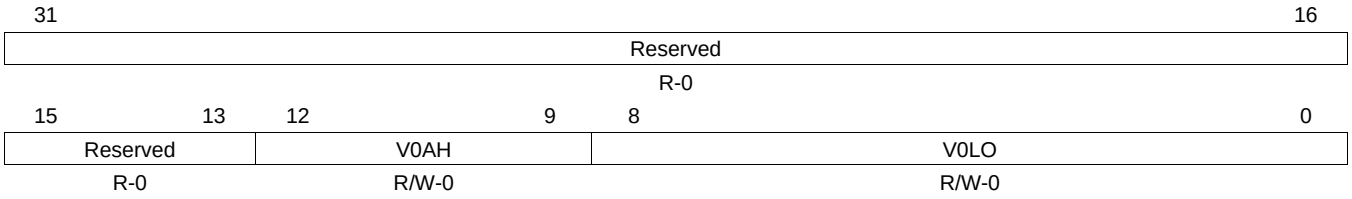
Table 96. Reserved 0 (RSV0) Field Descriptions

Bit	Field	Value	Description
31-0	Reserved	0	Any writes to these bit(s) must always have a value of 0.

6.2.8 Video Window 0 Offset (VIDWIN0OFST)

The video window 0 offset register is shown in Figure 117 and described in Table 97.

Figure 117. Video Window 0 Offset (VIDWIN0OFST)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 97. Video Window 0 Offset (VIDWIN0OFST) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-9	V0AH	0-Fh	Video window 0 SDRAM source address. High 4 MSBs of SDRAM source address. The SDRAM source address is specified as an offset from the SDRAM base address, in units of 32 bytes. This bit is latched by VD.
8-0	V0LO	0-1FFh	Video window 0 line offset. Number of burst transfers (32-bytes) in a horizontal line. Video data format is YCbYCr, or 32-bits per 2 pixels, which gives 16-pixels/burst: Line width in pixels/16 e.g., 720/16 = 45 (0x2D). Note: If line width setting for the window results in a non-integer value, round the value up to the next larger integer and organize the data in SDRAM so that each line begins on a burst boundary. This bit is latched by VD.

6.2.9 Video Window 1 Offset (VIDWIN1OFST)

The video window 1 offset register is shown in Figure 118 and described in Table 98.

Figure 118. Video Window 1 Offset (VIDWIN1OFST)

31	16
Reserved	
R-0	

15	13	12	9	8	0
Reserved		V1AH		V1LO	
R-0		R/W-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 98. Video Window 1 Offset (VIDWIN1OFST) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Reserved
12-9	V1AH	0-Fh	Video window 1 SDRAM source address. High 4 MSBs of SDRAM source address. The SDRAM source address is specified as an offset from the SDRAM base address, in units of 32 bytes. This bit is latched by VD.
8-0	V1LO	0-1FFh	Video window 1 line offset. Number of burst transfers (32-bytes) in a horizontal line. Video data format is YCbYCr, or 32-bits per 2 pixels, which gives 16-pixels/burst: Line width in pixels/16 e.g., 720/16 = 45 (0x2D). Note: If line width setting for the window results in a non-integer value, round the value up to the next larger integer and organize the data in SDRAM so that each line begins on a burst boundary. This bit is latched by VD.

6.2.10 Bitmap Window 0 Offset (OSDWIN0OFST)

The bitmap window 0 offset register is shown in Figure 119 and described in Table 99.

Figure 119. Bitmap Window 0 Offset (OSDWIN0OFST)

31	16
Reserved	
R-0	

15	13	12	9	8	0
Reserved		B0AH		O0LO	
R-0		R/W-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 99. Bitmap Window 0 Offset (OSDWIN0OFST) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-9	B0AH	0-Fh	Bitmap window 0 SDRAM source address. High 4 MSBs of SDRAM source address. The SDRAM source address is specified as an offset from the SDRAM base address, in units of 32 bytes. This bit is latched by VD.
8-0	O0LO	0-1FFh	OSD window 0 line offset. Number of burst transfers (32-bytes) in a horizontal line. This depends on OSD window data format (bits-per-pixel or bpp): Line width in pixels. bpp/256-bits-per-burst e.g., 64*8/256 = 2. Example: Offsets for 256 pixels horizontal: 1-bit mode: (256x 1)/256 = 1(0x0001) 2-bit mode: (256x 2)/256 = 2(0x0002) 4-bit mode: (256x 4)/256 = 4(0x0004) 8-bit mode: (256x 8)/256 = 8(0x0008) RGB565 mode: (256x16)/256 = 16(0x0010) RGB888 mode: (256x32)/256 = 32(0x0020) Note: If line width and bitdepth settings for the window results in a non-integer value, round the value up to the next larger integer and organize the data in SDRAM so that each line begins on a burst boundary. This bit is latched by VD.

6.2.11 Bitmap Window 1/Attribute Window Offset (OSDWIN1OFST)

The bitmap window 1/attribute window offset register is shown in Figure 120 and described in Table 100.

Figure 120. Bitmap Window 1/Attribute Window Offset (OSDWIN1OFST)

31	16
Reserved	
R-0	

15	13	12	9	8	0
Reserved		B1AH		O1LO	
R-0		R/W-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 100. Bitmap Window 1/Attribute Window Offset (OSDWIN1OFST) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-9	B1AH	0-Fh	Bitmap window 1 SDRAM source address. High 4 MSBs of SDRAM source address. The SDRAM source address is specified as an offset from the SDRAM base address, in units of 32 bytes. This bit is latched by VD.
8-0	O1LO	0-1FFh	OSD window 1/attribute window line offset. Number of burst transfers (32-bytes) in a horizontal line. This depends on OSD window data format (bits-per-pixel or bpp): Line width in pixels. bpp/256-bits-per-burst e.g., 64*8/256 = 2 Example: Offsets for 256 pixels horizontal: 1-bit mode: (256x 1)/256 = 1(0x0001) 2-bit mode: (256x 2)/256 = 2(0x0002) 4-bit mode: (256x 4)/256 = 4(0x0004) 8-bit mode: (256x 8)/256 = 8(0x0008) RGB565 mode: (256x16)/256 = 16(0x0010) RGB888 mode: (256x32)/256 = 32(0x0020) Note: If line width and bit depth settings for the window results in a non-integer value, round the value up to the next larger integer and organize the data in SDRAM so that each line begins on a burst boundary. This bit is latched by VD.

6.2.12 Video Window 0/1 Address - High (VIDWINADH)

The video window 0/1 address - high register is shown in Figure 121 and described in Table 101.

Figure 121. Video Window 0/1 Address - High (VIDWINADH)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
R-0															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Rsvd	V1AH							Rsvd	V0AH						
R-0	R/W-0							R-0	R/W-0						

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 101. Video Window 0/1 Address - High (VIDWINADH) Field Descriptions

Bit	Field	Value	Description
31-15	Reserved	0	Any writes to these bit(s) must always have a value of 0.
14-8	V1AH	0-7Fh	Video window 1 SDRAM source address. High 7 MSBs of SDRAM source address. The SDRAM source address is specified as an offset from the SDRAM base address, in units of 32 bytes. This bit is latched by VD.
7	Reserved	0	Any writes to these bit(s) must always have a value of 0.
6-0	V0AH	0-7Fh	Video window 0 SDRAM source address. High 7 MSBs of SDRAM source address. The SDRAM source address is specified as an offset from the SDRAM base address, in units of 32 bytes. This bit is latched by VD.

6.2.13 Video Window 0 Address - Low (VIDWIN0ADL)

The video window 0 address - low register is shown in Figure 122 and described in Table 102.

Figure 122. Video Window 0 Address - Low (VIDWIN0ADL)

31	16
Reserved	
R-0	

15	0
VIDWIN0ADL	
R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 102. Video Window 0 Address - Low (VIDWIN0ADL) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved
15-0	VIDWIN0ADL	0-FFFFh	Video window 0 SDRAM source address. Low 16 LSBs of SDRAM source address. The SDRAM source address is specified as an offset from the SDRAM base address, in units of 32 bytes. This bit is latched by VD.

6.2.14 Video Window 1 Address - Low (VIDWIN1ADL)

The video window 1 address - low register is shown in Figure 123 and described in Table 103.

Figure 123. Video Window 1 Address - Low (VIDWIN1ADL)

31	16
Reserved	
R-0	
15	0
VIDWIN1ADL	
R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 103. Video Window 1 Address - Low (VIDWIN1ADL) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15-0	VIDWIN1ADL	0-FFFFh	Video window 1 SDRAM source address. Low 16 LSBs of SDRAM source address. The SDRAM source address is specified as an offset from the SDRAM base address, in units of 32 bytes. This bit is latched by VD.

6.2.15 Bitmap Window 0/1 Address - High (OSDWINADH)

The bitmap window 0/1 address - high register is shown in Figure 124 and described in Table 104.

Figure 124. Bitmap Window 0/1 Address - High (OSDWINADH)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
R-0															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Rsvd	O1AH							Rsvd	O0AH						
R-0	R/W-0							R-0	R/W-0						

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 104. Bitmap Window 0/1 Address - High (OSDWINADH) Field Descriptions

Bit	Field	Value	Description
31-15	Reserved	0	Any writes to these bit(s) must always have a value of 0.
14-8	O1AH	0-7Fh	BMP window 1/attribute window SDRAM source address. High 7 MSBs of SDRAM source address. The SDRAM source address is specified as an offset from the SDRAM base address, in units of 32 bytes. This bit is latched by VD.
7	Reserved	0	Any writes to these bit(s) must always have a value of 0.
6-0	O0AH	0-7Fh	BMP window 0 SDRAM source address. High 7 MSBs of SDRAM source address. The SDRAM source address is specified as an offset from the SDRAM base address, in units of 32 bytes. This bit is latched by VD.

6.2.16 Bitmap Window 0 Address - Low (OSDWIN0ADL)

The bitmap window 0 address - low register is shown in Figure 125 and described in Table 105.

Figure 125. Bitmap Window 0 Address - Low (OSDWIN0ADL)

31	16
Reserved	
R-0	
15	0
BMPWIN0ADL	
R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 105. Bitmap Window 0 Address - Low (OSDWIN0ADL) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15-0	BMPWIN0ADL	0-FFFFh	BMP window 0 SDRAM source address. Low 16 LSBs of SDRAM source address. The SDRAM source address is specified offset from the SDRAM base address, in units of 32 bytes. This bit is latched by VD.

6.2.17 Bitmap Window 1/Attribute Address - Low (OSDWIN1ADL)

The bitmap window 1/attribute address - low register is shown in Figure 126 and described in Table 106.

Figure 126. Bitmap Window 1/Attribute Address - Low (OSDWIN1ADL)

31	16
Reserved	
R-0	

15	0
BMPWIN1ADL	
R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 106. Bitmap Window 1/Attribute Address - Low (OSDWIN1ADL) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15-0	BMPWIN1ADL	0-FFFFh	BMP window 1/attribute window SDRAM source address. Low 16 LSBs of SDRAM source address (specified in 32-byte units). The SDRAM source address is specified offset from the SDRAM base address in units of 32 bytes. This bit is latched by VD.

6.2.18 Base Pixel X (BASEPX)

The base pixel X register is shown in Figure 127 and described in Table 107.

Figure 127. Base Pixel X (BASEPX)

31	16
Reserved	
R-0	

15	10	9	0
Reserved		BPX	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 107. Base Pixel X (BASEPX) Field Descriptions

Bit	Field	Value	Description
31-10	Reserved	0	Any writes to these bit(s) must always have a value of 0.
9-0	BPX	0-3FFh	Base pixel in X. Horizontal base display reference position for all windows. Specified as number of pixels from HD. Value uses if the max of the register value or these minimums: Minimum value is 20 if EXTMODE.EXPMDSEL = 0 (pre blend filtering). Minimum value is 22 if EXTMODE.EXPMDSEL = 1 (post blend filtering). This bit is latched by VD.

6.2.19 Base Pixel Y (BASEPY)

The base pixel Y register is shown in Figure 128 and described in Table 108.

Figure 128. Base Pixel Y (BASEPY)

31	16
Reserved	
R-0	

15	9	8	0
Reserved		BPY	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

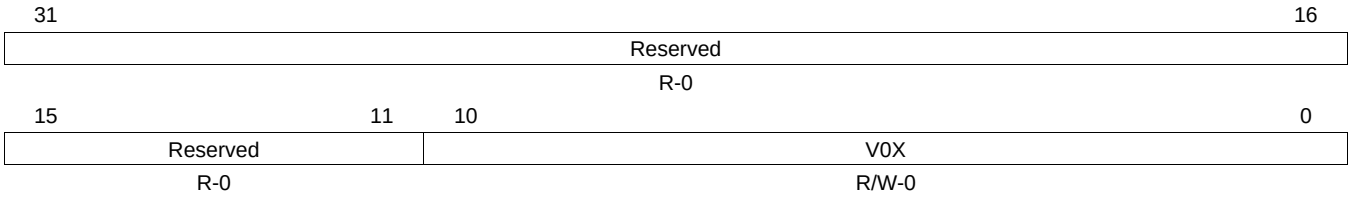
Table 108. Base Pixel Y (BASEPY) Field Descriptions

Bit	Field	Value	Description
31-9	Reserved	0	Any writes to these bit(s) must always have a value of 0.
8-0	BPY	0-1FFh	Base pixel (line) in Y. Vertical base display reference position for all windows. Specified as number of lines from VD. Value used is MAX(BPY,1), i.e., minimum value is 1. This bit is latched by VD.

6.2.20 Video Window 0 X-Position (VIDWIN0XP)

The video window 0 X-position register is shown in Figure 129 and described in Table 109.

Figure 129. Video Window 0 X-Position (VIDWIN0XP)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 109. Video Window 0 X-Position (VIDWIN0XP) Field Descriptions

Bit	Field	Value	Description
31-11	Reserved	0	Any writes to these bit(s) must always have a value of 0.
10-0	V0X	0-7FFh	Video window 0 X-position horizontal display start position. Number of pixels from display reference position (BASEPX). This bit is latched by VD.

6.2.21 Video Window 0 Y-Position (VIDWIN0YP)

The video window 0 Y-position register is shown in Figure 130 and described in Table 110.

Figure 130. Video Window 0 Y-Position (VIDWIN0YP)

31	16
Reserved	
R-0	

15	10	9	0
Reserved		V0Y	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

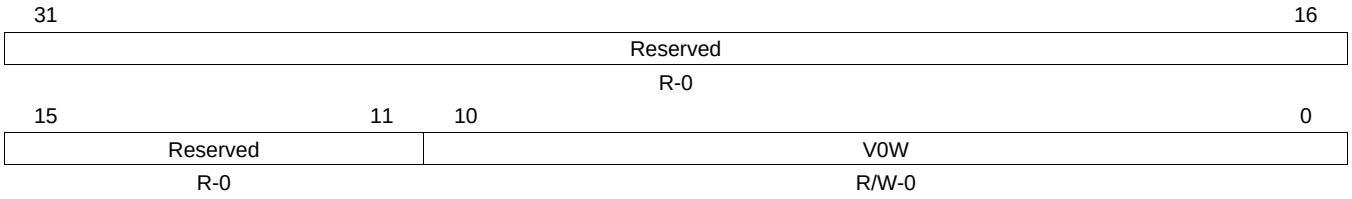
Table 110. Video Window 0 Y-Position (VIDWIN0YP) Field Descriptions

Bit	Field	Value	Description
31-10	Reserved	0	Any writes to these bit(s) must always have a value of 0.
9-0	V0Y	0-3FFh	Video window 0 Y-position vertical display start position. Number of lines from display reference position (BASEPY). This bit is latched by VD.

6.2.22 Video Window 0 X-Size (VIDWIN0XL)

The video window 0 X-size register is shown in Figure 131 and described in Table 111.

Figure 131. Video Window 0 X-Size (VIDWIN0XL)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 111. Video Window 0 X-Size (VIDWIN0XL) Field Descriptions

Bit	Field	Value	Description
31-11	Reserved	0	Any writes to these bit(s) must always have a value of 0.
10-0	V0W	0-7FFh	Video window 0 X-width. Horizontal display width in pixels. This bit is latched by VD.

6.2.23 Video Window 0 Y-Size (VIDWIN0YL)

The video window 0 Y-size register is shown in Figure 132 and described in Table 112.

Figure 132. Video Window 0 Y-Size (VIDWIN0YL)

31	16
Reserved	
R-0	

15	11	10	0
Reserved		V0H	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 112. Video Window 0 Y-Size (VIDWIN0YL) Field Descriptions

Bit	Field	Value	Description
31-11	Reserved	0	Any writes to these bit(s) must always have a value of 0.
10-0	V0H	0-7FFh	Video window 0 Y-height. Vertical display height in lines. This bit is latched by VD.

6.2.24 Video Window 1 X-Position (VIDWIN1XP)

The video window 1 X-position register is shown in Figure 133 and described in Table 113.

Figure 133. Video Window 1 X-Position (VIDWIN1XP)

31	16
Reserved	
R-0	

15	11	10	0
Reserved		V1X	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 113. Video Window 1 X-Position (VIDWIN1XP) Field Descriptions

Bit	Field	Value	Description
31-11	Reserved	0	Any writes to these bit(s) must always have a value of 0.
10-0	V1X	0-7FFh	Video window 1 X-position horizontal display start position. Number of pixels from display reference position (BASEPX). This bit is latched by VD.

6.2.25 Video Window 1 Y-Position (VIDWIN1YP)

The video window 1 Y-position register is shown in Figure 134 and described in Table 114.

Figure 134. Video Window 1 Y-Position (VIDWIN1YP)

31	16
Reserved	
R-0	

15	10	9	0
Reserved		V1Y	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

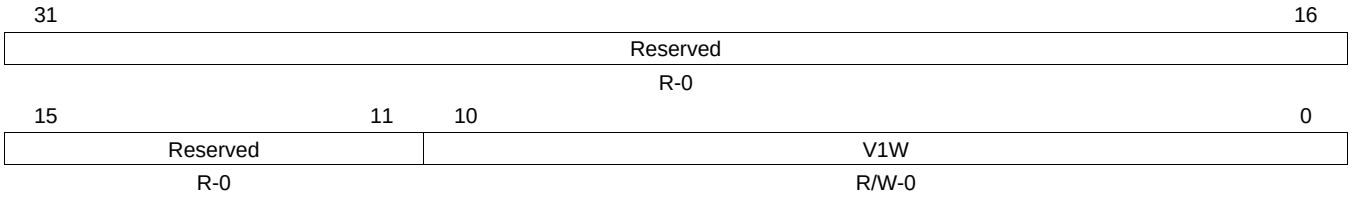
Table 114. Video Window 1 Y-Position (VIDWIN1YP) Field Descriptions

Bit	Field	Value	Description
31-10	Reserved	0	Any writes to these bit(s) must always have a value of 0.
9-0	V1Y	0-3FFh	Video window 1 Y-position vertical display start position. Number of lines from display reference position (BASEPY). This bit is latched by VD.

6.2.26 Video Window 1 X-Size (VIDWIN1XL)

The video window 1 X-size register is shown in Figure 135 and described in Table 115.

Figure 135. Video Window 1 X-Size (VIDWIN1XL)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 115. Video Window 1 X-Size (VIDWIN1XL) Field Descriptions

Bit	Field	Value	Description
31-11	Reserved	0	Any writes to these bit(s) must always have a value of 0.
10-0	V1W	0-7FFh	Video window 1 X-width. Horizontal display width in pixels. This bit is latched by VD.

6.2.27 Video Window 1 Y-Size (VIDWIN1YL)

The video window 1 Y-size register is shown in Figure 136 and described in Table 116.

Figure 136. Video Window 1 Y-Size (VIDWIN1YL)

31	16
Reserved	
R-0	

15	11	10	0
Reserved		V1H	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 116. Video Window 1 Y-Size (VIDWIN1YL) Field Descriptions

Bit	Field	Value	Description
31-11	Reserved	0	Any writes to these bit(s) must always have a value of 0.
10-0	V1H	0-7FFh	Video window 1 Y-height. Vertical display height in lines. This bit is latched by VD.

6.2.28 Bitmap Window 0 X-Position (OSDWIN0XP)

The bitmap window 0 X-position register is shown in Figure 137 and described in Table 117.

Figure 137. Bitmap Window 0 X-Position (OSDWIN0XP)

31	16
Reserved	
R-0	

15	11	10	0
Reserved		W0X	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 117. Bitmap Window 0 X-Position (OSDWIN0XP) Field Descriptions

Bit	Field	Value	Description
31-11	Reserved	0	Any writes to these bit(s) must always have a value of 0.
10-0	W0X	0-7FFh	BMP window 0 X-position horizontal display start position. Number of pixels from display reference position (BASEPX). This bit is latched by VD.

6.2.29 Bitmap Window 0 Y-Position (OSDWIN0YP)

The bitmap window 0 Y-position register is shown in Figure 138 and described in Table 118.

Figure 138. Bitmap Window 0 Y-Position (OSDWIN0YP)

31	16
Reserved	
R-0	

15	10	9	0
Reserved		W0Y	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 118. Bitmap Window 0 Y-Position (OSDWIN0YP) Field Descriptions

Bit	Field	Value	Description
31-10	Reserved	0	Any writes to these bit(s) must always have a value of 0.
9-0	W0Y	0-3FFh	OSD window 0 Y-position vertical display start position. Number of lines from display reference position (BASEPY). This bit is latched by VD.

6.2.30 Bitmap Window 0 X-Size (OSDWIN0XL)

The bitmap window 0 X-size register is shown in Figure 139 and described in Table 119.

Figure 139. Bitmap Window 0 X-Size (OSDWIN0XL)

31	16
Reserved	
R-0	

15	11	10	0
Reserved		W0W	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 119. Bitmap Window 0 X-Size (OSDWIN0XL) Field Descriptions

Bit	Field	Value	Description
31-11	Reserved	0	Any writes to these bit(s) must always have a value of 0.
10-0	W0W	0-7FFh	BMP window 0 X-width. Horizontal display width in pixels. This bit is latched by VD.

6.2.31 Bitmap Window 0 Y-Size (OSDWIN0YL)

The bitmap window 0 Y-size register is shown in Figure 140 and described in Table 120.

Figure 140. Bitmap Window 0 Y-Size (OSDWIN0YL)

31	16
Reserved	
R-0	

15	11	10	0
Reserved		W0H	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 120. Bitmap Window 0 Y-Size (OSDWIN0YL) Field Descriptions

Bit	Field	Value	Description
31-11	Reserved	0	Any writes to these bit(s) must always have a value of 0.
10-0	W0H	0-7FFh	BMP window 0 Y-height. Vertical display height in lines. This bit is latched by VD.

6.2.32 Bitmap Window 1 X-Position (OSDWIN1XP)

The bitmap window 1 X-position register is shown in Figure 141 and described in Table 121.

Figure 141. Bitmap Window 1 X-Position (OSDWIN1XP)

31	16
Reserved	
R-0	

15	11	10	0
Reserved		W1X	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 121. Bitmap Window 1 X-Position (OSDWIN1XP) Field Descriptions

Bit	Field	Value	Description
31-11	Reserved	0	Any writes to these bit(s) must always have a value of 0.
10-0	W1X	0-7FFh	BMP window 1 X-position horizontal display start position. Number of pixels from display reference position (BASEPX). This bit is latched by VD.

6.2.33 Bitmap Window 1 Y-Position (OSDWIN1YP)

The bitmap window 1 Y-position register is shown in Figure 142 and described in Table 122.

Figure 142. Bitmap Window 1 Y-Position (OSDWIN1YP)

31	16
Reserved	
R-0	

15	10	9	0
Reserved		W1Y	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 122. Bitmap Window 1 Y-Position (OSDWIN1YP) Field Descriptions

Bit	Field	Value	Description
31-10	Reserved	0	Any writes to these bit(s) must always have a value of 0.
9-0	W1Y	0-3FFh	BMP window 1 Y-position vertical display start position. Number of lines from display reference position (BASEPY). This bit is latched by VD.

6.2.34 Bitmap Window 1 X-Size (OSDWIN1XL)

The bitmap window 1 X-size register is shown in Figure 143 and described in Figure 143.

Figure 143. Bitmap Window 1 X-Size (OSDWIN1XL)

31	16
Reserved	
R-0	

15	11	10	0
Reserved		W1W	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 123. Bitmap Window 1 X-Size (OSDWIN1XL) Field Descriptions

Bit	Field	Value	Description
31-11	Reserved	0	Any writes to these bit(s) must always have a value of 0.
10-0	W1W	0-7FFh	BMP Window 1 X-Width Horizontal display width in pixels. This bit is latched by VD.

6.2.35 Bitmap Window 1 Y-Size (OSDWIN1YL)

The bitmap window 1 Y-size register is shown in Figure 144 and described in Table 124.

Figure 144. Bitmap Window 1 Y-Size (OSDWIN1YL)

31	16
Reserved	
R-0	

15	11	10	0
Reserved		W1H	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 124. Bitmap Window 1 Y-Size (OSDWIN1YL) Field Descriptions

Bit	Field	Value	Description
31-11	Reserved	0	Any writes to these bit(s) must always have a value of 0.
10-0	W1H	0-7FFh	BMP window 1 Y-height. Vertical display height in lines. This bit is latched by VD.

6.2.36 Rectangular Cursor Window X-Position (CURXP)

The rectangular cursor window X-position register is shown in Figure 145 and described in Table 125.

Figure 145. Rectangular Cursor Window X-Position (CURXP)

31	16
Reserved	
R-0	

15	11	10	0
Reserved		RCSX	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 125. Rectangular Cursor Window X-Position (CURXP) Field Descriptions

Bit	Field	Value	Description
31-11	Reserved	0	Any writes to these bit(s) must always have a value of 0.
10-0	RCSX	0-7FFh	Rectangular Cursor Window X-Position Horizontal display start position - number of pixels from display reference position (BASEPX). This bit is latched by VD.

6.2.37 Rectangular Cursor Window Y-Position (CURYP)

The rectangular cursor window Y-position register is shown in Figure 146 and described in Table 126.

Figure 146. Rectangular Cursor Window Y-Position (CURYP)

31	16
Reserved	
R-0	

15	10	9	0
Reserved		RCSY	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

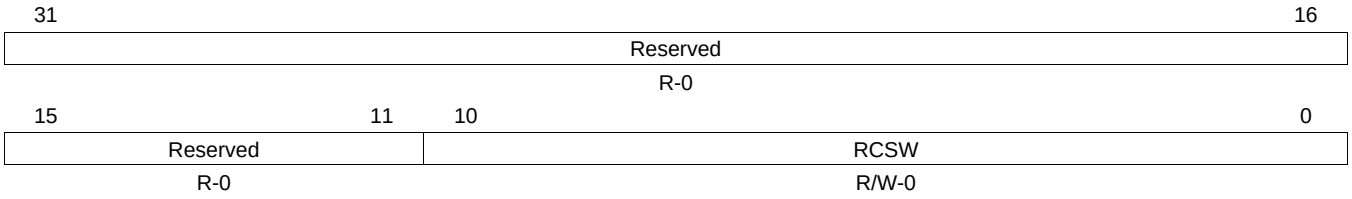
Table 126. Rectangular Cursor Window Y-Position (CURYP) Field Descriptions

Bit	Field	Value	Description
31-10	Reserved	0	Any writes to these bit(s) must always have a value of 0.
9-0	RCSY	0-3FFh	Rectangular Cursor window Y-position vertical display start position. Number of lines from display reference position (BASEPY). This bit is latched by VD.

6.2.38 Rectangular Cursor Window X-Size (CURXL)

The rectangular cursor window X-size register is shown in Figure 147 and described in Table 127.

Figure 147. Rectangular Cursor Window X-Size (CURXL)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

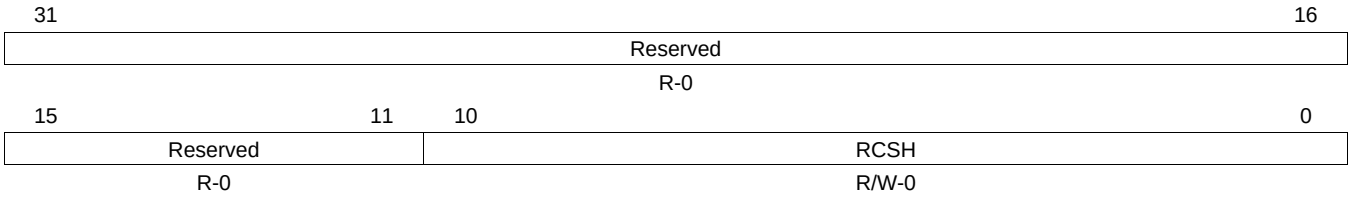
Table 127. Rectangular Cursor Window X-Size (CURXL) Field Descriptions

Bit	Field	Value	Description
31-11	Reserved	0	Any writes to these bit(s) must always have a value of 0.
10-0	RCSW	0-7FFh	Rectangular cursor window X-width. Horizontal display width in pixels. This bit is latched by VD. If user configures 0x00 for horizontal and vertical cursor size, 1 pixel square is displayed.

6.2.39 Rectangular Cursor Window Y-Size (CURYL)

The rectangular cursor window Y-size register is shown in Figure 148 and described in Table 128.

Figure 148. Rectangular Cursor Window Y-Size (CURYL)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 128. Rectangular Cursor Window Y-Size (CURYL) Field Descriptions

Bit	Field	Value	Description
31-11	Reserved	0	Any writes to these bit(s) must always have a value of 0.
10-0	RCSH	0-7FFh	Rectangular cursor window Y-height. Vertical display height in lines. Note: Specified in number of field line. Note: DM350 corrects and errata in previous DMxx devices which reduced display height by 1 line. Thus, using the same setting in DM350 used on other devices will result in an additional line (per field) being displayed. This bit is latched by VD.

6.2.40 Reserved 1 (RSV1)

The reserved 1 register is shown in Figure 149 and described in Table 129.

Figure 149. Reserved 1 (RSV1)

31	16
RSV1	
-	

15	0
RSV1	
-	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 129. Reserved 1 (RSV1) Field Descriptions

Bit	Field	Value	Description
31-0	RSV1	0	Reserved

6.2.41 Reserved 2 (RSV2)

The reserved 2 register is shown in Figure 150 and described in Table 130.

Figure 150. Reserved 2 (RSV2)

31-16
RSV2
--
15-0
RSV2
-

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 130. Reserved 2 (RSV2) Field Descriptions

Bit	Field	Value	Description
31-0	RSV2	0	Reserved

6.2.42 Window 0 Bitmap Value to Palette Map 0/1 (W0BMP01)

The window 0 bitmap value to palette map 0/1 register is shown in Figure 151 and described in Table 131.

Figure 151. Window 0 Bitmap Value to Palette Map 0/1 (W0BMP01)

31	16
Reserved	
R-0	

15	8	7	0
PAL01		PAL00	
R/W-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

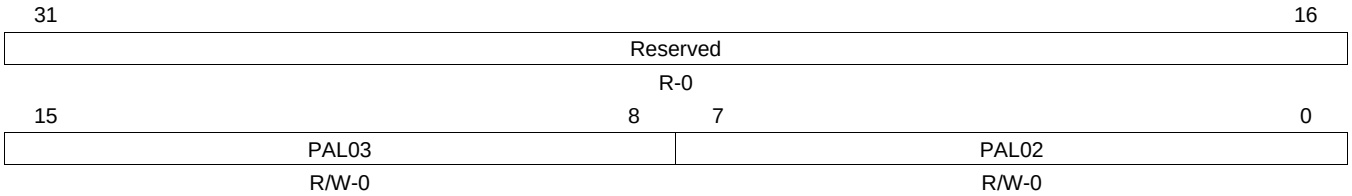
Table 131. Window 0 Bitmap Value to Palette Map 0/1 (W0BMP01) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved
15-8	PAL01	0-FFh	Palette address for bitmap value 1. OSD window 0 [4-bit].
7-0	PAL00	0-FFh	Palette address for bitmap value 0. OSD window 0 [4-bit, 2-bit, 1-bit].

6.2.43 Window 0 Bitmap Value to Palette Map 2/3 (W0BMP23)

The window 0 bitmap value to palette map 2/3 register is shown in Figure 152 and described in Table 132.

Figure 152. Window 0 Bitmap Value to Palette Map 2/3 (W0BMP23)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

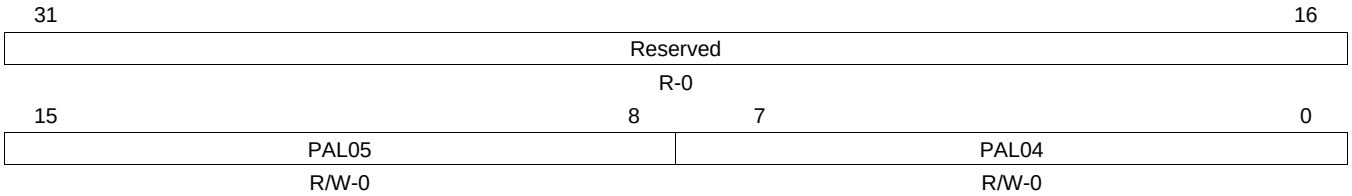
Table 132. Window 0 Bitmap Value to Palette Map 2/3 (W0BMP23) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved
15-8	PAL03	0-FFh	Palette address for bitmap value 3. OSD window 0 [4-bit].
7-0	PAL02	0-FFh	Palette address for bitmap value 2. OSD window 0 [4-bit].

6.2.44 Window 0 Bitmap Value to Palette Map 4/5 (W0BMP45)

The window 0 bitmap value to palette map 4/5 register is shown in Figure 153 and described in Table 133.

Figure 153. Window 0 Bitmap Value to Palette Map 4/5 (W0BMP45)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 133. Window 0 Bitmap Value to Palette Map 4/5 (W0BMP45) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved
15-8	PAL05	0-FFh	Palette address for bitmap value 5. OSD window 0 [4-bit, 2-bit].
7-0	PAL04	0-FFh	Palette address for bitmap value 4. OSD window 0 [4-bit].

6.2.45 Window 0 Bitmap Value to Palette Map 6/7 (W0BMP67)

The window 0 bitmap value to palette map 6/7 register is shown in Figure 154 and described in Table 134.

Figure 154. Window 0 Bitmap Value to Palette Map 6/7 (W0BMP67)

31	16
Reserved	
R-0	

15	8	7	0
PAL07		PAL06	
R/W-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

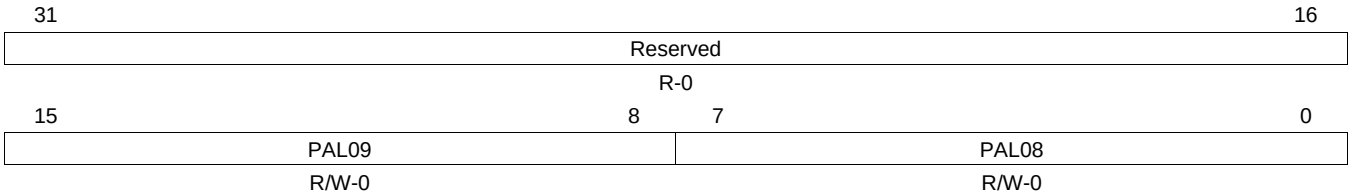
Table 134. Window 0 Bitmap Value to Palette Map 6/7 (W0BMP67) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved
15-8	PAL07	0-FFh	Palette address for bitmap value 7. OSD window 0 [4-bit].
7-0	PAL06	0-FFh	Palette address for bitmap value 6. OSD window 0 [4-bit].

6.2.46 Window 0 Bitmap Value to Palette Map 8/9 (W0BMP89)

The window 0 bitmap value to palette map 8/9 register is shown in Figure 155 and described in Table 135.

Figure 155. Window 0 Bitmap Value to Palette Map 8/9 (W0BMP89)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 135. Window 0 Bitmap Value to Palette Map 8/9 (W0BMP89) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved
15-8	PAL09	0-FFh	Palette address for bitmap value 9. OSD window 0 [4-bit].
7-0	PAL08	0-FFh	Palette address for bitmap value 8. OSD window 0 [4-bit].

6.2.47 Window 0 Bitmap Value to Palette Map A/B (W0BMPAB)

The window 0 bitmap value to palette map A/B register is shown in Figure 156 and described in Table 136.

Figure 156. Window 0 Bitmap Value to Palette Map A/B (W0BMPAB)

31	16
Reserved	
R-0	

15	8	7	0
PAL11		PAL10	
R/W-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

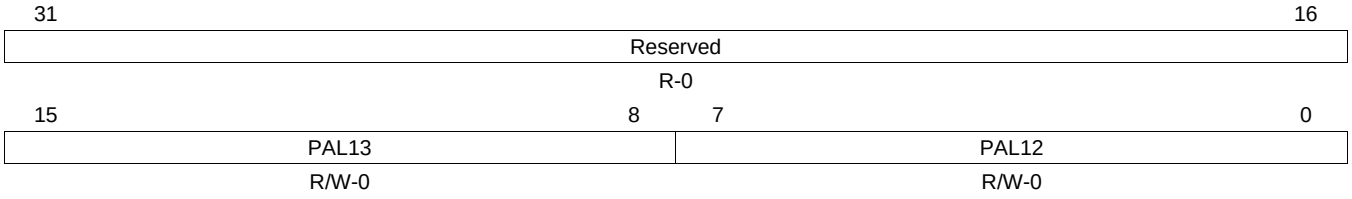
Table 136. Window 0 Bitmap Value to Palette Map A/B (W0BMPAB) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved
15-8	PAL11	0-FFh	Palette address for bitmap value B. OSD window 0 [4-bit].
7-0	PAL10	0-FFh	Palette address for bitmap value A. OSD window 0 [4-bit, 2-bit].

6.2.48 Window 0 Bitmap Value to Palette Map C/D (W0BMPCD)

The window 0 bitmap value to palette map C/D register is shown in Figure 157 and described in Table 137.

Figure 157. Window 0 Bitmap Value to Palette Map C/D (W0BMPCD)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 137. Window 0 Bitmap Value to Palette Map C/D (W0BMPCD) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved
15-8	PAL13	0-FFh	Palette address for bitmap value D. OSD window 0 [4-bit].
7-0	PAL12	0-FFh	Palette address for bitmap value C. OSD window 0 [4-bit].

6.2.49 Window 0 Bitmap Value to Palette Map E/F (W0BMPEF)

The window 0 bitmap value to palette map E/F register is shown in Figure 158 and described in Table 138.

Figure 158. Window 0 Bitmap Value to Palette Map E/F (W0BMPEF)

31	16
Reserved	
R-0	

15	8	7	0
PAL15		PAL14	
R/W-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

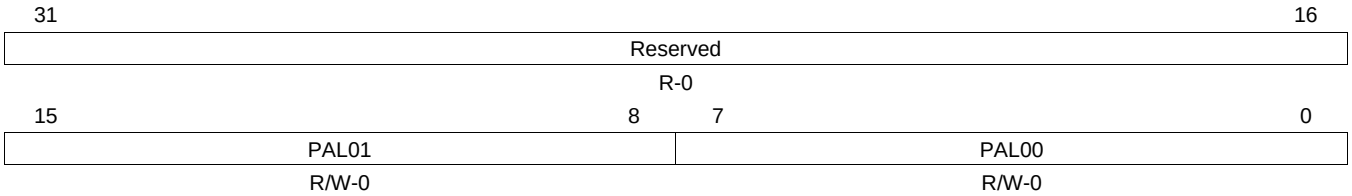
Table 138. Window 0 Bitmap Value to Palette Map E/F (W0BMPEF) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved
15-8	PAL15	0-FFh	Palette address for bitmap value F. OSD window 0 [4-bit, 2-bit, 1-bit].
7-0	PAL14	0-FFh	Palette address for bitmap value E. OSD window 0 [4-bit].

6.2.50 Window 1 Bitmap Value to Palette Map 0/1 (W1BMP01)

The window 1 bitmap value to palette map 0/1 register is shown in Figure 159 and described in Table 139.

Figure 159. Window 1 Bitmap Value to Palette Map 0/1 (W1BMP01)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 139. Window 1 Bitmap Value to Palette Map 0/1 (W1BMP01) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved
15-8	PAL01	0-FFh	Palette address for bitmap value 1. OSD window 1 [4-bit].
7-0	PAL00	0-FFh	Palette address for bitmap value 0. OSD window 1 [4-bit, 2-bit, 1-bit].

6.2.51 Window 1 Bitmap Value to Palette Map 2/3 (W1BMP23)

The window 1 bitmap value to palette map 2/3 register is shown in Figure 160 and described in Table 140.

Figure 160. Window 1 Bitmap Value to Palette Map 2/3 (W1BMP23)

31	16
Reserved	
R-0	

15	8	7	0
PAL03		PAL02	
R/W-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

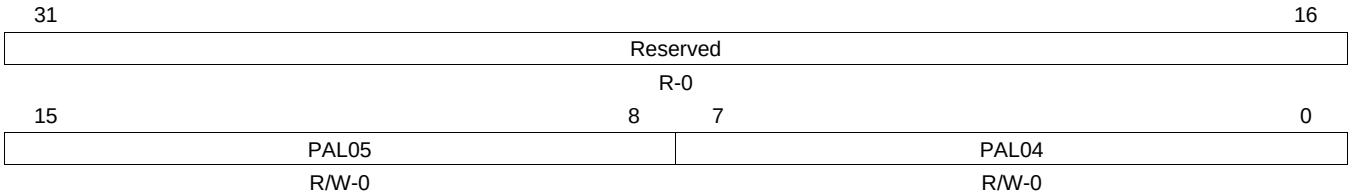
Table 140. Window 1 Bitmap Value to Palette Map 2/3 (W1BMP23) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved
15-8	PAL03	0-FFh	Palette address for bitmap value 3. OSD window 1 [4-bit].
7-0	PAL02	0-FFh	Palette address for bitmap value 2. OSD window 1 [4-bit].

6.2.52 Window 1 Bitmap Value to Palette Map 4/5 (W1BMP45)

The window 1 bitmap value to palette map 4/5 register is shown in Figure 161 and described in Table 141.

Figure 161. Window 1 Bitmap Value to Palette Map 4/5 (W1BMP45)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 141. Window 1 Bitmap Value to Palette Map 4/5 (W1BMP45) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved
15-8	PAL05	0-FFh	Palette address for bitmap value 5. OSD window 1 [4-bit, 2-bit].
7-0	PAL04	0-FFh	Palette address for bitmap value 4. OSD window 1 [4-bit].

6.2.53 Window 1 Bitmap Value to Palette Map 6/7 (W1BMP67)

The window 1 bitmap value to palette map 6/7 register is shown in Figure 162 and described in Table 142.

Figure 162. Window 1 Bitmap Value to Palette Map 6/7 (W1BMP67)

31	16
Reserved	
R-0	

15	8	7	0
PAL07		PAL06	
R/W-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

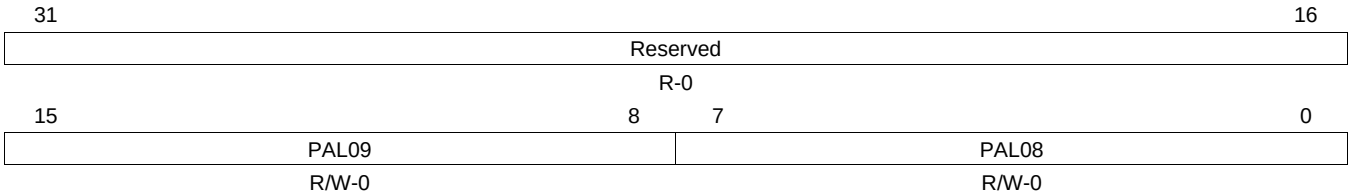
Table 142. Window 1 Bitmap Value to Palette Map 6/7 (W1BMP67) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved
15-8	PAL07	0-FFh	Palette address for bitmap value 7. OSD window 1 [4-bit].
7-0	PAL06	0-FFh	Palette address for bitmap value 6. OSD window 1 [4-bit].

6.2.54 Window 1 Bitmap Value to Palette Map 8/9 (W1BMP89)

The window 1 bitmap value to palette map 8/9 register is shown in Figure 163 and described in Table 143.

Figure 163. Window 1 Bitmap Value to Palette Map 8/9 (W1BMP89)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 143. Window 1 Bitmap Value to Palette Map 8/9 (W1BMP89) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved
15-8	PAL09	0-FFh	Palette address for bitmap value 9. OSD window 1 [4-bit].
7-0	PAL08	0-FFh	Palette address for bitmap value 8. OSD window 1 [4-bit].

6.2.55 Window 1 Bitmap Value to Palette Map A/B (W1BMPAB)

The window 1 bitmap value to palette map A/B register is shown in Figure 164 and described in Table 144.

Figure 164. Window 1 Bitmap Value to Palette Map A/B (W1BMPAB)

31	16
Reserved	
R-0	

15	8	7	0
PAL11		PAL10	
R/W-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 144. Window 1 Bitmap Value to Palette Map A/B (W1BMPAB) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved
15-8	PAL11	0-FFh	Palette address for bitmap value B. OSD window 1 [4-bit].
7-0	PAL10	0-FFh	Palette address for bitmap value A. OSD window 1 [4-bit, 2-bit].

6.2.56 Window 1 Bitmap Value to Palette Map C/D (W1BMPCD)

The window 1 bitmap value to palette map C/D register is shown in Figure 165 and described in Table 145.

Figure 165. Window 1 Bitmap Value to Palette Map C/D (W1BMPCD)

31	16
Reserved	
R-0	

15	8	7	0
PAL13		PAL12	
R/W-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 145. Window 1 Bitmap Value to Palette Map C/D (W1BMPCD) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved
15-8	PAL13	0-FFh	Palette address for bitmap value D. OSD window 1 [4-bit].
7-0	PAL12	0-FFh	Palette address for bitmap value C. OSD window 1 [4-bit].

6.2.57 Window 1 Bitmap Value to Palette Map E/F (W1BMPEF)

The window 1 bitmap value to palette map E/F register is shown in Figure 166 and described in Table 146.

Figure 166. Window 1 Bitmap Value to Palette Map E/F (W1BMPEF)

31	16
Reserved	
R-0	

15	8	7	0
PAL15		PAL14	
R/W-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 146. Window 1 Bitmap Value to Palette Map E/F (W1BMPEF) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved
15-8	PAL15	0-FFh	Palette address for bitmap value F. OSD window 1 [4-bit, 2-bit, 1-bit].
7-0	PAL14	0-FFh	Palette address for bitmap value E. OSD window 1 [4-bit].

6.2.58 Test Mode (VBNDRY)

The test mode register is shown in Figure 167 and described in Table 147.

Figure 167. Test Mode (VBNDRY)

31	16
Reserved	
R-0	

15	8	7	4	3	2	1	0
TSTPATNCHROMA		Reserved		VFILINCMD	VBNDRYPRCSEN	TEST1	TEST0
R/W-0		R-0		R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 147. Test Mode (VBNDRY) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved
15-8	TSTPATNCHROMA	0-FFh	Chrominance data input register for test mode.
7-4	Reserved	0	Reserved
3	VFILINCMD		Vertical filter increment mode. Increment mode of address counter in vertical expansion of video or bitmap windows. Turn ON to have vertical filtering increment past the end of the vertical display area. In this case, additional data to be processed for vertical filtering should be stored in SDRAM, immediately following the display data. Turn OFF to have vertical filtering stop incrmenting when it reaches the last display line. This is the DM320 equivalent mode
		0	Increment off (DM340 specific mode)
		1	Increment on (DM320 mode)
2	VBNDRYPRCSEN		Video boundary processing active. Enables video boundary processing. In x9/8 or x6/5 expansion mode, with dual video windows displayed, specific boundary processing can be used.
		0	OFF (same as DM320; no specific processing)
		1	ON (with specific processing; DM340 custom mode)
1	TEST1	0	Reserved
0	TEST0	0	Reserved

6.2.59 Extended Mode (EXTMODE)

The extended mode register is shown in Figure 168 and described in Table 148.

Figure 168. Extended Mode (EXTMODE)

31	16
Reserved	
R-0	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EXPMDSEL	SCRNHEXP		SCRNVEXP	OSD1BLDCHR	OSD0BLDCHR	ATNOSD1EN	ATNOSD0EN	OSDHRSZ15	VIDHRSZ15	ZMFILV1HEN	ZMFILV1VEN	ZMFILV0HEN	ZMFILV0VEN	EXPFILHEN	EXPFILVEN
R/W-0	R/W-0		R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 148. Extended Mode (EXTMODE) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved
15	EXPMDSEL		Expansion filtering mode select. Affects both horizontal or vertical directions. When enabled (filter after blending), SCRNHEXP and SCRNVEXP are used. If this bit is enabled, MODE.EF must be 0.
		0	Filter before blend (DM320 mode)
		1	Filter after blend (DM340 mode)
14-13	SCRNHEXP		Horizontal expansion mode. This is only used if EXPMDSEL = 1. Note: Make sure that window start position and displayed size is same as configured value of each window if either expansion ration is enabled.
		00	No expansion
		01	NTSC x9/8 horizontal expansion (VGA->D1)
		10	Horizontal expansion (VGA->960 pixel LCD)
		11	Reserved : Same as 00
12	SCRNVEXP		Vertical expansion mode. This is only used if EXPMDSEL = 1. Note: Make sure that window start position and displayed size is same as configured value of each window if either expansion ration is enabled.
		0	No expansion
		1	NTSC->PAL x6/5 vertical expansion
11	OSD1BLDCHR		OSD bitmap 1 blend characteristics. Enables pixel level blending between OSD bitmap 1 and video windows using RGB888 mode 8-bits of extended data with blend factor (3-bit). Note: Enabling this mode has no effect unless: • OSDWIN1MD.OASW = 0 (not attribute) • OSDWIN1MD.BMP1MD = 10 (RGB24) • OSDWIN1MD.OACT1 = 1 (window is displayed) In all other cases, this configuration value here is ignored.
		0	Global blend
		1	Pixel level blend
10	OSD0BLDCHR		OSD bitmap 0 blend characteristics. Enables pixel level blending between OSD bitmap 0 and video windows using RGB888 mode 8-bits of extended data with blend factor (3-bit). Note: Enabling this mode has no effect unless: • OSDWIN0MD.BMP0MD = 10 (RGB24) • OSDWIN0MD.OACT0 = 1 (window is displayed) In all other cases, this configuration value here is ignored.
		0	Global blend
		1	Pixel level blend
9	ATNOSD1EN		Attenuation enable for REC601 for OSD bitmap 1. Controls attenuation of data in bitmap window 1 based on REC601 limits. Note: This is only applied when RGB16 or RGB24 data is input (OSDWIN1MD.BMP1MD = 01 or 10).
		0	Normal levels (Y 0-255, Cr 0-255, Cb 0-255)
		1	Attenuated levels (Y 16-235, Cr 16-240, Cb 16-240)

Table 148. Extended Mode (EXTMODE) Field Descriptions (continued)

Bit	Field	Value	Description
8	ATNOSD0EN		Attenuation enable for REC601 for OSD bitmap 0. Controls attenuation of data in bitmap window 0 based on REC601 limits. Note: This is only applied when RGB16 or RGB24 data is input (OSDWIN0MD.BMP0MD = 01 or 10).
		0	Normal levels (Y 0-255, Cr 0-255, Cb 0-255)
		1	Attenuated levels (Y 16-235, Cr 16-240, Cb 16-240)
7	OSDHRSZ15		OSD bitmap window horizontal 1.5x expansion. This function is to enable a 640 pixel width image to be displayed as a 960 pixel wide image; i.e., VGA to specific LCD conversion. This expansion has no filtering; it just executes a pixel copy once per 3 pixels. Notice that target window of this register has to be higher priority if window 0 and window 1 are configured to be duplicated. Note: This setting only takes effect if: • MODE.OHRSZ = 0 (no other horizontal expansion) • EXTMODE.EXPMDSEL = 0 (filter before blend)
		0	Normal mode, depends on MODE.OHRSZ
		1	Horizontal x1.5 expansion.
6	VIDHRSZ15		OSD video window horizontal 1.5x expansion. This function is to enable a 640 pixel width image to be displayed as a 960 pixel wide image; i.e., VGA to specific LCD conversion. User can perform 2-tap filtering with user defined coefficients if MODE.EF = 1. Notice that target window of this register has to be higher priority if window 0 and window 1 are configured to be duplicated. Note: This setting only takes effect if: • MODE.VHRSZ = 0 (no other horizontal expansion) • EXTMODE.EXPMDSEL = 0 (filter before blend)
		0	Normal mode, depends on MODE.VHRSZ
		1	Horizontal x1.5 expansion.
5	ZMFILV1HEN		Video window 1 horizontal zoom filter. If this zoom filter is active, interpolation based on 2-tap filter with 1:1 coefficient is carried out. Note: this control is available only if: • MODE.EF = 0 (no other expansion filtering) • VIDWINMD.ACT1 = 1 (VidWin1 is displayed)
		0	No filter
		1	Filter active for horizontal direction
4	ZMFILV1VEN		Video window 1 vertical zoom filter. If this zoom filter is active, interpolation based on 2-tap filter with 1:1 coefficient is carried out. Note: this control is available only if: • MODE.EF = 0 (no other expansion filtering) • EXTMODE.EXPFILVEN = 0 (x6/5 vertical filter disabled) • VIDWINMD.ACT1 = 1 (VidWin1 is displayed)
		0	No filter
		1	Filter active for vertical direction
3	ZMFILV0HEN		Video window 0 horizontal zoom filter. If this zoom filter is active, interpolation based on 2-tap filter with 1:1 coefficient is carried out. Note: this control is available only if: • MODE.EF = 0 (no other expansion filtering) • VIDWINMD.ACT0 = 0 (VidWin0 is displayed)
		0	No filter
		1	Filter active for horizontal direction
2	ZMFILV0VEN		Video window 0 vertical zoom filter. If this zoom filter is active, interpolation based on 2-tap filter with 1:1 coefficient is carried out. Note: this control is available only if: • MODE.EF = 0 (no other expansion filtering) • EXTMODE.EXPFILVEN = 0 (x6/5 vertical filter disabled) • VIDWINMD.ACT0 = 0 (VidWin0 is displayed)
		0	No filter
		1	Filter active for vertical direction

Table 148. Extended Mode (EXTMODE) Field Descriptions (continued)

Bit	Field	Value	Description
1	EXPFILHEN		Horizontal expansion filter enable. This setting is only active if video window 0 or video window 1 is active. If the expansion filter is active, interpolation based on a 2-tap filter with coefficients in hardware is carried out. If inactive, no filtering is carried out (just pixel copy is available). Notice that this function is available only for video window, and targeted video window has to be higher priority if window 0 and window 1 are to be duplicated. Notice that this control register configures only horizontal filtering, so this configured value is available only when MODE.EF = 0 (no expansion filtering). Additionally, notice that configuration of this register bit is available only case that any expansion (x9/8(h) and x3/2(h)) works.
		0	Expansion Filter Off
		1	Expansion Filter On
0	EXPFILVEN		Vertical expansion filter enable. This setting is only active if video window 0 or video window 1 is active. If the expansion filter is active, interpolation based on a 2-tap filter with coefficients in hardware is carried out. If inactive, no filtering is carried out (just pixel copy is available). Notice that this function is available only for video window, and targeted video window has to be higher priority if window 0 and window 1 are to be duplicated. Notice that this control register configures only vertical filtering, so this configured value is available only when MODE.EF = 0 (no expansion filtering). Additionally, notice that configuration of this register bit is available only case that any expansion (x6/5(v)) works.
		0	Expansion Filter Off
		1	Expansion Filter On

6.2.60 Miscellaneous Control (MISCCTL)

The miscellaneous control register is shown in Figure 169 and described in Table 149.

Figure 169. Miscellaneous Control (MISCCTL)

31	16
Reserved	
R-0	

15	14	13	12	11	8	7	6	5	4	3	2	0
BLDSEL	YC420	BBF_TH	CRM_CALC	Reserved		FIELD_ID	DMANG	Rsvd	RSEL	CPBSY	Reserved	
R-0	R/W-0	R/W-0	R/W-0	R-0		R-0	R/C-0	R-0	R/W-0	R-0	R-00	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 149. Miscellaneous Control (MISCCTL) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved
15	BLDSEL		Blend factor select bit for RGB888 mode.
		0	Compatible blend factor selection; use [26:24] for blend (DM340/DM350 compatible)
		1	New blend factor selection; use [31:29] for Xena
14	YC420		Read data format select bit
		0	422
		1	420
13	BBF_TH		Bitmap blend factor through mode select bit
		0	use blend factor
		1	blend factor through mode
12	CRM_CALC		Blend calculation for Croma
		0	signed
		1	unsigned
11-8	Reserved	0	Reserved
7	FIELD_ID		Field ID. Equal to the value of current field.
		0	Top Field (ID=0)
		1	Bottom Field (ID=1)
6	DMANG		OSD DMA status. Write 1 to reset this field after an error.
		0	Successful DMA
		1	DMA no good, OSD bandwidth limitation
5	Reserved	0	Reserved
4	RSEL		CLUT ROM selection.
		0	Macintosh color look-up table (same as DM320)
		1	Color look-up table from DM270 and prior devices
3	CPBSY		CLUT write busy. Used when writing CLUT data to RAM.
		0	Not busy, okay to write
		1	Busy, do not write
2-0	Reserved	0	Reserved, set to 0.

6.2.61 CLUT RAM Y/Cb Setup (CLUTRAMYCB)

The CLUT RAM Y/Cb setup register is shown in Figure 170 and described in Table 150.

Figure 170. CLUT RAM Y/Cb Setup (CLUTRAMYCB)

31	16
Reserved	
R-0	

15	8	7	0
Y		CB	
R/W-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 150. CLUT RAM Y/Cb Setup (CLUTRAMYCB) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved
15-8	Y	0-FFh	Write Y-data into built-in CLUT-RAM. Note: It is necessary to write into CLUTRAMYCB before CLUTRAMCR.
7-0	CB	0-FFh	Write Cb-data into built-in CLUT-RAM. Note: It is necessary to write into CLUTRAMYCB before CLUTRAMCR.

6.2.62 CLUT RAM Cr/Mapping Setup (CLUTRAMCR)

The CLUT RAM Cr/mapping setup register is shown in Figure 171 and described in Table 151.

Figure 171. CLUT RAM Cr/Mapping Setup (CLUTRAMCR)

31	16
Reserved	
R-0	

15	8	7	0
CR		CADDR	
R/W-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 151. CLUT RAM Cr/Mapping Setup (CLUTRAMCR) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved
15-8	CR	0-FFh	Write Cr data into built-in CLUT-RAM. Note: It is necessary to write into CLUTRAMYCB before CLUTRAMCR.
7-0	CADDR	0-FFh	CLUT write palette address. When updating CLUT_RAM: • Verify CPBSY=0 in MISCCTL • Write CLUTRAMYCB before CLUTRAMCR

6.2.63 Transparent Color Code - Lower (TRANSPVALL)

The transparent color code - lower register is shown in Figure 172 and described in Table 152.

Figure 172. Transparent Color Code - Lower (TRANSPVALL)

31	16
Reserved	
R-0	

15	0
RGBL	
R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

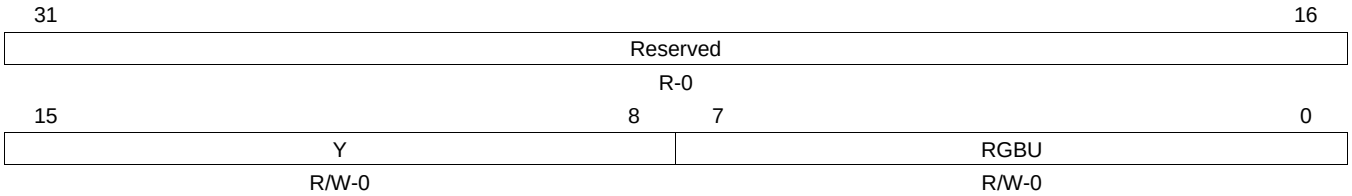
Table 152. Transparent Color Code - Lower (TRANSPVALL) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved
15-0	RGBL	0-FFFFh	RGB transparency value (lower 16). Transparent color code when RGB565 or RGB888 modes used in a bitmap window. • If RGB565 mode, user configures RGB565 transparent color code. • If RGB888 mode, user configures lower 16-bits of RGB888 transparent color code.

6.2.64 Transparent Color Code - Upper (TRANSPVALU)

The transparent color code - upper register is shown in Figure 173 and described in Table 153.

Figure 173. Transparent Color Code - Upper (TRANSPVALU)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 153. Transparent Color Code - Upper (TRANSPVALU) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved
15-8	Y	0-FFh	Luma transparency value. Transparent Luma color code when YC mode used in a bitmap window.
7-0	RGBU	0-FFh	RGB transparency value (upper 8). Transparent color code when RGB888 mode used in a bitmap window. If RGB888 mode, user configures upper 8-bits of RGB888 transparent color code.

6.2.65 Transparent Index Code for Bitmaps (TRANSPBMPIDX)

The transparent index code for bitmaps register is shown in Figure 174 and described in Table 154.

Figure 174. Transparent Index Code for Bitmaps (TRANSPBMPIDX)Register

31	16
Reserved	
R-0	

15	8	7	0
BMP1		BMP0	
R/W-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 154. Transparent Index Code for Bitmaps (TRANSPBMPIDX) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved
15-8	BMP1	0-FFh	OSD bitmap 1 transparent value. Bitmap value for transparent color for 1/2/4/8-bit modes of bitmap window 1. Any pixel matching the value configured here is treated as transparent. The pixel is blended to the window in back plane with blend factor configured as global value of bitmap window 1. Note: The bit width specified here must match the bit depth configured for the window (example): • 1-bit bitmap mode, bit[0] is evaluated • 2-bit bitmap mode, bits[1:0] are evaluated • 4-bit bitmap mode, bits[3:0] are evaluated
7-0	BMP0	0-FFh	OSD bitmap 0 transparent value. Bitmap value for transparent color for 1/2/4/8-bit modes of bitmap window 0. Any pixel matching the value configured here is treated as transparent. The pixel is blended to the window in back plane with blend factor configured as global value of bitmap window 0. Note: The bit width specified here must match the bit depth configured for the window (example): • 1-bit bitmap mode, bit[0] is evaluated • 2-bit bitmap mode, bits[1:0] are evaluated • 4-bit bitmap mode, bits[3:0] are evaluated

6.3 Video Encoder (VENC) Registers

Table 155 lists the memory-mapped registers for the video encoder (VENC). For the memory address of these registers, see the device-specific data manual.

Table 155. Video Encoder (VENC) Registers

Offset	Acronym	Register Description	Section
0h	VMOD	Video Mode	Section 6.3.1
4h	VIOCTL	Video Interface I/O Control	Section 6.3.2
8h	VDPRO	Video Data Processing	Section 6.3.3
Ch	SYNCCTL	Sync Control	Section 6.3.4
10h	HSPLS	Horizontal Sync Pulse Width	Section 6.3.5
14h	VSPLS	Vertical Sync Pulse Width	Section 6.3.6
18h	HINTVL	Horizontal Interval	Section 6.3.7
1Ch	HSTART	Horizontal Valid Data Start Position	Section 6.3.8
20h	HVALID	Horizontal Data Valid Range	Section 6.3.9
24h	VINTVL	Vertical Interval	Section 6.3.10
28h	VSTART	Vertical Valid Data Start Position	Section 6.3.11
2Ch	VVALID	Vertical Data Valid Range	Section 6.3.12
30h	HSDLY	Horizontal Sync Delay	Section 6.3.13
34h	VSDLY	Vertical Sync Delay	Section 6.3.14
38h	YCCCTL	YCbCr Control	Section 6.3.15
3Ch	RGBCTL	RGB Control	Section 6.3.16
40h	RGBCLP	RGB Level Clipping	Section 6.3.17
44h	LINECTL	Line ID Control	Section 6.3.18
48h	CULLLINE	Culling Line Control	Section 6.3.19
4Ch	LCDOUT	LCD Output Signal Control	Section 6.3.20
50h	BRT0	Brightness Start Position Signal Control	Section 6.3.21
54h	BRT1	Brightness Width Signal Control	Section 6.3.22
58h	ACCTL	LCD_AC Signal Control	Section 6.3.23
5Ch	PWM0	PWM Output Period	Section 6.3.24
60h	PWM1	PWM Output Pulse Width	Section 6.3.25
64h	DCLKCTL	DCLK Control	Section 6.3.26
68h	DCLKPTN0	DCLK Pattern 0	Section 6.3.27
6Ch	DCLKPTN1	DCLK Pattern 1	Section 6.3.28
70h	DCLKPTN2	DCLK Pattern 2	Section 6.3.29
74h	DCLKPTN3	DCLK Pattern 3	Section 6.3.30
78h	DCLKPTN0A	DCLK Auxiliary Pattern 0	Section 6.3.31
7Ch	DCLKPTN1A	DCLK Auxiliary Pattern 1	Section 6.3.32
80h	DCLKPTN2A	DCLK Auxiliary Pattern 2	Section 6.3.33
84h	DCLKPTN3A	DCLK Auxiliary Pattern 3	Section 6.3.34
88h	DCLKHSTT	Horizontal DCLK Mask Start Position	Section 6.3.35
8Ch	DCLKHSTTA	Horizontal Auxiliary DCLK Mask Start Position	Section 6.3.36
90h	DCLKHVLD	Horizontal DCLK Mask Range	Section 6.3.37
94h	DCLKVSTT	Vertical DCLK Mask Start Position	Section 6.3.38
98h	DCLKVVLD	Vertical DCLK Mask Range	Section 6.3.39
9Ch	CAPCTL	Closed Caption Control	Section 6.3.40
A0h	CAPDO	Closed Caption Odd Field Data	Section 6.3.41
A4h	CAPDE	Closed Caption Even Field Data	Section 6.3.42
A8h	ATR0	Video Attribute Data 0	Section 6.3.43
ACh	ATR1	Video Attribute Data 1	Section 6.3.44

Table 155. Video Encoder (VENC) Registers (continued)

Offset	Acronym	Register Description	Section
B0h	ATR2	Video Attribute Data 2	Section 6.3.45
B4h	RSV0	Reserved 0	Section 6.3.46
B8h	VSTAT	Video Status	Section 6.3.47
BCh	RAMADR	GCP/FRC Table RAM Address	Section 6.3.48
C0h	RAMPORT	GCP/FRC Table RAM Data Port	Section 6.3.49
C4h	DACTST	DAC Test	Section 6.3.50
C8h	YCOLVL	YOUT and COUT Levels	Section 6.3.51
CCh	SCPROG	Sub-Carrier Programming	Section 6.3.52
D0h	RSV1	Reserved 1	Section 6.3.53
D4h	RSV2	Reserved 2	Section 6.3.54
D8h	RSV3	Reserved 3	Section 6.3.55
DCh	CVBS	Composite Mode	Section 6.3.56
E0h	CMPNT	Component Mode	Section 6.3.57
E4h	ETMG0	CVBS Timing Control 0	Section 6.3.58
E8h	ETMG1	CVBS Timing Control 1	Section 6.3.59
ECh	ETMG2	CVBS Timing Control 2	Section 6.3.60
F0h	ETMG3	CVBS Timing Control 3	Section 6.3.61
F4h	DACSEL	DAC Output Select	Section 6.3.62
100h	ARGBX0	Analog RGB Matrix 0	Section 6.3.63
104h	ARGBX1	Analog RGB Matrix 1	Section 6.3.64
108h	ARGBX2	Analog RGB Matrix 2	Section 6.3.65
10Ch	ARGBX3	Analog RGB Matrix 3	Section 6.3.66
110h	ARGBX4	Analog RGB Matrix 4	Section 6.3.67
114h	DRGBX0	Digital RGB Matrix 0	Section 6.3.68
118h	DRGBX1	Digital RGB Matrix 1	Section 6.3.69
11Ch	DRGBX2	Digital RGB Matrix 2	Section 6.3.70
120h	DRGBX3	Digital RGB Matrix 3	Section 6.3.71
124h	DRGBX4	Digital RGB Matrix 4	Section 6.3.72
128h	VSTARTA	Vertical Data Valid Start Position For Even Field	Section 6.3.73
12Ch	OSDCLK0	OSD Clock Control 0	Section 6.3.74
130h	OSDCLK1	OSD Clock Control 1	Section 6.3.75
134h	HVLDCL0	Horizontal Valid Culling Control 0	Section 6.3.76
138h	HVLDCL1	Horizontal Valid Culling Control 1	Section 6.3.77
13Ch	OSDHADV	OSD Horizontal Sync Advance	Section 6.3.78
140h	CLKCTL	Clock Control	Section 6.3.79
144h	GAMCTL	Enable Gamma Correction	Section 6.3.80
148h	VVALIDA	Vertical Data Valid Area For Even Field	Section 6.3.81
14Ch	BATR0	Video Attribute 0 For Type B Packet	Section 6.3.82
150h	BATR1	Video Attribute 1 For Type B Packet	Section 6.3.83
154h	BATR2	Video Attribute 2 For Type B Packet	Section 6.3.84
158h	BATR3	Video Attribute 3 For Type B Packet	Section 6.3.85
15Ch	BATR4	Video Attribute 4 For Type B Packet	Section 6.3.86
160h	BATR5	Video Attribute 5 For Type B Packet	Section 6.3.87
164h	BATR6	Video Attribute 6 For Type B Packet	Section 6.3.88
168h	BATR7	Video Attribute 7 For Type B Packet	Section 6.3.89
16Ch	BATR8	Video Attribute 8 For Type B Packet	Section 6.3.90
170h	DACAMP	Gain and Offset	Section 6.3.91

Table 155. Video Encoder (VENC) Registers (continued)

Offset	Acronym	Register Description	Section
174h	XHINTVL	Horizontal Interval Extension	Section 6.3.92

6.3.1 Video Mode (VMOD)

The video mode register is shown in Figure 175 and described in Table 156.

Figure 175. Video Mode (VMOD)

31	16
Reserved	
R-0	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved		VDMD		ITLCL	ITLC	NSIT	HDMD	TVTYP		SLAVE	VMD	BLNK	Rsvd	VIE	VENC
R-0		R/W-0		R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		R/W-0	R/W-0	R/W-0	R-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 156. Video Mode (VMOD) Field Descriptions

Bit	Field	Value	Description
31-14	Reserved	0	
13-12	VDMD		Digital video output mode.
		0	YCC16
		1	YCC8
		2	Parallel RGB
		3	Serial RGB
11	ITLCL		Non-interlace line number select. Effective in standard SDTV non-interlace mode (VMD=0, ITCL=1).
		0	262 line (NTSC)/312 line (PAL)
		1	263 line (NTSC)/313 line (PAL)
10	ITLC		Scan Mode. Effective in standard mode (VMD=0).
		0	Interlace
		1	Non-interlace
9	NSIT		Nonstandard interlace mode. Effective in non-standard mode (VMD=1).
		0	Progressive
		1	Interlace
8	HDMD		HDTV mode. Effective in standard mode (VMD=0)
		0	SDTV
		1	HDTV
7-6	TVTYP		TV Format Type Select. Effective in standard mode (VMD=0).
			SDTV mode (HDMD=0):
		0	NTSC
		1	PAL
		2	Reserved
		3	Reserved
			HDTV mode (HDMD=1):
		0	525P
		1	625P
		2	1080I
		3	720P
5	SLAVE		Master/slave select.
		0	Master mode
		1	Slave mode
4	VMD		Video timing.
		0	NTSC/PAL/HDTV timing
		1	Not NTSC/PAL/HDTV timing

Table 156. Video Mode (VMOD) Field Descriptions (continued)

Bit	Field	Value	Description
3	BLNK		Blanking enable.
		0	Normal
		1	Force Blanking
2	Reserved	0	Reserved
1	VIE		Composite output enable.
		0	Fixed L level output
		1	Normal composite output
0	VENC		Video encoder enable.
		0	Disable
		1	Enable

6.3.2 Video Interface I/O Control (VIOCTL)

The video interface I/O control register is shown in Figure 176 and described in Table 157.

Figure 176. Video Interface I/O Control (VIOCTL)

31															16
Reserved															
R-0															
15	14	13	12	11		9	8	7	6	5	4	3	2	1	0
Rsvd	VCLKP	VCLKE	VCLKZ	Reserved			SYDIR	Reserved		DOMD		YCSWAP	YCDC	Reserved	YCDIR
R-0	R/W-0	R/W-0	R/W-1	R-0			R/W-1	R-0		R/W-0		R/W-0	R/W-0	R-0	R/W-1

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 157. Video Interface I/O Control (VIOCTL) Field Descriptions

Bit	Field	Value	Description
31-15	Reserved	0	
14	VCLKP		VCLK output polarity.
		0	Non-inverse
		1	Inverse
13	VCLKE		VCLK output enable. Note: Set to 1 to output DCLK from VCLK pin. Note: When set to 0, VCLKP (polarity control) is still available.
		0	Off
		1	On
12	VCLKZ		VCLK pin output enable
		0	Output
		1	High Impedance
11-9	Reserved	0	Reserved
8	SYDIR		HSYNC/VSYNC pin I/O control.
		0	Output
		1	Input
7-6	Reserved	0	Reserved
5-4	DOMD		Digital data output mode.
		0	Normal output
		1	Inverse output
		2	L level output
		3	H level output
3	YCSWAP		Swaps YOUT/COUT pins. Interchanges the output data of YOUT and COUT
		0	Normal output
		1	Interchange YOUT and COUT
2	YCDC		YOUT/COUT pin DC output mode. Setting DC out option will output the value in the YCOLVL register on YOUT/COUT pins. Effective only when YOUT/COUT pin is set as output (YCDIR=0).
		0	Normal output
		1	DC level output
1	Reserved	0	Reserved
0	YCDIR		YOUT/COUT I/O Direction. Allows use of YOUT/COUT pins as data input pin for CCDC
		0	Output
		1	Input

6.3.3 Video Data Processing (VDPRO)

The video data processing register is shown in Figure 177 and described in Table 158.

Figure 177. Video Data Processing (VDPRO)

31															16
Reserved															
R-0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PFLTC		PFLTY		PFLTR	Rsvd	CBTYP	CBMD	DAFUL	ATRGB	ATYCC	ATCOM	Reserved		CUPS	YUPS
R/W-0		R/W-0		R/W-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0		R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 158. Video Data Processing (VDPRO) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved
15-14	PFLTC		C pre-filter select. Note: When PFLTR and PFLTY are set to 1, set PFLTY to 1 to adjust delay between Y and C.
		0	No filter
		1	1+1
		2	1+2+1
		3	Reserved
13-12	PFLTY		Y pre-filter select.
		0	No filter
		1	1+1
		2	1+2+1
		3	Reserved
11	PFLTR		Pre-filter sampling frequency.
		0	ENC clock/2
		1	ENC clock
10	Reserved	0	Reserved
9	CBTYP		Color-bar type.
		0	75%
		1	100%
8	CBMD		Color-bar mode.
		0	Normal output
		1	Color-bar output
7	DAFUL		DAC full-swing output.
		0	Normal output
		1	Full-swing output
6	ATRGB		Input video attenuation control for RGB.
		0	No Attenuation
		1	0-255 -> REC601 specified level
5	ATYCC		Input video attenuation control for YCbCr
		0	No Attenuation
		1	0-255 -> REC601 specified level
4	ATCOM		Input video attenuation control for composite.
		0	No Attenuation
		1	0-255 -> REC601 specified level
3-2	Reserved	0	Reserved
1	CUPS		Chroma signal up sampling enable.
		0	Off
		1	On

Table 158. Video Data Processing (VDPRO) Field Descriptions (continued)

Bit	Field	Value	Description
0	YUPS		Y signal up sampling enable.
		0	Off
		1	On

6.3.4 Sync Control (SYNCCTL)

The sync control register is shown in Figure 178 and described in Table 159.

Figure 178. Sync Control (SYNCCTL)

31	16
Reserved	
R-0	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Rsvd	OVD	EXFMD		EXFIV	EXSYNC	EXVIV	EXHIV	CSP	CSE	SYSW	VSYNCS	VPL	HPL	SYEV	SYEH
R-0	R/W-0	R/W-0		R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 159. Sync Control (SYNCCTL) Field Descriptions

Bit	Field	Value	Description
31-15	Reserved	0	Reserved
14	OVD		OSD vsync delay.
		0	Not delay
		1	Delay 0.5H
13-12	EXFMD		External field detection mode. Effective in slave operation (SLAVE=1).
		0	Latch external field at external vsync rise edge.
		1	Use raw external field
		2	Use external vsync as field ID
		3	Detect external vsync phase
11	EXFIV		External field input inversion. Effective in slave operation.
		0	Non-inverse
		1	Inverse
10	EXSYNC		External sync select. Effective in slave operation.
		0	HSYNC/VSYNC pin
		1	CCD sync signal
9	EXVIV		External vertical sync input polarity.
		0	Active H
		1	Active L
8	EXHIV		External horizontal sync input polarity.
		0	Active H
		1	Active L
7	CSP		Composite sync output polarity. Note: Specifies polarity of composite sync output from COUT3(B6) pin in YCC8 or RGB8 mode
		0	Active H
		1	Active L
6	CSE		Composite sync output enable. Note: Output control of composite sync signal from COUT3(B6) pin in YCC8 or RGB8 mode. Writing 1 activates output, and writing 0 outputs inactive level determined by CSP.
		0	Off
		1	On
5	SYSW		Output sync select. Note: Applicable to standard mode only. Setting to 1 in standard mode outputs the pulse width processed by the SYNCPLS register as output sync signal.
		0	Normal
		1	Sync pulse width processing mode

Table 159. Sync Control (SYNCCTL) Field Descriptions (continued)

Bit	Field	Value	Description
4	VSYNCS		VSYNC pin output signal select.
		0	Vertical sync signal
		1	Composite sync signal
3	VPL		Vertical sync output polarity.
		0	Active H
		1	Active L
2	HPL		Horizontal sync output polarity.
		0	Active H
		1	Active L
1	SYEV		Vertical sync output enable. The output comes to ON when this is set to 1, and the signal selected by the VSSW is output from VSYNC pin. Setting 0 outputs inactive level determined by VPL.
		0	Off
		1	On
0	SYEH		Horizontal sync output enable. The output comes to ON when this is set to 1, and the signal selected by the VSSW is output from HSYNC pin. Setting 0 outputs inactive level determined by HPL.
		0	Off
		1	On

6.3.5 Horizontal Sync Pulse Width (HSPLS)

The horizontal sync pulse width register is shown in Figure 179 and described in Table 160.

Figure 179. Horizontal Sync Pulse Width (HSPLS)

31	16
Reserved	
R-0	

15	13	12	0
Reserved		HSPLS	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 160. Horizontal Sync Pulse Width (HSPLS) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Reserved
12-0	HSPLS	0-1FFFh	Horizontal sync pulse width. Set the pulse width of horizontal sync output from HSYNC pin in ENC clock. Effective in non-standard mode, or sync processing mode (SYSW=1) in standard mode.

6.3.6 Vertical Sync Pulse Width (VSPLS)

The vertical sync pulse width register is shown in Figure 180 and described in Table 161.

Figure 180. Vertical Sync Pulse Width (VSPLS)

31	16
Reserved	
R-0	

15	13	12	0
Reserved		VSPLS	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

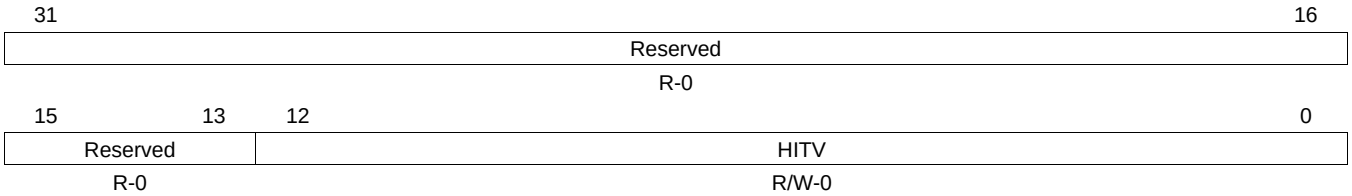
Table 161. Vertical Sync Pulse Width (VSPLS) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Reserved
12-0	VSPLS	0-1FFFh	Vertical sync pulse width. Set the pulse width of vertical sync output from VSYNC pin in lines. Effective in non-standard mode, or sync processing mode (SYSW=1) in standard mode.

6.3.7 Horizontal Interval (HINTVL)

The horizontal interval register is shown in Figure 181 and described in Table 162.

Figure 181. Horizontal Interval (HINTVL)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 162. Horizontal Interval (HINTVL) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Reserved
12-0	HINT	0-1FFFh	Horizontal interval. Effective in non-standard mode. Specify the number of ENC clocks. The interval is represented by HINT+1. If ENC clock/2 is used as OSD clock, ensure that even value is specified.

6.3.8 Horizontal Valid Data Start Position (HSTART)

The horizontal valid data start position register is shown in Figure 182 and described in Table 163.

Figure 182. Horizontal Valid Data Start Position (HSTART)

31	16
Reserved	
R-0	

15	13	12	0
Reserved		HSTART	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 163. Horizontal Valid Data Start Position (HSTART) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Reserved
12-0	HSTART	0-1FFFh	Horizontal data valid start position. Specify the number of ENC clocks from horizontal sync signal. LCD_OE rises at the position specified here and the data output starts.

6.3.9 Horizontal Data Valid Range (HVALID)

The horizontal data valid range register is shown in Figure 183 and described in Table 164.

Figure 183. Horizontal Data Valid Range (HVALID)

31	16
Reserved	
R-0	

15	13	12	0
Reserved		HVALID	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 164. Horizontal Data Valid Range (HVALID) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Reserved
12-0	HVALID	0-1FFFh	Horizontal data valid range. Specify the number of ENC clocks. LCD_OE is asserted during the period specified here and valid data is output. The data outside of valid range is output in L.

6.3.10 Vertical Interval (VINTVL)

The vertical interval register is shown in VENC_VINTVL_fig and described in Table 165.

Figure 184. Vertical Interval (VINTVL)

31-16
Reserved
R-0

15-13	12-0
Reserved	VITV
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 165. Vertical Interval (VINTVL) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved
12-0	VINT	0-1FFFh	Vertical interval. Effective in non-standard mode. Specify the number of lines. The interval is represented by VINT+1.

6.3.11 Vertical Valid Data Start Position (VSTART)

The vertical valid data start position register is shown in Figure 185 and described in Table 166.

Figure 185. Vertical Valid Data Start Position (VSTART)

31	16
Reserved	
R-0	

15	13	12	0
Reserved		VSTART	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

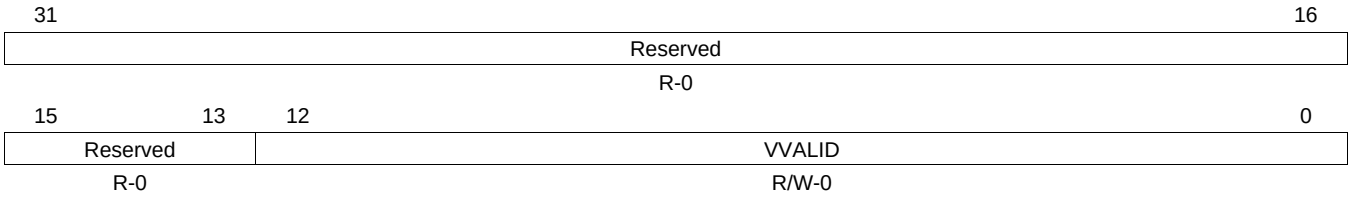
Table 166. Vertical Valid Data Start Position (VSTART) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Reserved
12-0	VSTART	0-1FFFh	Vertical valid data start position. Note: Specify number of lines.

6.3.12 Vertical Data Valid Range (VVALID)

The vertical data valid range register is shown in Figure 186 and described in Table 167.

Figure 186. Vertical Data Valid Range (VVALID)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 167. Vertical Data Valid Range (VVALID) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Reserved
12-0	VVALID	0-1FFFh	Vertical data valid range. Note: specify number of lines.

6.3.13 Horizontal Sync Delay (HSDLY)

The horizontal sync delay register is shown in Figure 187 and described in Table 168.

Figure 187. Horizontal Sync Delay (HSDLY)

31	16
Reserved	
R-0	

15	13	12	0
Reserved		HSDLY	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

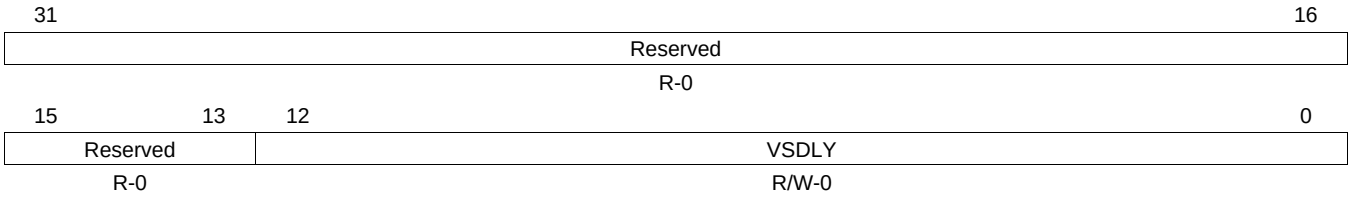
Table 168. Horizontal Sync Delay (HSDLY) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Reserved
12-0	HSDLY	0-1FFFh	Output delay of horizontal sync signal. This can delay horizontal sync output from HSYNC pin by ENC clock.

6.3.14 Vertical Sync Delay (VSDLY)

The vertical sync delay register is shown in Figure 188 and described in Table 169.

Figure 188. Vertical Sync Delay (VSDLY)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 169. Vertical Sync Delay (VSDLY) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Reserved
12-0	VSDLY	0-1FFFh	Output delay of vertical sync signal. Note: This will delay the VSYNC signal by ENC clock.

6.3.15 YCbCr Control (YCCCTL)

The YCbCr control register is shown in Figure 189 and described in Table 170.

Figure 189. YCbCr Control (YCCCTL)

31	16
Reserved	
R-0	

15	5	4	3	2	1	0
Reserved		CHM	YCP		FID656	R656
R-0		R/W-0	R/W-0		R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 170. YCbCr Control (YCCCTL) Field Descriptions

Bit	Field	Value	Description
31-5	Reserved	0	Reserved
4	CHM		Chroma output mode. Effective in YCC16/YCC8 Mode.
		0	Immediate sampling
		1	Latch at first pixel
3-2	YCP		YC output order. Operation varies depending on the mode.
		0	YCC16 mode - CbCr
		1	YCC16 mode - CrCb
		0	YCC8 mode - Cb-Y-Cr-Y
		1	YCC8 mode - Y-Cr-Y-Cb
		2	YCC8 mode - Cr-Y-Cb-Y
		3	YCC8 mode - Y-Cb-Y-Cr
1	FID656		Field toggle position. Effective in REC656 mode for interface. It switches the field ID toggle position for even field of interlace video. 0.5H before or 0.5H after VSYNC can be chosen.
		0	
		1	
0	R656		REC656 mode. This is ITU_R BT.656 format and is effective when the OSD clock runs at ENC clock/2.
		0	Normal
		1	REC656 mode

6.3.16 RGB Control (RGBCTL)

The RGB control register is shown in Figure 190 and described in Table 171.

Figure 190. RGB Control (RGBCTL)

31															16
Reserved															
R-0															
15	14	13	12	11	10	9	8	7	6			4	3	2	0
RGBLAT	Rsvd	IRSWP	IR9	IRONM	DFLTR	DFLTS		Rsvd	RGBEF				Rsvd	RGBOF	
R/W-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		R-0	R/W-0				R-0	R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 171. RGB Control (RGBCTL) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved
15	RGBLAT		RGB latch setting. Set 1 to latch and output the data input in serial RGB output. This is set when data with the same pixel are output serially.
		0	Normal output
		1	Latch mode
14	Reserved	0	Reserved
13	IRSWP		Swap order of data output in IronMan mode. Effective only IRONM=1.
		0	Normal
		1	Data swap
12	IR9		IronMan 9-bit mode. Effective only IRONM=1. When 1, 24-bit RGB data (upper 6_bits of each color) is serially output on 9_bit data bus. The output format of the first is R[7:2] and G[7:5] and the second is G[4:2] and B[7:2]. This order can be swapped by IRSWP register.
		0	8-bit
		1	9-bit
11	IRONM		IronMan type RGB output. Effective in SRGB mode.
		0	Normal
		1	Iron-man type
10	DFLTR		RGB LPF sampling frequency. Note: Effective in all digital modes with RGB output.
		0	ENC clock/2
		1	ENC clock
9-8	DFLTS		RGB LPF select. Note: Effective in all digital modes with RGB output.
		0	No filter
		1	3-Tap: 1+2+1
		2	7-Tap: 1+2+3+4+3+2+1
		3	Reserved
7	Reserved	0	Reserved

Table 171. RGB Control (RGBCTL) Field Descriptions (continued)

Bit	Field	Value	Description
6-4	RGBEF		RGB output order for even fields (Line ID = 1). Note: Effective in Serial RGB mode. The line ID at RGBCL=1 represents the culling line ID set in the CULLLINE register. At RGBCL=0, it represents normal line ID.
		0	R0-G1-B2
		1	R0-B1-G2
		2	G0-R1-B2
		3	G0-B1-R2
		4	B0-R1-G2
		5	B0-G1-R2
		6	Reserved
		7	Reserved
3	Reserved	0	Reserved
2-0	RGBOF		RGB output order for odd fields (Line ID = 0). Note: Effective in Serial RGB mode. The line ID at RGBCL=1 represents the culling line ID set in the CULLLINE register. At RGBCL=0, it represents normal line ID.
		0	R0-G1-B2
		1	R0-B1-G2
		2	G0-R1-B2
		3	G0-B1-R2
		4	B0-R1-G2
		5	B0-G1-R2
		6	Reserved
		7	Reserved

6.3.17 RGB Level Clipping (RGBCLP)

The RGB level clipping register is shown in Figure 191 and described in Table 172.

Figure 191. RGB Level Clipping (RGBCLP)

31	16
Reserved	
R-0	

15	8	7	0
UCLIP		OFST	
R/W-255		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 172. RGB Level Clipping (RGBCLP) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	
15-8	UCLIP	0-FFh	Upper clip level for RGB output. Note: Effective in all digital output modes with RGB output. Clipping is done following offset addition.
7-0	ROFST	0-FFh	Offset level for RGB output. Note: Effective in all digital output modes with RGB output. Offset specified here can be added to RGB converted from YCbCr.

6.3.18 Line ID Control (LINECTL)

The line ID control register is shown in Figure 192 and described in Table 173.

Figure 192. Line ID Control (LINECTL)

31															16
Reserved															
R-0															
15	14	13	12	11	10		8	7	6	5	4	3	2	1	0
EXIDP	EXIDE	Rsvd	VVLDF	VSTF	VCLID			VCLRD	VCL56	HLDF	HLDL	LINID	DCKCLP	DCKCLI	RGBCL
R/W-0	R/W-0	R-0	R/W-0	R/W-0	R/W-0			R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 173. Line ID Control (LINECTL) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved
15	EXIDP		External line ID signal input polarity. Effective at EXLID=1.
		0	Non-inverse
		1	Inverse
14	EXIDE		External line ID signal input mode.
		0	To use internal line ID
		1	To use external line ID
13	Reserved	0	Reserved
12	VVLDF		Vertical data valid range field mode.
		0	Normal mode
		1	Field mode
11	VSTF		Vertical data valid start position field mode.
		0	Normal mode
		1	Field mode
10-8	VCLID	0	Vertical culling line position. Specifies which line will be culled of every six lines. No culling will be applied when VCLID is greater than 5. This bit is effective when VCL56=1.
7	VCLRD		Vertical culling counter reset mode. When 0, the counter for vertical culling is reset to zero at vertical sync. When 1, it is reset to a random value at vertical sync. This bit is effective when VCL56=1.
		0	Reset to 0
		1	Reset to random value
6	VCL56		Digital output vertical culling. Enabling discards one line of video output every six lines. This can be used to output NTSC valid lines with PAL timing.
		0	No culling
		1	5/6 culling
5	HLDF		Digital output field hold. Note: Effective in non-standard mode. Enabling suspends the video output when current field output is completed. Reading the data from OSD is suspended during this period and the output of sync signal and video data are also suspended. Setting to 0 restarts output.
		0	Normal
		1	Output hold
4	HLDL		Digital output line hold. Note: Effective in non-standard mode. Enabling suspends the video output when current line output is completed. Reading the data from OSD is suspended during this period and the output of sync signal and video data are also suspended. Setting to 0 restarts output.
		0	Normal
		1	Output hold

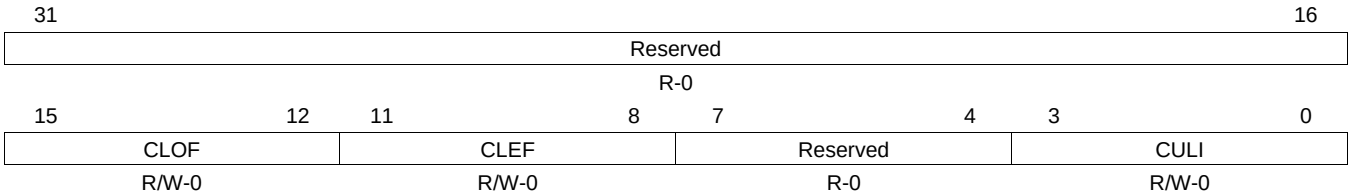
Table 173. Line ID Control (LINECTL) Field Descriptions (continued)

Bit	Field	Value	Description
3	LINID		Start line ID control in even field.
		0	Line ID=0
		1	Line ID=1
2	DCKCLP		DCLK pattern switching by culling line ID. When this is enabled, the DCLK pattern can be switched according to the culling line ID set by the CULLLINE register. The DCLK pattern on each line is specified by the DCLKPTN and DCLKPTNA registers.
		0	Off
		1	On
1	DCKCLI		DCLK polarity inversion by culling line ID. When this is disabled, the DCLK polarity is fixed anytime as specified by the VCLKP register. Enabling inverts this polarity according to the culling line ID set by the CULLLINE register.
		0	Off
		1	On
0	RGBCL		RGB output order switching by culling line ID. Disabling switches RGB output order every line. Enabling switches this order according to the XORed signal of the line ID and the culling line ID set by the CULLLINE register. The output order on each on each line is specified by RGBOF and RGBEF in the RGBCTL register.
		0	Off
		1	On

6.3.19 Culling Line Control (CULLLINE)

The culling line control register is shown in Figure 193 and described in Table 174.

Figure 193. Culling Line Control (CULLLINE)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 174. Culling Line Control (CULLLINE) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	
15-12	CLOF	0-Fh	Culling line ID toggle position (odd field). Specify toggle line numbers of culling line ID in odd field.
11-8	CLEF	0-Fh	Culling line ID toggle position (even field). Specify the culling line ID toggle position in even field.
7-4	Reserved	0-Fh	Reserved
3-0	CULI	0-Fh	Culling line ID inversion interval. This is set by line. The interval is represented by CULI+1.

6.3.20 LCD Output Signal Control (LCDOUT)

The LCD output signal control register is shown in Figure 194 and described in Table 175.

Figure 194. LCD Output Signal Control (LCDOUT)

31	16
Reserved	
R-0	

15	9	8	7	6	5	4	3	2	1	0
Reserved		OES	FIDP	PWMP	PWME	ACE	BRP	BRE	OEP	OEE
R-0		R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

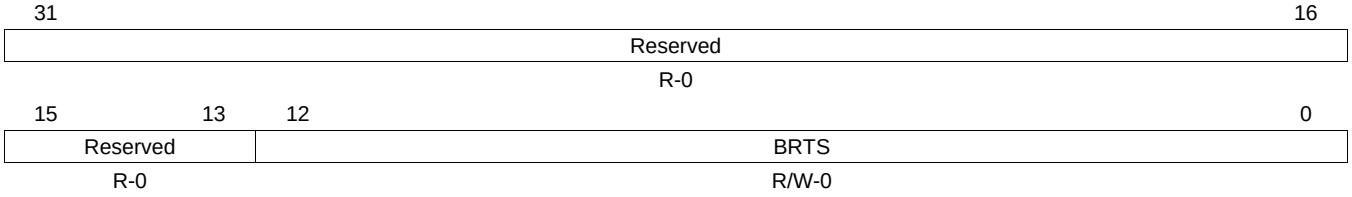
Table 175. LCD Output Signal Control (LCDOUT) Field Descriptions

Bit	Field	Value	Description
31-9	Reserved	0	Reserved
8	OES		Output enable signal selection. Maps LCD_OE or BRIGHT to alternate output (GIO71) Must also configure this output in SYS.PINMUX1.DLCD.
		0	LCD Output Enable signal
		1	Bright signal
7	FIDP		Field ID output polarity.
		0	Non-inverse
		1	Inverse
6	PWMP		PWM output pulse polarity.
		0	Active H
		1	Active L
5	PWME		PWM output control enable. Effective when digital output mode with PWM output is selected. PWM is output on COUT4 signal (i.e., use only in Serial RGB or YCC8 modes).
		0	Off
		1	On
4	ACE		LCD_AC output control enable. LCD_AC is output on COUT7 signal (i.e., use only in Serial RGB or YCC8 modes).
		0	Off
		1	On
3	BRP		Bright output polarity.
		0	Active H
		1	Active L
2	BRE		Bright output control enable. BRIGHT is output on COUT5 signal (i.e., use only in Serial RGB or YCC8 modes).
		0	Off
		1	On
1	OEP		LCD_OE output polarity.
		0	Active H
		1	Active L
0	OEE		LCD_OE output control enable. LCD_OE is output on COUT6 signal (i.e., use only in Serial RGB or YCC8 modes).
		0	Off
		1	On

6.3.21 Brightness Start Position Signal Control (BRT0)

The brightness start position signal control register is shown in Figure 195 and described in Table 176.

Figure 195. Brightness Start Position Signal Control (BRT0)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 176. Brightness Start Position Signal Control (BRT0) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Reserved
12-0	BRTS	0-1FFFh	Bright pulse start position. Specify the number of ENC cycles from HSYNC signal.

6.3.22 Brightness Width Signal Control (BRT1)

The brightness width signal control register is shown in Figure 196 and described in Table 177.

Figure 196. Brightness Width Signal Control (BRT1)

31	16
Reserved	
R-0	

15	13	12	0
Reserved		BRTW	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 177. Brightness Width Signal Control (BRT1) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Reserved
12-0	BRTW	0-1FFFh	Bright pulse width. Specify the number of ENC cycles.

6.3.23 LCD_AC Signal Control (ACCTL)

The LCD_AC signal control register is shown in Figure 197 and described in Table 178.

Figure 197. LCD_AC Signal Control (ACCTL)

31	16
Reserved	
R-0	

15	13	12	0
ACTF		ACTH	
R/W-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

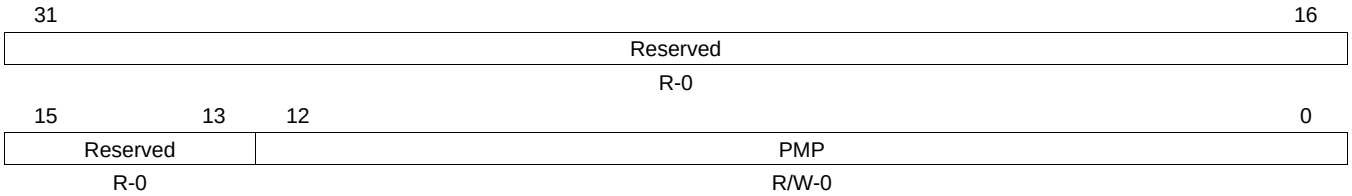
Table 178. LCD_AC Signal Control (ACCTL) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	
15-13	ACTF	0-7h	LCD_AC toggle interval. Note: LCD_AC is toggled every field specified here.
12-0	ACTH	0-1FFFh	LCD_AC toggle horizontal position. Note: LCD_AC is toggled by the number of ENC clocks from the rising edge of horizontal sync signal.

6.3.24 PWM Output Period (PWM0)

The PWM output period register is shown in Figure 198 and described in Table 179.

Figure 198. PWM Output Period (PWM0)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

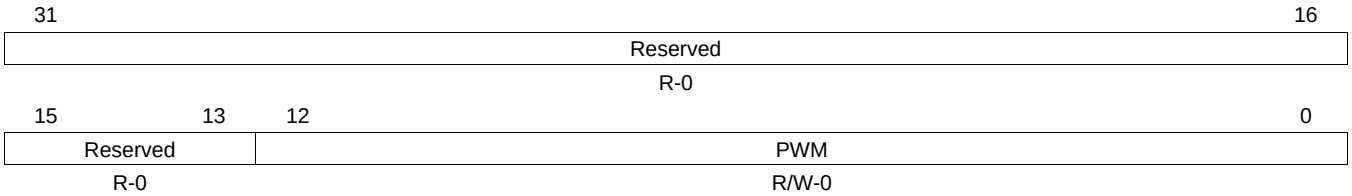
Table 179. PWM Output Period (PWM0) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Reserved
12-0	PMP	0-1FFFh	PWM output period. Specify the number of ENC clocks. Period is PMP + 1.

6.3.25 PWM Output Pulse Width (PWM1)

The PWM output pulse width register is shown in Figure 199 and described in Table 180.

Figure 199. PWM Output Pulse Width (PWM1)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 180. PWM Output Pulse Width (PWM1) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Reserved
12-0	PWM	0-1FFFh	PWM output pulse width. Specify the H pulse width by ENC clock. Setting to 0 makes PWM output L level always; setting bigger value than PMP sets to H level always.

6.3.26 DCLK Control (DCLKCTL)

The DCLK control register is shown in Figure 200 and described in Table 181.

Figure 200. DCLK Control (DCLKCTL)

31										16
Reserved										
R-0										
15	14	13-12	11	10	9	8	7	6	5	0
DCKIM	Rsvd	DOFST	DCKEC	DCKME	DCKOH	DCKIH	Reserved		DCKPW	
R/W-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 181. DCLK Control (DCLKCTL) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved
15	DCKIM		DCLK internal mode. When enabled, a different pattern can be specified for internal DCLK from output DCLK. In this mode, DCLKPTN0A-PCLKPTN3A and DCLKHSTTA are used to specify the internal DCLK pattern and its pattern valid bit width respectively. The DCLK pattern switching by culling line ID (DCKCLP=1) is no longer available in this mode.
		0	
		1	
14	Reserved	0	Reserved
13-12	DOFST		DCLK output offset. Adjust the DCLK delay output from VCLK pin by ENC clock. When DCLK output is configured as ENC clock gating with DCKEC=1 and DCKOH=0, these bits have no meaning.
		0	0
		1	-0.5
		2	0.5
		3	1
11	DCKEC		DCLK pattern mode. When 0, the specified value in DCLKPTN (or DCLKPTNA); register becomes the clock level of DCLK. When 1, DCLKPTN works as the clock enable for ENC clock.
		0	Level
		1	Enable
10	DCKME		DCLK mask enable. Masks are specified by the DCLKHSTT, DCLKHVLD, DCLKVSTT and DCLKVVLD registers. Enabling represents the mask is ON and outputs the clock in specified valid area. Disabling represents the mask is OFF and directly outputs the DCLK.
		0	Off
		1	On
9	DCKOH		DCLK output divide control. Enabling divides the clock by two and outputs it from VCLK pin. RGB data is output by the rising of internal DCLK and only divided clock output is output. Thus, this can be used to connect to the LCD that captures the data using both edges of DCLK.
		0	Divide by 1
		1	Divide by 2
8	DCKIH		Internal DCLK divide control. Enabling divides internal DCLK clock by two. When the clock output is divided by 1 (DCKOH=0), two clocks can be output per one data. Thus, this can be used to connect to the LCD that requires double clock frequency of data rate.
		0	Divide by 1
		1	Divide by 2
7-6	Reserved	0	Reserved
5-0	DCKPW	0-3Fh	DCLK pattern valid bit width. Note: Set the width of valid bits among all 64 bits in the DCLKPTN0-3 registers.

6.3.27 DCLK Pattern 0 (DCLKPTN0)

The DCLK pattern 0 register is shown in Figure 201 and described in Table 182.

Figure 201. DCLK Pattern 0 (DCLKPTN0)

31	16
Reserved	
R-0	
15	0
DCPTN0	
R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 182. DCLK Pattern 0 (DCLKPTN0) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved
15-0	DCPTN0	0-FFFFh	DCLK pattern (DCPT[15:0]). The specified bit pattern is output in resolution of ENC clock units When DCLK pattern switching mode (DCKCLP=1), it works only for the line with the culling line ID 0.

6.3.28 DCLK Pattern 1 (DCLKPTN1)

The DCLK pattern 1 register is shown in Figure 202 and described in Table 183.

Figure 202. DCLK Pattern 1 (DCLKPTN1)

31	16
Reserved	
R-0	

15	0
DCPTN1	
R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 183. DCLK Pattern 1 (DCLKPTN1) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved
15-0	DCPTN1	0-FFFFh	DCLK pattern (DCPT[31:16]). The specified bit pattern is output in resolution of ENC clock units When DCLK pattern switching mode (DCKCLP=1), it works only for the line with the culling line ID 0.

6.3.29 DCLK Pattern 2 (DCLKPTN2)

The DCLK pattern 2 register is shown in Figure 203 and described in Table 184.

Figure 203. DCLK Pattern 2 (DCLKPTN2)

31	16
Reserved	
R-0	

15	0
DCPTN2	
R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 184. DCLK Pattern 2 (DCLKPTN2) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved
15-0	DCPTN2	0-FFFFh	DCLK pattern (DCPT[47:32]). The specified bit pattern is output in resolution of ENC clock units When DCLK pattern switching mode (DCKCLP=1), it works only for the line with the culling line ID 0.

6.3.30 DCLK Pattern 3 (DCLKPTN3)

The DCLK pattern 3 register is shown in Figure 204 and described in Table 185.

Figure 204. DCLK Pattern 3 (DCLKPTN3)

31	16
Reserved	
R-0	

15	0
DCPTN3	
R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 185. DCLK Pattern 3 (DCLKPTN3) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved
15-0	DCPTN3	0-FFFFh	DCLK pattern (DCPT[63:48]). The specified bit pattern is output in resolution of ENC clock units When DCLK pattern switching mode (DCKCLP=1), it works only for the line with the culling line ID 0.

6.3.31 DCLK Auxiliary Pattern 0 (DCLKPTN0A)

The DCLK auxiliary pattern 0 register is shown in Figure 205 and described in Table 186.

Figure 205. DCLK Auxiliary Pattern 0 (DCLKPTN0A)

31	16
Reserved	
R-0	
15	0
DCPTN0A	
R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 186. DCLK Auxiliary Pattern 0 (DCLKPTN0A) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved
15-0	DCPTN0A	0-FFFFh	DCLK auxiliary pattern (DCPT[15:0]). The specified bit pattern is output in resolution of ENC clock units Specifies the DCLK pattern for the culling line ID 1 in DCLK pattern switching mode (DCKCLP=1). No meaning when DCKCLP=0.

6.3.32 DCLK Auxiliary Pattern 1 (DCLKPTN1A)

The DCLK auxiliary pattern 1 register is shown in Figure 206 and described in Table 187.

Figure 206. DCLK Auxiliary Pattern 1 (DCLKPTN1A)

31	16
Reserved	
R-0	
15	0
DCPTN1A	
R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 187. DCLK Auxiliary Pattern 1 (DCLKPTN1A) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved
15-0	DCPTN1A	0-FFFFh	DCLK auxiliary pattern (DCPT[31:16]). The specified bit pattern is output in resolution of ENC clock units Specifies the DCLK pattern for the culling line ID 1 in DCLK pattern switching mode (DCKCLP=1). No meaning when DCKCLP=0.

6.3.33 DCLK Auxiliary Pattern 2 (DCLKPTN2A)

The DCLK auxiliary pattern 2 register is shown in Figure 207 and described in Table 188.

Figure 207. DCLK Auxiliary Pattern 2 (DCLKPTN2A)

31	16
Reserved	
R-0	
15-0	0
DCPTN2A	
R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 188. DCLK Auxiliary Pattern 2 (DCLKPTN2A) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved
15-0	DCPTN2A	0-FFFFh	DCLK auxiliary pattern (DCPT[47:32]). The specified bit pattern is output in resolution of ENC clock units Specifies the DCLK pattern for the culling line ID 1 in DCLK pattern switching mode (DCKCLP=1). No meaning when DCKCLP=0.

6.3.34 DCLK Auxiliary Pattern 3 (DCLKPTN3A)

The DCLK auxiliary pattern 3 register is shown in Figure 208 and described in Table 189.

Figure 208. DCLK Auxiliary Pattern 3 (DCLKPTN3A)

31	16
Reserved	
R-0	
15-0	0
DCPTN3A	
R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 189. DCLK Auxiliary Pattern 3 (DCLKPTN3A) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved
15-0	DCPTN3A	0-FFFFh	DCLK auxiliary pattern (DCPT[63:48]). The specified bit pattern is output in resolution of ENC clock units Specifies the DCLK pattern for the culling line ID 1 in DCLK pattern switching mode (DCKCLP=1). No meaning when DCKCLP=0.

6.3.35 Horizontal DCLK Mask Start Position (DCLKHSTT)

The horizontal DCLK mask start position register is shown in Figure 209 and described in Table 190.

Figure 209. Horizontal DCLK Mask Start Position (DCLKHSTT)

31	16
Reserved	
R-0	

15	13	12	0
Reserved		DHS	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 190. Horizontal DCLK Mask Start Position (DCLKHSTT) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Reserved
12-0	DHS	0-1FFFh	Horizontal DCLK mask start position. Specified in number of ENC clocks from start of the horizontal sync signal.

6.3.36 Horizontal Auxiliary DCLK Mask Start Position (DCLKHSTTA)

The horizontal auxiliary DCLK mask start position register is shown in Figure 210 and described in Table 191.

Figure 210. Horizontal Auxiliary DCLK Mask Start Position (DCLKHSTTA)

31	16
Reserved	
R-0	

15	13	12	0
Reserved		DHSA	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

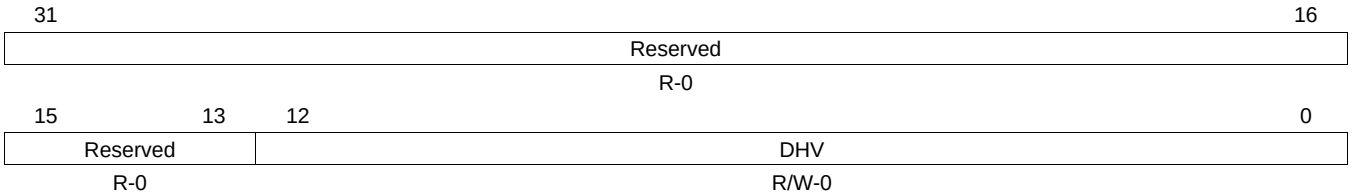
Table 191. Horizontal Auxiliary DCLK Mask Start Position (DCLKHSTTA) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Reserved
12-0	DHSA	0-1FFFh	Horizontal DCLK (auxiliary) mask start position. Specified in number of ENC clocks from start of the horizontal sync signal.

6.3.37 Horizontal DCLK Mask Range (DCLKHVLD)

The horizontal DCLK mask range register is shown in Figure 211 and described in Table 192.

Figure 211. Horizontal DCLK Mask Range (DCLKHVLD)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

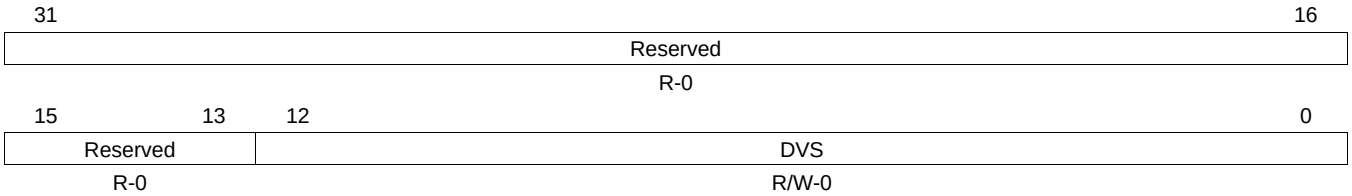
Table 192. Horizontal DCLK Mask Range (DCLKHVLD) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Reserved
12-0	DHV	0-1FFFh	Horizontal DCLK mask range. Specified in ENC clocks.

6.3.38 Vertical DCLK Mask Start Position (DCLKVSTT)

The vertical DCLK mask start position register is shown in Figure 212 and described in Table 193.

Figure 212. Vertical DCLK Mask Start Position (DCLKVSTT)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

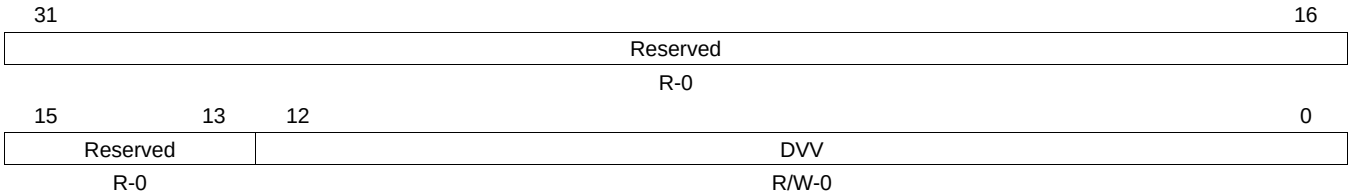
Table 193. Vertical DCLK Mask Start Position (DCLKVSTT) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Reserved
12-0	DVS	0-1FFFh	DCLK vertical mask start position. Specified in lines from vertical sync signal.

6.3.39 Vertical DCLK Mask Range (DCLKVVLD)

The vertical DCLK mask range register is shown in Figure 213 and described in Table 194.

Figure 213. Vertical DCLK Mask Range (DCLKVVLD)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 194. Vertical DCLK Mask Range (DCLKVVLD) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Reserved
12-0	DVV	0-1FFFh	DCLK vertical mask range. Specified in number of lines.

6.3.40 Closed-Caption Control (CAPCTL)

The closed-caption control register is shown in Figure 214 and described in Table 195.

Figure 214. Closed-Caption Control (CAPCTL)

31	16
Reserved	
R-0	

15	14	8	7	2	1	0
Rsvd	CADF		Reserved		CAPF	
R-0	R/W-0		R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 195. Closed-Caption Control (CAPCTL) Field Descriptions

Bit	Field	Value	Description
31-15	Reserved	0	Reserved
14-8	CADF	0-7Fh	Closed-caption default data register. When the caption data register (CAPDO or CAPDE) is not updated before the caption data transmission timing for the corresponding field, the ASCII code specified by this register is automatically transmitted for closed caption data.
7-2	Reserved	0	Reserved
1-0	CAPF		Closed-caption field select.
		0	No data output
		1	Even field
		2	Odd field
		3	Both fields

6.3.41 Closed-Caption Odd Field Data (CAPDO)

The closed-caption odd field data register is shown in Figure 215 and described in Table 196.

Figure 215. Closed-Caption Odd Field Data (CAPDO)

31	16
Reserved	
R-0	

15	14	8	7	6	0
Rsvd	CADO0		Rsvd	CADO1	
R-0	R/W-0		R-0	R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 196. Closed-Caption Odd Field Data (CAPDO) Field Descriptions

Bit	Field	Value	Description
31-15	Reserved	0	Reserved
14-8	CADO0	0-7Fh	Closed-caption default data 0 (odd field). Specify the ASCII code of the 1st byte to be transmitted in closed captioning for odd field. Parity bit is automatically calculated.
7	Reserved	0	Reserved
6-0	CADO1	0-7Fh	Closed-caption default data 1 (odd field). Specify the ASCII code of the 2nd byte to be transmitted in closed captioning for odd field. Parity bit is automatically calculated.

6.3.42 Closed-Caption Even Field Data (CAPDE)

The closed-caption even field data register is shown in Figure 216 and described in Table 197.

Figure 216. Closed-Caption Even Field Data (CAPDE)

31	16
Reserved	
R-0	

15	14	8	7	6	0
Rsvd	CADE0		Rsvd	CADE1	
R-0	R/W-0		R-0	R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 197. Closed-Caption Even Field Data (CAPDE) Field Descriptions

Bit	Field	Value	Description
31-15	Reserved	0	Reserved
14-8	CADE0	0-7Fh	Closed-caption default data 0 (even field). Specify the ASCII code of the 1st byte to be transmitted in closed captioning for odd field. Parity bit is automatically calculated.
7	Reserved	0	Reserved
6-0	CADE1	0-7Fh	Closed-caption default data 1 (even field). Specify the ASCII code of the 2nd byte to be transmitted in closed captioning for odd field. Parity bit is automatically calculated.

6.3.43 Video Attribute Data 0 (ATR0)

The video attribute data 0 register is shown in Figure 217 and described in Table 198.

Figure 217. Video Attribute Data 0 (ATR0)

31	16
Reserved	
R-0	

15	8	7	0
Reserved		ATR0	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 198. Video Attribute Data 0 (ATR0) Field Descriptions

Bit	Field	Value	Description
31-8	Reserved	0	Reserved
7-0	ATR0	0-FFh	Video attribute data register 0. NTSC - Set the WORD0 and WORD1 data: • Bit 7-6 is unused • Bit 5-2 is WORD1 • Bit 1-0 is WORD0 PAL - not used

6.3.44 Video Attribute Data 1 (ATR1)

The video attribute data 1 register is shown in Figure 218 and described in Table 199.

Figure 218. Video Attribute Data 1 (ATR1)

31	16
Reserved	
R-0	

15	8	7	0
Reserved		ATR1	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

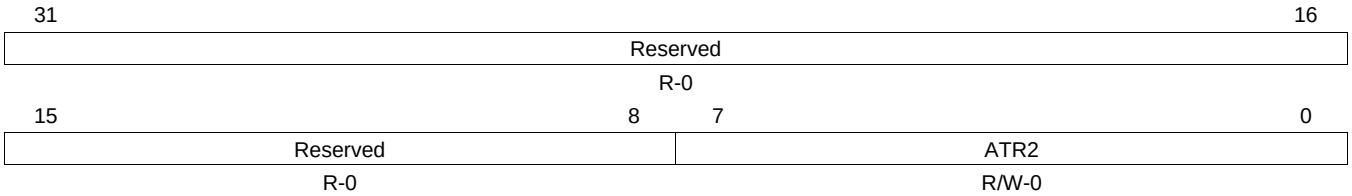
Table 199. Video Attribute Data 1 (ATR1) Field Descriptions

Bit	Field	Value	Description
31-8	Reserved	0	Reserved
7-0	ATR1	0-FFh	Video attribute data register 1. NTSC - Set the WORD2 data: • Bit 7-4 is WORD2 PAL - Set the GROUP1 and GROUP2 data: • Bit 7-4 is GROUP2 • Bit 3-0 is GROUP1

6.3.45 Video Attribute Data 2 (ATR2)

The video attribute data 2 register is shown in Figure 219 and described in Table 200.

Figure 219. Video Attribute Data 2 (ATR2)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 200. Video Attribute Data 2 (ATR2) Field Descriptions

Bit	Field	Value	Description
31-8	Reserved	0	Reserved
7-0	ATR2	0-FFh	Video attribute data register 2. NTSC - Set CRC data and enable attribute insertion: • Bit 7 is ATR_EN • Bit 6 is unused • Bit 5-0 is CRC PAL - Set GROUP3 and GROUP4 data and enable attribute insertion: • Bit 7 is ATR_EN • Bit 6 is ununsed • Bit 5-3 is GROUP4 • Bit 2-0 is GROUP3 ATR_EN: Attribute data insertion enable: • 0: No insertion • 1: Insertion

6.3.46 Reserved 0 (RSV0)

The reserved 0 register is shown in Figure 220 and described in Table 201.

Figure 220. Reserved 0 (RSV0)

31	16
Reserved	
R-0	

15	0
Reserved	
R-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 201. Reserved 0 (RSV0) Field Descriptions

Bit	Field	Value	Description
31-0	Reserved	0	Reserved

6.3.47 Video Status (VSTAT)

The video status register is shown in Figure 221 and described in Table 202.

Figure 221. Video Status (VSTAT)

31	16
Reserved	
R-0	

15	10	9	8	7	5	4	3	0
Reserved		CAEST	CAOST	Reserved		FIDST	Reserved	
R-0		R-0	R-0	R-0		R-0	R-0	

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

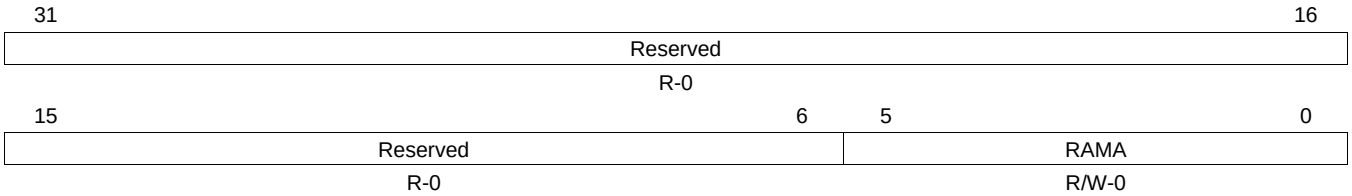
Table 202. Video Status (VSTAT) Field Descriptions

Bit	Field	Value	Description
31-10	Reserved	0	Reserved
9	CAEST		Closed-caption status (even field). Note: The bit automatically becomes 0 when transmission is done.
		0	Ready
		1	Data is being input
8	CAOST		Closed-caption status (odd field). Note: The bit automatically becomes 0 when transmission is done.
		0	Ready
		1	Data is being input
7-5	Reserved	0	Reserved
4	FIDST		Field ID monitor.
3-0	Reserved	0	Reserved

6.3.48 Gamma Correction Table RAM Address (RAMADR)

The GCP/FRC table RAM address register is shown in Figure 222 and described in Table 203.

Figure 222. Gamma Correction Table RAM Address (RAMADR)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

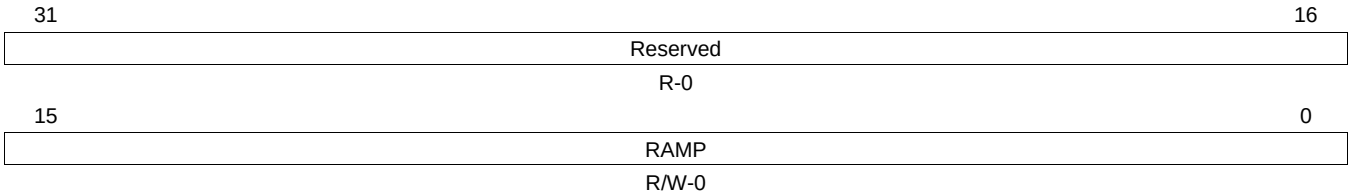
Table 203. Gamma Correction Table RAM Address (RAMADR) Field Descriptions

Bit	Field	Value	Description
31-6	Reserved	0	Reserved
5-0	RAMA	0-3Fh	Gamma correction table RAM address. Note: Auto-increment is done after every access to RAMP register; when RAMA = 0x7F, auto-increment does not occur.

6.3.49 GCP/FRC Table RAM Data Port (RAMPORT)

The GCP/FRC table RAM data port register is shown in Figure 223 and described in Table 204.

Figure 223. GCP/FRC Table RAM Data Port (RAMPORT)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

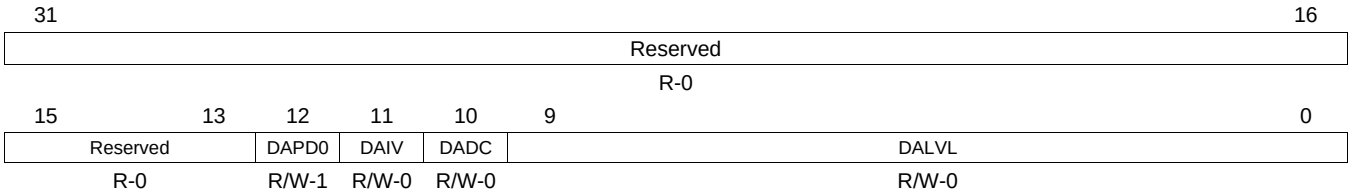
Table 204. GCP/FRC Table RAM Data Port (RAMPORT) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	
15-0	RAMP	0-FFFFh	RAM data port. Note: While reading, the data in the address specified in the RAMA register can be read. While writing, the data is written to the address specified in the RAMA register. The RAMA is automatically incremented every access to the RAMP register in both write and read cases.

6.3.50 DAC Test (DACTST)

The DAC test register is shown in Figure 224 and described in Table 205.

Figure 224. DAC Test (DACTST)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 205. DAC Test (DACTST) Field Descriptions

Bit	Field	Value	Description
31-15	Reserved	0	Reserved
14	DAPD2		DAC power down
		0	Normal
		1	Power down mode
13	DAPD1		DAC power down.
		0	Normal
		1	Power down mode
12	DAPD0		DAC power down.
		0	Normal
		1	Power down mode
11	DAIV		DAC output invert mode.
		0	Non-Inverse
		1	Inverse
10	DADC		DAC DC output mode. Note: Setting to 1 converts the value written in the DALVL register to DAC and directly outputs from DAOUT
		0	Normal
		1	DC output mode.
9-0	DALVL	0-3FFh	DC level control.

6.3.51 YOUT and COUT Levels (YCOLVL)

The YOUT and COUT levels register is shown in Figure 225 and described in Table 206.

Figure 225. YOUT and COUT Levels (YCOLVL)

31	16
Reserved	
R-0	

15	8	7	0
YLVL		CLVL	
R/W-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

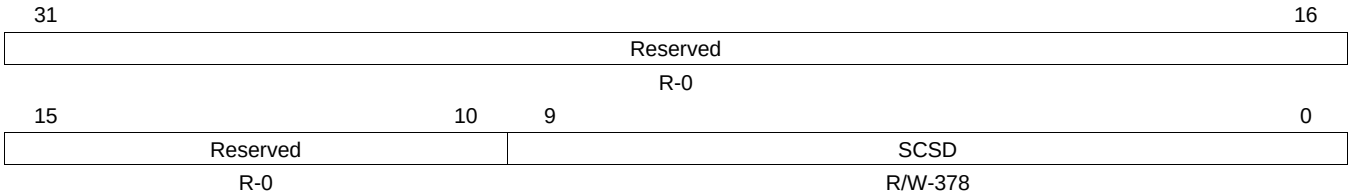
Table 206. YOUT and COUT Levels (YCOLVL) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved
15-8	YLVL	0-FFh	YOUT DC level. Specify the DC output level from YOUT pins when YOUT/COUT pin DC output mode (YCDC=1).
7-0	CLVL	0-FFh	COUT DC level. Specify the DC output level from COUT pins when YOUT/COUT pin DC output mode (YCDC=1).

6.3.52 Sub-Carrier Programming (SCPROG)

The sub-carrier programming register is shown in Figure 226 and described in Table 207.

Figure 226. Sub-Carrier Programming (SCPROG)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 207. Sub-Carrier Programming (SCPROG) Field Descriptions

Bit	Field	Value	Description
31-10	Reserved	0	Reserved
9-0	SCSD	0-3FFh	Sub-carrier initial phase value. The phase in degrees is SCSD/1024*360.

6.3.53 Reserved 1 (RSV1)

The reserved 1 register is shown in Figure 227 and described in Table 208.

Figure 227. Reserved 1 (RSV1)

31	16
Reserved	
R-0	

15	0
Reserved	
R-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 208. Reserved 1 (RSV1) Field Descriptions

Bit	Field	Value	Description
31-0	Reserved	0	Reserved

6.3.54 Reserved 2 (RSV2)

The reserved 2 register is shown in Figure 228 and described in Table 209.

Figure 228. Reserved 2 (RSV2)

31	16
Reserved	
R-0	

15	0
Reserved	
R-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 209. Reserved 2 (RSV2) Field Descriptions

Bit	Field	Value	Description
31-0	Reserved	0	Reserved

6.3.55 Reserved 3 (RSV3)

The reserved 3 register is shown in Figure 229 and described in Table 210.

Figure 229. Reserved 3 (RSV3)

31	16
Reserved	
R-0	

15	0
Reserved	
R-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 210. Reserved 3 (RSV3) Field Descriptions

Bit	Field	Value	Description
31-0	Reserved	0	Reserved

6.3.56 Composite Mode (CVBS)

The composite mode register is shown in Figure 230 and described in Table 211.

Figure 230. Composite Mode (CVBS)

31	16
Reserved	
R-0	

15	14 12	11 6	5	4	3	2	1	0
Rsvd	CYDLY	Reserved	CVLVL	CSTUP	CBLS	CRCUT	CBBLD	CSBLD
R-0	R/W-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 211. Composite Mode (CVBS) Field Descriptions

Bit	Field	Value	Description
31-15	Reserved	0	Reserved
14-12	CYDLY		Delay adjustment of Y signal in composite signal. Note: The value represented is 2s complement.
		0	0
		1	1
		2	2
		3	3
		4	-4
		5	-3
		6	-2
		7	-1
11-6	Reserved	0	Reserved
5	CVLVL		Composite video level (sync/white).
		0	286 mV/714 mV
		1	300 mV/70 0mV
4	CSTUP		Setup for composite.
		0	0%
		1	7.5%
3	CBLS		Blanking shape disable.
		0	Enable
		1	Disable
2	CRCUT		Chroma signal low-pass filter select.
		0	1.5 MHz cut-0ff
		1	3 MHz cut-off
1	CBBLD		Blanking build up time for composite output.
		0	140 µs
		1	300 µs
0	CSBLD		Sync build up time for composite output.
		0	140 µs
		1	200 µs

6.3.57 Component Mode (CMPNT)

The component mode register is shown in Figure 231 and described in Table 212.

Figure 231. Component Mode (CMPNT)

31	16
Reserved	
R-0	

15	14 12	11	10	9	8	7 6	5	4	3	2	1	0
MRGB	MYDLY	Rsvd	MSYR	MSYB	MSYG	MCLVL	MYLVL	MSTUP	MBLS	Rsvd	MBBLD	MSBLD
R/W-0	R/W-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-00	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 212. Component Mode (CMPNT) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved
15	MRGB		RGB select for component output.
		0	YPbPr
		1	RGB
14-12	MYDLY		Delay adjustment of Y signal for component output. Note: The value represented is 2s complement.
		0	0
		1	1
		2	2
		3	3
		4	-4
		5	-3
		6	-2
		7	-1
11	Reserved	0	Reserved
10	MSYR		Sync on Pr (or R).
		0	No Sync
		1	Sync on
9	MSYB		Sync on Pb (or B).
		0	No Sync
		1	Sync on
8	MSYG		Sync on Y (or G).
		0	No Sync
		1	Sync on
7-6	MCLVL		Chroma level for component YPbPr.
		0	350 mW (SMPTE N10)
		1	467 mV (Betacam)
		2	467 mV (MII)
		3	Reserved
5	MYLVL		Luma level (sync/white) for component YPbPr.
		0	286 mv/714 mV
		1	300 mV/700 mV
4	MSTUP		Setup for component YPbPr.
		0	0%
		1	7.5%

Table 212. Component Mode (CMPNT) Field Descriptions (continued)

Bit	Field	Value	Description
3	MBLS		Blanking shape disable.
		0	Enable
		1	Disable
2	Reserved	0	Reserved
1	MBBLD		Blanking build up time for component output.
		0	140 μs (interlace)
		1	300 μs (interlace)
		0	70 μs (progressive)
		1	150 μs (progressive)
0	MSBLD		Sync build up time for composite output.
		0	140 μs (interlace)
		1	200 μs (interlace)
		0	70 μs (progressive)
		1	100 μs (progressive)

6.3.58 CVBS Timing Control 0 (ETMG0)

The CVBS timing control 0 register is shown in Figure 232 and described in Table 213.

Figure 232. CVBS Timing Control 0 (ETMG0)

31	16
Reserved	
R-0	

15	12	11	8	7	4	3	0
Reserved		CEPW		CFSW		CLSW	
R-0		R/W-0		R/W-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

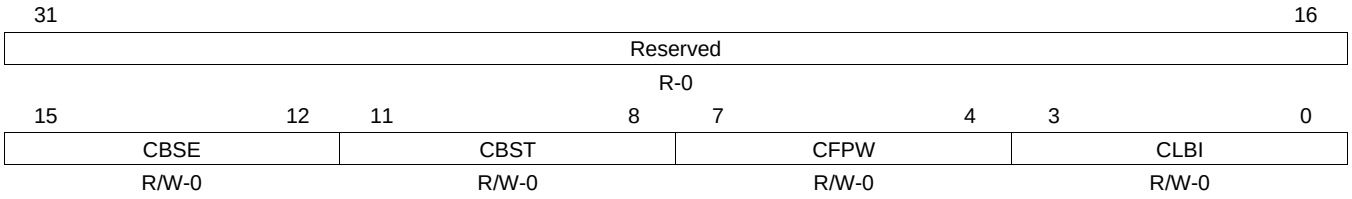
Table 213. CVBS Timing Control 0 (ETMG0) Field Descriptions

Bit	Field	Value	Description
31-12	Reserved	0	Reserved
11-8	CEPW	0-Fh	Equalizing pulse width offset for composite output. This is set by ENC clock. This register is represented as signed integer (2s complement).
7-4	CFSW	0-Fh	Field sync pulse width offset for composite output. This is set by ENC clock. This register is represented as signed integer (2s complement).
3-0	CLSW	0-Fh	Line sync pulse width offset for composite output. This is set by ENC clock. This register is represented as signed integer (2s complement).

6.3.59 CVBS Timing Control 1 (ETMG1)

The CVBS timing control 1 register is shown in Figure 233 and described in Table 214.

Figure 233. VBS Timing Control 1 (ETMG1)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 214. CVBS Timing Control 1 (ETMG1) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved
15-12	CBSE	0-Fh	Burst end position offset for composite output. This is set by ENC clock. This register is represented as signed integer (2s complement).
11-8	CBST	0-Fh	Burst start position offset for composite output. This is set by ENC clock. This register is represented as signed integer (2s complement).
7-4	CFPW	0-Fh	Front porch position offset for composite output. This is set by ENC clock. This register is represented as signed integer (2s complement).
3-0	CLBI	0-Fh	Line blanking end position offset for composite output. This is set by ENC clock. This register is represented as signed integer (2s complement).

6.3.60 CVBS Timing Control 2 (ETMG2)

The CVBS timing control 2 register is shown in Figure 234 and described in Table 215.

Figure 234. CVBS Timing Control 2 (ETMG2)

31	16
Reserved	
R-0	

15	12	11	8	7	4	3	0
Reserved		MEPW		MFSW		MLSW	
R-0		R/W-0		R/W-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 215. CVBS Timing Control 2 (ETMG2) Field Descriptions

Bit	Field	Value	Description
31-12	Reserved	0	Reserved
11-8	MEPW	0-Fh	Equalizing pulse width offset for component output. This is set by ENC clock. This register is represented as signed integer (2s complement).
7-4	MFSW	0-Fh	Field sync pulse width offset for component output. This is set by ENC clock. This register is represented as signed integer (2s complement).
3-0	MLSW	0-Fh	Line sync pulse width offset for component output. This is set by ENC clock. This register is represented as signed integer (2s complement).

6.3.61 CVBS Timing Control 3 (ETMG3)

The CVBS timing control 3 register is shown in Figure 235 and described in Table 216.

Figure 235. CVBS Timing Control 3 (ETMG3)

31	16
Reserved	
R-0	

15	8	7	4	3	0
Reserved		MFPW		MLBI	
R-0		R/W-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 216. CVBS Timing Control 3 (ETMG3) Field Descriptions

Bit	Field	Value	Description
31-8	Reserved	0	Reserved
7-4	MFPW	0-Fh	Front porch position offset for component output. This is set by ENC clock. This register is represented as signed integer (2s complement).
3-0	MLBI	0-Fh	Line blanking end position offset for component output. This is set by ENC clock. This register is represented as signed integer (2s complement).

6.3.62 DAC Output Select (DACSEL)

The DAC output select register is shown in Figure 236 and described in Table 217.

Figure 236. DAC Output Select (DACSEL)

31	16
Reserved	
R-0	

15 12	11 8	7 4	3 0
Reserved	DAC2S	DAC1S	DAC0S
R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 217. DAC Output Select (DACSEL) Field Descriptions

Bit	Field	Value	Description
31-12	Reserved	0	Reserved
11-8	DAC2S		DAC2 output select.
		0	CVBS
		1	S-Video Y
		2	S-Video C
		3	Y/G
		4	Pb/B
		5	Pr/R
		6-15	Reserved
7-4	DAC1S		DAC1 output select.
		0	CVBS
		1	S-Video Y
		2	S-Video C
		3	Y/G
		4	Pb/B
		5	Pr/R
		6-15	Reserved
3-0	DAC0S		DAC0 output select.
		0	CVBS
		1	S-Video Y
		2	S-Video C
		3	Y/G
		4	Pb/B
		5	Pr/R
		6-15	Reserved

6.3.63 Analog RGB Matrix 0 (ARGBX0)

The analog RGB matrix 0 register is shown in Figure 237 and described in Table 218.

Figure 237. Analog RGB Matrix 0 (ARGBX0)

31	16
Reserved	
R-0	

15	11	10	0
Reserved		AGV	
R-0		R/W-1024	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

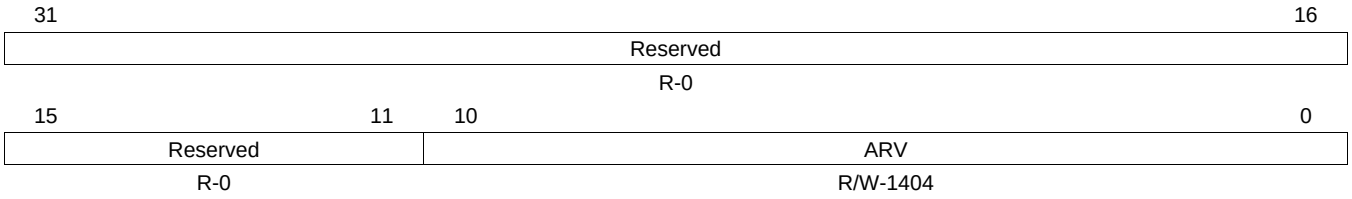
Table 218. Analog RGB Matrix 0 (ARGBX0) Field Descriptions

Bit	Field	Value	Description
31-11	Reserved	0	Reserved
10-0	AGY	0-7FFh	YCbCr->RGB matrix coefficient GY for analog RGB output. Default is 1024 (0x400).

6.3.64 Analog RGB Matrix 1 (ARGBX1)

The analog RGB matrix 1 register is shown in Figure 238 and described in Table 219.

Figure 238. Analog RGB Matrix 1 (ARGBX1)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 219. Analog RGB Matrix 1 (ARGBX1) Field Descriptions

Bit	Field	Value	Description
31-11	Reserved	0	Reserved
10-0	ARV	0-7FFh	YCbCr->RGB matrix coefficient RV for analog RGB output. Default is 1404 (0x57C).

6.3.65 Analog RGB Matrix 2 (ARGBX2)

The analog RGB matrix 2 register is shown in Figure 239 and described in Table 220.

Figure 239. Analog RGB Matrix 2 (ARGBX2)

31	16
Reserved	
R-0	

15	11	10	0
Reserved		AGU	
R-0		R/W-345	

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

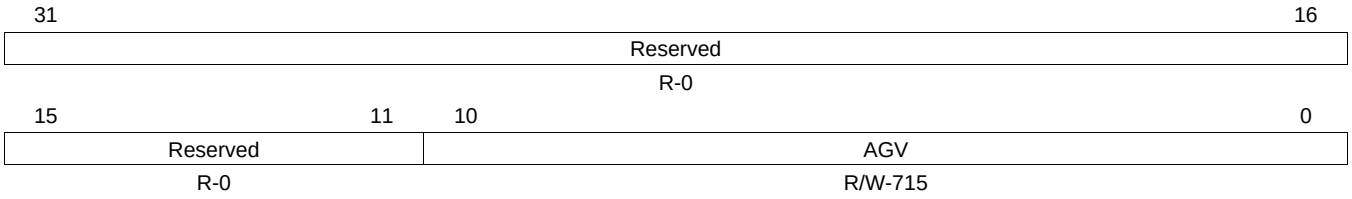
Table 220. Analog RGB Matrix 2 (ARGBX2) Field Descriptions

Bit	Field	Value	Description
31-11	Reserved	0	Reserved
10-0	AGU	0-7FFh	YCbCr->RGB matrix coefficient GU for analog RGB output. Default is 345 (0x159).

6.3.66 Analog RGB Matrix 3 (ARGBX3)

The analog RGB matrix 3 register is shown in Figure 240 and described in Table 221.

Figure 240. Analog RGB Matrix 3 (ARGBX3)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

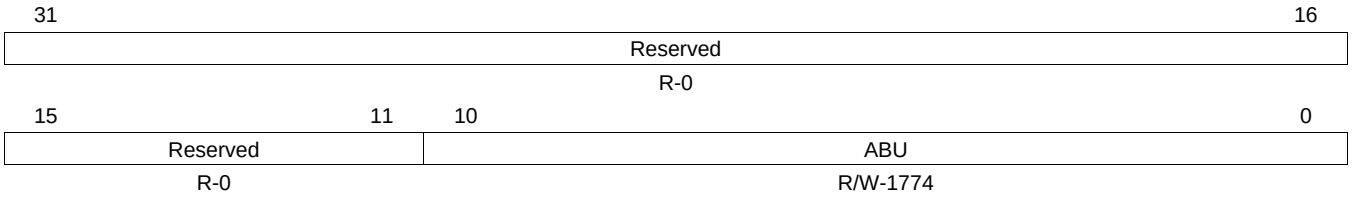
Table 221. Analog RGB Matrix 3 (ARGBX3) Field Descriptions

Bit	Field	Value	Description
31-11	Reserved	0	Reserved
10-0	AGV	0-7FFh	YCbCr->RGB matrix coefficient GV for analog RGB output. Default is 715 (0x2CB).

6.3.67 Analog RGB Matrix 4 (ARGBX4)

The analog RGB matrix 4 register is shown in Figure 241 and described in Table 222.

Figure 241. Analog RGB Matrix 4 (ARGBX4)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 222. Analog RGB Matrix 4 (ARGBX4) Field Descriptions

Bit	Field	Value	Description
31-11	Reserved	0	Reserved
10-0	ABU	0-7FFh	YCbCr->RGB matrix coefficient BU for analog RGB output. Default is 1774 (0x2CB).

6.3.68 Digital RGB Matrix 0 (DRGBX0)

The digital RGB matrix 0 register is shown in Figure 242 and described in Table 223.

Figure 242. Digital RGB Matrix 0 (DRGBX0)

31	16
Reserved	
R-0	

15	11	10	0
Reserved		DGY	
R-0		R/W-1024	

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

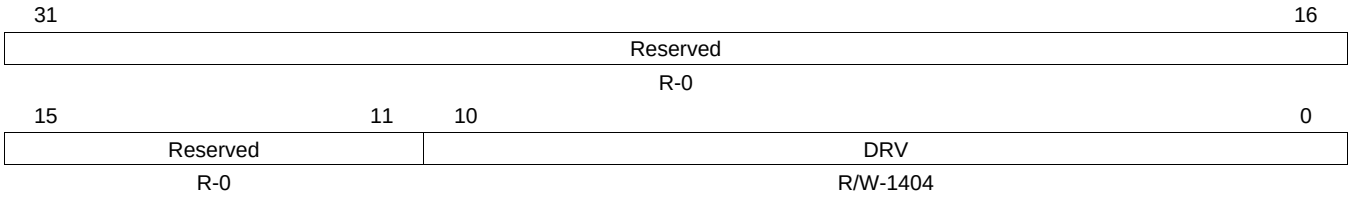
Table 223. Digital RGB Matrix 0 (DRGBX0) Field Descriptions

Bit	Field	Value	Description
31-11	Reserved	0	Reserved
10-0	DGY	0-7FFh	YCbCr->RGB matrix coefficient GY for analog RGB output Default is 1024 (0x400) . Refer section 4.5.4.7.1 for conversion equation.

6.3.69 Digital RGB Matrix 1 (DRGBX1)

The digital RGB matrix 1 register is shown in Figure 243 and described in Table 224.

Figure 243. Digital RGB Matrix 1 (DRGBX1)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

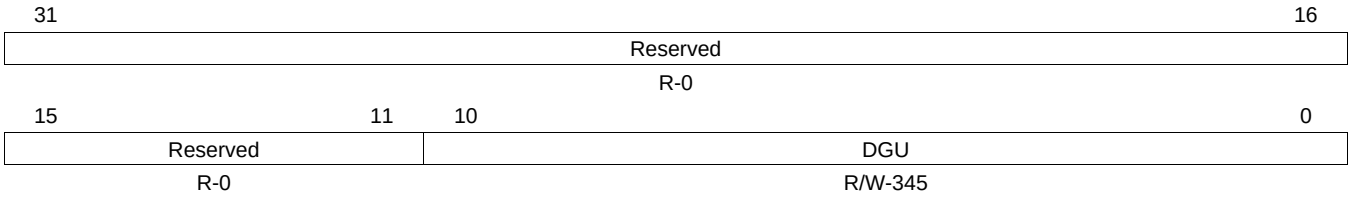
Table 224. Digital RGB Matrix 1 (DRGBX1) Field Descriptions

Bit	Field	Value	Description
15-11	Reserved	0	Reserved
10-0	DRV	0-7FFh	YCbCr->RGB matrix coefficient RV for analog RGB output. Default is 1404 (0x57C).

6.3.70 Digital RGB Matrix 2 (DRGBX2)

The digital RGB matrix 2 register is shown in Figure 244 and described in Table 225.

Figure 244. Digital RGB Matrix 2 (DRGBX2)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

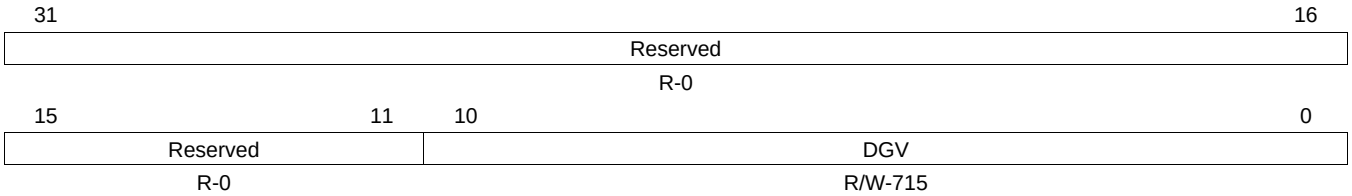
Table 225. Digital RGB Matrix 2 (DRGBX2) Field Descriptions

Bit	Field	Value	Description
31-11	Reserved	0	Reserved
10-0	DGU	0-7FFh	YCbCr->RGB matrix coefficient GU for analog RGB output. Default is 345 (0x159).

6.3.71 Digital RGB Matrix 3 (DRGBX3)

The digital RGB matrix 3 register is shown in Figure 245 and described in Table 226.

Figure 245. Digital RGB Matrix 3 (DRGBX3)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 226. Digital RGB Matrix 3 (DRGBX3) Field Descriptions

Bit	Field	Value	Description
31-11	Reserved	0	Reserved
10-0	DGV	0-7FFh	YCbCr->RGB matrix coefficient GV for analog RGB output. Default is 715 (0x2CB).

6.3.72 Digital RGB Matrix 4 (DRGBX4)

The digital RGB matrix 4 register is shown in Figure 246 and described in Table 227.

Figure 246. Digital RGB Matrix 4 (DRGBX4)

31	16
Reserved	
R-0	

15	12	11	0
Reserved		DBU	
R-0		R/W-1774	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

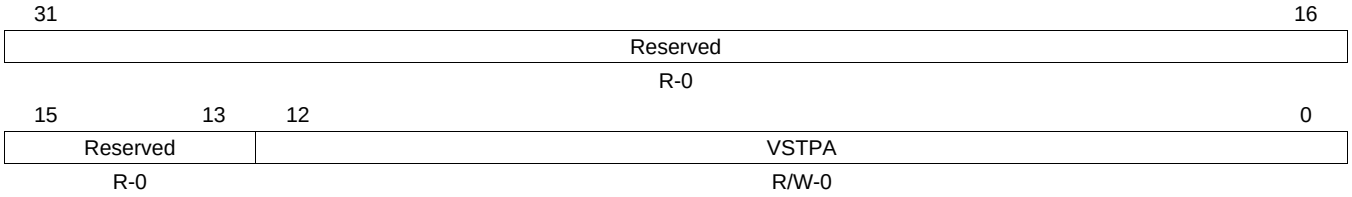
Table 227. Digital RGB Matrix 4 (DRGBX4) Field Descriptions

Bit	Field	Value	Description
31-12	Reserved	0	Reserved
11-0	DBU	0-FFFh	YCbCr->RGB matrix coefficient BU for analog RGB output. Default is 1774 (0x6EE).

6.3.73 Vertical Data Valid Start Position For Even Field (VSTARTA)

The vertical data valid start position for even field register is shown in Figure 247 and described in Table 228.

Figure 247. Vertical Data Valid Start Position For Even Field (VSTARTA)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 228. Vertical Data Valid Start Position For Even Field (VSTARTA) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Reserved
12-0	VSTPA	0-1FFFh	Vertical data valid start position for even field. Specify the number of lines.

6.3.74 OSD Clock Control 0 (OSDCLK0)

The OSD clock control 0 register is shown in Figure 248 and described in Table 229.

Figure 248. OSD Clock Control 0 (OSDCLK0)

31	16
Reserved	
R-0	

15	4	3	0
Reserved		OCPW	
R-0		R/W-1	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 229. OSD Clock Control 0 (OSDCLK0) Field Descriptions

Bit	Field	Value	Description
31-4	Reserved	0	Reserved
3-0	OCPW	0-Fh	OSD clock pattern bit width. Sets the width of valid bit among all 16 bits in the OSDCLK1 register. The number of the valid bits is counted from LSB side to MSB side of the OSDCLK1.

6.3.75 OSD Clock Control 1 (OSDCLK1)

The OSD clock control 1 register is shown in Figure 249 and described in Table 230.

Figure 249. OSD Clock Control 1 (OSDCLK1)

31	16
Reserved	
R-0	

15	0
OCPT	
R/W-2	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

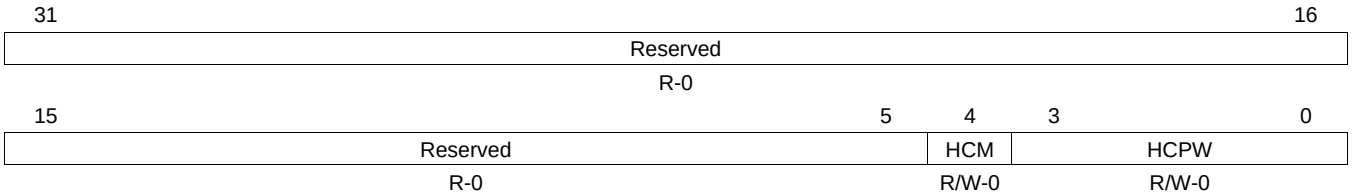
Table 230. OSD Clock Control 1 (OSDCLK1) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved
15-0	OCPT	0-FFFFh	OSD Clock Pattern.

6.3.76 Horizontal Valid Culling Control 0 (HVLDCL0)

The horizontal valid culling control 0 register is shown in Figure 250 and described in Table 231.

Figure 250. Horizontal Valid Culling Control 0 (HVLDCL0)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 231. Horizontal Valid Culling Control 0 (HVLDCL0) Field Descriptions

Bit	Field	Value	Description
31-5	Reserved	0	Reserved
4	HCM		Horizontal valid culling mode. When enabled, the LCD_OE signal is gated by the pattern specified by HCPT register.
		0	Normal mode
		1	Horizontal valid culling mode
3-0	HCPW	0	Horizontal valid culling pattern bit width. Set the width of valid bit among all 16 bits in the HVLDCL1 register. The number of the valid bits is counted from LSB side to MSB side of the HVLDCL1.

6.3.77 Horizontal Valid Culling Control 1 (HVLDCL1)

The horizontal valid culling control 1 register is shown in Figure 251 and described in Table 232.

Figure 251. Horizontal Valid Culling Control 1 (HVLDCL1)

31	16
Reserved	
R-0	

15	0
HCPT	
R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

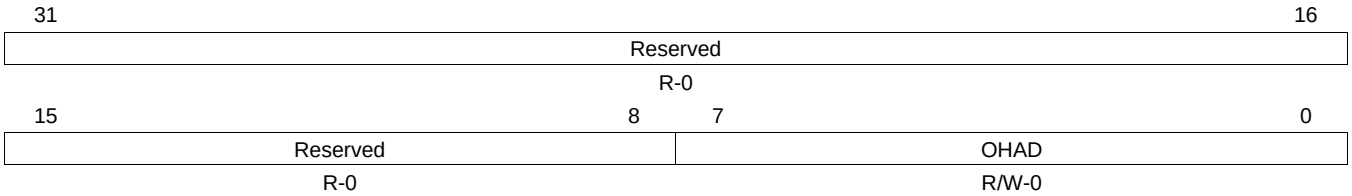
Table 232. Horizontal Valid Culling Control 1 (HVLDCL1) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved
15-0	HCPT	0-FFFh	Horizontal Valid Culling Pattern

6.3.78 OSD Horizontal Sync Advance (OSDHADV)

The OSD horizontal sync advance register is shown in Figure 252 and described in Table 233.

Figure 252. OSD Horizontal Sync Advance (OSDHADV)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 233. OSD Horizontal Sync Advance (OSDHADV) Field Descriptions

Bit	Field	Value	Description
31-8	Reserved	0	Reserved
7-0	OHAD	0-FFh	OSD horizontal sync advance. OSD horizontal sync assertion timing can be advanced by this register. By default, the timing is adjusted so that OSD timing related registers and VENC timing related registers are aligned. Specify the number of ENC clocks.

6.3.79 Clock Control (CLKCTL)

The clock control register is shown in Figure 253 and described in Table 234.

Figure 253. Clock Control (CLKCTL)

31	16
Reserved	
R-0	

15	9	8	7	5	4	3	1	0
Reserved		CLKGAM	Reserved		CLKDIG	Reserved		CLKENC
R-0		R/W-0	R-0		R/W-0	R-0		R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 234. Clock Control (CLKCTL) Field Descriptions

Bit	Field	Value	Description
31-9	Reserved	0	Reserved
8	CLKGAM		Clock enable for gamma correction table. Turn on this bit when you want to change the gamma correction table. Gamma correction circuit is controlled by CLKDIG.
		0	Off
		1	On
7-5	Reserved	0	Reserved
4	CLKDIG		Clock enable for digital LCD controller.
		0	Off
		1	On
3-1	Reserved	0	Reserved
0	CLKENC		Clock enable for video encoder.
		0	Off
		1	On

6.3.80 Enable Gamma Correction (GAMCTL)

The enable gamma correction register is shown in Figure 254 and described in Table 235.

Figure 254. Enable Gamma Correction (GAMCTL)

31	16
Reserved	
R-0	

15	7	6	5	4	3	2	1	0
Reserved		DAFUL2	DAFUL1	DAFUL0	Reserved		GAMUQ	GAMON
R-0		R/W-0	R/W-0	R/W-0	R-0		R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

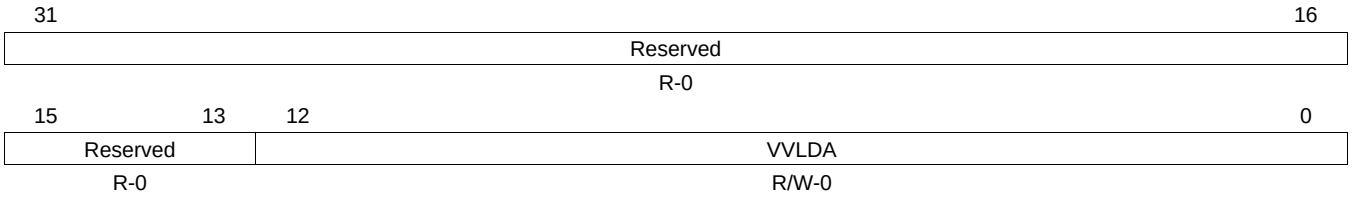
Table 235. Enable Gamma Correction (GAMCTL) Field Descriptions

Bit	Field	Value	Description
31-7	Reserved	0	Reserved
6	DAFUL2		DAC2 full-swing output.
		0	Normal output
		1	Full-swing output
5	DAFUL1		DAC1 full-swing output.
		0	Normal output
		1	Full-swing output
4	DAFUL0		DAC0 full-swing output.
		0	Normal output
		1	Full-swing output
3-2	Reserved	0	Reserved
1	GAMUQ		Unique RGB gamma table mode.
		0	Off
		1	On
0	GAMON		Gamma correction enable.
		0	Off
		1	On

6.3.81 Vertical Data Valid Area For Even Field (VVALIDA)

The vertical data valid area for even field register is shown in Figure 255 and described in Table 236.

Figure 255. Vertical Data Valid Area For Even Field (VVALIDA)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

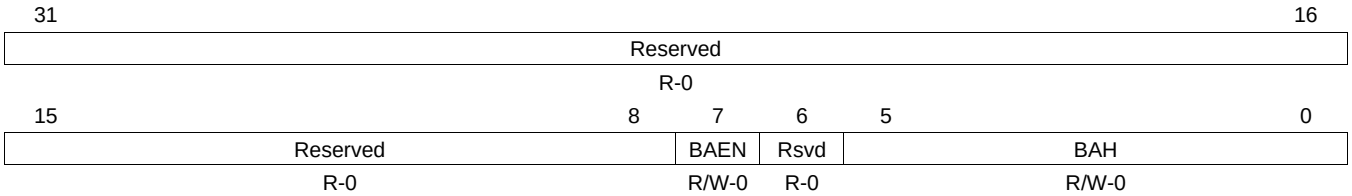
Table 236. Vertical Data Valid Area For Even Field (VVALIDA) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Reserved
12-0	VVLDA	0-1FFFh	Vertical data valid range for even field. Specify the number of lines.

6.3.82 Video Attribute 0 For Type B Packet (BATR0)

The video attribute 0 for type B packet register is shown in Figure 256 and described in Table 237.

Figure 256. Video Attribute 0 For Type B Packet (BATR0)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 237. Video Attribute 0 For Type B Packet (BATR0) Field Descriptions

Bit	Field	Value	Description
31-8	Reserved	0	Reserved
7	BAEN		Type B packet insertion enable. Available in 525P/1080I/720P. When set to 1, type B packet is inserted to the appropriate line (line 40 for 525P, line 18 and 581 for 1080I and line 23 for 720P).
		0	No insertion
		1	Insertion
6	Reserved	0	Reserved
5-0	BAH	0-3Fh	Type B packet header. Specifies h0-h5.

6.3.83 Video Attribute 1 For Type B Packet (BATR1)

The video attribute 1 for type B packet register is shown in Figure 257 and described in Table 238.

Figure 257. Video Attribute 1 For Type B Packet (BATR1)

31	16
Reserved	
R-0	

15	0
BAP	
R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 238. Video Attribute 1 For Type B Packet (BATR1) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved
15-0	BAP	0-FFFFh	Type B packet header. Specifies p0-p15.

6.3.84 Video Attribute 2 For Type B Packet (BATR2)

The video attribute 2 for type B packet register is shown in Figure 258 and described in Table 239.

Figure 258. Video Attribute 2 For Type B Packet (BATR2)

31	16
Reserved	
R-0	

15	0
BAP	
R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 239. Video Attribute 2 For Type B Packet (BATR2) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved
15-0	BAP	0-FFFFh	Type B packet header. Specifies p16-p31.

6.3.85 Video Attribute 3 For Type B Packet (BATR3)

The video attribute 3 for type B packet register is shown in Figure 259 and described in Table 240.

Figure 259. Video Attribute 3 For Type B Packet (BATR3)

31	16
Reserved	
R-0	

15	0
BAP	
R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

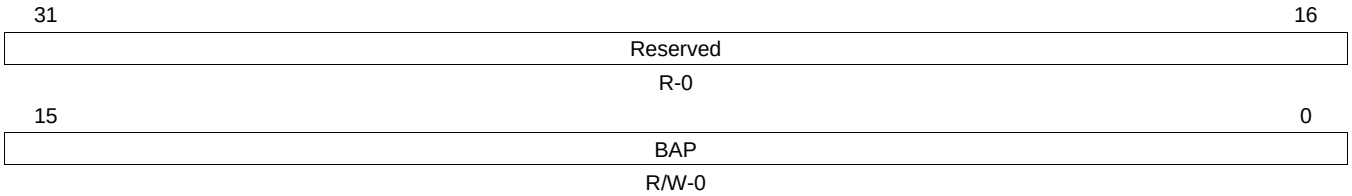
Table 240. Video Attribute 3 For Type B Packet (BATR3) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved
15-0	BAP	0-FFFFh	Type B packet header. Specifies p32-p47.

6.3.86 Video Attribute 4 For Type B Packet (BATR4)

The video attribute 4 for type B packet register is shown in Figure 260 and described in Table 241.

Figure 260. Video Attribute 4 For Type B Packet (BATR4)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 241. Video Attribute 4 For Type B Packet (BATR4) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved
15-0	BAP	0-FFFFh	Type B packet header. Specifies p48-p63.

6.3.87 Video Attribute 5 For Type B Packet (BATR5)

The video attribute 5 for type B packet register is shown in Figure 261 and described in Table 242.

Figure 261. Video Attribute 5 For Type B Packet (BATR5)

31	16
Reserved	
R-0	

15	0
BAP	
R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

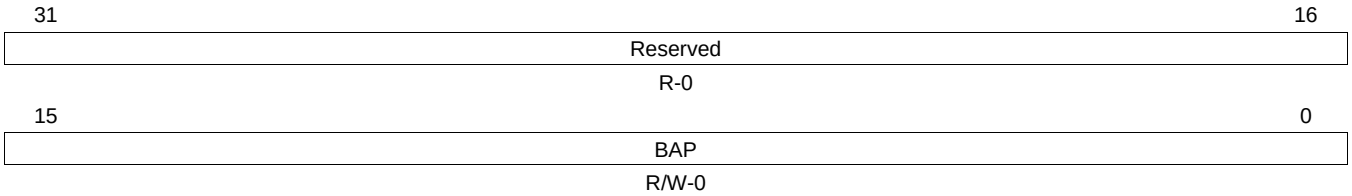
Table 242. Video Attribute 5 For Type B Packet (BATR5) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved
15-0	BAP	0-FFFFh	Type B packet header. Specifies p64-p79.

6.3.88 Video Attribute 6 For Type B Packet (BATR6)

The video attribute 6 for type B packet register is shown in Figure 262 and described in Table 243.

Figure 262. Video Attribute 6 For Type B Packet (BATR6)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 243. Video Attribute 6 For Type B Packet (BATR6) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved
15-0	BAP	0-FFFFh	Type B packet header. Specifies p80-p95.

6.3.89 Video Attribute 7 For Type B Packet (BATR7)

The video attribute 7 for type B packet register is shown in Figure 263 and described in Table 244.

Figure 263. Video Attribute 7 For Type B Packet (BATR7)

31	16
Reserved	
R-0	

15	0
BAP	
R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

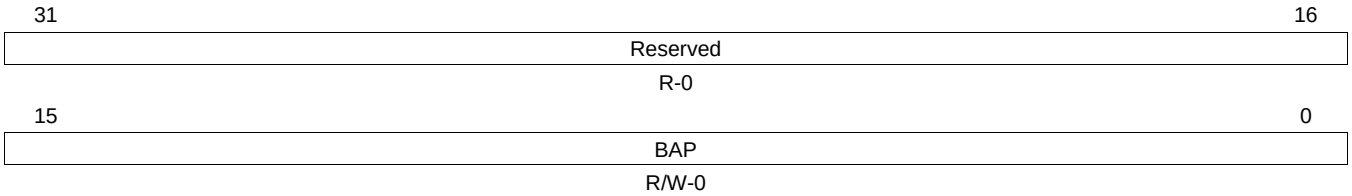
Table 244. Video Attribute 7 For Type B Packet (BATR7) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved
15-0	BAP	0-FFFFh	Type B packet header. Specifies p96-p111.

6.3.90 Video Attribute 8 For Type B Packet (BATR8)

The video attribute 8 for type B packet register is shown in Figure 264 and described in Table 245.

Figure 264. Video Attribute 8 For Type B Packet (BATR8)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 245. Video Attribute 8 For Type B Packet (BATR8) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved
15-0	BAP	0-FFFFh	Type B packet header. Specifies p112-p127.

6.3.91 Gain and Offset (DACAMP)

The gain and offset register is shown in Figure 265 and described in Table 246.

Figure 265. Gain and Offset (DACAMP)

31	16
Reserved	
R-0	

15	10	9	0
DAOF		DAGA	
R/W-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 246. Gain and Offset (DACAMP) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved
15-10	DAOF	3Fh	DAC output offset. Effective in DAC full range output mode (DAFUL=1).
9-0	DAGA	0-3FFh	DAC output gain. Effective in DAC full range output mode (DAFUL=1). Format is 1 bit integer and 9 bit fraction. DAC output code is represented by this equation.

6.3.92 Horizontal Interval Extension (XHINTVL)

The horizontal interval extension is shown in Figure 266 and described in Table 247.

Figure 266. Horizontal Interval Extension (XHINTVL)

31	16
Reserved	
R-0	

15	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved		XH11	XH10	XH9	XH8	XH7	XH6	XH5	XH4	XH3	XH2	XH1	XH0
R-0		R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 247. Gain and Offset (DACAMP) Field Descriptions

Bit	Field	Value	Description
31-12	Reserved	0	Reserved
11-0	XH*n*	0-FFFh	Horizontal interval extension. Extends the horizontal interval of the standard HD timing to support various frame rates. Specify XH11-XH0 by the number of ENC clock cycles. Effective only in the standard 1080i and 720p mode.

Appendix A Revision History

This document has been revised to include the following technical change(s).

Table 248. Document Revision History

Reference	Additions/Modifications/Deletions
Table 9	Corrected Pin names.
Table 11	Changed Function/Mux Control from PINMUX[22], VCLK = 0 to PINMUX1[22], VCLK = 0.
Table 13	Changed Function/Mux Control from PINMUX[22], VCLK = 0 to PINMUX1[22]. VCLK = 0.
Table 14	Corrected Pin names.

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