66AK2Hx KeyStone[™] Multicore DSP+ARM[®] System-on-Chips

TEXAS INSTRUMENTS

Overview

The 66AK2Hx platform is TI's first to combine quad ARM[®] Cortex[™]-A15 MPCore[™] processors with up to eight TMS320C66x high-performance DSPs using the KeyStone II multicore architecture. Unlike previous Cortex-A15-based devices that were designed for consumer products, the 66AK2Hx platform provides up to 5.6 GHz of ARM and 9.6 GHz of DSP processing coupled with security and packet processing and Ethernet switching, all at lower power than multi-chip solutions. This makes these devices optimal for embedded infrastructure applications like cloud computing, media processing, highperformance computing, transcoding, security, gaming, analytics and virtual desktop.

Power and Performance

The combined floating-point processing power of the Cortex-A15 processors and the C66x DSP cores is more than 63 GFLOPS of doubleprecision performance and more than 198 GFLOPS of single-precision performance – providing the best embedded performance per watt in the industry. Combining this real-time performance with a general-purpose embedded processor yields new opportunities for bringing powerful analytics to emerging applications.

Fast and Wide Packet Interfaces

Processing performance alone does not differentiate infrastructure from consumer applications. High-

Key Features

Key features of 66AK2Hx devices include:

CorePac Processors

- Up to four Cortex-A15 processors, 19600
 Dhrystone MIPS
- Up to eight C66x DSP cores, 352 GMACS/198 GFLOPS

Network AcceleratorPac

- Packet coprocessor (IPv4/IPv6) for Layer 2–4
- Security coprocessor IPSec/SRTP
- Five-port 1-Gb Ethernet switch

Memory

- Cache-coherent Multicore Shared Memory Controller (MSMC)
- 1MB per core Level 2 RAM/cache
- 6MB shared memory with ECC and cache coherency
- Two DDR3/3L 1600 interfaces with ECC

performance networking interfaces are critical to deliver data to processors fast enough. The addition of an on-chip five-port 1G Ethernet switch, three-port 10G Ethernet switch, packet coprocessor and security coprocessor provides carrier-grade Ethernet throughput without the increase in ARM[®] or DSP processor loading that normally comes from layer 2-4 processing, encryption and decryption. Other high-performance SerDes interfaces, like Serial RapidIO[®] and PCIe, deliver data to processors at infrastructure speeds, enabling the 66AK2Hx platform to handle tremendous data throughput.

KeyStone II Architecture

- Multicore Navigator; brings single-core programming simplicity to multicore SoCs
- 16,000 atomic hardware queues
- TeraNet on-chip interconnect providing more than two terabits per second throughput
- Low power 9–14 Watts at 55°C case temperature, 11 Watts typical for 66AK2H06 SoC

High speed I/O

- 10 Gigabit Ethernet up to 20 Gbps
- PCI Express Gen2—up to 10 Gbps
- Serial RapidIO V2.1—up to 20 Gbps
- USB 3.0
- HyperLink up to 100 Gbaud for chip-to-chip interconnect

For more technical detail see the **data manual**.

The TeraNet is a multilevel interconnection of high-speed nonblocking channels that deliver more than two terabits per second of concurrent throughput – enabling full multicore entitlement where every processing element can operate near full capacity all of the time.

The two 50-Gbaud HyperLinks use a low-overhead protocol that extends the TeraNet off the device to other KeyStone SoCs and thirdparty devices making them appear as one larger device while simplifying software development, reducing latency and improving system performance.

High-Speed Memory for Demanding Applications

Infrastructure applications demand non-blocking, high-performance memory with error correction. For KeyStone II, TI upgraded the multicore shared memory controller (MSMC) so that memories can operate at the speed of the processor cores which reduces latency and contention while providing highbandwidth interconnections between processor cores and shared internal and external memory. The 72-bit DDR3/3L controllers run at 1600 MT/s with optional error correction (ECC) support and hardware-based cache coherency, enabling more than 20 GB/s data transfers between external and internal memory. The devices provide a second DDR3/3L controller dedicated to maximizing I/O performance.

Tools and Software to Reduce Development Time

TI's development tools and runtime software support make migration and development for heterogeneous platforms simpler than ever.

The Multicore Software Development Kit (MCSDK) provides support for open source Linux[™] and TI's SYS/BIOS operating system for ARM and C66x DSP cores. Evaluation modules (EVMs) will be available with the MCSDK and preloaded example projects. TI also provides optimized single and multicore DSP libraries for FFT, image



▲ TI's KeyStone 66AK2H14 SoC

and video analytics, matrix math and other commonly used algorithms.

TI was the first to support the OpenMP[®] API for multicore DSPs and will continue to advance OpenMP support for KeyStone II platforms. TI's OpenMP software uses a packetbased network-on-chip interconnect called Multicore Navigator to get the best multicore performance. The combination of OpenMP and Multicore Navigator frees developers from complex queue management and allows developers to use industry-standard APIs for programming TI's devices. Support for OpenCL is coming soon.

Code Composer Studio[™] Integrated Development Environment provides a development environment that reduces porting time and can be used as a plug-in to the open-source Eclipse Integrated Development Environment. TI also plans to support Open Source development and profiling tools for KeyStone II-based SoCs.

For more information about the 66AK2Hx platform and TI's portfolio of KeyStone multicore devices please visit **www.ti.com/multicore**.

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