Application Report
SPRAC53A–December 2016–Revised December 2018

AM572x Thermal Considerations

Michael Erdahl

ABSTRACT

This application report discusses thermal performance of the Sitara™ AM572x series processors. Data presented demonstrates the effects of different thermal management strategies in terms of processor junction temperature and power consumption across CPU loading and ambient temperature.

Contents

List of Figures

List of Tables

Trademarks

Sitara is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

1 Overview

The heterogeneous multicore AM5728 general-purpose (GP) evaluation module (EVM) was used in this experiment to gather thermal data with different processor loading, operating performance points (OPP) and ambient temperature. Ambient temperature was controlled with programmable environmental chamber.

The collected data can be utilized to correlate the thermal performance of the processor and power consumption at a given processor load and junction temperature, based on ambient temperature and thermal management.

Tests were repeated with the following thermal management:

- Bare package (no heatsink)
- Low-cost heatsink (provided with GP and Beagleboard-X15 community boards)
- Low-cost heatsink with fan (heatsink was not changed)

2 References

- To learn more about thermal management, visit http://www.ti.com/thermal
- Thermal Design Guide for DSP and ARM Application Processors
- Thermal models can be found in the Models section of Tools and Software in the product folder: http://www.ti.com/product/AM5728/toolssoftware

3 Important Notes

The environmental chamber used to collect this data circulates air internally to maintain homogeneous internal temperature, and does not accurately simulate the environment on the bench or end product. This is important to consider in passive cooling applications where air circulation can significantly impact PCB, package, and heatsink power dissipation efficiency.

Data presented in this test was gathered with a typical device, representing nominal silicon process and leakage. Thermal performance and power consumption can vary significantly due to process variation. Extra margin must be designed in to account for worst case process variation (leakage).

4 Test Overview

The following CPU loading schemes were characterized with the AM572x GP EVM for this report.

4.1 OS Idle

AM57x processor is idling at the Linux Matrix graphical user interface (GUI). Here, the processor cores are active, consuming minimal power.

4.2 Dhrystone Single Core

Dhrystone is a single-threaded benchmark, capable of utilizing approximately 100% of one ARM Cortex-A15 core. Dhyrstone is included in the TI Processor SDK. Tests were conducted with the A15 running at 1.0GHz (OPP_NOM) and 1.5GHz (OPP_HIGH).

4.3 Dhyrstone Dual Core

Dhrystone benchmark instances running on each ARM Cortex-A15 core. Tests were conducted with the A15 running at 1.0GHz (OPP_NOM) and 1.5GHz (OPP_HIGH).

4.4 Temperature Measurement

Reported temperature data is measured by on-die sensors to approximate actual junction temperature. Temperature for each use-case is measured after soaking for 5 minutes. Under lab conditions, it was determined a 5 minute period allows the processor to reach stable temperature.

The TI Processor SDK provides Linux drivers for these sensors, and can be queried from the command-line, for example:

```
# cat /sys/class/thermal/thermal_zone0/temp
71800
```

4.5 OPP Definitions

Operating performance points (OPP) levels imply fixed voltage and frequency targets on a per-subsystem basis. The table below lists frequency of each subsystem per OPP for the AM57x processor.

Dynamic Voltage Frequency Scaling (DVFS) refers to a software technique where the various SoC AVS rails are changed from one OPP level to another in order to either adapt to a changing work-load, or in order to avoid device operation outside of desired temperature bounds.

The SoC only supports DVFS on the MPU rail. Other OPP levels should be set by the initial bootloader. Fixed OPP levels can affect the thermal and power estimates of your system. Ensure the selected OPP level meets the application's needs, and all thermal testing is conducted at the desired OPP level.

Table 1. Supported OPP vs Max Frequency

Voltage Domain	Clock Domain	OPP_NOM Max Frequency (MHz)	OPP_OD Max Frequency (MHz)	OPP_HIGH Max Frequency (MHz)
VD_MPU	MPU_CLK	1000	1176	1500
VD_DSPEVE	DSP_CLK	600	700	750
VD_IVA	IVA_GCLK	388.3	430	532
VD_GPU	GPU_CLK	425.6	500	532
VD_CORE	CORE_IPUx_CLK	212.8	N/A	N/A
	L3_CLK	266		
	DDR3/ DDR3L	532 (DDR3-1066)		
VD_RTC	RTC_FCLK	0.034	N/A	N/A

4.6 Default OPP Levels

Tests were conducted with Processor SDK 03.00.00.04, with following default OPP levels:

OPP			
MPU	**GPU**	**DSP**	**IVA**
NOM	HIGH	HIGH	HIGH

Typically, the MPU domain OPP level can scale dynamically between OPP_NOM, OPP_OD and OPP_HIGH, in Linux using the CPUFreq driver, based on CPU load and selected governor. For the tests in this document, the “userspace” governor was used, and MPU frequency was manually set at the Linux prompt.

GPU, DSP and IVA cores are have fixed OPP levels, and clock-gated when not in use. Today's OPP levels for GPU, DSP and IVA cores can be changed by recompiling U-Boot with the desired OPP level.

5 Data and Results

This section contains the raw data and graphs of the test experiments described above. All data was gathered running the latest Linux Processor SDK.

All tests were conducted with an LCD module installed, which adds extra power.

5.1 OPP Settings and Linux Thermal Framework

Operating performance points for each major compute subsystem is given below. For clock speeds, see Section 4.5. GPU, DSP and IVA cores are clock-gated due to inactivity.

MPU OPP level was held constant for each test. Additionally, the Linux thermal framework was disabled to hold the OPP constant as the processor heats, and prevents thermal shutdown. This was done for data gathering purposes, and is not recommended for a production system.

5.2 Power and Thermal Chamber Measurements (Nom Unit) - SoC Power vs Tambient

The tables below contains power consumption and junction temperature measured running OS Idle, Dhrystone single core and Dhrystone dual core use cases at different controlled ambient temperatures and varying thermal management schemes. Silicon process type is nominal. Dhrystone tests were repeated with MPU at OPP_NOM (1.0 GHz) and OPP_HIGH (1.5 GHz). OPP_OD adds only a modest power increase over OPP_NOM.

Junction temperature and power reported in the following sections were sampled at the same time, and are presented in separate tables to aid comprehension.

5.3 OS Idle (MPU @ OPP_NOM)

Table 2. Processor OPP Settings

OPP			
MPU	**GPU**	**DSP**	**IVA**
NOM	HIGH	HIGH	HIGH

	Ta (°C)						
Therm Mgmt	**25**	**40**	**50**	**60**	**70**	**80**	**90**
No Heatsink (°C)	46	61	71	82	94		
Heatsink (°C)	43	58	68	78	88	100	
Heatsink + Fan (°C)	38	52	61	70	81	89	100

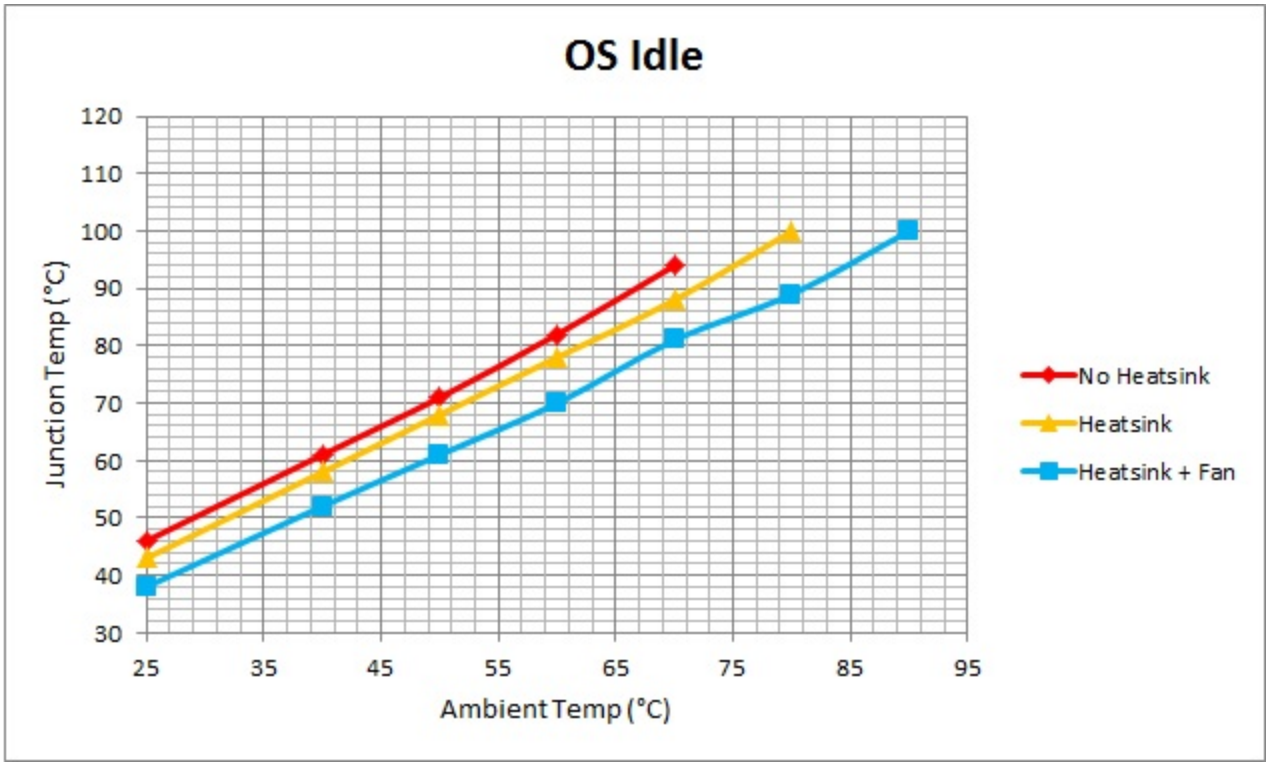

Figure 1. Junction Temperature vs Ambient Temperature

Therm Mgmt	Ta (°C)						
	25	40	50	60	70	80	90
No Heatsink (mW)	1117	1360	1509	1760	2103		
Heatsink (mW)	1118	1281	1447	1649	1923	2304	
Heatsink + Fan (mW)	1064	1203	1332	1542	1712	1973	2323

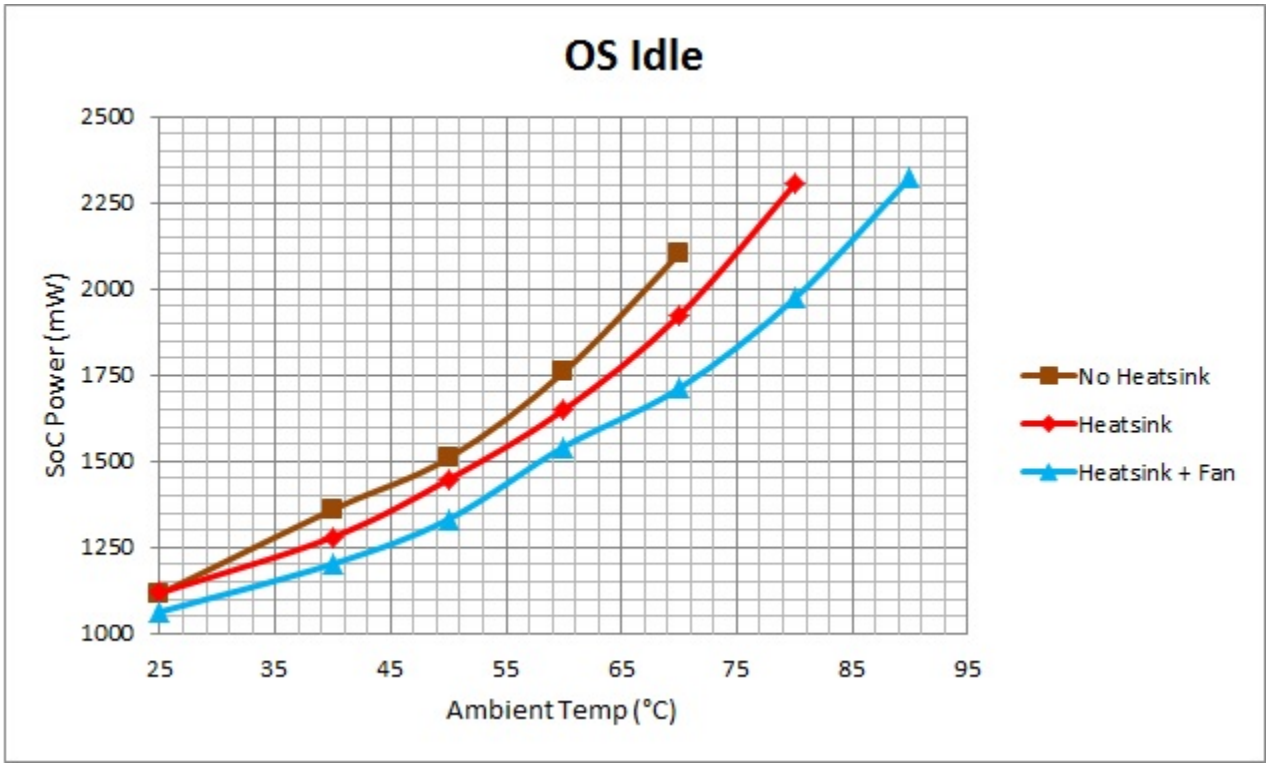

Figure 2. Power Consumption vs Ambient Temperature

5.4 Dhrystone Single Core (MPU @ OPP_NOM)

Table 3. Processor OPP Settings

OPP			
MPU	**GPU**	**DSP**	**IVA**
NOM	HIGH	HIGH	HIGH

	Ta (°C)						
Therm Mgmt	**25**	**40**	**50**	**60**	**70**	**80**	**90**
No Heatsink (°C)	53	68	78	88	100		
Heatsink (°C)	48	63	72	84	94		
Heatsink + Fan (°C)	41	54	64	73	82	94	104

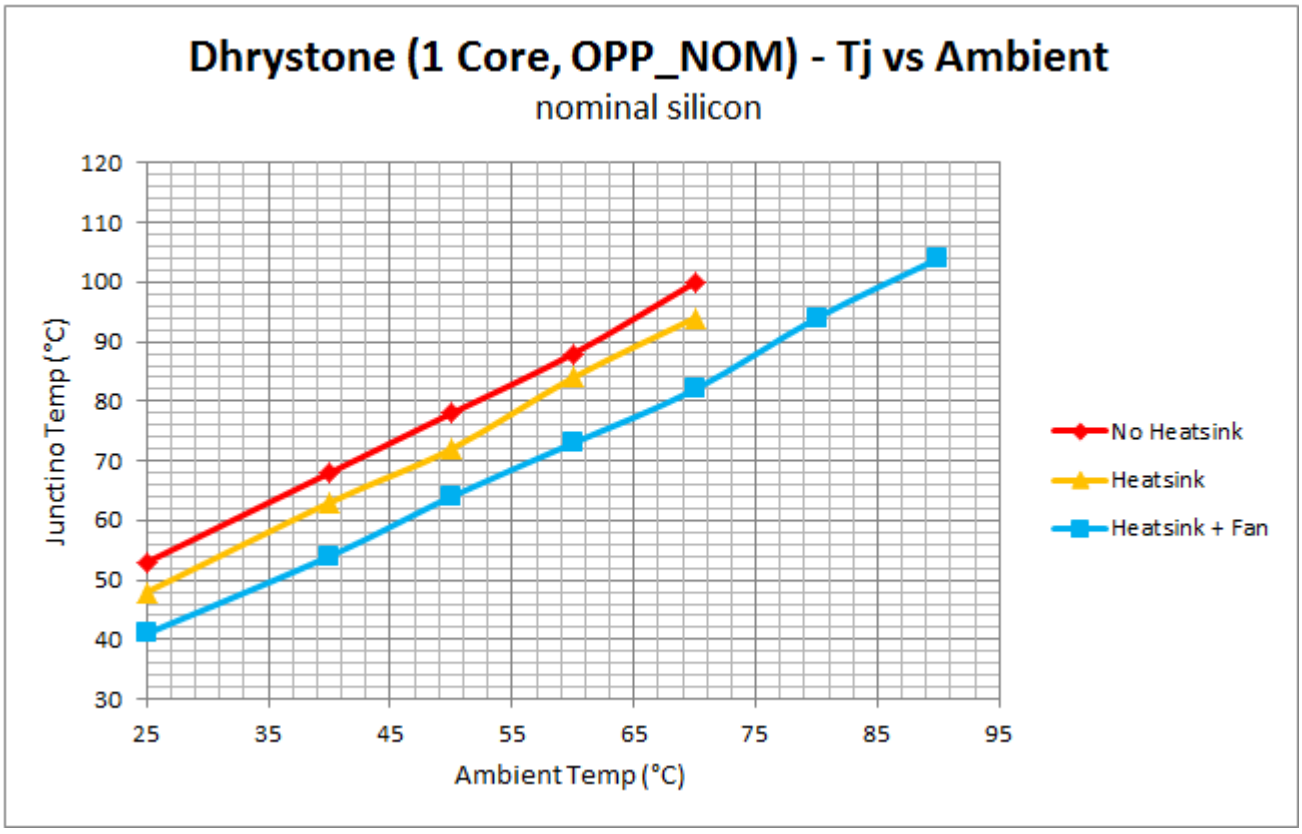

Figure 3. Junction Temperature vs Ambient Temperature

Therm Mgmt	Ta (°C)						
	25	40	50	60	70	80	90
No Heatsink (mW)	2092	2291	2559	2800	3223		
Heatsink (mW)	2031	2240	2430	2671	3012		
Heatsink + Fan (mW)	1961	2158	2268	2452	2678	2992	3380

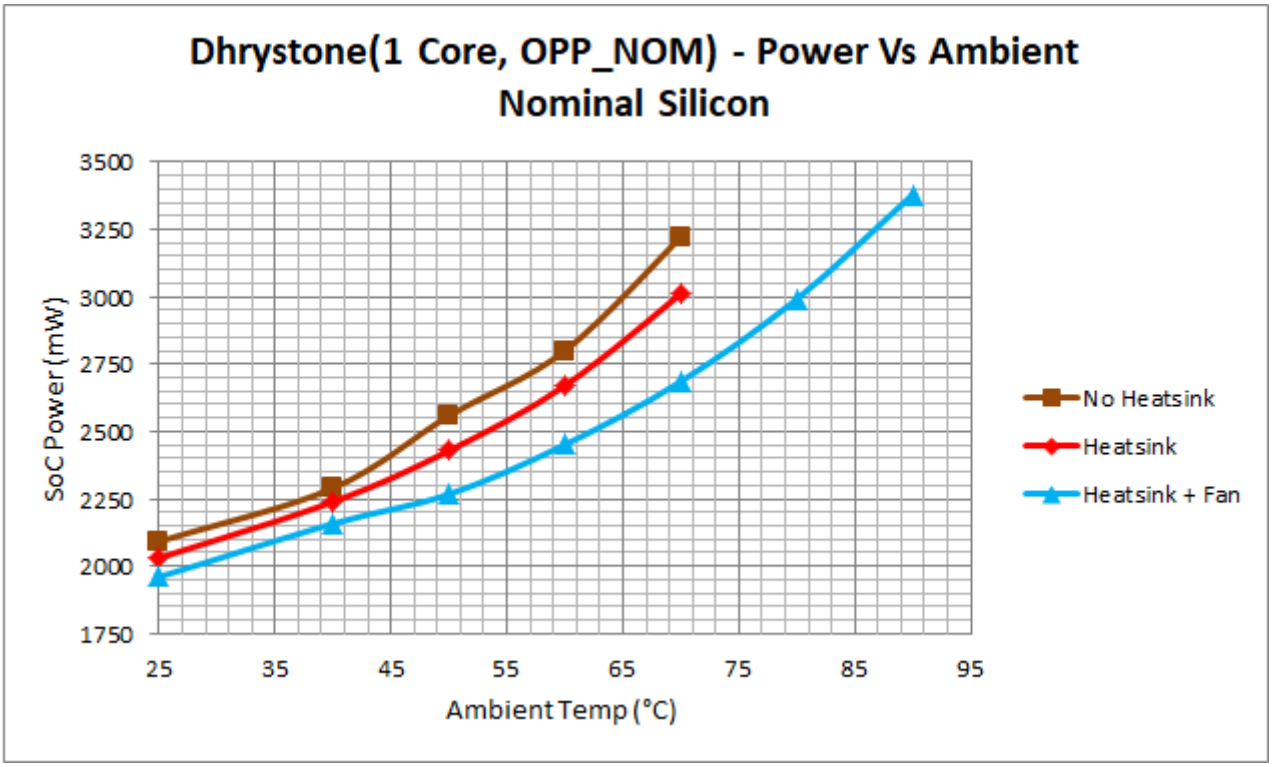

Figure 4. Power Consumption vs Ambient Temperature

5.5 Dhrystone Single Core (MPU @ OPP_HIGH)

Table 4. Processor OPP Settings

OPP			
MPU	**GPU**	**DSP**	**IVA**
HIGH	HIGH	HIGH	HIGH

	Ta (°C)						
Therm Mgmt	**25**	**40**	**50**	**60**	**70**	**80**	**90**
No Heatsink (°C)	66	84	99				
Heatsink (°C)	58	74	86	99			
Heatsink + Fan (°C)	46	62	71	82	92	104	

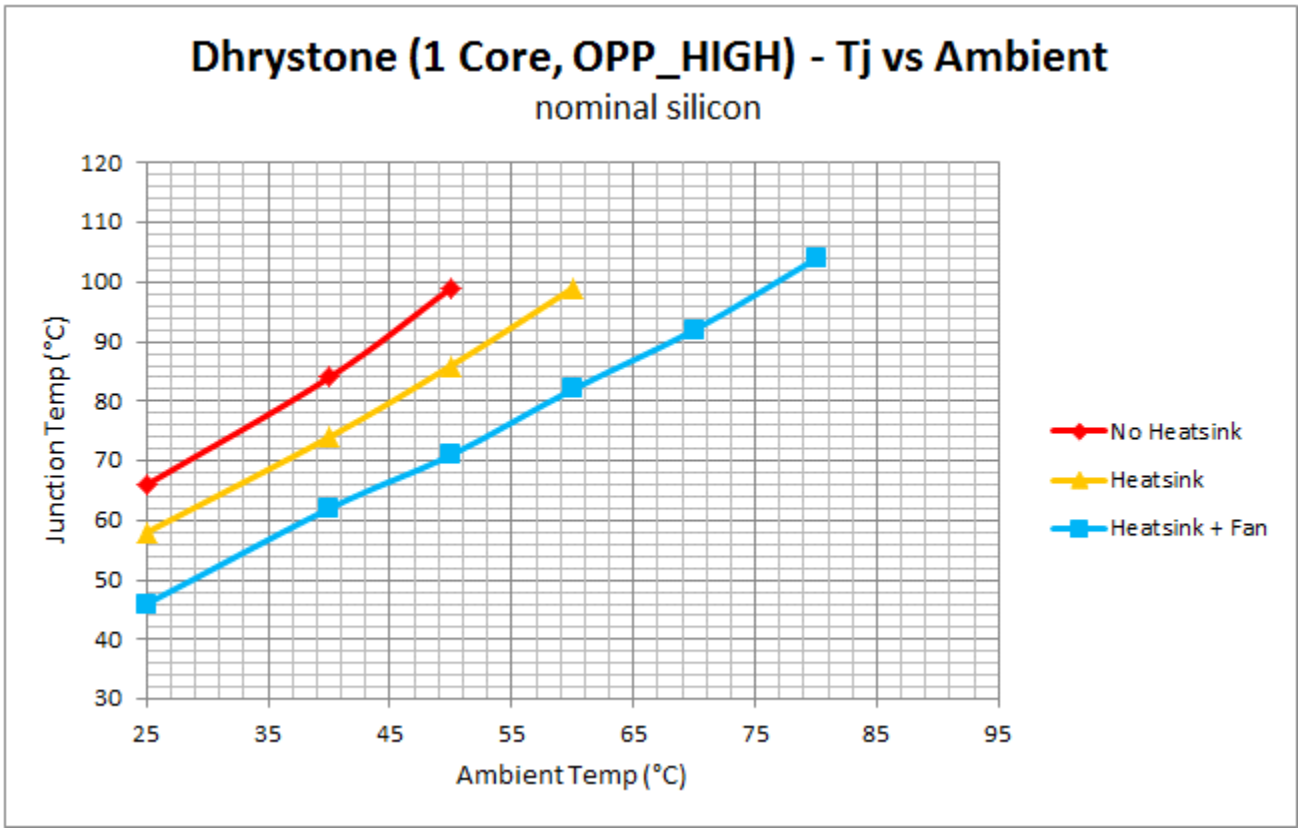

Figure 5. Junction Temperature vs Ambient Temperature

Therm Mgmt	Ta (°C)						
	25	40	50	60	70	80	90
No Heatsink (mW)	4076	4758	5523				
Heatsink (mW)	3953	4429	4879	5572			
Heatsink + Fan (mW)	3735	4070	4350	4744	5190	5835	

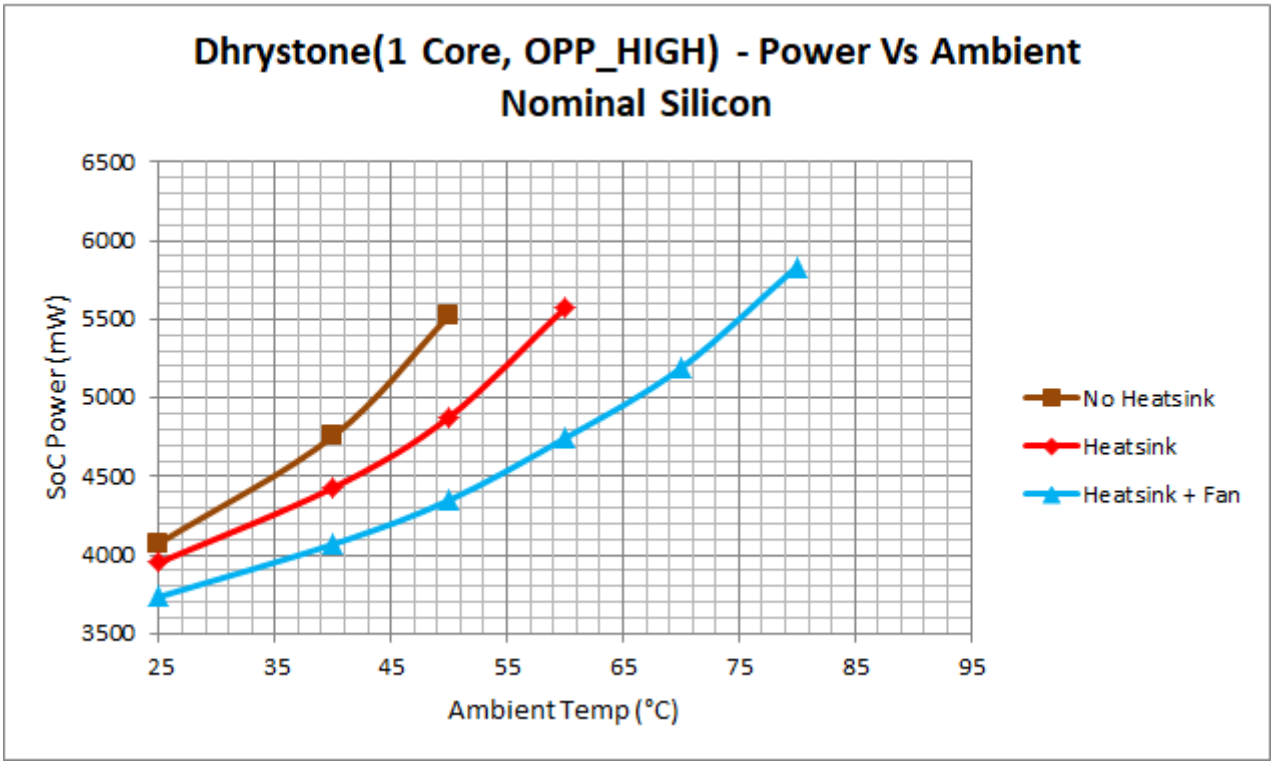

Figure 6. Power Consumption vs Ambient Temperature

5.6 Dhrystone Dual Core (MPU @ OPP_NOM)

Table 5. Processor OPP Settings

OPP			
MPU	**GPU**	**DSP**	**IVA**
NOM	HIGH	HIGH	HIGH

	Ta (°C)						
Therm Mgmt	**25**	**40**	**50**	**60**	**70**	**80**	**90**
No Heatsink (°C)	58	74	84	94			
Heatsink (°C)	52	67	78	88	100		
Heatsink + Fan (°C)	43	58	65	76	87	97	

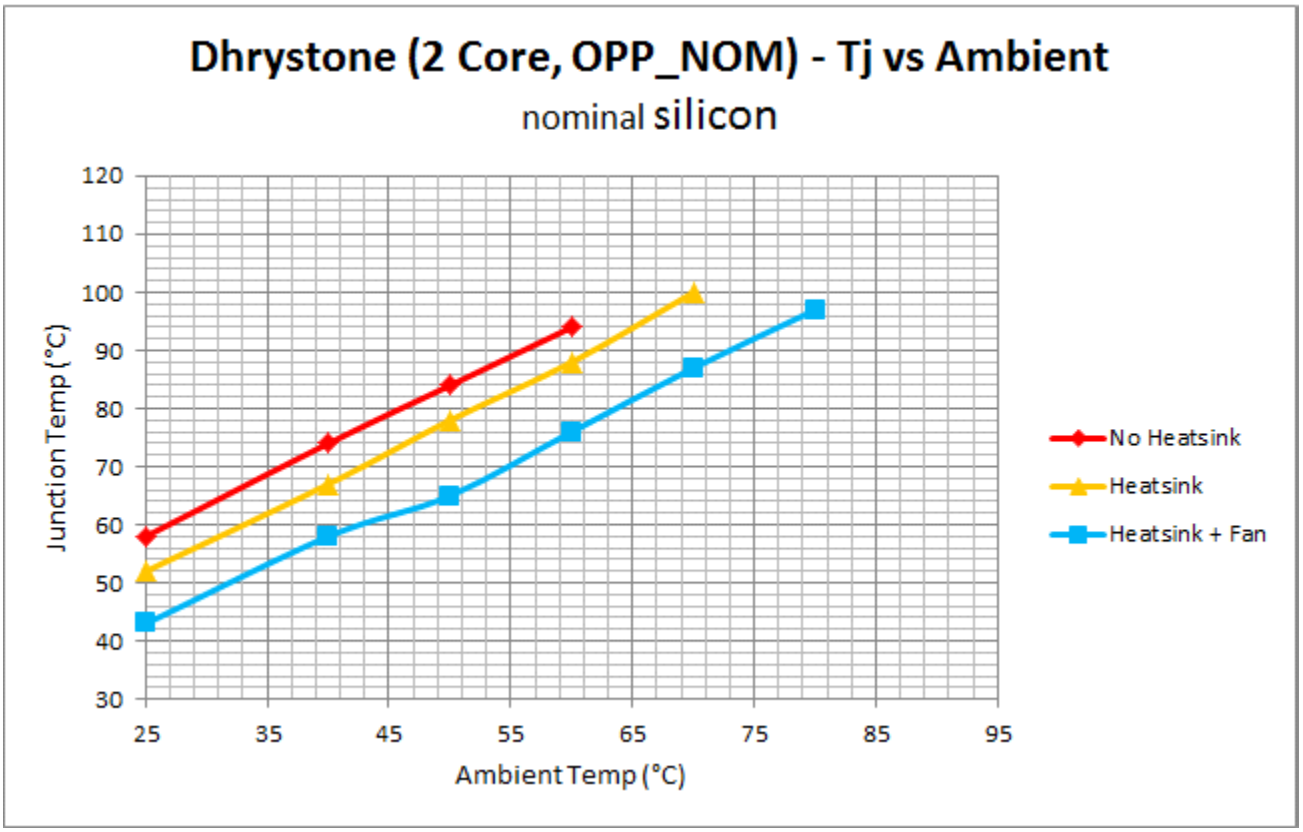

Figure 7. Junction Temperature vs Ambient Temperature

Therm Mgmt	Ta (°C)						
	25	40	50	60	70	80	90
No Heatsink (mW)	3048	3317	3574	3927			
Heatsink (mW)	3001	3210	3393	3654	4059		
Heatsink + Fan (mW)	2874	3056	3176	3382	3681	4001	

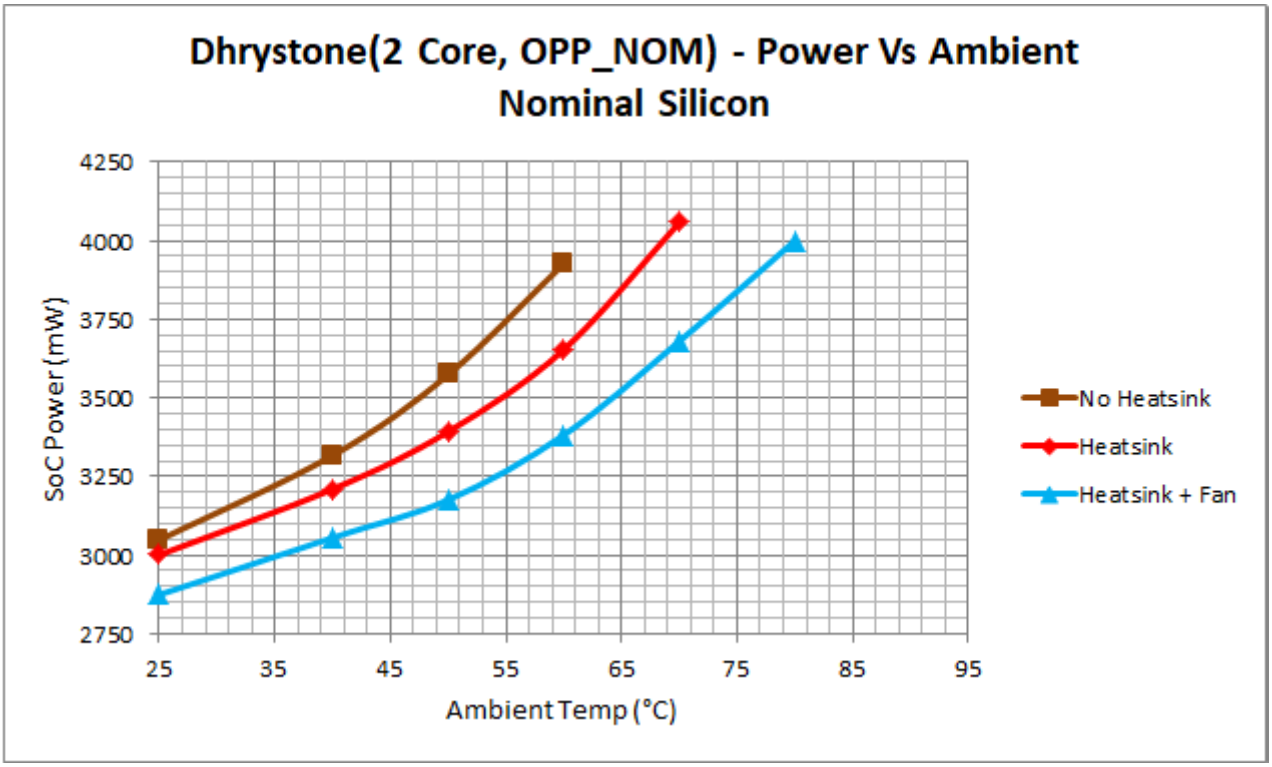

Figure 8. Power Consumption vs Ambient Temperature

5.7 Dhrystone Dual Core (MPU @ OPP_HIGH)

Table 6. Processor OPP Settings

OPP			
MPU	**GPU**	**DSP**	**IVA**
HIGH	HIGH	HIGH	HIGH

	Ta (°C)						
Therm Mgmt	**25**	**40**	**50**	**60**	**70**	**80**	**90**
No Heatsink (°C)	84	104					
Heatsink (°C)	71	89	103				
Heatsink + Fan (°C)	54	69	80	90	102		

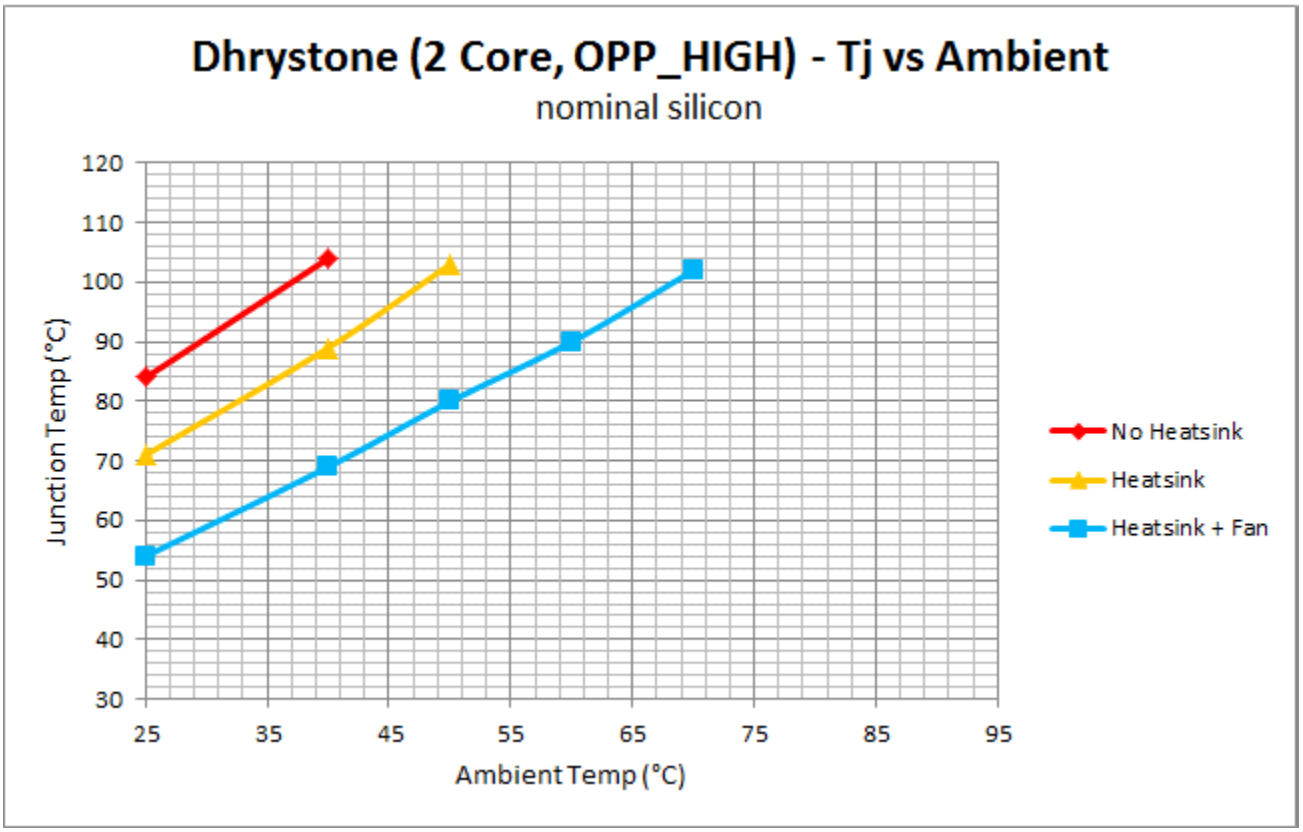

Figure 9. Junction Temperature vs Ambient Temperature

Therm Mgmt	Ta (°C)						
	25	40	50	60	70	80	90
No Heatsink (mW)	6868	7785					
Heatsink (mW)	6448	7166	7651				
Heatsink + Fan (mW)	6068	6466	6846	7220	7859		

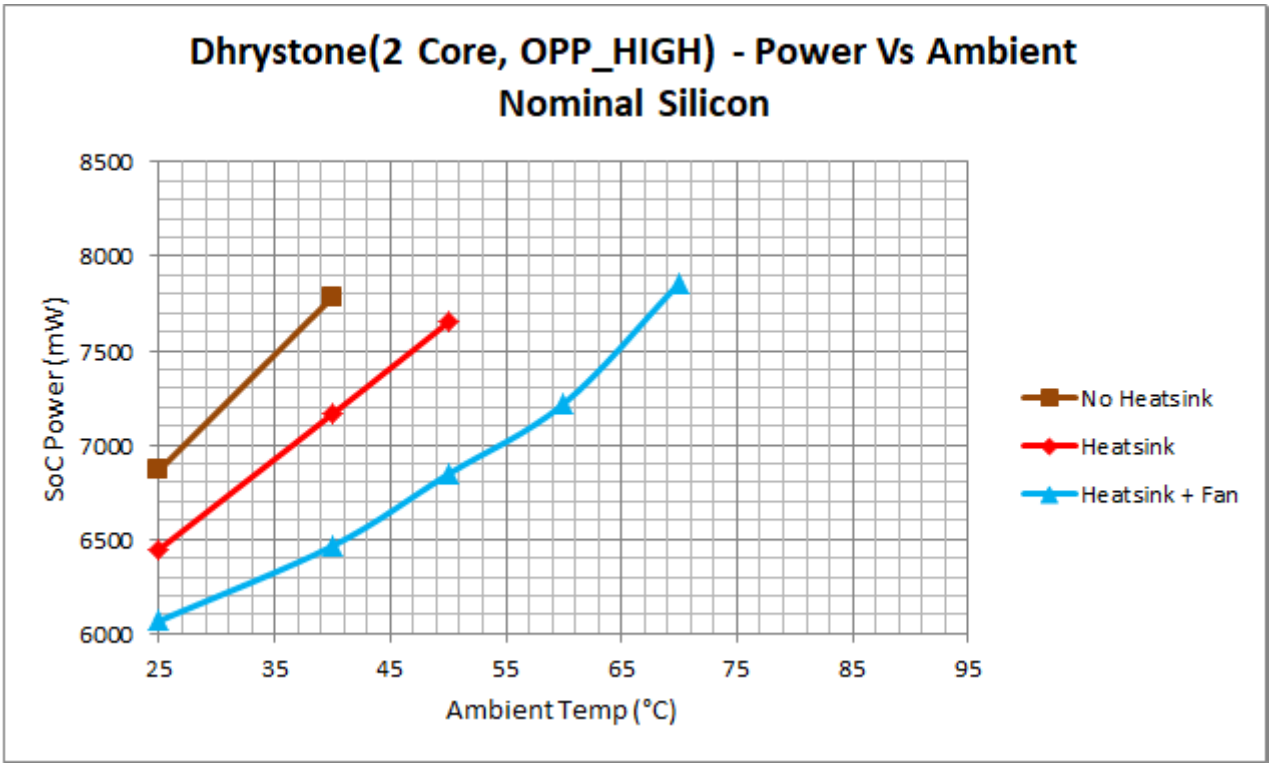

Figure 10. Power Consumption vs Ambient Temperature

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (December 2016) to A Revision	Page
• The Power vs Ambient temperature graphs has been updated with new one for Dhrystone(1 core, OPP_NOM), Dhrystone(1 Core, OPP_HIGH), Dhrystone(2 Core, OPP_NOM) and Dhrystone(2 Core, OPP_HIGH).....	2

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265