Application Report
SPRABL8–April 2014

Migrating from TMS320C5515 to TMS320C5517

ABSTRACT

The TMS320C5515 and the TMS320C5505 will henceforth in this document be referred to as C5515/05. The TMS320C5517 will henceforth in this document be referred to as C5517.

This document provides the minimum changes required to migrate from the C5515/05 to the C5517. Enhancements or new features of the C5517 that do not affect migrating from the C5515/05 to the C5517 are also briefly mentioned in this document.

All efforts have been made to provide a comprehensive list of changes. An update will be provided if additional changes are identified.

More information on the C5517 DSP can be found in *TMS320C5517 Fixed-Point Digital Signal Processor* (literature number SPRS727).

Register descriptions for the C5517 are detailed in *TMS320C5517 Digital Signal Processor Technical Reference Manual* (literature number SPRUH16).

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1 Overview

The following table shows the major differences between the two devices. Peripherals that are not included in the table have no changes.

Table 1. Differences Between Devices

	C5517	C5515/05	Note
Max CPU Speed (PLL output)	75 MHz at 1.05 V 175 MHz at 1.3 V 200 MHz at 1.4 V	60 and 75 MHz at 1.05 V 100 and 120 MHz at 1.3 V 150 MHz at 1.4 V (only C5505)	See Section 3
I/O Voltage	1.8, 2.75, and 3.3 V (2.5 V is no longer supported)	1.8, 2.5, 2.75, and 3.3 V	See Section 3
On-chip Oscillator and USB_LDO	If CLK_SEL = 0 at reset: The on-chip USB oscillator will provide clock to PLL. The on-chip USB oscillator and USB_LDO will be enabled and can't be disabled. If CLK_SEL = 1 at reset: The CLKIN pin will be selected as the clock source to PLL. The on-chip USB oscillator and USB_LDO will be disabled but can be enabled by software.	The on-chip USB oscillator and USB_LDO are always disabled at reset but can be enabled by software. The on-chip RTC oscillator is always enabled at reset and can be disabled by software. If CLK_SEL = 0 at reset: The on-chip RTC oscillator will provide clock to PLL If CLK_SEL = 1 at reset: The CLKIN pin will be selected as the clock source to PLL.	See Section 6
PLL	New PLL module VDDA_PLL must be powered externally.	VDDA_PLL may be powered by ANA_LDOO	See Section 4
ANA_LDO	ANA_LDO can provides power only to VDDA_ANA, not to VDDA_PLL.	ANA_LDO can provide power to both VDDA_ANA and VDDA_PLL.	See Section 4
CLKOUT	No glitch when switching modes and source. Mode: Divider, Stopped at low state, and Hi-Z mode.	Glitch when switching modes or source. Mode: Bypass and Hi-Z mode (not divider).	See Section 7 **Note:** CLKOUT on both devices is only for debug purposes.
Bootloader	Supports unencrypted boot image from McSPI, UHPI, SD and SDHC, eMMC and MMC, and UART. Read GPIO[26:21] ports to determine peripherals and method to boot from and CPU clock speed. Latch GPIO[26:21] ports at 10th clock after reset.	Supports only encrypted boot-image from USB and MMC and SD Does not support UART boot. Bootloader checks each peripheral for boot signature in a predefined order.	See Section 9
Pins and Peripherals	All pins will be in Hi-Z state while RESET signal is held low. They will get back to their reset conditions at 10 CPU cycles after RESET. More I/O pins have internal pullup and pulldown options. No LCD controller. LCD is replaced with UHPI. 1 I2S module is replaced with McSPI. A total f 3 I2S modules are available. McBSP has been added. Total 40 pins have new function. System DMA supports I2S, McBSP, McSPI, MMC and SD, SAR, UART, and EMIF.	4 I2S modules LCD controller No McBSP No UHPI No McSPI System DMA supports I2S, MMC and SD, SAR, UART, and EMIF	See Section 5.5 for details on pin out changes See Section 7 for I/O pullup and pulldown changes
Timer Interrupt	Timer interrupt can routed to the NMI interrupt (the highest interrupt priority).	Timer interrupt stays at low interrupt priority.	See Section 8
Timer clock source	Timer clock source can be PLL output, PLL input, GPIO0, GPIO6, GPIO12, GPIO18, GPIO24, or the on-chip USB oscillator.	Only PLL output	See Section 8.3

Table 1. Differences Between Devices (continued)

	C5517	C5515/05	Note
FFT Co-processor	HWA FFT API Address	HWA FFT API Address	
	0x00fefefc _hwafft_br	0x00ff6cd6 _hwafft_br	
	0x00feff10 _hwafft_8pts	0x00ff6cea _hwafft_8pts	
	0x00feffff _hwafft_16pts	0x00ff6dd9 _hwafft_16pts	
	0x00ff0155 _hwafft_32pts	0x00ff6f2f _hwafft_32pts	
	0x00ff045e _hwafft_64pts	0x00ff7238 _hwafft_64pts	
	0x00ff05f3 _hwafft_128pts	0x00ff73cd _hwafft_128pts	
	0x00ff0804 _hwafft_256pts	0x00ff75de _hwafft_256pts	
	0x00ff0a02 _hwafft_512pts	0x00ff77dc _hwafft_512pts	
	0x00ff0c7c _hwafft_1024pts	0x00ff7a56 _hwafft_1024pts	

2 Operating Conditions

2.1 Operating Voltages and CPU Speeds

The C5517 supports a CPU speed of up to 200 MHz. See the details in Table 2.

Table 2. Operating Voltages and CPU speeds for C5517 and C5515/05

Supply Pins	C5517		C5515/05	
CV_{DD}	1.05 V	75 MHz	1.05 V	60 and 75 MHz
	1.3 V	175 MHz	1.3 V	100 and 120 MHz
	1.4 V	200 MHz	1.4 V	150 MHz (C5505 only)
DV_{DDIO}, DV_{DDEMIF}, DV_{DDRTC}	1.8, 2.75, and 3.3 V		1.8, 2.5, 2.75, and 3.3 V	
All other power domains	No changes			

3 LDOs

Both the C5517 and the C5515/05 have three on-chip LDOs (ANA_LDO, DSP_LDO, and USB_LDO). No feature has been changed to LDOs but the usage is different.

3.1 USB_LDO

When CLK_SEL = 0 at reset, the USB_LDO is automatically enabled and cannot be turned off.

When CLK_SEL = 1 at reset, the USB_LDO is automatically disabled but can be enabled by writing 1 to bit 0 of the LDO Control Register (7004h).

For more details on the LDO Control Register (LDOCNTL), see the chapter *System Control* in *TMS320C5517 Digital Signal Processor Technical Reference Manual* (literature number SPRUH16).

3.2 ANA_LDO

On the C5517, the ANA_LDOO can provide power to the VDDA_ANA pin but cannot provide power to VDDA_PLL anymore. The new PLL in the C5517 consumes more power than that of the PLL in the C5515/05: typically ~5mA at 312 MHz. Due to the higher current, the ANA_LDOO cannot provide power to VDDA_PLL. VDDA_PLL must be powered externally.

3.3 LDO Specification

Table 3 describes the input, outputs, input voltage ranges, regulated output voltages, and power management portions of the C5517.

Table 3. On-chip Regulator Operating Conditions

	Input		Output			
	Input Pin	**Input Voltage Range**	**Output Pin**	**Output Voltage**	**Max Output Current Output**	**Section Powered**
ANA LDO	LDOI	1.8 V ~ 3.6 V	ANA_LDOO	1.3V	4 mA	V_{DDA_ANA}
DSP LDO	LDOI	1.8 V ~ 3.6 V	DSP_LDOO	1.3 V (DSP_LDO_V =1)	250 mA	CV_{DD}
				1.3 V (DSP_LDO_V =0)		
USB LDO	LDOI	1.8 V ~ 3.6 V	USB_LDOO	1.3 V	25 mA	USB_V_{DD1P3} USB_V_{DDA1P3}

4 Pin and Package Considerations

4.1 Package

The C5517 and the C5515/05 have the same package: 196 pin, 10x10 mm with 0.65-mm pitch, Green (Pb-free and environmentally friendly) nFBGA ZCH package. For more information, see *TMS320C5517 Fixed-Point Digital Signal Processor* (literature number SPRS727).

4.2 Pin Compatibility

The C5517 and the C5515/05 can be pin-to-pin compatible if the following conditions are satisfied:

- The new peripherals (McBSP, McSPI, and UHPI) in the serial port 0, serial port 1, and parallel port will always be disabled.
- The LCD module (in parallel port) and I2S1 module (in serial port 1) of the C5515/05 are not needed.
- VDDA_PLL (1.3V) is supplied by an external power source, not by the ANA_LDO.
- If CLK_SEL = 0 at reset, the on-chip USB oscillator must generate a 12-MHz clock.
- The RSV16 pin is tied directly to V_{SS}.

If all of the previous conditions are met, the C5517 and the C5515/05 are pin-to-pin compatible and the C5515/05 can be replaced with the C5517 without hardware modification. However, the C5517 has a new bootloader that latches the GPIO[26:21]/EM_A[20:15] pins at reset to determine boot mode. Those pins may need external pullups and pulldowns to set a proper boot mode configuration (see Section 10 for details).

4.3 Peripheral Changes

The LCD and one I2S for C5515/05 are replaced by the McBSP, UHPI and McSPI for C5517.

- No LCD controller. LCD is replaced with UHPI.
- One I2S module is replaced with McSPI. A total of three I2S modules are available.
- System DMA supports I2S, McBSP, McSPI, MMC and SD, SAR, UART, and EMIF.
- 40 pins have new functions.

The functions of these new peripherals are not the scope of this migration guide. For more information, see the *TMS320C5517 Digital Signal Processor Technical Reference Manual* (SPRUH16).

4.4 Pin Map

The serial port 0, serial port 1, parallel ports, and SDRAM control signals have new functions because the McBSP, McSPI, and UHPI ports share those pins with other peripherals. The SDRAM control signals are part of parallel port and are multiplexed with UHPI control signals controlled by the EBSR register [1C00h] in the C5517.

Pins with new functions on the C5517 are shown as shaded areas in Figure 1.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
P	**EM_DQM1**/ UHPI_HBE1	DV_{DDEMIF}	DV_{DDIO}	**SPI_CS0**/ UHPI_HCNTL0	**SPI_CS2**/ UHPI_HR_NW	**SPI_RX**/ UHPI_HD[0]	**GP[12]**/ UHPI_HD[2]	DV_{DDIO}	**GP[15]**/ UHPI_HD[5]	**GP[17]**/ UHPI_HD[7]	**I2S2_FS**/ **UHPI_HD[9]**/ **GP[19]**/ **SPI_CS0**	**I2S2_DX**/ UHPI_HD[11]/ GP[27]/ SPI_TX	**UART_CTS**/ UHPI_HD[13]/ GP[29]/ I2S3_FS	**UART_TXD**/ UHPI_HD[15]/ GP[31]/ I2S3_DX
N	**GP[21]**/ EM_A[15]	**EM_SDCKE**/ UHPI_HHWIL	**SPI_CLK**/ UHPI_HINT	**SPI_CS1**/ UHPI_HCNTL1	**SPI_CS3**/ UHPI_HRDY	**SPI_TX**/ UHPI_HD[1]	**GP[13]**/ UHPI_HD[3]	**GP[14]**/ UHPI_HD[4]	**GP[16]**/ UHPI_HD[6]	**I2S2_CLK**/ UHPI_HD[8]/ GP[18]/ SPI_CLK	**I2S2_RX**/ UHPI_HD[10]/ GP[20]/ SPI_RX	**UART_RTS**/ UHPI_HD[12]/ GP[28]/ I2S3_CLK	**UART_RXD**/ UHPI_HD[14]/ GP[30]/ I2S3_RX	DV_{DDIO}
M	EM_A[14]	EM_D[5]	EM_SDCLK	$\overline{EM\_CS3}$	EMU1	TCK	TDO	XF	$\overline{TRST}$	**MMC0_D1**/ I2S0_RX/ GP[3]/ McBSP_DR	**MMC0_CMD**/ I2S0_FS/ GP[1]/ McBSP_FSX	**MMC1_D1**/ McSPI_SOMI/ GP[9]	**MMC1_CLK**/ McSPI_CLK/ GP[6]	**MMC1_D0**/ McSPI_SIMO/ GP[8]
L	EM_A[13]	EM_A[10]	EM_D[12]	EM_D[4]	CV_{DD}	EMU0	TDI	TMS	**MMC0_D0**/ I2S0_DX/ GP[2]/ McBSP_DX	**MMC0_CLK**/ I2S0_CLK/ GP[0]/ McBSP_CLKX	**MMC0_D3**/ GP[5]/ McBSP_ CLKR_CLKS	**MMC0_D2**/ GP[4]/ McBSP_FSR	**MMC1_D3**/ McSPI_CS2/ GP[11]	**MMC1_CMD**/ McSPI_CS0/ GP[7]
K	EM_A[12]/ (CLE)	EM_A[11]/ (ALE)	EM_D[14]	EM_D[13]	EM_D[6]	EM_WAIT3	DV_{DDIO}	V_{SS}	V_{SS}	CV_{DD}	V_{SS}	DV_{DDIO}	V_{SS}	**MMC1_D2**/ McSPI_CS1/ GP[10]
J	EM_A[8]	EM_A[9]	**GP[26]**/ EM_A[20]	EM_D[15]	DV_{DDEMIF}	CV_{DD}	V_{SS}	V_{SS}	V_{SS}	RSV1	RSV2	USB_VBUS	USB_V_{DD1P3}	USB_DM
H	$\overline{EM\_WE}$	EM_A[7]	EM_D[7]	EM_WAIT5	DV_{DDEMIF}	V_{SS}	DV_{DDEMIF}	CV_{DD}	USB_ V_{SSA1P3}	USB_ V_{DDA1P3}	USB_ V_{SSA3P3}	USB_ V_{DDA3P3}	USB_V_{SS1P3}	USB_DP
G	EM_WAIT4	**GP[24]**/ EM_A[18]	EM_D[0]	**GP[25]**/ EM_A[19]	DV_{DDEMIF}	V_{SS}	V_{SS}	USB_V_{DDPLL}	USB_R1	USB_V_{SSREF}	USB_V_{SSPLL}	USB_V_{DDOSC}	USB_MXI	USB_MXO
F	EM_A[6]	**GP[23]**/ EM_A[17]	EM_D[2]	EM_D[9]	DV_{DDEMIF}	CV_{DD}	DV_{DDIO}	DV_{DDRTC}	V_{SS}	V_{SS}	USB_V_{SSOSC}	USB_LDOO	LDOI	LDOI
E	EM_A[2]	**GP[22]**/ EM_A[16]	EM_D[8]	$\overline{EM\_OE}$	EM_D[1]	DV_{DDEMIF}	$\overline{INT1}$	WAKEUP	V_{SS}	DSP_LDOO	V_{SS}	V_{SS}	V_{SS}	V_{SS}
D	EM_A[5]	EM_A[3]	EM_D[10]	EM_D[3]	EM_WAIT2	$\overline{RESET}$	V_{SS}	RTC_ CLKOUT	V_{SSA_PLL}	GPAIN0	V_{SS}	$\overline{DSP\_LDO\_EN}$	RSV16	RSV3
C	EM_A[4]	EM_A[1]	$\overline{EM\_CS4}$	EM_D[11]	$\overline{EM\_CS2}$	$\overline{INT0}$	CLK_SEL	CV_{DDRTC}	V_{SSRTC}	V_{DDA_PLL}	GPAIN3	RSV0	RSV5	RSV4
B	EM_BA[1]	EM_A[0]	$\overline{EM\_CS0}$/ $\overline{UHPI\_HDS1}$	$\overline{EM\_SDCAS}$/ $\overline{UHPI\_HCS}$	**EM_DQM0**/ UHPI_HBE0	EM_R/$\overline{W}$	SCL	SDA	RTC_XI	V_{SSA_ANA}	GPAIN2	LDOI	BG_CAP	V_{SSA_ANA}
A	EM_BA[0]	DV_{DDEMIF}	$\overline{EM\_CS5}$	$\overline{EM\_CS1}$/ $\overline{UHPI\_HDS2}$	DV_{DDEMIF}	$\overline{EM\_SDRAS}$/ $\overline{UHPI\_HAS}$	CLKOUT	CLKIN	RTC_XO	V_{DDA_ANA}	GPAIN1	ANA_LDOO	V_{SS}	V_{SS}

NOTE: Shaded pins indicate new functions on the C5517.

Figure 1. Pins With New Functions On C5517

4.5 Pins With New Functions

Table 4 provides the full list of the pins that are multiplexed with the new C5517 peripherals: McBSP, McSPI, and UHPI. Note that the SDRAM control signals (B3, B4, B5, A4, and A6) are multiplexed with UHPI control signals and can be programmed by the EBSR register [1C00h].

Note: The reset default is in **bold**.

Table 4. Pins With New Functions

Ball No.	C5517 Pin Name	C5515/05 Pin Name	Note
P1	**EM_DQM1**/UHPI_HBE1	EM_DQM1	Add: UHPI
P4	**SPI_CS0**/UHPI_HCNTL0	LCD_CS0_E0/SPI_CS0	Added: UHPI Removed: LCD
P5	**SPI_CS2**/UHPI_HR_NW	LCD_RW_WRB/SPI_CS2	Added: UHPI Removed: LCD
P6	**SPI_RX**/UHPI_HD[0]	LCD_D[0]/SPI_RX	Added: UHPI Removed: LCD
P7	**GP[12]**/UHPI_HD[2]	LCD_D[2]/GP[12]	Added: UHPI Removed: LCD
P9	**GP[15]**/UHPI_HD[5]	LCD_D[5]/GP[15]	Added: UHPI Removed: LCD
P10	**GP[17]**/UHPI_HD[7]	LCD_D[7]/GP[17]	Added: UHPI Removed: LCD
P11	**I2S2_FS**/UHPI_HD[9]/ GP[19]/SPI_CS0	LCD_D[9]/I2S2_FS/ GP[19]/SPI_CS0	Added: UHPI Removed: LCD
P12	**I2S2_DX**/UHPI_HD[11]/ GP[27]/SPI_TX	LCD_D[11]/I2S2_DX/ GP[27]/SPI_TX	Added: UHPI Removed: LCD
P13	**UART_CTS**/UHPI_HD[13]/ GP[29]/I2S3_FS	LCD_D[13]/UART_CTS/ GP[29]/I2S3_FS	Added: UHPI Removed: LCD
P14	**UART_TXD**/UHPI_HD[15]/ GP[31]/I2S3_DX	LCD_D[15]/UART_TXD/ GP[31]/I2S3_DX	Added: UHPI Removed: LCD
N2	**$\overline{\text{EM\_SDCKE}}$**/UHPI_HHWIL	EM_SDCKE	Added: UHPI
N3	**SPI_CLK**/UHPI_HINT	LCD_EN_RDB/SPI_CLK	Added: UHPI Removed: LCD
N4	**SPI_CS1**/UHPI_HCNTL1	LCD_CS1_EN1/SPI_CS1	Added: UHPI Removed: LCD
N5	**SPI_CS3**/UHPI_HRDY	LCD_RS/SPI_CS3	Added: UHPI Removed: LCD
N6	**SPI_TX**/UHPI_HD[1]	LCD_D[1]/SPI_TX	Added: UHPI Removed: LCD
N7	**GP[13]**/UHPI_HD[3]	LCD_D[3]/GP[13]	Added: UHPI Removed: LCD
N8	**GP[14]**/UHPI_HD[4]	LCD_D[4]/GP[14]	Added: UHPI Removed: LCD
N9	**GP[16]**/UHPI_HD[6]	LCD_D[6]/GP[16]	Added: UHPI Removed: LCD
N10	**I2S2_CLK**/UHPI_HD[8]/ GP[18]/SPI_CLK	LCD_D[8]/I2S2_CLK/ GP[18]/SPI_CLK	Added: UHPI Removed: LCD
N11	**I2S2_RX**/UHPI_HD[10]/ GP[20]/SPI_RX	LCD_D[10]/I2S2_RX/ GP[20]/SPI_RX	Added: UHPI Removed: LCD

Table 4. Pins With New Functions (continued)

Ball No.	C5517 Pin Name	C5515/05 Pin Name	Note
N12	**UART_RTS**/UHPI_HD[12]/ GP[28]/I2S3_CLK	LCD_D[12]/UART_RTS/ GP[28]/I2S3_CLK	Added: UHPI Removed: LCD
N13	**UART_RXD**/UHPI_HD[14]/ GP[30]/I2S3_RX	LCD_D[14]/UART_RXD/ GP[30]/I2S3_RX	Added: UHPI Removed: LCD
M10	**MMC0_D1**/I2S0_RX/ GP[3]/McBSP_DR	MMC0_D1/I2S0_RX/GP[3]	Added: McBSP
M11	**MMC0_CMD**/I2S0_FS/ GP[1]/McBSP_FSX	MMC0_CMD/I2S0_FS/GP[1]	Added: McBSP
M12	**MMC1_D1**/McSPI_SOMI/GP[9]	MMC1_D1/I2S1_RX/GP[9]	Added: McSPI Removed: I2S
M13	**MMC1_CLK**/McSPI_CLK/GP[6]	MMC1_CLK/I2S1_CLK/GP[6]	Added: McSPI Removed: I2S
M14	**MMC1_D0**/McSPI_SIMO/GP[8]	MMC1_D0/I2S1_DX/GP[8]	Added: McSPI Removed: I2S
L9	**MMC0_D0**/I2S0_DX/ GP[2]/McBSP_DX	MMC0_D0/I2S0_DX/GP[2]	Added: McBSP
L10	**MMC0_CLK**/I2S0_CLK/ GP[0]/McBSP_CLKX	MMC0_CLK/I2S0_CLK/GP[0]	Added: McBSP
L11	**MMC0_D3**/GP[5]/ McBSP_CLKR_CLKS	MMC0_D3/GP[5]	Added: McBSP
L12	**MMC0_D2**/GP[4]/ McBSP_FSR	MMC0_D2/GP[4]	Added: McBSP
L13	**MMC1_D3**/McSPI_CS2/GP[11]	MMC1_D3/GP[11]	Added: McSPI
L14	**MMC1_CMD**/McSPI_CS0/GP[7]	MMC1_CMD/I2S1_FS/GP[7]	Added: McSPI Removed: I2S
K14	**MMC1_D2**/McSPI_CS1/GP[10]	MMC1_D2/GP[10]	Added: McSPI
B3	**$\overline{\text{EM\_CS0}}$**/UHPI_HDS1	$\overline{\text{EM\_CS0}}$	Added: UHPI
B4	**$\overline{\text{EM\_SDCAS}}$**/UHPI_HCS	$\overline{\text{EM\_SDCAS}}$	
B5	**$\overline{\text{EM\_DQM0}}$**/UHPI_HBE0	$\overline{\text{EM\_DQM0}}$	
A4	**$\overline{\text{EM\_CS1}}$**/UHPI_HDS2	$\overline{\text{EM\_CS1}}$	
A6	**$\overline{\text{EM\_SDRAS}}$**/UHPI_HAS	$\overline{\text{EM\_SDRAS}}$	

4.6 Serial Port 0 Pin Mapping

The Serial Port 0 in the C5517 consists of six signals that support four different modes. By selecting one of these modes in the External Bus Selection Register [1C00h], the appropriate six signals are mapped to shared pins on the device.

- **MMC and SD mode:** All six signals of the MultiMedia Card and Secure Digital port are routed to the six external signals of the Serial Port 0.
- **I2S mode:** All four signals of the I2S module and 2 GPIO signals are routed to the six external signals of the Serial Port 0.
- **GPIO mode:** Six GPIO signals are routed to the six external signals of the Serial Port 0.
- **McBSP mode:** All six signals of the Multichannel Buffered Serial Port are routed to the six external signals of the Serial Port 0.

The selection of the Serial Port 0 is set by the External Bus Selection Register.

Table 5. Serial Port 0 Pin Multiplexing

Ball	SP0MODE00 (default)		SP0MODE01		SP0MODE10		SP0MODE11	
	C5517	C5515/05	C5517	C5515/05	C5517	C5515/05	C5517	C5515/05
L10	MMC0_CLK	MMC0_CLK	I2S0_CLK	I2S0_CLK	GPIO[0]	GPIO[0]	McBSP_CLKX	Reserved
M11	MMC0_CMD	MMC0_CMD	I2S0_FS	I2S0_FS	GPIO[1]	GPIO[1]	McBSP_FSX	Reserved
L9	MMC0_D0	MMC0_D0	I2S0_DX	I2S0_DX	GPIO[2]	GPIO[2]	McBSP_DX	Reserved
M10	MMC0_D1	MMC0_D1	I2S0_RX	I2S0_RX	GPIO[3]	GPIO[3]	McBSP_DR	Reserved
L12	MMC0_D2	MMC0_D2	GPIO[4]	GPIO[4]	GPIO[4]	GPIO[4]	McBSP_FSR	Reserved
L11	MMC0_D3	MMC0_D3	GPIO[5]	GPIO[5]	GPIO[5]	GPIO[5]	McBSP_CLKR or McBSP_CLKS (Bit 15 of EBSR register)	Reserved

4.7 Serial Port 1 Pin Mapping

The Serial Port 1 in the C5517 consists of six signals that support four different modes. By selecting one of these modes in the External Bus Selection Register [1C00h], the appropriate six signals are mapped to shared pins on the device.

- **MMC and SD mode:** All six signals of the MultiMedia Card and Secure Digital port are routed to the six external signals of the Serial Port 1.
- **McSPI mode:** All four signals of the McSPI module are routed to the four external signals of the Serial Port 1.
- **GPIO mode:** Six GPIO signals are routed to the six external signals of the Serial Port 1.

The selection of the Serial Port1 mode is set by the External Bus Selection Register.

Table 6. Serial Port 1 Pin Multiplexing

Ball	SP1MODE00 (default)		SP1MODE01		SP1MODE10	
	C5517	C5515/05	C5517	C5515/05	C5517	C5515/05
M13	MMC1_CLK	MMC1_CLK	McSPI_CLK	I2S1_CLK	GPIO[6]	GPIO[6]
L14	MMC1_CMD	MMC1_CMD	McSPI_CS0	I2S1_FS	GPIO[7]	GPIO[7]
M14	MMC1_D0	MMC1_D0	McSPI_SIMO	I2S1_DX	GPIO[8]	GPIO[8]
M12	MMC1_D1	MMC1_D1	McSPI_SOMI	I2S1_RX	GPIO[9]	GPIO[9]
K14	MMC1_D2	MMC1_D2	McSPI_CS1	GPIO[10]	GPIO[10]	GPIO[10]
L13	MMC1_D3	MMC1_D3	McSPI_CS2	GPIO[11]	GPIO[11]	GPIO[11]

4.8 Parallel Port Pin Mapping

Because UHPI replaces LCD, the parallel port comprises 28 signals that support seven different modes:

- **16-bit multiplexed UHPI:** All 28 signals of the UHPI module are routed to the 28 external signals of the Parallel Port.
- **6-Bit GPIO, SPI, UART, I2S and SDRAM:** Six GPIO, seven signals (four chip selects) of the SPI module, four signals of the UART module, four signals of the I2S module, and seven SDRAM controls signals are routed to the 28 external signals of the parallel port.
- **8-Bit GPIO, and SDRAM:** Eight GPIO and seven SDRAM controls signals are routed to the 28 external signals of the parallel port.
- **SPI, I2S and SDRAM:** Four signals of the SPI module, four signals of the I2S module and seven SDRAM controls signals are routed to the 28 external signals of the parallel port.
- **UART, I2S and SDRAM:** Four signals of the UART module, four signals of the I2S module, and seven SDRAM controls signals are routed to the 28 external signals of the parallel port.
- **UART, SPI and SDRAM:** Four signals of the UART module, four signals of the SPI module, and seven SDRAM controls signals are routed to the 28 external signals of the parallel port.
- **6-Bit GPIO, SPI, 2 I2S, and SDRAM:** Six GPIO, seven signals (four chip selects) of the SPI module, two sets of four signals of the I2S module, and seven SDRAM controls signals are routed to the 28 external signals of the parallel port.

The selection of the parallel port mode is set by the External Bus Selection Register.

Table 7. Parallel Port Pin Multiplexing

Ball	PPMODE 000		PPMODE 001		PPMODE 010		PPMODE 011		PPMODE 100		PPMODE 101		PPMODE 110	
	C5517	C5515/ 5505[1]	C5517[1]	C5515/ 5505	C5517	C5515/ 5505	C5517	C5515/ 5505	C5517	C5515/ 5505	C5517	C5515/ 5505	C5517	C5515/ 5505
N3	UHPI_ HINT	LCD_EN_ RDB	SPI_CLK	SPI_CLK	Reserved	LCD_EN_ RDB	Reserved	LCD_EN_ RDB	Reserved	LCD_EN_ RDB	Reserved	LCD_EN_ RDB	SPI_CLK	SPI_CLK
P6	UHPI_ HD[0]	LCD_D[0]	SPI_RX	SPI_RX	Reserved	LCD_D[0]	Reserved	LCD_D[0]	Reserved	LCD_D[0]	Reserved	LCD_D0	SPI_RX	SPI_RX
N6	UHPI_ HD[1]	LCD_D[1]	SPI_TX	SPI_TX	Reserved	LCD_D[1]	Reserved	LCD_D[1]	Reserved	LCD_D[1]	Reserved	LCD_D1	SPI_TX	SPI_TX
P7	UHPI_ HD[2]	LCD_D[2]	GPIO[12]	GPIO12	Reserved	LCD_D[2]	Reserved	LCD_D[2]	Reserved	LCD_D[2]	Reserved	LCD_D2	GPIO[12]	GPIO[12]
N7	UHPI_ HD[3]	LCD_D[3]	GPIO[13]	GPIO13	Reserved	LCD_D[3]	Reserved	LCD_D[3]	Reserved	LCD_D[3]	Reserved	LCD_D3	GPIO[13]	GPIO[13]
N8	UHPI_ HD[4]	LCD_D[4]	GPIO[14]	GPIO14	Reserved	LCD_D[4]	Reserved	LCD_D[4]	Reserved	LCD_D[4]	Reserved	LCD_D4	GPIO[14]	GPIO[14]
P9	UHPI_ HD[5]	LCD_D[5]	GPIO[15]	GPIO15	Reserved	LCD_D[5]	Reserved	LCD_D[5]	Reserved	LCD_D[5]	Reserved	LCD_D5	GPIO[15]	GPIO[15]
N9	UHPI_ HD[6]	LCD_D[6]	GPIO[16]	GPIO16	Reserved	LCD_D[6]	Reserved	LCD_D[6]	Reserved	LCD_D[6]	Reserved	LCD_D6	GPIO[16]	GPIO[16]
P10	UHPI_ HD[7]	LCD_D[7]	GPIO[17]	GPIO17	Reserved	LCD_D[7]	Reserved	LCD_D[7]	Reserved	LCD_D[7]	Reserved	LCD_D7	GPIO[17]	GPIO[17]
N10	UHPI_ HD[8]	LCD_D[8]	I2S2_CLK	I2S2_CLK	GPIO18	GPIO[18]	SPI_CLK	SPI_CLK	I2S2_CLK	I2S2_CLK	SPI_CLK	SPI_CLK	I2S2_CLK	I2S2_CLK
P11	UHPI_ HD[9]	LCD_D[9]	I2S2_FS	I2S2_FS	GPIO19	GPIO[19]	SPI_CS0	SPI_CS0	I2S2_FS	I2S2_FS	SPI_CS0	SPI_CS0	I2S2_FS	I2S2_FS
N11	UHPI_ HD[10]	LCD_D[10]	I2S2_RX	I2S2_RX	GPIO20	GPIO[20]	SPI_RX	SPI_RX	I2S2_RX	I2S2_RX	SPI_RX	SPI_RX	I2S2_RX	I2S2_RX
P12	UHPI_ HD[11]	LCD_D[11]	I2S2_DX	I2S2_DX	GPIO27	GPIO[27]	SPI_TX	SPI_TX	I2S2_DX	I2S2_DX	SPI_TX	SPI_TX	I2S2_DX	I2S2_DX
N12	UHPI_ HD[12]	LCD_D[12]	UART_ RTS	UART_ RTS	GPIO28	GPIO[28]	I2S3_CLK	I2S3_CLK	UART_ RTS	UART_ RTS	UART_ RTS	UART_ RTS	I2S3_CLK	I2S3_CLK
P13	UHPI_ HD[13]	LCD_D[13]	UART_ CTS	UART_ CTS	GPIO29	GPIO[29]	I2S3_FS	I2S3_FS	UART_ CTS	UART_ CTS	UART_ CTS	UART_ CTS	I2S3_FS	I2S3_FS
N13	UHPI_ HD[14]	LCD_D[14]	UART_ RXD	UART_ RXD	GPIO30	GPIO[30]	I2S3_RX	I2S3_RX	UART_ RXD	UART_ RXD	UART_ RXD	UART_ RXD	I2S3_RX	I2S3_RX
P14	UHPI_ HD[15]	LCD_D[15]	UART_ TXD	UART_ TXD	GPIO31	GPIO[31]	I2S3_DX	I2S3_DX	UART_ TXD	UART_ TXD	UART_ TXD	UART_ TXD	I2S3_DX	I2S3_DX
P4	UHPI_ HCNTL0	LCD_CS0	SPI_CS0	SPI_CS0	Reserved	LCD_CS0	Reserved	LCD_CS0	Reserved	LCD_CS0	Reserved	LCD_CS0	SPI_CS0	SPI_CS0

(1) Default

Table 7. Parallel Port Pin Multiplexing (continued)

Ball	PPMODE 000		PPMODE 001		PPMODE 010		PPMODE 011		PPMODE 100		PPMODE 101		PPMODE 110	
	C5517	C5515/ 5505[1]	C5517[1]	C5515/ 5505	C5517	C5515/ 5505	C5517	C5515/ 5505	C5517	C5515/ 5505	C5517	C5515/ 5505	C5517	C5515/ 5505
N4	UHPI_ HCNTL1	LCD_CS1	SPI_CS1	SPI_CS1	Reserved	LCD_CS1	Reserved	LCD_CS1	Reserved	LCD_CS1	Reserved	LCD_CS1	SPI_CS1	SPI_CS1
P5	UHPI_ HR_NW	LCD_RW_ WRB	SPI_CS2	SPI_CS2	Reserved	LCD_RW_ WRB	Reserved	LCD_RW_ WRB	Reserved	LCD_RW_ WRB	Reserved	LCD_RW_ WRB	SPI_CS2	SPI_CS2
N5	UHPI_ HRDY	LCD_RS	SPI_CS3	SPI_CS3	Reserved	LCD_RS	Reserved	LCD_RS	Reserved	LCD_RS	Reserved	LCD_RS	SPI_CS3	SPI_CS3
B5	UHPI_ HBE0	EM_ DQM[0]	EM_ DQM[0]	EM_ DQM[0]	EM_ DQM[0]	EM_ DQM[0]	EM_ DQM[0]	EM_ DQM[0]	EM_ DQM[0]	EM_ DQM[0]	EM_ DQM[0]	EM_ DQM[0]	EM_ DQM[0]	EM_ DQM[0]
P1	UHPI_ HBE1	EM_ DQM[1]	EM_ DQM[1]	EM_ DQM[1]	EM_ DQM[1]	EM_ DQM[1]	EM_ DQM[1]	EM_ DQM[1]	EM_ DQM[1]	EM_ DQM[1]	EM_ DQM[1]	EM_ DQM[1]	EM_ DQM[1]	EM_ DQM[1]
A6	UHPI_ HAS	$\overline{\text{EM\_SDRAS}}$	$\overline{\text{EM\_SDRAS}}$	$\overline{\text{EM\_SDRAS}}$	$\overline{\text{EM\_SDRAS}}$	$\overline{\text{EM\_SDRAS}}$	$\overline{\text{EM\_SDRAS}}$	$\overline{\text{EM\_SDRAS}}$	$\overline{\text{EM\_SDRAS}}$	$\overline{\text{EM\_SDRAS}}$	$\overline{\text{EM\_SDRAS}}$	$\overline{\text{EM\_SDRAS}}$	$\overline{\text{EM\_SDRAS}}$	$\overline{\text{EM\_SDRAS}}$
B4	UHPI_ HCS	$\overline{\text{EM\_SDCAS}}$	$\overline{\text{EM\_SDCAS}}$	$\overline{\text{EM\_SDCAS}}$	$\overline{\text{EM\_SDCAS}}$	$\overline{\text{EM\_SDCAS}}$	$\overline{\text{EM\_SDCAS}}$	$\overline{\text{EM\_SDCAS}}$	$\overline{\text{EM\_SDCAS}}$	$\overline{\text{EM\_SDCAS}}$	$\overline{\text{EM\_SDCAS}}$	$\overline{\text{EM\_SDCAS}}$	$\overline{\text{EM\_SDCAS}}$	$\overline{\text{EM\_SDCAS}}$
B3	UHPI_ HDS1	$\overline{\text{EM\_CS0}}$	$\overline{\text{EM\_CS0}}$	$\overline{\text{EM\_CS0}}$	$\overline{\text{EM\_CS0}}$	$\overline{\text{EM\_CS0}}$	$\overline{\text{EM\_CS0}}$	$\overline{\text{EM\_CS0}}$	$\overline{\text{EM\_CS0}}$	$\overline{\text{EM\_CS0}}$	$\overline{\text{EM\_CS0}}$	$\overline{\text{EM\_CS0}}$	$\overline{\text{EM\_CS0}}$	$\overline{\text{EM\_CS0}}$
A4	UHPI_ HDS2	$\overline{\text{EM\_CS1}}$	$\overline{\text{EM\_CS1}}$	$\overline{\text{EM\_CS1}}$	$\overline{\text{EM\_CS1}}$	$\overline{\text{EM\_CS1}}$	$\overline{\text{EM\_CS1}}$	$\overline{\text{EM\_CS1}}$	$\overline{\text{EM\_CS1}}$	$\overline{\text{EM\_CS1}}$	$\overline{\text{EM\_CS1}}$	$\overline{\text{EM\_CS1}}$	$\overline{\text{EM\_CS1}}$	$\overline{\text{EM\_CS1}}$
N2	UHPI_ HHWIL	EM_ SDCKE	EM_ SDCKE	EM_ SDCKE	EM_ SDCKE	EM_ SDCKE	EM_ SDCKE	EM_ SDCKE	EM_ SDCKE	EM_ SDCKE	EM_ SDCKE	EM_ SDCKE	EM_ SDCKE	EM_ SDCKE

4.9 External Bus Selection Registers (EBSR)

The External Bus Selection Register (EBSR) determines the mapping of the UHPI, I2S1, I2S2, UART, SPI, McBSP, McSPI, and GPIO signals to 28 signals of the external parallel port pins. It also determines the mapping of the I2S, McBSP, McSPI, GPIO, or MMC and SD ports to serial port 0 pins and serial port 1 pins. The EBSR register is located at port address 1C00h. Once the bit fields of this register are changed, the routing of the signals takes place on the next CPU clock cycle.

For more details on the External Bus Selection Register (EBSR), see the chapter *System Control* in *TMS320C5517 Digital Signal Processor Technical Reference Manual* (literature number SPRUH16).

5 Clocking

5.1 Clock Source

On the C5515/05, the on-chip RTC oscillator and the CLKIN port were the two sources of the PLL input. On the C5517, the on-chip USB oscillator and the CLKIN port are the two sources of the PLL clock input. The on-chip RTC oscillator drives only the RTC module.

When CLK_SEL = 0 at reset, the on-chip USB oscillator is automatically enabled and used as the source of PLL input clock. In this configuration, the USB oscillator cannot be turned off.

When CLK_SEL = 1 at reset, the external LVCMOS compatible clock input fed into the CLKIN pin will be used as the source of PLL. The on-chip USB oscillator is automatically disabled but can be enabled by writing 0 to the bit 2 of USB System Control Register (1C32h). The USB Oscillator Disable bit reflects the status of the CLK_SEL pin at reset.

For more details on the USB System Control Register (USBSCR), see the chapter *System Control* in *TMS320C5517 Digital Signal Processor Technical Reference Manual* (literature number SPRUH16).

Table 8. PLL Reference Clock Source

CLK_SEL	PLL Clock Source	Frequency Supported
0	USB Oscillator	12 MHz
1	CLKIN Pin	0–30 MHz

5.2 PLL Power (VDDA_PLL)

On the C5515/05, the ANA_LDO can provide a regulated 1.3 V to both VDDA_PLL and VDDA_ANA. On the C5517, however, the VDDA_PLL must be powered externally. The new PLL in the C5517 consumes more power than the PLL in the C5515/05, typically ~5mA at 312 MHz.

5.3 PLL Changes

The PLL in the C5517 is different than for the C5515/05. The new PLL has an internal input reference divider and a post-divider valid frequency range of 1.7–6.79 MHz.

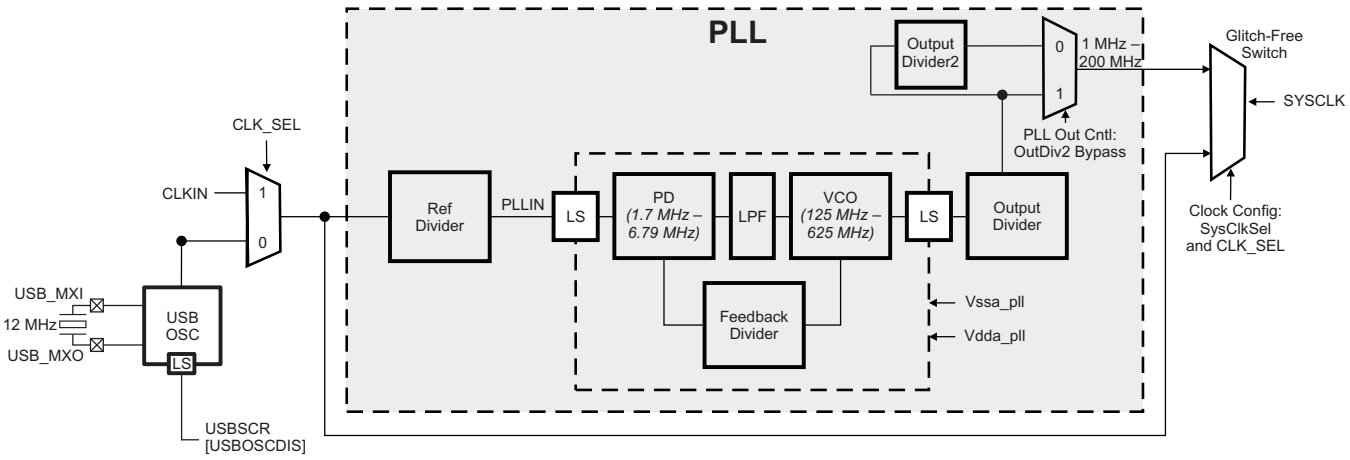

Figure 2. System PLL Block Diagram

The output frequency of the PLL is given by Equation 1:

$$\text{SystemClock} = \text{InputClock} \times \left[\frac{\left(\frac{\text{PLLM}}{256} + 1 \right)}{(\text{RD}+1) \times (0\text{D}+1) \times 2(0\text{D2}+1)} \right] \quad (1)$$

5.4 PLL Registers

To migrate from C5515/05 to C5517, the PLL registers configuration must be updated to get a suitable output frequency. The sequence of configuring PLL registers has not been changed.

The PLL registers include:

- PLL Multiplier Register (PMR)
- PLL Input Control Register (PICR)
- PLL Control Register (PCR)
- PLL Output Divider Register (PODCR)

For more details on the PLL registers, see the chapter *System Control* in *TMS320C5517 Digital Signal Processor Technical Reference Manual* (literature number SPRUH16).

5.5 Initializing PLL From PLL Power Down

If the PLL is powered down (PLLPWRDN (bit 13) is set to 1 in PLL Control Register (1C22h)), perform the following procedure to initialize the PLL:

1. The PLL should be held in reset and in bypass mode. If not:
   (a) Set SYSCLKSEL (bit 0) to 0 in Clock Configuration Register 2 (1C1Fh) to switch the PLL to bypass mode.
   (b) Wait 4 clock cycles to ensure that the PLL has switched to bypass mode.
   (c) Set PLLRST (bit 14) to 1 in PLL Control Register.
2. Clear PLLPWRDN in PLL Control Register to power up the analog circuitry in the PLL.
3. Program the desired values for:
   - Multiplier value (bit 15) and reference divider (bits 5–0) in PLL Input Control Register (1C21h)
   - Output Divider (bits 2–0) and Output Divider2 (bits 15–11) in PLL Output Divider Control Register (1C23h)
4. Clear the PLL reset bit in PLL Control Register.
5. Wait for the minimum lock time.
6. Clear SYSCLKSEL in Clock Configuration Register 2 to remove the PLL from bypass mode.

5.6 Changing PLL Multiplier

If the PLL is not powered down (PLL PWRDN (bit 13) is set to 0 in PLL Control Register (1C22h)), perform the following procedure to change the PLL:

1. Set SYSCLKSEL (bit 0) to 0 in Clock Configuration Register 2 (1C1Fh) to switch the PLL to bypass mode.
2. Wait 4 clock cycles to ensure that the PLL has switched to bypass mode.
3. Set PLLRST (bit 14) to 1 in PLL Control Register.
4. Program the desired values for:
   - Multiplier value (bit 15) and reference divider (bits 5–0) in PLL Input Control Register (1C21h)
   - Output Divider (bits 2–0) and Output Divider2 (bits 15–11) in PLL Output Divider Control Register (1C23h)
5. Clear the PLL reset bit in PLL Control Register.
6. Wait for the minimum lock time.
7. Clear SYSCLKSEL in Clock Configuration Register 2 to remove the PLL from bypass mode.

5.7 USB Oscillator Stabilization

At power-up, crystal oscillator circuits will typically oscillate at a very high frequency before settling to the desired crystal frequency. The C5517 modified the ripple counter circuit that gates clocks to the device while the USB oscillator is stabilizing. When CLK_SEL is low at reset, the USB oscillator is selected as the clock source to the PLL chip and this stabilization circuit must delay clocks for at least 10 mS.

5.8 Peripheral Reset

All peripherals can be reset through software by the Peripheral Reset Control Register. The Peripheral Software Reset Counter Register controls the number of system clock cycles that will maintain the peripheral reset signal low once activated by the corresponding Peripheral Reset Control Register. On the C5517, some of these bits are changed by the addition of McBSP and McSPI.

For more details on the Peripheral Software Reset Counter Register (PSRCR) and Peripheral Reset Control Register (PRCR), see the chapter *System Control* in *TMS320C5517 Digital Signal Processor Technical Reference Manual* (literature number SPRUH16).

5.9 Clock Stop Request and Acknowledge

On the C5517, McBSP uses a clock request and acknowledge mechanism to stop the clocks. Thus, additional bits are added to the Peripheral Clock Stop Request and Acknowledge Register. The Peripheral Clock Stop Request and Acknowledge Register is used by the EMIF, USB, McBSP, McSPI, UHPI, and UART to create a handshake system to request permission to stop the clock. This handshake ensures that current bus transactions are completed before the clock is stopped.

To stop the clock to the EMIF or USB, set the corresponding clock stop request bit in the CLKSTOP register, then wait for the peripheral to set the corresponding clock stop acknowledge bit. Once this bit is set, you can idle the corresponding clock in the PCGCR1 and PCGCR2.

To stop the clock to the UHPI, McBSP, or UART, set the corresponding clock stop request bit in the CLKSTOP register, then wait for the peripheral to set the corresponding clock stop acknowledge bit. Once this bit is set, the corresponding clock is also idle at the same time. Setting the corresponding clock gating in the PCGCR1 and PCGCR2 is not required.

To enable the clock to the EMIF, UHPI, McBSP, McSPI, USB, or UART, first enable the clock to the peripheral through PCGCR1 or PCGCR2, then clear the corresponding clock stop request bit in the CLKSTOP register.

For more details on the CLKSTOP1 and CLKSTOP2 registers, see the chapter *System Control* in *TMS320C5517 Digital Signal Processor Technical Reference Manual* (literature number SPRUH16).

5.10 Peripheral Clock Gating Configuration Register

The replacement of the McSPI for I2S1 and the addition of McBSP require changes to the Peripheral Clock Gating Configuration Register.

The Peripheral Clock Gating Configuration Register dictates what portions of the device peripherals will be disabled. In contrast to the Idle Control Register, these bits take effect immediately and do not require an idle instruction.

For more details on the Peripheral Clock Gating Configuration Registers (PCGCR1/2), see the chapter *System Control* in *TMS320C5517 Digital Signal Processor Technical Reference Manual* (literature number SPRUH16).

6 I/Os

6.1 I/O Reset States

On the C5517, all digital I/O pins will be in a high-impedance state while the RESETN pin is held active (low). They will return to their reset conditions at 65535 CPU cycles if CLK_SEL = 1 and 131071 CPU cycles if CLK_SEL = 0 after the RESETN pin is deactivated (high).

For more details, see the section titled *Pin Behavior at Reset* in *TMS320C5517 Fixed-Point Digital Signal Processor* (literature number SPRS727).

When the bidirectional signals are configured as inputs or the outputs are in a high-impedance state, the input pads are in floating. To prevent floating inputs and to minimize I/O power, the C5517 offers individual configuration of the internal pullup and pulldown signal of the bidirectional I/Os.

6.2 Internal Pullup and Pulldown for I/O Pins

On the C5517, all bidirectional pins are capable of individual configuring internal pullups (IPU) or pulldowns (IPD) capability comparing to that of the C5515/05. Table 9 shows the C5517 I/O pins and the configuration system register connections. Note that the pulldown control is independent of the Serial Port or Parallel Port Routing. The pullup or pulldown is enabled at reset.

Table 9. I/O Pin List, Pull, and Register Description

Terminal Name In C5517	Ball	I/O Type in C5517	IPU and IPD C5517	IPU and IPD C5515/05	IPU and IPD Register In C5517
GP[26]/EM_A[20]	J3	I/O/Z, IPD, BH	Yes	Yes	0x1C18[5]
GP[25]/EM_A[19]	G4	I/O/Z, IPD, BH	Yes	Yes	0x1C18[4]
GP[24]/EM_A[18]	G2	I/O/Z, IPD, BH	Yes	Yes	0x1C18[3]
GP[23]/EM_A[17]	F2	I/O/Z, IPD, BH	Yes	Yes	0x1C18[2]
GP[22]/EM_A[16]	E2	I/O/Z, IPD, BH	Yes	Yes	0x1C18[1]
GP[21]/EM_A[15]	N1	I/O/Z, IPD, BH	Yes	Yes	0x1C18[0]
EM_A[14:0]	M1, L1, K1, K2, L2, J2, J1, H2, F1, D1, C1, D2, E1, C2, B2	I/O/Z, IPD, BH	Yes	No	0x1C4D[14:0]
EM_CS[5:4]	A3, C3	I/O/Z, IPD, BH	Yes	No	0x1C4F[1:0]
$\overline{\text{EM\_CS[3:2]}}$	M4, C5	I/O/Z, IPD, BH	Yes	No	0x1C4F[3:2]
$\overline{\text{EM\_WE}}$	H1	I/O/Z, IPD, BH	Yes	No	0x1C4F[4]
$\overline{\text{EM\_OE}}$	E4	I/O/Z, IPD, BH	Yes	No	0x1C4F[5]
$\overline{\text{EM\_R/W}}$	B6	I/O/Z, IPD, BH	Yes	No	0x1C4F[6]
EM_DQM1/UHPI_HBE1	P1	I/O/Z, IPD, BH	Yes	No	0x1C4F[8]
EM_DQM0/UHPI_HBE0	B5	I/O/Z, IPD, BH	Yes	No	0x1C4F[7]
EM_BA[1:0]	B1,A1	I/O/Z, IPD, BH	Yes	No	0x1C4F[10:9]
EM_WAIT[5:4]	H4,G1	I/O/Z, IPD, BH	Yes	No	0x1C4F[12:11]
$\overline{\text{EM\_WAIT[3:2]}}$	K6,D5	I/O/Z, IPD, BH	Yes	No	0x1C4F[13:12]
EM_SDCLK	M3	I/O/Z, IPD, BH	Yes	No	0x1C50[0]
EM_SDCKE/UHPI_HHWIL	N2	I/O/Z, IPD, BH	Yes	No	0x1C50[1]
$\overline{\text{EM\_SDCAS}}$/UHPI_HCS	B4	I/O/Z, IPD, BH	Yes	No	0x1C50[2]
$\overline{\text{EM\_SDRAS}}$/UHPI_HAS	A6	I/O/Z, IPD, BH	Yes	No	0x1C50[3]
$\overline{\text{EM\_CS1}}$/UHPI_HDS2	A4	I/O/Z, IPD, BH	Yes	No	0x1C50[5]
$\overline{\text{EM\_CS0}}$/UHPI_HDS1	B3	I/O/Z, IPD, BH	Yes	No	0x1C50[4]
EM_D[15:0]	J4, K3, K4, L3, C4, D3, F4, E3, H3, K5, M2, L4, D4, F3, E5, G3	I/O/Z, IPD, BH	Yes	No	0x1C4C[15:0]
$\overline{\text{INT[1:0]}}$	E7,C6	I, IPU, BH	Yes	Yes	0x1C18[14:13]
$\overline{\text{RESET}}$	D6	I, IPU, BH	Yes	Yes	0x1C18[12]
MMC0_D3/GP[5]/ McBSP_CLKR_CLKS	L11	I/O/Z, IPD, BH	Yes	Yes	0x1C17[5]

Table 9. I/O Pin List, Pull, and Register Description (continued)

Terminal Name In C5517	Ball	I/O Type in C5517	IPU and IPD C5517	IPU and IPD C5515/05	IPU and IPD Register In C5517
MMC0_D2/GP[4]/ McBSP_FSR	L12	I/O/Z, IPD, BH	Yes	Yes	0x1C17[4]
MMC0_D1/I2S0_RX/ GP[3]/McBSP_DR	M10	I/O/Z, IPD, BH	Yes	Yes	0x1C17[3]
MMC0_D0/I2S0_DX/ GP[2]/McBSP_DX	L9	I/O/Z, IPD, BH	Yes	Yes	0x1C17[2]
MMC0_CMD/I2S0_FS/ GP[1]/McBSP_FSX	M11	I/O/Z, IPD, BH	Yes	Yes	0x1C17[1]
MMC0_CLK/I2S0_CLK/ GP[0]/McBSP_CLKX	L10	I/O/Z, IPD, BH	Yes	Yes	0x1C17[0]
MMC1_D3/McSPI_CS2/GP[11]	L13	I/O/Z, IPD, BH	Yes	Yes	0x1C17[13]
MMC1_D2/McSPI_CS1/GP[10]	K14	I/O/Z, IPD, BH	Yes	Yes	0x1C17[12]
MMC1_D1/McSPI_SOMI/GP[9]	M12	I/O/Z, IPD, BH	Yes	Yes	0x1C17[11]
MMC1_D0/McSPI_SIMO/GP[8]	M14	I/O/Z, IPD, BH	Yes	Yes	0x1C17[10]
MMC1_CMD/McSPI_CS0/GP[7]	L14	I/O/Z, IPD, BH	Yes	Yes	0x1C17[9]
MMC1_CLK/McSPI_CLK/GP[6]	M13	I/O/Z, IPD, BH	Yes	Yes	0x1C17[8]
SPI_CLK/UHPI_HINT	N3	I/O/Z, IPD, BH	Yes	No	0x1C50[12]
SPI_CS3/UHPI_HRDY	N5	I/O/Z, IPD, BH	Yes	No	0x1C50[11]
SPI_CS2/UHPI_HR_NW	P5	I/O/Z, IPD, BH	Yes	No	0x1C50[10]
SPI_CS1/UHPI_HCNTL1	N4	I/O/Z, IPD, BH	Yes	No	0x1C50[9]
SPI_CS0/UHPI_HCNTL0	P4	I/O/Z, IPD, BH	Yes	No	0x1C50[8]
UART_TXD/UHPI_HD[15]/ GP[31]/I2S3_DX	P14	I/O/Z, IPD, BH	Yes	Yes	0x1C19[15]
UART_RXD/UHPI_HD[14]/ GP[30]/I2S3_RX	N13	I/O/Z, IPD, BH	Yes	Yes	0x1C19[14]
UART_CTS/UHPI_HD[13]/ GP[29]/I2S3_FS	P13	I/O/Z, IPD, BH	Yes	Yes	0x1C19[13]
UART_RTS/UHPI_HD[12]/ GP[28]/I2S3_CLK	N12	I/O/Z, IPD, BH	Yes	Yes	0x1C19[12]
I2S2_DX/UHPI_HD[11]/ GP[27]/SPI_TX	P12	I/O/Z, IPD, BH	Yes	Yes	0x1C19[11]

Table 9. I/O Pin List, Pull, and Register Description (continued)

Terminal Name In C5517	Ball	I/O Type in C5517	IPU and IPD C5517	IPU and IPD C5515/05	IPU and IPD Register In C5517
I2S2_RX/UHPI_HD[10]/ GP[20]/SPI_RX	N11	I/O/Z, IPD, BH	Yes	Yes	0x1C19[10]
I2S2_FS/UHPI_HD[9]/ GP[19]/SPI_CS0	P11	I/O/Z, IPD, BH	Yes	Yes	0x1C19[9]
I2S2_CLK/UHPI_HD[8]/ GP[18]/SPI_CLK	N10	I/O/Z, IPD, BH	Yes	Yes	0x1C19[8]
GP[17]/UHPI_HD[7]	P10	I/O/Z, IPD, BH	Yes	Yes	0x1C19[7]
GP[16]/UHPI_HD[6]	N9	I/O/Z, IPD, BH	Yes	Yes	0x1C19[6]
GP[15]/UHPI_HD[5]	P9	I/O/Z, IPD, BH	Yes	Yes	0x1C19[5]
GP[14]/UHPI_HD[4]	N8	I/O/Z, IPD, BH	Yes	Yes	0x1C19[4]
GP[13]/UHPI_HD[3]	N7	I/O/Z, IPD, BH	Yes	Yes	0x1C19[3]
GP[12]/UHPI_HD[2]	P7	I/O/Z, IPD, BH	Yes	Yes	0x1C19[2]
SPI_TX/UHPI_HD[1]	N6	I/O/Z, IPD, BH	Yes	No	0x1C19[1]
SPI_RX/UHPI_HD[0]	P6	I/O/Z, IPD, BH	Yes	No	0x1C19[0]
XF	M8	I/O/Z, IPU, BH	No	No	No change
CLKOUT	A7	I/O/Z, IPD, BH	Yes	No	IPD is controlled by sysreg 0x1C24[15]. When the pin is tri-stated, the pulldown comes ON (and vice-versa).
CLKIN	A8	I, IPD, BH	Yes	No	0x1C18[15]
CLKSEL	C7	I, IPD, BH	No	No	No change
TCK	M6	I, IPU, BH	Yes	Yes	0x1C18[8]
TDI	L7	I, IPU, BH	Yes	Yes	0x1C18[10]
TDO	M7	I/O/Z, IPU, BH	Yes	No	0x1C18[6]
TMS	L8	I, IPU, BH	Yes	Yes	0x1C18[9]
$\overline{\text{TRST}}$	M9	I, IPD, BH	Yes	No	0x1C18[7]
EMU[1:0]	M5,L6	I/O/Z, IPU, BH	Yes	Yes	0x1C18[11]

7 CLKOUT

NOTE: CLKOUT is only for debug purposes and is not a clock source to external devices.

7.1 Changing Clock Source State

On the C5517 the new implementation will:

- Allow clock gating in a low state (the CLKOUT clock will stop in the low state)
- Support glitchless clock switching when the user software implements the following protocol: first gated CLKOUT, then changes the CLKOUT source, and then un-gated the CLKOUT.
- A new divider in the CLKOUT path will allow dividing any of the existing clock sources by even divide ratios: 2, 4, 6, 8, 10, or bypass the divider.

For more details on the CLKOUT Configuration Register (CLKOUTCR), see the chapter *System Control* in *TMS320C5517 Digital Signal Processor Technical Reference Manual* (literature number SPRUH16).

8 Timer

8.1 Adding Timer Reset State

In order to remove the possibility of glitches in the timer counter clock source, the timers need to be held in reset while the clock source is changed. C5517 adds a timer reset bit in the Timer Control Register to reset the timer for each individual timer (Timer0, Timer1, and Timer2).

For more details on the Timer Control Registers (T*n*CR), see the chapter *32-Bit Timer/Watchdog Timer* in *TMS320C5517 Digital Signal Processor Technical Reference Manual* (literature number SPRUH16).

8.2 Muxing of Timer Interrupts

C5517 allows the routing of the timer interrupts through the Timer Interrupt Selection Register.

For more details on the Timer Interrupt Selection Register (TISR), see the chapter *System Control* in *TMS320C5517 Digital Signal Processor Technical Reference Manual* (literature number SPRUH16).

8.3 Adding an External Clock to Timers

The C5517 allows adding an external input clock to the timers through the Timer Input Selection Register. The setting of this register overrides any other GPIO routing. This prevents the programmer from inadvertently clearing an interrupt by writing to other bits in this register.

For more details on the Timer Input Selection Register (T*n*INSR), see the chapter *32-Bit Timer/Watchdog Timer* in *TMS320C5517 Digital Signal Processor Technical Reference Manual* (literature number SPRUH16).

9 Bootloader

The C5517 bootloader includes the following changes to support new features:

- Supports new PLL
- Adds support for unencrypted boot image from:
  - McSPI
  - UHPI
  - SD and SDHC
  - eMMC and MMC
  - UART
- Supports 16-bit multiplexed UHPI boot mode
- EM_A[20:15]/GPIO[26:21] pins will be latched to determine boot mode

In order to determine which boot mode to invoke, C5517 latches the value of EM_A[20:15]/GPIO[26:21] into the BootMode[5:0] bits in the BootMode Register [1C34h] at reset. This register is a read-only register for the bootloader to determine boot mode options.

For more details, see the section titled *BootMode Implementation and Requirements* in *TMS320C5517 Fixed-Point Digital Signal Processor* (literature number SPRS727).

Table 10. BootMode Peripheral Boot Source Configuration when CLK_SEL = 1

Boot Mode Description	BootMode[5:4]	BootMode[3:0]	System Clock when CLK_SEL = 1
NOR 16-bit data Boot	00	0000	11.2896 MHz
			12.0 or 12.288 MHz
			16.8 MHz
			19.2 MHz
NAND 8-bit or 16-bit data Boot	00	0001	11.2896 MHz
			12.0 or 12.288 MHz
			16.8 MHz
			19.2 MHz
UART0 9600 baud Boot	00	0010	11.2896 MHz
	01		12.0 or 12.288 MHz
	10		16.8 MHz
	11		19.2 MHz
UART0 57600 baud Boot	00	0011	11.2896 MHz
	01		12.0 or 12.288 MHz
	10		16.8 MHz
	11		19.2 MHz
UART0 115200 baud Boot	00	0100	11.2896 MHz
	01		12.0 or 12.288 MHz
	10		16.8 MHz
	11		19.2 MHz
SPI 16-bit or 24-bit address Boot, < 1MHz	00	0101	11.2896 MHz
	01		12.0 or 12.288 MHz
	10		16.8 MHz
	11		19.2 MHz
SPI 16-bit or 24-bit address Boot, < 10 MHz	00	0110	11.2896 MHz
	01		12.0 or 12.288 MHz
	10		16.8 MHz
	11		19.2 MHz
Reserved	00	0111	N/A

Table 10. BootMode Peripheral Boot Source Configuration when CLK_SEL = 1 (continued)

Boot Mode Description	BootMode[5:4]	BootMode[3:0]	System Clock when CLK_SEL = 1
I2C 16-bit or 24-bit address Boot, 400kHz	00	1000	11.2896 MHz
	01		12.0 or 12.288 MHz
	10		16.8 MHz
	11		19.2 MHz
SD and SDHC eMMC and MMC Controller 0 Boot	00	1001	11.2896 MHz
			12.0 or 12.288 MHz
			16.8 MHz
			19.2 MHz
SD and SDHC eMMC and MMC Controller 1 Boot	00	1010	11.2896 MHz
			12.0 or 12.288 MHz
			16.8 MHz
			19.2 MHz
Reserved	00	1011	N/A
UHPI 16-bit multiplexed mode Boot	00	1100	11.2896 MHz
			12.0 or 12.288 MHz
			16.8 MHz
			19.2 MHz
McSPI 24-bit address serial flash Boot, 10 MHz	00	1101	11.2896 MHz
			12.0 or 12.288 MHz
			16.8 MHz
			19.2 MHz
McSPI 24-bit address serial flash Boot, 40 MHz	00	1110	11.2896 MHz
			12.0 or 12.288 MHz
			16.8 MHz
			19.2 MHz
USB Boot	00	1111	11.2896 MHz
			12.0 or 12.288 MHz
			16.8 MHz
			19.2 MHz

10 Memory Map

The C5517 adds the capability to access the byte address range of FE0000h – FFFFFFh via the EMIF's external memory space on EM_CS5. On the C5515/05, the byte address range FE0000h – FFFFFFh was used for the on-chip ROM, regardless of MPNMC bit status.

When the MPNMC bit field of the ST3 status register is cleared (by default), the byte address range of FE0000h – FFFFFFh is used for the on-chip ROM. When the MPNMC bit field of the ST3 status register is set through software, the on-chip ROM is disabled and not present in the memory map, and the byte address range of FE0000h – FFFFFFh is directed to the EMIF's external memory space on EM_CS5.

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Date	Revision	Notes
April 2014	*	Initial Release

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