Application Report
SPRABA8–June 2010

PCB Assembly Guidelines for 0.5mm Package-on-Package Applications Processor, Part II

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ABSTRACT

Once the main printed circuit board (PCB) has been designed, the assembly guidelines for the 0.5mm package-on-package (PoP) applications processor and companion memory device must be considered. PoP applications processors have an enormous number of variables associated with assembly. The following factors have a major effect on the quality and reliability of PCB assembly: PoP applications processor solder paste requirements, solder paste deposition and reflow profile, and the fluxing or solder paste deposition onto the memory prior to assembly.

There are two common techniques used for PoP assembly – one-pass and two-pass. Although both will be discussed, Texas Instruments (TI) recommends the one-pass process, as it is the most economical and produces approximately the same assembly yield. This paper provides a starting point for establishing a set of assembly guidelines; however, it can not cover all of the possible variations. It is strongly recommended that you perform actual studies in conjunction with your assembly vendors to optimize the PoP assembly process.

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1 Introduction

This paper is the second of two parts. **Part I**, *PCB Design Guidelines for 0.5mm Package-on-Package Applications Processor, Part I* (SPRABB3), covers the main **PCB design guidelines**. The design of the main PCB to which the applications processor is mounted dominates the PoP failure mechanisms.

NOTE: Be sure and read and apply the guidelines in Part I before beginning PoP assembly.

This document, **Part II**, covers the **assembly guidelines** for printed circuit boards that use the PoP applications processor. Included are assembly options as well as suggestions to use when qualifying and working with your assembly vendors, either internal or contract. Figure 1 illustrates the PoP assembly.

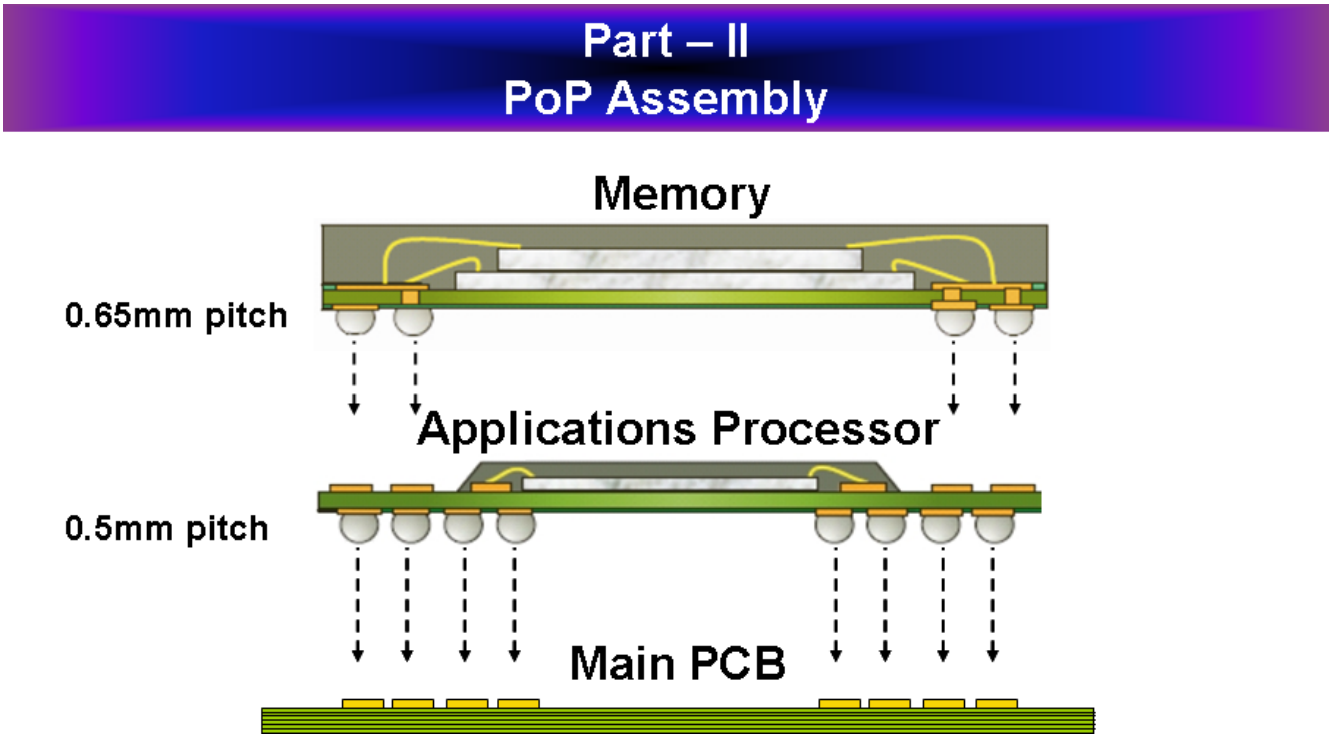

Figure 1. Part II - PoP Assembly

2 Scope of These Guidelines

The focus for this document is the assembly of the applications processor with its companion memory mounted on top – hence the package-on-package name. These guidelines do not cover all aspects of automated assembly, nor is this a study of the reliability of the PoP applications processor.

Assembly of PoP devices and PCBs for fine-pitch BGA packages at 0.5mm and smaller is still new for most assembly vendors. It is more of an art than a science. Thus, the material in this document will age and go out of date quickly.

Since this is a rapidly evolving technology, spend some time reading recently published articles, papers and company presentations on all aspects of fine-pitch board design. Spend time discussing this topic with your assembly vendor. Find out what they know, what experience they have, and review their process documentation of fine pitch packages. Time spent pre-planning and discussing is time well spent.

A common theme emerged as this paper was developed and after an extensive literature search was conducted. Fine pitch BGA assembly, especially PoP assembly, is considered a differentiator among assembly vendors. In many cases, it is a proprietary technology and can not be discussed without the execution of non-disclosure agreements.

If your assembly vendor does not have PoP assembly experience, be prepared to allow time for several learning cycles before committing to volume production. The use of the OMAP EVM board gerbers will be a big help. Use it to help your assembly vendor work through the always-present issues of bringing up a new process. Based on your findings, you may discover assembly vendors you previously used do not have the capability of assembling PoP components and you must locate an assembly vendor with better equipment.

Assembly success comes from experienced companies willing to work together. The most common pairing is an assembly vendor and a PCB board fabricator. Such companies openly share ideas and provide feedback to all parties involved in the board design, fabrication, and assembly.

TI has explored several companies that have worked together and found some common points of agreement on assembly guidelines. The suggestions and recommendations discussed in this document originated with these companies. Always take advantage of any recommended changes from a vendor's design for manufacturability (DFM) studies. Also, don't be afraid to change a board layout to fit the suggestions of the assembly vendor.

As a final word of advice, have lots of patience.

3 Teamwork

Everyone involved in the design, fabrication, and assembly of complex, fine-pitch PCBs must work together as a team to achieve low-cost and reliable products. The days of tossing circuit diagrams over the cubical wall to the board designer who then tosses them to the assembly vendor are gone. Most PCB designs being done today require a team approach and the entire process, from component selection to assembly, requires careful coordination.

The typical team is composed of members from four sub-teams that represent the four major steps in product fabrication: the component suppliers (semiconductors, passives, mechanical, etc.), the PCB designer, the PCB fabricator, and the PCB assembly vendor. In some cases there may be additional members or some members may do more than one job.

Each team member brings his or her own experiences and design guidelines to bear on the task. As a result, it is not uncommon to find conflicting guidelines. These conflicts must be resolved prior to the start of work. Unresolved conflicts will result in poor assembly yields at best, or 100% failure at worst. Constant and frequent communication is the key to resolving conflicts and everyone must be in the loop.

Get to know your team members and be sure to have frequent meetings as the project proceeds from design through production. It will be money and time well spent.

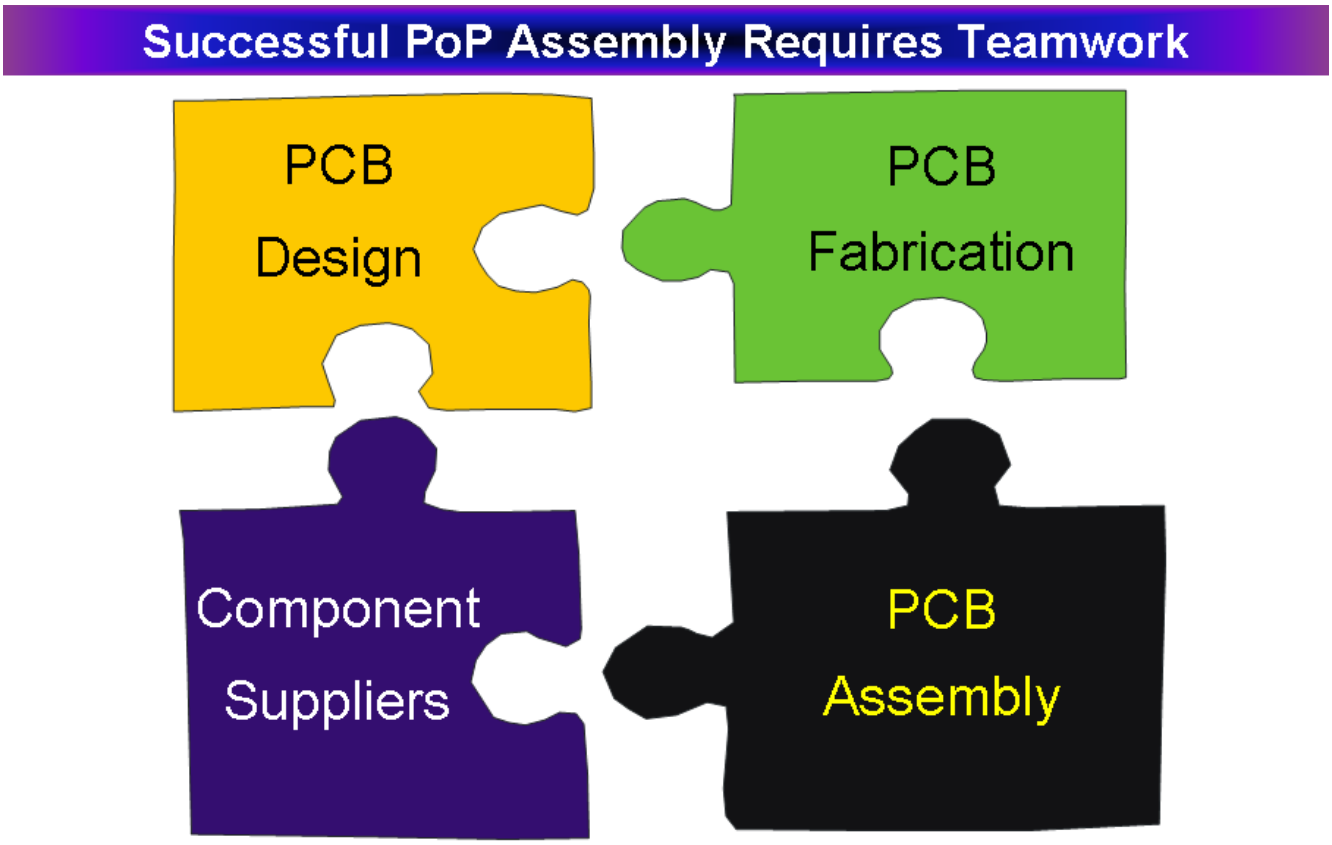

Figure 2. Teamwork Needs for POP Assembly

4 Reference Schematics and PCB Designs

Ask your TI field applications engineer if there are any reference schematics and PCB designs available for the specific applications processor used in your design. Time spent studying the various layers, routing strategies and component placements will help with your PCB design. However, the PCB assemblies designed for TI evaluation modules and verification debug boards may not be representative of your system requirements. These PCB designs are normally being used in a lab environment for development purposes and may not be complete in terms of required design, marketing, and/or manufacturing related protective considerations, including product safety and environmental measures typically found in end products that incorporate such semiconductor components or PCBs. For example, they may not meet your system requirements for electromagnetic compatibility, restricted substances (RoHS), recycling (WEEE), FCC, CE, or UL.

Also, don't forget to review the appropriate datasheets and design guidelines for the memory devices prior to board layout.

5 Assembly Options

There are two options to consider when deciding to build PoP assemblies; a one-pass option and a two-pass option.

In a one-pass assembly the applications processor is first mounted to the main printed circuit board, the memory is mounted to the applications processor, and the finished printed circuit board is then run through the reflow oven in a single pass. TI has used this process with several assembly vendors and none have reported any issues and the yields have been good.

The two-pass assembly has an intermediate step in which the companion memory is first mounted to the applications processor; then these two parts are placed in a carrier tray and reflowed. These joined devices are then mounted on the main PCB and the finished PCB is reflowed a second time. Figure 3 and Figure 4 show these processes.

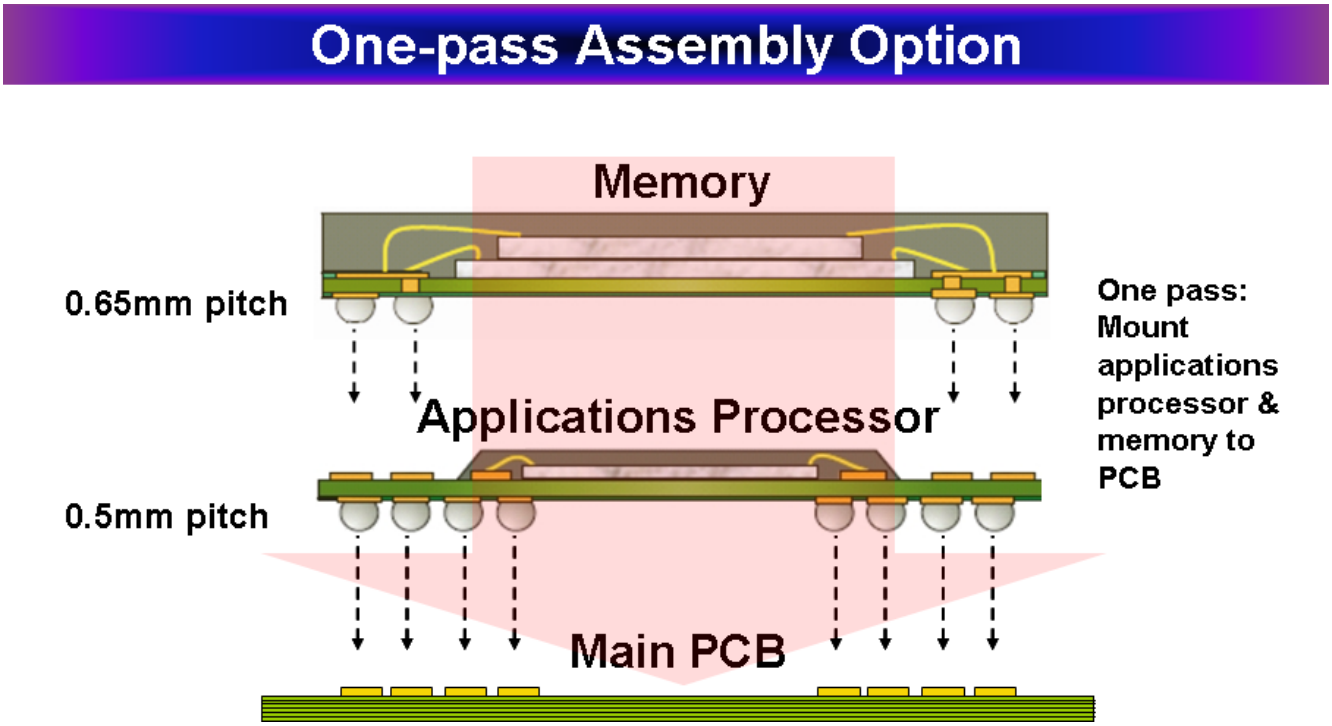

Figure 3. One-Pass Assembly

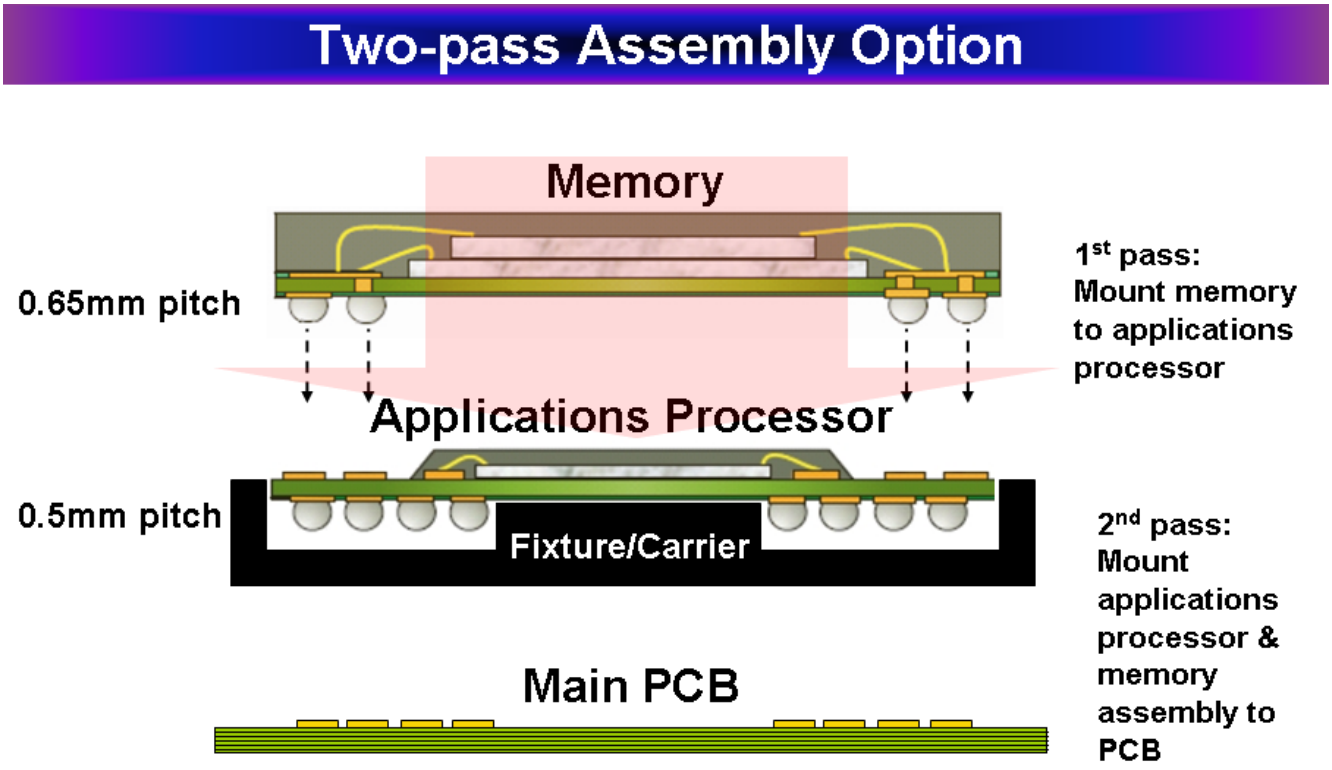

Figure 4. Two-Pass Assembly

6 Solder Paste

The most critical issue related to assembly materials and process parameters is the proper fluxing of the attachment surfaces and the creation of proper metallurgical bonds during the SMT reflow process.

Solder paste characteristics that are important from a process perspective include the solder powder particle size, metallurgy, slump, temperature and humidity sensitivity, solder content, type of flux residue, viscosity, and the propensity for solder balling. No-clean eutectic solder pastes with high metal content are used widely in this type of PCB assembly.

The choice of the particle size used in the solder powder for area array is dependent on the device pitch. As the device pitch decreases, the aperture size will shrink and a smaller particle size solder paste may be required.

When depositing solder paste, a slight amount of overprint of the board pad is desirable to get better paste release by increasing the area ratio. Overprinting also provides a slightly larger volume of paste to minimize coplanarity issues. The use of the appropriate round aperture provides this small amount of overprint. See *PCB Design Guidelines for 0.5mm Package-on-Package Applications Processor, Part I* (SPRABB3) for information on how the overprint amount and solder paste volume is controlled by various solder paste screen parameters.

7 Memory Attachment Options

Memory attachment to the top of the applications processor is often considered one of the critical and most troublesome tasks in PoP assembly. Fortunately, this has not been true. In fact it is the processor-to-main PCB assembly that has proven to be a challenging task.

The primary concern is creating a strong solder joint between the memory ball and the applications processor pad. Standard solder paste screening can not be performed because the encapsulated die is elevated above the surface of the solder pads. The two processes to be described have been developed and used in volume production: paste deposition and flux dipping. For very high volume production, the flux dipping is preferred due to its simplicity and speed. A third option is solder paste dipping which has emerged as an alternative.

Note: There are several papers describing this technique but TI has no experience with it so it will not be discussed.

7.1 Flux Dipping

Flux dipping is being used successfully in high volume assembly facilities where one-pass assembly is utilized. The concept is simple: dip the solder balls of the memory into flux and then mount the device onto the applications processor.

The primary parameter that controls a good joint using this technique is the depth to which the solder ball is dipped, and thus the thickness of the flux.

TI performed a series of experiments using Senju 529D-1 flux applied to different heights of the memory solder ball. The experiment was simple in nature:

1. Apply flux to different levels relative to the ball height.
2. Mount memory to the applications processor.
3. Pull the memory off the applications processor.
4. Inspect each pad to determine if the removal pulled the ball from the pad (bad) or the pad from the application processor (good).

Repeat this test with a different flux level and compare the results of these tests to determine the optimum depth.

See Figure 5 to Figure 8 for a graphical display of these experiments and results.

Figure 5. Experiment Setup

Experiment Setup and Conditions

Test Flux:	Senju 529D-1
OMAP Processor:	TI OMAP2420
Memory:	Samsung memory (daisy chain test device)
Flux Levels:	60um, 150um, and 190um (190um is 1/2 of ball height)

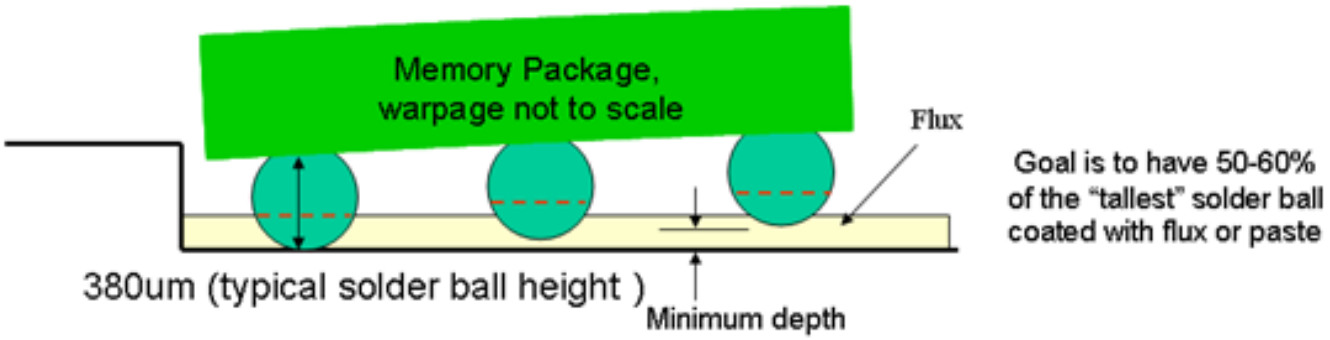

Figure 6. Experiment II

Experiment Results

Dipping depth (um)	Cold joint (# or units)	Cold joint (# of pads)
60um	3/5	10/760 pad
150um	1/5	2/760 pad
190um	0/17	0/2584 pad

This experiment has been done on numerous test boards with the same results. In summary, applying the proper amount of flux, to the proper level as measured relative to the ball height, insures against cold solder joints.

After dipping, mounting and reflowing, the memory was mechanically pulled from the processor. The following images show the cold solder joints, where the ball did not attach to the pad using only a 60um deep application. Not all joints are bad, but only one was needed to declare the test a failure.

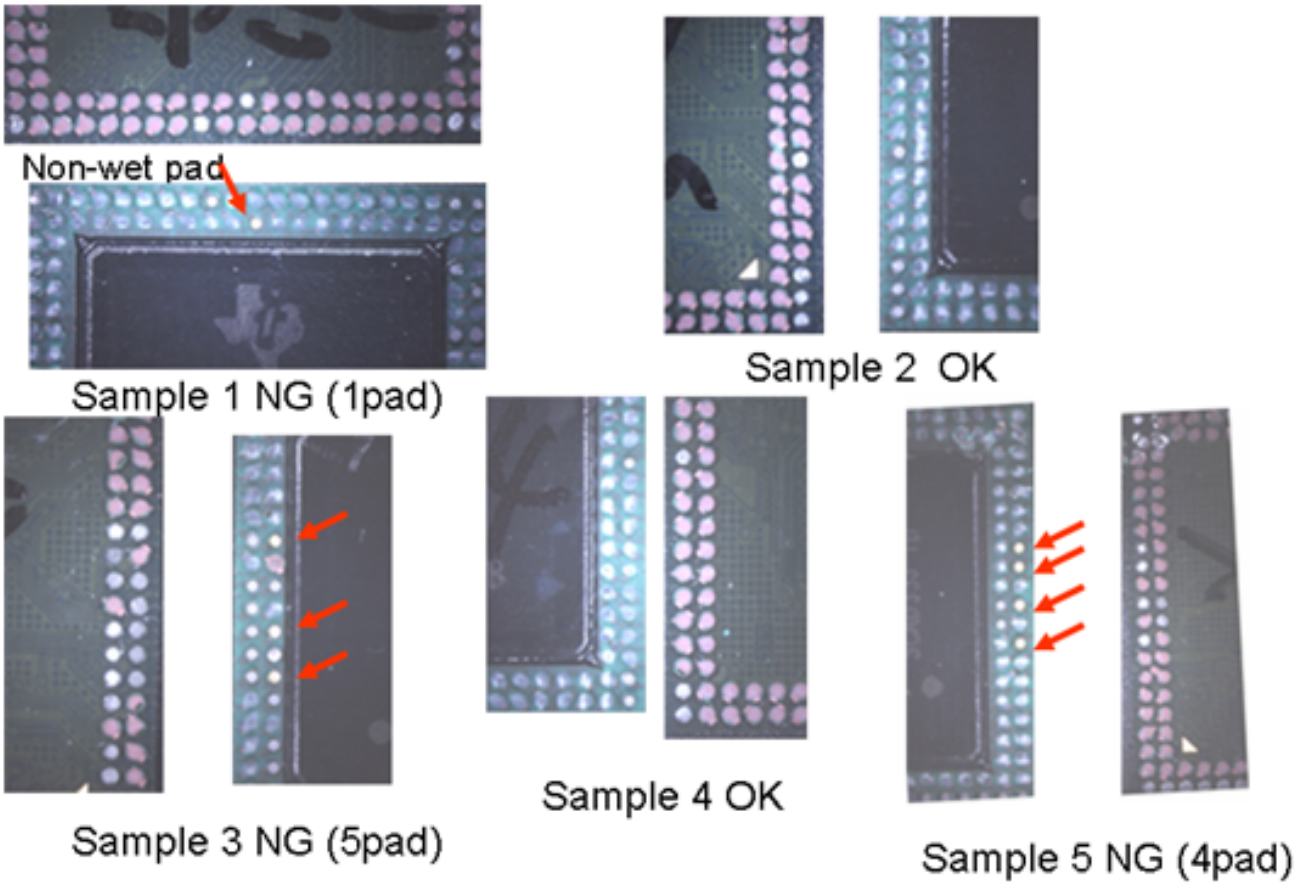

Figure 7. Sample NG

The images below show the five samples with one failure with a flux level at 150um. Upon reaching 190um of flux, or about ½ of the ball height, all samples passed the test.

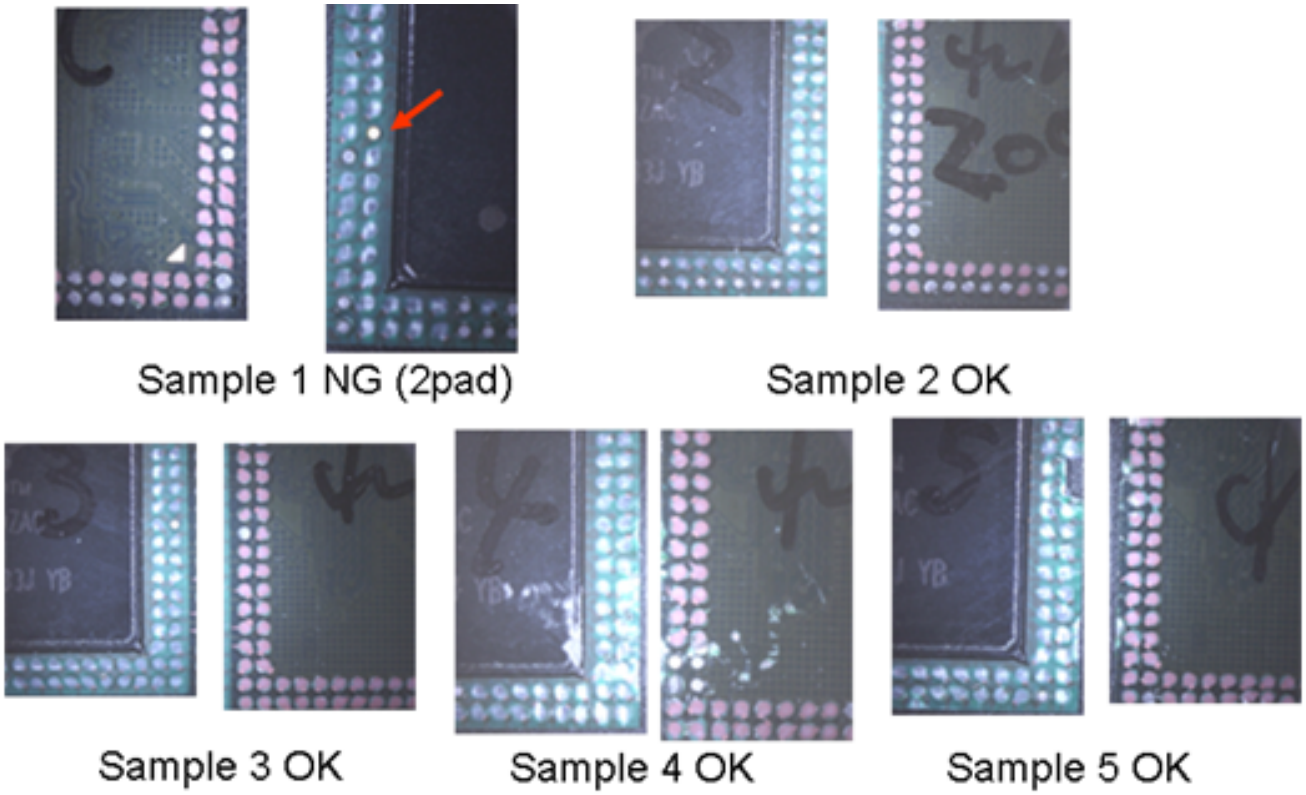

Figure 8. Sample OK

From this experiment, TI recommends that when dip fluxing memory balls, the flux must cover approximately one half of the memory ball height to insure a good solder joint. Also, each ball must be covered with approximately the same amount of flux.

7.1.1 Flux Dipping Equipment

Flux dipping equipment may be necessary and may not be available in your assembly vendor. A Panasonic DT401 multi-functional placement machine with a DT401 Flux Transfer Unit was used during the TI evaluation of the stacking process.

For more information about this equipment, contact Panasonic directly. Panasonic Factory Solutions Company of America, 1-847-495-6100, PFSAmarketing@us.panasonic.com or www.panasonicfa.com.

8 Reflow Atmosphere

Nitrogen gives shorter wetting time, better wetting (appearance) and fewer voids (inclusion of gas) in the solder joint. With SnAgCu paste, the nitrogen atmosphere decreases the wetting to about half the time needed for wetting in air, based on several published papers. TI has repeated these tests and confirms that a nitrogen atmosphere provides the widest process window. This means that the time for temperatures over melting point can be shortened by the use of nitrogen. Figure 9 shows the differences between reflow in nitrogen (left image) and air (right image) with SnAgCu solder. The number of voids is much less and the size of the voids is smaller when nitrogen has been used in reflow soldering.

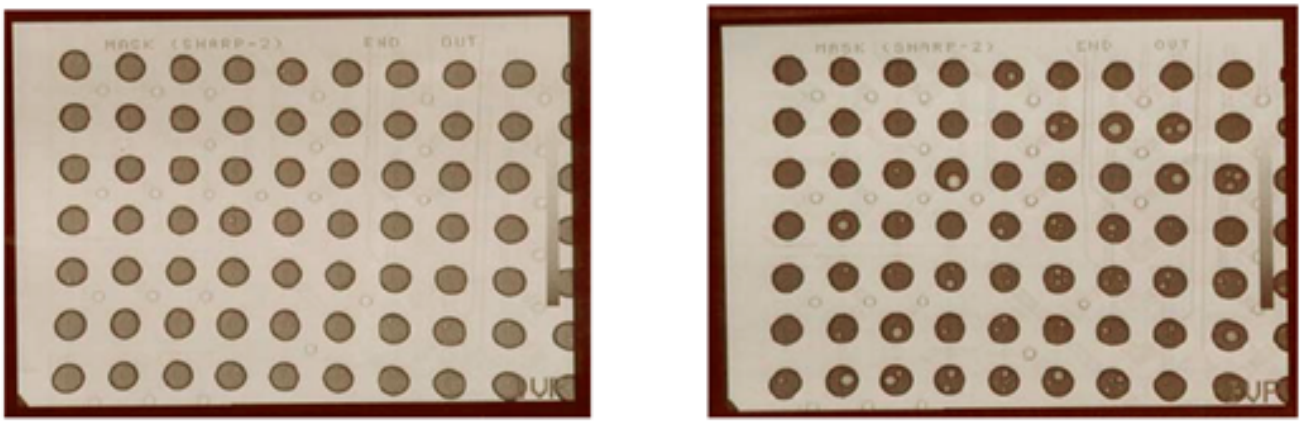

Figure 9. Reflow in Nitrogran and Air

8.1 Reflow

The most popular method of reflowing solder is based on forced convection and/or IR radiation. Some other methods of solder reflow are vapor phase, laser, and hot bar. Mesh belt and edge conveyors are commonly used in reflow ovens. Critical parameters that need to be controlled in the reflow profile are the peak reflow temperature, oxygen level, dwell time above liquidous, soak time, ramp rate, cooling rate, conveyor speed, and the temperature difference across the assembly (ΔT).

The ramp rate in the preheat zone needs to be in a reasonable range. If the rate is too low, the assembly might not be able to reach the required soak temperature fast enough. On the other hand, if the rate is too high, components might be thermally shocked, which causes failure.

Proper soak temperature and soak times are required to evaporate solvents and to activate flux in the paste. The soak time has a significant influence on the temperature difference among components. The longer the small components are kept at a fixed temperature level, the better the chance that the large components can reach the same temperature level.

The solder paste must be elevated to a temperature that is generally 20 to 50 degrees greater than its melting point. Unfortunately, high reflow temperature can also promote intermetallic growth and brittle solder joints.

Typically, the dwell time above liquidous is about 50-70 seconds. Long dwell time may result in dewetting and reoxidation of solder joints while short dwell time can lead to non-wetting.

For the OMAP 2430 EVM, CircuitCo in Richardson, Texas used the following temperature profile for assembly of about 50 prototypes (see Figure 10).

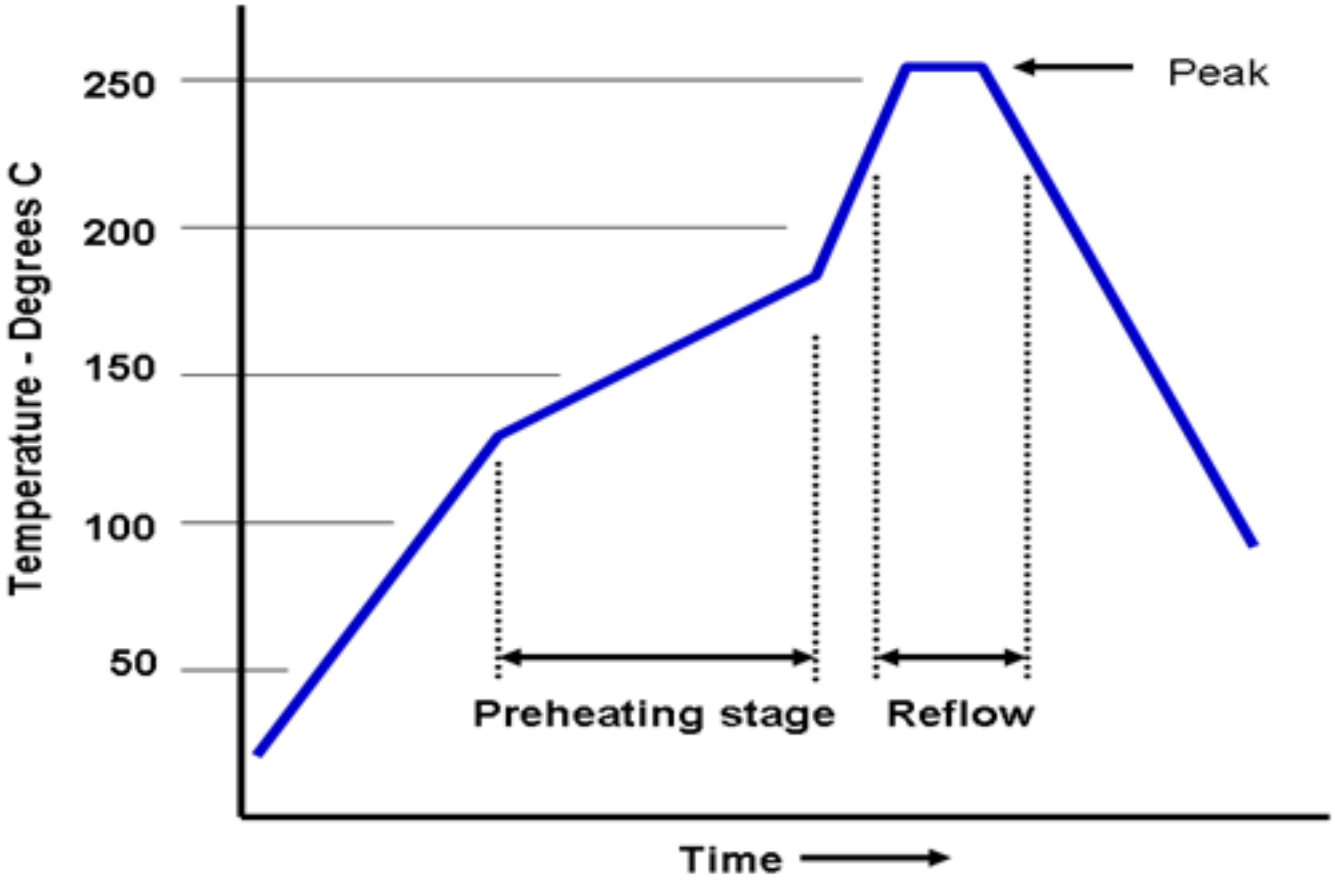

Figure 10. Temperature Profile

Circuitco OMAP 2430 Reflow Profile:	
Pre-heat Temp	120 deg C
Pre-heat Dwell	120 sec
Time above liquid	135 sec
Duration Peak	20 sec
Peak Reflow Temp	255 deg C
Cool down	8 deg C/ sec
For this assembly, the following paste and fluxes were used.	
Solder Paste Chemistry	Sn95.5-Ag3.0-Cu0.5
Paste supplier and part number	Kester EM907
Tacky flux (memory)	Kester TSF 6850 water soluable
No clean flux (processor)	Kester TSF 6592

No problems were found with the 50 prototypes. However, this was a very small sample so your results may vary.

9 Thermal Warpage

A critical aspect of PoP assembly is the type and amount of warpage that can occur during reflow of the processor and the memory. BGA package warpage during reflow soldering can cause open solder joint failure and in the PoP case it's more critical at the top solder joints (memory to applications processor) than at the solder joints between the applications processor and the main PCB. As discussed in Part-I, proper PCB design will stop almost all of the common problems at that interface since it is more a case of providing sufficient solder paste and properly sized pads between the paste and the BGA. However, in most cases, there is only flux applied to the memory device before it is reflowed. Thus, there is no additional paste volume to help with filling the void as the two packages move apart during reflow.

Minimizing warpage is a trade-off between materials, temperature control and time. Your assembly vendor should have recommended profiles for a PoP assembly. Also, memory suppliers have done extensive testing and material selection to minimize warpage. However, it is always present and it may not always be repeatable from batch to batch. Be sure and talk to the memory suppliers and obtain their presentations and papers.

Locate and read the references provided at the end of this paper that specifically discuss thermal warpage issues and test findings. Incorporate these insights into your own assembly process and you will find that your PoP assemblies yield as well as non-PoP fine pitch BGA assemblies.

10 Troubleshooting

There are literally thousands of variables that affect the overall success of fine pitch assembly. This is where close cooperation with your assembly vendor and a willingness to try different experiments pays off.

The best way to explain many of the variables and interactions that can cause yield issues is through the use of an Ishikawa (or fishbone) diagram which shows the causes of a certain event. Cause-and-effect diagrams can reveal key relationship among various variables and possible causes and, perhaps, provide additional insight into a process's behavior.

Typically, causes in the diagram are often based around a certain category. For most assembly issues, the category is yield and the primary causes are equipment, process, people, materials, environment, and management.

Figure 11 is a simple diagram that provides an overview of major causes of stress on BGA packages and solder joints.

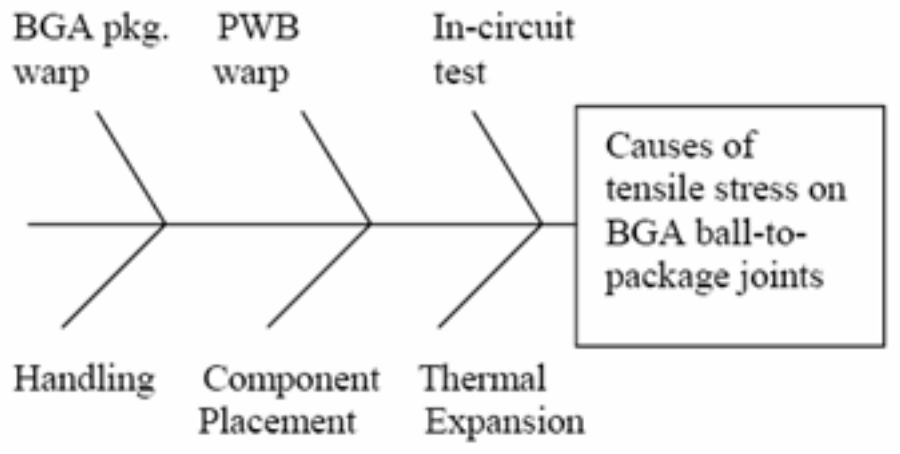

Figure 11. Causes of Stress on BGA Packages and Solder Joints

Figure 12 is typical fishbone diagram that highlights the various causes and effects surrounding assembly yield. Such a diagram, modified to suit your requirements, is invaluable in creating a systematic process for evaluating various problems related to fine pitch assembly.

There is an excellent software package, XMIND, that helps build this type of diagram. It also has brain-storming tools suitable for use in both troubleshooting and trouble prevention. See the reference section for the weblink.

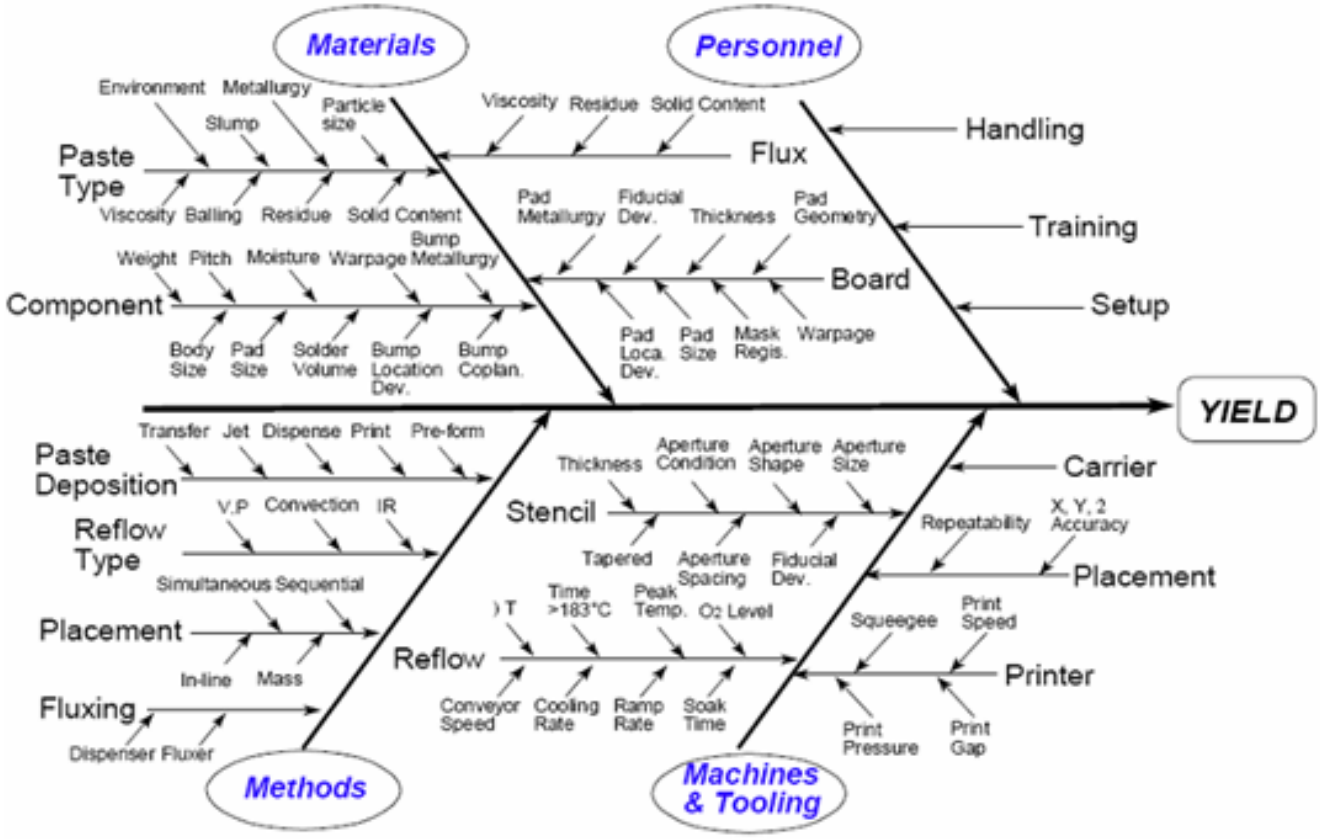

Figure 12. Fishbone Diagram Highlighting Various Causes and Effects Surrounding Assembly Yield

Finally, don't be surprised that major assembly issues are tracked down to a seemingly benign source. In other words, the cause of the problem will be, in many cases, something relatively simple.

11 References

Jeff De Serrano, Inter-Circuit Solutions, Inc.; 400 Black Castle Drive, Lewisville, Texas 75056, Office: 972.410.0067

Ron Weindorf, AMS (Austin Division), 9715 A Burnet Road, Suite 500, Austin, Texas 78758, (512) 491-7411

Clint Cooley, CircuitCo, Richardson, TX 75081.

Ellen Damaso, South Central Region, Micron Technology, Inc. (972) 521-5373.

Jennifer Griffin, ACD, 1250 American Parkway, Richardson, TX 75081 972-664-0900.

Randall Massey, Franklin D Asbell, Chuck Snyder, Network Circuits, Incorporated, 3210 Conflans Rd, Irving, TX , 75061-6338

Hiroyuki Sano, Texas Instruments – Ibaraki, Japan, Tsukuba

Kenji Masumoto, Texas Instruments - Hiji Packaging Development

Articles, Papers, Presentations

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"Printed Circuits Handbook - 6th Edition," Clyde Coombs, Jr., McGraw-Hill, January 2008.

"Package on Package (PoP) Stacking and Board Level Reliability, Results of Joint Industry Study," Dreiza, Smith, Dunn, Vijayaragavan, Werner, www.amkor.com/products/notes_papers/PoP_Stacking_IMAPS_0306.pdf

Product References

Interposers: Interconnect Systems, Inc. 759 Flynn Road, Camarillo, CA 93012, USA, (805) 482-2870. wwwlisipkg.com

Interposers and BGA sockets: Process Science, Inc., 10960 E. Crystal Falls Pkwy, Suite 400, Leander, TX 78641, 512.259.7070, http://www.process-sciences.com

Custom Interposers: Zephyr Engineering, Inc. 1620 West Fountainhead Parkway Suite 303, Tempe AZ 85282, 480-736-8714, www.zpci.com

Adapters for mounting Lead-free BGA for use on boards processed with lower temperature, Tin/Lead solder profiles: Advanced Interconnections Corp., 5 Energy Way, West Warwick, RI 02893 800-424-9850 or 401-823-5200; fax: 401-823-8723 E-mail: info@advanced.com Web: http://www.advanced.com

"XMIND – 2008," PC based software for fishbone diagrams, mindmaps and brainstorming sessions, www.xmind.org/us

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RFID	www.ti-rfid.com	Space, Avionics & Defense	www.ti.com/space-avionics-defense
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