Application Report
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TMS320C6472/TMS320TCI6486 Hardware Design Guide

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ABSTRACT

This application report describes system design considerations for the TMS320C6472/TMS320TCI6486 (C6472/TCI6486) Digital Signal Processor (DSP). The objective of this document is to simplify the design of the C6472/TCI6486 device into a system/board design. In some cases, there is information overlapping with the *TMS320TCI6486 Communications Infrastructure* data manual (SPRS300) or the *TMS320C6472 Fixed-Point Digital Signal Processor* data manual (SPRS612). If the information does not match, the data manual information takes precedence.

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1 C6472/TCI6486 Documentation

The following is a list of available documents relevant to a C6472/TCI6486-based design:

- Data Manual/Errata
  - *TMS320TCI6486 Communications Infrastructure* data manual (SPRS300)
  - *TMS320C6472 Fixed-Point Digital Signal Processor* data manual (SPRS612)
  - *TMS320TCI6486 Digital Signal Processor Silicon Errata* (SPRZ247)
  - *TMS320C6472 Digital Signal Processor Silicon Errata* (SPRZ300)
- User's Guides/Reference Guides
  - *Flip Chip Ball Grid Array Package Reference Guide* (SPRU811)
  - *TMS320C64x/C64x+ DSP CPU and Instruction Set Reference Guide* (SPRU732)
  - *TMS320C64x+ Megamodule Reference Guide* (SPRU871)
  - *TMS320C64x+ DSP Cache User's Guide* (SPRU862)
  - *TMS320C64x Technical Overview* (SPRU395)
  - *TMS320C6000 Programmer's Guide* (SPRU198)
  - *TMS320TCI648x Bootloader User's Guide* (SPRUEA7)
  - *TMS320C645x/C647x Bootloader User's Guide* (SPRUEC6)
  - *TMS320C6472/TMS320TCI648x DSP Software-Programmable Phase-Locked Loop (PLL) Controller User's Guide* (SPRU806)
  - *TMS320C6472/TMS320TCI6486 DSP Host Port Interface (HPI) User's Guide* (SPRUEG1)
  - *TMS320C6472/TMS320TCI6486 DSP Telecom Serial Interface Port (TSIP) User's Guide* (SPRUEG4)
  - *TMS320C6472/TMS320TCI648x DSP General-Purpose Input/Output (GPIO) User's Guide* (SPRU725)
  - *TMS320C6472/TMS320TCI648x DSP 64-Bit Timer User's Guide* (SPRU818)
  - *TMS320C6472/TMS320TCI648x DSP Enhanced DMA (EDMA3) Controller User's Guide* (SPRU727)
  - *TMS320C6472/TMS320TCI648x DSP Inter-Integrated Circuit (I2C) Module User's Guide* (SPRUE11)
  - *TMS320C6472/TMS320TCI6486 DSP Ethernet Media Access Controller (EMAC)/Management Data Input/Output (MDIO) Module User's Guide* (SPRUEF8)
  - *TMS320C6472/TMS320TCI6486 DSP Universal Test and Operations PHY Interface for ATM 2 (UTOPIA2) User's Guide* (SPRUEG2)
  - *TMS320C6472/TMS320TCI648x DSP Serial RapidIO User's Guide* (SPRUE13)
  - *TMS320C6472/TMS320TCI648x DSP DDR2 Memory Controller User's Guide* (SPRU894)
  - *TMS320C6472/TMS320TCI6486 Power/Sleep Controller (PSC) User's Guide* (SPRUEG3)
  - *TMS320C6472/TMS320TCI6486 Shared Memory Controller (SMC) User's Guide* (SPRUEG5)
  - *High-Speed DSP Systems Design Reference Guide* (SPRU889)
  - *Emulation and Trace Headers Technical Reference Manual* (SPRU655)
  - *XDS560 Emulator Technical Reference* (SPRU589)
  - *TMS320C6000 Optimizing Compiler v6.0 Beta User's Guide* (SPRU187)
  - *TMS320C6000 Assembly Language Tools v6.0 Beta User's Guide* (SPRU186)
  - *TMS320C64x+ DSP Big-Endian Library Programmer's Reference* (SPRUEC5)
  - *TMS320C64x+ DSP Little-Endian Library Programmer's Reference* (SPRUEB8)
- Application Reports
  - *TMS320C64x to TMS320C64x+ CPU Migration Guide* (SPRAA84)
  - *EDMA v3.0 (EDMA3) Migration Guide for TMS320TCI648x DSP* (SPRAAC1)
  - *TMS320C6472/TMS320TCI6486 Serial RapidIO Implementation Guidelines* (SPRAAT9)
  - *TMS320C6472/TMS320TCI6486 DDR2 Implementation Guidelines* (SPRAAT7)
  - *TMS320C6472/TMS320TCI6486 EMAC Implementation Guide* (SPRAAU2)
  - *TMS320C6472/TMS320TCI6486 Power Consumption Summary* (SPRAAS4)
  - *TMS320C6472/TMS320TCI6486 Throughput* (SPRAAY0)
  - *Using IBIS Models for Timing Analysis* (SPRA839)

- *TCI6486 ZTZ IBIS Model* (SPRM359)
- *C6472 ZTZ IBIS Model* (SPRM383)
- *TCI6486 ZTZ BSDL Model* (SPRM316)
- *C6472 ZTZ BSDL Model* (SPRM384)
- *TNETV3020/TCI6486 Power Reference Design* (SLVR307)
- *Using Advanced Event Triggering to Find and Fix Intermittent Real-Time Bugs* (SPRA753)
- *Using Advanced Event Triggering to Debug Real-time Problems in High Speed Embedded Microprocessor Systems* (SPRA387)

2 Device Configuration and Initialization

On the C6472/TCI6486 device, boot mode and certain device configuration options are determined at device reset release. The basic information on configuration options, boot-mode options, and use of the power configuration registers is found in the *TMS320TCI6486 Communications Infrastructure* data manual (SPRS300) or the *TMS320C6472 Fixed-Point Digital Signal Processor* data manual (SPRS612).

2.1 Device Reset

There are several ways to reset the C6472/TCI6486 device and these are described in the *TMS320TCI6486 Communications Infrastructure* data manual (SPRS300) or the *TMS320C6472 Fixed-Point Digital Signal Processor* data manual (SPRS612). The two external resets, $\overline{\text{POR}}$ and $\overline{\text{RESET}}$, need to be driven to a valid logic level at all times. $\overline{\text{POR}}$ must be asserted (low) on a powerup while the clocks and power planes become stable. After all power supplies are on and the clocks are stable, $\overline{\text{POR}}$ can be de-asserted (high). If $\overline{\text{RESET}}$ is software-controlled, it will normally be low after $\overline{\text{POR}}$ high. The wake-from-$\overline{\text{POR}}$ sequence will not complete until $\overline{\text{RESET}}$ is also de-asserted (high). $\overline{\text{RESET}}$ is also used from the operating state to issue a warm reset, which performs the same as a $\overline{\text{POR}}$ except that test and emulation logic are not reset. If warm reset is not needed, $\overline{\text{RESET}}$ can be pulled up to DV_{DD33}.

Both $\overline{\text{POR}}$ and $\overline{\text{RESET}}$ cause the device configuration pins to be re-sampled. Memory contents are not preserved when these external resets occur. The GEM cores are reset along with all other modules. Also, whenever either reset is active, all 3.3-V outputs, other than $\overline{\text{RESETSTAT}}$, are tri-stated. All other outputs return to an inactive state. The internal pull-up (IPU) or internal pull-down (IPD) resistors hold floating inputs and outputs at a stable state during this time unless disabled by the configuration inputs multiplexed with GPIO[5:0] and the MACSEL0[2:0] and MACSEL1[1:0] inputs. ($\overline{\text{RESET}}$ does not reset emulation logic or PLL3. $\overline{\text{RESET}}$ also does not tri-state JTAG output TDO.)

There are also internally generated resets. A system or soft reset is generated by emulation or the watchdog timer (if appropriately configured). This reset is similar to the resets caused by the external pins, except that the configuration is not latched and the PLLs do not re-lock. $\overline{\text{RESETSTAT}}$ still indicates this event. Individual GEM resets and module resets are also supported through memory-mapped registers. Individual GEM resets may also be asserted using the $\overline{\text{LRESET}}$ interface. These are not indicated on $\overline{\text{RESETSTAT}}$. The module-level resets must be used with care to prevent stalling transactions and hanging the DSP.

We recommend testpad access to the SYSCLKOUT signal. This can be used to verify the DSP is active and running even when other test methods are unsuccessful. It can also be used to determine the settings of PLL1 and the core clock rate. We also recommend testpad access to the $\overline{\text{RESETSTAT}}$ and BOOTACTIVE outputs for similar debug access if they are not accessible otherwise.

2.2 Device Configuration Inputs

The C6472/TCI6486 device configuration options are sampled from configuration pins. The value is latched at startup and stored in either the DEVSTAT or DEVCTL registers. For details on the configuration options, see the *TMS320TCI6486 Communications Infrastructure* data manual (SPRS300) or the *TMS320C6472 Fixed-Point Digital Signal Processor* data manual (SPRS612). These device configuration pins are shown in Table 1.

Table 1. Device Configuration Inputs

Device Configuration Input	Register	Function	IPU/IPD	Alt. Function
LENDIAN	DEVSTAT	Device endian mode	IPU	
BOOTMODE[3:0]	DEVSTAT	Boot mode	IPU	GPIO[9:6]
DDREN	DEVSTAT	Enable DDR EMIF	IPD	
SYSCLKOUTEN	DEVSTAT	Enable SYSCLKOUT	IPD	GPIO[15]
MACSEL0[2:0]	DEVSTAT	EMAC0 interface select	IPD	
RIOEN	DEVSTAT	Enable RapidIO	IPD	
MACSEL1[1:0]	DEVSTAT	EMAC1 interface select	IPD	
CFGGP[4:0]	DEVSTAT	General-purpose configuration inputs	IPD	GPIO[14:10]
HPI_EN	DEVCTL	IPU/IPD enable on HPI	IPD	GPIO[0]
UTOPIA_EN	DEVCTL	IPU/IPD enable on UTOPIA	IPD	GPIO[1]
TSIP0_EN	DEVCTL	IPD enable on TSIP0	IPD	GPIO[2]
TSIP1_EN	DEVCTL	IPD enable on TSIP1	IPD	GPIO[3]
TSIP2_EN	DEVCTL	IPD enable on TSIP2	IPD	GPIO[4]
EMAC1_EN	DEVCTL	IPU/IPD enable on EMAC1	IPD	GPIO[5]

The C6472/TCI6486 device contains internal pull-up (IPU) or internal pull-down (IPD) resistors on all 3.3-V input and output pins. Since some system designs require these to be disabled when the corresponding interface is bussed, including the time when the C6472/TCI6486 is held in reset, there are external configuration inputs provided for this control. These are the six configuration inputs multiplexed with GPIO[5:0]. These six configuration inputs also enable or disable the output buffers for their respective interfaces. Therefore, whenever the internal resistors are enabled, the associated output buffers are disabled.

Many of the configuration pins are multiplexed with GPIO pins. These pins are re-sampled during subsequent reset events. Designs must return these configuration pins to the required configuration state whenever a reset occurs to assure proper operation after reset release. The output $\overline{\text{RESETSTAT}}$ is used to indicate a reset is in progress and it can be used with external logic to force the desired values to be present before the pins are re-sampled.

If the internal pull-up or pull-down resistors are expected to set these levels, the reset condition must exist long enough for these pins to reach the desired state. Internal pull-up or pull-down resistors have a resistance range of 10 kΩ to 100 kΩ. This internal resistance along with the capacitance of any attached trace and attached components must be considered. Additionally, designs that have multiple DSPs with their configuration inputs connected together need to be configured such that the combined effect of these internal resistors are accommodated when selecting the external configuration resistor value.

If the configuration pins are routed out from the device, the internal pull-up or pull-down resistor should not be relied upon. The track attached to this input degrades the noise immunity of this input. Adding an external resistor restores the expected robustness. In most applications, an external 1-kΩ pull-up or pull-down resistor is a good solution when opposing the internal resistor. If no internal resistor is present, if the internal resistor is disabled, or if the external resistor goes to the same supply as the internal resistor, then an external 10-kΩ pull-up or pull-down resistor is a good solution.

2.3 Boot Modes

The interfaces that support a bootloading process are: I2C, HPI, UTOPIA, Serial RapidIO®, and Ethernet. For a summary of the boot modes supported, see the *TMS320TCI6486 Communications Infrastructure* data manual (SPRS300) or the *TMS320C6472 Fixed-Point Digital Signal Processor* data manual

(SPRS612). For details regarding boot modes, see the *TMS320TCI648x Bootloader User's Guide* (SPRUEA7) or the *TMS320C645x/C647x Bootloader User's Guide*(SPRUEC6). The I2C interface is also used to augment the internally defined boot modes. This interface supplies either customer-defined boot code or configuration tables to support standard boot modes. More information regarding I2C interface use to augment booting is found in the *TMS320TCI648x Bootloader User's Guide* (SPRUEA7) or the *TMS320C645x/C647x Bootloader User's Guide*(SPRUEC6).

There are three primary boot types: immediate, host, and ROM. Boot modes for I2C, UTOPIA, SRIO, and Ethernet use code in the ROM to facilitate the boot process. Host boot allows an external host (via HPI) to load code and configure peripherals while the C64x+ megamodules are held in reset. Once the host has fully configured the device, it releases the C64x+ megamodules to begin execution. Immediate boot allows the C64x+ megamodules to begin execution at the base of L2 memory as soon as reset is released. If a C64x+ megamodule is started in immediate boot and no code is loaded, results are unpredictable. JTAG emulation is always able to connect to a DSP during normal operation or when booting in through ROM or by the host. However, it may not be able to connect to a core that is not running valid code. The C64x+ megamodule needs to be forced back into reset to guarantee the emulator can connect.

The Ethernet boot modes will not operate in gigabit mode unless the core clock is running faster than 375 MHz. Packet errors occur if this requirement is not met. This occurs if using EMAC boot mode over GMII or RGMII and CFGGP[4]=0 when CLKIN1<37.5 MHz or regardless of CFGGP[4] setting with the CLKIN1 rate less than 18.75 MHz. I2C boot mode can be used to solve this problem.

Host boot mode allows memory to be programmed through the HPI while the C64x+ megamodules are halted. The HPI peripheral operates on clocks derived from PLL1 (core clock PLL). After reset release, this PLL is disabled and in bypass. Since the HPI peripheral clocks are derived from PLL1, initial accesses are very slow. It is recommended that the PLL be configured first through HPI accesses. Then, accesses to download the boot image and initialize the remainder of the device will complete much faster. For more information regarding this configuration, see the *TMS320TCI6486 Communications Infrastructure* data manual (SPRS300) or the *TMS320C6472 Fixed-Point Digital Signal Processor* data manual (SPRS612) and the *TMS320C6472/TMS320TCI648x DSP Software-Programmable Phase-Locked Loop (PLL) Controller User's Guide* (SPRU806). **Note:** To guarantee valid cycle completion, all host interfaces connected to the HPI must correctly observe the $\overline{\text{HRDY}}$ output.

2.4 Boot/Initialization Sequence

Generic bring-up procedure:

- Follow power-up and reset sequencing per the *TMS320TCI6486 Communications Infrastructure* data manual (SPRS300) or the *TMS320C6472 Fixed-Point Digital Signal Processor* data manual (SPRS612).
- When the $\overline{\text{POR}}$ (or $\overline{\text{RESET}}$ on a warm boot) signal is de-asserted, the boot-mode options are latched and the boot-mode selection controls what happens next:
  - Booting over I2C puts the device in a state where it loads code and/or configuration parameter contents into memory, then either the new code is executed after the last code section is copied or execution continues in ROM after the configuration parameters are loaded.
  - Booting over Serial RapidIO, UTOPIA, or Ethernet puts the device in a state where it is waiting to receive cells/packets containing code that will be placed into memory which is then executed after the last section is received.
  - Booting over HPI holds the C64x+ megamodules in a reset state until code is written into memory and then the host releases the cores to execute.
- Boot code (at a minimum) should configure the PLL1 core clock frequency and also enable and configure the required peripherals unless they were already configured by the boot process.

3 Clocking

3.1 PLLs

3.1.1 Clock PLL and PLL Controller

A description of the PLLs and PLL Controllers along with register definitions is found in the *TMS320TCI6486 Communications Infrastructure* data manual (SPRS300) or the *TMS320C6472 Fixed-Point Digital Signal Processor* data manual (SPRS612) and the *TMS320C6472/TMS320TCI648x DSP Software-Programmable Phase-Locked Loop (PLL) Controller User's Guide* (SPRU806).

3.1.2 PLL Operation

The CPU core clock is derived from the PLL attached to CLKIN1. The core clock PLL multiplier is not set by reset configuration strapping. The PLL multiplier can be written by any master device on the system interconnect that initiates memory writes. This includes the six C64x+ megamodules and the HPI and SRIO peripherals. In general, a host should only program the PLL during the host-boot procedure using HPI and the software architecture for the software executing on the device should designate a single C64x+ megamodule to be responsible for any programming of the PLL during operation. The core clock speed must not be more than the rated speed grade, 500 MHz, 625 MHz, or 700 MHz. The default PLL multipliers that can be programmed using the ROM boot modes are x10 and x20, so the CLKIN1 frequency must be no more than 50 MHz or 25 MHz, respectively. Since this PLL is programmable, many other CLKIN1 frequencies can be used. For details on setting the CLKIN1 PLL multiplier and divider settings, see the *TMS320TCI6486 Communications Infrastructure* data manual (SPRS300) or the *TMS320C6472 Fixed-Point Digital Signal Processor* data manual (SPRS612) and the *TMS320C6472/TMS320TCI648x DSP Software-Programmable Phase-Locked Loop (PLL) Controller User's Guide* (SPRU806).

3.1.3 PLL Configuration

The following process should be followed to change the PLL after it has been operating. The wait times are conservative durations to guarantee proper operation. This process highlights PLL1 since this is the only PLL that has a programmable multiplier. Similar steps must be taken to reset and restart PLL2 or PLL3, if needed.

- Program PLLEN=0 (PLL bypass mode) and PLLRST=1 (reset PLL) in PLLCTL register.
- Program PLLM for the desired multiplier.
- Wait for at least 256 CLKIN1 cycles for the PLL to reset.
- Set PLLRST=0 to de-assert PLL reset.
- Wait for 2000 CLKIN1 cycles for the PLL to lock.
- Set PLLEN=1 to switch from Bypass mode to PLL mode.

3.2 PLL1, PLL2, PLL3, and SRIO Reference Clock Solutions

This section describes the clock requirements and a system solution for the input clocks to the C6472/TCI6486 device that require special consideration. CLKIN1 is the reference clock to PLL1 that is used to generate the CPU core clock. CLKIN2 is the reference clock to PLL2 that is used to generate the clocks for the EMAC subsystems. CLKIN3 is the reference clock to PLL3 that is used to generate the DDR2 clock. These clock inputs must be driven from low-jitter clock sources. The SRIO reference clock (RIOCLK, RIOCLK#) requires a differential, low-jitter clock source and proper termination.

It is also assumed that multiple devices may be used on board designs, so the proposed system solutions include clock fan-out buffers.

3.2.1 Clock Requirement

The clock requirements are given in Table 2.

Table 2. Reference Clock Requirements

Clock Input	Logic	Input Jitter [1]	Trise/Tfall	Duty Cycle	Stability	Frequency [2]	PLL Frequency
CLKIN1	LVCMOS or LVTTL	100 ps pk-pk	Max 1.2 ns[3]	40/60%	50 PPM	15.625[4] - 50 MHz	500/625/700 MHz
CLKIN2	LVCMOS or LVTTL	100 ps pk-pk	Max 1.2 ns[3]	40/60%	50 PPM	25 MHz	500 MHz
CLKIN3	LVCMOS or LVTTL	100 ps pk-pk	Max 1.2 ns[3]	40/60%	50 PPM	20.0 - 26.67 MHz	400 - 533 MHz
RIOCLK, RIOCLK#	Differential LVDS or LVPECL	4 ps RMS 56 ps pk-pk @ $1x10E^{-12}$ BER	50 ps - 700 ps[5]	45/55%	50 PPM	125 MHz or 156.25 MHz	3.125 GHz

(1) Assumes a Gaussian distribution. Peak-peak jitter assumes 100,000 points.
(2) Recommended operating frequencies based on component availability and supported PLL multipliers.
(3) Trise/Tfall values are given for CLKIN1, CLKIN2, and CLKIN3 transitions from 0.8 V, V_{IL}(max), to 2.0 V, V_{IH}(min). A Trise/Tfall value of 1.2 ns maximum between 0.8 V and 2.0 V translates to a minimum slew rate of 1 V/ns.
(4) Minimum frequency is 19.531MHz for 625 MHz and 21.875 MHz for 700 MHz CPU operation at a PLL multiplier of 32.
(5) RIOCLK Trise/Tfall values are given for 20% to 80% of the voltage swing. These rise/fall times assume the maximum jitter values. Slower rise/fall times can be used if the jitter is lower.

3.2.2 CLKIN1, CLKIN2, and CLKIN3 Solutions

CLKIN1, CLKIN2, and CLKIN3 have similar requirements for a clock source, so the same clocking solutions (except for frequency) can be used for all.

3.2.2.1 Single Device Solution

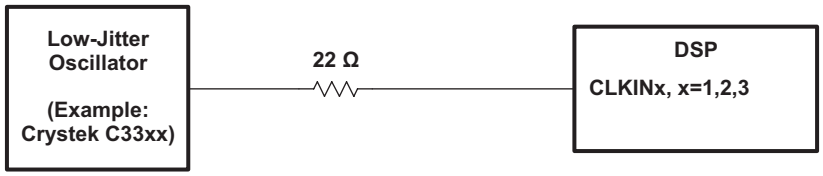
It is assumed that the source clock for each of these clocks is an oscillator on the same board as the TMS320C6472/TMS320TCI6486. Use of distributed clocks may require a jitter cleaner device such as the CDCM7005 (see http://focus.ti.com/docs/prod/folders/print/cdcm7005.html). Most PLL-based clock generators do not meet the input jitter requirement. If an on-board oscillator is used with one C6472/TCI6486, no other components should be needed except for termination resistors.

For CLKIN1, CLKIN2, and CLKIN3, a low-jitter CMOS oscillator is sufficient. A series termination resistor (nominally 22 Ω) at the source is suggested (see Figure 1). Examples of appropriate oscillators are:

- Crystek C33xx Model HCMOS: http://www.crystek.com/spec-sheets/C33xx.pdf
- Fox model F4100 series 3.3 V tight stability HCMOS: http://foxonline.com/pdfs/f4100.pdf

These oscillators have not been tested but are examples of oscillators that meet the specification requirements for CLKIN1, CLKIN2, and CLKIN3.

Figure 1. CLKIN1, CLKIN2, and CLKIN3 Single Device Clock Solution



3.2.2.2 Fan-Out Solutions

For systems with multiple TMS320C6472/TMS320TCI6486 devices it may be preferred to use one oscillator and a fan-out buffer instead of multiple oscillators. This would allow for fewer components as well as lower cost. The fan-out buffer increases the jitter at the clock input so care must be taken in selecting the combination of oscillator and fan-out buffer.

In most cases, the same oscillators described in Section 3.2.2.1 can be used for the fan-out case. The oscillator output specifications should be compared to the fan-out buffer input specifications to make sure they are compatible.

A low-jitter fan-out buffer is required which generally means a non-PLL based fan-out buffer should be used. Suggested solutions for fan-out buffers for CLKIN1, CLKIN2, and CLKIN3:

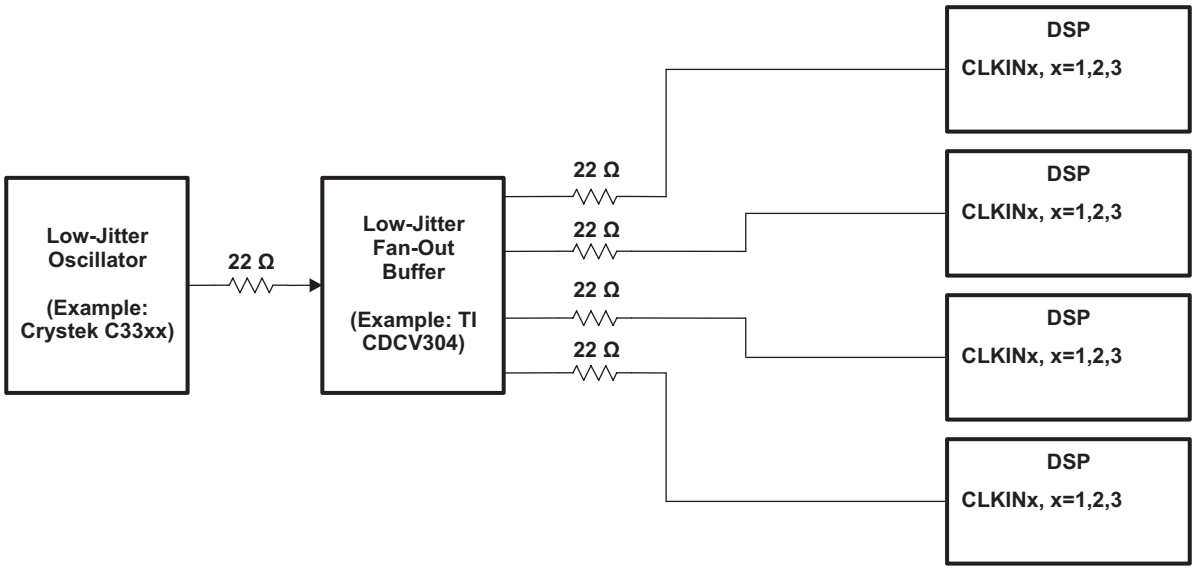
- TI CDCV304 1:4 Clock buffer: http://focus.ti.com/lit/ds/symlink/cdcv304.pdf
- TI CDCVF2310 1:10 Clock buffer: http://focus.ti.com/lit/ds/symlink/cdcvf2310.pdf

For details on the jitter performance of these buffers, see the following documents:

- CDCV304: *Using TI's CDCV304 w/Backplane Transceiver* (SCAA052)
- CDCVF2310: *Using TI's CDCVF2310 and CDCVF25081 with TLK1501 Serial Transceiver* (SCAA064)

These buffers have not been tested. Figure 2 shows a diagram of a solution that allows an oscillator and a fan-out buffer to provide CLKIN1, CLKIN2, or CLKIN3 for up to 4 DSPs. Up to 10 DSPs could be supported with the CDCVF2310 which would be the same circuit without the series resistors since the CDCVF2310 has built-in 22-Ω resistors. The buffer outputs should not be used to drive additional fan-out buffers since the jitter will accumulate.

Figure 2. CLKIN1, CLKIN2, and CLKIN3 Multiple Device Clock Solution



3.2.2.3 Layout Recommendations

Placement and terminations:

- Place the oscillator close to the destination.
- Place the series termination close to the clock source.
- Optimize the value of the series termination resistor to reduce over-shoot and under-shoot while not violating the Trise/Tfall input specification. TI suggests the customer use IBIS simulations to determine the correct value of the termination resistor.

Trace routing:

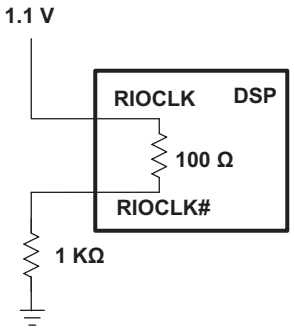
- Place a GND plane below the oscillator and buffer
- Place a solid GND reference plane under the clock traces.
- Do not route the digital signals near or under the clock sources.
- Maintain at least 25 mil spacing to other traces.

3.2.3 RIOCLK/RIOCLK# Solutions

The Serial RapidIO reference clock requires special considerations because it is differential, must be low skew, and requires termination. Either an LVDS or LVPECL clock source can be used, but they require different terminations. The input buffer sets its own common mode voltage so AC coupling is necessary. It also includes a 100-Ω differential termination resistor, eliminating the need for an external 100-Ω termination when using an LVDS driver. For generation information on AC termination schemes, see *AC-Coupling Between Differential LVPECL, LVDS, HSTL, and CML* (SCAA059). For information on DC-coupling, see *DC-Coupling Between Differential LVPECL, LVDS, HSTL, and CML* (SCAA062).

If SRIO is unused, these inputs should be connected to produce a valid logic level. The recommended connections are shown in Figure 3. The 1 KΩ resistor is used to reduce power.

Figure 3. Unused RIOCLK/RIOCLK# Connections



3.2.3.1 Single Device Solution

It is assumed that the source clock is an oscillator on the same board as the TMS320C6472/TMS320TCI6486 device. Use of distributed clocks may require a jitter cleaner device such as the CDCM7005 (see http://focus.ti.com/docs/prod/folders/print/cdcm7005.html). If an on-board oscillator is used with one C6472/TCI6486 no other components should be needed, except for termination resistors.

For the Serial RapidIO reference clock, examples of appropriate oscillators are:

- Pletronics LVDS LV77D oscillator: http://www.pletronics.com/pdf/LV77D%203.3v.pdf
- Pletronics LVPECL PE77D oscillator: http://www.pletronics.com/pdf/PE77D%203.3v.pdf

These oscillators have not been tested but are examples of oscillators that meet the specification requirements for RIOCLK/RIOCLK#.

Figure 4 shows an LVDS-based solution including terminations. Figure 5 shows an LVPECL-based solution including terminations. The terminations shown are still being investigated and should be considered preliminary.

Figure 4. RIOCLK Single Device LVDS Clock Solution

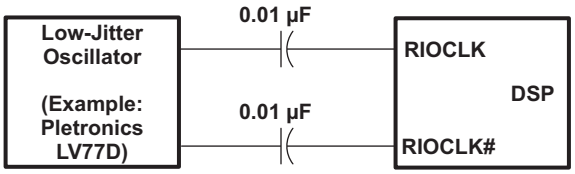
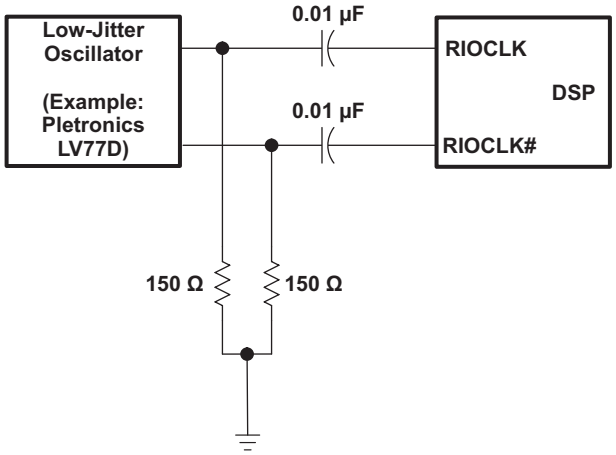


Figure 5. RIOCLK Single Device LVPECL Clock Solution



3.2.3.2 Fan-Out Solutions

For systems with multiple TMS320C6472/TMS320TCI6486 devices, it may be preferred to use one oscillator and a fan-out buffer instead of multiple oscillators. This would allow for fewer components as well as lower cost. The fan-out buffer increases the jitter at the clock input so care must be taken in selecting the combination of oscillator and fan-out buffer.

In most cases, the same oscillators described in Section 3.2.3.1 can be used for the fan-out case. The oscillator output specifications should be compared to the fan-out buffer input specifications to make sure they are compatible.

A low-jitter fan-out buffer is required, which generally means a non-PLL based fan-out buffer should be used. Suggested solutions for a fan-out buffer are:

- TI CDCLVD110A LVDS 2:10 Clock fan-out buffer: http://focus.ti.com/lit/ds/symlink/cdclvd110a.pdf
- TI CDCLVP110 LVPECL 2:10 Clock fan-out buffer: http://focus.ti.com/lit/ds/symlink/cdclvp110.pdf

The SN65LVDS104/108/116 are an alternate set of LVDS buffers from TI in 4-port, 8-port, and 16-port versions (see http://focus.ti.com/lit/ds/symlink/sn65lvds108.pdf).

These buffers have not been tested but are examples of buffers that meet the specification requirements for RIOCLK/RIOCLK#.

For the SN65LVDS108, jitter performance is found in its data sheet. For the CDCLVP110, jitter characteristics are found in its data sheet and discussed in the *Advantage of Using TI's Lowest Jitter Differential Clock Buffer* application report (SCAA068).

Figure 6 shows a diagram of a solution that allows an LVDS oscillator and an LVDS fan-out buffer to provide RIOCLK/RIOCLK# for up to 10 DSPs. Figure 7 shows an LVPECL solution for up to 10 DSPs. The fan-out buffer outputs should not be used to drive additional fan-out buffers since the jitter will accumulate.

Figure 6. RIOCLK Multiple Devices LVDS Clock Solution

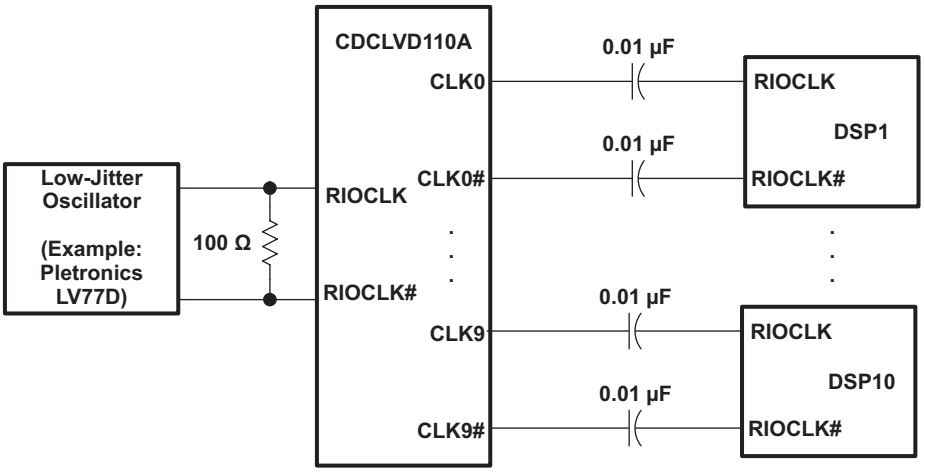
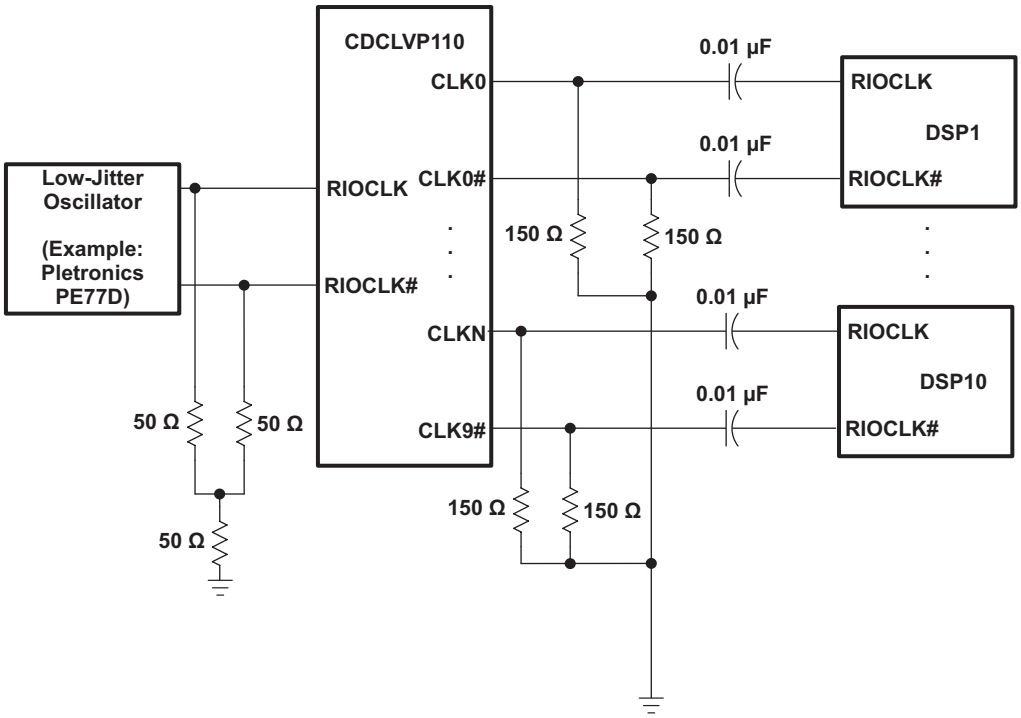


Figure 7. RIOCLK Multiple Devices LVPECL Clock Solution



3.2.3.3 Layout Recommendations (LVDS and LVPECL)

Placement:

- Place the oscillator, buffer, and DSPs as close to each other as practical.
- Place the fan-out buffers in a central area to equalize the trace lengths to each DSP.
- Place the AC coupling capacitors near the receivers.
- Place the 50-Ω resistors used in LVPECL DC termination near the receiver.
- Place the 150-Ω resistors used in LVPECL AC termination near the driver.
- Place the 100-Ω resistors used in LVDS terminations near the receiver.

Trace routing:

- Place a GND plane below the oscillator and buffer.

- Place a solid GND reference plane under the clock traces.
- Do not route the digital signals near or under the clock sources.
- Traces are 100 Ω differential impedance and 50 Ω single-ended impedance.
- Route the clock routes as differential pairs with no more than 2 vias per connection (not counting pin escapes).
- Match the number of vias on each side of a differential pair.
- Differential clock routes must be length matched to within 10 mils.
- Maintain at least 25 mil spacing to other traces.

4 Power Supply

The power supply voltages needed for the C6472/TCI6486 device are shown in Table 3. For definitions of the power supplies, see the *TMS320TCI6486 Communications Infrastructure* data manual (SPRS300) or the *TMS320C6472 Fixed-Point Digital Signal Processor* data manual (SPRS612).

Table 3. Power Supply Requirements

Name	Voltage	Type	Tolerance
CV_{DD}	1.0/1.1/1.2 V	Core Supply	5%
CV_{DD2}	1.0/1.1/1.2 V	Core Supply - SRIO	5%
CV_{DD1}	1.2 V	Core Supply - DDR	5%
DV_{DD33}	3.3 V	I/O Supply	5%
DV_{DD18}	1.8 V	I/O Supply	5%
DV_{DD15}	1.5 V/1.8 V	I/O Supply	5%
$AV_{DDA1}/AV_{DDA2}/AV_{DDA3}$	1.8 V	Analog Supply - PLLs	5%
AV_{DDA4}	1.8 V	Analog Supply - DDR DLL	5%
DV_{DDR}	1.8 V	Analog Supply - SRIO	5%
$DV_{DDD}/AV_{DDA}/AV_{DDT}$	1.2 V	SERDES Supply - SRIO	5%

4.1 Power Plane Generation

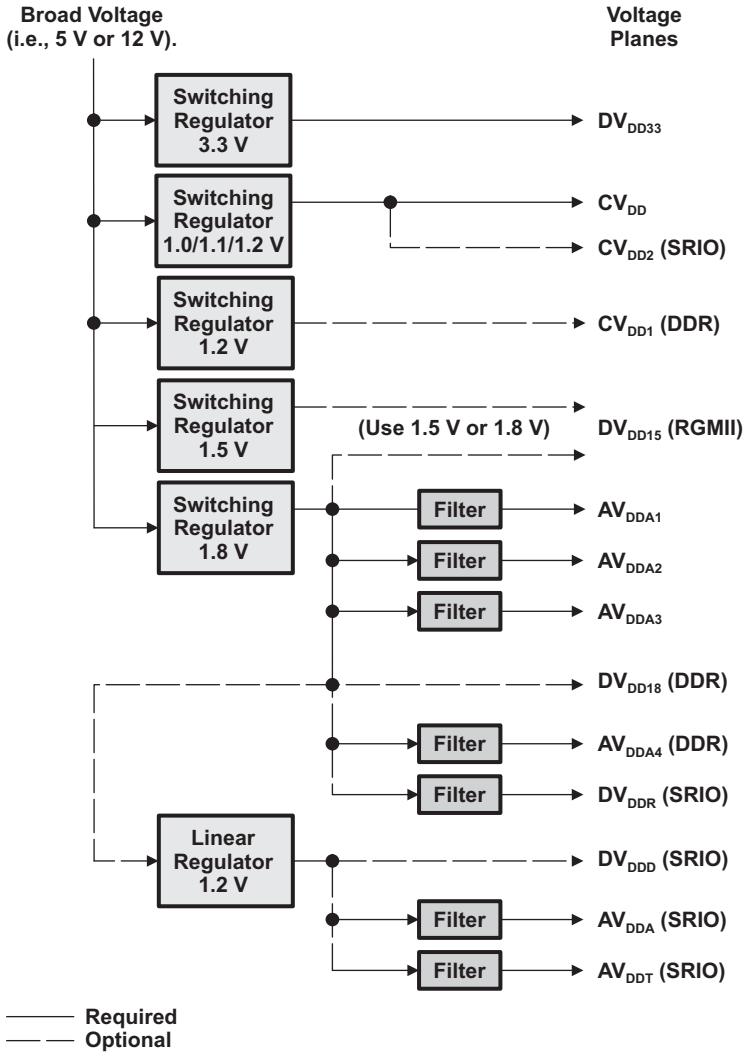
All power supplies are generated from switching supplies, with the exception of the SRIO 1.2-V supplies (DV_{DDD}, AV_{DDA}, and AV_{DDT}). Due to the noise sensitivity of the SRIO SERDES links, a linear regulator with proper filtering is strongly recommended. One solution for a suitable 1.8-V to 1.2-V linear regulator is the UC385-ADJ (http://focus.ti.com/lit/ds/symlink/uc385-adj.pdf) which can support multiple DSPs. A switching regulator plus filtering can be used if the AC noise is guaranteed to be less than ±25 mV. However, the DDR EMIF logic supply CV_{DD1} must not be directly connected to these SRIO 1.2-V power inputs.

Filters are recommended to isolate the different analog power inputs to improve noise rejection. The digital I/O supplies and core logic supplies of like voltage can be combined to simplify layout, assuming sufficient decoupling is provided. An overview of the recommended power supply generation architecture is shown in Figure 8.

The DV_{DD15} supply operates at either 1.5 V or 1.8 V. Operation at 1.8 V consumes somewhat more power than 1.5-V operation, but eliminates the need for a separate 1.5-V supply. Most Ethernet PHYs that support RGMII v2.0 operation support the HSTL interface at either 1.5 V or 1.8 V.

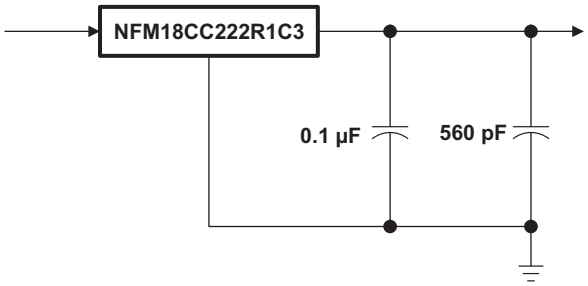
The optional power supplies are noted with dashed lines in Figure 8. These are power inputs that can be connected directly to V_{SS} if the associated peripheral is not used and is disabled.

Figure 8. Power Supply Generation



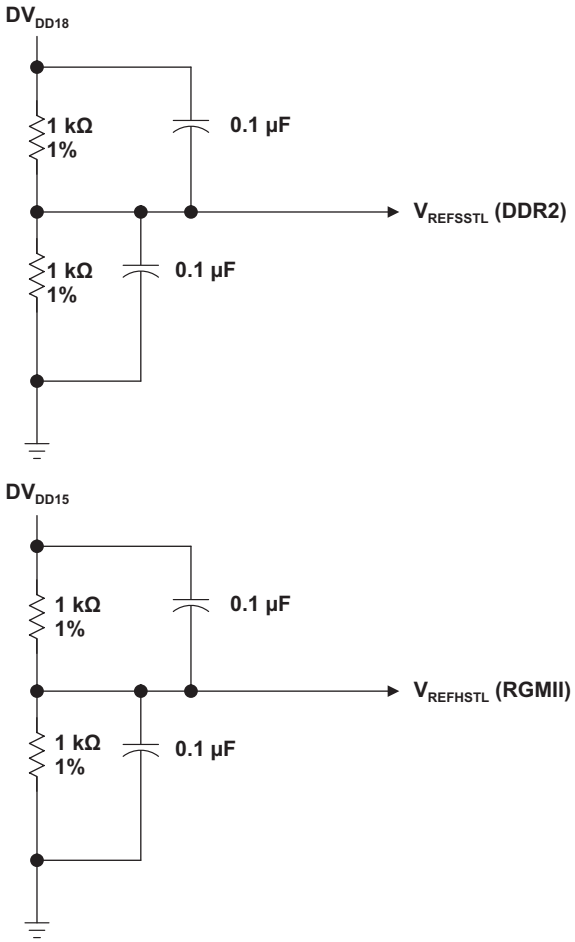
The recommended filter circuit for Figure 8 is given in Figure 9. The filter component shown is a Murata part. If a different part is cross-referenced, the frequency envelope must be considered. This solution has been tested.

Figure 9. Recommended Power Supply Filter



The reference voltages used for the SSTL (DDR2) and HSTL (RGMII) interfaces are intended to operate at half the supply voltage supplied to those interfaces. This is done through a simple voltage divider as shown in Figure 10. More details on $V_{REFSSTL}$ can be found in *TMS320C6472/TMS320TCI6486 DDR2 Implementation Guidelines* (SPRAAT7). Note that if the interface is not used and is disabled, the associated reference voltage can be connected directly to V_{SS}.

Figure 10. Reference Voltage Generation



4.2 Power Supply Sequencing

The recommended power sequence is described in the *TMS320TCI6486 Communications Infrastructure* data manual (SPRS300) or the *TMS320C6472 Fixed-Point Digital Signal Processor* data manual (SPRS612). This is the sequence that is used for manufacturing device test. The C6472/TCI6486 device is designed to have no sequencing requirements. Therefore, other sequences may work but have not been verified at this time. Therefore, it is strongly recommended that this sequence be followed.

Although the recommended power sequence has 3.3-V power ramping before the core voltage, bus contention does not occur on the bidirectional interfaces since special circuitry has been added that holds the 3.3-V I/Os in tri-state during the power supply ramp-up period.

There are multiple ways to generate a controlled power sequence. A microcontroller or PLD can be used to control power supply sequencing. Alternatively, TI has power management products that can be used such as the TPS3808 (http://focus.ti.com/lit/ds/symlink/tps3808g33.pdf). Also, power circuits are available with auto-track capability such as the PTH05050W so that all of the I/O supplies can ramp simultaneously (http://www.ti.com/lit/gpn/pth05050w).

4.3 Voltage Plane Power Requirements

Power requirements are highly dependent on the usage of the device. Most of the power is consumed in the DSP processing cores. This power varies as the application code uses the core modules with different levels of parallelism. The power consumption is also dependent on which peripherals are used as well as their frequencies and percentage of utilization.

A *TMS320C6472/TMS320TCI6486 Power Consumption Summary* application report (SPRAAS4) along with a configurable power estimation spreadsheet has been developed to allow estimation of the maximum power consumption under different circumstances. It displays the maximum power consumption on the power supply rails during the operating conditions described. The maximum power consumption for the two sample applications contained in the spreadsheet is listed in Table 4.

Table 4. Maximum Power

Power Signal	Voltage	AMR 204 Max Power (mW)	PCM 504 Max Power (mW)
DV_{DD33}	3.3 V	159	160
DV_{DD15}	1.5 V	0	0
DV_{DD18}	1.8 V	0	96
AV_{DDA1}, AV_{DDA2}, AV_{DDA3}, AV_{DDA4}	1.8 V	77	167
CV_{DD}, CV_{DD2}	1.0 V	3390	3426
CV_{DD1}	1.2 V	0	305
AV_{DDA}, AV_{DDT}, DV_{DDD}	1.2 V	0	0
DV_{DDR}	1.8 V	0	0
Total		3626	4153

Neither of these scenarios uses RGMII or SRIO and their power supply inputs are assumed to be connected to V_{SS} or left NC. Also, the AMR 204 application does not use DDR2 so its power supply inputs are also assumed to be connected to V_{SS} or left NC.

The power estimation spreadsheet can be used to provide customized numbers for specific applications. The values observed on a board design running this application load are always at or below the numbers provided by the spreadsheet.

4.4 Power Supply Layout Recommendations

To minimize inductance and resistance in the power delivery path, locate core and I/O supply voltage regulators close to the DSP (or DSP array) . Additionally, when designing for high-performance applications utilizing C6472/TCI6486 DSPs, the PCB will include separate power planes for core, I/O, and ground, all bypassed with high-quality, low-ESL/ESR capacitors.

For $V_{REFHSTL}$ and $V_{REFSSTL}$, use one reference voltage divider for both the C6472/TCI6486 and the reference voltage input on the attached device. Use the same supply for the I/O voltages between the 2 parts. Place the V_{REF} resistor divider between the 2 devices and make the routes as directly as possible with a minimum 20 mil wide trace. Ensure a 2x trace width clearance between the routing of the reference voltage and any switching signals.

The filter circuits are placed as close to the corresponding C6472/TCI6486 power supply pin(s) as possible. Do not route digital switching signals near or directly under the filter circuits.

4.5 Voltage Tolerances, Noise, and Transients

The voltage tolerances specified in the *TMS320TCI6486 Communications Infrastructure* data manual (SPRS300) or the *TMS320C6472 Fixed-Point Digital Signal Processor* data manual (SPRS612) include all DC tolerances and the transient response of the power supply. These specify the absolute maximum and minimum levels that must be maintained at the C6472/TCI6486 pins under all conditions. Special attention to the power supply solution is needed to achieve this level of performance, especially the 5% tolerance on the core power plane (CV_{DD}).

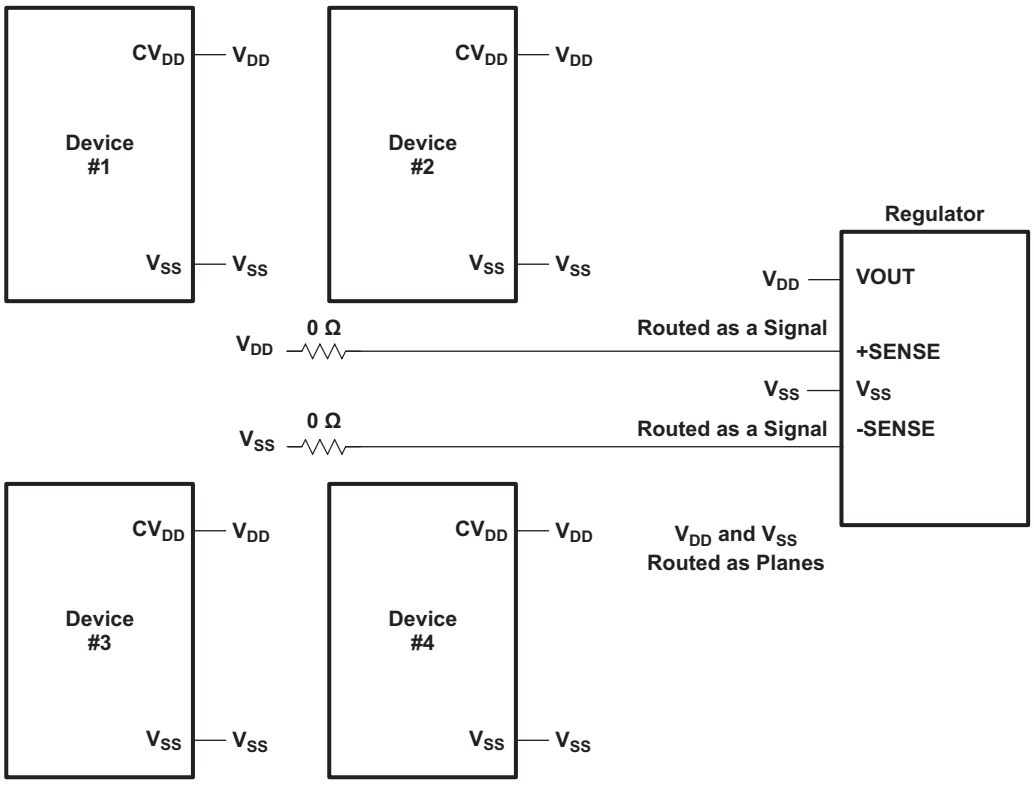
In order to maintain the 5% tolerance at the pins, the tolerance must be a combination of the power supply DC output accuracy, the voltage drop from the supply to the load and the effect of transients. A reasonable goal for the DC power supply output accuracy is 3%, leaving 2% for the transients. At 1.0 V, a 5% tolerance is ±50 mV. This allows ±30 mV of DC accuracy from the output of the power supply and another ±20 mV due to transients.

Power plane IR drop is another factor to consider, especially if there are multiple DSPs in a group on a board. Power planes, even if no splits are present, have impedance. With large currents running across the power planes the voltage drop must be considered. This same issue also applies to ground planes with heavy currents.

4.5.1 Using Remote Sense Power Supplies

Use of a power supply that supports the remote sense capability allows the power supply to control the voltage at the load. Special layout care must be used to keep this sense trace from being lost during PCB layout. One solution is placement of a small resistor at the load and connecting the sense trace to the voltage plane through it. If a group of DSPs on the board are supplied by a single core power supply, place the sense resistor at the center of this group. If a negative sense pin is supported by the voltage regulator, handle it in a similar way. An example of this type of implementation is shown in Figure 11.

Figure 11. Multiple DSP Remote Sense Connections



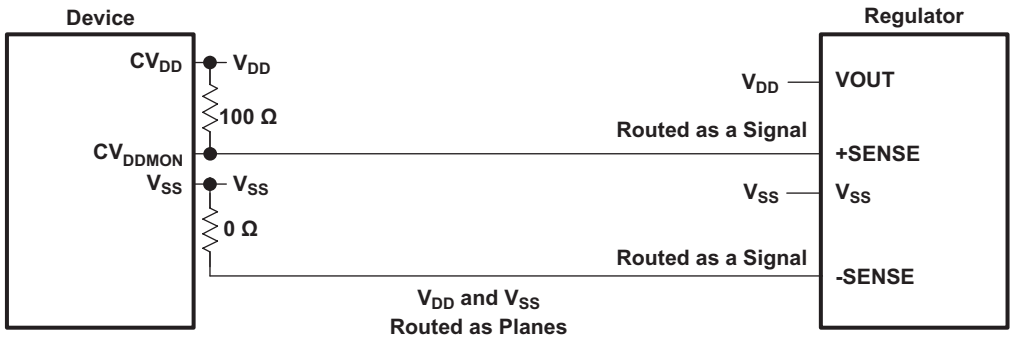
If the connection is between one DSP and one voltage regulator, there are voltage monitor pins available for this application. Voltage monitor pins cannot be used in multiple DSP implementations such as shown in Figure 11. The monitor pins indicate the voltage on the die and, therefore, provide the best remote sense voltage. Early *TMS320TCI6486 Communications Infrastructure* data manual (SPRS300) or *TMS320C6472 Fixed-Point Digital Signal Processor* data manual (SPRS612) editions have these pins grouped with their respective power supplies. The voltage monitor pins are described in Table 5.

Table 5. Die Voltage Monitor Pins

Voltage Plane	Pin Number	Description
CV_{DDMON}	AE9	Die side core voltage monitor
$DV_{DD33MON}$	V5	Die side 3.3 V (DV_{DD33}) voltage monitor
$DV_{DD18MON}$	D12	Die side 1.8 V (DV_{DD18}) voltage monitor
$DV_{DD15MON}$	AG13	Die side 1.5 V or 1.8 V (DV_{DD15}) voltage monitor

These monitor pins are connected directly to the positive-side sense pin of the voltage regulator. Since the voltage regulator output could become unstable and driven to a high voltage if the positive sense line does not receive the correct voltage, it is recommended to place a 100-Ω resistor near the DSP, between the voltage plane and the monitor pin. If the V_{DDMON} connection to the DSP is not present, the positive sense will still regulate to the proper voltage. If a negative sense pin is provided by the regulator, it should be connected to the GND plane near the DSP using a 0-Ω resistor. The single DSP remote sense connections are shown in Figure 12.

Figure 12. Single DSP Remote Sense Connections



4.5.2 Voltage Plane IR Drop

The voltage gradient (IR drop) across the copper planes needs to be considered, whether or not a supply with the remote sense capability is used, when an array of DSPs is implemented. The DSPs closer to the supply have a slightly higher voltage and the DSPs farther from the supply have a slightly lower voltage. This voltage differential is minimized by making the copper planes thicker or by spacing the DSPs across a wider area of the plane. Be sure to consider both the core power plane(s) and the ground plane(s). The resistance of the plane is determined by the following formula:

$$R = \rho * \text{length}/(\text{width} * \text{thickness})$$

where ρ is the resistivity of copper equal to 1.72E-8 Ω-meters. PCB layer thickness is normally stated in ounces. One ounce of copper is about 0.0012 inches or 30.5E-6 meters thick. The width must be de-rated to account for vias and other obstructions. A 50 mm wide strip of 1-oz copper plane de-rated 50% for vias has a resistance of 0.57 mΩ per inch.

4.6 Power-Supply Decoupling and Bulk Capacitors

In order to properly decouple the supply planes from system noise, place as many capacitors (caps) as possible close to the DSP. Assuming 0402 caps, the user should be able to fit the number of capacitors given in Table 7. These caps need to be close to the DSP, no more than 1.25 cm maximum distance to be effective. Ideally, these caps should be connected directly to the via attached to the BGA power pin. Parasitic inductance limits the effectiveness of the decoupling capacitors; therefore the physically smaller 0402 capacitors are recommended. As with selection of any component, verification of capacitor availability over the product's production lifetime should be considered.

Proper capacitance values are also important. Small bypass caps (near 560 pF) should be placed closest to the power pins. Medium bypass caps (100 nF or as large as can be obtained in a small package)

should be the next closest. TI recommends placing decoupling capacitors immediately next to the BGA vias, using the *interior* BGA space and at least the corners of the *exterior*. The inductance of the via connect may eliminate the effectiveness of the capacitor, so proper via connections are important. Trace length from the pad to the via should be no more than 10 mils and the width of the trace should be the same width as the pad.

Larger caps can be placed further away for bulk decoupling. Large bulk caps should be furthest away (but still as close as possible).

4.6.1 Selecting Bulk Capacitance

There are 2 factors that need to be considered when selecting the bulk capacitance: the effective ESR for the power plane capacitors and the amount of capacitance needed to provide power during periods when the voltage regulator cannot respond.

The overall impedance of the core power plane is determined by:

(Allowable Voltage Deviation due to Current Transients)/(Max Current)

In Section 4.5, it was suggested that the allowable voltage deviation allowed due to transient response is 20 mV. The max current, shown in Table 4, is currently estimated at 3.5 A. So, the impedance requirement is 20 mV/3.5 A = 5.7 mΩ. The power plane also has some impedance. An estimate of 2 mΩ requires a total effective decoupling ESR of 3.7 mΩ. So, the effective ESR of the bulk capacitors should not exceed this value. Multiple bulk capacitors in parallel help achieve this overall ESR.

The amount of the bulk capacitance is determined by the amount of time that the power regulator cannot respond to the power demand and the amount of power that needs to be delivered during this time. The worst-case transient would be for all six cores to simultaneously transition from idle to the maximum activity power. The idle power is shown in the power estimation spreadsheet next to the heading ***Baseline***; for this voltage and maximum case temperature, it is 1.85 A. Therefore, the worst-case current step will be 3.5 A - 1.85 A = 1.65 A.

The decoupling capacitors provide the immediate current through the transition but the bulk capacitors need to supply this current until the voltage regulator can respond. A typical power regulator has about a 10-kHz bandwidth with a large capacitive load (needed to maintain the 20 mV deviation). Assuming this bandwidth and a 1.65 A current transient, the minimum bulk capacitance needed is estimated at 1650 µF. So, for this case the bulk capacitance needs to add up to at least 1650 µF and have an effective ESR of less than 3.7 mΩ. The capacitance may need to be further increased to cover temperature derating. Examples of suitable capacitors are shown in Table 6.

Table 6. Bulk Capacitor Examples

Manufacturer	Type	Part Number	C	Vmax	ESR	Quantity
AVX	Tantalum	TPME477*006#0018	470 µF	6.3 V	18 mΩ	5
KEMET	Tantalum	T530X687M004ASE005	680 µF	4 V	5 mΩ	3
SANYO	POS-CAP	2R5TPD1000M5	1000 µF	2.5 V	5 mΩ	2

Capacitor selection should be done as shown above for the specific power supply implementation. If multiple C6472/TCI6486 devices are used on a single core power plane the total capacitance could be reduced per device if the expectation was that the transients would not occur on all devices simultaneously.

4.6.2 Recommended Capacitance

Recommended capacitor selection is given in Table 7. The C6472/TCI6486 capacitor selection does not necessarily include power supply output capacitance. Output capacitors are provided along with the power supply reference designs.

Table 7. Capacitor Recommendations

Voltage Supply	Capacitors	Total Capacitance	Voltage
CV_{DD}	14 * 560 pF 26 * 100 nF 3 * 680 µF	2043 µF	1.0/1.1/1.2-V Core
CV_{DD1} (if used)	3 * 560 pF 3 * 100 nF 1 * 10 µF	10.3 µF	1.2-V DDR Logic
CV_{DD2} (if used)	3 * 560 pF 3 * 100 nF 1 * 10 µF	10.3 µF	1.0/1.1/1.2-V SRIO Logic
DV_{DD33}	14 * 560 pF 26 * 100 nF 2 * 100 µF	203 µF	3.3-V I/O
DV_{DD18}	5 * 560 pF 9 * 100 nF 2 * 100 µF	201 µF	1.8-V DDR I/O
DV_{DD15} (if used)	4 * 560 pF 4 * 100 nF 2 * 10 µF	20.4 µF	1.5/1.8-V RGMII I/O
AV_{DDA1}, AV_{DDA2}, AV_{DDA3}, AV_{DDA4}, DV_{DDR} (if used)	Filter per pin (see Figure 9)	NA	1.8 V
DV_{DDD}, AV_{DDA}, AV_{DDT} (if used)	Filter per pin (see Figure 9)	NA	1.2 V

4.7 Discrete and Module Power Supply Solutions

TI can supply recommended power supply designs for discrete or module-based solutions, upon request.

4.8 Power-Saving Options

4.8.1 Clock Gating Unused Peripherals

The C6472/TCI6486 device can keep (or put) inactive/unused peripherals into a low-power state. This capability is discussed in the *TMS320TCI6486 Communications Infrastructure* data manual (SPRS300) or the *TMS320C6472 Fixed-Point Digital Signal Processor* data manual (SPRS612). All peripherals that are not enabled are clock gated in order to conserve power. After power-up, only those peripherals that are needed should be enabled.

Peripherals can also be disabled and put back into a lower power state. However, this should only be done if no accesses to the peripheral will occur.

4.8.2 Power-Down Peripherals

Some peripherals that are disabled via the reset configuration can have their dedicated power planes connected to V_{SS} or left NC. This achieves the lowest possible power dissipation in these modules. These peripherals are:

- SRIO: All SRIO power planes - CV_{DD2}, DV_{DDR}, DV_{DDD}, AV_{DDA}, and AV_{DDT}
- DDR2: ALL DDR2 power planes and associated pins - CV_{DD1}, DV_{DD18}, AV_{DDA3}, AV_{DDA4}, $DV_{DD18MON}$, HHV18EN, PTV18N, PTV18P, and $V_{REFSSTL}$
- RGMII: All RGMII power planes and associated pins - DV_{DD15}, $DV_{DD15MON}$, HHV15EN, PTV15N, PTV15P, and $V_{REFHSTL}$

For details on how to handle disabled peripherals, see the peripheral-specific chapters at the end of this document. More detail regarding powering down unused peripherals can also be found in the *TMS320TCI6486 Communications Infrastructure* data manual (SPRS300) or the *TMS320C6472 Fixed-Point Digital Signal Processor* data manual (SPRS612).

4.8.3 General Power-Saving Techniques

The following are some additional methods for reducing power:

- Lower frequency operation means lower power. The core and peripherals should be operated at the lowest frequency that meets the user's requirements. Active power is proportional to DSP clock frequency.
- Reducing the case temperature lowers the leakage power. Leakage power increases exponentially to junction temperature. Improving the DSP cooling lowers power dissipation.
- SRIO link power does not scale linearly with data rate. So, a single 2.5-Gbps link consumes less power than two 1.25-Gbps links. Also, running a 1.25-Gbps link at 80% utilization consumes less power than running a 3.125-Gbps link at 30%.
- RGMII operation at 1.5 V has lower power consumption than at 1.8 V.

5 I/O Buffers

5.1 PTV Compensated Buffers

The impedance of I/O buffers is affected by process, temperature, and voltage. For some interfaces, these impedance changes make it difficult to meet specifications across the full range of these parameters. For that reason, the C6472/TCI6486 device uses process, temperature, voltage (PTV) compensated I/O buffers for critical interfaces. The PTV compensation works by adjusting internal impedances to nominal values based on external reference resistances. The interfaces that use PTV-compensated I/O buffers and the details on the reference resistances are given in Table 8.

Table 8. PTV-Compensated Interfaces

Interface	Operating Voltage	Reference resistance
DDR2	1.8 V (DV_{DD18})	200-Ω resistor from PTV18P to GND
		200-Ω resistor from PTV18N to DV_{DD18}
RGMII	1.5/1.8 V (DV_{DD15})	200-Ω resistor from PTV15P to GND
		200-Ω resistor from PTV15N to DV_{DD15}

The resistors used should be 1% tolerance or better. If the DDR2 interface is not used, PTV18P and PTV18N can be connected directly to GND or be left NC. If the RGMII interface is not used, PTV15P and PTV15N can be connected directly to GND or be left NC.

5.2 I/O Timings

The I/O timings in the *TMS320TCI6486 Communications Infrastructure* data manual (SPRS300) or the *TMS320C6472 Fixed-Point Digital Signal Processor* data manual (SPRS612) are given for the tester test load. These timings need to be adjusted based on the actual board topology. In general, *TMS320TCI6486 Communications Infrastructure* data manual (SPRS300) or *TMS320C6472 Fixed-Point Digital Signal Processor* data manual (SPRS612) timings for interfaces that existed on previous DSPs have remained the same. However, some differences exist. For details, see the *TMS320TCI6486 Communications Infrastructure* data manual (SPRS300) or the *TMS320C6472 Fixed-Point Digital Signal Processor* data manual (SPRS612). Since the C6472/TCI6486 device is a completely new device, the nominal timings may be different than the previous DSPs and the I/O buffers may perform differently with a particular board topology. For these reasons, it is highly recommended that timing for all high-speed interfaces (with the exception of DDR and SRIO) on a C6472/TCI6486 design be checked using IBIS simulations. For more details on performing IBIS simulations, see the *Using IBIS Models for Timing Analysis* application report (SPRA839).

6 Peripherals

This section covers each of the C6472/TCI6486 device's peripherals/modules. This section is intended to be used in addition to the information provided in the *TMS320TCI6486 Communications Infrastructure* data manual (SPRS300) or the *TMS320C6472 Fixed-Point Digital Signal Processor* data manual (SPRS612), the module user's guides provided for each of the peripherals, and relevant application reports. The 4 types of documents should be used as follows:

- Data Manual: AC timings and register offsets
- Module User's Guides: Functional description and programming guide
- Applications Reports: System-level issues
- This Chapter: Hardware implementation issues and system-level issues not covered in the separate application reports

Each peripheral section includes recommendations on how to handle pins on interfaces that are disabled or for unused pins on interfaces that are enabled. Generally, if internal pull-ups or pull-downs are included, the pins can be left floating. Any pin that is output only can always be floated. If internal pull-ups and pull-downs are not included or disabled, pins can normally still be floated with no functional issues for the device. However, this may allow additional leakage current that can be eliminated if internal or external pull-ups or pull-downs are used. When pull-ups or pull-downs are used the leakage current is approximately 100 µA per pin. When the pins are floating the leakage current can be several milliamps. Although the recommendations normally indicate using external pull-up resistors, pull-down resistors can also be used. The leakage is the same whether pull-ups or pull-downs are used. Connections directly to power or ground can be used only if the pins can be guaranteed to never be configured as outputs.

6.1 Host Port Interface (HPI) Memory Access

Documentation for HPI:

- *TMS320C6472/TMS320TCI6486 DSP Host Port Interface (HPI) User's Guide* (SPRUEG1)
- *TCI6486 ZTZ BSDL Model* (SPRM316)
- *C6472 ZTZ BSDL Model* (SPRM384)
- *Using IBIS Models for Timing Analysis* (SPRA839)

6.1.1 HPI Configuration

The HPI peripheral operates on a clock derived from the DSP CPU core PLL. Therefore, the performance of the HPI interface changes as the output clock from the first PLL changes. This is especially noticeable during host boot mode when PLL1 starts in bypass. Since HPI accesses can be used to program the core clock PLL, it is recommended that this be done at the beginning of the host boot process to minimize the time needed to download the boot image.

It is possible to configure the C6472/TCI6486 to bootload application code over the HPI interface. Boot over HPI is a feature that is selected using boot-mode options. For details on boot-mode options, see the *TMS320TCI6486 Communications Infrastructure* data manual (SPRS300) or the *TMS320C6472 Fixed-Point Digital Signal Processor* data manual (SPRS612) and the *TMS320TCI648x Bootloader User's Guide* (SPRUEA7) or the *TMS320C645x/C647x Bootloader User's Guide*(SPRUEC6).

If HPI is not used, the configuration input GP00/HPI_EN or the corresponding bit in the DEVCTL can be configured to disable the output buffers and enable the internal pull-up and pull-down resistors on these pins.

The HPI interface is flexible and can be connected gluelessly to most microprocessors. As such, it has more input pins than the minimum needed to allow this flexibility. The internal pull-up resistors on the pins $\overline{\text{HAS}}$, $\overline{\text{HINT}}$, and $\overline{\text{HCS}}$ are always active so that any of these pins can be left unconnected if not used in the chosen implementation. If any other input-only or input/output pin is not needed and HPI is in use, it will need an external pull-up resistor.

6.1.2 HPI System Implementation

Series resistors should be used on all of the HPI control signals that are edge sensitive. Depending on the implementation, this may include any or all of the pins $\overline{HAS}$, $\overline{HDS2}$, $\overline{HDS1}$, and $\overline{HCS}$. This prevents glitches on the signal transitions that could initiate invalid HPI cycles, potentially corrupting memory. Most implementations do not need series terminations on the other HPI control and data lines as long as the traces are kept short and routed cleanly.

In a bused architecture where several DSPs are connected to the same host interface, the traces should be routed from DSP to DSP in a single, multi-drop route without branches. Then a single termination can be implemented at the end of the bus to reduce over-shoot and under-shoot to reduce EMI and crosstalk. This need is even more likely when the host bus passes through board-to-board connectors. To determine the optimum value, simulations using the IBIS models should be performed to validate signal integrity and AC timings.

6.2 Telecom Serial Interface Port (TSIP)

Documentation for TSIP:

- *TMS320C6472/TMS320TCI6486 DSP Telecom Serial Interface Port (TSIP) User's Guide* (SPRUEG4)
- *TCI6486 ZTZ BSDL Model* (SPRM316)
- *C6472 ZTZ BSDL Model* (SPRM384)
- *Using IBIS Models for Timing Analysis* (SPRA839)

6.2.1 TSIP Configuration

TSIP0, TSIP1, and TSIP2 are independent serial interface ports. Each one has two clock inputs, two frame sync inputs, eight serial data inputs, and eight serial data outputs. All interface timing is derived from the clock and frame sync inputs. Each TSIP can be individually configured to operate at either 8.192 Mbps, 16.384 Mbps, or 32.768 Mbps. All eight lanes are used at 8.192 Mbps, only the first four lanes are used at 16.384 Mbps, and only the first two lanes are used when at 32.768 Mbps.

If any of the TSIP ports are not used, the corresponding configuration input pins GP02/TSIP0_EN, GP03/TSIP1_EN or GP04/TSIP2_EN can be pulled down to disable the output buffers and enable the internal pull-down resistors on the pins. This can also be accomplished by setting the appropriate bits in the DEVCTL register. The bit positions in the DEVCTL register also allow the internal pull-down resistors for the upper four serial data input and output lanes to be enabled for 16.384 Mbps operation. Similarly, when operating in 32.768 Mbps mode, DEVCTL bits can be configured to enable the internal pull-down resistors for the upper six serial data input and output lanes while the lower two serial data input and output lanes are in use.

The TSIP controls for the internal pull-down resistors do not support all possibilities. If only one clock input on an active TSIP port is driven, the other clock input needs an external pull-down resistor. Similarly, if only one frame sync input on an active TSIP port is driven, the other frame sync input needs an external pull-down resistor. The clock inputs or the frame sync inputs can be tied together but you must consider the effects of the increased loading on timing margins. The serial input and output data lines are configurable for two, four, or eight active. If the number of active lanes is other than two, four, or eight, the unused inputs also need an external pull-down resistor. External pull-up or pull-down resistors are also recommended for the output lanes if these traces are left floating for long periods of time to minimize leakage.

The TSIP configuration can be used to create a driven high or low output and eliminate the need for the external resistors, in some cases.

6.2.2 TSIP System Implementation

Series resistors should be used on TSIP clock inputs that are edge sensitive. This prevents glitches on the clock signal transitions that could potentially disrupt TSIP timing. Most implementations do not need series terminations on the other TSIP control and data lines as long as the traces are kept short and routed cleanly.

The maximum TSIP performance is achievable only when using point-to-point connections. Termination

resistors are only rarely needed in this topology. In a bused architecture where several DSPs are connected to the same TSIP interface, the traces should be routed from DSP to DSP in a single, multi-drop route without branches. Then a single termination can be implemented at the end of the bus to reduce over-shoot and under-shoot to reduce EMI and crosstalk. This need is even more likely whenever a TSIP bus passes through board to board connectors. To determine the optimum value, simulations using the IBIS models should be performed to validate signal integrity and AC timings.

Multiple DSPs can be connected to a common TSIP bus using TDM mode. The additional loads require a reduction in the operating frequency. Also, the specific routing topology becomes much more significant as additional DSPs are included. The way to determine the best topology and maximum operating frequency is by performing IBIS simulations.

6.3 GPIO Pins

Documentation for GPIO/interrupts:

- *TMS320C6472/TMS320TCI648x DSP General-Purpose Input/Output (GPIO) User's Guide* (SPRU725)
- *TMS320TCI648x Bootloader User's Guide* (SPRUEA7)
- *TMS320C645x/C647x Bootloader User's Guide*(SPRUEC6)
- *TCI6486 ZTZ BSDL Model* (SPRM316)
- *C6472 ZTZ BSDL Model* (SPRM384)
- *Using IBIS Models for Timing Analysis* (SPRA839)

6.3.1 GPIO Pin Configuration

All GPIO pins are multiplexed with configuration inputs. They are all available for GPIO use after the pins have been sampled at reset release. Since the configuration inputs are re-sampled by most reset events, the output pin $\overline{\text{RESETSTAT}}$ must be monitored to allow these configuration inputs to return to their configuration level prior to being sampled. Timing for this is discussed in the *TMS320TCI6486 Communications Infrastructure* data manual (SPRS300) or the *TMS320C6472 Fixed-Point Digital Signal Processor* data manual (SPRS612).

All GPIO pins need to be enabled via software before they can be configured. All GPIO pins default to inputs. All GPIO pins can be used as interrupts and/or EDMA events.

The GPIO module operates at CPU core clock divided by 6. The fastest a GPIO can be switched is at half this rate. For example, at a CPU core frequency of 500 MHz the GPIO module clock is 83 MHz and the max GPIO clock switching rate is 41.5 MHz (or a max clock rate of 20.75 MHz).

All GPIO pins have internal pull-down or pull-up resistors, so they can be left unconnected if not used. However, it is assumed all will be connected for configuration purposes. Even if not needed for the system application, it is recommended to have these connected to support debug activities.

6.3.2 GPIO Pin System Implementation

It is recommended that GPIO pins used to drive an edge-sensitive signal like an interrupt have series termination resistors to prevent glitches on the signal transitions (22 or 33 Ω being typical values). It is equally important that GPIO inputs that are edge-sensitive be driven from sources that have series termination resistors. The value (or need) for the series resistor can be determined by simulating with the IBIS models.

If a GPIO pin needs to default to a particular state (low or high), an external resistor should be used. An external resistor value of 1.0 kΩ is recommended to make sure that it overrides the internal pull-up or pull-down resistor present on the GPIO pin. Additional consideration is needed if multiple GPIO pins are bussed together. Each internal pull-up or pull-down resistor may have a value as low as 10 kΩ. The parallel combination of all internal resistors must be considered to guarantee valid input voltage levels when the configuration input values are sampled.

6.4 Timers

Documentation for timers:

- *TMS320C6472/TMS320TCI648x DSP 64-Bit Timer User's Guide* (SPRU818)
- *TMS320C64x/C64x+ DSP CPU and Instruction Set Reference Guide* (SPRU732)
- *TCI6486 ZTZ BSDL Model* (SPRM316)
- *C6472 ZTZ BSDL Model* (SPRM384)
- *Using IBIS Models for Timing Analysis* (SPRA839)

6.4.1 Timer Configuration

There are 12 timers in the C6472/TCI6486 device. Six timers are general-purpose timers and the other six are associated individually with a CPU core. Each timer needs to be enabled via software after a reset before it can be used.

Each of the general-purpose timers can be configured as a single 64-bit timer or as two 32-bit timers. The timers associated with the CPU cores are driven by a CPU/6 clock. The general-purpose timers also receive an input from TIMI0 and TIMI1. Also, any of the general-purpose timers can be configured to drive TIMO2.

If either of the external timer inputs or the timer output is not used, the pins can be left unconnected and the internal pull-downs will hold the pins at a low state.

6.4.2 Timer System Implementation

Since all timer input and output signals are edge-sensitive, it is recommended that they have series termination resistors to prevent glitches on the signal transitions. The value (or need) for the series resistor can be determined by simulating with the IBIS models.

External timer input signals are synchronized to the internal timer clock. Since the timer operates on the CPU core clock divided by 6, the timer logic may not register the signal from the input pin for up to six CPU clock cycles after it arrives.

6.5 Inter-Integrated Circuit (I2C) Interface

Documentation for I2C interface:

- *TMS320C6472/TMS320TCI648x DSP Inter-Integrated Circuit (I2C) Module User's Guide* (SPRUE11)
- *TMS320TCI648x Bootloader User's Guide* (SPRUEA7)
- *TMS320C645x/C647x Bootloader User's Guide*(SPRUEC6)
- *TCI6486 ZTZ BSDL Model* (SPRM316)
- *C6472 ZTZ BSDL Model* (SPRM384)
- *Using IBIS Models for Timing Analysis* (SPRA839)
- Philips I2C Version 2.1 Specification

6.5.1 I2C Configuration

The I2C peripheral needs to be enabled via software before use. The input clock for the I2C module is core clock divided by 6. There is a prescaler in the I2C module that needs to be setup to reduce this frequency to an internal module clock of 7 to 12 MHz.

If the I2C signals are not used, the SDA and SCL pins can be left floating. This causes a slight increase in power due to leakage that can be avoided by having external pull-up resistors.

It is possible to configure the C6472/TCI6486 device to bootload application code over the I2C interface. Boot over I2C is a feature that is selected using boot-mode options. For details on boot-mode options, see the *TMS320TCI6486 Communications Infrastructure* data manual (SPRS300) or the *TMS320C6472 Fixed-Point Digital Signal Processor* data manual (SPRS612) and the *TMS320TCI648x Bootloader User's Guide* (SPRUEA7) or the *TMS320C645x/C647x Bootloader User's Guide*(SPRUEC6).

6.5.2 I2C System Implementation

External pull-up resistors to 3.3 V are needed on the I2C signals (SCL, SDA). The recommended pull-up value is 4.7 kΩ.

Multiple I2C devices can be connected to the interface but the speed may need to be reduced (400 kHz is the maximum) if many devices are connected.

6.6 Ethernet MAC (EMAC)

Documentation for EMAC:

- *TMS320C6472/TMS320TCI6486 DSP Ethernet Media Access Controller (EMAC)/Management Data Input/Output (MDIO) Module User's Guide* (SPRUEF8)
- *TMS320TCI648x Bootloader User's Guide* (SPRUEA7)
- *TMS320C645x/C647x Bootloader User's Guide*(SPRUEC6)
- *TCI6486 ZTZ BSDL Model* (SPRM316)
- *C6472 ZTZ BSDL Model* (SPRM384)
- *Using IBIS Models for Timing Analysis* (SPRA839)

6.6.1 EMAC and MDIO Interface Configuration

The C6472/TCI6486 device contains two independent Ethernet MAC modules, EMAC0 and EMAC1, and a shared MDIO controller. Both EMAC ports and the MDIO interface can be configured to use HSTL levels and be compatible with RGMII v2.0. Alternatively, these modules can be configured for use with separate pins that support 3.3-V LVCMOS I/O through the interface modes GMII, MII, RMII, or S3MII.

Only one mode can be used at a time for each EMAC port. The mode used is selected at device reset based on the MACSEL0[2:0] and MACSEL1[1:0] configuration pins. Also, because some of these pins are shared, not all combinations are valid. To see how these pins are shared, see the *TMS320TCI6486 Communications Infrastructure* data manual (SPRS300) or the *TMS320C6472 Fixed-Point Digital Signal Processor* data manual (SPRS612).

All EMAC port connections are point-to-point only.

There are two sets of MDIO interfaces (LVCMOS and HSTL). The selection follows that for EMAC0. If EMAC0 is configured for RGMII mode, then the MDIO controller will use its HSTL pins. Otherwise, it uses its LVCMOS pins.

It is possible to configure the C6472/TCI6486 device to bootload application code over either Ethernet MAC port interface. Boot over EMAC is a feature that is selected using boot-mode options. For details on boot-mode options, see the and the *TMS320TCI648x Bootloader User's Guide* (SPRUEA7) or the *TMS320C645x/C647x Bootloader User's Guide*(SPRUEC6).

Even if an EMAC port is enabled by the boot mode, it should be re-configured via application software to ensure optimum performance.

All EMAC modules and interfaces require that PLL2 be enabled and that the input clock at CLKIN2 be 25 MHz. Otherwise, operation is undefined.

The CLKIN2 input contains an internal pull-down resistor and it can be left not connected if EMAC is not needed.

The RGMII interface HSTL buffers can either be operated at 1.5 V or 1.8 V. This is done by powering the DV_{DD15} supply at either 1.5 V or 1.8 V. Operation at either of these voltages uses the same AC timings. 1.8-V operation consumes slightly more power than 1.5-V operation but eliminates the need for creation of a separate 1.5-V supply. $V_{REFHSTL}$ is generated using a resistor divider from DV_{DD15} and, therefore, scales accordingly.

All LVCMOS EMAC pins contain internal pull-up or pull-down resistors. These are enabled or disabled based on the settings of GP05/EMAC1_EN, MACSEL0[2:0], and MACSEL1[1:0]. Signals that are not used can be left not connected. For unused RGMII signals, these can be left floating if DV_{DD15} and $V_{REFHSTL}$ are connected to GND. Alternatively, if these supplies are powered, the RGMII input pins should be pulled to ground.

The 3.3-V MDIO pins GMDCLK and GMDIO only have their internal pull-up resistors enabled when MACSEL0 indicates RGMII. If these pins contain any value other than [011], the IPU resistors are disabled and an external pull-up resistor is needed on each of these two pins.

6.6.2 GMII/MII System Implementation

For termination, follow the switch/PHY recommendations. If none are provided, it is recommended to use series resistance terminations on the clock lines and optionally on the data lines. Typical values of 22 Ω or 33 Ω are normally adequate but IBIS simulations can be used to verify the best value with a specific board implementation.

The MII interface expects to receive MTCLK and MRCLK as inputs. This is the standard configuration for connecting directly to a PHY. When implementing the MII interface with an Ethernet switch, the one chosen must be configurable such that it can drive both clocks as outputs.

GMII is a source-synchronous interface with clock and sync timing propagated in both directions. It is designed for point-to-point implementations on a single board. Because this interface operates at 125 MHz, trace routing and length must be controlled.

6.6.3 System Implementation of RMII

The RMII reference clock is an input. This allows the EMAC port to be connected to either a switch or a PHY. An external clock source should provide an aligned reference clock to the RMII reference clock input and to the RMII device connected to the other side of the interface. This clock should be provided to both RMII endpoints by a zero-delay clock buffer and matched-length clock traces.

6.6.4 S3MII System Implementation

S3MII is a source-synchronous interface with clock and sync timing propagated in both directions. It is designed for point-to-point implementations on a single board and also across a backplane. Because this interface operates at 125 MHz, trace routing and length must be controlled.

6.6.5 RGMII System Implementation

The RGMII interface is compliant with the RGMII version 2.0 specification found at http://www.hp.com/rnd/pdfs/RGMIIv2_0_final_hp.pdf.

The electrical signaling is compatible to JEDEC specification JESD8-6 (http://www.jedec.org/download/search/jesd8-6.pdf).

Although the JEDEC specification specifically details 1.5-V HSTL signaling, the C6472/TCI6486 device and most other RGMII v2.0 devices support operation at 1.8 V. Some devices support RGMII v1.3 (LVCMOS levels) but not RGMII v2.0 levels. Information on how to perform voltage translation from the C6472/TCI6486 1.5-V/1.8-V interface to an LVCMOS 2.5-V/3.3-V interface that operates at gigabit speeds (125 MHz) is given in Appendix A.

The RGMII interface operates at 125 MHz and clocks data on both edges of the clocks. This connection should be routed with high-speed interface routing rules. The RGMII specification provides timing information at both the receiver and the transmitter. The user must verify that the timing variations due to board topology are not more than allowed by the RGMII specification. C6472/TCI6486 HSTL IBIS models are provided to aid in this analysis.

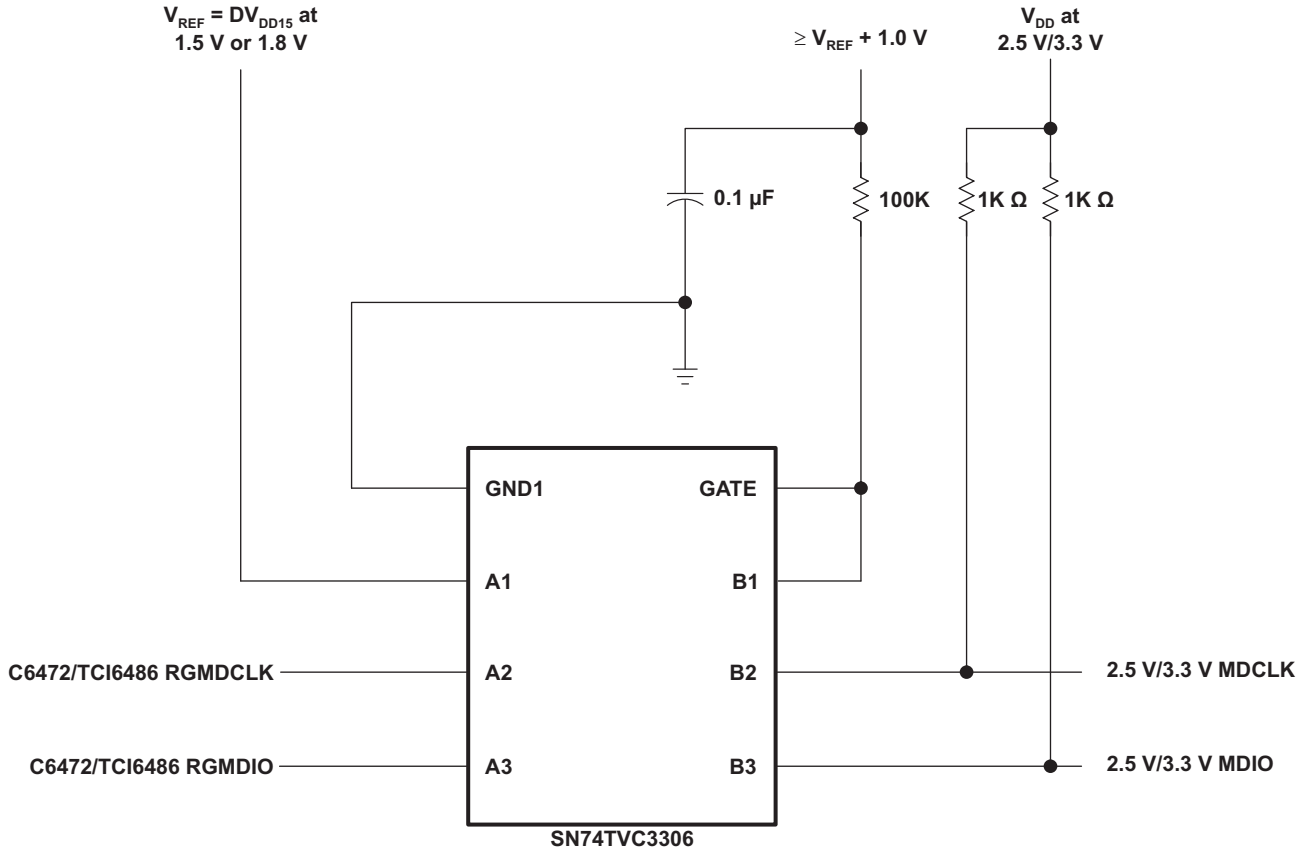
The C6472/TCI6486 device implements an internal delay (referred to as RGMII-ID in the RGMII specification) on the transmit signals but not on the receive signals. So, the connected device should use normal mode on the transmit side (no delay) and internal delay mode on the receive side. If the connected device does not support internal delay on the receive side, the proper delay needs to be created at the board level by routing the RXC signal longer than the receive data signals. The RGMII specification calls for this trace delay to be between 1.5 ns and 2.0 ns. Assuming a trace flight time of 170 ps/inch, the clock should be routed about 10.3 inches longer than the data and control. Flight time is dependent on board stackup and this length should be adjusted for the flight time of the specific board design.

The RGMII connections between the DSP and the PHY or switch are high-speed source-synchronous links. As such, they all need series termination resistors close to the driver side of each net. They should also be routed together with similar via placement and loosely length-matched to within 250 mils for each direction.

The C6472/TCI6486 RGMII interface supports the optional in-band signaling defined in the v2.0 interface specification. It can automatically detect and adapt to the reported link status. The implementation also offers a feature to force the internal state of link status, link speed, and duplex so that the in-band signaling is not required.

Some RGMII v2.0 devices have the MDIO interface implemented as 2.5-V/3.3-V LVCMOS. If RGMII is selected for EMAC0 on the C6472/TCI6486 device, only the HSTL MDIO interface is active. The circuit shown in Figure 13 has been used for this purpose. For more information and additional voltage translation options, see the *Selecting the Right Level-Translation Solution* application report (SCEA035).

Figure 13. HSTL-to-LVCMOS Translation



6.7 UTOPIA

Documentation for UTOPIA:

- *TMS320C6472/TMS320TCI6486 DSP Universal Test and Operations PHY Interface for ATM 2 (UTOPIA2) User's Guide* (SPRUEG2)
- *TMS320TCI648x Bootloader User's Guide* (SPRUEA7)
- *TMS320C645x/C647x Bootloader User's Guide*(SPRUEC6)
- *TCI6486 ZTZ BSDL Model* (SPRM316)
- *C6472 ZTZ BSDL Model* (SPRM384)
- *Using IBIS Models for Timing Analysis* (SPRA839)

6.7.1 UTOPIA Configuration

The UTOPIA RX and TX clocks are supplied externally and support clock rates up to 50 MHz. These must be provided to all devices attached to the UTOPIA bus including the UTOPIA master from a zero-delay clock buffer. These clock nets need series termination resistors and they need to be length-matched.

It is possible to configure the C6472/TCI6486 device to bootload application code over the UTOPIA interface. Boot over UTOPIA is a feature that is selected using boot-mode options. For details on boot-mode options, see the *TMS320TCI6486 Communications Infrastructure* data manual (SPRS300) or the *TMS320C6472 Fixed-Point Digital Signal Processor* data manual (SPRS612) and the *TMS320TCI648x Bootloader User's Guide* (SPRUEA7) or the *TMS320C645x/C647x Bootloader User's Guide*(SPRUEC6).

Even if the UTOPIA interface is enabled by the boot mode, it should be re-configured via application software to ensure optimum performance.

If UTOPIA is not used, the configuration input GP01/UTOPIA_EN or the corresponding bits in the DEVCTL can be configured to disable the output buffers and enable the internal pull-up and pull-down resistors on these pins. The bits in the DEVCTL register also allow for 8-bit UTOPIA operation. When configured this way, the UXDATA[15:8] and URDATA[15:8] pins can be left not connected because the internal pull-down resistors will be enabled.

6.7.2 UTOPIA System Implementation

The UTOPIA interface supports multiple devices on the same bus using polled, multi-PHY mode.

The 50 MHz operation should not be an issue in a point-to-point connection. However, if multiple devices are loaded on the bus, operation at 50 MHz may not be possible. It is recommended to run IBIS simulations to check the signal integrity and maximum operating frequency for a particular board topology.

6.8 Serial RapidIO (SRIO)

Documentation for SRIO:

- *TMS320C6472/TMS320TCI648x DSP Serial RapidIO User's Guide* (SPRUE13)
- *TMS320C6472/TMS320TCI6486 Serial RapidIO Implementation Guidelines* (SPRAAT9)
- *TMS320TCI648x Bootloader User's Guide* (SPRUEA7)
- *TMS320C645x/C647x Bootloader User's Guide*(SPRUEC6)

6.8.1 SRIO Configuration

The SRIO peripheral on the C6472/TCI6486 device is a totally independent module. It has separate input and output pins as well as separate power supply and clock inputs. It can be completely powered down without impacting the operation of the remainder of the DSP. When it is operational, it provides a flexible, low-pin-count, high-throughput packet interface for data transfer.

The SRIO peripheral is enabled/disabled by the input RIOEN, as defined in the *TMS320TCI6486 Communications Infrastructure* data manual (SPRS300) or the *TMS320C6472 Fixed-Point Digital Signal Processor* data manual (SPRS612). Even if enabled by this pin, it still needs to be enabled via software after a reset.

There are two SRIO lanes on the C6472/TCI6486 device. They can be enabled and disabled individually. They can be configured for either 1.25 Gbps, 2.5 Gbps, or 3.125 Gbps but both lanes must operate at the same data rate.

SRIO requires a dedicated differential reference clock: RIOCLKP and RIOCLKN. Recommended frequencies for this clock are 125 MHz and 156.25 MHz. The serializer/deserializer (SERDES) used in the SRIO solution has a PLL that needs to be configured based on this reference clock and the desired link rate. Link rates can be full, half, or quarter rate relative to the PLL frequency. See Table 9 for PLL multiplier settings relative to link rate.

Table 9. SRIO PLL Multiplier Settings

Reference Clock	PLL Multiplier	Full Rate	Half Rate	Quarter Rate
125 MHz	12.5	3.125 Gbps	not used	not used
156.25 MHz	10	3.125 Gbps	not used	not used
125 MHz	10	2.5 Gbps	1.25 Gbps	not used
156.25 MHz	8	2.5 Gbps	1.25 Gbps	not used

Even if the SRIO interface is enabled by the boot mode, it should be re-configured via application software to ensure optimum performance.

It is possible to configure the C6472/TCI6486 device to bootload application code over the SRIO interface. Boot over SRIO is a feature that is selected using boot-mode options. For details on boot-mode options, see the *TMS320TCI6486 Communications Infrastructure* data manual (SPRS300) or the *TMS320C6472 Fixed-Point Digital Signal Processor* data manual (SPRS612) and the *TMS320TCI648x Bootloader User's Guide* (SPRUEA7) or the *TMS320C645x/C647x Bootloader User's Guide*(SPRUEC6).

SRIO power pins can be connected to ground or left floating in order to reduce power. Alternatively, if the SRIO peripheral is enabled but only one link is used, the pins for the unused link can be left floating and no terminations are needed.

6.8.2 SRIO System Implementation

For information regarding supported topologies and layout guidelines, see the *TMS320C6472/TMS320TCI6486 Serial RapidIO Implementation Guidelines* (SPRAAT9). Suggestions on SRIO reference clocking solutions can be found in Section 3.2.3. SRIO power planes and power filtering requirements are covered in Section 4.

6.9 DDR2

Documentation for DDR2:

- *TMS320C6472/TMS320TCI648x DSP DDR2 Memory Controller User's Guide* (SPRU894)
- *TMS320C6472/TMS320TCI6486 DDR2 Implementation Guidelines* (SPRAAT7)
- *TMS320TCI648x Bootloader User's Guide* (SPRUEA7)
- *TMS320C645x/C647x Bootloader User's Guide*(SPRUEC6)
- JEDEC JESD79-2A: http://www.jedec.org/download/search/JESD79-2A.pdf

6.9.1 DDR2 Configuration

The DDR2 peripheral is enabled/disabled by the input DDREN, as defined in the *TMS320TCI6486 Communications Infrastructure* data manual (SPRS300) or the *TMS320C6472 Fixed-Point Digital Signal Processor* data manual (SPRS612). Even if enabled by this pin, it still needs to be enabled via software after a reset.

The DDR2 clock is derived from PLL3, which uses the CLKIN3 reference clock input. The DDR2 clock is 10x the CLKIN3 frequency. Therefore, a 26.667 MHz input to CLKIN3 runs the DDR clock at 266.67 MHz to support DDR2-533 operation. Since the PLL3 multiplier is fixed, the clock input CLKIN3 must be adjusted to support the DDR2 operating range from DDR2-400 up to DDR2-533.

If the DDR2 peripheral is powered but disabled, all interface signals can be left floating as long as $V_{REFSSTL}$ is connected to GND. Alternatively, if all DDR2 power sources are connected to ground or left floating, all of the DDR2 inputs and outputs can also be left not connected. CLKIN3 has an internal pull-down resistor and it can be left floating if not used.

If the DDR2 is operated in 16-bit mode, the upper DDR2 bi-directional pins should be pulled to valid states. BSDDQS2P, BSDDQS3P, and BED[31:16] should have pull-up resistors to DV_{DD18}. BSDDQS2N and BSDDQS3N should have pull-down resistors to GND. BSDDQM2 and BSDDQM3 can be left not connected.

6.9.2 DDR2 System Implementation

For information regarding supported topologies and layout guidelines, see the *TMS320C6472/TMS320TCI6486 DDR2 Implementation Guidelines* (SPRAAT7). Suggestions on CLKIN3 reference clocking solutions can be found in Section 3.2.2. DDR power planes and power filtering requirements are covered in Section 4.

6.10 JTAG/Emulation

Documentation for JTAG/emulation:

- *Emulation and Trace Headers Technical Reference Manual* (SPRU655)
- *XDS560 Emulator Technical Reference* (SPRU589)
- *TCI6486 ZTZ BSDL Model* (SPRM316)
- *C6472 ZTZ BSDL Model* (SPRM384)

6.10.1 JTAG/Emulation Configuration

The JTAG interface can be used for boundary scan and emulation. The boundary scan implementation is compliant to both IEEE 1149.1 and 1149.6 (for Serial RapidIO ports). Boundary scan can be used regardless of the device configuration.

As an emulation interface, the JTAG port can be used in various modes:

- Standard emulation: requires only five standard JTAG signals.
- HS-RTDX emulation: requires five standard JTAG signals plus EMU0 and EMU1. EMU0 and EMU1 are bi-directional in this mode.
- Trace port: the trace port allows real-time dumping of certain internal data. The trace port uses the EMU[18:0] pins to output the trace data. However, the number of pins used is configurable and limited to those currently supported in software.

Emulation can be used regardless of the device configuration.

For supported JTAG clocking rates (TCLK), see the *TMS320TCI6486 Communications Infrastructure* data manual (SPRS300) or the *TMS320C6472 Fixed-Point Digital Signal Processor* data manual (SPRS612). The EMU[18:0] signals can operate up to 166 Mbps, depending on the quality of the board-level implementation.

Any unused emulation port signals can be left floating.

6.10.2 JTAG/Emulation System Implementation

For most system-level implementation details, see the *Emulation and Trace Headers Technical Reference Manual* (SPRU655).

For a single DSP connection where the trace feature will not be used the standard non-buffered connections can be used. If the trace will be used, the JTAG signals should be buffered and TCLK and RTCLK should be buffered separately.

If multiple DSPs are included on the board and a chained JTAG interface is desired, the suggested implementation is to use a single 60-pin header with the following connections:

- Buffer and daisy chain the TDI and TDO.
- Buffer and connect TCLK, TMS, and $\overline{\text{TRST}}$ to all DSPs. RTCLK should be buffered separately from TCLK.
- Connect EMU0 and EMU1 to all DSPs (do not buffer).
- Connect EMU18:2 to one of the DSPs (the one which will be traced).

No external pull-up or pull-down resistors are needed at the DSP pins since there are internal pull-ups/downs on all emulation signals. However, if the JTAG interface is buffered, the signals at the emulation/JTAG connector require biasing. TCLK and $\overline{\text{TRST}}$ should have pull-down resistors. TMS and TDI should have pull-up resistors.

The *Emulation and Trace Headers Technical Reference Manual* (SPRU655) indicates that there should be a 100-kΩ resistor between the TVD pin and the devices JTAG I/O voltage. This value results in a significant voltage drop with some emulators, so the resistor should be 1 kΩ, instead.

It is not recommended to add both a 60-pin header and a 14-pin header due to signal integrity concerns. 60-pin-to-14-pin adapters are available to allow connection of emulators that only support the 14-pin connector.

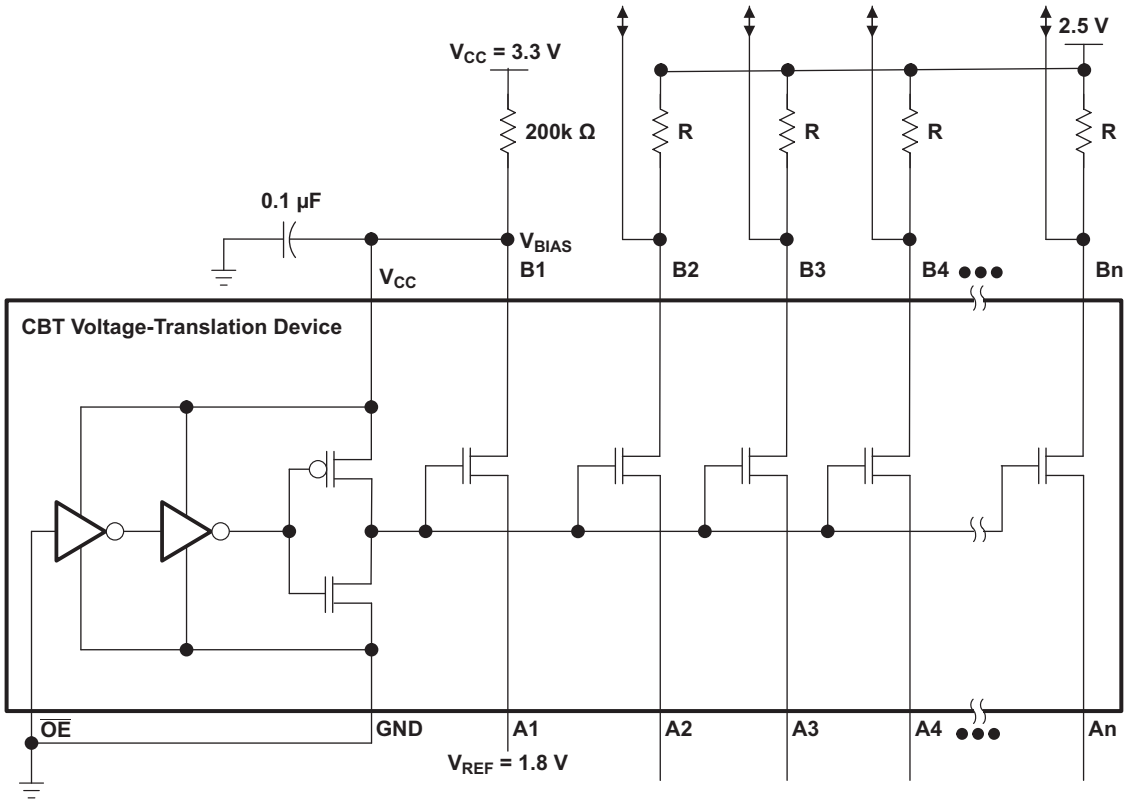
Appendix A C6472/TCI6486 RGMII 1.5-V/1.8-V-to-2.5-V/3.3-V Translation

The C6472/TCI6486 device includes a variable voltage RGMII for connection to a gigabit-capable Ethernet switch or PHY. The C6472/TCI6486 interface can be configured to run at either 1.5 V or 1.8 V I/O; controlled directly by the voltage applied to the DV_{DD15} pins of the device (see the device data manual). These rails are complaint with the RGMII specification; however, in practice it has been found that in many cases a level translation is required between industries offering for Ethernet switch connections, which are slightly slower in migration to these lower voltage nodes.

Voltage translation of the RGMII interface is a somewhat complicated task, insomuch as the interface must be level-translated but still support dual-data rates at up to 125 MHz operation. This can be very difficult to achieve using standard LVCMOS-type buffers for two reasons. First, such buffers often add up to 4 ns propagation delay to the buffered signals, making timing margins exceptionally small at the 125 MHz rate. Second, such buffers often provide little to no guarantee of relative propagation delays across buffers in the same device and further specify all timings with only a single output switching, which is not realistic in a gigabit Ethernet application.

As an alternative to the LVCMOS type buffers, a good solution can be found using TVC-type buffers or CBT buffers in a TVC configuration. Texas Instruments has an excellent application report describing the configuration, *Selecting the Right Level Translation Solution* (SCEA035). An example of this application is shown in Figure 14 using a CBT3245 in a TVC voltage-clamp configuration. The CBT3245 is an 8 in/out buffer, making it a nice fit for the six lines requiring translation in a single direction of a gigabit Ethernet application. Using this solution, two CBT3245s can be used: one for transmit, one for receive to complete the translation.

Figure 14. RGMII Voltage-Level Translation Circuit



The CBT and TVC families of buffers are excellent in this application. Both are simple FET switches, which offer sub-ns propagation delays. Because each FET switch is independent, the relative delays are matched very closely because process variations affect all switches equally. Unlike LVCMOS buffers, these switches offer no additional current drive, however, since gigabit Ethernet connections are simple point-point connections this is not a concern.

As an FET switch, the circuit in either the TVC or CBT application is the same. A single in/out pair is chosen to set the voltage clamp voltage to 1.8 V on the C6472/TCI6486 side; 1.5 V could also be used if that voltage is used for the C6472/TCI6486 RGMII interface. Because all the gates of the CBT/TVC in/out pairs are connected, this sets the clamp voltage for all the other pairs of ins/outs because VGS for the FET is fixed. However, note that the buffer itself is powered using a 3.3 V supply. This is necessary to establish a voltage at least 1 V greater than the low-side clamp voltage (18 V + 1 V = 2.8 V) in this case.

The configuration shown above is technically a bidirectional solution; though gigabit Ethernet by its definition is unidirectional. When driving from the C6472/TCI6486 to the switch/PHY, signals vary from 0 V to 1.5 V/1.8 V. At the low (0 V) voltage level, the FET is turned on and both sides of the buffer see a low level. When a 1.5 V/1.8 V logic high is applied, the FET is turned off because this voltage matches (nearly) the voltage applied to the gate. In this case, the pullups on the high voltage side (switch/PHY side) of the buffer pull the output to the high-side rail. Therefore, in both cases the logic levels on both sides of the buffer match to their respective rails. The application circuit shown above is shown for the C6472/TCI6486's transmit direction; that is, from the C6472/TCI6486 to the switch. In the receive direction, the application circuit is the same except that the pullups to the 2.5 V side of the buffer, the switch/PHY side, are not needed and should be omitted. In this case, pullups to 1.5 V/1.8 V are not required, as the buffer acts as a clamp and holds the output voltage to the 1.5 V/1.8 V level, providing the translation directly.

The values for the pullups on the high-voltage side of the CBT/TVC buffer are important. The basic trade-off that needs to be made is finding a value that is strong enough to pull to the high-side rail quickly to produce a good low-high edge rate (recall that this is when the FET turns off), but is not too strong so as to not allow the low side to pull the output to a level below the V_{IL} specification of the switch/PHY device when a low is driven (and the FET is on).

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