Interfacing TMS320VC5510 to SBSRAM

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ABSTRACT

The TMS320C55x™ (C55x™) External Memory Interface (EMIF) supports a glueless interface to high-density and high-speed synchronous burst static random access memories (SBSRAM). For clocking SBSRAMs, the EMIF can operate at numerous C55x DSP CPU clock output frequency multiples. Examples are given for system-level connection and register configuration for the different types of SBSRAM memory supported.

NOTE: Before interfacing C55x devices with SBSRAM within a particular system application, please consult the latest device datasheets and errata to confirm which silicon revisions support SBSRAM.

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1 C55x SBSRAM Interface

The TMS320C55x (C55x) External Memory Interface (EMIF) supports a glueless interface to high-density and high-speed SBSRAMs. The EMIF interfaces directly to 32-bit-wide industry-standard, non-parity synchronous burst SRAMs. SBSRAMs are available in both Flow Through and Pipeline types. However, the C55x EMIF interfaces only to Pipeline SBSRAM. Pipeline SBSRAM has the ability to operate at higher frequencies with sustained throughput. Also, the C55x EMIF can interface to parity type Pipeline SBSRAM memories, but the unused parity bits on these memories should be tied low. The C55x EMIF can operate at the following DSP CPU clock output frequency multiples for SBSRAM: 1x and 1/2x.

The signals provided on the C55x EMIF pins for SBSRAM usage are described in Table 1. For a complete listing of all C55x pins, consult the latest device datasheets.

Table 1. C55x EMIF/SBSRAM Signal Descriptions

Signal	State	Description
A21 (MSB) to A0 (LSB)	O/Z	22-bit parallel address port. Internal data, program and DMA busses are multiplexed into a single external address bus. Placed in high impedance in hold mode.
D31 (MSB) to D0 (LSB)	I/O/Z	32-bit parallel data port. Internal data, program and DMA busses are multiplexed into a single external data bus. Outputs placed in high impedance in hold mode.
$\overline{\text{CE0}}$	O/Z	Active-low chip select for memory space CE0. Placed in high impedance in hold mode.
$\overline{\text{CE1}}$	O/Z	Active-low chip select for memory space CE1. Placed in high impedance in hold mode.
$\overline{\text{CE2}}$	O/Z	Active-low chip select for memory space CE2. Placed in high impedance in hold mode.
$\overline{\text{CE3}}$	O/Z	Active-low chip select for memory space CE3. Placed in high impedance in hold mode.
$\overline{\text{BE}}$ [3:0]	O/Z	Byte enable control. Placed in high impedance in hold mode.
$\overline{\text{SSADS}}$	O/Z	SBSRAM address strobe. Placed in high impedance in hold mode.
$\overline{\text{SSOE}}$	O/Z	SBSRAM output enable. Placed in high impedance in hold mode.
$\overline{\text{SSWE}}$	O/Z	SBSRAM write enable. Placed in high impedance in hold mode.
CLKMEM	O/Z	Memory interface clock for SBSRAM or SDRAM. Placed in high impedance in hold mode.

2 SBSRAM Interface Operation

The three C55x EMIF SBSRAM specific control signals ($\overline{\text{SSADS}}$, $\overline{\text{SSOE}}$, and $\overline{\text{SSWE}}$) are latched by the SBSRAM on the rising edge of CLKMEM to determine the current operation. These signals are only valid if the chip select line for the SBSRAM is driven low by $\overline{\text{CE}}$n. The $\overline{\text{CE}}$ [3:0] signals are decoded by the EMIF from the address and enable the SBSRAM in only a single CE memory region. The $\overline{\text{SSADS}}$ signal indicates when the SBSRAM should latch a new address. The $\overline{\text{SSOE}}$ signal enables the output of the bidirectional data bus pins of the SBSRAM. The $\overline{\text{SSWE}}$ signal determines which CLKMEM rising edges are used to latch the write data. The EMIF $\overline{\text{BE}}$[3:0] signals in conjunction with the $\overline{\text{SSWE}}$ signal, selectively allow one or more bytes to be written at a time to the SBSRAM. For reads, all four $\overline{\text{BE}}$[3:0] signals are driven active-low. The C55x EMIF transfers the appropriate data to the proper internal busses, depending on the type of read: byte, single word, double word, or dual word. For more specific details on SBSRAM interface operation, including read and write timing characteristics, refer to *TMS320C55x Peripherals Reference Guide* (SPRU317) and the C55x device datasheets.

3 C55x EMIF Registers

Configuration of the C55x EMIF is achieved through a set of memory-mapped registers that are addressable through internal I/O memory space. The memory-mapped registers are shown in Table 2. **The shaded sections are irrelevant to SBSRAM.**

Table 2. C55x EMIF Memory-mapped Registers

I/O Space Word Address	Name
0x0800	EMIF Global Control Register
0x0801	EMIF Global Reset Register
0x0802	EMIF Bus Error Status Register
0x0803	EMIF CE0 Space Control Register 1
0x0804	EMIF CE0 Space Control Register 2
0x0805	EMIF CE0 Space Control Register 3
0x0806	EMIF CE1 Space Control Register 1
0x0807	EMIF CE1 Space Control Register 2
0x0808	EMIF CE1 Space Control Register 3
0x0809	EMIF CE2 Space Control Register 1
0x080A	EMIF CE2 Space Control Register 2
0x080B	EMIF CE2 Space Control Register 3
0x080C	EMIF CE3 Space Control Register 1
0x080D	EMIF CE3 Space Control Register 2
0x080E	EMIF CE3 Space Control Register 3
0x080F	EMIF SDRAM Control Register 1
0x0810	EMIF SDRAM Period Register
0x0811	EMIF SDRAM Counter Register
0x0812	EMIF SDRAM Initialization Register
0x0813	EMIF SDRAM Control Register 2

3.1 EMIF Global Control Register

The EMIF Global Control Register contains configurable parameters that are common to all CE spaces. The register bit locations and brief parameter descriptions are given in Figure 1 and Table 3. The primary bits of concern for SBSRAM in this register are Memory Clock Enable (MEMCEN), Memory Frequency (MEMFREQ), and Write Posting Enable (WPE).

The EMIF has two write posting registers that are enabled/disabled by WPE. If write posting is enabled (WPE = 1), the write posting registers are used to store the write address and data, such that the CPU may be acknowledged by the EMIF with zero wait states. The CPU is then free to carry on with the next access, and the posted write operations will be run externally as time slots become available. If the next access is for internal memory and not for the EMIF, the internal memory access is able to run concurrently with a slower external memory write operation.

The write posting registers are freely associated with either of the two data-write data buses of the CPU (E and F busses). For example, a section of code that consists of only E bus writes benefits from two levels of write posting. When write posting is disabled (WPE = 0), a request from the E or F bus is acknowledged as the write data is driven onto the external bus. It might be useful during debug to disable write posting. Write posting is disabled at reset on the C55x device. For more details, refer to *TMS320C55x Peripherals Reference Guide* (SPRU317*)*.

15 12	11 9	8	7	6	5	4	3	2	1	0
Reserved	**MEMFREQ**	Reserved	**WPE**	Reserved	**MEMCEN**	Reserved	ARDY	$\overline{\text{HOLD}}$	$\overline{\text{HOLDA}}$	NOHOLD
R, +0	RW, +000	RW, +0	RW, +0	RW, +0	RW, +1	R, +0	R, +x	R, +x	R, +0	RW, +0

NOTES: The following applies to the register diagrams in this document:

1. R means read only.
2. W means write only.
3. RW means both read and write allowed.
4. +0 indicates the reset value is logic-low.
5. +1 indicates the reset value is logic-high.
6. +x indicates the reset value reflects the pin state or is insignificant.
7. **Shaded areas are not directly related to SBSRAM.**

Figure 1. EMIF Global Control Register Diagram

Table 3. EMIF Global Control Register Bit Field Description

Field	Description
NOHOLD	External HOLD Disable NOHOLD=0, hold enabled NOHOLD=1, hold disabled
$\overline{\text{HOLDA}}$	Value of $\overline{\text{HOLDA}}$ output
$\overline{\text{HOLD}}$	Value of $\overline{\text{HOLD}}$ input
ARDY	Value of ARDY input. The value of ARDY bit is invalid when no asynchronous accesses are occurring.
MEMCEN	Memory Clock Enable MEMCEN=0, CLKMEM held high MEMCEN=1, CLKMEM output enabled
WPE	Write Posting Enable WPE=0, Write Posting is disabled WPE=1, Write Posting is enabled
MEMFREQ	Memory Clock Frequency – controls the CLKMEM output clock frequency: Value CLKMEM frequency 000 DSP CPU CLKOUT frequency 001 DSP CPU CLKOUT frequency /2 Other Reserved

NOTE: MEMFREQ should be changed when MEMCEN = 0

3.2 EMIF Global Reset Register

Any write to this register will cause a reset of the EMIF state machine, but does not change the current configuration values. This register cannot be read (See Figure 2).

Figure 2. C55x EMIF Global Reset Register

3.3 C55x CE Space Control Registers

There are four CE spaces supported by the C55x EMIF. Each space is configured by a set of three CE Space Control Registers. The MTYPE field identifies the memory type for the CE space. In CEn Space Control Register 1, bits 14:12, MTYPE=100b selects SBSRAM. **The remaining fields in the register do not apply to SBSRAM**. Figure 3, Figure 4, and Figure 5 give the bit arrangements for the CE Space Control Registers. Table 4 contains detailed descriptions of the configuration fields.

15	14 12	11 8	7 2	1 0
Reserved	**MTYPE**	READ SETUP	READ STROBE	READ HOLD
R, +0	RW, +010	RW, +1111	RW, +111111	RW, +11

Figure 3. C55x EMIF CEn Space Control Register 1

15	14 12	11 8	7 2	1 0
EXTENDED HOLD READ	EXTENDED HOLD WRITE	WRITE SETUP	WRITE STROBE	WRITE HOLD
R, +01	RW, +01	RW, +1111	RW, +111111	RW, +11

Figure 4. C55x EMIF CEn Space Control Register 2

15 8	7 0
Reserved	TIMEOUT
R, +00000000	RW, +00000000

Figure 5. C55x EMIF CEn Space Control Register 3

Table 4. EMIF CEn Space Control Registers Field Description

Field	Description
READ SETUP WRITE SETUP	Setup width. Number of DSP clock cycles of setup for address, chip enable ($\overline{CE}$) and byte enables ($\overline{BE}$ [0–3]) before read strobe ($\overline{ARE}$) or write strobe ($\overline{AWE}$) falls. For asynchronous read access, this is also the setup time of $\overline{AOE}$ before $\overline{ARE}$ falls.
READ STROBE WRITE STROBE	Strobe width. The widths of read strobe ($\overline{ARE}$) and write strobe ($\overline{AWE}$) in DSP clock cycles.
READ HOLD WRITE HOLD	Hold width. Number of DSP clock cycles that address and byte strobes ($\overline{BE}$[0–3]) are held after read strobe ($\overline{ARE}$) or write strobe ($\overline{AWE}$) rises. For asynchronous read accesses, this is the hold time of $\overline{AOE}$ after $\overline{ARE}$ rising.
MTYPE	**Memory Type:** MTYPE=000b, 8-bit-wide asynchronous interface MTYPE=001b, 16-bit-wide asynchronous interface MTYPE=010b, 32-bit-wide asynchronous interface MTYPE=011b, 32-bit-wide or 16-bit-wide SDRAM. The SDACC bit in SDRAM Control Register 2 selects between 16 or 32 bits. All SDRAM widths must be the same. **MTYPE=100b, 32-bit-wide SBSRAM** MTYPE=Other, reserved
Extended Hold Read	Number of DSP clock cycles after the last asynchronous read access in a given region before a write access or access to a different region can start. All CEn signals are inactive during this period. Add 1 to the number to include the automatic 1 cycle between region changes.
Extended Hold Write	Number of DSP clock cycles after the last asynchronous write access in a given region before a Write access or access to a different region can start. All CEn signals are inactive during this period. Add 1 to the number to include the automatic 1 cycle between region changes.
TIMEOUT	Length of the bus error timeout. Only valid when the asynchronous MTYPE is selected. TIMEOUT = 0, bus error timer disabled TIMEOUT= N, bus error signaled after N (between 1 and 255) DSP clock cycles.

4 SBSRAM Interfacing Considerations

The C55x EMIF SBSRAM interface can operate at C55x DSP CPU clock output frequency multiples of 1x and 1/2x. The desired speed is selected by programming the MEMFREQ bits in the C55x EMIF Global Control Register. The $\overline{GW}$ signal provided by the major SBSRAM manufacturers allows all four bytes to be written at once. This feature is not directly supported on the C55x EMIF. However, the EMIF $\overline{BE}$[3:0] signals in conjunction with the $\overline{SSWE}$ signal, selectively allow one or more bytes to be written at a time to the SBSRAM. For reads, all four $\overline{BE}$[3:0] signals are driven active-low. The $\overline{ADV}$ signal of the SBSRAM is used to allow the SBSRAM device to generate addresses internally for interfacing to controllers which cannot provide addresses quickly enough. Nevertheless, the C55x EMIF does not require the use of this signal because it generates the addresses at the required rate. The MODE signal of the SBSRAM should be set for Linear Burst. For more specific information on the SBSRAM signals, refer to the manufacturer's datasheets.

4.1 C55x EMIF Interface to Non-parity, Pipeline SBSRAM

An example of C55x EMIF interfaced to non-parity (x32) pipeline SBSRAM is shown in Figure 6.

The SBSRAM is enabled in CE0 memory space by the EMIF $\overline{CE}$0 output connected to the SBSRAM $\overline{CE}$ input. The unused C55x EMIF $\overline{CE}$[3:1] outputs can be left floating, but the unused SBSRAM chip selects and other inputs should be tied off as shown. SBSRAM signals CE2 and $\overline{CE}$2 (chip enables) are tied to their active states. SBSRAM MODE is tied low for Linear Burst. All other unused SBSRAM signals (ZZ, $\overline{ADV}$, $\overline{ADSP}$, and $\overline{GW}$) are tied to their inactive states.

CE0 Space Control Register1 MTYPE field is set to100b.

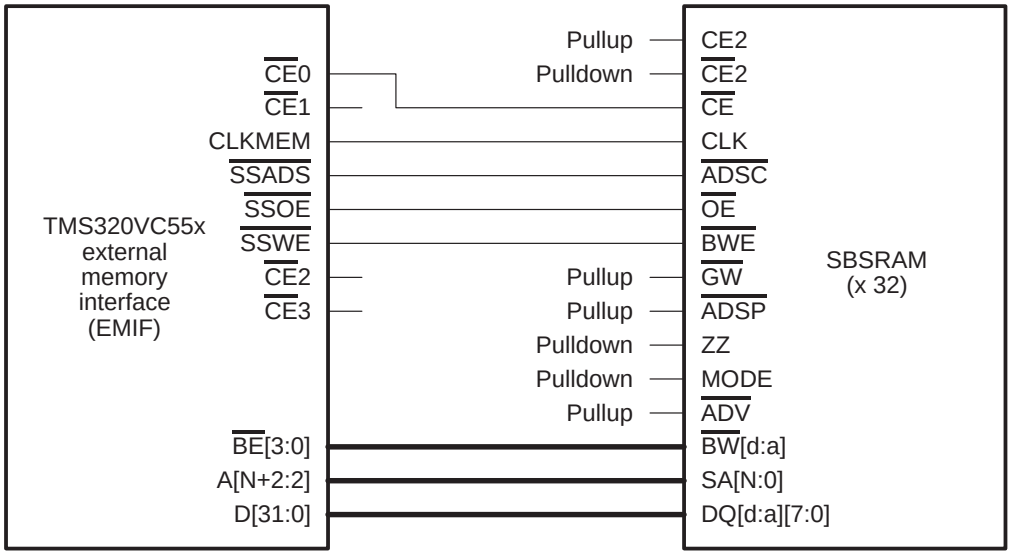

Figure 6. C55x EMIF Interface to Non-parity, Pipeline SBSRAM

4.2 C55x EMIF Interface to Parity (x36), Pipeline SBSRAM

The following example in Figure 7 shows the C55x EMIF interfaced to a parity (x36) pipeline SBSRAM. The unused parity data bits DQP [d:a] should be tied off as shown to reduce power.

CE0 Space Control Register1 MTYPE field is set to100b.

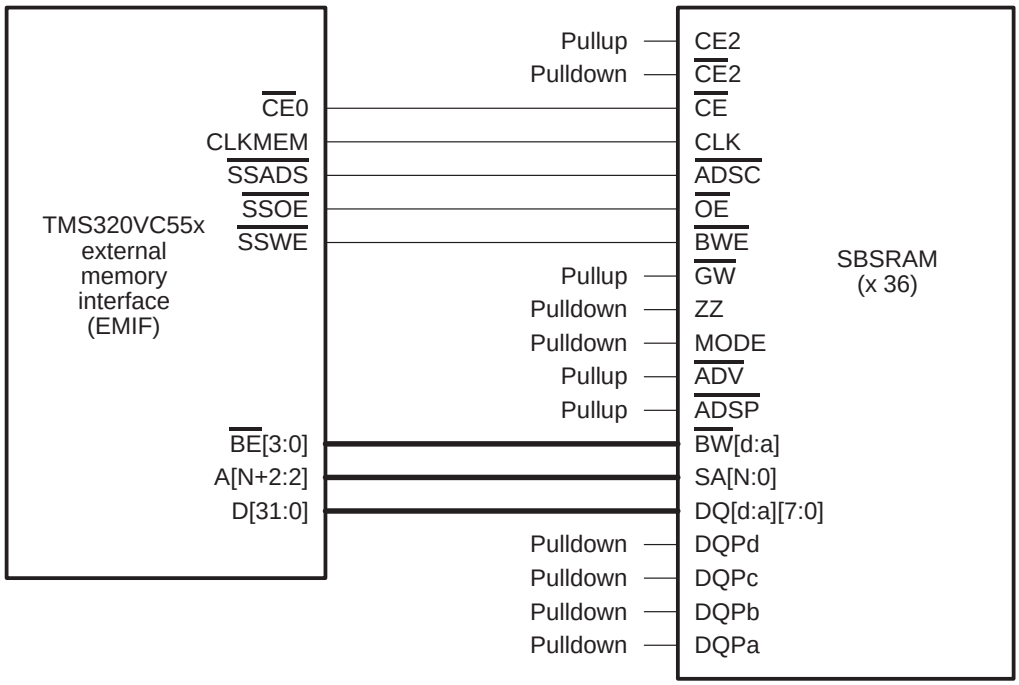

Figure 7. C55x EMIF Interface to Parity (x36), Pipeline SBSRAM

4.3 C55x EMIF Interface to 2 Parity (x18), Pipeline SBSRAMs

An example in Figure 8 shows the C55x EMIF interfaced to two parity (x18) pipeline SBSRAMs. The EMIF D[31:0] data bus and BE[3:0] byte enables are split between the two memories.

CE0 Space Control Register1 MTYPE field is set to100b.

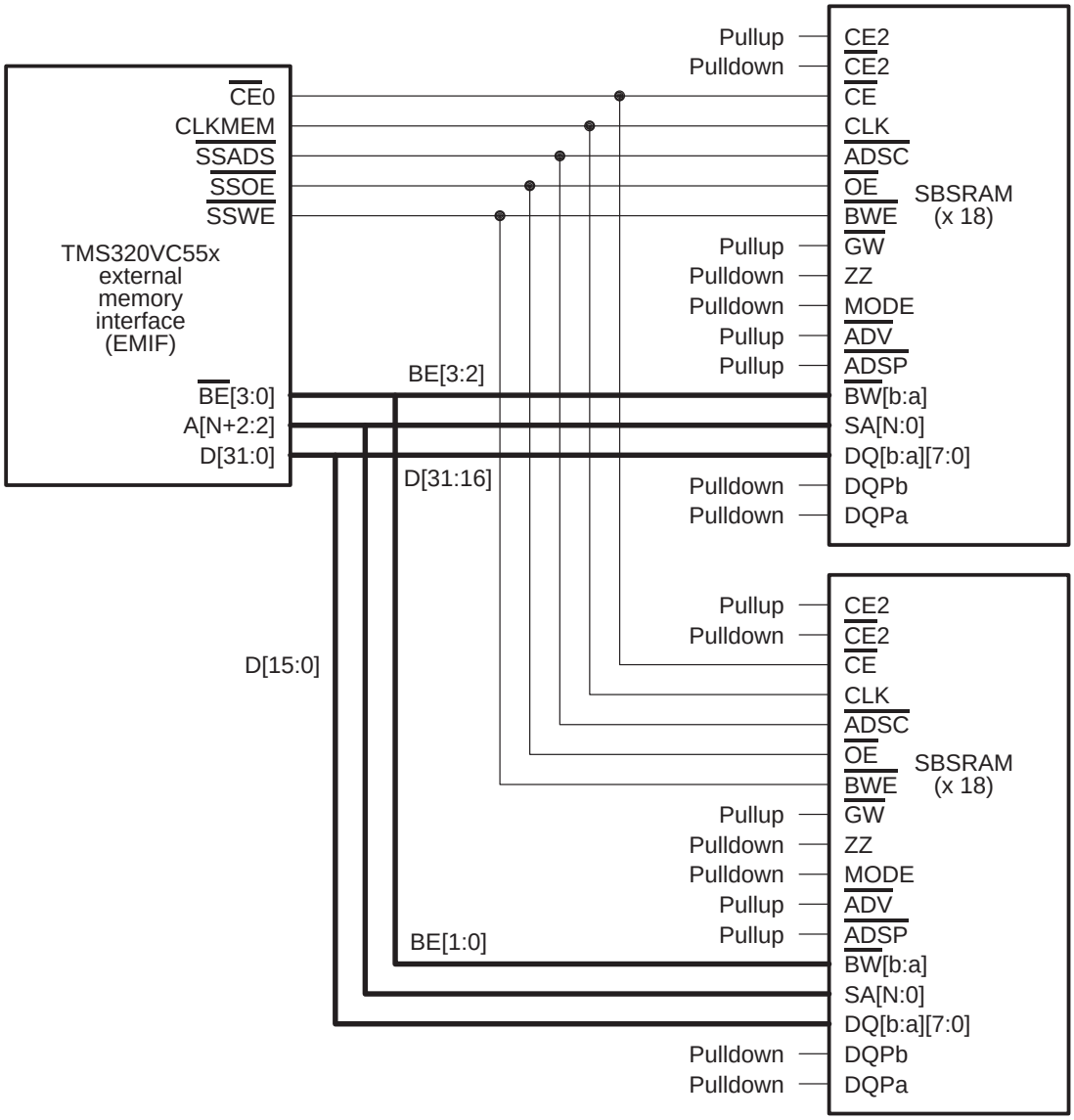

Figure 8. C55x EMIF Interface to 2 Parity (x18), Pipeline SBSRAMs

4.4 SBSRAM Power Down Modes

The major SBSRAM manufacturers support a power saving snooze mode. When an asynchronous external pin (ZZ) on the SBSRAM is active-high, the device enters a low-power standby mode. All data in the memory array is maintained, and all other SBSRAM inputs besides ZZ are ignored. For latency between disable/enable of the snooze mode and valid access to the SBSRAM consult the manufacturer's datasheet. Typically, this latency is up to four clock cycles for both entering and exiting snooze mode. The C55x EMIF does not directly support this capability. However, the enable/disable of ZZ can be accomplished with the use of a C55x general purpose I/O pin. Figure 9 shows an example of this using general purpose I/O pin IO7.

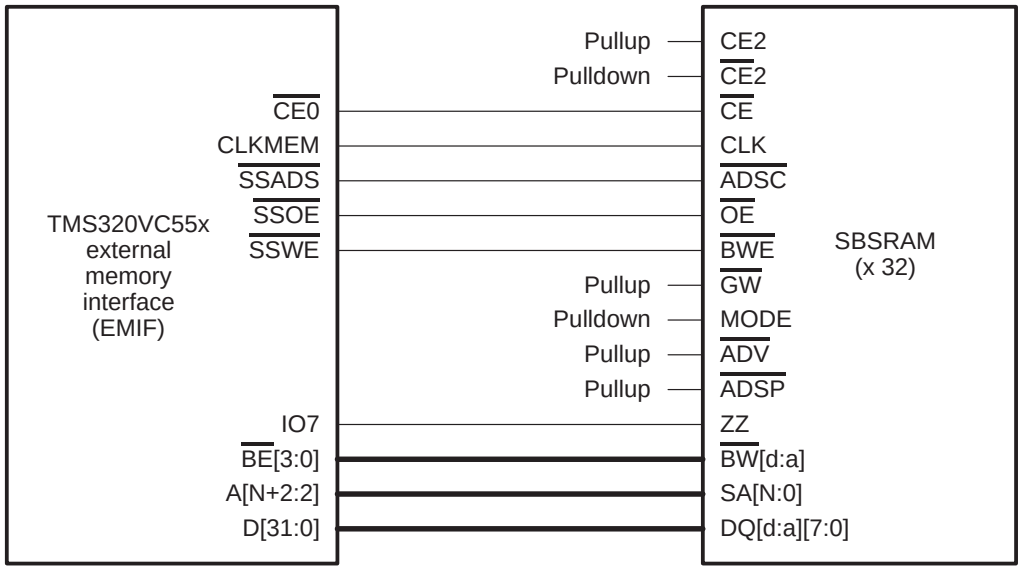

Figure 9. C55x Interface to a Non-parity (x32) SBSRAM Using IO7 to Control ZZ Power Down

The C55x EMIF does directly support another power down mode of the SBSRAM. With SBSRAM chip-select lines inactive and ADSC inactive, a reduced power state is achieved. To further reduce power, if CLKMEM is not used for other memories, CLKMEM can be turned off with the MEMCEN bit of the EMIF Global Control Register.

5 SBSRAM Memory Examples

SBSRAM memories that are compatible with the C55x EMIF are shown below in Table 5. The latest manufacturer's datasheets should be consulted prior to system implementation. Links to the manufacturer's websites are given for easy access to documentation.

Table 5. Example SBSRAMs for Use With C55x EMIF

Size	Arrangement	Manufacturer	Part Number	Manufacturer's website
16 Mbit	512K x32	Micron	MT58L512Y32P	http://www.micron.com
8 Mbit	256K x32	Micron	MT58L256L32P	http://www.micron.com
4 Mbit	128K x32	Micron	MT58L128V32P1	http://www.micron.com
2 Mbit	64K x32	Micron	MT58L64L32P	http://www.micron.com
1 Mbit	32K x32	Micron	MT58L32V32P	http://www.micron.com
2 Mbit	64K x32	NEC	mPD432232L	http://www.nec.com
1 Mbit	32K x32	NEC	mPD431632L	http://www.nec.com
4 Mbit	128K x32	Samsung	K7A403200M	http://www.samsung.com
2 Mbit	64K x32	Samsung	K7A203200M	http://www.samsung.com

6 References

1. *TMS320C55x Peripherals Reference Guide* (SPRU317).
2. *TMS320VC5510, Fixed-Point Digital Signal Processor* (SPRS076).
3. MT58L128V32P1, MT58L128V36P1, 4 Mb SYNCBURST™ SRAM, Micron Semiconductor Products, Inc.
4. Using Parity SRAMs in Nonparity Applications (TN-58-12), Micron Semiconductor Products, Inc.
5. Design Tips: SYNCBURST™ SRAM Standards (TN-58-04), Micron Semiconductor Products, Inc.

Appendix A C55x EMIF Block Diagram

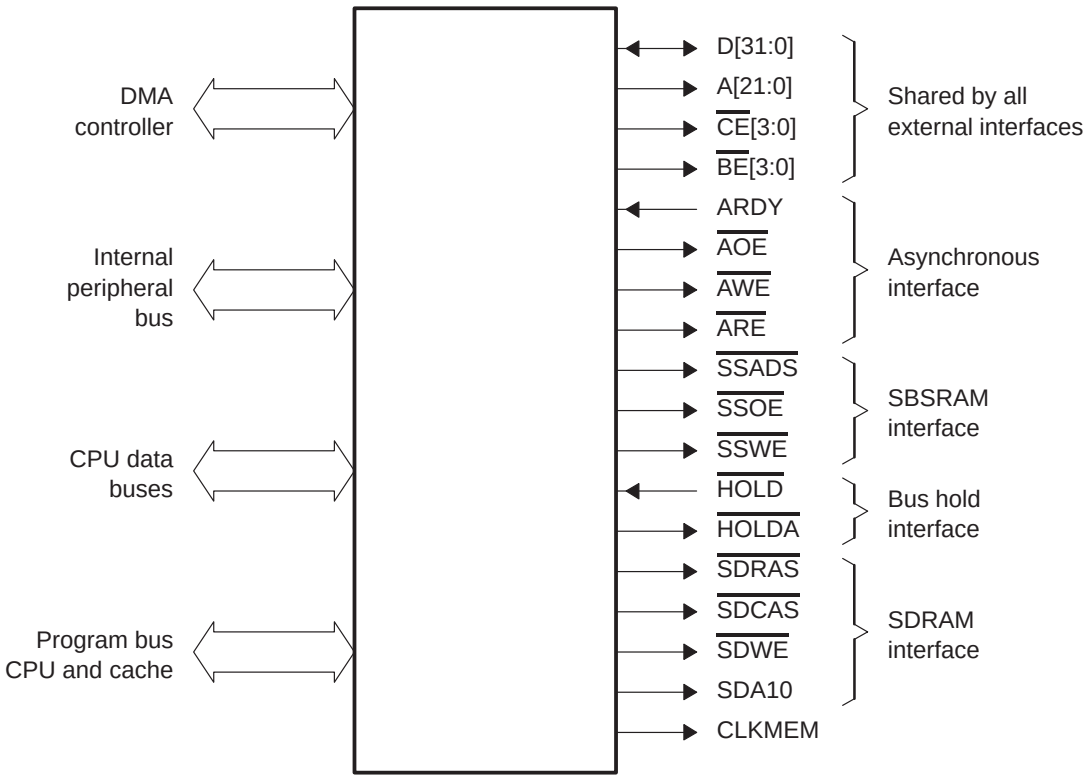

Figure A–1. C55x EMIF Block Diagram

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