Application Report
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TMS320C6000 Host Port to MPC860 Interface

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ABSTRACT

This application report describes an interface between the Motorola MPC860 microprocessor and the host port interface (HPI) of a Texas Instruments TMS320C6000™ (C6000™) digital signal processor (DSP) device. This document includes a schematic showing connections between the two devices, PAL equations, and verification that timing requirements are met for each device (tables and timing diagrams).

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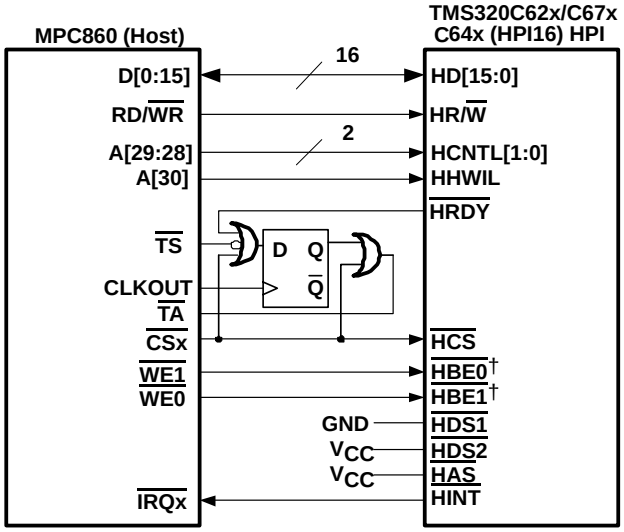
1 MPC860 Interface

The Motorola MPC860 PowerQUICC (quad integrated communication controller) is a single-chip integrated microprocessor. The PowerQUICC family incorporates the MC68360's communications-oriented peripheral set and integrates additional enhancements. The PowerQUICC family integrates a 32-bit embedded PowerPC core central processing unit (CPU), memory controller, RISC-based communication processor module (CPM), and system functions on a single chip.

Figure 1 and Figure 2 show diagrams of the host (MPC860) interface to the HPI in TMS320C62x™, TMS320C67x™, and TMS320C64x™ devices, while Table 1 shows the pin connections.



† TMS320C6201/C6701 Only

Figure 1. MPC860 to TMS320C62x/C67x/C64x (HPI16) HPI Interface Block Diagram

TMS320C62x, TMS320C67x, and TSM320C64x are trademarks of Texas Instruments.

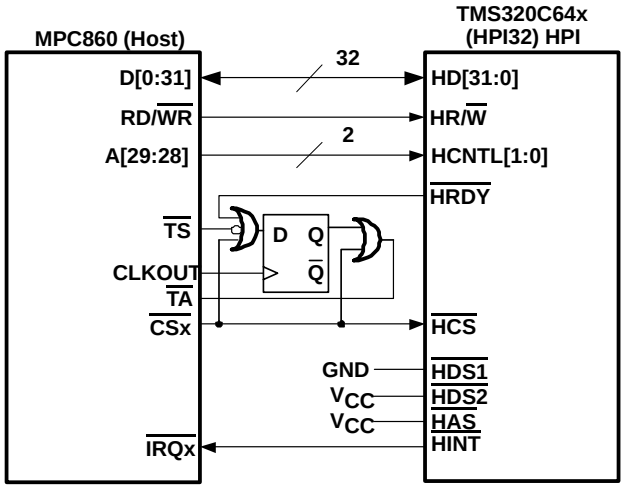


Figure 2. MPC860 to TMS320C64x (HPI32) HPI Interface Block Diagram

Table 1. MPC860 to HPI Pin Connections

HPI Pin	MPC860 Pin	Comments
HCNTL[1:0]	A[28:29]	Address bits of MPC860 are used as control signals. A31 is the LSB of the MPC860 address bus.
HHWIL	A[30]	Halfword identification input
HR/$\overline{W}$	RD/$\overline{WR}$	Indicates a read or write access
16-bit:HD[15:0] 32-bit:HD[31:0]	16-bit:D[0:15] 32-bit:HD[0:31]	MPC860 uses D[0:15] for a 16-bit port interface and D[0:31] for a 32-bit port interface. D0 is the MSB of the MPC860 data bus; HD31 is the MSB of HPI.
$\overline{HDS1}$	GND	$\overline{HDS1}$ and $\overline{HDS2}$ are internally exclusively-NORed. $\overline{HDS1}$ and $\overline{HDS2}$ are tied logic low and high, respectively, to enable data strobe at all time.
$\overline{HDS2}$	V_{CC}	See above.
$\overline{HAS}$	V_{CC}	Because host device MPC860 has separate address and data bus, $\overline{HAS}$ does not need to be used. $\overline{HAS}$ is tied inactive high.
$\overline{HCS}$	$\overline{CSx}$	Any one of $\overline{CS1}$ to $\overline{CS5}$ of MPC860 can be connected to $\overline{HCS}$ as the chip-select signal. This also serves as the data-strobe signal in this case (because no separate MPC860 data strobe signal is used).
$\overline{HBE0}$	$\overline{WE1}$	Byte enable (TMS320C6201/C6701 only)
$\overline{HBE1}$	$\overline{WE0}$	Byte enable (TMS320C6201/C6701 only)
$\overline{HRDY}$	$\overline{TA}$	SETA bit in the MPC860 option register is set to 1 to indicate that $\overline{TA}$ is generated externally by HPI. $\overline{HRDY}$ is synchronized using the bus clock and connected to $\overline{TA}$.
$\overline{HINT}$	$\overline{IRQx}$	See the *MPC860 User's Manual* for the desired interrupt level ($\overline{IRQ0}$ to $\overline{IRQ7}$).

For 32-bit accesses, the MPC860 data bus D[0:31] is connected to the HPI data bus HD[31:0] in reverse order, that is, D0 is connected to HD31, D1 is connected to HD30, D2 is connected to HD29, etc. This is because the most significant bit (MSB) of the MPC860 data bus is D0 and the MSB of the HPI data bus is HD32. For 16-bit accesses, the MPC860 data bus D[0:15] is connected to the HPI data bus HD[15:0] in reverse order. D0 is connected to HD15, D1 is connected to HD14, etc.

The transfer-acknowledge (TA) signal of the MPC860 chip is a synchronous signal; therefore, the HRDY signal of the HPI must be synchronized for the interface to function properly.

1.1 Configuration

The MPC860's memory controller is responsible for the control of up to eight memory banks and provides a set of eight programmable chip-select signals. A chip-select of the MPC860 is tied to the $\overline{\text{HCS}}$ input of the HPI. This simplifies the interfacing to the HPI.

Status bits for each one of the memory banks are in the memory controller status register (MSTAT). There is only one MSTAT for the entire memory controller. Each memory bank has a base register (BR) and an option register (OR). The MSTAT reports write-protect violations and parity errors for every bank. The BRx and the ORx registers are specific to memory bank x. The BR contains a valid (V) bit that indicates that the register information for that chip-select is valid.

Each one of the OR registers defines the attributes for the general-purpose chip-select machine when accessing the corresponding bank.

The general-purpose chip-select machine (GPCM) allows a glue-less and flexible interface between the MPC860 and HPI. If the MS bits in the BRx of the selected bank (Bank x) select the GPCM machine, the attributes for the memory cycle initiated are taken from the ORx register. These attributes include the CSNT, ACS(0:1), SCY(0:3), TRLX, EHTR, and SETA fields.

The configuration of the BR and OR is shown in Table 2 and Table 3.

Table 2. Base Register (BR) Relevant Bits

Bit Field	Description	Value
BA[0:16]	Base address The base-address field, the upper 17 bits of each base-address register, and the address-type code field are compared to the address on the address bus to determine if a memory bank controlled by the memory controller is being accessed by an internal bus master. These bits are used in conjunction with the AM[0:16] bits in the OR.	
PS[0:1]	Port Size This field specifies the port size of this memory region.	10 = 16-bit port size 00 = 32-bit port size
WP	Write protect This bit can restrict write accesses within the address range of a base register.	0 = Both read and write accesses are allowed.
MS[0:1]	Machine select This field specifies the machine selected for the memory operations handling.	00 = GPCM
V	Valid bit This bit indicates that the contents of the base register and the option register pair are valid. The $\overline{\text{CS}}$ signal does not assert until the V-bit is set.	1 = This bank is valid.

Table 3. Option Register (OR) Relevant Bits

Bit Field	Description	Value
AM[0:16]	Address mask The address mask provides masking on any corresponding bits in the associated base register. By masking the address bits independently, external devices of different size address ranges can be used.	
ATM[0:2]	Address type mask This field can be used to mask certain address type bits, allowing more than one address space type to be assigned to a chip-select.	
CSNT	Chip-select negation time This attribute is used to determine when $\overline{CS}$/$\overline{WE}$ are negated during an external memory write access handled by the GPCM.	0 = $\overline{CS}$/$\overline{WE}$ are negated normally.
ACS[0:1]	Address to chip-select setup It allows the $\overline{CS}$ assertion to be delayed relative to the address change.	11 = $\overline{CS}$ is output half a clock later than the address lines.
$\overline{BI}$	Burst inhibit This attribute determines whether or not this memory bank supports burst accesses.	1 = This bank does not support burst accesses.
SCY[0:3]	Cycle length in clocks	Because an external $\overline{TA}$ response is selected, SCY bits are not used.
SETA	External transfer acknowledge	1 = $\overline{TA}$ is generated by external logic.
TRLX	Timing relaxed This bit, when asserted, modifies the timing of the signals that control the memory devices when the GPCM is selected to handle the memory access initiated to this memory region.	0 = Normal timing is generated by GPCM.
EHTR	Extended hold time on read access. This bit, when asserted, inserts an idle clock cycle after a read access from the current bank and any MPC860.	0 = Normal timing is generated by the memory controller.

1.2 MPC860 to HPI Timing Verification

To verify proper operation, two functions have been examined:

1. an MPC860 write to HPI.
2. an MPC860 read from HPI.

In each instance, timing requirements were compared for each of the devices. The results are shown in the following tables and timing diagrams.

In the following figures and tables, tPLD and tCO represent the propagation time from input to combinatorial output and the propagation time from the clock to output, respectively, for the PALLV22V10.

Note that on a first halfword write, when $\overline{CS}$ becomes valid, $\overline{HRDY}$ indicates that the HPI is busy completing the internal portion of a previous HPI request.

The parameters in Figure 3 through Figure 6 and Table 4 through Table 9 are named in the same way as those in the data sheets listed in the Reference section of this report. Actual timing parameter values are listed in Appendix A and Appendix B.

The tables and timing diagrams show that the timing parameters for both devices are met in the interface of the MPC860 and the HPI. This interface is based on an MPC860/40-MHz device and all TMS320C6x™ HPI devices.

TMS320C6x is a trademark of Texas Instruments.

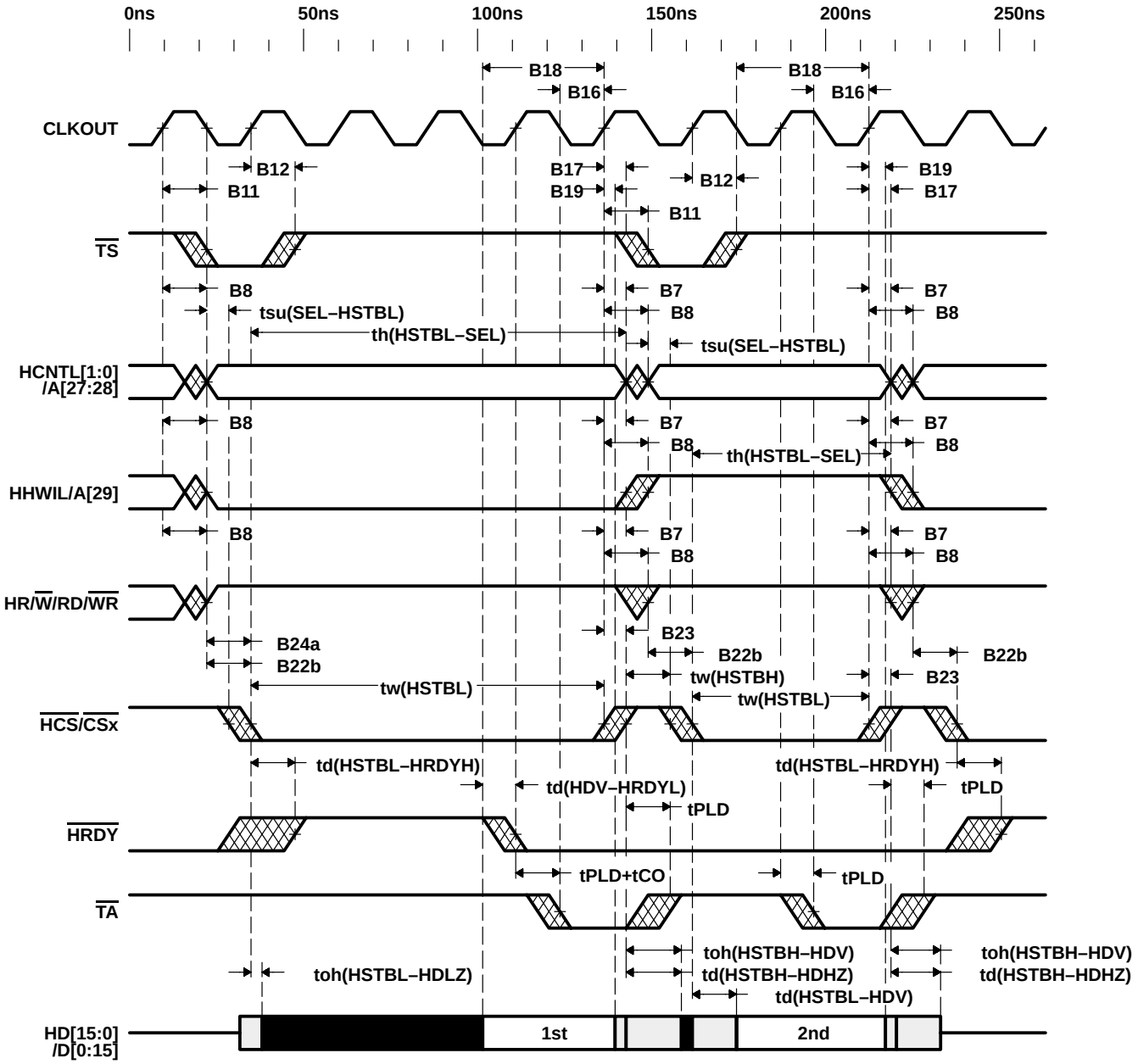


Figure 3. MPC860 Reads Internal Memory of TMS320C62x/C67x/C64x (HPI16 Mode) Using HPI (Read Without Auto-Increment)

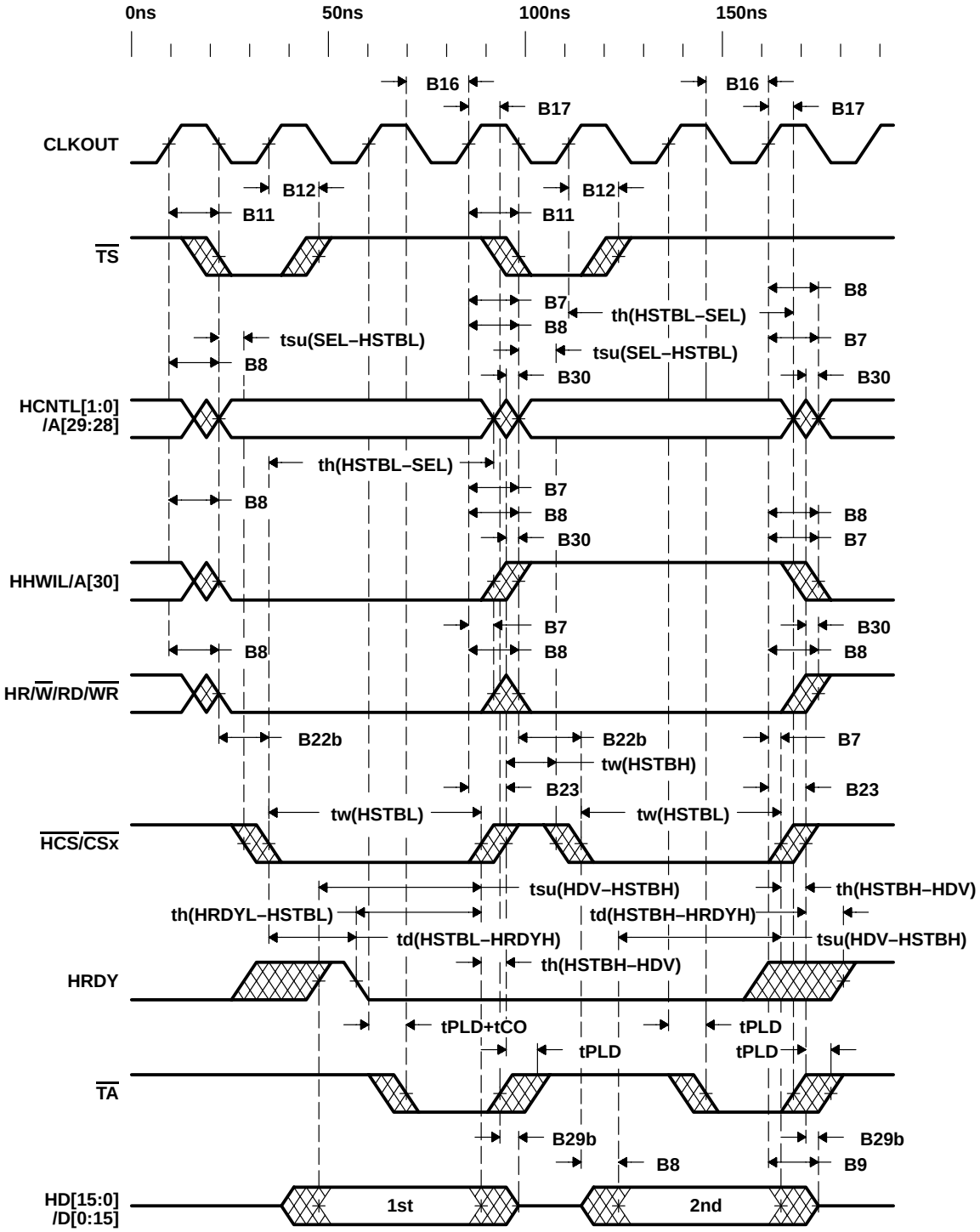


Figure 4. MPC860 Write to TMS320C62x/C67x/C64x (HPI16 Mode) HPI

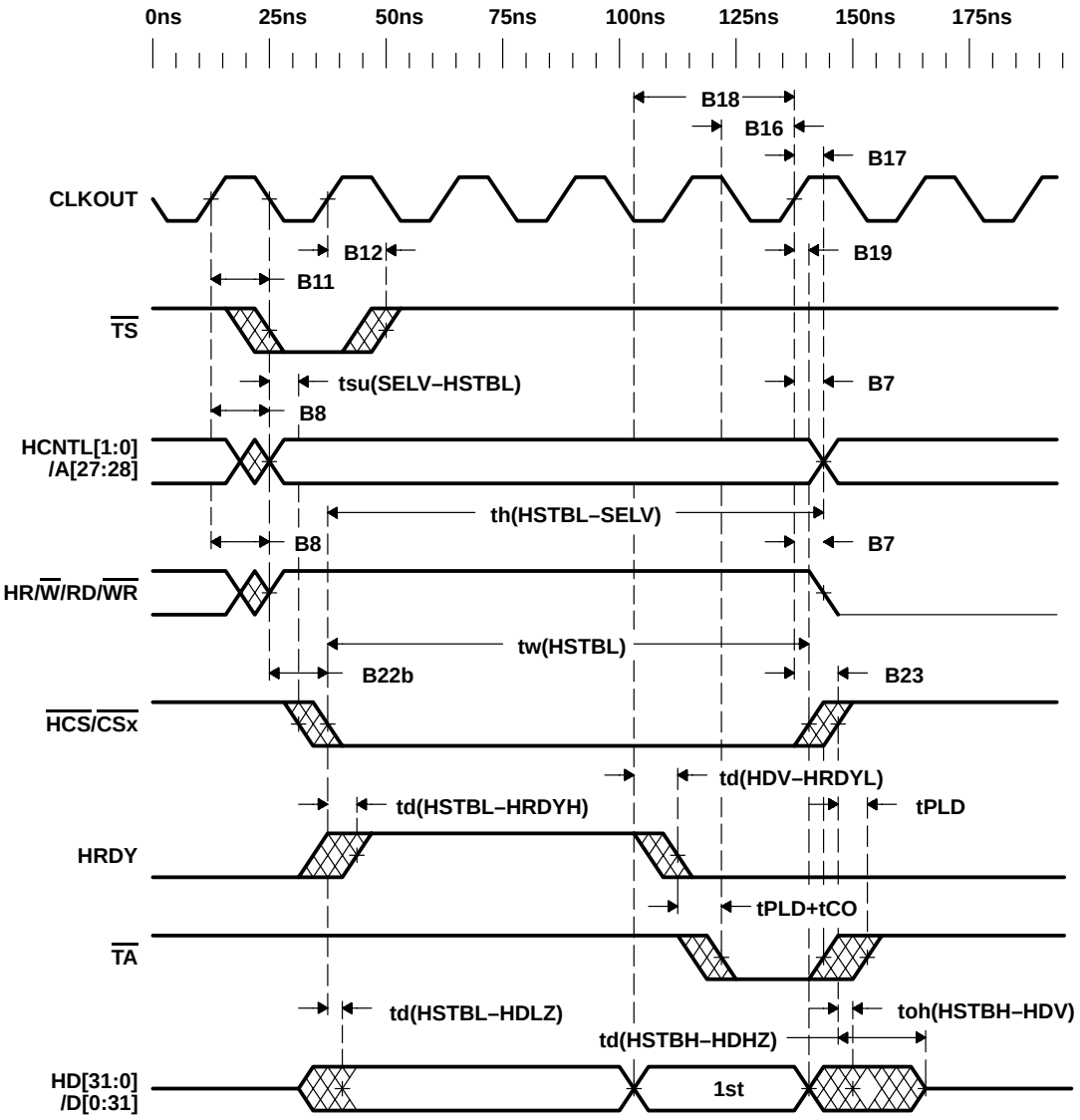


Figure 5. MPC860 Reads Internal Memory of TMS320C64x (HPI32 Mode) Using HPI (Read Without Auto-Increment)

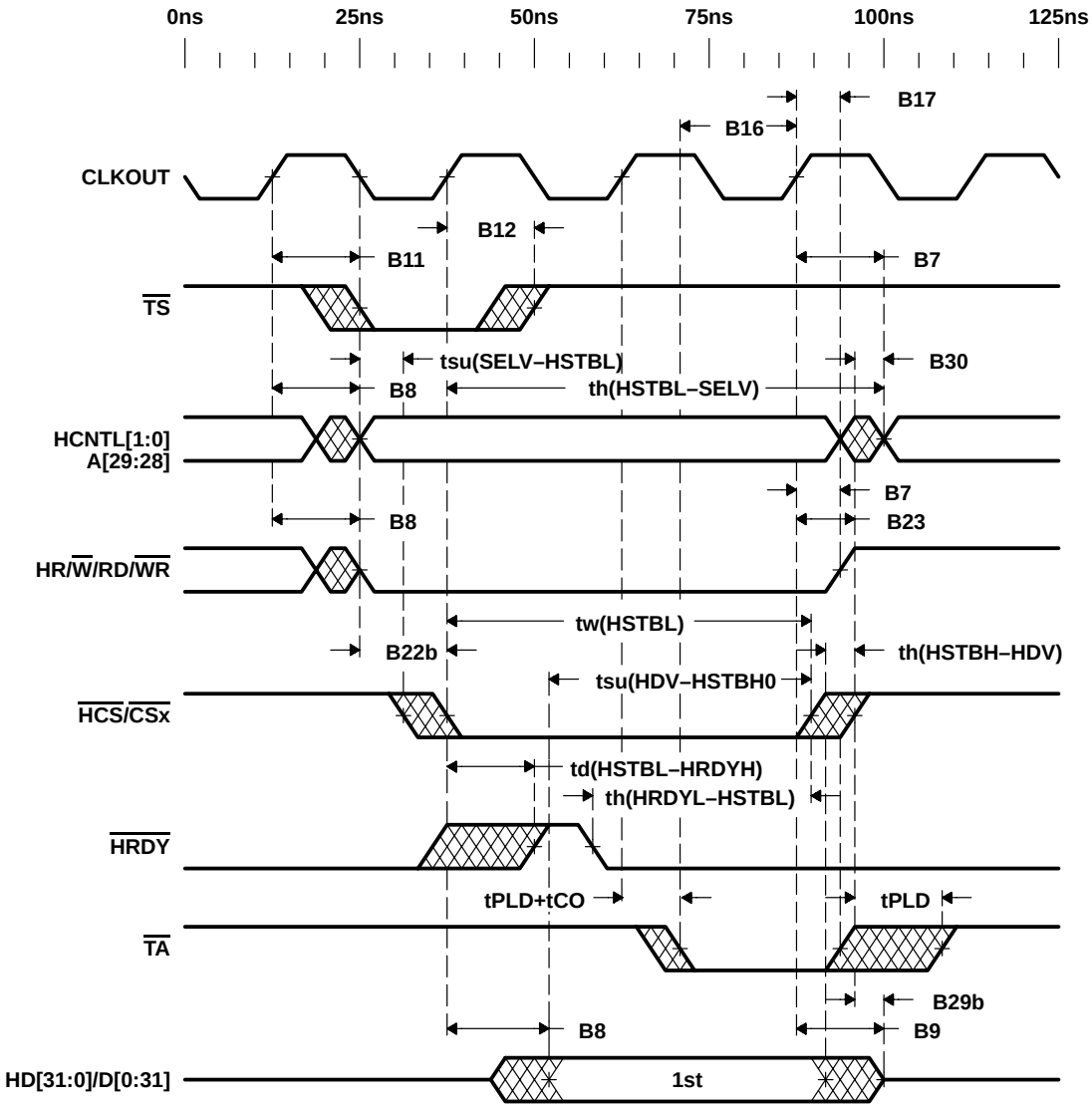


Figure 6. MPC860 Write to TMS320C64x (HPI32 Mode) HPI

Table 4. Timing Requirements for the C6201/C6701 HPI

HPI Symbol	MPC860 Symbol		Min HPI (ns)	Min MPC860 (ns)
$t_{su(SEL-HSTBL)}$	B24a	Setup time, Select signals valid before HSTROBE low	4	10
$t_{h(HSTBL-SEL)}$	$2.5*P_M$ –B22b + B7	Hold time, select signals valid after HSTROBE low	2	55.75
$t_{w(HSTBL)}$	$2.5*P_M$ – B22b +B23	Pulse Duration, HSTROBE low	$2*P_H$=10	51.5
$t_{w(HSTBH)}$	$0.5*P_M$ – B23 + B22b	Pulse Duration, HSTROBE high	$2*P_H$=10	10.75
$t_{su(HDV-HSTBH)}$	$2*P_M$ – B8 + B23	Setup time, host data valid before HSTROBE high	3	39
$t_{h(HSTBH-HDV)}$	B29b	Hold time, host data valid after HSTROBE high	2	4.25
$t_{h(HRDYL-HSTBL)}$	$0.5*P_M$ + B23	Hold time, HSTROBE low after HRDY low	1	14.5

NOTE: P_H = Period of TMS320C6201/C6701 clock = 5 ns at 200 MHz.
P_M = Period of MPC860 clock = 25 ns at 40 MHz.

Table 5. Timing Requirements for MPC860 Interfaced to the C6201/C6701 HPI

HPI Symbol	MPC860 Symbol		Min HPI (ns)	Min MPC860 (ns)
B23 + $t_{h(HSTBH-HDV)}$	B19	Input data hold time from CLKOUT rising edge	4	1
$2.5*P_M$ – B22b – $t_{d(HSTBL-HDV)}$	B18	Data in valid to clock high (read setup time)	37.5	6
P_M – t_{PLD}-t_{CO}	B16	$\overline{TA}$ valid to CLKOUT (setup time)	15	9.75
B23+t_{PLD}	B17	CLKOUT to $\overline{TA}$ valid (hold time)	7	1

NOTE: P_H = Period of TMS320C6201/C6701 clock = 5 ns at 200 MHz.
P_M = Period of MPC860 clock = 25 ns at 40 MHz.

Table 6. Timing Requirements for the C6211/C6711 HPI

HPI Symbol	MPC860 Symbol	Parameter	Min HPI (ns)	Min MPC860 (ns)
$t_{su(SEL-HSTBL)}$	B24a	Setup time, select signals valid before HSTROBE low	5	10
$t_{h(HSTBL-SEL)}$	$2.5P_M$ –B22b + B7	Hold time, select signals valid after HSTROBE low	4	55.75
$t_{w(HSTBL)}$	$2.5P_M$ – B22b + B23	Pulse Duration, HSTROBE low	$4P_H$=24	51.5
$t_{w(HSTBH)}$	$0.5P_M$ – B23 + B22b	Pulse Duration, HSTROBE high	$4P_H$=24	10.75†
$t_{su(HDV-HSTBH)}$	$2P_M$ – B8 + B23	Setup time, host data valid before HSTROBE high	5	39
$t_{h(HSTBH-HDV)}$	B29b	Hold time, host data valid after HSTROBE high	3	4.25
$t_{h(HRDYL-HSTBL)}$	$0.5P_M$ + B23	Hold time, HSTROBE low after HRDY low	2	14.5

† To ensure that $t_{w(HSTBH)}$ is not violated for the C6211/C6711, the MPC860 should insert at least 13.25 ns of time between consecutive accesses to the HPI

NOTE: P_H = Period of TMS320C6211/C6711 clock = 6 ns at 167 MHz.
P_M = Period of MPC860 clock = 25 ns at 40 MHz.

Table 7. Timing Requirements for MPC860 Interfaced to the C6211/C6711 HPI

HPI Symbol	MPC860 Symbol		Min HPI (ns)	Min MPC860 (ns)
B23 + $t_{h(HSTBH-HDV)}$	B19	Input data hold time from CLKOUT rising edge	5	1
2.5*P_M – B22b – $t_{d(HSTBL-HDV)}$	B18	Data in valid to clock high (read setup time)	38.5	6
P_M – t_{PLD}-t_{CO}	B16	$\overline{TA}$ valid to CLKOUT (setup time)	15	9.75
B23+t_{PLD}	B17	CLKOUT to $\overline{TA}$ valid (hold time)	7	1

NOTE: P_H = Period of TMS320C6211/C6711 clock = 6 ns at 167 MHz.
P_M = Period of MPC860 clock = 25 ns at 40 MHz.

Table 8. Timing Requirements for the C64x HPI

HPI Symbol	MPC860 Symbol	Parameter	Min HPI (ns)	Min MPC860 (ns)
$t_{su(SEL-HSTBL)}$	B24a	Setup time, select signals valid before HSTROBE low	5	10
$t_{h(HSTBL-SEL)}$	2.5†P_M –B22b + B7	Hold time, select signals valid after HSTROBE low	2	55.75
$t_{w(HSTBL)}$	2.5†P_M – B22b +B23	Pulse Duration, HSTROBE low	4†P_H=10	51.5
$t_{w(HSTBH)}$	0.5†P_M – B23 + B22b	Pulse Duration, HSTROBE high	4†P_H=10	10.75
$t_{su(HDV-HSTBH)}$	2*P_M – B8 + B23	Setup time, host data valid before HSTROBE high	5	39
$t_{h(HSTBH-HDV)}$	B29b	Hold time, host data valid after HSTROBE high	2	4.25
$t_{h(HRDYL-HSTBL)}$	0.5†P_M + B23	Hold time, HSTROBE low after HRDY low	2	14.5

NOTE: P_H = Period of TMS320C64x DSP clock = 2.5 ns at 400 MHz.
P_M = Period of MPC860 clock = 25 ns at 40 MHz.
NOTE: The timing specifications above are preliminary and the actual numbers may vary with a TMS part. Please refer to the latest data sheet for numbers.

Table 9. Timing Requirements for MPC860 Interfaced to the C64x HPI

HPI Symbol	MPC860 Symbol		Min HPI (ns)	Min MPC860 (ns)
B23 + $t_{h(HSTBH-HDV)}$	B19	Input data hold time from CLKOUT rising edge	5	1
2.5*P_M – B22b – $t_{d(HSTBL-HDV)}$	B18	Data in valid to clock high (read setup time)	41.5	6
P_M – t_{PLD}-t_{CO}	B16	$\overline{TA}$ valid to CLKOUT (setup time)	15	9.75
B23+t_{PLD}	B17	CLKOUT to $\overline{TA}$ valid (hold time)	7	1

NOTE: P_H = Period of TMS320C64x DSP clock = 2.5 ns at 400 MHz.
P_M = Period of MPC860 clock = 25 ns at 40 MHz.
NOTE: The timing specifications above are preliminary and the actual numbers may vary with a TMS part. Please refer to the latest data sheet for numbers.

2 References

1. *TMS320C6000 Peripherals Reference Guide* (SPRU190).
2. *TMS320C6201 Digital Signal Processor* (SPRS051).
3. *TMS320C6701 Floating-Point Digital Signal Processor* (SPRS067).
4. *TMS320C6211, TMS320C6211B Fixed-Point Digital Signal Processors* (SPRS073).
5. *TMS320C6416 Fixed-Point Digital Signal Processor* (SPRS164).
6. MPC860 Data Sheet, Motorola, Inc.
7. MPC860 User's Guide, Motorola, Inc.

Appendix A TMS320C6x Timing Requirements

Table A–1. TMS320C6201/C6701 Host Port Timing Specifications

Symbol	Characteristic	Min (ns)	Max (ns)
$t_{su(SEL-HSTBL)}$	Setup time, select signals§ valid before HSTROBE† low	4	
$t_{h(HSTBL-SEL)}$	Hold time, select signals§ valid after HSTROBE† low	2	
$t_{w(HSTBL)}$	Pulse duration, HSTROBE† low	2P‡	
$t_{w(HSTBH)}$	Pulse duration, HSTROBE† high between consecutive accesses	2P‡	
$t_{su(HDV-HSTBH)}$	Setup time, host data valid before HSTROBE† high	3	
$t_{h(HSTBH-HDV)}$	Hold time, host data valid after HSTROBE† high	2	
$t_{h(HRDYL-HSTBL)}$	Hold time, HSTROBE† low after HRDY low. HSTROBE† should not be inactivated until HRDY is active (low); otherwise, HPI writes will not complete properly.	1	
$t_{d(HCS-HRDY)}$	Delay time, HCS to HRDY¶	1	9
$t_{d(HSTBL-HRDYH)}$	Delay time, HSTROBE† low to HRDY high#	3	12
$t_{oh(HSTBL-HDLZ)}$	Output hold time, HD low impedance after HSTROBE† low for an HPI read	4	
$t_{d(HDV-HRDYL)}$	Delay time, HD valid to HRDY low	P‡ – 3	P‡ + 3
$t_{oh(HSTBH-HDV)}$	Output hold time, HD valid after HSTROBE† high	2	12
$t_{d(HSTBH-HDHZ)}$	Delay time, HSTROBE† high to HD high impedance	3	12
$t_{d(HSTBL-HDV)}$	Delay time, HSTROBE† low to HD valid	3	12
$t_{d(HSTBH-HRDYH)}$	Delay time, HSTROBE† high to HRDY high‖	3	12

† HSTROBE refers to the following logical operation on HCS, HDS1, and HDS2: [NOT(HDS1 XOR HDS2)] OR HCS.
‡ P = 1/CPU clock frequency in ns. For example, when running parts at 200 MHz, use P = 5 ns.
§ § Select signals include: HCNTRL[1:0], HR/W, and HHWIL.
¶ HCS enables HRDY, and HRDY is always low when HCS is high. The case where HRDY goes high when HCS falls indicates that HPI is busy completing a previous HPID write or READ with autoincrement.
# This parameter is used during an HPID read. At the beginning of the first half-word transfer on the falling edge of HSTROBE, the HPI sends the request to the DMA auxiliary channel, and HRDY remains high until the DMA auxiliary channel loads the requested data into HPID.
‖ This parameter is used after the second half-word of an HPID write or autoincrement read. HRDY remains low if the access is not an HPID write or autoincrement read. Reading or writing to HPIC or HPIA does not affect the HRDY signal.

Table A–2. TMS320C6211/C6711 Host Port Timing Specifications

Symbol	Characteristic	Min (ns)	Max (ns)
$t_{su(SELV-HSTBL)}$	Setup time, select signals§ valid before HSTROBE† low	5	
$t_{h(HSTBL-SELV)}$	Hold time, select signals§ valid after HSTROBE† low	4	
$t_{w(HSTBL)}$	Pulse duration, HSTROBE† low	4P‡	
$t_{w(HSTBH)}$	Pulse duration, HSTROBE† high between consecutive accesses	4P‡	
$t_{su(HDV-HSTBH)}$	Setup time, host data valid before HSTROBE† high	5	
$t_{h(HSTBH-HDV)}$	Hold time, host data valid after HSTROBE† high	3	
$t_{h(HRDYL-HSTBL)}$	Hold time, HSTROBE† low after HRDY low. HSTROBE† should not be inactivated until HRDY is active (low); otherwise, HPI writes will not complete properly.	2	
$t_{d(HCS-HRDY)}$	Delay time, HCS to HRDY¶	1	15
$t_{d(HSTBL-HRDYH)}$	Delay time, HSTROBE† low to HRDY high#	3	15
$t_{oh(HSTBL-HDLZ)}$	Output hold time, HD low impedance after HSTROBE† low for an HPI read	2	
$t_{d(HDV-HRDYL)}$	Delay time, HD valid to HRDY low	2P‡ – 4	2P‡
$t_{oh(HSTBH-HDV)}$	Output hold time, HD valid after HSTROBE† high	3	15
$t_{d(HSTBH-HDHZ)}$	Delay time, HSTROBE† high to HD high impedance	3	15
$t_{d(HSTBL-HDV)}$	Delay time, HSTROBE† low to HD valid	3	15
$t_{d(HSTBH-HRDYH)}$	Delay time, HSTROBE† high to HRDY high‖	3	15

† HSTROBE refers to the following logical operation on HCS, HDS1, and HDS2: [NOT(HDS1 XOR HDS2)] OR HCS.
‡ P = 1/CPU clock frequency in ns. For example, when running parts at 167 MHz, use P = 6 ns.
§ § Select signals include: HCNTRL[1:0], HR/W, and HHWIL.
¶ HCS enables HRDY, and HRDY is always low when HCS is high. The case where HRDY goes high when HCS falls indicates that HPI is busy completing a previous HPID write or READ with autoincrement.
# This parameter is used during an HPID read. At the beginning of the first half-word transfer on the falling edge of HSTROBE, the HPI sends the request to the DMA auxiliary channel, and HRDY remains high until the DMA auxiliary channel loads the requested data into HPID.
‖ This parameter is used after the second half-word of an HPID write or autoincrement read. HRDY remains low if the access is not an HPID write or autoincrement read. Reading or writing to HPIC or HPIA does not affect the HRDY signal.

Table A–3. TMS320C64x Host Port Timing Specifications

Symbol	Characteristic	Min (ns)	Max (ns)
$t_{su(SELV-HSTBL)}$	Setup time, select signals§ valid before HSTROBE† low	5	
$t_{h(HSTBL-SELV)}$	Hold time, select signals§ valid after HSTROBE† low	2	
$t_{w(HSTBL)}$	Pulse duration, HSTROBE† low	4P‡	
$t_{w(HSTBH)}$	Pulse duration, HSTROBE† high between consecutive accesses	4P‡	
$t_{su(HDV-HSTBH)}$	Setup time, host data valid before HSTROBE† high	5	
$t_{h(HSTBH-HDV)}$	Hold time, host data valid after HSTROBE† high	2	
$t_{h(HRDYL-HSTBL)}$	Hold time, HSTROBE† low after HRDY low. HSTROBE† should not be inactivated until HRDY is active (low); otherwise, HPI writes will not complete properly.	2	
$t_{d(HCS-HRDY)}$	Delay time, HCS to HRDY¶	1	7
$t_{d(HSTBL-HRDYH)}$	Delay time, HSTROBE† low to HRDY high#	3	12
$t_{oh(HSTBL-HDLZ)}$	Output hold time, HD low impedance after HSTROBE† low for an HPI read	2	
$t_{d(HDV-HRDYL)}$	Delay time, HD valid to HRDY low	2P‡ – 6	
$t_{oh(HSTBH-HDV)}$	Output hold time, HD valid after HSTROBE† high	3	
$t_{d(HSTBH-HDHZ)}$	Delay time, HSTROBE† high to HD high impedance		12
$t_{d(HSTBL-HDV)}$	Delay time, HSTROBE† low to HD valid		12
$t_{d(HSTBH-HRDYH)}$	Delay time, HSTROBE† high to HRDY high‖	3	12

† HSTROBE refers to the following logical operation on HCS, HDS1, and HDS2: [NOT(HDS1 XOR HDS2)] OR HCS.
‡ P = 1/CPU clock frequency in ns. For example, when running parts at 600 MHz, use P = 1.67 ns.
§ Select signals include: HCNTRL[1:0], HR/W, and HHWIL.
¶ HCS enables HRDY, and HRDY is always low when HCS is high. The case where HRDY goes high when HCS falls indicates that HPI is busy completing a previous HPID write or READ with autoincrement.
# This parameter is used during an HPID read. At the beginning of the first half-word transfer on the falling edge of HSTROBE, the HPI sends the request to the DMA auxiliary channel, and HRDY remains high until the DMA auxiliary channel loads the requested data into HPID.
‖ This parameter is used after the second half-word of an HPID write or autoincrement read. HRDY remains low if the access is not an HPID write or autoincrement read. Reading or writing to HPIC or HPIA does not affect the HRDY signal.

The timing requirements in the tables above are provided for quick reference only. For detailed description, notes, and restrictions, please see the data sheets listed in the Reference section of this report.

Appendix B MPC860 Timing Requirements

Table B–1. Motorola MPC860 Timing Parameters

Symbol	Characteristic	Min (ns)	Max (ns)
B7	CLKOUT to A[0:31], RD/$\overline{WR}$,D invalid	6.25	
B8	CLKOUT to A(0:31), RD/$\overline{WR}$,D(0:31),DP(0:3) valid	6.25	13
B9	CLKOUT to A(0:31),RD/$\overline{WR}$,D(0:31) High-Z	6.25	13
B11	CLKOUT to $\overline{TS}$,$\overline{BB}$ assertion	6.25	12.25
B12	CLKOUT to $\overline{TS}$,$\overline{BB}$ negation	6.25	13
B18	Data, DP valid to CLKOUT rising edge (setup time)	6	
B19	CLKOUT rising edge to data, DP valid (hold time)	1	
B22	CLKOUT rising edge to $\overline{CS}$ asserted (GPCM ACS = 00,TRLX = 0)	6.25	13
B22b	CLKOUT rising edge to $\overline{CS}$ asserted (GPCM ACS = 11,TRLX = 0)	6.25	13
B23	CLKOUT rising edge to $\overline{CS}$ negated – $\overline{GPCM}$ read access	2	8
B24a	A(0:31) to $\overline{CS}$ asserted (GPCM ACS = 11, TRLX = 0)	10.5	
B25	CLKOUT rising edge to $\overline{OE}$,$\overline{WE}$(0:3) asserted		9
B26	CLKOUT rising edge to $\overline{OE}$ negated	2	9
B28	CLKOUT rising edge to $\overline{WE(0:3)}$ negated – $\overline{GPCM}$ write access, CSNT = 0		9
B29B	$\overline{CS}$ negated to data Hi-Z (write access) CSNT=0	4.25	
B29	$\overline{WE(0:3)}$ negated to D Hi-Z – $\overline{GPCM}$ write access, CSNT=0	4.25	
B30	$\overline{CS}$,$\overline{WE(0:3)}$ negated to A(0:31) invalid – $\overline{GPCM}$ write access	4.25	
B11A	CLKOUT to $\overline{TA}$,$\overline{BI}$ assertion	2.5	9.25
B12A	CLKOUT to $\overline{TA}$,$\overline{BI}$ negation	2.5	11
B13A	CLKOUT to $\overline{TA}$ $\overline{BI}$ Hi-Z	2.5	15
B7	CLOCKOUT to D[31:0] invalid	6.25	
B16	$\overline{TA}$ valid to CLKOUT (setup time)	9.75	
B17	CLKOUT to $\overline{TA}$ (hold time)	1	

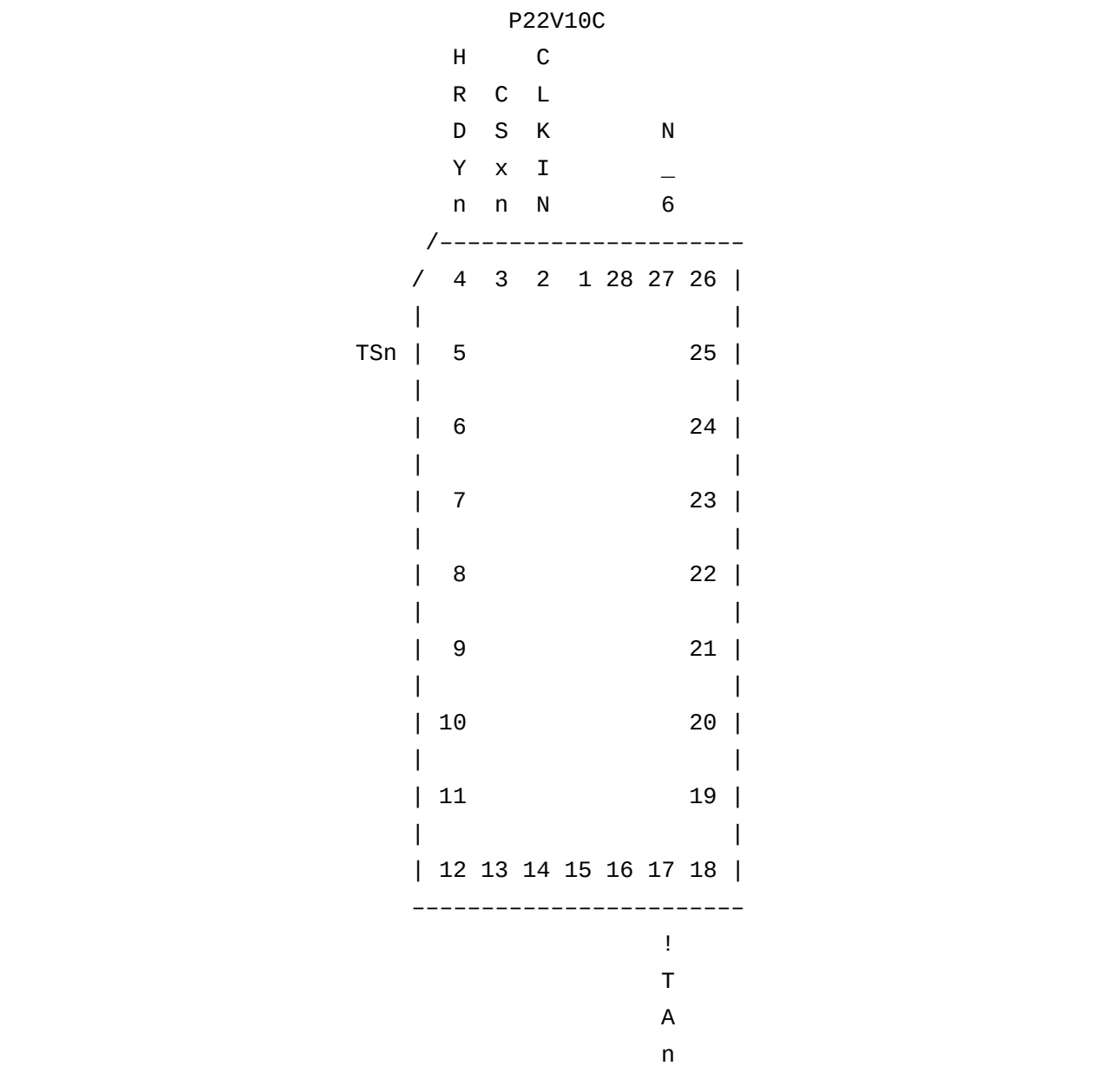
The timing requirements in Table 13 are provided for quick reference only. For detailed description, notes, and restrictions, please visit Motorola's web site at http://www.motorola.com.

Appendix C PAL Equations

```
Synario 3.10  –  Device Utilization Chart         Fri Apr 09 17:42:38 1999
hpi2860.bls
------------------------------------------------------------------------------
Module                    : 'hpi2860'
------------------------------------------------------------------------------
Input files:
    ABEL PLA file         : hpi2860.tt3
    Device library        : P22V10C.dev
Output files:
    Report file           : hpi2860.rep
    Programmer load file  : hpi2860.jed
------------------------------------------------------------------------------
```

```
Synario 3.10  –  Device Utilization Chart         Fri Apr 09 17:42:38 1999
hpi2860.bls
P22V10C Programmed Logic:
--------------------------------------------------------------------------------
TAn     = !(  !N_6.Q & !CSxn );
N_6.D   = (  CSxn
           #   HRDYn
           #   !TSn ); ” ISTYPE ’INVERT’
N_6.C   = (  CLKIN );
```

Synario 3.10 – Device Utilization Chart Fri Apr 09 17:42:38 1999
hpi2860.bls
P22V10C Chip Diagram:



```
Synario 3.10  –  Device Utilization Chart         Fri Apr 09 17:42:38 1999
hpi2860.bls
P22V10C Resource Allocations:
```

Device Resources	Resource Available	Design Requirement	Unused
Input Pins:			
Input:	12	4	8 (66 %)
Output Pins:			
In/Out:	10	2	8 (80 %)
Output:	–	–	–
Buried Nodes:			
Input Reg:	–	–	–
Pin Reg:	10	1	9 (90 %)
Buried Reg:	–	–	–


```
Synario 3.10  –  Device Utilization Chart         Fri Apr 09 17:42:38 1999
hpi2860.bls
P22V10C Product Terms Distribution:
```

Signal Name	Pin Assigned	Terms Used	Terms Max	Terms Unused
TAn	17	1	8	7
N_6.D	27	3	8	5

```
     ==== List of Inputs/Feedbacks ====
```

Signal Name	Pin	Pin Type
CLKIN	2	CLK/IN
CSxn	3	INPUT
HRDYn	4	INPUT
TSn	5	INPUT

Synario 3.10 – Device Utilization Chart Fri Apr 09 17:42:39 1999

hpi2860.bls

P22V10C Unused Resources:

Pin Number	Pin Type	Product Terms	Flip–flop Type
6	INPUT	–	–
7	INPUT	–	–
9	INPUT	–	–
10	INPUT	–	–
11	INPUT	–	–
12	INPUT	–	–
13	INPUT	–	–
16	INPUT	–	–
18	BIDIR	NORMAL 10	D
19	BIDIR	NORMAL 12	D
20	BIDIR	NORMAL 14	D
21	BIDIR	NORMAL 16	D
23	BIDIR	NORMAL 16	D
24	BIDIR	NORMAL 14	D
25	BIDIR	NORMAL 12	D
26	BIDIR	NORMAL 10	D

```
Synario 3.10  –  Device Utilization Chart         Fri Apr 09 17:42:39 1999
hpi2860.bls
P22V10C Fuse Map:
--------------------------------------------------------------------------------
       0          10         20         30         40
   44: ---------- ---------- ---------- ---------- ----
   88: ----X----- ---------- ---------- ---------- ----
  132: --------X- ---------- ---------- ---------- ----
  176: ---------- ---X------ ---------- ---------- ----
 5368: ---------- ---------- ---------- ---------- ----
 5412: --X--X---- ---------- ---------- ---------- ----
       0          10
 5808: XXXXXXXXXX XXXXXXXXX-
```

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