TMS320C6000 Host Port to the i80960 Microprocessors Interface

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ABSTRACT

This application report describes the interface between the Texas Instruments (TI) TMS320C6000™ digital signal processor (DSP) host port and the Intel 80960 microprocessor. The document includes schematics showing connections between the two devices, PAL equations, and verification that timing requirements are met for each device (tables and timing diagrams).

Note:
This application report has not been verified in a board design.

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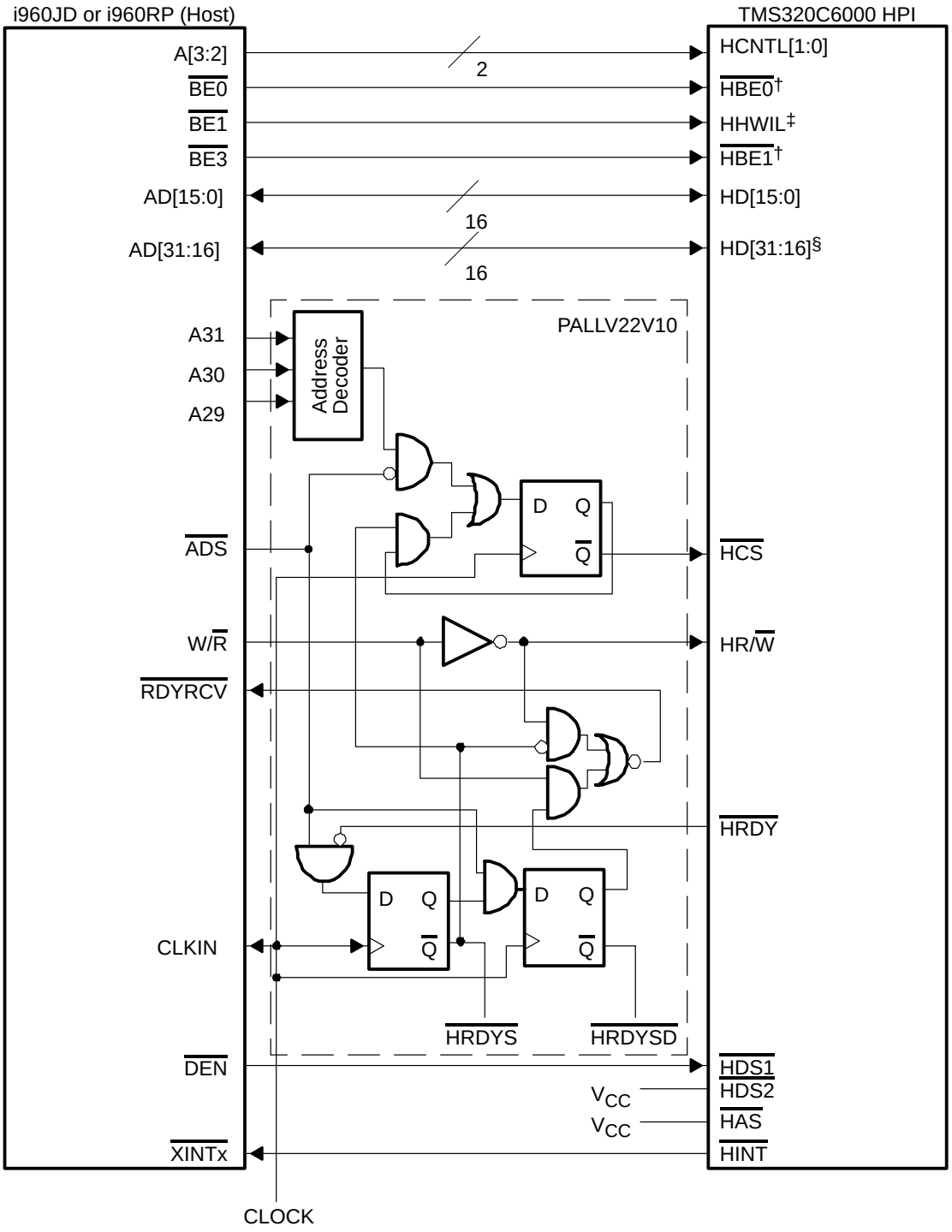
1 Intel 80960Jx/80960Rx Interface

The series of Intel 80960 microprocessor Jx family (JA, JF, and JD) members are differentiated by frequency core speed, operation voltage, and cache size.

- The first proliferation, the 80960JF, utilizes a 4-KB, two-way, set-associative instruction cache and 2-KB, direct-mapped data cache at 5 V and 3 V.
- The Intel 80960 JA has a 2-KB instruction cache and 1-KB data cache at 5 V and 3 V.
- The highest proliferation, the Intel 80960 JD, contains a 4-KB-instruction cache, 2-KB data cache, plus an internal clock doubler.
- The Intel 80960 RP/RD I/O processor incorporates the JF/JD RISC processor core, a PCI-PCI bridge, an I2C interface for system management features, memory controller, two DMA controllers as well as several other peripherals required to meet server performance requirements.

Figure 1 shows a diagram of the host (Intel 80960Jx/Rx) interface to the HPI and Table 2 shows the pin connections.



† C6201/C6701 only
‡ C64x (HPI32 mode) only
§ C62x/C67x/C64x (HPI16 mode) only

Figure 1. Intel 80960Jx (80960Rx) to HPI Interface Block Diagram

Table 1. Intel 80960Jx to HPI Pin Connections

HPI Pin	80960Jx Pin	Comments
HCNTL[1:0]	A[3:2]	Address bits of Intel 80960JD/RP are used as control signals.
HHWIL	$\overline{BE1}$	$\overline{BE1}$ identifies the first or second half-word of transfer. Not used for HPI32 mode transfers.
HR/$\overline{W}$	Inverted W/$\overline{R}$	Indicates a read or write access. Because the TMS320C6000 HPI port has a read-write (HR/$\overline{W}$) line with the opposite polarity of Intel 80960JD/RP's read-write pin, an inverter is used to connect these two lines.
HD[31:0]	AD[31:0]	Data bus. HD[31:16]/AD[31:16] used only for HPI32 mode.
$\overline{HDS1}$	$\overline{DEN}$	$\overline{DEN}$ serves as the data strobe in this configuration.
$\overline{HDS2}$	V_{CC}	See above.Tied high to allow the inputs to $\overline{HDS1}$ and $\overline{HCS}$ control $\overline{HSTROBE}$
$\overline{HAS}$	V_{CC}	Address latch enable is not used in this interface.
$\overline{HCS}$	Address lines A[31:29] are decoded and synchronized using $\overline{ADS}$.	Because the Intel 80960JD/RP does not have a chip-select line, it is necessary to use decode logic as an input to $\overline{HCS}$.
$\overline{HBE0}$	$\overline{BE0}$	HPI uses this value on writes only. This signal is present only on the C6201/C6701.
$\overline{HBE1}$	$\overline{BE3}$	HPI uses this value on writes only. This signal is present only on the C6201/C6701.
$\overline{HRDY}$	$\overline{RDYRCV}$	Asynchronous ready output is synchronized and connected to the $\overline{RDYRCV}$.
$\overline{HINT}$	$\overline{XINTx}$	Any external interrupt can be chosen.

The Intel 80960 local bus is a synchronous interface for burst transactions. However, the Intel 80960 host can perform only non-burst HPI transactions (HPI is an asynchronous interface).

Because the HPI is not 5-V tolerant, the voltage translation is necessary if the Intel 80960 runs at 5 V (voltage translation is not shown in the block diagram).

The HPI is mapped using A[31:29] into one of the 8 memory regions. The selected memory region has to be configured as either 16 or 32 bits wide, depending on the interface.

The interface shown in Figure 1 is not using address latch enable to latch control signals. If ALE is used to latch the HPI control signals (ALE tied to $\overline{HAS}$) there is not enough time to generate and latch the $\overline{HCS}$ signal, because $\overline{HCS}$ must be asserted prior to the falling edge of $\overline{HAS}$. In this interface, $\overline{HAS}$ is tied to V_{CC} and the internal $\overline{HSTROBE}$ signal is generated by asserting $\overline{HCS}$ or $\overline{HDS1}$, whichever comes last ($\overline{HDS1}$ is tied to $\overline{DEN}$). The $\overline{HCS}$ signal is asserted and latched on the rising edge of the CLKIN, if the Intel 80960 initiates the address phase of a data transfer ($\overline{ADS}$ is asserted), and the output from the address decoder is high.

To guarantee that the timing requirement t_h(HSTBH-HDV) is met during an HPI write, the internal HSTROBE is generated differently for read and write cycles. During a read transfer, HSTROBE is asserted on the rising edge of SYSCLK when the address is matched and $\overline{\text{ADS}}$ is low. HSTROBE is negated when synchronized HRDY indicates a ready status. During a write transfer, synchronized HRDY (HRDYS) is used to de-assert HSTROBE, while HRDYS delayed for one clock (HRDYSD) is used to generate the ready signal for the Intel 80960. This way, the Intel 80960 holds the data on the bus and ends the transfer one clock after HSTROBE is negated. This is done to meet the data hold timing requirement of the HPI.

2 Configuration

The only programmable physical memory attribute for the Intel 80960Jx microprocessor is the bus width, which can be 8-, 16-, or 32-bits wide. For the purposes of assigning memory attributes, the physical address space is partitioned into 8 fixed 512-MB regions determined by the upper three address bits. The physical memory attributes for each region are programmable through the PMCON registers. The PMCON registers are loaded from the control table. The Intel 80960Jx microprocessor provides one PMCON register for each region. The bus width for a region is controlled by the BW[1:0] bits in the PMCON register. For a 16-bit interface, BW1 = 0 and BW0 = 1. For a 32-bit interface, BW1 = 1 and BW0 = 0.

All eight PMCON registers are loaded automatically during system auto-initialization. Following a hardware reset, the PMCON register contents are marked invalid in the bus control (BCON) register. The initial PMCON register values are stored in the control table in the initialization boot record. After a hardware reset, the processor first loads all PMCON registers from the control table. The processor then loads BCON from the control table. The BCON.ctv bit in BCON must be set to use the programmed PMCON values for each memory region.

The default logical memory configuration register (DLMCON) provides default logical memory control for those accesses not falling within a region defined by the logical memory control register pairs. On the Intel 80960Jx, the byte order programmed in the DLMCON register controls byte ordering for the entire 32-bit memory space. The DCEN bit field of the DLMCON register must be set to zero to disable data caching. The BE bit field of the DLMCON register must be set to zero to enable little-endian byte order for all accesses.

The interrupt controller register of the Intel 80960Jx processors controls basic functionality, such as interrupt mode, signal detection, global enable/disable, mask operation, interrupt vector caching, and sampling mode (for detailed information on interrupt configuration, please see the *I960 Jx Microprocessor Developer's Manual*).

3 Intel 80960JD to HPI Timing Verification

To verify proper operation, two functions have been examined:

- An Intel 80960JD write to HPI.
- An Intel 80960JD read from HPI.

In each instance, timing requirements were compared for each of the devices and the results are shown in Figure 2 through Figure 5 and Table 2 through Table 7.

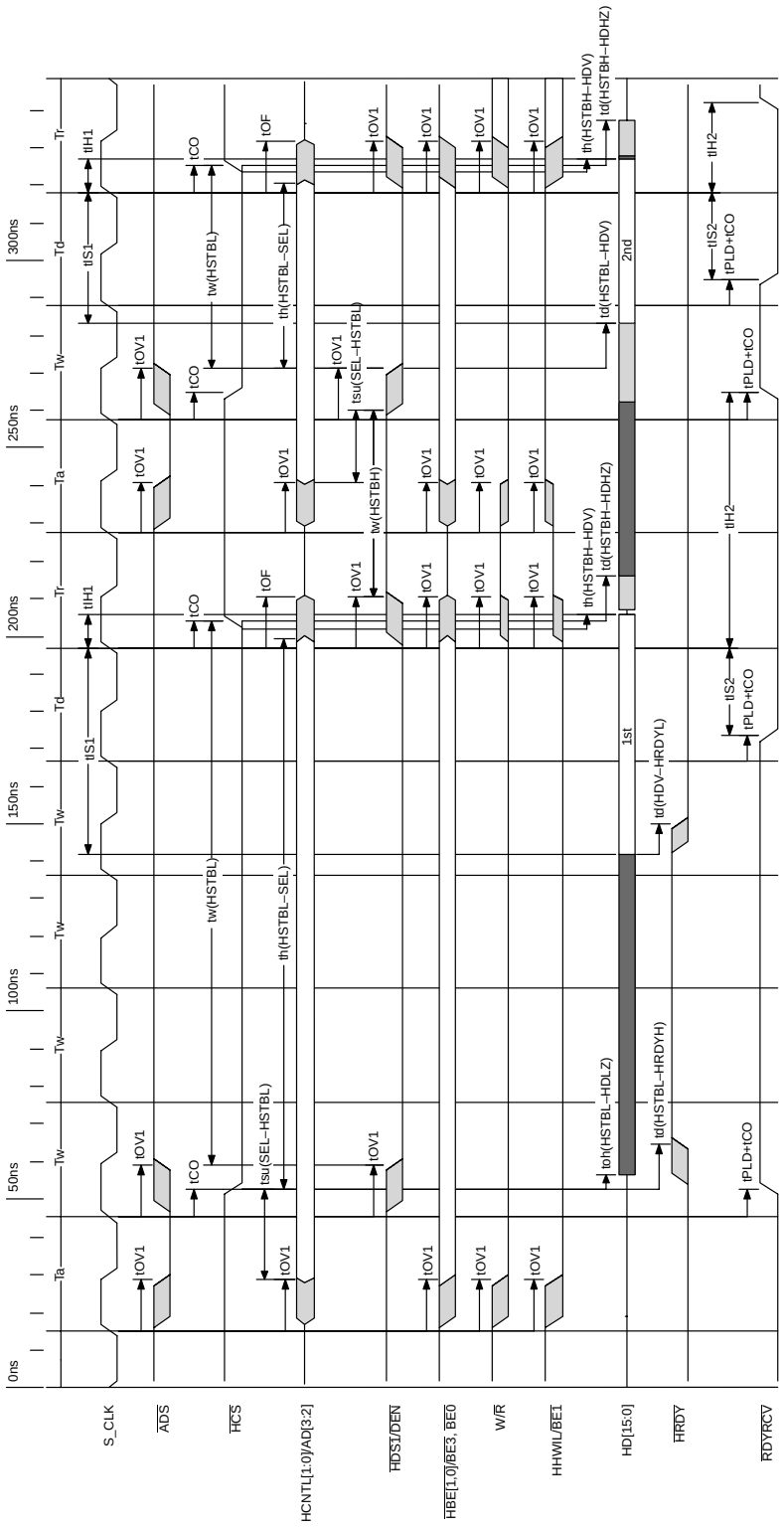


Figure 2. Intel 80960JD Reads Internal Memory of TMS320C62x/C67x/C64x (HPI16) Using HPI

TMS320C62x, C67x, and C64x are trademarks of Texas Instruments.

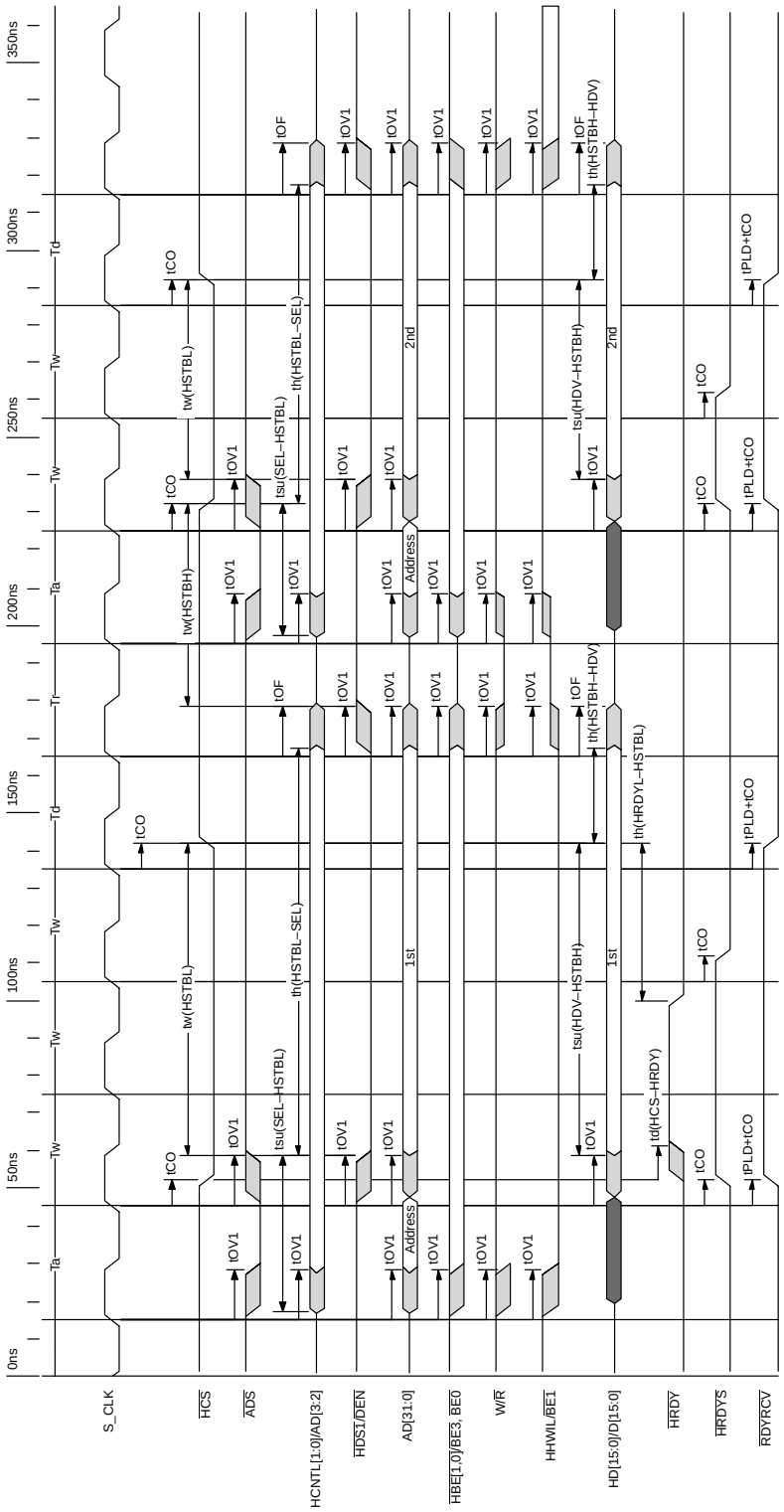


Figure 3. Intel 80960JD Write to TMS320C62x/C67x/C64x (HPI16) HPI

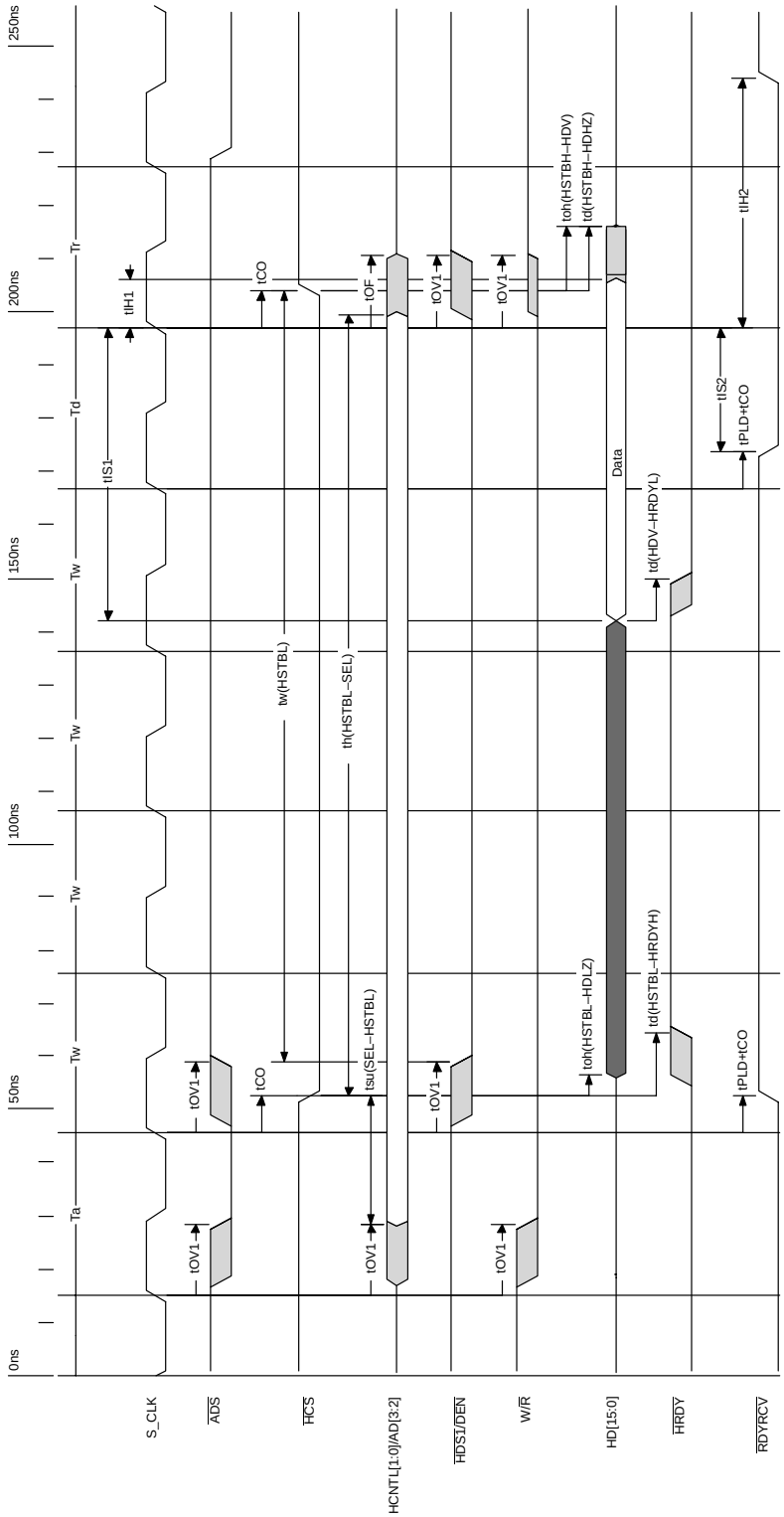


Figure 4. Intel 80960JD Reads Internal Memory of TMS320C64x (HPI16) Using HPI (Read Without Auto-Increment)

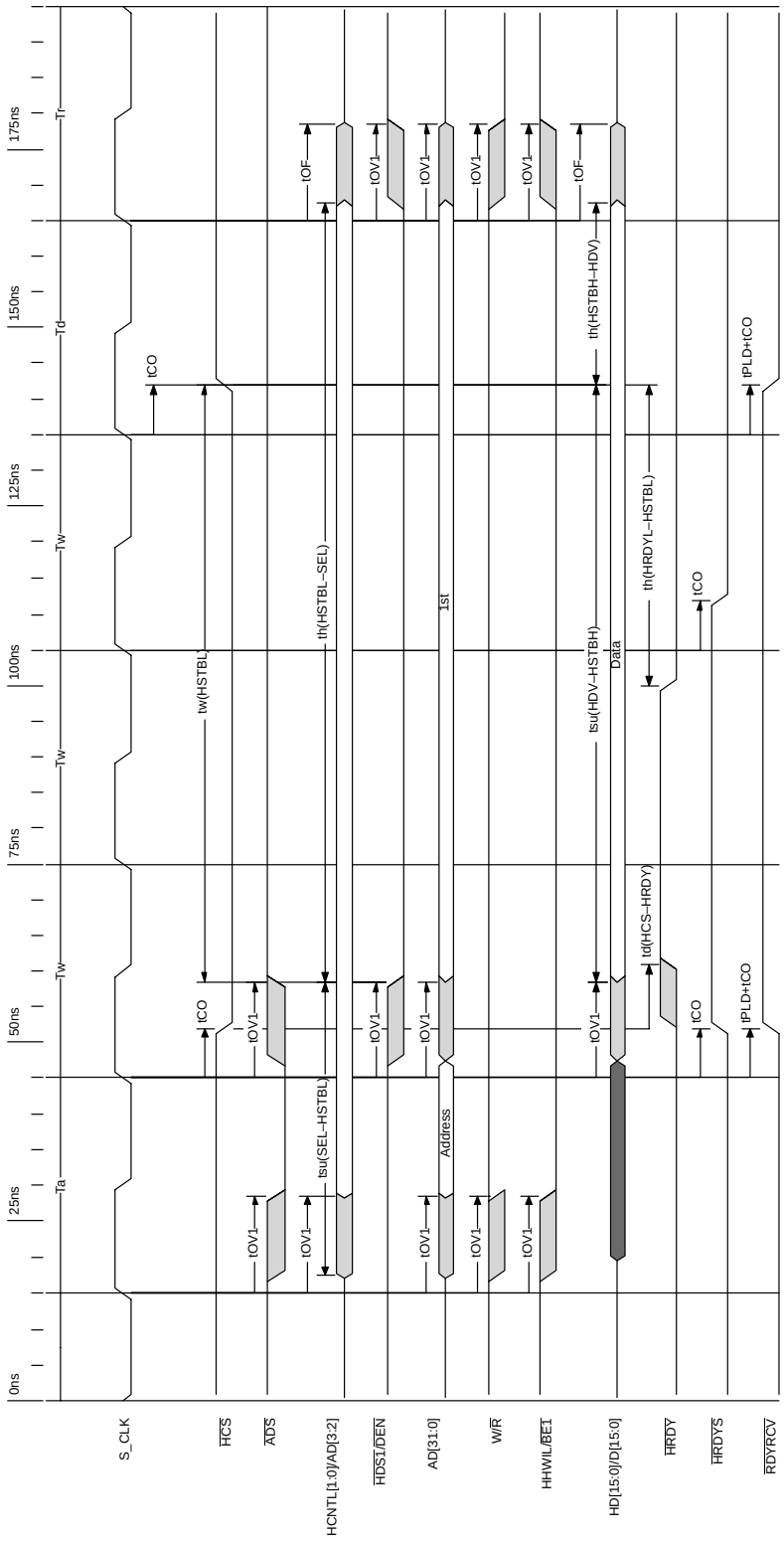


Figure 5. Intel 80690JD Write to TMS320C64x (HPI32) HPI

Table 2. Timing Requirements for TMS320C6201/C6701 HPI

HPI Symbol	80960JD Symbol	Parameter	Min HPI (ns)	Min 80960JD (ns)
t_w(HSTBL)	2tcyc†	Pulse width of $\overline{\text{HDS}}$ low	2*P‡ = 10	60
t_w(HSTBH)	2tcyc† - Max[tOV1] + Min[tOV1]	Pulse width of $\overline{\text{HDS}}$ low	2*P‡ = 10	49
t_{su}(SEL-HSTBL)	tcyc† - Max[tOV1] + Min[tOV1]	Setup time, select signals valid before $\overline{\text{HSTROBE}}$ low	4	19
t_h(HSTBL-SEL)	2tcyc† - Max[tOV1] + Min[tOF]	Setup Hold time, select signals valid before $\overline{\text{HSTROBE}}$ low	2	49
t_{su}(HDV-HSTBH)	2tcyc† - Max[tOV1] + tCO§	Setup time, host data valid before $\overline{\text{HDS}}$ high	3	53.5
t_h(HSTBH-HDV)	tcyc† - tCO§ + Min[tOF]	Hold time, host data valid after $\overline{\text{HDS}}$ high	2	25.5
t_h(HRDYL-HSTBL)	tCO§	Hold time, host data valid after $\overline{\text{HDS}}$ highHold time, $\overline{\text{HSTROBE}}$ low after $\overline{\text{HRDY}}$ valid	1	7

† tcyc denotes one clock cycle time of the 80960JD. At 33-MHz operating frequency, tcyc = 30 ns.
‡ P denotes the TMS320C6x™ CPU period. P = 5 ns @ 200 MHz.
§ tCO denotes PLD propagation.

Table 3. Timing Requirements for 80960JD Interfaced With TMS320C6201/C6701 HPI

HPI Symbol	80960JD Symbol	Parameter	Min HPI (ns)	Min 80960JD (ns)
2tcyc† - tOV1 - t_d(HSTBL-HDV)	tIS1	Input setup to CLKIN - AD[31:0]	34.5	6
tCO‡ + t_{oh}(HSTBH-HDV)	tIH1	Input hold from CLKIN - AD[31:0]	9	1.5
tcyc† - tCO‡ - tPLD	tIS2	Input setup to CLKIN - RDYRCV	23	6.5
2tcyc† + tCO‡ + tPLD	tIH2	Input hold from CLKIN - RDYRCV	67	1

† tcyc denotes one clock cycle time of the 80960JD. At 33-MHz operating frequency, tcyc = 30 ns.
‡ tCO denotes PLD propagation.

Table 4. Timing Requirements for TMS320C6211/C6711 HPI

HPI Symbol	80960JD Symbol	Parameter	Min HPI (ns)	Min 80960JD (ns)
t_w(HSTBL)	2tcyc†	Pulse width of $\overline{\text{HDS}}$ low	4*P‡ = 24	60
t_w(HSTBH)	2tcyc† - Max[tOV1] + Min[tOV1]	Pulse width of $\overline{\text{HDS}}$ low	4*P‡ = 24	49
t_{su}(SELV-HSTBL)	tcyc† - Max[tOV1] + Min[tOV1]	Setup time, select signals valid before $\overline{\text{HSTROBE}}$ low	5	19
t_h(HSTBL-SELV)	2tcyc† - Max[tOV1] + Min[tOF]	Hold time, select signals valid before $\overline{\text{HSTROBE}}$ low	4	49
t_{su}(HDV-HSTBH)	2tcyc† - Max[tOV1] + tCO§	Setup time, host data valid before $\overline{\text{HDS}}$ high	5	53.5
t_h(HSTBH-HDV)	tcyc† - tCO§ + Min[tOF]	Hold time, host data valid after $\overline{\text{HDS}}$ high	3	25.5
t_h(HRDYL-HSTBL)	tCO§	Hold time, $\overline{\text{HSTROBE}}$ low after $\overline{\text{HRDY}}$ valid	2	7

† tcyc denotes one clock cycle time of the 80960JD. At 33-MHz operating frequency, tcyc = 30 ns.
‡ P denotes the TMS320C6x CPU period. P = 6 ns @ 167 MHz.
§ tCO denotes PLD propagation.

Table 5. Timing Requirements for 80960JD Interfaced With TMS320C6211/C6711 HPI

HPI Symbol	80960JD Symbol	Parameter	Min HPI (ns)	Min 80960JD (ns)
2tcyc† - tOV1 - t_d(HSTBL-HDV)	tIS1	Input setup to CLKIN - AD[31:0]	31.5	6
tCO‡ + t_{oh}(HSTBH-HDV)	tIH1	Input hold from CLKIN - AD[31:0]	10	1.5
tcyc† - tCO‡ - tPLD	tIS2	Input setup to CLKIN - RDYRCV	23	6.5
2tcyc† + tCO‡ + tPLD	tIH2	Input hold from CLKIN - RDYRCV	67	1

† tcyc denotes one clock cycle time of the 80960JD. At 33-MHz operating frequency, tcyc = 30 ns.
‡ tCO denotes PLD propagation.

Table 6. Timing Requirements for TMS320C64x HPI

HPI Symbol	80960JD Symbol	Parameter	Min HPI (ns)	Min 80960JD (ns)
t_w(HSTBL)	2tcyc†	Pulse width of $\overline{\text{HDS}}$ low	4*P‡ = 10	60
t_w(HSTBH)	2tcyc† - Max[tOV1] + Min[tOV1]	Pulse width of $\overline{\text{HDS}}$ low	4*P‡ = 10	49
t_{su}(SELV-HSTBL)	tcyc† - Max[tOV1] + Min[tOV1]	Setup time, select signals valid before $\overline{\text{HSTROBE}}$ low	5	19
t_h(HSTBL-SELV)	2tcyc† - Max[tOV1] + Min[tOF]	Hold time, select signals valid before $\overline{\text{HSTROBE}}$ low	2	49
t_{su}(HDV-HSTBH)	2tcyc† - Max[tOV1] + tCO§	Setup time, host data valid before $\overline{\text{HDS}}$ high	5	53.5
t_h(HSTBH-HDV)	tcyc† - tCO§ + Min[tOF]	Hold time, host data valid after $\overline{\text{HDS}}$ high	2	25.5
t_h(HRDYL-HSTBL)	tCO§	Hold time, $\overline{\text{HSTROBE}}$ low after $\overline{\text{HRDY}}$ valid	2	7

† tcyc denotes one clock cycle time of the 80960JD. At 33-MHz operating frequency, tcyc = 30 ns.
‡ P denotes the TMS320C6x CPU period. P = 2.5 ns @ 400 MHz.
§ tCO denotes PLD propagation.
NOTE: The timing specifications above are preliminary and the actual numbers may vary with a TMS part. Please refer to the latest datasheet for numbers.

Table 7. Timing Requirements for 80960JD Interfaced With TMS320C64x HPI

HPI Symbol	80960JD Symbol	Parameter	Min HPI (ns)	Min 80960JD (ns)
2tcyc† - tOV1 - t_d(HSTBL-HDV)	tIS1	Input setup to CLKIN - AD[31:0]	34.5	6
tCO‡ + t_{oh}(HSTBH-HDV)	tIH1	Input hold from CLKIN - AD[31:0]	10	1.5
tcyc† - tCO‡ - tPLD	tIS2	Input setup to CLKIN - RDYRCV	23	6.5
2tcyc† + tCO‡ + tPLD	tIH2	Input hold from CLKIN - RDYRCV	67	1

† tcyc denotes one clock cycle time of the 80960JD. At 33-MHz operating frequency, tcyc = 30 ns.
‡ tCO denotes PLD propagation.
NOTE: The timing specifications above are preliminary and the actual numbers may vary with a TMS part. Please refer to the latest datasheet for numbers.

In Figure 2 through Figure 5 and Table 2 through Table 7, tPLD and tCO represent the propagation time from input to combinatorial output, and propagation time from the clock to output, respectively, for PALLV22V10.

The timing parameters above are named the same as those in the data sheets listed in the *References* on page 16. Actual timing parameter values are listed in the Appendixes.

Figure 2 through Figure 5 and Table 2 through Table 7 above show that the timing parameters for both devices are met in the interface of Intel 80960JD and HPI. This interface is based on an Intel 80960JD/33-MHz device and all TMS320C6x™ HPI devices.

4 Intel 80960RP to HPI Timing Verification

To verify proper operation, two functions have been examined:

- An Intel 80960RP write to HPI
- An Intel 80960RP read from HPI

In each instance, timing requirements were compared for each of the devices and the results are shown in Table 8 through Table 13 (timing diagrams are similar to the ones shown for the Intel 80960JD).

Table 8. Timing Requirements for TMS320C6201/C6701 HPI

HPI Symbol	80960RP Symbol	Parameter	Min HPI (ns)	Min 80960RP (ns)
t_w(HSTBL)	2tcyc†	Pulse width of $\overline{\text{HDS}}$ low	2*P‡ = 10	60
t_w(HSTBH)	2tcyc† - Max[tOV1] + Min[tOV1]	Pulse width of $\overline{\text{HDS}}$ low	2*P‡ = 10	47.5
t_{su}(SEL-HSTBL)	tcyc† - Max[tOV1] + Min[tOV1]	Setup time, select signals valid before $\overline{\text{HSTROBE}}$ low	4	17.5
t_{su}(HSTBL-SEL)	2tcyc† - Max[tOV1] + Min[tOF]	Setup time, select signals valid before $\overline{\text{HSTROBE}}$ low	2	47.5
t_h(HDV-HSTBH)	2tcyc† - Max[tOV1] + tCO§	Hold time, host data valid before $\overline{\text{HDS}}$ high	3	51.5
t_h(HSTBH-HDV)	tcyc† - tCO§ + Min[tOF]	Hold time, host data valid after $\overline{\text{HDS}}$ high	2	26
t_h(HRDYL-HSTBL)	tCO§	Hold time, $\overline{\text{HSTROBE}}$ low after $\overline{\text{HRDY}}$ valid	1	7

† tcyc denotes one clock cycle time of the 80960RP. At 33-MHz operating frequency, tcyc = 30 ns.
‡ P denotes the TMS320C6x CPU period. P = 5 ns @ 200 MHz.
§ tCO denotes PLD propagation.

Table 9. Timing Requirements for 80960RP interfaced with TMS320C6201/C6701 HPI

HPI Symbol	80960RP Symbol	Parameter	Min HPI (ns)	Min 80960RP (ns)
2tcyc† - tOV1 - t_d(HSTBL-HDV)	tIS1	Input setup to CLKIN - AD[31:0]	34.5	5
tCO‡ + t_{oh}(HSTBH-HDV)	tIH1	Input hold from CLKIN - AD[31:0]	9	2
tcyc† - tCO‡ - tPLD	tIS2	Input setup to CLKIN - RDYRCV	23	10
2tcyc† + tCO‡ + tPLD	tIH2	Input hold from CLKIN - RDYRCV	67	2

† tcyc denotes one clock cycle time of the 80960RP. At 33-MHz operating frequency, tcyc = 30 ns.
‡ tCO denotes PLD propagation.

Table 10. Timing Requirements for TMS320C6211/C6711 HPI

HPI Symbol	80960RP Symbol	Parameter	Min HPI (ns)	Min 80960RP (ns)
t_w(HSTBL)	2tcyc†	Pulse width of $\overline{\text{HDS}}$ low	4*P‡ = 24	60
t_w(HSTBH)	2tcyc† - Max[tOV1] + Min[tOV1]	Pulse width of $\overline{\text{HDS}}$ low	4*P‡ = 24	47.5
t_{su}(SELV-HSTBL)	tcyc† - Max[tOV1] + Min[tOV1]	Setup time, select signals valid before $\overline{\text{HSTROBE}}$ low	5	17.5
t_{su}(HSTBL-SEL)	2tcyc† - Max[tOV1] + Min[tOF]	Setup time, select signals valid before $\overline{\text{HSTROBE}}$ low	4	47.5
t_h(HDV-HSTBH)	2tcyc† - Max[tOV1] + tCO§	Hold time, host data valid before $\overline{\text{HDS}}$ high	5	51.5
t_h(HSTBH-HDV)	tcyc† - tCO§ + Min[tOF]	Hold time, host data valid after $\overline{\text{HDS}}$ high	3	26
t_h(HRDYL-HSTBL)	tCO§	Hold time, $\overline{\text{HSTROBE}}$ low after $\overline{\text{HRDY}}$ valid	2	7

† tcyc denotes one clock cycle time of the 80960RP. At 33-MHz operating frequency, tcyc = 30 ns.
‡ P denotes the TMS320C6x CPU period. P = 6 ns @ 167 MHz.
§ tCO denotes PLD propagation.

Table 11. Timing Requirements for 80960RP interfaced with TMS320C6211/C6711 HPI

HPI Symbol	80960RP Symbol	Parameter	Min HPI (ns)	Min 80960RP (ns)
2tcyc† - tOV1 - t_d(HSTBL-HDV)	tIS1	Input setup to CLKIN - AD[31:0]	31.5	5
tCO‡ + t_{oh}(HSTBH-HDV)	tIH1	Input hold from CLKIN - AD[31:0]	10	2
tcyc† - tCO‡ - tPLD	tIS2	Input setup to CLKIN - RDYRCV	23	10
2tcyc† + tCO‡ + tPLD	tIH2	Input hold from CLKIN - RDYRCV	67	2

† tcyc denotes one clock cycle time of the 80960RP. At 33-MHz operating frequency, tcyc = 30 ns.
‡ tCO denotes PLD propagation.

Table 12. Timing Requirements for TMS320C64x HPI

HPI Symbol	80960RP Symbol	Parameter	Min HPI (ns)	Min 80960RP (ns)
t_w(HSTBL)	2tcyc†	Pulse width of $\overline{\text{HDS}}$ low	4*P‡ = 10	60
t_w(HSTBH)	2tcyc† - Max[tOV1] + Min[tOV1]	Pulse width of $\overline{\text{HDS}}$ low	4*P‡ = 10	47.5
t_{su}(SELV-HSTBL)	tcyc† - Max[tOV1] + Min[tOV1]	Setup time, select signals valid before $\overline{\text{HSTROBE}}$ low	5	17.5
t_{su}(HSTBL-SEL)	2tcyc† - Max[tOV1] + Min[tOF]	Setup time, select signals valid before $\overline{\text{HSTROBE}}$ low	2	47.5
t_h(HDV-HSTBH)	2tcyc† - Max[tOV1] + tCO§	Hold time, host data valid before $\overline{\text{HDS}}$ high	5	51.5
t_h(HSTBH-HDV)	tcyc† - tCO§ + Min[tOF]	Hold time, host data valid after $\overline{\text{HDS}}$ high	2	26
t_h(HRDYL-HSTBL)	tCO§	Hold time, $\overline{\text{HSTROBE}}$ low after $\overline{\text{HRDY}}$ valid	2	7

† tcyc denotes one clock cycle time of the 80960RP. At 33-MHz operating frequency, tcyc = 30 ns.
‡ P denotes the TMS320C6x CPU period. P = 2.5 ns @ 400 MHz.
§ tCO denotes PLD propagation.
NOTE: The timing specifications above are preliminary and the actual numbers may vary with a TMS part. Please refer to the latest datasheet for numbers.

Table 13. Timing Requirements for 80960RP interfaced with TMS320C64x HPI

HPI Symbol	80960RP Symbol	Parameter	Min HPI (ns)	Min 80960RP (ns)
2tcyc† - tOV1 - t_d(HSTBL-HDV)	tIS1	Input setup to CLKIN - AD[31:0]	34.5	5
tCO‡ + t_{oh}(HSTBH-HDV)	tIH1	Input hold from CLKIN - AD[31:0]	10	2
tcyc† - tCO‡ - tPLD	tIS2	Input setup to CLKIN - RDYRCV	23	10
2tcyc† + tCO‡ + tPLD	tIH2	Input hold from CLKIN - RDYRCV	67	2

† tcyc denotes one clock cycle time of the 80960RP. At 33-MHz operating frequency, tcyc = 30 ns.
‡ tCO denotes PLD propagation.
NOTE: The timing specifications above are preliminary and the actual numbers may vary with a TMS part. Please refer to the latest datasheet for numbers.

In Table 8 through Table 13 above, tPLD and tCO represent the propagation time from input to combinatorial output, and propagation time from the clock to output respectively for the PALLV22V10.

The timing parameters above are named in the same way as those in the data sheets listed in the *References* section of this report. on page 16. Actual timing parameter values are listed in the Appendixes.

Table 8 through Table 13 above show that the timing parameters for both devices are met in the interface of the Intel 80960RP and HPI. This interface is based on an Intel 80960RP/33-MHz device and all TMS320C6x HPI devices.

5 References

1. *TMS320C6200 Peripherals Reference Guide* (SPRU190).
2. *TMS320C6201 Fixed-Point Digital Signal Processor* (SPRS051).
3. *TMS320C6701 Floating-Point Digital Signal Processor* (SPRS067).
4. *TMS320C6211/TMS320C6211B Fixed-Point Digital Signal Processors, TMS320C6711 Floating-Point Digital Signal Processor* (SPRS073).
5. *TMS320C6416 Fixed-Point Digital Signal Processor* (SPRS164).
6. *80960JD 3.3V Embedded 32-Microprocessor Data Sheet*, Order number 272971, November 1996, Intel Corporation
7. *80960RP/RD I/O Processor at 3.3V Data Sheet*, Order number 273001, January 1997, Intel Corporation.
8. *PALLV22V10 and PALLV22V10Z Families Data Sheet*, Vantis Corporation, http://web.vantis.com/
9. *I960 Jx Microprocessor Developer's Manual*, Order number 272483-002, December 1997, Intel Corporation.

Appendix A TMS320C6x Timing Requirements

The timing requirements in Table A–1 are provided for quick reference only. For detailed description, notes, and restrictions, see the data sheets listed in the *References* section of this report.

Table A–1. TMS320C6x Host Port Timing Specifications

		C6201/C6701		C6211/C6711		C64x	
Characteristic	**Symbol**	**Min (ns)**	**Max (ns)**	**Min (ns)**	**Max (ns)**	**Min (ns)**	**Max (ns)**
Setup time, select signals§ valid before HSTROBE† low	t_{su}(SELV-HSTBL)	4		5		5	
Hold time, select signals§ valid after HSTROBE† low	t_h(HSTBL-SELV)	2		4		2	
Pulse duration, HSTROBE† low	t_w(HSTBL)	2P‡		4P‡		4P‡	
Pulse duration, HSTROBE† high between consecutive accesses	t_w(HSTBH)	2P‡		4P‡		4P‡	
Setup time, host data valid before HSTROBE† high	t_{su}(HDV-HSTBH)	3		5		5	
Hold time, host data valid after HSTROBE† high	t_h(HSTBH-HDV)	2		3		2	
Hold time, HSTROBE† low after HRDY low.	t_h(HRDYL-HSTBL)	1		2		2	
Delay time, HCS to HRDY¶	t_d(HCS-HRDY)	1	9	1	15	1	7
Delay time, HSTROBE† low to HRDY high#	t_d(HSTBL-HRDYH)	3	12	3	15	3	12
Output hold time, HD low impedance after HSTROBE† low for an HPI read	t_{oh}(HSTBL-HDLZ)	4		2		2	
Delay time, HD valid to HRDY low	t_d(HDV-HRDYL)	P‡ – 3	P‡ + 3	2P‡ – 4	2P‡	2P‡ – 6	
Output hold time, HD valid after HSTROBE† high	t_{oh}(HSTBH-HDV)	2	12	3	15	3	
Delay time, HSTROBE† high to HD high impedance	t_d(HSTBH-HDHZ)	3	12	3	15		12
Delay time, HSTROBE† low to HD valid	t_d(HSTBL-HDV)	3	12	3	15		12
Delay time, HSTROBE† high to HRDY high‖	t_d(HSTBH-HRDYH)	3	12	3	15	3	12

† HSTROBE refers to the following logical operation on HCS, HDS1, and HDS2: [NOT(HDS1 XOR HDS2)] OR HCS.
‡ P = 1/CPU clock frequency in ns. For example, when running parts at 200 MHz, use P = 5 ns.
§ Select signals include: HCNTRL[1:0], HR/W, and HHWIL.
¶ HCS enables HRDY, and HRDY is always low when HCS is high. The case where HRDY goes high when HCS falls indicates that HPI is busy completing a previous HPID write or READ with autoincrement.
# This parameter is used during an HPID read. At the beginning of the first half-word transfer on the falling edge of HSTROBE, the HPI sends the request to the DMA auxiliary channel, and HRDY remains high until the DMA auxiliary channel loads the requested data into HPID.
‖ This parameter is used after the second half-word of an HPID write or autoincrement read. HRDY remains low if the access is not an HPID write or autoincrement read. Reading or writing to HPIC or HPIA does not affect the HRDY signal.

Appendix B Intel 80960JD Timing Requirements

The timing requirements in Table B–1 are provided for quick reference only. For detailed description, notes, and restrictions, see the *80960JD 3.3V Embedded 32-Microprocessor* data sheet.

Table B–1. Intel 80960JD Timing Parameters

Characteristic	Symbol	Min (ns)	Max (ns)
Output valid delay, except ALE inactive and DT/$\overline{R}$ for 3.3-V input signals	tOV1	2.5	13.5
Output float delay	tOF	2.5	13.5
Input setup to $\overline{\text{CLKIN}}$ AD[31:0]	tIS1	6	
Input hold from CLKIN AD[31:0]	tIH1	1.5	
Input setup to CLKIN $\overline{\text{RDYRCV}}$	tIS2	6.5	
Input hold from CLKIN $\overline{\text{RDYRCV}}$	tIH2	1	
Address valid to ALE Inactive	tLX	10	
ALE width	tLXL	8	
Address hold from ALE inactive	tLXA	8	
DT/$\overline{R}$ valid to $\overline{\text{DEN}}$ active	tDXD	8	

Appendix C Intel 80960RP Timing Requirements

The timing requirements in Table C–1 are provided for quick reference only. For detailed description, notes, and restrictions, see the *80960RP/RD I/O Processor at 3.3V* data sheet.

Table C–1. Intel 80960RP Timing Parameters

Characteristic	Symbol	Min (ns)	Max (ns)
Output valid delay, except ALE inactive and DT/$\overline{R}$ for 3.3-V input signals	tOV1	3	15.5
Output float delay	tOF	3	13
Input setup to $\overline{CLKIN}$ AD[31:0]	tIS1	5	
Input hold from CLKIN AD[31:0]	tIH1	2	
Input setup to CLKIN $\overline{RDYRCV}$	tIS2	10	
Input hold from CLKIN $\overline{RDYRCV}$	tIH2	2	
ALE width	tLXL	4.5	
Address hold from ALE inactive	tLXA	4.5	
DT/$\overline{R}$ valid to $\overline{DEN}$ active	tDXD	4.5	

Appendix D PAL Equations

```
                                                                        Page 1
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80960_1.bls


--------------------------------------------------------------------------------
Module                    : '80960_1'
--------------------------------------------------------------------------------
Input files:

    ABEL PLA file         : 80960_1.tt3
    Device library        : P22V10C.dev

Output files:

    Report file           : 80960_1.rep
    Programmer load file  : 80960_1.jed
--------------------------------------------------------------------------------


                                                                        Page 2
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P22V10C Programmed Logic:
--------------------------------------------------------------------------------


RDYRCVn     = (   !N_16.Q & WnR
                #   !N_25.Q & !WnR );

N_16.D   = (  N_25.Q & ADSn ); " ISTYPE 'BUFFER'
N_16.C   = (  CLKIN );

N_25.D   = (  ADSn & !HRDY ); " ISTYPE 'BUFFER'
N_25.C   = (  CLKIN );

N_12.D   = (  !N_25.Q & N_12.Q
            #   !ADSn & A29
            #   !ADSn & A30
            #   !ADSn & !A31 ); " ISTYPE 'BUFFER'
N_12.C   = (  CLKIN );

HRnW     = (  !WnR );

HCSn     = (  !N_12.Q );
```

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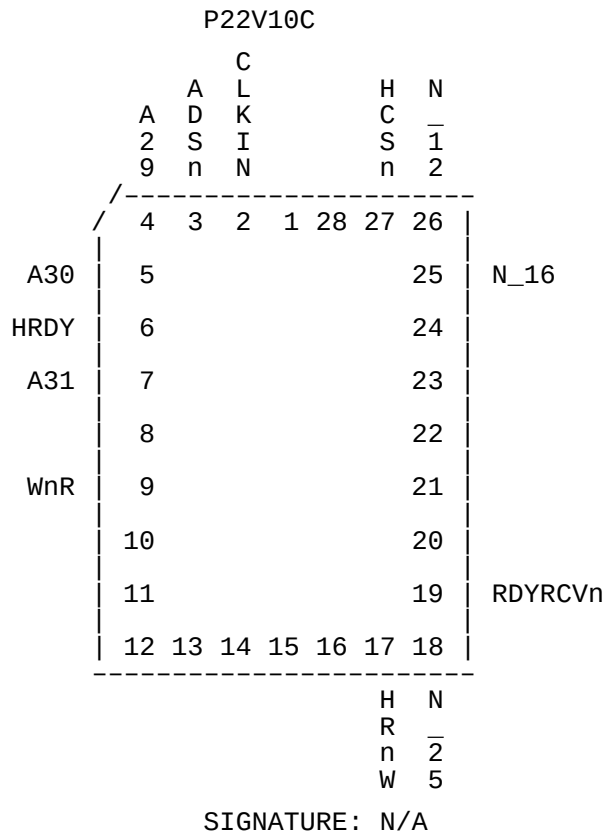
P22V10C Chip Diagram:



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P22V10C Resource Allocations:

Device Resources	Resource Available	Design Requirement	Unused
Input Pins:			
Input:	12	7	5 (41 %)
Output Pins:			
In/Out:	10	6	4 (40 %)
Output:	–	–	–
Buried Nodes:			
Input Reg:	–	–	–
Pin Reg:	10	3	7 (70 %)
Buried Reg:	–	–	–

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P22V10C Product Terms Distribution:

Signal Name	Pin Assigned	Terms Used	Terms Max	Terms Unused
RDYRCVn	19	2	12	10
N_16.D	25	1	12	11
N_25.D	18	1	10	9
N_12.D	26	4	10	6
HRnW	17	1	8	7
HCSn	27	1	8	7

==== List of Inputs/Feedbacks ====

Signal Name	Pin	Pin Type
CLKIN	2	CLK/IN
ADSn	3	INPUT
A29	4	INPUT
A30	5	INPUT
HRDY	6	INPUT
A31	7	INPUT
WnR	9	INPUT

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P22V10C Unused Resources:

Pin Number	Pin Type	Product Terms	Flip-flop Type
10	INPUT	–	–
11	INPUT	–	–
12	INPUT	–	–
13	INPUT	–	–
16	INPUT	–	–
20	BIDIR	NORMAL 14	D
21	BIDIR	NORMAL 16	D
23	BIDIR	NORMAL 16	D
24	BIDIR	NORMAL 14	D

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P22V10C Fuse Map:

```
       0          10         20         30         40
   44: ---------- ---------- ---------- ---------- ----
   88: ------X--- ---------- ---------- ---------- ----
  440: ---------- ---------- ---------- ---------- ----
  484: -------X-- ---------- ---------- ----X----- ----
  528: -----X--X- ---------- ---------- ---------- ----
  572: -----X---- --X------- ---------- ---------- ----
  616: -----X---- ---------- -X-------- ---------- ----
  924: ---------- ---------- ---------- ---------- ----
  968: ----X----- ---------- ---------- -----X---- ----
 4312: ---------- ---------- ---------- ---------- ----
 4356: ---------- X--------- ----X----- ---------- ----
 4400: ---------- ---------- -----X---- ----X----- ----
 4884: ---------- ---------- ---------- ---------- ----
 4928: ----X----- -------X-- ---------- ---------- ----
 5368: ---------- ---------- ---------- ---------- ----
 5412: ---------- ---------- -----X---- ---------- ----
       0          10
 5808: ---X-XXXXX XXXX---X--
```

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