User's Guide

LMK3H2108A18 Register Map

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About This Manual

This document is the configuration summary and register guide specific to the LMK3H2108A18 configuration. For the configuration summaries of the other LMK3H2108xyy configurations, refer to the appropriate configuration addendum on the LMK3H2108 product page.

Fields that are marked as read-only can differ from the default values listed. Reserved fields, DIE_ID_x, and STORED_CRC are subject to change from device to device.

Notational Conventions

This document uses the following conventions.

- Hexadecimal numbers can be shown with the suffix h or the prefix 0x. For example, the following number is 40 hexadecimal (decimal 64): 40h or 0x40.
- Registers in this document are shown in figures and described in tables.
  - Each register figure shows a rectangle divided into fields that represent the fields of the register. Each field is labeled with its bit name, its beginning and ending bit numbers above, and its read/write properties with default reset value below. A legend explains the notation used for the properties.
  - Reserved bits in a register figure can have one of multiple meanings:
    - Not implemented on the device
    - Reserved for future device expansion
    - Reserved for TI testing
    - Reserved configurations of the device that are not supported
  - Writing nondefault values to the Reserved bits could cause unexpected behavior and should be avoided.

Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

Related Documentation

For more information about usage of the LMK3H2108 device, please refer to the LMK3H2104 and LMK3H2108 data sheet.

Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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1 Configuration Overview

1.1 LMK3H2108A18 Configuration Information

Table 1-1. LMK3H2108A18 Frequency Configuration

OTP Page	OUT0 (MHz)	OUT1 (MHz)	OUT2 (MHz)	OUT3 (MHz)	OUT4 (MHz)	OUT5 (MHz)	OUT6 (MHz)	OUT7 (MHz)
OTP Page 0	100	100	100	100	100	100	100	100
OTP Page 1	100	100	100	100	100	100	100	100
OTP Page 2	100	100	100	100	100	100	100	100
OTP Page 3	100	100	100	100	100	100	100	100

Table 1-2. LMK3H2108A18 I2C Configuration

OTP Page	I2C Configuration
OTP Page 0	I2C Address: 0x68 1 Byte Register Addressing
OTP Page 1	I2C Address: 0x68 1 Byte Register Addressing
OTP Page 2	I2C Address: 0x68 1 Byte Register Addressing
OTP Page 3	I2C Address: 0x68 1 Byte Register Addressing

OTP Page 0

Table 1-3. LMK3H2108A18 GPI Settings, OTP Page 0

GPI Pin	Pin Behavior	Polarity	Internal Pull-Down	Internal Pull-Up
GPI0	GPI	Normal	Enabled	Disabled
GPI1	GPI	Normal	Enabled	Disabled
GPI2	GPI	Normal	Enabled	Disabled
GPI3	GPI	Normal	Enabled	Disabled
GPI4	GPI	Normal	Enabled	Disabled
GPI5	GPI	Normal	Enabled	Disabled

Table 1-4. LMK3H2108A18 GPIO Settings, OTP Page 0

GPIO Pin	Pin Behavior	Polarity	Internal Pull-Down	Internal Pull-Up
GPIO0	Dynamic OTP	Normal	Enabled	Disabled
GPIO1	Dynamic OTP	Normal	Enabled	Disabled
GPIO2	GPI	Normal	Enabled	Disabled
GPIO3	Status Output, CLK_READY	Normal	Enabled	Disabled
GPIO4	Global OE	Inverted	Enabled	Disabled

Table 1-5. LMK3H2108A18 Input Settings, OTP Page 0

Input	Powered Up/Down	Input Format	Input Termination
IN_0	Powered Down	N/A (IN0 Unused)	None, DC
IN_1	Powered Down	N/A (IN1 Unused)	None, DC
IN_2	Powered Down	N/A (IN2 Unused)	None, DC

Table 1-6. LMK3H2108A18 Output Settings, OTP Page 0

Output	Frequency (MHz)	Format	Clock Source	Output State	OE Group	SSC Behavior
OUT0	100	85 Ω LP-HCSL	PATH1	Enabled	Global OE Only	Disabled
OUT1	100	85 Ω LP-HCSL	PATH1	Enabled	Global OE Only	Disabled
OUT2	100	85 Ω LP-HCSL	PATH1	Enabled	Global OE Only	Disabled
OUT3	100	85 Ω LP-HCSL	PATH1	Enabled	Global OE Only	Disabled
OUT4	100	85 Ω LP-HCSL	PATH1	Enabled	Global OE Only	Disabled
OUT5	100	85 Ω LP-HCSL	PATH1	Enabled	Global OE Only	Disabled
OUT6	100	85 Ω LP-HCSL	PATH1	Enabled	Global OE Only	Disabled
OUT7	100	85 Ω LP-HCSL	PATH1	Enabled	Global OE Only	Disabled

OTP Page 1

Table 1-7. LMK3H2108A18 GPI Settings, OTP Page 1

GPI Pin	Pin Behavior	Polarity	Internal Pull-Down	Internal Pull-Up
GPI0	GPI	Normal	Enabled	Disabled
GPI1	GPI	Normal	Enabled	Disabled
GPI2	GPI	Normal	Enabled	Disabled
GPI3	GPI	Normal	Enabled	Disabled
GPI4	GPI	Normal	Enabled	Disabled
GPI5	GPI	Normal	Enabled	Disabled

Table 1-8. LMK3H2108A18 GPIO Settings, OTP Page 1

GPIO Pin	Pin Behavior	Polarity	Internal Pull-Down	Internal Pull-Up
GPIO0	Dynamic OTP	Normal	Enabled	Disabled
GPIO1	Dynamic OTP	Normal	Enabled	Disabled
GPIO2	GPI	Normal	Enabled	Disabled
GPIO3	Status Output, CLK_READY	Normal	Enabled	Disabled
GPIO4	Global OE	Inverted	Enabled	Disabled

Table 1-9. LMK3H2108A18 Input Settings, OTP Page 1

Input	Powered Up/Down	Input Format	Input Termination
IN_0	Powered Down	N/A (IN0 Unused)	None, DC
IN_1	Powered Down	N/A (IN1 Unused)	None, DC
IN_2	Powered Down	N/A (IN2 Unused)	None, DC

Table 1-10. LMK3H2108A18 Output Settings, OTP Page 1

Output	Frequency (MHz)	Format	Clock Source	Output State	OE Group	SSC Behavior
OUT0	100	85 Ω LP-HCSL	PATH1	Enabled	Global OE Only	Enabled, -0.25% Down-spread
OUT1	100	85 Ω LP-HCSL	PATH1	Enabled	Global OE Only	Enabled, -0.25% Down-spread
OUT2	100	85 Ω LP-HCSL	PATH1	Enabled	Global OE Only	Enabled, -0.25% Down-spread
OUT3	100	85 Ω LP-HCSL	PATH1	Enabled	Global OE Only	Enabled, -0.25% Down-spread
OUT4	100	85 Ω LP-HCSL	PATH1	Enabled	Global OE Only	Enabled, -0.25% Down-spread
OUT5	100	85 Ω LP-HCSL	PATH1	Enabled	Global OE Only	Enabled, -0.25% Down-spread
OUT6	100	85 Ω LP-HCSL	PATH1	Enabled	Global OE Only	Enabled, -0.25% Down-spread
OUT7	100	85 Ω LP-HCSL	PATH1	Enabled	Global OE Only	Enabled, -0.25% Down-spread

OTP Page 2

Table 1-11. LMK3H2108A18 GPI Settings, OTP Page 2

GPI Pin	Pin Behavior	Polarity	Internal Pull-Down	Internal Pull-Up
GPI0	GPI	Normal	Enabled	Disabled
GPI1	GPI	Normal	Enabled	Disabled
GPI2	GPI	Normal	Enabled	Disabled
GPI3	GPI	Normal	Enabled	Disabled
GPI4	GPI	Normal	Enabled	Disabled
GPI5	GPI	Normal	Enabled	Disabled

Table 1-12. LMK3H2108A18 GPIO Settings, OTP Page 2

GPIO Pin	Pin Behavior	Polarity	Internal Pull-Down	Internal Pull-Up
GPIO0	Dynamic OTP	Normal	Enabled	Disabled
GPIO1	Dynamic OTP	Normal	Enabled	Disabled
GPIO2	GPI	Normal	Enabled	Disabled
GPIO3	Status Output, CLK_READY	Normal	Enabled	Disabled
GPIO4	Global OE	Inverted	Enabled	Disabled

Table 1-13. LMK3H2108A18 Input Settings, OTP Page 2

Input	Powered Up/Down	Input Format	Input Termination
IN_0	Powered Down	N/A (IN0 Unused)	None, DC
IN_1	Powered Down	N/A (IN1 Unused)	None, DC
IN_2	Powered Down	N/A (IN2 Unused)	None, DC

Table 1-14. LMK3H2108A18 Output Settings, OTP Page 2

Output	Frequency (MHz)	Format	Clock Source	Output State	OE Group	SSC Behavior
OUT0	100	85 Ω LP-HCSL	PATH1	Enabled	Global OE Only	Enabled, -0.3% Down-spread
OUT1	100	85 Ω LP-HCSL	PATH1	Enabled	Global OE Only	Enabled, -0.3% Down-spread
OUT2	100	85 Ω LP-HCSL	PATH1	Enabled	Global OE Only	Enabled, -0.3% Down-spread
OUT3	100	85 Ω LP-HCSL	PATH1	Enabled	Global OE Only	Enabled, -0.3% Down-spread
OUT4	100	85 Ω LP-HCSL	PATH1	Enabled	Global OE Only	Enabled, -0.3% Down-spread
OUT5	100	85 Ω LP-HCSL	PATH1	Enabled	Global OE Only	Enabled, -0.3% Down-spread
OUT6	100	85 Ω LP-HCSL	PATH1	Enabled	Global OE Only	Enabled, -0.3% Down-spread
OUT7	100	85 Ω LP-HCSL	PATH1	Enabled	Global OE Only	Enabled, -0.3% Down-spread

OTP Page 3

Table 1-15. LMK3H2108A18 GPI Settings, OTP Page 3

GPI Pin	Pin Behavior	Polarity	Internal Pull-Down	Internal Pull-Up
GPI0	GPI	Normal	Enabled	Disabled
GPI1	GPI	Normal	Enabled	Disabled
GPI2	GPI	Normal	Enabled	Disabled
GPI3	GPI	Normal	Enabled	Disabled
GPI4	GPI	Normal	Enabled	Disabled
GPI5	GPI	Normal	Enabled	Disabled

Table 1-16. LMK3H2108A18 GPIO Settings, OTP Page 3

GPIO Pin	Pin Behavior	Polarity	Internal Pull-Down	Internal Pull-Up
GPIO0	Dynamic OTP	Normal	Enabled	Disabled
GPIO1	Dynamic OTP	Normal	Enabled	Disabled
GPIO2	GPI	Normal	Enabled	Disabled
GPIO3	Status Output, CLK_READY	Normal	Enabled	Disabled
GPIO4	Global OE	Inverted	Enabled	Disabled

Table 1-17. LMK3H2108A18 Input Settings, OTP Page 3

Input	Powered Up/Down	Input Format	Input Termination
IN_0	Powered Down	N/A (IN0 Unused)	None, DC
IN_1	Powered Down	N/A (IN1 Unused)	None, DC
IN_2	Powered Down	N/A (IN2 Unused)	None, DC

Table 1-18. LMK3H2108A18 Output Settings, OTP Page 3

Output	Frequency (MHz)	Format	Clock Source	Output State	OE Group	SSC Behavior
OUT0	100	85 Ω LP-HCSL	PATH1	Enabled	Global OE Only	Enabled, -0.5% Down-spread
OUT1	100	85 Ω LP-HCSL	PATH1	Enabled	Global OE Only	Enabled, -0.5% Down-spread
OUT2	100	85 Ω LP-HCSL	PATH1	Enabled	Global OE Only	Enabled, -0.5% Down-spread
OUT3	100	85 Ω LP-HCSL	PATH1	Enabled	Global OE Only	Enabled, -0.5% Down-spread
OUT4	100	85 Ω LP-HCSL	PATH1	Enabled	Global OE Only	Enabled, -0.5% Down-spread
OUT5	100	85 Ω LP-HCSL	PATH1	Enabled	Global OE Only	Enabled, -0.5% Down-spread
OUT6	100	85 Ω LP-HCSL	PATH1	Enabled	Global OE Only	Enabled, -0.5% Down-spread
OUT7	100	85 Ω LP-HCSL	PATH1	Enabled	Global OE Only	Enabled, -0.5% Down-spread

2 Device Register Map

Table 2-1 lists the memory-mapped registers for the Device registers. All register offset addresses not listed in Table 2-1 should be considered as reserved locations and the register contents should not be modified.

Table 2-1. Register Map

Offset (Hex)	Register Acronym	Bit							
		7	6	5	4	3	2	1	0
0h	R0	VENDOR_ID[7:0]							
1h	R1	VENDOR_ID[15:8]							
2h	R2	FLOAT_VDDO_6	FLOAT_VDDO_5	FLOAT_VDDO_3_4	FLOAT_VDDO_1_2	FLOAT_VDDO_0	FLOAT_VDDR	FLOAT_VDDX	OTP_BURNT
3h	R3	RES	GPIO1_PU_RB		GPIO0_PU_RB		RES		FLOAT_VDDO_7
4h	R4	RES						GPIO2_PU_RB	
5h	R5	RES					OTP_PAGE_SEL_DYN_DEBOUNCE	RES	
6h	R6	I2C_REG_ADDR_FMT	I2C_TRGT_ADDR						
8h	R8	PWRGD_SAMPLE_TMR							
9h	R9	RES	SUP_LVL_RAMP_TMR						PWRGD_SAMPLE_TMR_EN
Ah	R10	GLOBAL_SUP_DET_TMR							
Bh	R11	FOD0_PD	BAW_PD	AUTO_FOD_PD_EN	CRC_IGNORE	PIN_RESAMPLE_DIS	OTP_AUTOLOAD_DIS	PDN	GLOBAL_SUP_DET_TMR_EN
Ch	R12	RES				IN2_PD	IN1_PD	IN0_PD	FOD1_PD
Dh	R13	PWRGD_PWRDN_PIN_SEL				RES			
Eh	R14	RES			GPI0_FUNC				
Fh	R15	RES			GPI1_FUNC				
10h	R16	RES			GPI2_FUNC				
11h	R17	RES			OE_GLOBAL	RES			
12h	R18	RES			GPI3_FUNC				
13h	R19	RES			GPI4_FUNC				
14h	R20	RES			GPI5_FUNC				
15h	R21	RES			GPIO0_FUNC				
16h	R22	RES			GPIO1_FUNC				
17h	R23	RES			GPIO2_FUNC				
18h	R24	RES			GPIO3_FUNC				
19h	R25	RES			GPIO4_FUNC				
1Ah	R26	GPIO1_OUT_SRC_SEL				GPIO0_OUT_SRC_SEL			
1Bh	R27	GPIO3_OUT_SRC_SEL				GPIO2_OUT_SRC_SEL			
1Ch	R28	GPI3_POLARITY	GPI2_POLARITY	GPI1_POLARITY	GPI0_POLARITY	GPIO4_OUT_SRC_SEL			
1Dh	R29	GPI0_PULL_DN_EN	GPIO4_POLARITY	GPIO3_POLARITY	GPIO2_POLARITY	GPIO1_POLARITY	GPIO0_POLARITY	GPI5_POLARITY	GPI4_POLARITY
1Eh	R30	GPI3_PULL_DN_EN	RES		GPI2_PULL_UP_EN	GPI2_PULL_DN_EN	GPI1_PULL_UP_EN	GPI1_PULL_DN_EN	GPI0_PULL_UP_EN
1Fh	R31	GPIO1_PULL_DN_EN	GPIO0_PULL_UP_EN	GPIO0_PULL_DN_EN	GPI5_PULL_UP_EN	GPI5_PULL_DN_EN	GPI4_PULL_UP_EN	GPI4_PULL_DN_EN	GPI3_PULL_UP_EN
20h	R32	GPIO0_NUM_IN_LVL	GPIO4_PULL_UP_EN	GPIO4_PULL_DN_EN	GPIO3_PULL_UP_EN	GPIO3_PULL_DN_EN	GPIO2_PULL_UP_EN	GPIO2_PULL_DN_EN	GPIO1_PULL_UP_EN

Table 2-1. Register Map (continued)

Offset (Hex)	Register Acronym	Bit							
		7	6	5	4	3	2	1	0
21h	R33	GPI3_LIVE_RB	GPI2_LIVE_RB	GPI1_LIVE_RB	GPI0_LIVE_RB	RES		GPIO2_NUM_IN_LVL	GPIO1_NUM_IN_LVL
22h	R34	GPIO2_LIVE_RB		GPIO1_LIVE_RB		GPIO0_LIVE_RB		GPI5_LIVE_RB	GPI4_LIVE_RB
23h	R35	RES	GPIO4_GPO_VAL	GPIO3_GPO_VAL	GPIO2_GPO_VAL	GPIO1_GPO_VAL	GPIO0_GPO_VAL	GPIO4_LIVE_RB	GPIO3_LIVE_RB
24h	R36	RES		GPI1_OE_GRP_SEL			GPI0_OE_GRP_SEL		
25h	R37	RES		GPI3_OE_GRP_SEL			GPI2_OE_GRP_SEL		
26h	R38	RES		GPI5_OE_GRP_SEL			GPI4_OE_GRP_SEL		
27h	R39	RES		GPIO1_OE_GRP_SEL			GPIO0_OE_GRP_SEL		
28h	R40	RES		GPIO3_OE_GRP_SEL			GPIO2_OE_GRP_SEL		
29h	R41	GPIO4_OUT_SIG_TYPE	GPIO3_OUT_SIG_TYPE	GPIO2_OUT_SIG_TYPE	GPIO1_OUT_SIG_TYPE	GPIO0_OUT_SIG_TYPE	GPIO4_OE_GRP_SEL		
2Ah	R42	RES		IN2_RCVR_FMT		IN1_RCVR_FMT		IN0_RCVR_FMT	
2Bh	R43	RES		IN1_TERMINATION_SEL			IN0_TERMINATION_SEL		
2Ch	R44	IN1_LOS_THRESH	IN0_LOS_THRESH	IN2_LOS_EN	IN1_LOS_EN	IN0_LOS_EN	IN2_TERMINATION_SEL		
2Dh	R45	PERST_BUF_IN0_STS	PERST_BUF_IN2		PERST_BUF_IN1		PERST_BUF_IN0		IN2_LOS_THRESH
2Eh	R46	RES			PERST_BUF_IN2_LOS_EN	PERST_BUF_IN1_LOS_EN	PERST_BUF_IN0_LOS_EN	PERST_BUF_IN2_STS	PERST_BUF_IN1_STS
2Fh	R47	RES	FOD0_N_DIV						
30h	R48	RES	FOD1_N_DIV						
31h	R49	FOD0_NUM[7:0]							
32h	R50	FOD0_NUM[15:8]							
33h	R51	FOD0_NUM[23:16]							
34h	R52	FOD1_NUM[7:0]							
35h	R53	FOD1_NUM[15:8]							
36h	R54	FOD1_NUM[23:16]							
37h	R55	FOD1_CFG_UPDATE	FOD0_CFG_UPDATE	PATH1_DIV			PATH0_DIV		
39h	R57	RES	FOD_PH_OFFSET_N_DIV						
3Ah	R58	FOD_PH_OFFSET_NUM[7:0]							
3Bh	R59	FOD_PH_OFFSET_NUM[15:8]							
3Ch	R60	RES	FOD0_SSC_CONFIG_SEL			FOD0_SSC_MOD_TYPE	FOD0_SSC_EN	FOD_PH_OFFSET_FOD_SEL	FOD_PH_OFFSET_SHIFT_NOW
3Dh	R61	FOD0_SSC_STEPS[7:0]							
3Eh	R62	RES			FOD0_SSC_STEPS[12:8]				
3Fh	R63	FOD0_DCO_STEP_SIZE[7:0]							
40h	R64	FOD0_DCO_STEP_SIZE[15:8]							
41h	R65	RES			FOD1_SSC_CONFIG_SEL			FOD1_SSC_MOD_TYPE	FOD1_SSC_EN
42h	R66	FOD1_SSC_STEPS[7:0]							
43h	R67	RES			FOD1_SSC_STEPS[12:8]				
44h	R68	FOD1_DCO_STEP_SIZE[7:0]							
45h	R69	FOD1_DCO_STEP_SIZE[15:8]							

Table 2-1. Register Map (continued)

Offset (Hex)	Register Acronym	Bit							
		7	6	5	4	3	2	1	0
46h	R70	RES		FOD1_DCO_DEC	FOD1_DCO_INC	FOD1_DCO_EN	FOD0_DCO_DEC	FOD0_DCO_INC	FOD0_DCO_EN
47h	R71	FOD0_DCO_STEPS_STAT[7:0]							
48h	R72	FOD0_DCO_STEPS_STAT[15:8]							
49h	R73	FOD1_DCO_STEPS_STAT[7:0]							
4Ah	R74	FOD1_DCO_STEPS_STAT[15:8]							
4Bh	R75	RES	FOD0_DCO_N_DIV_STAT						
4Ch	R76	FOD0_DCO_NUM_STAT[7:0]							
4Dh	R77	FOD0_DCO_NUM_STAT[15:8]							
4Eh	R78	FOD0_DCO_NUM_STAT[23:16]							
4Fh	R79	RES	FOD1_DCO_N_DIV_STAT						
50h	R80	FOD1_DCO_NUM_STAT[7:0]							
51h	R81	FOD1_DCO_NUM_STAT[15:8]							
52h	R82	FOD1_DCO_NUM_STAT[23:16]							
53h	R83	BANK1_CLK_SEL			BANK0_CLK_SEL			PATH1_EDGE_COMB_EN	PATH0_EDGE_COMB_EN
54h	R84	RES		BANK3_CLK_SEL			BANK2_CLK_SEL		
55h	R85	RES		BANK5_CLK_SEL			BANK4_CLK_SEL		
56h	R86	BANK0_CH_DIV[7:0]							
57h	R87	BANK0_CH_DIV[15:8]							
58h	R88	BANK2_CH_DIV				BANK1_CH_DIV			
59h	R89	RES							IN0_LOS
5Ah	R90	BANK4_CH_DIV				BANK3_CH_DIV			
5Bh	R91	PERST_BUF_BANK1		PERST_BUF_BANK0		BANK5_CH_DIV			
5Ch	R92	PERST_BUF_BANK5		PERST_BUF_BANK4		PERST_BUF_BANK3		PERST_BUF_BANK2	
5Dh	R93	BANK1_AUTO_CLK_SWITCHBACK_EN	BANK0_AUTO_CLK_SWITCHBACK_EN	BANK5_AUTO_CLK_SWITCHOVER_EN	BANK4_AUTO_CLK_SWITCHOVER_EN	BANK3_AUTO_CLK_SWITCHOVER_EN	BANK2_AUTO_CLK_SWITCHOVER_EN	BANK1_AUTO_CLK_SWITCHOVER_EN	BANK0_AUTO_CLK_SWITCHOVER_EN
5Eh	R94	BANK3_AUTO_CLK_SWITCHOVER_CLK_SEL	BANK2_AUTO_CLK_SWITCHOVER_CLK_SEL	BANK1_AUTO_CLK_SWITCHOVER_CLK_SEL	BANK0_AUTO_CLK_SWITCHOVER_CLK_SEL	BANK5_AUTO_CLK_SWITCHBACK_EN	BANK4_AUTO_CLK_SWITCHBACK_EN	BANK3_AUTO_CLK_SWITCHBACK_EN	BANK2_AUTO_CLK_SWITCHBACK_EN
5Fh	R95	BANK5_CLK_SWITCHOVER_TYPE	BANK4_CLK_SWITCHOVER_TYPE	BANK3_CLK_SWITCHOVER_TYPE	BANK2_CLK_SWITCHOVER_TYPE	BANK1_CLK_SWITCHOVER_TYPE	BANK0_CLK_SWITCHOVER_TYPE	BANK5_AUTO_CLK_SWITCHOVER_CLK_SEL	BANK4_AUTO_CLK_SWITCHOVER_CLK_SEL
60h	R96	BANK1_SWITCHOVER_FRC_CLK_EN	BANK0_SWITCHOVER_FRC_CLK_EN	BANK5_CLK_DIS_ON_LOS	BANK4_CLK_DIS_ON_LOS	BANK3_CLK_DIS_ON_LOS	BANK2_CLK_DIS_ON_LOS	BANK1_CLK_DIS_ON_LOS	BANK0_CLK_DIS_ON_LOS
61h	R97	OUT1_SLEW_RATE		OUT0_SLEW_RATE		BANK5_SWITCHOVER_FRC_CLK_EN	BANK4_SWITCHOVER_FRC_CLK_EN	BANK3_SWITCHOVER_FRC_CLK_EN	BANK2_SWITCHOVER_FRC_CLK_EN
62h	R98	OUT5_SLEW_RATE		OUT4_SLEW_RATE		OUT3_SLEW_RATE		OUT2_SLEW_RATE	
63h	R99	OUT1_CMOS_SLEW_RATE		OUT0_CMOS_SLEW_RATE		OUT7_SLEW_RATE		OUT6_SLEW_RATE	
64h	R100	OUT5_CMOS_SLEW_RATE		OUT4_CMOS_SLEW_RATE		OUT3_CMOS_SLEW_RATE		OUT2_CMOS_SLEW_RATE	
65h	R101	OUT1_DIS_STATE		OUT0_DIS_STATE		OUT7_CMOS_SLEW_RATE		OUT6_CMOS_SLEW_RATE	
66h	R102	OUT5_DIS_STATE		OUT4_DIS_STATE		OUT3_DIS_STATE		OUT2_DIS_STATE	
67h	R103	OUT0_FMT		RES		OUT7_DIS_STATE		OUT6_DIS_STATE	
68h	R104	OUT4_FMT		OUT3_FMT		OUT2_FMT		OUT1_FMT	

Table 2-1. Register Map (continued)

Offset (Hex)	Register Acronym	Bit							
		7	6	5	4	3	2	1	0
69h	R105	RES							IN1_LOS
6Ah	R106	OUT1_CMOS_1P2V_EN	OUT0_CMOS_1P2V_EN	OUT7_FMT		OUT6_FMT		OUT5_FMT	
6Bh	R107	RES		OUT7_CMOS_1P2V_EN	OUT6_CMOS_1P2V_EN	OUT5_CMOS_1P2V_EN	OUT4_CMOS_1P2V_EN	OUT3_CMOS_1P2V_EN	OUT2_CMOS_1P2V_EN
6Ch	R108	OUT1_OE_GRP				OUT0_OE_GRP			
6Dh	R109	OUT3_OE_GRP				OUT2_OE_GRP			
6Eh	R110	OUT5_OE_GRP				OUT4_OE_GRP			
6Fh	R111	OUT7_OE_GRP				OUT6_OE_GRP			
70h	R112	OUT1_LPHCSL_VOD_SEL				OUT0_LPHCSL_VOD_SEL			
71h	R113	OUT3_LPHCSL_VOD_SEL				OUT2_LPHCSL_VOD_SEL			
72h	R114	OUT5_LPHCSL_VOD_SEL				OUT4_LPHCSL_VOD_SEL			
73h	R115	OUT7_LPHCSL_VOD_SEL				OUT6_LPHCSL_VOD_SEL			
74h	R116	OUT3_SYNC_MODE		OUT2_SYNC_MODE		OUT1_SYNC_MODE		OUT0_SYNC_MODE	
75h	R117	OUT7_SYNC_MODE		OUT6_SYNC_MODE		OUT5_SYNC_MODE		OUT4_SYNC_MODE	
76h	R118	OUT3P_OE_CMOS	OUT2N_OE_CMOS	OUT2P_OE_CMOS	OUT1N_OE_CMOS	OUT1P_OE_CMOS	OUT0N_OE_CMOS	OUT0P_OE_CMOS	SINGLE_CMOS_EN_SYNC
77h	R119	OUT7P_OE_CMOS	OUT6N_OE_CMOS	OUT6P_OE_CMOS	OUT5N_OE_CMOS	OUT5P_OE_CMOS	OUT4N_OE_CMOS	OUT4P_OE_CMOS	OUT3N_OE_CMOS
78h	R120	OUT6_FREQ_DET_EN	OUT5_FREQ_DET_EN	OUT4_FREQ_DET_EN	OUT3_FREQ_DET_EN	OUT2_FREQ_DET_EN	OUT1_FREQ_DET_EN	OUT0_FREQ_DET_EN	OUT7N_OE_CMOS
79h	R121	RES							IN2_LOS
7Ah	R122	OUT4_FREQ_DET_THRESH	OUT3_FREQ_DET_THRESH	OUT2_FREQ_DET_THRESH	OUT1_FREQ_DET_THRESH	OUT0_FREQ_DET_THRESH	RES		OUT7_FREQ_DET_EN
7Bh	R123	OUT2_AMP_DET_EN	OUT1_AMP_DET_EN	OUT0_AMP_DET_EN	RES		OUT7_FREQ_DET_THRESH	OUT6_FREQ_DET_THRESH	OUT5_FREQ_DET_THRESH
7Ch	R124	OUT_AMP_DET_THRESH	RES		OUT7_AMP_DET_EN	OUT6_AMP_DET_EN	OUT5_AMP_DET_EN	OUT4_AMP_DET_EN	OUT3_AMP_DET_EN
7Dh	R125	CRC_ERROR_EVT_INTR_EN	IN2_LOS_LMT_EVT_INTR_EN	IN1_LOS_LMT_EVT_INTR_EN	IN0_LOS_LMT_EVT_INTR_EN	IN2_LOS_EVT_INTR_EN	IN1_LOS_EVT_INTR_EN	IN0_LOS_EVT_INTR_EN	DEV_INTR
7Eh	R126	OUT3N_FREQ_ERR_EVT_INTR_EN	OUT3P_FREQ_ERR_EVT_INTR_EN	OUT2N_FREQ_ERR_EVT_INTR_EN	OUT2P_FREQ_ERR_EVT_INTR_EN	OUT1N_FREQ_ERR_EVT_INTR_EN	OUT1P_FREQ_ERR_EVT_INTR_EN	OUT0N_FREQ_ERR_EVT_INTR_EN	OUT0P_FREQ_ERR_EVT_INTR_EN
7Fh	R127	OUT7N_FREQ_ERR_EVT_INTR_EN	OUT7P_FREQ_ERR_EVT_INTR_EN	OUT6N_FREQ_ERR_EVT_INTR_EN	OUT6P_FREQ_ERR_EVT_INTR_EN	OUT5N_FREQ_ERR_EVT_INTR_EN	OUT5P_FREQ_ERR_EVT_INTR_EN	OUT4N_FREQ_ERR_EVT_INTR_EN	OUT4P_FREQ_ERR_EVT_INTR_EN
80h	R128	OUT2N_AMP_ERR_EVT_INTR_EN	OUT2P_AMP_ERR_EVT_INTR_EN	OUT1N_AMP_ERR_EVT_INTR_EN	OUT1P_AMP_ERR_EVT_INTR_EN	OUT0N_AMP_ERR_EVT_INTR_EN	OUT0P_AMP_ERR_EVT_INTR_EN	RES	
81h	R129	OUT6N_AMP_ERR_EVT_INTR_EN	OUT6P_AMP_ERR_EVT_INTR_EN	OUT5N_AMP_ERR_EVT_INTR_EN	OUT5P_AMP_ERR_EVT_INTR_EN	OUT4N_AMP_ERR_EVT_INTR_EN	OUT4P_AMP_ERR_EVT_INTR_EN	OUT3N_AMP_ERR_EVT_INTR_EN	OUT3P_AMP_ERR_EVT_INTR_EN
82h	R130	RES	IN2_LOS_EVT	IN1_LOS_EVT	IN0_LOS_EVT	RES		OUT7N_AMP_ERR_EVT_INTR_EN	OUT7P_AMP_ERR_EVT_INTR_EN
83h	R131	IN1_LOS_CNTR				IN0_LOS_CNTR			
84h	R132	LOS_LMT				IN2_LOS_CNTR			
85h	R133	OUT0N_FREQ_GOOD	OUT0P_FREQ_GOOD	CRC_ERROR_EVT	CRC_ERROR	CRC_DONE	IN2_LOS_LMT_EVT	IN1_LOS_LMT_EVT	IN0_LOS_LMT_EVT
86h	R134	OUT4N_FREQ_GOOD	OUT4P_FREQ_GOOD	OUT3N_FREQ_GOOD	OUT3P_FREQ_GOOD	OUT2N_FREQ_GOOD	OUT2P_FREQ_GOOD	OUT1N_FREQ_GOOD	OUT1P_FREQ_GOOD

Table 2-1. Register Map (continued)

Offset (Hex)	Register Acronym	Bit							
		7	6	5	4	3	2	1	0
87h	R135	RES		OUT7N_FREQ_GOOD	OUT7P_FREQ_GOOD	OUT6N_FREQ_GOOD	OUT6P_FREQ_GOOD	OUT5N_FREQ_GOOD	OUT5P_FREQ_GOOD
88h	R136	OUT3N_FREQ_ERR_EVT	OUT3P_FREQ_ERR_EVT	OUT2N_FREQ_ERR_EVT	OUT2P_FREQ_ERR_EVT	OUT1N_FREQ_ERR_EVT	OUT1P_FREQ_ERR_EVT	OUT0N_FREQ_ERR_EVT	OUT0P_FREQ_ERR_EVT
89h	R137	OUT7N_FREQ_ERR_EVT	OUT7P_FREQ_ERR_EVT	OUT6N_FREQ_ERR_EVT	OUT6P_FREQ_ERR_EVT	OUT5N_FREQ_ERR_EVT	OUT5P_FREQ_ERR_EVT	OUT4N_FREQ_ERR_EVT	OUT4P_FREQ_ERR_EVT
8Ah	R138	OUT2N_AMP_GOOD	OUT2P_AMP_GOOD	OUT1N_AMP_GOOD	OUT1P_AMP_GOOD	OUT0N_AMP_GOOD	OUT0P_AMP_GOOD	RES	
8Bh	R139	OUT6N_AMP_GOOD	OUT6P_AMP_GOOD	OUT5N_AMP_GOOD	OUT5P_AMP_GOOD	OUT4N_AMP_GOOD	OUT4P_AMP_GOOD	OUT3N_AMP_GOOD	OUT3P_AMP_GOOD
8Ch	R140	OUT1N_AMP_ERR_EVT	OUT1P_AMP_ERR_EVT	OUT0N_AMP_ERR_EVT	OUT0P_AMP_ERR_EVT	RES		OUT7N_AMP_GOOD	OUT7P_AMP_GOOD
8Dh	R141	OUT5N_AMP_ERR_EVT	OUT5P_AMP_ERR_EVT	OUT4N_AMP_ERR_EVT	OUT4P_AMP_ERR_EVT	OUT3N_AMP_ERR_EVT	OUT3P_AMP_ERR_EVT	OUT2N_AMP_ERR_EVT	OUT2P_AMP_ERR_EVT
8Eh	R142	RES				OUT7N_AMP_ERR_EVT	OUT7P_AMP_ERR_EVT	OUT6N_AMP_ERR_EVT	OUT6P_AMP_ERR_EVT
8Fh	R143	RES				PROD_REV_ID			
90h	R144	OTP_ID							
93h	R147	UNLOCK_PROTECTED_REG							
94h	R148	VDDR_SUP_LVL_DET_RB		VDDX_SUP_LVL_DET_RB		VDDD_SUP_LVL_DET_RB		VDDA_SUP_LVL_DET_RB	
95h	R149	VDDO_5_SUP_LVL_DET_RB		VDDO_3_4_SUP_LVL_DET_RB		VDDO_1_2_SUP_LVL_DET_RB		VDDO_0_SUP_LVL_DET_RB	
96h	R150	RES				VDDO_7_SUP_LVL_DET_RB		VDDO_6_SUP_LVL_DET_RB	
99h	R153	RES		OTP_PAGE0_SEL_CODE					
9Ah	R154	RES		OTP_PAGE1_SEL_CODE					
9Bh	R155	RES		OTP_PAGE2_SEL_CODE					
9Ch	R156	RES		OTP_PAGE3_SEL_CODE					
9Dh	R157	OTP_PAGE_RB		OTP_PAGE_SEL_CODE_RB					
BBh	R187	CRC_COMPUTED							
BCh	R188	RES						BOOTOSC_CLK_DIS	RES
FDh	R253	RES						PAGE_SEL_0	
13Fh	R319	RES							CLK_READY
240h	R576	RES							OUT0_DIS
244h	R580	RES							OUT1_DIS
248h	R584	RES							OUT2_DIS
24Ch	R588	RES							OUT3_DIS
250h	R592	RES							OUT4_DIS
254h	R596	RES							OUT5_DIS
258h	R600	RES							OUT6_DIS
25Ch	R604	RES							OUT7_DIS
270h	R624	RES						PATH1_FOD_SEL	RES
2E9h	R745	OUT2P_INV_POL	OUT1P_INV_POL	OUT0P_INV_POL	RES				
2EAh	R746	OUT2N_INV_POL	OUT1N_INV_POL	OUT0N_INV_POL	OUT7P_INV_POL	OUT6P_INV_POL	OUT5P_INV_POL	OUT4P_INV_POL	OUT3P_INV_POL

Table 2-1. Register Map (continued)

Offset (Hex)	Register Acronym	Bit							
		7	6	5	4	3	2	1	0
2EBh	R747	RES			OUT7N_INV_POL	OUT6N_INV_POL	OUT5N_INV_POL	OUT4N_INV_POL	OUT3N_INV_POL
2FAh	R762	DIE_ID_1[7:0]							
2FBh	R763	RES	DIE_ID_1[14:8]						
2FCh	R764	DIE_ID_2[7:0]							
2FEh	R766	DIE_ID_2[15:8]							
2FFh	R767	DIE_ID_3[7:0]							
300h	R768	DIE_ID_3[15:8]							
302h	R770	STORED_CRC							

3 Device Registers

Table 3-1 lists the memory-mapped registers for the Device registers. All register offset addresses not listed in Table 3-1 should be considered as reserved locations and the register contents should not be modified.

Table 3-1. DEVICE Registers

Offset	Acronym	Register Name	Section
0h	R0		Section 3.1
1h	R1		Section 3.2
2h	R2		Section 3.3
3h	R3		Section 3.4
4h	R4		Section 3.5
5h	R5		Section 3.6
6h	R6		Section 3.7
8h	R8		Section 3.8
9h	R9		Section 3.9
Ah	R10		Section 3.10
Bh	R11		Section 3.11
Ch	R12		Section 3.12
Dh	R13		Section 3.13
Eh	R14		Section 3.14
Fh	R15		Section 3.15
10h	R16		Section 3.16
11h	R17		Section 3.17
12h	R18		Section 3.18
13h	R19		Section 3.19
14h	R20		Section 3.20
15h	R21		Section 3.21
16h	R22		Section 3.22
17h	R23		Section 3.23
18h	R24		Section 3.24
19h	R25		Section 3.25
1Ah	R26		Section 3.26
1Bh	R27		Section 3.27
1Ch	R28		Section 3.28
1Dh	R29		Section 3.29
1Eh	R30		Section 3.30
1Fh	R31		Section 3.31
20h	R32		Section 3.32
21h	R33		Section 3.33
22h	R34		Section 3.34
23h	R35		Section 3.35
24h	R36		Section 3.36
25h	R37		Section 3.37
26h	R38		Section 3.38
27h	R39		Section 3.39
28h	R40		Section 3.40
29h	R41		Section 3.41
2Ah	R42		Section 3.42
2Bh	R43		Section 3.43

Table 3-1. DEVICE Registers (continued)

Offset	Acronym	Register Name	Section
2Ch	R44		Section 3.44
2Dh	R45		Section 3.45
2Eh	R46		Section 3.46
2Fh	R47		Section 3.47
30h	R48		Section 3.48
31h	R49		Section 3.49
32h	R50		Section 3.50
33h	R51		Section 3.51
34h	R52		Section 3.52
35h	R53		Section 3.53
36h	R54		Section 3.54
37h	R55		Section 3.55
39h	R57		Section 3.56
3Ah	R58		Section 3.57
3Bh	R59		Section 3.58
3Ch	R60		Section 3.59
3Dh	R61		Section 3.60
3Eh	R62		Section 3.61
3Fh	R63		Section 3.62
40h	R64		Section 3.63
41h	R65		Section 3.64
42h	R66		Section 3.65
43h	R67		Section 3.66
44h	R68		Section 3.67
45h	R69		Section 3.68
46h	R70		Section 3.69
47h	R71		Section 3.70
48h	R72		Section 3.71
49h	R73		Section 3.72
4Ah	R74		Section 3.73
4Bh	R75		Section 3.74
4Ch	R76		Section 3.75
4Dh	R77		Section 3.76
4Eh	R78		Section 3.77
4Fh	R79		Section 3.78
50h	R80		Section 3.79
51h	R81		Section 3.80
52h	R82		Section 3.81
53h	R83		Section 3.82
54h	R84		Section 3.83
55h	R85		Section 3.84
56h	R86		Section 3.85
57h	R87		Section 3.86
58h	R88		Section 3.87
59h	R89		Section 3.88
5Ah	R90		Section 3.89
5Bh	R91		Section 3.90

Table 3-1. DEVICE Registers (continued)

Offset	Acronym	Register Name	Section
5Ch	R92		Section 3.91
5Dh	R93		Section 3.92
5Eh	R94		Section 3.93
5Fh	R95		Section 3.94
60h	R96		Section 3.95
61h	R97		Section 3.96
62h	R98		Section 3.97
63h	R99		Section 3.98
64h	R100		Section 3.99
65h	R101		Section 3.100
66h	R102		Section 3.101
67h	R103		Section 3.102
68h	R104		Section 3.103
69h	R105		Section 3.104
6Ah	R106		Section 3.105
6Bh	R107		Section 3.106
6Ch	R108		Section 3.107
6Dh	R109		Section 3.108
6Eh	R110		Section 3.109
6Fh	R111		Section 3.110
70h	R112		Section 3.111
71h	R113		Section 3.112
72h	R114		Section 3.113
73h	R115		Section 3.114
74h	R116		Section 3.115
75h	R117		Section 3.116
76h	R118		Section 3.117
77h	R119		Section 3.118
78h	R120		Section 3.119
79h	R121		Section 3.120
7Ah	R122		Section 3.121
7Bh	R123		Section 3.122
7Ch	R124		Section 3.123
7Dh	R125		Section 3.124
7Eh	R126		Section 3.125
7Fh	R127		Section 3.126
80h	R128		Section 3.127
81h	R129		Section 3.128
82h	R130		Section 3.129
83h	R131		Section 3.130
84h	R132		Section 3.131
85h	R133		Section 3.132
86h	R134		Section 3.133
87h	R135		Section 3.134
88h	R136		Section 3.135
89h	R137		Section 3.136
8Ah	R138		Section 3.137

Table 3-1. DEVICE Registers (continued)

Offset	Acronym	Register Name	Section
8Bh	R139		Section 3.138
8Ch	R140		Section 3.139
8Dh	R141		Section 3.140
8Eh	R142		Section 3.141
8Fh	R143		Section 3.142
90h	R144		Section 3.143
93h	R147		Section 3.144
94h	R148		Section 3.145
95h	R149		Section 3.146
96h	R150		Section 3.147
99h	R153		Section 3.148
9Ah	R154		Section 3.149
9Bh	R155		Section 3.150
9Ch	R156		Section 3.151
9Dh	R157		Section 3.152
BBh	R187		Section 3.153
BCh	R188		Section 3.154
FDh	R253		Section 3.155
13Fh	R319		Section 3.156
240h	R576		Section 3.157
244h	R580		Section 3.158
248h	R584		Section 3.159
24Ch	R588		Section 3.160
250h	R592		Section 3.161
254h	R596		Section 3.162
258h	R600		Section 3.163
25Ch	R604		Section 3.164
270h	R624		Section 3.165
2E9h	R745		Section 3.166
2EAh	R746		Section 3.167
2EBh	R747		Section 3.168
2FAh	R762		Section 3.169
2FBh	R763		Section 3.170
2FCh	R764		Section 3.171
2FEh	R766		Section 3.172
2FFh	R767		Section 3.173
300h	R768		Section 3.174
302h	R770		Section 3.175

Complex bit access types are encoded to fit into small table cells. Table 3-2 shows the codes that are used for access types in this section.

Table 3-2. Device Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		

Table 3-2. Device Access Type Codes (continued)

Access Type	Code	Description
W	W	Write
W1C	W 1C	Write 1 to clear
Reset or Default Value		
-n		Value after reset or the default value

3.1 R0 Register (Offset = 0h) [Reset = 8Bh]

R0 is shown in Table 3-3.

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Table 3-3. R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	VENDOR_ID[7:0]	R	8Bh	Vendor ID, two bytes total. Complete Value: 0x038B

3.2 R1 Register (Offset = 1h) [Reset = 03h]

R1 is shown in Table 3-4.

Return to the Summary Table.

Table 3-4. R1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	VENDOR_ID[15:8]	R	3h	Vendor ID, two bytes total. Complete Value: 0x038B

3.3 R2 Register (Offset = 2h) [Reset = 00h]

R2 is shown in Table 3-5.

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Table 3-5. R2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	FLOAT_VDDO_6	R/W	0h	Float VDDO_6 Supply. Determines whether or not the VDDO_6 power supply will be expected. If expected, the pin's supply level will be analyzed to determine when it is safe to enable OUT6. If not expected, the device will ignore the VDDO_6 pin. 0h = Used; The device assumes that VDDO_6 is present, and VDDO_6 must be connected for proper operation 1h = Floating; The device assumes that VDDO_6 is not present, and VDDO_6 may be floating (unconnected)
6	FLOAT_VDDO_5	R/W	0h	Float VDDO_5 Supply. Determines whether or not the VDDO_5 power supply will be expected. If expected, the pin's supply level will be analyzed to determine when it is safe to enable OUT5. If not expected, the device will ignore the VDDO_5 pin. 0h = Used; The device assumes that VDDO_5 is present, and VDDO_5 must be connected for proper operation 1h = Floating; The device assumes that VDDO_5 is not present, and VDDO_5 may be floating (unconnected)
5	FLOAT_VDDO_3_4	R/W	0h	Float VDDO_3_4 Supply. Determines whether or not the VDDO_3_4 power supply will be expected. If expected, the pin's supply level will be analyzed to determine when it is safe to enable OUT3 and OUT4. If not expected, the device will ignore the VDDO_3_4 pin. 0h = Used; The device assumes that VDDO_3_4 is present, and VDDO_3_4 must be connected for proper operation 1h = Floating; The device assumes that VDDO_3_4 is not present, and VDDO_3_4 may be floating (unconnected)
4	FLOAT_VDDO_1_2	R/W	0h	Float VDDO_1_2 Supply. Determines whether or not the VDDO_1_2 power supply will be expected. If expected, the pin's supply level will be analyzed to determine when it is safe to enable OUT1 and OUT2. If not expected, the device will ignore the VDDO_1_2 pin. 0h = Used; The device assumes that VDDO_1_2 is present, and VDDO_1_2 must be connected for proper operation 1h = Floating; The device assumes that VDDO_1_2 is not present, and VDDO_1_2 may be floating (unconnected)
3	FLOAT_VDDO_0	R/W	0h	Float VDDO_0 Supply. Determines whether or not the VDDO_0 power supply will be expected. If expected, the pin's supply level will be analyzed to determine when it is safe to enable OUT0. If not expected, the device will ignore the VDDO_0 pin. 0h = Used; The device assumes that VDDO_0 is present, and VDDO_0 must be connected for proper operation 1h = Floating; The device assumes that VDDO_0 is not present, and VDDO_0 may be floating (unconnected)
2	FLOAT_VDDR	R/W	0h	Float VDDR Supply. Determines whether or not the VDDR power supply will be expected. If expected, the pin's supply level will be analyzed to determine when it is safe to enable the IN[2:1]/GPI[5:2] blocks. If not expected, the device will ignore the VDDR pin. 0h = Used; The device assumes that VDDR is present, and VDDR must be connected for proper operation 1h = Floating; The device assumes that VDDR is not present, and VDDR may be floating (unconnected)
1	FLOAT_VDDX	R/W	0h	Float VDDX Supply. Determines whether or not the VDDX power supply will be expected. If expected, the pin's supply level will be analyzed to determine when it is safe to enable the IN0/GPI[1:0] block. If not expected, the device will ignore the VDDX pin. 0h = Used; The device assumes that VDDX is present, and VDDX must be connected for proper operation 1h = Floating; The device assumes that VDDX is not present, and VDDX may be floating (unconnected)

Table 3-5. R2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	OTP_BURNT	R	0h	Indicates whether or not the OTP has been programmed, and controls whether or not the OTP data will be loaded into the registers during the power-up sequence. Note: This field will be loaded from the OTP at power-up, regardless of the value of OTP_BURNT.

3.4 R3 Register (Offset = 3h) [Reset = 00h]

R3 is shown in Table 3-6.

Return to the Summary Table.

Table 3-6. R3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6-5	GPIO1_PU_RB	R	0h	GPIO1 Pin Power-up Value Readback 0h = 0: Low 1h = 1: Mid 3h = 3: High
4-3	GPIO0_PU_RB	R	0h	GPIO0 Pin Power-up Value Readback 0h = 0: Low 1h = 1: Mid 3h = 3: High
2	RESERVED	R	0h	Reserved
1	RESERVED	R	0h	Reserved
0	FLOAT_VDDO_7	R/W	0h	Float VDDO_7 Supply. Determines whether or not the VDDO_7 power supply will be expected. If expected, the pin's supply level will be analyzed to determine when it is safe to enable OUT7. If not expected, the device will ignore the VDDO_7 pin. 0h = Used; The device assumes that VDDO_7 is present, and VDDO_7 must be connected for proper operation 1h = Floating; The device assumes that VDDO_7 is not present, and VDDO_7 may be floating (unconnected)

3.5 R4 Register (Offset = 4h) [Reset = 00h]

R4 is shown in Table 3-7.

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Table 3-7. R4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	0h	Reserved
1-0	GPIO2_PU_RB	R	0h	GPIO2 Pin Power-up Value Readback 0h = 0: Low 1h = 1: Mid 3h = 3: High

3.6 R5 Register (Offset = 5h) [Reset = 00h]

R5 is shown in Table 3-8.

Return to the Summary Table.

Table 3-8. R5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6	RESERVED	R	0h	Reserved
5	RESERVED	R	0h	Reserved
4	RESERVED	R	0h	Reserved
3	RESERVED	R	0h	Reserved
2	OTP_PAGE_SEL_DYN_DEBOUNCE	R/W	0h	OTP Page Selection (Dynamic) Debounce Interval. Sets the amount of time that all dynamic OTP page selection pins must be stable before the device responds to a level change on any dynamic OTP page selection pin. Once all active dynamic OTP page selection pins have been stable for the selected amount of time, the resulting OTP Page Selection Code is registered and the selected page is loaded into the device registers. Any dynamic OTP page selection pin level changes that occur between the expiration of the debounce interval and completion of OTP autoload will be ignored until OTP autoload finishes. If the registered OTP Page Selection Code matches the current OTP Page Selection Code (for example, a short pulse was observed on the pin) or if the registered OTP Page Selection Code is invalid, no OTP autoload will occur. 0h = 133ns 1h = 4.2us
1	RESERVED	R	0h	Reserved
0	RESERVED	R	0h	Reserved

3.7 R6 Register (Offset = 6h) [Reset = 68h]

R6 is shown in Table 3-9.

Return to the Summary Table.

Table 3-9. R6 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	I2C_REG_ADDR_FMT	R/W	0h	I2C Register Address Format. Selects between 1-Byte Addressing and 2-Byte Addressing. In 1-Byte Addressing, only one byte of register address (the lower 8 bits) must be transmitted. The upper 2 bits are controlled by the PAGE_SEL_x register fields. In 2-Byte Addressing, two bytes of register address (all 10 bits) must be transmitted. The PAGE_SEL_x register fields are ignored. The required value of this field should be loaded from OTP. 0h = 1-Byte Addressing; The upper 2 bits of the register address must be written to the PAGE_SEL field. 1h = 2-Byte Addressing; The PAGE_SEL field is not used. Instead, all ten register bits are acces through two subsequent 8-bit I2C accesses.
6-0	I2C_TRGT_ADDR	R/W	68h	I2C target address 7 bits, does not include R/W bit. This field is locked, and requires unlocking UNLOCK_PROTECTED_REG before using.

3.8 R8 Register (Offset = 8h) [Reset = 00h]

R8 is shown in Table 3-10.

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Table 3-10. R8 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PWRGD_SAMPLE_TMR	R/W	0h	PWRGD Function Sampling Timer. The value of this field sets the earliest time that the GPIO pin assigned with the PWRGD/PWRDN# function will be sampled for use with the PWRGD function. This timer exists to ensure that the pin is not sampled before it is stable. This timer starts once the voltages of both VDDA and VDDD reach 1.62V. When the timer expires, the value of the pin starts being evaluated for use with the PWRGD function. If PWRGD is asserted before the timer expires, the PWRGD function is seen to be asserted upon timer expiration. If PWRGD is asserted after the timer expires, the PWRGD function is seen to be asserted as the pin value changes. The timer is enabled/disabled using PWRGD_SAMPLE_TMR_EN. The timer is ignored if no pin is assigned with the PWRGD/ PWRDN# function (for that case, see SUP_LVL_RAMP_TMR and GLOABL_SUP_DET_TMR). The timer duration, which can range from 0.1ms to 25.6ms, is configured using the following equation: PWRGD_SAMPLE_TMR = 10 * timer_duration (ms) - 1

3.9 R9 Register (Offset = 9h) [Reset = 12h]

R9 is shown in Table 3-11.

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Table 3-11. R9 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6-1	SUP_LVL_RAMP_TMR	R/W	9h	Supply Level Ramp-up Timer. The value of this field controls the duration of the Supply Level Ramp-up Timer. For each power supply pin (VDDA, VDDD, VDDX, VDDR, VDDO_*, VDD_REF), a timer exists to ensure that the device does not begin operation until the power supply pin has ramped up to its final voltage. For each pin, this timer starts once the pin voltage reaches 1.62V. When the timer expires, the device assumes that the power supply is fully ramped up, and supply detection for that pin no longer gates device operation. The user must set this field according to the longest expected power supply ramp-up time, measured from 1.62V to the final voltage. This timer is ignored if a GPIO pin is assigned with the PWRGD/PWRDN# function (for that case, see PWRGD_SAMPLE_TMR). The timer duration, which can range from 0.1ms to 6.4ms, is configured using the following equation: SUP_LVL_RAMP_TMR = 10 * timer_duration (ms) - 1
0	PWRGD_SAMPLE_TMR_EN	R/W	0h	PWRGD Function Sampling Timer Enable. When set to 0x1, the PWRGD Functrion Sampling Timer is used to delay sampling of the GPIO pin assigned with the PWRGD/PWRDN# function. See PWRGD_SAMPLE_TMR for further details. When set to 0x0, timer is not used, and the pin begins getting sampled immediately after pin functions are loaded from the OTP.

3.10 R10 Register (Offset = Ah) [Reset = 2Ch]

R10 is shown in Table 3-12.

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Table 3-12. R10 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	GLOBAL_SUP_DET_TMR	R/W	2Ch	Global Supply Detect Timer. The value of this field controls the duration of the Global Supply Detect Timer. This timer exists to ensure that if one of the supply detect pins (VDDA, VDDD, VDDX, VDDR, VDDO_*, VDD_REF) fails to ramp up, the device will not hang. This timer starts once the voltages of both VDDA and VDDD reach 1.62V. Once all power supply pins that are expected to be used (FLOAT_VDDx == 0x0) reach 1.62V and their corresponding Supply Level Ramp-Up Timer expires, the device will begin all remaining power-up sequence steps and clocks will start. If this timer expires before that condition occurs, the device will stop waiting for power supply pins to ramp up, and the device will begin all remaining power-up sequence steps. While this prevents the device from hanging, it may result in unintended behavior. The user must set this field according to the longest allowable delay between core power supplies starting to ramp up, and the first output clocks starting. The timer is enabled/disabled using GLOBAL_SUP_DET_TMR_EN. This timer is ignored a GPIO pin is assigned with the PWRGD/ PWRDN# function (for that case, see PWRGD_SAMPLE_TMR). The timer duration, which can range from 0.1ms to 25.6ms, is configured using the following equation: GLOBAL_SUP_DET_TMR = 10 * timer_duration (ms) - 1

3.11 R11 Register (Offset = Bh) [Reset = 30h]

R11 is shown in Table 3-13.

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Table 3-13. R11 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	FOD0_PD	R/W	0h	FOD0 Power-Down. Setting this bit to 1 turns off power to FOD0. This can be used to reduce power consumption in configurations where FOD0 is not used. 0h = Powered Up; FOD0 is not powered down. 1h = Powered Down; If FOD0 is not needed (pure buffer mode operation), then FOD0 is powered down for current savings. In general, FOD0 should be used for clock generation from the BAW resonator if only one FOD is needed.
6	BAW_PD	R/W	0h	BAW Power-Down. Setting this bit to 1 turns off power to the BAW. This can be used to reduce power consumption in configurations where the BAW is not used. 0h = Powered Up; The internal BAW resonator is not powered down. 1h = Powered Down; If the internal BAW resonator is not needed (pure buffer mode operation), then the BAW is powered down for current savings when setting this field to a 1. When powering off the BAW, both FODs should also be powered off.
5	AUTO_FOD_PD_EN	R/W	1h	Automatic FOD Power-down Enable. When enabled, if an FOD is not selected as the source of any output clock or reference clock, that FOD will be automatically powered down. If an 0h = No; If an FOD is not used for any outputs, it will still be powered up (increasing current consumption and potentially FOD-FOD crosstalk) 1h = Yes; If an FOD is not used for any outputs, it will still be automatically powered down (reducing current consumption and potentially FOD-FOD crosstalk)
4	CRC_IGNORE	R/W	1h	CRC Ignore. When set to 0x1 (default), if a CRC error is detected during OTP autoload, the CRC_ERROR status bit will be set, but the device will attempt to continue to power up normally with the loaded OTP data. When set to 0x0, if a CRC error is detected, the CRC_ERROR status bit will be set, and the device power-up sequence will stop. In this case, no output clocks will be generated. 0h = Halt; If there is a CRC error (CRC_ERROR set to 1), the device will halt the startup process. No output clocks will be generated. 1h = Ignore; If there is a CRC error (CRC_ERROR set to 1), it will be ignored, and the device will attempt to start up normally.
3	PIN_RESAMPLE_DIS	R/W	0h	Pin Resample Disable. By default, when the device exits power-down mode (the PWRDN# pin is deasserted or the PDN register field is written to 0x0), GPIO0, GPIO1, and GPIO2 are sampled. Each sampled value is used for OTP Page Selection (Power-Up) if the corresponding OTP_PAGE_SEL_PU_x register field is configured to use the GPIO pin. If this field has a value of 0x1 while exiting power-down mode, this pin re-sampling will not occur, and the last sampled values of the GPIO pins will be retained.
2	OTP_AUTOLOAD_DIS	R/W	0h	OTP Autoload Disable. By default, when the device exits power-down mode (the PWRDN# pin is deasserted or the PDN register field is written to 0x0), OTP data is loaded into the device registers; however, if OTP_AUTOLOAD_DIS has a value of 0x1 while exiting power-down mode, this data transfer will not occur. The OTP_AUTOLOAD_DIS register field has no effect on dynamic OTP page changes. When changing the device settings and doing a PDN toggle to recalibrate the FODs, this field should be written to a 1 before PDN is cleared to prevent reloading from OTP.

Table 3-13. R11 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	PDN	R/W	0h	Power-Down. Writing this bit with 0x1, which is equivalent to asserting the PWRDN# pin, causes the device to enter a power-down mode. Writing this bit with 0x0, which is equivalent to deasserting the PWRDN# pin, casuse the device to exit power-down mode. The resulting behavior from entering/exiting power-down mode is defined by the PIN_RESAMPLE_DIS and OTP_AUTOLOAD_DIS register fields. When modifying the FOD divider values, TI recommends setting PDN to 1, setting OTP_AUTOLOAD_DIS to 1, then setting PDN to 0 to recalibrate the FODs for best performance.
0	GLOBAL_SUP_DET_TMR_EN	R/W	0h	Global Supply Detect Timer Enable. When set to 0x1, the Global Supply Detect Timer is used to prevent the device from hanging if one of the power supply pins is slow to ramp up. See GLOBAL_SUP_DET_TMR for further details. When set to 0x0, timer is not used, and if a supply pin is slow to ramp up, the device will hang until it finishes ramping up.

3.12 R12 Register (Offset = Ch) [Reset = 0Fh]

R12 is shown in Table 3-14.

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Table 3-14. R12 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	Reserved
3	IN2_PD	R/W	1h	IN2 Power-Down. Setting this bit to 1 turns off power to IN2. This can be used to reduce power consumption in configurations where IN2 is not used. 0h = Powered Up; IN_2 is not powered down. 1h = Powered Down; Setting this field to a 1 reduces power consumption in configurations where IN_2 is not used.
2	IN1_PD	R/W	1h	IN1 Power-Down. Setting this bit to 1 turns off power to IN1. This can be used to reduce power consumption in configurations where IN1 is not used. 0h = Powered Up; IN_1 is not powered down. 1h = Powered Down; Setting this field to a 1 reduces power consumption in configurations where IN_1 is not used.
1	IN0_PD	R/W	1h	IN0 Power-Down. Setting this bit to 1 turns off power to IN0. This can be used to reduce power consumption in configurations where IN0 is not used. 0h = Powered Up; IN_0 is not powered down. 1h = Powered Down; Setting this field to a 1 reduces power consumption in configurations where IN_0 is not used.
0	FOD1_PD	R/W	1h	FOD1 Power-Down. Setting this bit to 1 turns off power to FOD1. This can be used to reduce power consumption in configurations where FOD1 is not used. 0h = Powered Up; FOD1 is not powered down. 1h = Powered Down; If FOD1 is not needed (pure buffer mode operation), then FOD1 is powered down for current savings. In general, FOD0 should be used for clock generation from the BAW resonator if only one FOD is needed.

3.13 R13 Register (Offset = Dh) [Reset = 80h]

R13 is shown in Table 3-15.

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Table 3-15. R13 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	PWRGD_PWRDN_PIN_SEL	R/W	8h	PWRGD/PWRDN# Pin Select. Selects which pin, if any, is used for the PWRGD/PWRDN# function. When a pin is assigned the PWRGD/PWRDN# function, the value of the corresponding GPIx_FUNC/GPIOx_FUNC field is ignored, with one exception: If a pin is assigned the PWRGD/PWRDN# function (via this field) and the OTP Page Selection (Dynamic) function (via GPIx_FUNC/GPIOx_FUNC) a hybrid function will be selected, which enables selection of functional/power-down OTP pages. Whether or not a pin is assigned with the PWRGD/PWRDN# function has an influence of the device power-up sequence (see Figure 7-3). 2h = 2: GPI_2 3h = 3: GPI_3 4h = 4: GPI_4 5h = 5: GPI_5 6h = 6: GPIO_0 7h = 7: GPIO_1 8h = 8: GPIO_2 9h = 9: GPIO_3 Ah = 10: GPIO_4 Fh = 15: Unused
3-0	RESERVED	R	0h	Reserved

3.14 R14 Register (Offset = Eh) [Reset = 0Ch]

R14 is shown in Table 3-16.

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Table 3-16. R14 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0h	Reserved
4-0	GPI0_FUNC	R/W	Ch	GPI0 Function. Determines the function of GPI0. If "Group Output Enable" is selected, see "GPI0_OE_GRP_SEL" to select the Output Enable Group for GPI0. If "GPI" is selected, see "GPI0_LIVE_RB" for pin value readback. If GPI0 is not used, select "GPI". 0h = 0: Group OE 1h = 1: Global OE 3h = 3: I2C Bit 0 4h = 4: I2C Bit 1 6h = 6: PERST_IN0# 7h = 7: PERST_IN1# 8h = 8: PERST_IN2# Ch = 12: GPI

3.15 R15 Register (Offset = Fh) [Reset = 0Ch]

R15 is shown in Table 3-17.

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Table 3-17. R15 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0h	Reserved
4-0	GPI1_FUNC	R/W	Ch	GPI1 Function. Determines the function of GPI1. If "Group Output Enable" is selected, see "GPI1_OE_GRP_SEL" to select the Output Enable Group for GPI1. If "GPI" is selected, see "GPI1_LIVE_RB" for pin value readback. If GPI1 is not used, select "GPI". 0h = 0: Group OE 1h = 1: Global OE 3h = 3: I2C Bit 0 4h = 4: I2C Bit 1 6h = 6: PERST_IN0# 7h = 7: PERST_IN1# 8h = 8: PERST_IN2# Ch = 12: GPI

3.16 R16 Register (Offset = 10h) [Reset = 0Ch]

R16 is shown in Table 3-18.

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Table 3-18. R16 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0h	Reserved
4-0	GPI2_FUNC	R/W	Ch	GPI2 Function. Determines the function of GPI2. If "Group Output Enable" is selected, see "GPI2_OE_GRP_SEL" to select the Output Enable Group for GPI2. If "GPI" is selected, see "GPI2_LIVE_RB" for pin value readback. If GPI2 is not used, select "GPI". 0h = 0: Group OE 1h = 1: Global OE 2h = 2: Reserved 3h = 3: I2C Bit 0 4h = 4: I2C Bit 1 6h = 6: PERST_IN0# 7h = 7: PERST_IN1# 8h = 8: PERST_IN2# Ch = 12: GPI

3.17 R17 Register (Offset = 11h) [Reset = 10h]

R17 is shown in Table 3-19.

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Table 3-19. R17 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6	RESERVED	R	0h	Reserved
5	RESERVED	R	0h	Reserved
4	OE_GLOBAL	R/W	1h	Global Output Enable. When set to 0, all outputs are disabled. When set to 1, all other contributors are considered to determine if each output is enabled. 0h = Outputs Disabled; When set to a 0, all outputs will be disabled. 1h = Other Logic for OE; When set to 1, all other contributors are considered to determine if each output is enabled.
3	RESERVED	R	0h	Reserved
2	RESERVED	R	0h	Reserved
1	RESERVED	R	0h	Reserved
0	RESERVED	R	0h	Reserved

3.18 R18 Register (Offset = 12h) [Reset = 0Ch]

R18 is shown in Table 3-20.

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Table 3-20. R18 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0h	Reserved
4-0	GPI3_FUNC	R/W	Ch	GPI3 Function. Determines the function of GPI3. If "Group Output Enable" is selected, see "GPI3_OE_GRP_SEL" to select the Output Enable Group for GPI3. If "GPI" is selected, see "GPI3_LIVE_RB" for pin value readback. If GPI3 is not used, select "GPI". 0h = 0: Group OE 1h = 1: Global OE 3h = 3: I2C Bit 0 4h = 4: I2C Bit 1 6h = 6: PERST_IN0# 7h = 7: PERST_IN1# 8h = 8: PERST_IN2# Ch = 12: GPI

3.19 R19 Register (Offset = 13h) [Reset = 0Ch]

R19 is shown in Table 3-21.

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Table 3-21. R19 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0h	Reserved
4-0	GPI4_FUNC	R/W	Ch	GPI4 Function. Determines the function of GPI4. If "Group Output Enable" is selected, see "GPI4_OE_GRP_SEL" to select the Output Enable Group for GPI4. If "GPI" is selected, see "GPI4_LIVE_RB" for pin value readback. If GPI4 is not used, select "GPI". 0h = 0: Group OE 1h = 1: Global OE 3h = 3: I2C Bit 0 4h = 4: I2C Bit 1 6h = 6: PERST_IN0# 7h = 7: PERST_IN1# 8h = 8: PERST_IN2# Ch = 12: GPI

3.20 R20 Register (Offset = 14h) [Reset = 0Ch]

R20 is shown in Table 3-22.

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Table 3-22. R20 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0h	Reserved
4-0	GPI5_FUNC	R/W	Ch	GPI5 Function. Determines the function of GPI5. If "Group Output Enable" is selected, see "GPI5_OE_GRP_SEL" to select the Output Enable Group for GPI5. If "GPI" is selected, see "GPI5_LIVE_RB" for pin value readback. If GPI5 is not used, select "GPI". 0h = 0: Group OE 1h = 1: Global OE 3h = 3: I2C Bit 0 4h = 4: I2C Bit 1 6h = 6: PERST_IN0# 7h = 7: PERST_IN1# 8h = 8: PERST_IN2# Ch = 12: GPI

3.21 R21 Register (Offset = 15h) [Reset = 05h]

R21 is shown in Table 3-23.

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Table 3-23. R21 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0h	Reserved
4-0	GPIO0_FUNC	R/W	5h	GPIO0 Function. Determines the function of GPIO0. If "Group Output Enable" is selected, see "GPIO0_OE_GRP_SEL" to select the Output Enable Group for GPIO0. If "GPI" is selected, see "GPIO0_LIVE_RB" for pin value readback. If "Status Output" is selected, see "GPIO0_OUT_SRC_SEL" to select the status output signal. If "GPO" is selected, see "GPIO0_GPO_VAL" to set the output value. If GPIO0 is not used, select "GPI". 0h = 0: Group OE 1h = 1: Global OE 2h = 2: Reserved 3h = 3: I2C Bit 0 4h = 4: I2C Bit 1 5h = 5: Dynamic OTP 6h = 6: PERST_IN0# 7h = 7: PERST_IN1# 8h = 8: PERST_IN2# Ch = 12: GPI 10h = 16: Status Output 11h = 17: GPO

3.22 R22 Register (Offset = 16h) [Reset = 05h]

R22 is shown in Table 3-24.

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Table 3-24. R22 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0h	Reserved
4-0	GPIO1_FUNC	R/W	5h	GPIO1 Function. Determines the function of GPIO1. If "Group Output Enable" is selected, see "GPIO1_OE_GRP_SEL" to select the Output Enable Group for GPIO1. If "GPI" is selected, see "GPIO1_LIVE_RB" for pin value readback. If "Status Output" is selected, see "GPIO1_OUT_SRC_SEL" to select the status output signal. If "GPO" is selected, see "GPIO1_GPO_VAL" to set the output value. If GPIO1 is not used, select "GPI". 0h = 0: Group OE 1h = 1: Global OE 3h = 3: I2C Bit 0 4h = 4: I2C Bit 1 5h = 5: Dynamic OTP 6h = 6: PERST_IN0# 7h = 7: PERST_IN1# 8h = 8: PERST_IN2# Ch = 12: GPI 10h = 16: Status Output 11h = 17: GPO

3.23 R23 Register (Offset = 17h) [Reset = 0Ch]

R23 is shown in Table 3-25.

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Table 3-25. R23 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0h	Reserved
4-0	GPIO2_FUNC	R/W	Ch	GPIO2 Function. Determines the function of GPIO2. If "Group Output Enable" is selected, see "GPIO2_OE_GRP_SEL" to select the Output Enable Group for GPIO2. If "GPI" is selected, see "GPIO2_LIVE_RB" for pin value readback. If "Status Output" is selected, see "GPIO2_OUT_SRC_SEL" to select the status output signal. If "GPO" is selected, see "GPIO2_GPO_VAL" to set the output value. If GPIO2 is not used, select "GPI". 0h = 0: Group OE 1h = 1: Global OE 3h = 3: I2C Bit 0 4h = 4: I2C Bit 1 5h = 5: Dynamic OTP 6h = 6: PERST_IN0# 7h = 7: PERST_IN1# 8h = 8: PERST_IN2# Ch = 12: GPI 10h = 16: Status Output 11h = 17: GPO

3.24 R24 Register (Offset = 18h) [Reset = 10h]

R24 is shown in Table 3-26.

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Table 3-26. R24 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0h	Reserved
4-0	GPIO3_FUNC	R/W	10h	GPIO3 Function. Determines the function of GPIO3. If "Group Output Enable" is selected, see "GPIO3_OE_GRP_SEL" to select the Output Enable Group for GPIO3. If "GPI" is selected, see "GPIO3_LIVE_RB" for pin value readback. If "Status Output" is selected, see "GPIO3_OUT_SRC_SEL" to select the status output signal. If "GPO" is selected, see "GPIO3_GPO_VAL" to set the output value. If GPIO3 is not used, select "GPI". 0h = 0: Group OE 1h = 1: Global OE 3h = 3: I2C Bit 0 4h = 4: I2C Bit 1 6h = 6: PERST_IN0# 7h = 7: PERST_IN1# 8h = 8: PERST_IN2# Ch = 12: GPI 10h = 16: Status Output 11h = 17: GPO

3.25 R25 Register (Offset = 19h) [Reset = 01h]

R25 is shown in Table 3-27.

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Table 3-27. R25 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0h	Reserved
4-0	GPIO4_FUNC	R/W	1h	GPIO4 Function. Determines the function of GPIO4. If "Group Output Enable" is selected, see "GPIO4_OE_GRP_SEL" to select the Output Enable Group for GPIO4. If "GPI" is selected, see "GPIO4_LIVE_RB" for pin value readback. If "Status Output" is selected, see "GPIO4_OUT_SRC_SEL" to select the status output signal. If "GPO" is selected, see "GPIO4_GPO_VAL" to set the output value. If GPIO4 is not used, select "GPI". 0h = 0: Group OE 1h = 1: Global OE 3h = 3: I2C Bit 0 4h = 4: I2C Bit 1 6h = 6: PERST_IN0# 7h = 7: PERST_IN1# 8h = 8: PERST_IN2# Ch = 12: GPI 10h = 16: Status Output 11h = 17: GPO

3.26 R26 Register (Offset = 1Ah) [Reset = 00h]

R26 is shown in Table 3-28.

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Table 3-28. R26 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	GPIO1_OUT_SRC_SEL	R/W	0h	GPIO1 Output Source Select. Determines which signal is selected for output when GPIO1_FUNC is set to "Status Output". If GPIO1_FUNC is set to any other function, the value of this field is ignored. 0h = 0: IN0_LOS 1h = 1: IN1_LOS 2h = 2: IN2_LOS 3h = 3: IN0_LOS_EVT 4h = 4: IN1_LOS_EVT 5h = 5: IN2_LOS_EVT 6h = 6: IN0_LOS_LMT_EVT 7h = 7: IN1_LOS_LMT_EVT 8h = 8: IN2_LOS_LMT_EVT 9h = 9: CLK_READY Ah = 10: IN0_PERST_BUF_MODE_STAT Bh = 11: IN1_PERST_BUF_MODE_STAT Ch = 12: IN2_PERST_BUF_MODE_STAT Dh = 13: DEV_INTR
3-0	GPIO0_OUT_SRC_SEL	R/W	0h	GPIO0 Output Source Select. Determines which signal is selected for output when GPIO0_FUNC is set to "Status Output". If GPIO0_FUNC is set to any other function, the value of this field is ignored. 0h = 0: IN0_LOS 1h = 1: IN1_LOS 2h = 2: IN2_LOS 3h = 3: IN0_LOS_EVT 4h = 4: IN1_LOS_EVT 5h = 5: IN2_LOS_EVT 6h = 6: IN0_LOS_LMT_EVT 7h = 7: IN1_LOS_LMT_EVT 8h = 8: IN2_LOS_LMT_EVT 9h = 9: CLK_READY Ah = 10: IN0_PERST_BUF_MODE_STAT Bh = 11: IN1_PERST_BUF_MODE_STAT Ch = 12: IN2_PERST_BUF_MODE_STAT Dh = 13: DEV_INTR

3.27 R27 Register (Offset = 1Bh) [Reset = 90h]

R27 is shown in Table 3-29.

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Table 3-29. R27 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	GPIO3_OUT_SRC_SEL	R/W	9h	GPIO3 Output Source Select. Determines which signal is selected for output when GPIO3_FUNC is set to "Status Output". If GPIO3_FUNC is set to any other function, the value of this field is ignored. 0h = 0: IN0_LOS 1h = 1: IN1_LOS 2h = 2: IN2_LOS 3h = 3: IN0_LOS_EVT 4h = 4: IN1_LOS_EVT 5h = 5: IN2_LOS_EVT 6h = 6: IN0_LOS_LMT_EVT 7h = 7: IN1_LOS_LMT_EVT 8h = 8: IN2_LOS_LMT_EVT 9h = 9: CLK_READY Ah = 10: IN0_PERST_BUF_MODE_STAT Bh = 11: IN1_PERST_BUF_MODE_STAT Ch = 12: IN2_PERST_BUF_MODE_STAT Dh = 13: DEV_INTR
3-0	GPIO2_OUT_SRC_SEL	R/W	0h	GPIO2 Output Source Select. Determines which signal is selected for output when GPIO2_FUNC is set to "Status Output". If GPIO2_FUNC is set to any other function, the value of this field is ignored. 0h = 0: IN0_LOS 1h = 1: IN1_LOS 2h = 2: IN2_LOS 3h = 3: IN0_LOS_EVT 4h = 4: IN1_LOS_EVT 5h = 5: IN2_LOS_EVT 6h = 6: IN0_LOS_LMT_EVT 7h = 7: IN1_LOS_LMT_EVT 8h = 8: IN2_LOS_LMT_EVT 9h = 9: CLK_READY Ah = 10: IN0_PERST_BUF_MODE_STAT Bh = 11: IN1_PERST_BUF_MODE_STAT Ch = 12: IN2_PERST_BUF_MODE_STAT Dh = 13: DEV_INTR

3.28 R28 Register (Offset = 1Ch) [Reset = 00h]

R28 is shown in Table 3-30.

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Table 3-30. R28 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GPI3_POLARITY	R/W	0h	GPI3 Polarity. Selects between normal and inverted polarity for the GPI3 pin. For 'Normal' polarity, functions ending with '#' are active-low, and functions ending without '#' are active-high. For 'Inverted' polarity, functions ending with '#' are active-high, and functions ending without '#' are active-low. 0h = Normal 1h = Inverted
6	GPI2_POLARITY	R/W	0h	GPI2 Polarity. Selects between normal and inverted polarity for the GPI2 pin. For 'Normal' polarity, functions ending with '#' are active-low, and functions ending without '#' are active-high. For 'Inverted' polarity, functions ending with '#' are active-high, and functions ending without '#' are active-low. 0h = Normal 1h = Inverted
5	GPI1_POLARITY	R/W	0h	GPI1 Polarity. Selects between normal and inverted polarity for the GPI1 pin. For 'Normal' polarity, functions ending with '#' are active-low, and functions ending without '#' are active-high. For 'Inverted' polarity, functions ending with '#' are active-high, and functions ending without '#' are active-low. 0h = Normal 1h = Inverted
4	GPI0_POLARITY	R/W	0h	GPI0 Polarity. Selects between normal and inverted polarity for the GPI0 pin. For 'Normal' polarity, functions ending with '#' are active-low, and functions ending without '#' are active-high. For 'Inverted' polarity, functions ending with '#' are active-high, and functions ending without '#' are active-low. 0h = Normal 1h = Inverted
3-0	GPIO4_OUT_SRC_SEL	R/W	0h	GPIO4 Output Source Select. Determines which signal is selected for output when GPIO4_FUNC is set to "Status Output". If GPIO4_FUNC is set to any other function, the value of this field is ignored. 0h = 0: IN0_LOS 1h = 1: IN1_LOS 2h = 2: IN2_LOS 3h = 3: IN0_LOS_EVT 4h = 4: IN1_LOS_EVT 5h = 5: IN2_LOS_EVT 6h = 6: IN0_LOS_LMT_EVT 7h = 7: IN1_LOS_LMT_EVT 8h = 8: IN2_LOS_LMT_EVT 9h = 9: CLK_READY Ah = 10: IN0_PERST_BUF_MODE_STAT Bh = 11: IN1_PERST_BUF_MODE_STAT Ch = 12: IN2_PERST_BUF_MODE_STAT Dh = 13: DEV_INTR

3.29 R29 Register (Offset = 1Dh) [Reset = C0h]

R29 is shown in Table 3-31.

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Table 3-31. R29 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GPI0_PULL_DN_EN	R/W	1h	GPI0 Internal Pull-down Resistor Enable
6	GPIO4_POLARITY	R/W	1h	GPIO4 Polarity. Selects between normal and inverted polarity for the GPIO4 pin. For 'Normal' polarity, functions ending with '#' are active-low, and functions ending without '#' are active-high. For 'Inverted' polarity, functions ending with '#' are active-high, and functions ending without '#' are active-low. This value affects both input and output functions. 0h = Normal 1h = Inverted
5	GPIO3_POLARITY	R/W	0h	GPIO3 Polarity. Selects between normal and inverted polarity for the GPIO3 pin. For 'Normal' polarity, functions ending with '#' are active-low, and functions ending without '#' are active-high. For 'Inverted' polarity, functions ending with '#' are active-high, and functions ending without '#' are active-low. This value affects both input and output functions. 0h = Normal 1h = Inverted
4	GPIO2_POLARITY	R/W	0h	GPIO2 Polarity. Selects between normal and inverted polarity for the GPIO2 pin. For 'Normal' polarity, functions ending with '#' are active-low, and functions ending without '#' are active-high. For 'Inverted' polarity, functions ending with '#' are active-high, and functions ending without '#' are active-low. This value affects both input and output functions. 0h = Normal 1h = Inverted
3	GPIO1_POLARITY	R/W	0h	GPIO1 Polarity. Selects between normal and inverted polarity for the GPIO1 pin. For 'Normal' polarity, functions ending with '#' are active-low, and functions ending without '#' are active-high. For 'Inverted' polarity, functions ending with '#' are active-high, and functions ending without '#' are active-low. This value affects both input and output functions. 0h = Normal 1h = Inverted
2	GPIO0_POLARITY	R/W	0h	GPIO0 Polarity. Selects between normal and inverted polarity for the GPIO0 pin. For 'Normal' polarity, functions ending with '#' are active-low, and functions ending without '#' are active-high. For 'Inverted' polarity, functions ending with '#' are active-high, and functions ending without '#' are active-low. This value affects both input and output functions. 0h = Normal 1h = Inverted
1	GPI5_POLARITY	R/W	0h	GPI5 Polarity. Selects between normal and inverted polarity for the GPI5 pin. For 'Normal' polarity, functions ending with '#' are active-low, and functions ending without '#' are active-high. For 'Inverted' polarity, functions ending with '#' are active-high, and functions ending without '#' are active-low. 0h = Normal 1h = Inverted
0	GPI4_POLARITY	R/W	0h	GPI4 Polarity. Selects between normal and inverted polarity for the GPI4 pin. For 'Normal' polarity, functions ending with '#' are active-low, and functions ending without '#' are active-high. For 'Inverted' polarity, functions ending with '#' are active-high, and functions ending without '#' are active-low. 0h = Normal 1h = Inverted

3.30 R30 Register (Offset = 1Eh) [Reset = 8Ah]

R30 is shown in Table 3-32.

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Table 3-32. R30 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GPI3_PULL_DN_EN	R/W	1h	GPI3 Internal Pull-down Resistor Enable
6-5	RESERVED	R	0h	Reserved
4	GPI2_PULL_UP_EN	R/W	0h	GPI2 Internal Pull-up Resistor Enable
3	GPI2_PULL_DN_EN	R/W	1h	GPI2 Internal Pull-down Resistor Enable
2	GPI1_PULL_UP_EN	R/W	0h	GPI1 Internal Pull-up Resistor Enable
1	GPI1_PULL_DN_EN	R/W	1h	GPI1 Internal Pull-down Resistor Enable
0	GPI0_PULL_UP_EN	R/W	0h	GPI0 Internal Pull-up Resistor Enable

3.31 R31 Register (Offset = 1Fh) [Reset = AAh]

R31 is shown in Table 3-33.

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Table 3-33. R31 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GPIO1_PULL_DN_EN	R/W	1h	GPIO1 Internal Pull-down Resistor Enable
6	GPIO0_PULL_UP_EN	R/W	0h	GPIO0 Internal Pull-up Resistor Enable
5	GPIO0_PULL_DN_EN	R/W	1h	GPIO0 Internal Pull-down Resistor Enable
4	GPI5_PULL_UP_EN	R/W	0h	GPI5 Internal Pull-up Resistor Enable
3	GPI5_PULL_DN_EN	R/W	1h	GPI5 Internal Pull-down Resistor Enable
2	GPI4_PULL_UP_EN	R/W	0h	GPI4 Internal Pull-up Resistor Enable
1	GPI4_PULL_DN_EN	R/W	1h	GPI4 Internal Pull-down Resistor Enable
0	GPI3_PULL_UP_EN	R/W	0h	GPI3 Internal Pull-up Resistor Enable

3.32 R32 Register (Offset = 20h) [Reset = 2Ah]

R32 is shown in Table 3-34.

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Table 3-34. R32 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GPIO0_NUM_IN_LVL	R/W	0h	GPIO0, Number of Input Voltage Levels. When GPIO0 is used as an input, this field configures GPIO0 to expect either 2-level or 3-level input signals. When "2-level" is selected, there is one input voltage decision theshold that splits the operational range of the pin into 2 ranges: LOW and HIGH. When "3-level" is selected, there are two input voltage decision thresholds that split the operational range of the pin into 3 ranges: LOW, MID, and HIGH. While GPIO0 is used as an output, this field is ignored. While GPIO0 is used for any input function that is not "Power-up OTP Page Selection" or "OTP Page Selection (Dynamic)", or if GPIO0 is assigned with the PWRGD/PWRDN# function, this field is ignored. 0h = 2-Level 1h = 3-Level
6	GPIO4_PULL_UP_EN	R/W	0h	GPIO4 Internal Pull-up Resistor Enable
5	GPIO4_PULL_DN_EN	R/W	1h	GPIO4 Internal Pull-down Resistor Enable
4	GPIO3_PULL_UP_EN	R/W	0h	GPIO3 Internal Pull-up Resistor Enable
3	GPIO3_PULL_DN_EN	R/W	1h	GPIO3 Internal Pull-down Resistor Enable
2	GPIO2_PULL_UP_EN	R/W	0h	GPIO2 Internal Pull-up Resistor Enable
1	GPIO2_PULL_DN_EN	R/W	1h	GPIO2 Internal Pull-down Resistor Enable
0	GPIO1_PULL_UP_EN	R/W	0h	GPIO1 Internal Pull-up Resistor Enable

3.33 R33 Register (Offset = 21h) [Reset = 00h]

R33 is shown in Table 3-35.

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Table 3-35. R33 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GPI3_LIVE_RB	R	0h	GPI3 Pin Live Value Readback
6	GPI2_LIVE_RB	R	0h	GPI2 Pin Live Value Readback
5	GPI1_LIVE_RB	R	0h	GPI1 Pin Live Value Readback
4	GPI0_LIVE_RB	R	0h	GPI0 Pin Live Value Readback
3-2	RESERVED	R	0h	Reserved
1	GPIO2_NUM_IN_LVL	R/W	0h	GPIO2, Number of Input Voltage Levels. When GPIO2 is used as an input, this field configures GPIO2 to expect either 2-level or 3-level input signals. When "2-level" is selected, there is one input voltage decision theshold that splits the operational range of the pin into 2 ranges: LOW and HIGH. When "3-level" is selected, there are two input voltage decision thresholds that split the operational range of the pin into 3 ranges: LOW, MID, and HIGH. While GPIO2 is used as an output, this field is ignored. While GPIO2 is used for any input function that is not "Power-up OTP Page Selection" or "OTP Page Selection (Dynamic)", or if GPIO0 is assigned with the PWRGD/PWRDN# function, this field is ignored. 0h = 2-Level 1h = 3-Level
0	GPIO1_NUM_IN_LVL	R/W	0h	GPIO1, Number of Input Voltage Levels. When GPIO1 is used as an input, this field configures GPIO1 to expect either 2-level or 3-level input signals. When "2-level" is selected, there is one input voltage decision theshold that splits the operational range of the pin into 2 ranges: LOW and HIGH. When "3-level" is selected, there are two input voltage decision thresholds that split the operational range of the pin into 3 ranges: LOW, MID, and HIGH. While GPIO1 is used as an output, this field is ignored. While GPIO1 is used for any input function that is not "Power-up OTP Page Selection" or "OTP Page Selection (Dynamic)", or if GPIO0 is assigned with the PWRGD/PWRDN# function, this field is ignored. 0h = 2-Level 1h = 3-Level

3.34 R34 Register (Offset = 22h) [Reset = 00h]

R34 is shown in Table 3-36.

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Table 3-36. R34 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	GPIO2_LIVE_RB	R	0h	GPIO2 Pin Live Value Readback 0h = 0: LOW 1h = 1: MID 3h = 3: HIGH
5-4	GPIO1_LIVE_RB	R	0h	GPIO1 Pin Live Value Readback 0h = 0: LOW 1h = 1: MID 3h = 3: HIGH
3-2	GPIO0_LIVE_RB	R	0h	GPIO0 Pin Live Value Readback 0h = 0: LOW 1h = 1: MID 3h = 3: HIGH
1	GPI5_LIVE_RB	R	0h	GPI5 Pin Live Value Readback
0	GPI4_LIVE_RB	R	0h	GPI4 Pin Live Value Readback

3.35 R35 Register (Offset = 23h) [Reset = 00h]

R35 is shown in Table 3-37.

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Table 3-37. R35 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6	GPIO4_GPO_VAL	R/W	0h	GPIO4 GPO Output Value. When GPIO4 is configured for the "GPO" function, the value in this register field determines whether the pin is driven LOW or HIGH. When GPIO4 is not configured for the "GPO" function, this register field is ignored. 0h = LOW 1h = HIGH
5	GPIO3_GPO_VAL	R/W	0h	GPIO3 GPO Output Value. When GPIO3 is configured for the "GPO" function, the value in this register field determines whether the pin is driven LOW or HIGH. When GPIO3 is not configured for the "GPO" function, this register field is ignored. 0h = LOW 1h = HIGH
4	GPIO2_GPO_VAL	R/W	0h	GPIO2 GPO Output Value. When GPIO2 is configured for the "GPO" function, the value in this register field determines whether the pin is driven LOW or HIGH. When GPIO2 is not configured for the "GPO" function, this register field is ignored. 0h = LOW 1h = HIGH
3	GPIO1_GPO_VAL	R/W	0h	GPIO1 GPO Output Value. When GPIO1 is configured for the "GPO" function, the value in this register field determines whether the pin is driven LOW or HIGH. When GPIO1 is not configured for the "GPO" function, this register field is ignored. 0h = LOW 1h = HIGH
2	GPIO0_GPO_VAL	R/W	0h	GPIO0 GPO Output Value. When GPIO0 is configured for the "GPO" function, the value in this register field determines whether the pin is driven LOW or HIGH. When GPIO0 is not configured for the "GPO" function, this register field is ignored. 0h = LOW 1h = HIGH
1	GPIO4_LIVE_RB	R	0h	GPIO4 Pin Live Value Readback
0	GPIO3_LIVE_RB	R	0h	GPIO3 Pin Live Value Readback

3.36 R36 Register (Offset = 24h) [Reset = 08h]

R36 is shown in Table 3-38.

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Table 3-38. R36 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	Reserved
5-3	GPI1_OE_GRP_SEL	R/W	1h	GPI1 Output Enable Group Select. When GPI1 is configured for the "Group Output Enable" function, this field determines which output enable group GPI1 will control. If GPI1 is not configured for the "Group Output Enable" function, this field is ignored. 0h = OE_GROUP_0 1h = OE_GROUP_1 2h = OE_GROUP_2 3h = OE_GROUP_3 4h = OE_GROUP_4
2-0	GPI0_OE_GRP_SEL	R/W	0h	GPI0 Output Enable Group Select. When GPI0 is configured for the "Group Output Enable" function, this field determines which output enable group GPI0 will control. If GPI0 is not configured for the "Group Output Enable" function, this field is ignored. 0h = OE_GROUP_0 1h = OE_GROUP_1 2h = OE_GROUP_2 3h = OE_GROUP_3 4h = OE_GROUP_4

3.37 R37 Register (Offset = 25h) [Reset = 1Ah]

R37 is shown in Table 3-39.

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Table 3-39. R37 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	Reserved
5-3	GPI3_OE_GRP_SEL	R/W	3h	GPI3 Output Enable Group Select. When GPI3 is configured for the "Group Output Enable" function, this field determines which output enable group GPI3 will control. If GPI3 is not configured for the "Group Output Enable" function, this field is ignored. 0h = OE_GROUP_0 1h = OE_GROUP_1 2h = OE_GROUP_2 3h = OE_GROUP_3 4h = OE_GROUP_4
2-0	GPI2_OE_GRP_SEL	R/W	2h	GPI2 Output Enable Group Select. When GPI2 is configured for the "Group Output Enable" function, this field determines which output enable group GPI2 will control. If GPI2 is not configured for the "Group Output Enable" function, this field is ignored. 0h = OE_GROUP_0 1h = OE_GROUP_1 2h = OE_GROUP_2 3h = OE_GROUP_3 4h = OE_GROUP_4

3.38 R38 Register (Offset = 26h) [Reset = 2Ch]

R38 is shown in Table 3-40.

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Table 3-40. R38 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	Reserved
5-3	GPI5_OE_GRP_SEL	R/W	5h	GPI5 Output Enable Group Select. When GPI5 is configured for the "Group Output Enable" function, this field determines which output enable group GPI5 will control. If GPI5 is not configured for the "Group Output Enable" function, this field is ignored. 0h = OE_GROUP_0 1h = OE_GROUP_1 2h = OE_GROUP_2 3h = OE_GROUP_3 4h = OE_GROUP_4 5h = OE_GROUP_5
2-0	GPI4_OE_GRP_SEL	R/W	4h	GPI4 Output Enable Group Select. When GPI4 is configured for the "Group Output Enable" function, this field determines which output enable group GPI4 will control. If GPI4 is not configured for the "Group Output Enable" function, this field is ignored. 0h = OE_GROUP_0 1h = OE_GROUP_1 2h = OE_GROUP_2 3h = OE_GROUP_3 4h = OE_GROUP_4

3.39 R39 Register (Offset = 27h) [Reset = 2Dh]

R39 is shown in Table 3-41.

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Table 3-41. R39 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	Reserved
5-3	GPIO1_OE_GRP_SEL	R/W	5h	GPIO1 Output Enable Group Select. When GPIO1 is configured for the "Group Output Enable" function, this field determines which output enable group GPIO1 will control. If GPIO1 is not configured for the "Group Output Enable" function, this field is ignored. 0h = OE_GROUP_0 1h = OE_GROUP_1 2h = OE_GROUP_2 3h = OE_GROUP_3 4h = OE_GROUP_4 5h = OE_GROUP_7
2-0	GPIO0_OE_GRP_SEL	R/W	5h	GPIO0 Output Enable Group Select. When GPIO0 is configured for the "Group Output Enable" function, this field determines which output enable group GPIO0 will control. If GPIO0 is not configured for the "Group Output Enable" function, this field is ignored. 0h = OE_GROUP_0 1h = OE_GROUP_1 2h = OE_GROUP_2 3h = OE_GROUP_3 4h = OE_GROUP_4 5h = OE_GROUP_6

3.40 R40 Register (Offset = 28h) [Reset = 2Dh]

R40 is shown in Table 3-42.

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Table 3-42. R40 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	Reserved
5-3	GPIO3_OE_GRP_SEL	R/W	5h	GPIO3 Output Enable Group Select. When GPIO3 is configured for the "Group Output Enable" function, this field determines which output enable group GPIO3 will control. If GPIO3 is not configured for the "Group Output Enable" function, this field is ignored. 0h = OE_GROUP_0 1h = OE_GROUP_1 2h = OE_GROUP_2 3h = OE_GROUP_3 4h = OE_GROUP_4 5h = OE_GROUP_9
2-0	GPIO2_OE_GRP_SEL	R/W	5h	GPIO2 Output Enable Group Select. When GPIO2 is configured for the "Group Output Enable" function, this field determines which output enable group GPIO2 will control. If GPIO2 is not configured for the "Group Output Enable" function, this field is ignored. 0h = OE_GROUP_0 1h = OE_GROUP_1 2h = OE_GROUP_2 3h = OE_GROUP_3 4h = OE_GROUP_4 5h = OE_GROUP_8

3.41 R41 Register (Offset = 29h) [Reset = 05h]

R41 is shown in Table 3-43.

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Table 3-43. R41 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GPIO4_OUT_SIG_TYPE	R/W	0h	GPIO4 Output Signal Type. When GPIO4 is used as an output, this field selects between CMOS and Open-Drain output signal types. When GPIO4 is used as an input, the value of this field is ignored. 0h = LVCMOS 1h = Open-Drain
6	GPIO3_OUT_SIG_TYPE	R/W	0h	GPIO3 Output Signal Type. When GPIO3 is used as an output, this field selects between CMOS and Open-Drain output signal types. When GPIO3 is used as an input, the value of this field is ignored. 0h = LVCMOS 1h = Open-Drain
5	GPIO2_OUT_SIG_TYPE	R/W	0h	GPIO2 Output Signal Type. When GPIO2 is used as an output, this field selects between CMOS and Open-Drain output signal types. When GPIO2 is used as an input, the value of this field is ignored. 0h = LVCMOS 1h = Open-Drain
4	GPIO1_OUT_SIG_TYPE	R/W	0h	GPIO1 Output Signal Type. When GPIO1 is used as an output, this field selects between CMOS and Open-Drain output signal types. When GPIO1 is used as an input, the value of this field is ignored. 0h = LVCMOS 1h = Open-Drain
3	GPIO0_OUT_SIG_TYPE	R/W	0h	GPIO0 Output Signal Type. When GPIO0 is used as an output, this field selects between CMOS and Open-Drain output signal types. When GPIO0 is used as an input, the value of this field is ignored. 0h = LVCMOS 1h = Open-Drain
2-0	GPIO4_OE_GRP_SEL	R/W	5h	GPIO4 Output Enable Group Select. When GPIO4 is configured for the "Group Output Enable" function, this field determines which output enable group GPIO4 will control. If GPIO4 is not configured for the "Group Output Enable" function, this field is ignored. 0h = OE_GROUP_0 1h = OE_GROUP_1 2h = OE_GROUP_2 3h = OE_GROUP_3 4h = OE_GROUP_4 5h = OE_GROUP_10

3.42 R42 Register (Offset = 2Ah) [Reset = 00h]

R42 is shown in Table 3-44.

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Table 3-44. R42 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	Reserved
5-4	IN2_RCVR_FMT	R/W	0h	IN2 Input Receiver Format. This field configures the IN2 receiver for a specific input clock format, with options of: N/A, LVCMOS IN2_P, LVCMOS IN2_N, and Differential IN2. 0h = N/A (IN2 Unused) 1h = LVCMOS IN2_P 2h = LVCMOS IN2_N 3h = Differential IN2
3-2	IN1_RCVR_FMT	R/W	0h	IN1 Input Receiver Format. This field configures the IN1 receiver for a specific input clock format, with options of: N/A, LVCMOS IN1_P, LVCMOS IN1_N, and Differential IN1. 0h = N/A (IN1 Unused) 1h = LVCMOS IN1_P 2h = LVCMOS IN1_N 3h = Differential IN1
1-0	IN0_RCVR_FMT	R/W	0h	IN0 Input Receiver Format. This field configures the IN0 receiver for a specific input clock format, with options of: N/A, LVCMOS IN0_P, LVCMOS IN0_N, and Differential IN0. 0h = N/A (IN0 Unused) 1h = LVCMOS IN0_P 2h = LVCMOS IN0_N 3h = Differential IN0

3.43 R43 Register (Offset = 2Bh) [Reset = 00h]

R43 is shown in Table 3-45.

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Table 3-45. R43 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	Reserved
5-3	IN1_TERMINATION_SEL	R/W	0h	IN1 Termination Select. 0h = None, DC; No termination, no internal bias (LVCMOS inputs, LP-HCSL inputs, and other DC-coupled inputs that do not require integrated input termination) 1h = None, AC; No termination, with internal bias (AC-coupled inputs that do not require integrated input termination) 2h = 50 Ω to GND; 50 Ω to GND on both P and N (HCSL inputs that require 100 Ω differential impedance and other DC-coupled inputs that require 50 Ω to GND) 3h = 42.5 Ω to GND; 42.5 Ω to GND on both P and N (HCSL inputs that require 85 Ω differential impedance and other DC-coupled inputs that require 42.5 Ω to GND) 4h = 100 Ω P to N; 100 Ω between P and N (DC-LVDS) 5h = 50 Ω to bias; 50 Ω to internal bias on both P and N (AC-LVDS and other AC-coupled inputs that require 50 Ω to AC-GND) 6h = 50 Ω to DC and GND; 50 Ω to DC on both P and N. DC is 50 Ω to GND. (DC-LVPECL) 7h = 42.5 Ω to bias; 42.5 Ω to internal bias on both P and N (AC-coupled inputs that require 42.5 Ω to AC-GND)
2-0	IN0_TERMINATION_SEL	R/W	0h	IN0 Termination Select. 0h = None, DC; No termination, no internal bias (LVCMOS inputs, LP-HCSL inputs, and other DC-coupled inputs that do not require integrated input termination) 1h = None, AC; No termination, with internal bias (AC-coupled inputs that do not require integrated input termination) 2h = 50 Ω to GND; 50 Ω to GND on both P and N (HCSL inputs that require 100 Ω differential impedance and other DC-coupled inputs that require 50 Ω to GND) 3h = 42.5 Ω to GND; 42.5 Ω to GND on both P and N (HCSL inputs that require 85 Ω differential impedance and other DC-coupled inputs that require 42.5 Ω to GND) 4h = 100 Ω P to N; 100 Ω between P and N (DC-LVDS) 5h = 50 Ω to bias; 50 Ω to internal bias on both P and N (AC-LVDS and other AC-coupled inputs that require 50 Ω to AC-GND) 6h = 50 Ω to DC and GND; 50 Ω to DC on both P and N. DC is 50 Ω to GND. (DC-LVPECL) 7h = 42.5 Ω to bias; 42.5 Ω to internal bias on both P and N (AC-coupled inputs that require 42.5 Ω to AC-GND)

3.44 R44 Register (Offset = 2Ch) [Reset = 00h]

R44 is shown in Table 3-46.

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Table 3-46. R44 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	IN1_LOS_THRESH	R/W	0h	IN1 Loss of Signal Detector Threshold. Selects the minimum valid frequency for IN1. If IN1 is below this frequency, LOS will be asserted. 0h = 1 MHz 1h = 25 MHz
6	IN0_LOS_THRESH	R/W	0h	IN0 Loss of Signal Detector Threshold. Selects the minimum valid frequency for IN0. If IN0 is below this frequency, LOS will be asserted. 0h = 1 MHz 1h = 25 MHz
5	IN2_LOS_EN	R/W	0h	0x0 = Disables Loss-Of-Signal 0x1 = Enables Loss-Of-Signal detector
4	IN1_LOS_EN	R/W	0h	0x0 = Disables Loss-Of-Signal 0x1 = Enables Loss-Of-Signal detector
3	IN0_LOS_EN	R/W	0h	0x0 = Disables Loss-Of-Signal 0x1 = Enables Loss-Of-Signal detector
2-0	IN2_TERMINATION_SEL	R/W	0h	IN2 Termination Select. 0h = None, DC; No termination, no internal bias (LVCMOS inputs, LP-HCSL inputs, and other DC-coupled inputs that do not require integrated input termination) 1h = None, AC; No termination, with internal bias (AC-coupled inputs that do not require integrated input termination) 2h = 50 Ω to GND; 50 Ω to GND on both P and N (HCSL inputs that require 100 Ω differential impedance and other DC-coupled inputs that require 50 Ω to GND) 3h = 42.5 Ω to GND; 42.5 Ω to GND on both P and N (HCSL inputs that require 85 Ω differential impedance and other DC-coupled inputs that require 42.5 Ω to GND) 4h = 100 Ω P to N; 100 Ω between P and N (DC-LVDS) 5h = 50 Ω to bias; 50 Ω to internal bias on both P and N (AC-LVDS and other AC-coupled inputs that require 50 Ω to AC-GND) 6h = 50 Ω to DC and GND; 50 Ω to DC on both P and N. DC is 50 Ω to GND. (DC-LVPECL) 7h = 42.5 Ω to bias; 42.5 Ω to internal bias on both P and N (AC-coupled inputs that require 42.5 Ω to AC-GND)

3.45 R45 Register (Offset = 2Dh) [Reset = 00h]

R45 is shown in Table 3-47.

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Table 3-47. R45 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	PERST_BUF_IN0_STS	R	0h	IN0 Buffer Mode Status. This field indicates whether or not one or more output banks are currently using Buffer Mode with IN0. 0h = Inactive 1h = Active
6-5	PERST_BUF_IN2	R/W	0h	IN2 Buffer Mode Select. Selects if and how Buffer Mode with IN2 is activated. For "Disabled", IN2 is unavailable for clock source selection by banks using Buffer Mode. For any bank where BANKx_BUF_MODE_CLK_SEL is set to "Enabled, Select IN2", the normal clock selection (BANKx_CLK_SEL) will be used instead. For "Edge-Triggered (Enabled on PERST_IN2# Deassertion)", Buffer Mode with IN2 is activated on the first deassertion of the PERST_IN2# signal. For any bank where BANKx_BUF_MODE_CLK_SEL is set to "Enabled, Select IN2", IN2 will be selected when Buffer Mode becomes active. Until that point, the normal clock selection (BANKx_CLK_SEL) will be used. For "Level-Triggered (Enable/Disable Follows PERST_IN2#)", Buffer Mode with IN2 is activate whenever the PERST_IN2# signal is deasserted. For any bank where BANKx_BUF_MODE_CLK_SEL is set to "Enabled, Select IN2", IN2 will be selected whenever Buffer Mode is active. At all other times, the normal clock selection (BANKx_CLK_SEL) will be used. For "Always On", Buffer Mode with IN2 is always active. For any bank where BANKx_BUF_MODE_CLK_SEL is set to "Enabled, Select IN2", IN2 will be selected at all times. 0h = Disabled 1h = Edge; Edge-Triggered (PERST_IN0# Deassertion) 2h = Level; Level-Triggered (Follows PERST_IN0#) 3h = Enabled
4-3	PERST_BUF_IN1	R/W	0h	IN1 Buffer Mode Select. Selects if and how Buffer Mode with IN1 is activated. For "Disabled", IN1 is unavailable for clock source selection by banks using Buffer Mode. For any bank where BANKx_BUF_MODE_CLK_SEL is set to "Enabled, Select IN1", the normal clock selection (BANKx_CLK_SEL) will be used instead. For "Edge-Triggered (Enabled on PERST_IN1# Deassertion)", Buffer Mode with IN1 is activated on the first deassertion of the PERST_IN1# signal. For any bank where BANKx_BUF_MODE_CLK_SEL is set to "Enabled, Select IN1", IN1 will be selected when Buffer Mode becomes active. Until that point, the normal clock selection (BANKx_CLK_SEL) will be used. For "Level-Triggered (Enable/Disable Follows PERST_IN1#)", Buffer Mode with IN1 is activate whenever the PERST_IN1# signal is deasserted. For any bank where BANKx_BUF_MODE_CLK_SEL is set to "Enabled, Select IN1", IN1 will be selected whenever Buffer Mode is active. At all other times, the normal clock selection (BANKx_CLK_SEL) will be used. For "Always On", Buffer Mode with IN1 is always active. For any bank where BANKx_BUF_MODE_CLK_SEL is set to "Enabled, Select IN1", IN1 will be selected at all times. 0h = Disabled 1h = Edge; Edge-Triggered (PERST_IN0# Deassertion) 2h = Level; Level-Triggered (Follows PERST_IN0#) 3h = Enabled

Table 3-47. R45 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-1	PERST_BUF_IN0	R/W	0h	IN0 Buffer Mode Select. Selects if and how Buffer Mode with IN0 is activated. For "Disabled", IN0 is unavailable for clock source selection by banks using Buffer Mode. For any bank where BANKx_BUF_MODE_CLK_SEL is set to "Enabled, Select IN0", the normal clock selection (BANKx_CLK_SEL) will be used instead. For "Edge-Triggered (Enabled on PERST_IN0# Deassertion)", Buffer Mode with IN0 is activated on the first deassertion of the PERST_IN0# signal. For any bank where BANKx_BUF_MODE_CLK_SEL is set to "Enabled, Select IN0", IN0 will be selected when Buffer Mode becomes active. Until that point, the normal clock selection (BANKx_CLK_SEL) will be used. For "Level-Triggered (Enable/Disable Follows PERST_IN0#)", Buffer Mode with IN0 is activate whenever the PERST_IN0# signal is deasserted. For any bank where BANKx_BUF_MODE_CLK_SEL is set to "Enabled, Select IN0", IN0 will be selected whenever Buffer Mode is active. At all other times, the normal clock selection (BANKx_CLK_SEL) will be used. For "Always On", Buffer Mode with IN0 is always active. For any bank where BANKx_BUF_MODE_CLK_SEL is set to "Enabled, Select IN0", IN0 will be selected at all times. 0h = Disabled 1h = Edge; Edge-Triggered (PERST_IN0# Deassertion) 2h = Level; Level-Triggered (Follows PERST_IN0#) 3h = Enabled
0	IN2_LOS_THRESH	R/W	0h	IN2 Loss of Signal Detector Threshold. Selects the minimum valid frequency for IN2. If IN2 is below this frequency, LOS will be asserted. 0h = 1 MHz 1h = 25 MHz

3.46 R46 Register (Offset = 2Eh) [Reset = 00h]

R46 is shown in Table 3-48.

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Table 3-48. R46 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0h	Reserved
4	PERST_BUF_IN2_LOS_EN	R/W	0h	IN2 Buffer Mode, Loss-of-Signal Enable. This field determines whether or not clock selection for banks using Buffer Mode with IN2 is dependent on the selected the IN2_LOS status. When set to 0, Buffer Mode with IN2 can become and remain active, regardless of the IN2_LOS status. When set to 1, Buffer Mode with IN2 can only become active while IN2_LOS is deasserted, and if IN2_LOS is asserted while Buffer Mode with IN2 is already active, Buffer Mode with IN2 will be deactivated, and all deactivated banks will switch back to the normal clock selection (BANKx_CLK_SEL).
3	PERST_BUF_IN1_LOS_EN	R/W	0h	IN1 Buffer Mode, Loss-of-Signal Enable. This field determines whether or not clock selection for banks using Buffer Mode with IN1 is dependent on the selected the IN1_LOS status. When set to 0, Buffer Mode with IN1 can become and remain active, regardless of the IN1_LOS status. When set to 1, Buffer Mode with IN1 can only become active while IN1_LOS is deasserted, and if IN1_LOS is asserted while Buffer Mode with IN1 is already active, Buffer Mode with IN1 will be deactivated, and all deactivated banks will switch back to the normal clock selection (BANKx_CLK_SEL).
2	PERST_BUF_IN0_LOS_EN	R/W	0h	IN0 Buffer Mode, Loss-of-Signal Enable. This field determines whether or not clock selection for banks using Buffer Mode with IN0 is dependent on the selected the IN0_LOS status. When set to 0, Buffer Mode with IN0 can become and remain active, regardless of the IN0_LOS status. When set to 1, Buffer Mode with IN0 can only become active while IN0_LOS is deasserted, and if IN0_LOS is asserted while Buffer Mode with IN0 is already active, Buffer Mode with IN0 will be deactivated, and all deactivated banks will switch back to the normal clock selection (BANKx_CLK_SEL).
1	PERST_BUF_IN2_STS	R	0h	IN2 Buffer Mode Status. This field indicates whether or not one or more output banks are currently using Buffer Mode with IN2. 0h = Inactive 1h = Active
0	PERST_BUF_IN1_STS	R	0h	IN1 Buffer Mode Status. This field indicates whether or not one or more output banks are currently using Buffer Mode with IN1. 0h = Inactive 1h = Active

3.47 R47 Register (Offset = 2Fh) [Reset = 0Ch]

R47 is shown in Table 3-49.

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Table 3-49. R47 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6-0	FOD0_N_DIV	R/W	Ch	FOD0 Divide Ratio, Integer Part. This field, along with FOD0_NUM, sets the divide ratio of FOD0, which divides the BAW oscillator clock down to a clock with a frequency ranging between 100MHz and 400MHz. This is the first of up to three stages of clock division for output clocks originating from the BAW oscillator. Write FOD0_CFG_UPDATE to 0x1 for this value to take effect.

3.48 R48 Register (Offset = 30h) [Reset = 0Ch]

R48 is shown in Table 3-50.

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Table 3-50. R48 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6-0	FOD1_N_DIV	R/W	Ch	FOD1 Divide Ratio, Integer Part. This field, along with FOD1_NUM, sets the divide ratio of FOD1, which divides the BAW oscillator clock down to a clock with a frequency ranging between 100MHz and 400MHz. This is the first of up to three stages of clock division for output clocks originating from the BAW oscillator. Write FOD1_CFG_UPDATE to 0x1 for this value to take effect.

3.49 R49 Register (Offset = 31h) [Reset = 8Fh]

R49 is shown in Table 3-51.

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Table 3-51. R49 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	FOD0_NUM[7:0]	R/W	8Fh	FOD0 Divide Ratio, Fractional Part. This field, along with FOD0_N_DIV, sets the divide ratio of FOD0, which divides the BAW oscillator clock down to a clock with a frequency ranging between 100MHz and 400MHz. This is the first of up to three stages of clock division for output clocks originating from the BAW oscillator. Write FOD0_CFG_UPDATE to 0x1 for this value to take effect.

3.50 R50 Register (Offset = 32h) [Reset = C2h]

R50 is shown in Table 3-52.

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Table 3-52. R50 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	FOD0_NUM[15:8]	R/W	C2h	FOD0 Divide Ratio, Fractional Part. This field, along with FOD0_N_DIV, sets the divide ratio of FOD0, which divides the BAW oscillator clock down to a clock with a frequency ranging between 100MHz and 400MHz. This is the first of up to three stages of clock division for output clocks originating from the BAW oscillator. Write FOD0_CFG_UPDATE to 0x1 for this value to take effect.

3.51 R51 Register (Offset = 33h) [Reset = 55h]

R51 is shown in Table 3-53.

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Table 3-53. R51 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	FOD0_NUM[23:16]	R/W	55h	FOD0 Divide Ratio, Fractional Part. This field, along with FOD0_N_DIV, sets the divide ratio of FOD0, which divides the BAW oscillator clock down to a clock with a frequency ranging between 100MHz and 400MHz. This is the first of up to three stages of clock division for output clocks originating from the BAW oscillator. Write FOD0_CFG_UPDATE to 0x1 for this value to take effect.

3.52 R52 Register (Offset = 34h) [Reset = 8Fh]

R52 is shown in Table 3-54.

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Table 3-54. R52 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	FOD1_NUM[7:0]	R/W	8Fh	FOD1 Divide Ratio, Fractional Part. This field, along with FOD1_N_DIV, sets the divide ratio of FOD1, which divides the BAW oscillator clock down to a clock with a frequency ranging between 100MHz and 400MHz. This is the first of up to three stages of clock division for output clocks originating from the BAW oscillator. Write FOD1_CFG_UPDATE to 0x1 for this value to take effect.

3.53 R53 Register (Offset = 35h) [Reset = C2h]

R53 is shown in Table 3-55.

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Table 3-55. R53 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	FOD1_NUM[15:8]	R/W	C2h	FOD1 Divide Ratio, Fractional Part. This field, along with FOD1_N_DIV, sets the divide ratio of FOD1, which divides the BAW oscillator clock down to a clock with a frequency ranging between 100MHz and 400MHz. This is the first of up to three stages of clock division for output clocks originating from the BAW oscillator. Write FOD1_CFG_UPDATE to 0x1 for this value to take effect.

3.54 R54 Register (Offset = 36h) [Reset = 55h]

R54 is shown in Table 3-56.

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Table 3-56. R54 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	FOD1_NUM[23:16]	R/W	55h	FOD1 Divide Ratio, Fractional Part. This field, along with FOD1_N_DIV, sets the divide ratio of FOD1, which divides the BAW oscillator clock down to a clock with a frequency ranging between 100MHz and 400MHz. This is the first of up to three stages of clock division for output clocks originating from the BAW oscillator. Write FOD1_CFG_UPDATE to 0x1 for this value to take effect.

3.55 R55 Register (Offset = 37h) [Reset = 08h]

R55 is shown in Table 3-57.

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Table 3-57. R55 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	FOD1_CFG_UPDATE	R/W	0h	FOD1 Configuration Update. To change the frequency of FOD1, first write FOD1_N_DIV and FOD1_NUM with the desired values (writing these fields does not cause the new values to take effect). Then, when ready for the new frequency configuration to take effect, write this field with 0x1.
6	FOD0_CFG_UPDATE	R/W	0h	FOD0 Configuration Update. To change the frequency of FOD0, first write FOD0_N_DIV and FOD0_NUM with the desired values (writing these fields does not cause the new values to take effect). Then, when ready for the new frequency configuration to take effect, write this field with 0x1.
5-3	PATH1_DIV	R/W	1h	FOD PATH1 Post-divider Divide Ratio. This field sets the divide ratio of the FOD PATH1 Post-divider, which divides an FOD clock down to a clock with a frequency ranging between 2.5MHz and 200MHz. This is the second of up to three stages of clock division for output clocks originating from the BAW oscillator. When PATH1_EDGE_COMB_EN is set to 0x1 (FOD PATH1 is configured for the using the Edge Combiner), this field must be set to 0x0. 0h = Disabled; When using the edge combiner, set this field to Disabled 1h = FOD / 2 2h = FOD / 4 3h = FOD / 6 4h = FOD / 8 5h = FOD / 10 6h = FOD / 20 7h = FOD / 40
2-0	PATH0_DIV	R/W	0h	FOD PATH0 Post-divider Divide Ratio. This field sets the divide ratio of the FOD PATH0 Post-divider, which divides an FOD clock down to a clock with a frequency ranging between 2.5MHz and 200MHz. This is the second of up to three stages of clock division for output clocks originating from the BAW oscillator. When PATH0_EDGE_COMB_EN is set to 0x1 (FOD PATH0 is configured for the using the Edge Combiner), this field must be set to 0x0. 0h = Disabled; When using the edge combiner, set this field to Disabled 1h = FOD / 2 2h = FOD / 4 3h = FOD / 6 4h = FOD / 8 5h = FOD / 10 6h = FOD / 20 7h = FOD / 40

3.56 R57 Register (Offset = 39h) [Reset = 00h]

R57 is shown in Table 3-58.

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Table 3-58. R57 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6-0	FOD_PH_OFFSET_N_DIV	R/W	0h	FOD Phase Offset, Integer Part. The full phase offset (delay) of the FOD indicated by FOD_PH_OFFSET_FOD_SEL (FODx) with respect to the other FOD, is defined through 2 fields: FOD_PH_OFFSET_N_DIV and FOD_PH_OFFSET_NUM. The values of these fields are determined through the follwoing equation: 400ps * (FOD_PH_OFFSET_N_DIV + (FOD_PH_OFFSET_NUM / 2^{16})) = FODx Offset (ps) Phase offsets are applied at power-up, and subsequently upon writing FOD_PH_OFFSET_SHIFT_NOW with 0x1.

3.57 R58 Register (Offset = 3Ah) [Reset = 00h]

R58 is shown in Table 3-59.

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Table 3-59. R58 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	FOD_PH_OFFSET_NUM[7:0]	R/W	0h	FOD Phase Offset, Fractional Part (Byte 0). See FOD_PH_OFFSET_N_DIV.

3.58 R59 Register (Offset = 3Bh) [Reset = 00h]

R59 is shown in Table 3-60.

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Table 3-60. R59 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	FOD_PH_OFFSET_NUM[15:8]	R/W	0h	FOD Phase Offset, Fractional Part (Byte 0). See FOD_PH_OFFSET_N_DIV.

3.59 R60 Register (Offset = 3Ch) [Reset = 00h]

R60 is shown in Table 3-61.

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Table 3-61. R60 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6-4	FOD0_SSC_CONFIG_SEL	R/W	0h	FOD0 SSC Setting. Selects between custom SSC control and 4 different SSC presets. 0h = Custom 1h = -0.1% Down-spread 2h = -0.25% Down-spread 3h = -0.3% Down-spread 4h = -0.5% Down-spread
3	FOD0_SSC_MOD_TYPE	R/W	0h	FOD0 SSC Modulation Type. Selectable between down-spread and center-spread 0h = Down-spread 1h = Center-spread
2	FOD0_SSC_EN	R/W	0h	FOD0 SSC Enable. Enables SSC on output clocks sourced from FOD0.
1	FOD_PH_OFFSET_FOD_SEL	R/W	0h	FOD Phase Offset FOD Select. Determines which FOD will be delayed in order to produce a phase offset between the two FODs. 0h = FOD0 1h = FOD1
0	FOD_PH_OFFSET_SHIFT_NOW	R/W	0h	FOD Phase Offset Shift Now. When written with 0x1, the FOD indicated by FOD_PH_OFFSET_FOD_SEL will be delayed with respect to the other FOD, according to the values of FOD_PH_OFFSET_N_DIV and FOD_PH_OFFSET_NUM.

3.60 R61 Register (Offset = 3Dh) [Reset = 00h]

R61 is shown in Table 3-62.

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Table 3-62. R61 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	FOD0_SSC_STEPS[7:0]	R/W	0h	FOD0 SSC Steps, Byte 0. Sets the number of frequency steps in each segment of the triangular modulation profile. For down-spread, this is the number of frequency steps between the nominal frequency and maximum down-spread. For center-spread, this is the number of frequency steps between the nominal frequency and both maximum down-spread and maximum up-spread. This should be calculated based on the FOD0 frequency and the desired SSC modulation freqency.

3.61 R62 Register (Offset = 3Eh) [Reset = 00h]

R62 is shown in Table 3-63.

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Table 3-63. R62 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0h	Reserved
4-0	FOD0_SSC_STEPS[12:8]	R/W	0h	FOD0 SSC Steps, Byte 0. Sets the number of frequency steps in each segment of the triangular modulation profile. For down-spread, this is the number of frequency steps between the nominal frequency and maximum down-spread. For center-spread, this is the number of frequency steps between the nominal frequency and both maximum down-spread and maximum up-spread. This should be calculated based on the FOD0 frequency and the desired SSC modulation freqency.

3.62 R63 Register (Offset = 3Fh) [Reset = 00h]

R63 is shown in Table 3-64.

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Table 3-64. R63 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	FOD0_DCO_STEP_SIZE[7:0]	R/W	0h	FOD0 DCO Step Size, Byte 0. Sets the size of the FOD0 frequency steps used for both SSC and DCO. For SSC, this should be calculated based on the number of SSC steps, the SSC modulation type, and the desired SSC magnitude. For DCO, this should be calculated based on the FOD0 frequency and the desired PPM change per DCO adjustment.

3.63 R64 Register (Offset = 40h) [Reset = 00h]

R64 is shown in Table 3-65.

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Table 3-65. R64 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	FOD0_DCO_STEP_SIZE[15:8]	R/W	0h	FOD0 DCO Step Size, Byte 0. Sets the size of the FOD0 frequency steps used for both SSC and DCO. For SSC, this should be calculated based on the number of SSC steps, the SSC modulation type, and the desired SSC magnitude. For DCO, this should be calculated based on the FOD0 frequency and the desired PPM change per DCO adjustment.

3.64 R65 Register (Offset = 41h) [Reset = 00h]

R65 is shown in Table 3-66.

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Table 3-66. R65 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0h	Reserved
4-2	FOD1_SSC_CONFIG_SEL	R/W	0h	FOD1 SSC Setting. Selects between custom SSC control and 4 different SSC presets. 0h = Custom 1h = -0.1% Down-spread 2h = -0.25% Down-spread 3h = -0.3% Down-spread 4h = -0.5% Down-spread
1	FOD1_SSC_MOD_TYPE	R/W	0h	FOD1 SSC Modulation Type. Selectable between down-spread and center-spread 0h = Down-spread 1h = Center-spread
0	FOD1_SSC_EN	R/W	0h	FOD1 SSC Enable. Enables SSC on output clocks sourced from FOD1.

3.65 R66 Register (Offset = 42h) [Reset = 00h]

R66 is shown in Table 3-67.

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Table 3-67. R66 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	FOD1_SSC_STEPS[7:0]	R/W	0h	FOD1 SSC Steps, Byte 0. Sets the number of frequency steps in each segment of the triangular modulation profile. For down-spread, this is the number of frequency steps between the nominal frequency and maximum down-spread. For center-spread, this is the number of frequency steps between the nominal frequency and both maximum down-spread and maximum up-spread. This should be calculated based on the FOD1 frequency and the desired SSC modulation freqency.

3.66 R67 Register (Offset = 43h) [Reset = 00h]

R67 is shown in Table 3-68.

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Table 3-68. R67 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0h	Reserved
4-0	FOD1_SSC_STEPS[12:8]	R/W	0h	FOD1 SSC Steps, Byte 0. Sets the number of frequency steps in each segment of the triangular modulation profile. For down-spread, this is the number of frequency steps between the nominal frequency and maximum down-spread. For center-spread, this is the number of frequency steps between the nominal frequency and both maximum down-spread and maximum up-spread. This should be calculated based on the FOD1 frequency and the desired SSC modulation freqency.

3.67 R68 Register (Offset = 44h) [Reset = 00h]

R68 is shown in Table 3-69.

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Table 3-69. R68 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	FOD1_DCO_STEP_SIZE[7:0]	R/W	0h	FOD1 DCO Step Size, Byte 0. Sets the size of the FOD0 frequency steps used for both SSC and DCO. For SSC, this should be calculated based on the number of SSC steps, the SSC modulation type, and the desired SSC magnitude. For DCO, this should be calculated based on the FOD1 frequency and the desired PPM change per DCO adjustment.

3.68 R69 Register (Offset = 45h) [Reset = 00h]

R69 is shown in Table 3-70.

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Table 3-70. R69 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	FOD1_DCO_STEP_SIZE[15:8]	R/W	0h	FOD1 DCO Step Size, Byte 0. Sets the size of the FOD0 frequency steps used for both SSC and DCO. For SSC, this should be calculated based on the number of SSC steps, the SSC modulation type, and the desired SSC magnitude. For DCO, this should be calculated based on the FOD1 frequency and the desired PPM change per DCO adjustment.

3.69 R70 Register (Offset = 46h) [Reset = 00h]

R70 is shown in Table 3-71.

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Table 3-71. R70 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	Reserved
5	FOD1_DCO_DEC	R/W1C	0h	FOD1 DCO Increment. With FOD1_DCO_EN set to 0x1, writing a 1 to this field will cause the FOD1 frequency to increase. If FOD1_DCO_EN is set to 0x1, any writes to this field will be ignored.
4	FOD1_DCO_INC	R/W1C	0h	FOD1 DCO Increment. With FOD1_DCO_EN set to 0x1, writing a 1 to this field will cause the FOD1 frequency to increase. If FOD1_DCO_EN is set to 0x1, any writes to this field will be ignored.
3	FOD1_DCO_EN	R/W	0h	FOD1 DCO Enable. Enables DCO on output clocks driven by FOD1.
2	FOD0_DCO_DEC	R/W1C	0h	FOD0 DCO Increment. With FOD0_DCO_EN set to 0x1, writing a 1 to this field will cause the FOD0 frequency to increase. If FOD0_DCO_EN is set to 0x1, any writes to this field will be ignored.
1	FOD0_DCO_INC	R/W1C	0h	FOD0 DCO Increment. With FOD0_DCO_EN set to 0x1, writing a 1 to this field will cause the FOD0 frequency to increase. If FOD0_DCO_EN is set to 0x1, any writes to this field will be ignored.
0	FOD0_DCO_EN	R/W	0h	FOD0 DCO Enable. Enables DCO on output clocks driven by FOD0.

3.70 R71 Register (Offset = 47h) [Reset = 00h]

R71 is shown in Table 3-72.

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Table 3-72. R71 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	FOD0_DCO_STEPS_STAT[7:0]	R	0h	FOD0 DCO Steps Status, Byte 0. Reading this field returns the numer of steps that the FOD0 frequency has been adjusted by.

3.71 R72 Register (Offset = 48h) [Reset = 00h]

R72 is shown in Table 3-73.

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Table 3-73. R72 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	FOD0_DCO_STEPS_STAT[15:8]	R	0h	FOD0 DCO Steps Status, Byte 0. Reading this field returns the numer of steps that the FOD0 frequency has been adjusted by.

3.72 R73 Register (Offset = 49h) [Reset = 00h]

R73 is shown in Table 3-74.

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Table 3-74. R73 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	FOD1_DCO_STEPS_STAT[7:0]	R	0h	FOD1 DCO Steps Status, Byte 0. Reading this field returns the numer of steps that the FOD1 frequency has been adjusted by.

3.73 R74 Register (Offset = 4Ah) [Reset = 00h]

R74 is shown in Table 3-75.

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Table 3-75. R74 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	FOD1_DCO_STEPS_STAT[15:8]	R	0h	FOD1 DCO Steps Status, Byte 0. Reading this field returns the numer of steps that the FOD1 frequency has been adjusted by.

3.74 R75 Register (Offset = 4Bh) [Reset = 00h]

R75 is shown in Table 3-76.

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Table 3-76. R75 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6-0	FOD0_DCO_N_DIV_STAT	R	0h	FOD0 DCO Integer Readback. Reading this value returns the value of the FOD0 divisor's integer portion, after it has been adjusted by the DCO logic.

3.75 R76 Register (Offset = 4Ch) [Reset = 00h]

R76 is shown in Table 3-77.

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Table 3-77. R76 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	FOD0_DCO_NUM_STAT[7:0]	R	0h	FOD0 DCO Numerator Readback, Byte 0. Reading this value returns the value of the FOD0 divisor's fractional portion, after it has been adjusted by the DCO logic.

3.76 R77 Register (Offset = 4Dh) [Reset = 00h]

R77 is shown in Table 3-78.

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Table 3-78. R77 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	FOD0_DCO_NUM_STAT[15:8]	R	0h	FOD0 DCO Numerator Readback, Byte 0. Reading this value returns the value of the FOD0 divisor's fractional portion, after it has been adjusted by the DCO logic.

3.77 R78 Register (Offset = 4Eh) [Reset = 00h]

R78 is shown in Table 3-79.

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Table 3-79. R78 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	FOD0_DCO_NUM_STAT[23:16]	R	0h	FOD0 DCO Numerator Readback, Byte 0. Reading this value returns the value of the FOD0 divisor's fractional portion, after it has been adjusted by the DCO logic.

3.78 R79 Register (Offset = 4Fh) [Reset = 00h]

R79 is shown in Table 3-80.

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Table 3-80. R79 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6-0	FOD1_DCO_N_DIV_STAT	R	0h	FOD1 DCO Integer Readback. Reading this value returns the value of the FOD1 divisor's integer portion, after it has been adjusted by the DCO logic.

3.79 R80 Register (Offset = 50h) [Reset = 00h]

R80 is shown in Table 3-81.

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Table 3-81. R80 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	FOD1_DCO_NUM_STAT[7:0]	R	0h	FOD1 DCO Numerator Readback, Byte 0. Reading this value returns the value of the FOD1 divisor's fractional portion, after it has been adjusted by the DCO logic.

3.80 R81 Register (Offset = 51h) [Reset = 00h]

R81 is shown in Table 3-82.

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Table 3-82. R81 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	FOD1_DCO_NUM_STAT[15:8]	R	0h	FOD1 DCO Numerator Readback, Byte 0. Reading this value returns the value of the FOD1 divisor's fractional portion, after it has been adjusted by the DCO logic.

3.81 R82 Register (Offset = 52h) [Reset = 00h]

R82 is shown in Table 3-83.

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Table 3-83. R82 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	FOD1_DCO_NUM_STAT[23:16]	R	0h	FOD1 DCO Numerator Readback, Byte 0. Reading this value returns the value of the FOD1 divisor's fractional portion, after it has been adjusted by the DCO logic.

3.82 R83 Register (Offset = 53h) [Reset = 90h]

R83 is shown in Table 3-84.

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Table 3-84. R83 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	BANK1_CLK_SEL	R/W	4h	BANK1 Clock Selection. Selects the clock source for BANK1 (OUT1, OUT2). For FOD0, select "PATH0" and set PATH0_EDGE_COMB_EN to 0x0. For FOD1, select "PATH1". For the Edge Combiner, select "PATH0" and set PATH0_EDGE_COMB_EN to 0x1. Manual Clock Switchover can be achieved by writing to this field while clocks are active. 0h = 0: IN_0 1h = 1: IN_1 2h = 2: IN_2 3h = 3: PATH0 4h = 4: PATH1
4-2	BANK0_CLK_SEL	R/W	4h	BANK0 Clock Selection. Selects the clock source for BANK0 (OUT0). For FOD0, select "PATH0" and set PATH0_EDGE_COMB_EN to 0x0. For FOD1, select "PATH1". For the Edge Combiner, select "PATH0" and set PATH0_EDGE_COMB_EN to 0x1. Manual Clock Switchover can be achieved by writing to this field while clocks are active. 0h = 0: IN_0 1h = 1: IN_1 2h = 2: IN_2 3h = 3: PATH0 4h = 4: PATH1
1	PATH1_EDGE_COMB_EN	R/W	0h	FOD PATH1 Edge Combiner Enable. This field determines whether output clock banks that select FOD PATH1 as their clock source will be driven by the output of the Edge Combiner or by the output of FOD PATH1 Post-divider. When set to 1, the Edge Combiner will be enabled, and the two FODs will both generate clocks with a frequency determined by the FOD0 Divide Ratio settings. TI recommends not modifying the value of this field. 0h = PATH1_DIV 1h = Edge Combiner
0	PATH0_EDGE_COMB_EN	R/W	0h	FOD PATH0 Edge Combiner Enable. This field determines whether output clock banks that select FOD PATH0 as their clock source will be driven by the output of the Edge Combiner or by the output of FOD PATH0 Post-divider. When set to 1, the Edge Combiner will be enabled, and the two FODs will both generate clocks with a frequency determined by the FOD0 Divide Ratio settings. 0h = PATH0_DIV 1h = Edge Combiner

3.83 R84 Register (Offset = 54h) [Reset = 24h]

R84 is shown in Table 3-85.

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Table 3-85. R84 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	Reserved
5-3	BANK3_CLK_SEL	R/W	4h	BANK3 Clock Selection. Selects the clock source for BANK3 (OUT5). For FOD0, select "PATH0" and set PATH0_EDGE_COMB_EN to 0x0. For FOD1, select "PATH1". For the Edge Combiner, select "PATH0" and set PATH0_EDGE_COMB_EN to 0x1. Manual Clock Switchover can be achieved by writing to this field while clocks are active. 0h = 0: IN_0 1h = 1: IN_1 2h = 2: IN_2 3h = 3: PATH0 4h = 4: PATH1
2-0	BANK2_CLK_SEL	R/W	4h	BANK2 Clock Selection. Selects the clock source for BANK2 (OUT3, OUT4). For FOD0, select "PATH0" and set PATH0_EDGE_COMB_EN to 0x0. For FOD1, select "PATH1". For the Edge Combiner, select "PATH0" and set PATH0_EDGE_COMB_EN to 0x1. Manual Clock Switchover can be achieved by writing to this field while clocks are active. 0h = 0: IN_0 1h = 1: IN_1 2h = 2: IN_2 3h = 3: PATH0 4h = 4: PATH1

3.84 R85 Register (Offset = 55h) [Reset = 24h]

R85 is shown in Table 3-86.

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Table 3-86. R85 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	Reserved
5-3	BANK5_CLK_SEL	R/W	4h	BANK5 Clock Selection. Selects the clock source for BANK5 (OUT7). For FOD0, select "PATH0" and set PATH0_EDGE_COMB_EN to 0x0. For FOD1, select "PATH1". For the Edge Combiner, select "PATH0" and set PATH0_EDGE_COMB_EN to 0x1. Manual Clock Switchover can be achieved by writing to this field while clocks are active. 0h = 0: IN_0 1h = 1: IN_1 2h = 2: IN_2 3h = 3: PATH0 4h = 4: PATH1
2-0	BANK4_CLK_SEL	R/W	4h	BANK4 Clock Selection. Selects the clock source for BANK4 (OUT6). For FOD0, select "PATH0" and set PATH0_EDGE_COMB_EN to 0x0. For FOD1, select "PATH1". For the Edge Combiner, select "PATH0" and set PATH0_EDGE_COMB_EN to 0x1. Manual Clock Switchover can be achieved by writing to this field while clocks are active. 0h = 0: IN_0 1h = 1: IN_1 2h = 2: IN_2 3h = 3: PATH0 4h = 4: PATH1

3.85 R86 Register (Offset = 56h) [Reset = 01h]

R86 is shown in Table 3-87.

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Table 3-87. R86 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BANK0_CH_DIV[7:0]	R/W	1h	Divisor for the BANK0 (OUT0) channel divider (Byte 0). For a divisor of 65536, value = 0. For any other divisor, value = divisor.

3.86 R87 Register (Offset = 57h) [Reset = 00h]

R87 is shown in Table 3-88.

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Table 3-88. R87 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BANK0_CH_DIV[15:8]	R/W	0h	Divisor for the BANK0 (OUT0) channel divider (Byte 0). For a divisor of 65536, value = 0. For any other divisor, value = divisor.

3.87 R88 Register (Offset = 58h) [Reset = 11h]

R88 is shown in Table 3-89.

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Table 3-89. R88 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	BANK2_CH_DIV	R/W	1h	Divisor for the BANK2 (OUT3, OUT4) channel divider. For a divisor of 16, value = 0. For any other divisor, value = divisor.
3-0	BANK1_CH_DIV	R/W	1h	Divisor for the BANK1 (OUT1, OUT2) channel divider. For a divisor of 16, value = 0. For any other divisor, value = divisor.

3.88 R89 Register (Offset = 59h) [Reset = 01h]

R89 is shown in Table 3-90.

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Table 3-90. R89 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0h	Reserved
0	IN0_LOS	R/W	1h	IN0 Loss-of-Signal. This is set to 1 to indicate that IN0 is currently invalid. 0h = IN_0 Valid 1h = IN_0 Invalid

3.89 R90 Register (Offset = 5Ah) [Reset = 11h]

R90 is shown in Table 3-91.

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Table 3-91. R90 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	BANK4_CH_DIV	R/W	1h	Divisor for the BANK4 (OUT6) channel divider. For a divisor of 16, value = 0. For any other divisor, value = divisor.
3-0	BANK3_CH_DIV	R/W	1h	Divisor for the BANK3 (OUT5) channel divider. For a divisor of 16, value = 0. For any other divisor, value = divisor.

3.90 R91 Register (Offset = 5Bh) [Reset = 01h]

R91 is shown in Table 3-92.

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Table 3-92. R91 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	PERST_BUF_BANK1	R/W	0h	BANK1 Buffer Mode Clock Selection. This field enables/disables Buffer Mode for BANK1 and selects the clock source to be used for BANK1 when Buffer Mode is active. For "Disabled" BANK1 will defer to the normal clock selection (BANK1_CLK_SEL). If this field selects a clock source that is unavailable or not active, BANK1 will defer to the normal clock selection (BANK1_CLK_SEL). 0h = BANK1_CLK_SEL 1h = IN_0 2h = IN_1 3h = IN_2
5-4	PERST_BUF_BANK0	R/W	0h	BANK0 Buffer Mode Clock Selection. This field enables/disables Buffer Mode for BANK0 and selects the clock source to be used for BANK0 when Buffer Mode is active. For "Disabled" BANK0 will defer to the normal clock selection (BANK0_CLK_SEL). If this field selects a clock source that is unavailable or not active, BANK0 will defer to the normal clock selection (BANK0_CLK_SEL). 0h = BANK0_CLK_SEL 1h = IN_0 2h = IN_1 3h = IN_2
3-0	BANK5_CH_DIV	R/W	1h	Divisor for the BANK5 (OUT7) channel divider. For a divisor of 16, value = 0. For any other divisor, value = divisor.

3.91 R92 Register (Offset = 5Ch) [Reset = 00h]

R92 is shown in Table 3-93.

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Table 3-93. R92 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	PERST_BUF_BANK5	R/W	0h	BANK5 Buffer Mode Clock Selection. This field enables/disables Buffer Mode for BANK5 and selects the clock source to be used for BANK5 when Buffer Mode is active. For "Disabled" BANK5 will defer to the normal clock selection (BANK5_CLK_SEL). If this field selects a clock source that is unavailable or not active, BANK5 will defer to the normal clock selection (BANK5_CLK_SEL). 0h = BANK5_CLK_SEL 1h = IN_0 2h = IN_1 3h = IN_2
5-4	PERST_BUF_BANK4	R/W	0h	BANK4 Buffer Mode Clock Selection. This field enables/disables Buffer Mode for BANK4 and selects the clock source to be used for BANK4 when Buffer Mode is active. For "Disabled" BANK4 will defer to the normal clock selection (BANK4_CLK_SEL). If this field selects a clock source that is unavailable or not active, BANK4 will defer to the normal clock selection (BANK4_CLK_SEL). 0h = BANK4_CLK_SEL 1h = IN_0 2h = IN_1 3h = IN_2
3-2	PERST_BUF_BANK3	R/W	0h	BANK3 Buffer Mode Clock Selection. This field enables/disables Buffer Mode for BANK3 and selects the clock source to be used for BANK3 when Buffer Mode is active. For "Disabled" BANK3 will defer to the normal clock selection (BANK3_CLK_SEL). If this field selects a clock source that is unavailable or not active, BANK3 will defer to the normal clock selection (BANK3_CLK_SEL). 0h = BANK3_CLK_SEL 1h = IN_0 2h = IN_1 3h = IN_2
1-0	PERST_BUF_BANK2	R/W	0h	BANK2 Buffer Mode Clock Selection. This field enables/disables Buffer Mode for BANK2 and selects the clock source to be used for BANK2 when Buffer Mode is active. For "Disabled" BANK2 will defer to the normal clock selection (BANK2_CLK_SEL). If this field selects a clock source that is unavailable or not active, BANK2 will defer to the normal clock selection (BANK2_CLK_SEL). 0h = BANK2_CLK_SEL 1h = IN_0 2h = IN_1 3h = IN_2

3.92 R93 Register (Offset = 5Dh) [Reset = FFh]

R93 is shown in Table 3-94.

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Table 3-94. R93 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	BANK1_AUTO_CLK_SWITCHBACK_EN	R/W	1h	BANK1 Automatic Clock Switchback Enable. When enabled, after BANK1 undergoes a Automatic Clock Switchover, if the original clock source is re-validated, BANK1 will immediately switch back to it. This bit is ignored unless BANK1_AUTO_CLK_SWITCHOVER_EN is set to 1.
6	BANK0_AUTO_CLK_SWITCHBACK_EN	R/W	1h	BANK0 Automatic Clock Switchback Enable. When enabled, after BANK0 undergoes a Automatic Clock Switchover, if the original clock source is re-validated, BANK0 will immediately switch back to it. This bit is ignored unless BANK0_AUTO_CLK_SWITCHOVER_EN is set to 1.
5	BANK5_AUTO_CLK_SWITCHOVER_EN	R/W	1h	BANK5 Automatic Clock Switchover Enable. Assuming that BANK5 is sourced by an input clock, if the input clock is determined to be invalid (LOS), BANK5 will automatically switch its clock source to the FOD-generated clock selected by the BANK5_AUTO_CLK_SWITCHOVER_CLK_SEL. Cannot be enabled simultaneously with BANK5_CLK_DIS_ON_LOS or BANK5 Buffer Mode.
4	BANK4_AUTO_CLK_SWITCHOVER_EN	R/W	1h	BANK4 Automatic Clock Switchover Enable. Assuming that BANK4 is sourced by an input clock, if the input clock is determined to be invalid (LOS), BANK4 will automatically switch its clock source to the FOD-generated clock selected by the BANK4_AUTO_CLK_SWITCHOVER_CLK_SEL. Cannot be enabled simultaneously with BANK4_CLK_DIS_ON_LOS or BANK4 Buffer Mode.
3	BANK3_AUTO_CLK_SWITCHOVER_EN	R/W	1h	BANK3 Automatic Clock Switchover Enable. Assuming that BANK3 is sourced by an input clock, if the input clock is determined to be invalid (LOS), BANK3 will automatically switch its clock source to the FOD-generated clock selected by the BANK3_AUTO_CLK_SWITCHOVER_CLK_SEL. Cannot be enabled simultaneously with BANK3_CLK_DIS_ON_LOS or BANK3 Buffer Mode.
2	BANK2_AUTO_CLK_SWITCHOVER_EN	R/W	1h	BANK2 Automatic Clock Switchover Enable. Assuming that BANK2 is sourced by an input clock, if the input clock is determined to be invalid (LOS), BANK2 will automatically switch its clock source to the FOD-generated clock selected by the BANK2_AUTO_CLK_SWITCHOVER_CLK_SEL. Cannot be enabled simultaneously with BANK2_CLK_DIS_ON_LOS or BANK2 Buffer Mode.
1	BANK1_AUTO_CLK_SWITCHOVER_EN	R/W	1h	BANK1 Automatic Clock Switchover Enable. Assuming that BANK1 is sourced by an input clock, if the input clock is determined to be invalid (LOS), BANK1 will automatically switch its clock source to the FOD-generated clock selected by the BANK1_AUTO_CLK_SWITCHOVER_CLK_SEL. Cannot be enabled simultaneously with BANK1_CLK_DIS_ON_LOS or BANK1 Buffer Mode.
0	BANK0_AUTO_CLK_SWITCHOVER_EN	R/W	1h	BANK0 Automatic Clock Switchover Enable. Assuming that BANK0 is sourced by an input clock, if the input clock is determined to be invalid (LOS), BANK0 will automatically switch its clock source to the FOD-generated clock selected by the BANK0_AUTO_CLK_SWITCHOVER_CLK_SEL. Cannot be enabled simultaneously with BANK0_CLK_DIS_ON_LOS or BANK0 Buffer Mode.

3.93 R94 Register (Offset = 5Eh) [Reset = FFh]

R94 is shown in Table 3-95.

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Table 3-95. R94 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	BANK3_AUTO_CLK_SWITCHOVER_CLK_SEL	R/W	1h	BANK3 Automatic Clock Switchover Clock Select. Selects the clock source that is switched to if the original BANK3 clock source is determined to be invalid. This bit is ignored unless BANK3_AUTO_CLK_SWITCHOVER_EN is set to 1. 0h = PATH0 1h = PATH1
6	BANK2_AUTO_CLK_SWITCHOVER_CLK_SEL	R/W	1h	BANK2 Automatic Clock Switchover Clock Select. Selects the clock source that is switched to if the original BANK2 clock source is determined to be invalid. This bit is ignored unless BANK2_AUTO_CLK_SWITCHOVER_EN is set to 1. 0h = PATH0 1h = PATH1
5	BANK1_AUTO_CLK_SWITCHOVER_CLK_SEL	R/W	1h	BANK1 Automatic Clock Switchover Clock Select. Selects the clock source that is switched to if the original BANK1 clock source is determined to be invalid. This bit is ignored unless BANK1_AUTO_CLK_SWITCHOVER_EN is set to 1. 0h = PATH0 1h = PATH1
4	BANK0_AUTO_CLK_SWITCHOVER_CLK_SEL	R/W	1h	BANK0 Automatic Clock Switchover Clock Select. Selects the clock source that is switched to if the original BANK0 clock source is determined to be invalid. This bit is ignored unless BANK0_AUTO_CLK_SWITCHOVER_EN is set to 1. 0h = PATH0 1h = PATH1
3	BANK5_AUTO_CLK_SWITCHBACK_EN	R/W	1h	BANK5 Automatic Clock Switchback Enable. When enabled, after BANK5 undergoes a Automatic Clock Switchover, if the original clock source is re-validated, BANK5 will immediately switch back to it. This bit is ignored unless BANK5_AUTO_CLK_SWITCHOVER_EN is set to 1.
2	BANK4_AUTO_CLK_SWITCHBACK_EN	R/W	1h	BANK4 Automatic Clock Switchback Enable. When enabled, after BANK4 undergoes a Automatic Clock Switchover, if the original clock source is re-validated, BANK4 will immediately switch back to it. This bit is ignored unless BANK4_AUTO_CLK_SWITCHOVER_EN is set to 1.
1	BANK3_AUTO_CLK_SWITCHBACK_EN	R/W	1h	BANK3 Automatic Clock Switchback Enable. When enabled, after BANK3 undergoes a Automatic Clock Switchover, if the original clock source is re-validated, BANK3 will immediately switch back to it. This bit is ignored unless BANK3_AUTO_CLK_SWITCHOVER_EN is set to 1.
0	BANK2_AUTO_CLK_SWITCHBACK_EN	R/W	1h	BANK2 Automatic Clock Switchback Enable. When enabled, after BANK2 undergoes a Automatic Clock Switchover, if the original clock source is re-validated, BANK2 will immediately switch back to it. This bit is ignored unless BANK2_AUTO_CLK_SWITCHOVER_EN is set to 1.

3.94 R95 Register (Offset = 5Fh) [Reset = FFh]

R95 is shown in Table 3-96.

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Table 3-96. R95 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	BANK5_CLK_SWITCHOVER_TYPE	R/W	1h	BANK5 Clock Switchover Type. Selects whether BANK5 Automatic Clock Switchover/Switchback, Manual Clock Switchover via I2C, and PERST#-triggered Buffer Mode clock switching, are glitchless or not. 0h = Immediate 1h = Glitchless
6	BANK4_CLK_SWITCHOVER_TYPE	R/W	1h	BANK4 Clock Switchover Type. Selects whether BANK4 Automatic Clock Switchover/Switchback, Manual Clock Switchover via I2C, and PERST#-triggered Buffer Mode clock switching, are glitchless or not. 0h = Immediate 1h = Glitchless
5	BANK3_CLK_SWITCHOVER_TYPE	R/W	1h	BANK3 Clock Switchover Type. Selects whether BANK3 Automatic Clock Switchover/Switchback, Manual Clock Switchover via I2C, and PERST#-triggered Buffer Mode clock switching, are glitchless or not. 0h = Immediate 1h = Glitchless
4	BANK2_CLK_SWITCHOVER_TYPE	R/W	1h	BANK2 Clock Switchover Type. Selects whether BANK2 Automatic Clock Switchover/Switchback, Manual Clock Switchover via I2C, and PERST#-triggered Buffer Mode clock switching, are glitchless or not. 0h = Immediate 1h = Glitchless
3	BANK1_CLK_SWITCHOVER_TYPE	R/W	1h	BANK1 Clock Switchover Type. Selects whether BANK1 Automatic Clock Switchover/Switchback, Manual Clock Switchover via I2C, and PERST#-triggered Buffer Mode clock switching, are glitchless or not. This bit is ignored unless BANK1_AUTO_CLK_SWITCHOVER_EN is set to 1. 0h = Immediate 1h = Glitchless
2	BANK0_CLK_SWITCHOVER_TYPE	R/W	1h	BANK0 Clock Switchover Type. Selects whether BANK0 Automatic Clock Switchover/Switchback, Manual Clock Switchover via I2C, and PERST#-triggered Buffer Mode clock switching, are glitchless or not. 0h = Immediate 1h = Glitchless
1	BANK5_AUTO_CLK_SWITCHOVER_CLK_SEL	R/W	1h	BANK5 Automatic Clock Switchover Clock Select. Selects the clock source that is switched to if the original BANK5 clock source is determined to be invalid. This bit is ignored unless BANK5_AUTO_CLK_SWITCHOVER_EN is set to 1. 0h = PATH0 1h = PATH1
0	BANK4_AUTO_CLK_SWITCHOVER_CLK_SEL	R/W	1h	BANK4 Automatic Clock Switchover Clock Select. Selects the clock source that is switched to if the original BANK4 clock source is determined to be invalid. This bit is ignored unless BANK4_AUTO_CLK_SWITCHOVER_EN is set to 1. 0h = PATH0 1h = PATH1

3.95 R96 Register (Offset = 60h) [Reset = 00h]

R96 is shown in Table 3-97.

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Table 3-97. R96 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	BANK1_SWITCHOVER_FRC_CLK_EN	R/W	0h	Force BANK1 Switchover. When enabled, changing BANK1_CLK_SEL on OTP pages allows for switching between FODs and inputs, but changing BANK1_CLK_SEL via I2C will not change the active clock source. When disabled, changing BANK1_CLK_SEL on OTP pages does not allow for switching between FODs and inputs, but changing BANK1_CLK_SEL via I2C will change the active clock source. 0h = Switchover through I2C; Changing the value of BANK1_CLK_SEL through OTP page changing will not work. Changing the value of BANK1_CLK_SEL through I2C will have an impact. 1h = Switchover through OTP; Changing the value of BANK1_CLK_SEL through OTP page changing will work. Changing the value of BANK1_CLK_SEL through I2C will not have an impact.
6	BANK0_SWITCHOVER_FRC_CLK_EN	R/W	0h	Force BANK0 Switchover. When enabled, changing BANK0_CLK_SEL on OTP pages allows for switching between FODs and inputs, but changing BANK0_CLK_SEL via I2C will not change the active clock source. When disabled, changing BANK0_CLK_SEL on OTP pages does not allow for switching between FODs and inputs, but changing BANK0_CLK_SEL via I2C will change the active clock source. 0h = Switchover through I2C; Changing the value of BANK0_CLK_SEL through OTP page changing will not work. Changing the value of BANK0_CLK_SEL through I2C will have an impact. 1h = Switchover through OTP; Changing the value of BANK0_CLK_SEL through OTP page changing will work. Changing the value of BANK0_CLK_SEL through I2C will not have an impact.
5	BANK5_CLK_DIS_ON_LOS	R/W	0h	BANK5 Clock Disable on Loss-of-Signal. When enabled, if BANK5 is sourced by an input clock, and that input clock is determined to be invalid, BANK5 clocks will be automatically disabled. Cannot be enabled simultaneously with BANK5_AUTO_CLK_SWITCHOVER_EN or BANK5 Buffer Mode. 0h = No LOS Disable 1h = Disabled on LOS
4	BANK4_CLK_DIS_ON_LOS	R/W	0h	BANK4 Clock Disable on Loss-of-Signal. When enabled, if BANK4 is sourced by an input clock, and that input clock is determined to be invalid, BANK4 clocks will be automatically disabled. Cannot be enabled simultaneously with BANK4_AUTO_CLK_SWITCHOVER_EN or BANK4 Buffer Mode. 0h = No LOS Disable 1h = Disabled on LOS
3	BANK3_CLK_DIS_ON_LOS	R/W	0h	BANK3 Clock Disable on Loss-of-Signal. When enabled, if BANK3 is sourced by an input clock, and that input clock is determined to be invalid, BANK3 clocks will be automatically disabled. Cannot be enabled simultaneously with BANK3_AUTO_CLK_SWITCHOVER_EN or BANK3 Buffer Mode. 0h = No LOS Disable 1h = Disabled on LOS
2	BANK2_CLK_DIS_ON_LOS	R/W	0h	BANK2 Clock Disable on Loss-of-Signal. When enabled, if BANK2 is sourced by an input clock, and that input clock is determined to be invalid, BANK2 clocks will be automatically disabled. Cannot be enabled simultaneously with BANK2_AUTO_CLK_SWITCHOVER_EN or BANK2 Buffer Mode. 0h = No LOS Disable 1h = Disabled on LOS

Table 3-97. R96 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	BANK1_CLK_DIS_ON_LOS	R/W	0h	BANK1 Clock Disable on Loss-of-Signal. When enabled, if BANK1 is sourced by an input clock, and that input clock is determined to be invalid, BANK1 clocks will be automatically disabled. Cannot be enabled simultaneously with BANK1_AUTO_CLK_SWITCHOVER_EN or BANK1 Buffer Mode. 0h = No LOS Disable 1h = Disabled on LOS
0	BANK0_CLK_DIS_ON_LOS	R/W	0h	BANK0 Clock Disable on Loss-of-Signal. When enabled, if BANK0 is sourced by an input clock, and that input clock is determined to be invalid, BANK0 clocks will be automatically disabled. Cannot be enabled simultaneously with BANK0_AUTO_CLK_SWITCHOVER_EN or BANK0 Buffer Mode. 0h = No LOS Disable 1h = Disabled on LOS

3.96 R97 Register (Offset = 61h) [Reset = 00h]

R97 is shown in Table 3-98.

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Table 3-98. R97 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	OUT1_SLEW_RATE	R/W	0h	OUT1 Slew Rate (differential and 1.2V LVCMOS). Controls the slew rate for OUT1. 0x0 is the fastest setting and 0x3 is the slowest setting. Actual slew rate depends on the OUT1 clock format and the VDDO_1_2 supply level. If OUT1 is set for LVCMOS (except for 1.2V LVCMOS), this field will be ignored (see OUT1_CMOS_SLEW_RATE). 0h = 2.4 V/ns - 3.7 V/ns 1h = 2.2 V/ns - 3.4 V/ns 2h = 2.0 V/ns - 3.1 V/ns 3h = 1.8 V/ns - 2.8 V/ns
5-4	OUT0_SLEW_RATE	R/W	0h	OUT0 Slew Rate (differential and 1.2V LVCMOS). Controls the slew rate for OUT0. 0x0 is the fastest setting and 0x3 is the slowest setting. Actual slew rate depends on the OUT0 clock format and the VDDO_0 supply level. If OUT0 is set for LVCMOS (except for 1.2V LVCMOS), this field will be ignored (see OUT0_CMOS_SLEW_RATE). 0h = 2.4 V/ns - 3.7 V/ns 1h = 2.2 V/ns - 3.4 V/ns 2h = 2.0 V/ns - 3.1 V/ns 3h = 1.8 V/ns - 2.8 V/ns
3	BANK5_SWITCHOVER_FRC_CLK_EN	R/W	0h	Force BANK5 Switchover. When enabled, changing BANK5_CLK_SEL on OTP pages allows for switching between FODs and inputs, but changing BANK5_CLK_SEL via I2C will not change the active clock source. When disabled, changing BANK5_CLK_SEL on OTP pages does not allow for switching between FODs and inputs, but changing BANK5_CLK_SEL via I2C will change the active clock source. 0h = Switchover through I2C; Changing the value of BANK5_CLK_SEL through OTP page changing will not work. Changing the value of BANK5_CLK_SEL through I2C will have an impact. 1h = Switchover through OTP; Changing the value of BANK5_CLK_SEL through OTP page changing will work. Changing the value of BANK5_CLK_SEL through I2C will not have an impact.
2	BANK4_SWITCHOVER_FRC_CLK_EN	R/W	0h	Force BANK4 Switchover. When enabled, changing BANK4_CLK_SEL on OTP pages allows for switching between FODs and inputs, but changing BANK4_CLK_SEL via I2C will not change the active clock source. When disabled, changing BANK4_CLK_SEL on OTP pages does not allow for switching between FODs and inputs, but changing BANK4_CLK_SEL via I2C will change the active clock source. 0h = Switchover through I2C; Changing the value of BANK4_CLK_SEL through OTP page changing will not work. Changing the value of BANK4_CLK_SEL through I2C will have an impact. 1h = Switchover through OTP; Changing the value of BANK4_CLK_SEL through OTP page changing will work. Changing the value of BANK4_CLK_SEL through I2C will not have an impact.

Table 3-98. R97 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	BANK3_SWITCHOVER_FRC_CLK_EN	R/W	0h	Force BANK3 Switchover. When enabled, changing BANK3_CLK_SEL on OTP pages allows for switching between FODs and inputs, but changing BANK3_CLK_SEL via I2C will not change the active clock source. When disabled, changing BANK3_CLK_SEL on OTP pages does not allow for switching between FODs and inputs, but changing BANK3_CLK_SEL via I2C will change the active clock source. 0h = Switchover through I2C; Changing the value of BANK3_CLK_SEL through OTP page changing will not work. Changing the value of BANK3_CLK_SEL through I2C will have an impact. 1h = Switchover through OTP; Changing the value of BANK3_CLK_SEL through OTP page changing will work. Changing the value of BANK3_CLK_SEL through I2C will not have an impact.
0	BANK2_SWITCHOVER_FRC_CLK_EN	R/W	0h	Force BANK2 Switchover. When enabled, changing BANK2_CLK_SEL on OTP pages allows for switching between FODs and inputs, but changing BANK2_CLK_SEL via I2C will not change the active clock source. When disabled, changing BANK2_CLK_SEL on OTP pages does not allow for switching between FODs and inputs, but changing BANK2_CLK_SEL via I2C will change the active clock source. 0h = Switchover through I2C; Changing the value of BANK2_CLK_SEL through OTP page changing will not work. Changing the value of BANK2_CLK_SEL through I2C will have an impact. 1h = Switchover through OTP; Changing the value of BANK2_CLK_SEL through OTP page changing will work. Changing the value of BANK2_CLK_SEL through I2C will not have an impact.

3.97 R98 Register (Offset = 62h) [Reset = 00h]

R98 is shown in Table 3-99.

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Table 3-99. R98 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	OUT5_SLEW_RATE	R/W	0h	OUT5 Slew Rate (differential and 1.2V LVCMOS). Controls the slew rate for OUT5. 0x0 is the fastest setting and 0x3 is the slowest setting. Actual slew rate depends on the OUT5 clock format and the VDDO_5 supply level. If OUT5 is set for LVCMOS (except for 1.2V LVCMOS), this field will be ignored (see OUT5_CMOS_SLEW_RATE). 0h = 2.4 V/ns - 3.7 V/ns 1h = 2.2 V/ns - 3.4 V/ns 2h = 2.0 V/ns - 3.1 V/ns 3h = 1.8 V/ns - 2.8 V/ns
5-4	OUT4_SLEW_RATE	R/W	0h	OUT4 Slew Rate (differential and 1.2V LVCMOS). Controls the slew rate for OUT4. 0x0 is the fastest setting and 0x3 is the slowest setting. Actual slew rate depends on the OUT4 clock format and the VDDO_3_4 supply level. If OUT3 is set for LVCMOS (except for 1.2V LVCMOS), this field will be ignored (see OUT4_CMOS_SLEW_RATE). 0h = 2.4 V/ns - 3.7 V/ns 1h = 2.2 V/ns - 3.4 V/ns 2h = 2.0 V/ns - 3.1 V/ns 3h = 1.8 V/ns - 2.8 V/ns
3-2	OUT3_SLEW_RATE	R/W	0h	OUT3 Slew Rate (differential and 1.2V LVCMOS). Controls the slew rate for OUT3. 0x0 is the fastest setting and 0x3 is the slowest setting. Actual slew rate depends on the OUT3 clock format and the VDDO_3 supply level. If OUT3 is set for LVCMOS (except for 1.2V LVCMOS), this field will be ignored (see OUT3_CMOS_SLEW_RATE). 0h = 2.4 V/ns - 3.7 V/ns 1h = 2.2 V/ns - 3.4 V/ns 2h = 2.0 V/ns - 3.1 V/ns 3h = 1.8 V/ns - 2.8 V/ns
1-0	OUT2_SLEW_RATE	R/W	0h	OUT2 Slew Rate (differential and 1.2V LVCMOS). Controls the slew rate for OUT2. 0x0 is the fastest setting and 0x3 is the slowest setting. Actual slew rate depends on the OUT2 clock format and the VDDO_2 supply level. If OUT2 is set for LVCMOS (except for 1.2V LVCMOS), this field will be ignored (see OUT2_CMOS_SLEW_RATE). 0h = 2.4 V/ns - 3.7 V/ns 1h = 2.2 V/ns - 3.4 V/ns 2h = 2.0 V/ns - 3.1 V/ns 3h = 1.8 V/ns - 2.8 V/ns

3.98 R99 Register (Offset = 63h) [Reset = 00h]

R99 is shown in Table 3-100.

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Table 3-100. R99 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	OUT1_CMOS_SLEW_RATE	R/W	0h	OUT1 Slew Rate (CMOS). Controls the slew rate for OUT1. 0x0 is the fastest setting and 0x3 is the slowest setting. Actual slew rate depends on the VDDO_1 supply level. If OUT1 is set for differential or 1.2V LVCMOS, this field will be ignored. If OUT1 is not configured for LVCMOS, this field will be ignored (see OUT1_SLEW_RATE). 0h = 3.1 V/ns - 5.2 V/ns 1h = 2.6 V/ns - 5 V/ns 2h = 1.7 V/ns - 4.0 V/ns 3h = 1.3 V/ns - 3.5 V/ns
5-4	OUT0_CMOS_SLEW_RATE	R/W	0h	OUT0 Slew Rate (CMOS). Controls the slew rate for OUT0. 0x0 is the fastest setting and 0x3 is the slowest setting. Actual slew rate depends on the VDDO_0 supply level. If OUT0 is set for differential or 1.2V LVCMOS, this field will be ignored. If OUT0 is not configured for LVCMOS, this field will be ignored (see OUT0_SLEW_RATE). 0h = 3.1 V/ns - 5.2 V/ns 1h = 2.6 V/ns - 5 V/ns 2h = 1.7 V/ns - 4.0 V/ns 3h = 1.3 V/ns - 3.5 V/ns
3-2	OUT7_SLEW_RATE	R/W	0h	OUT7 Slew Rate (differential and 1.2V LVCMOS). Controls the slew rate for OUT7. 0x0 is the fastest setting and 0x3 is the slowest setting. Actual slew rate depends on the OUT7 clock format and the VDDO_7 supply level. If OUT7 is set for LVCMOS (except for 1.2V LVCMOS), this field will be ignored (see OUT7_CMOS_SLEW_RATE). 0h = 2.4 V/ns - 3.7 V/ns 1h = 2.2 V/ns - 3.4 V/ns 2h = 2.0 V/ns - 3.1 V/ns 3h = 1.8 V/ns - 2.8 V/ns
1-0	OUT6_SLEW_RATE	R/W	0h	OUT6 Slew Rate (differential and 1.2V LVCMOS). Controls the slew rate for OUT6. 0x0 is the fastest setting and 0x3 is the slowest setting. Actual slew rate depends on the OUT6 clock format and the VDDO_6 supply level. If OUT6 is set for LVCMOS (except for 1.2V LVCMOS), this field will be ignored (see OUT6_CMOS_SLEW_RATE). 0h = 2.4 V/ns - 3.7 V/ns 1h = 2.2 V/ns - 3.4 V/ns 2h = 2.0 V/ns - 3.1 V/ns 3h = 1.8 V/ns - 2.8 V/ns

3.99 R100 Register (Offset = 64h) [Reset = 00h]

R100 is shown in Table 3-101.

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Table 3-101. R100 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	OUT5_CMOS_SLEW_RATE	R/W	0h	OUT5 Slew Rate (CMOS). Controls the slew rate for OUT5. 0x0 is the fastest setting and 0x3 is the slowest setting. Actual slew rate depends on the VDDO_5 supply level. If OUT5 is set for differential or 1.2V LVCMOS, this field will be ignored. If OUT5 is not configured for LVCMOS, this field will be ignored (see OUT5_SLEW_RATE). 0h = 3.1 V/ns - 5.2 V/ns 1h = 2.6 V/ns - 5 V/ns 2h = 1.7 V/ns - 4.0 V/ns 3h = 1.3 V/ns - 3.5 V/ns
5-4	OUT4_CMOS_SLEW_RATE	R/W	0h	OUT4 Slew Rate (CMOS). Controls the slew rate for OUT4. 0x0 is the fastest setting and 0x3 is the slowest setting. Actual slew rate depends on the VDDO_3_4 supply level. If OUT4 is set for differential or 1.2V LVCMOS, this field will be ignored. If OUT4 is not configured for LVCMOS, this field will be ignored (see OUT4_SLEW_RATE). 0h = 3.1 V/ns - 5.2 V/ns 1h = 2.6 V/ns - 5 V/ns 2h = 1.7 V/ns - 4.0 V/ns 3h = 1.3 V/ns - 3.5 V/ns
3-2	OUT3_CMOS_SLEW_RATE	R/W	0h	OUT3 Slew Rate (CMOS). Controls the slew rate for OUT3. 0x0 is the fastest setting and 0x3 is the slowest setting. Actual slew rate depends on the VDDO_3_4 supply level. If OUT3 is set for differential or 1.2V LVCMOS, this field will be ignored. If OUT3 is not configured for LVCMOS, this field will be ignored (see OUT3_SLEW_RATE). 0h = 3.1 V/ns - 5.2 V/ns 1h = 2.6 V/ns - 5 V/ns 2h = 1.7 V/ns - 4.0 V/ns 3h = 1.3 V/ns - 3.5 V/ns
1-0	OUT2_CMOS_SLEW_RATE	R/W	0h	OUT2 Slew Rate (CMOS). Controls the slew rate for OUT2. 0x0 is the fastest setting and 0x3 is the slowest setting. Actual slew rate depends on the VDDO_1_2 supply level. If OUT2 is set for differential or 1.2V LVCMOS, this field will be ignored. If OUT2 is not configured for LVCMOS, this field will be ignored (see OUT2_SLEW_RATE). 0h = 3.1 V/ns - 5.2 V/ns 1h = 2.6 V/ns - 5 V/ns 2h = 1.7 V/ns - 4.0 V/ns 3h = 1.3 V/ns - 3.5 V/ns

3.100 R101 Register (Offset = 65h) [Reset = 00h]

R101 is shown in Table 3-102.

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Table 3-102. R101 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	OUT1_DIS_STATE	R/W	0h	OUT1 Disabled State. Selects the state of OUT0_P and OUT0_N when OUT0 is disabled. For AC-LVDS clocks, LOW/LOW must be selected. DC-LVDS clocks may select any disabled state. For either LVDS coupling, "LOW/LOW" is not descriptive of the output clock behavior; the output clock will instead behave as HIGH/LOW. 0h = P/N: HIGH/LOW 1h = P/N: LOW/HIGH 2h = P/N: LOW/LOW; For LVDS clocks, LOW/LOW is not valid, and if selected, HIGH/LOW will be used instead. 3h = P/N: HI-Z/HI-Z
5-4	OUT0_DIS_STATE	R/W	0h	OUT0 Disabled State. Selects the state of OUT0_P and OUT0_N when OUT0 is disabled. For AC-LVDS clocks, LOW/LOW must be selected. DC-LVDS clocks may select any disabled state. For either LVDS coupling, "LOW/LOW" is not descriptive of the output clock behavior; the output clock will instead behave as HIGH/LOW. 0h = P/N: HIGH/LOW 1h = P/N: LOW/HIGH 2h = P/N: LOW/LOW; For LVDS clocks, LOW/LOW is not valid, and if selected, HIGH/LOW will be used instead. 3h = P/N: HI-Z/HI-Z
3-2	OUT7_CMOS_SLEW_RATE	R/W	0h	OUT7 Slew Rate (CMOS). Controls the slew rate for OUT7. 0x0 is the fastest setting and 0x3 is the slowest setting. Actual slew rate depends on the VDDO_7 supply level. If OUT7 is set for differential or 1.2V LVCMOS, this field will be ignored. If OUT7 is not configured for LVCMOS, this field will be ignored (see OUT7_SLEW_RATE). 0h = 3.1 V/ns - 5.2 V/ns 1h = 2.6 V/ns - 5 V/ns 2h = 1.7 V/ns - 4.0 V/ns 3h = 1.3 V/ns - 3.5 V/ns
1-0	OUT6_CMOS_SLEW_RATE	R/W	0h	OUT6 Slew Rate (CMOS). Controls the slew rate for OUT6. 0x0 is the fastest setting and 0x3 is the slowest setting. Actual slew rate depends on the VDDO_6 supply level. If OUT6 is set for differential or 1.2V LVCMOS, this field will be ignored. If OUT6 is not configured for LVCMOS, this field will be ignored (see OUT6_SLEW_RATE). 0h = 3.1 V/ns - 5.2 V/ns 1h = 2.6 V/ns - 5 V/ns 2h = 1.7 V/ns - 4.0 V/ns 3h = 1.3 V/ns - 3.5 V/ns

3.101 R102 Register (Offset = 66h) [Reset = 00h]

R102 is shown in Table 3-103.

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Table 3-103. R102 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	OUT5_DIS_STATE	R/W	0h	OUT5 Disabled State. Selects the state of OUT0_P and OUT0_N when OUT0 is disabled. For AC-LVDS clocks, LOW/LOW must be selected. DC-LVDS clocks may select any disabled state. For either LVDS coupling, "LOW/LOW" is not descriptive of the output clock behavior; the output clock will instead behave as HIGH/LOW. 0h = P/N: HIGH/LOW 1h = P/N: LOW/HIGH 2h = P/N: LOW/LOW; For LVDS clocks, LOW/LOW is not valid, and if selected, HIGH/LOW will be used instead. 3h = P/N: HI-Z/HI-Z
5-4	OUT4_DIS_STATE	R/W	0h	OUT4 Disabled State. Selects the state of OUT0_P and OUT0_N when OUT0 is disabled. For AC-LVDS clocks, LOW/LOW must be selected. DC-LVDS clocks may select any disabled state. For either LVDS coupling, "LOW/LOW" is not descriptive of the output clock behavior; the output clock will instead behave as HIGH/LOW. 0h = P/N: HIGH/LOW 1h = P/N: LOW/HIGH 2h = P/N: LOW/LOW; For LVDS clocks, LOW/LOW is not valid, and if selected, HIGH/LOW will be used instead. 3h = P/N: HI-Z/HI-Z
3-2	OUT3_DIS_STATE	R/W	0h	OUT3 Disabled State. Selects the state of OUT0_P and OUT0_N when OUT0 is disabled. For AC-LVDS clocks, LOW/LOW must be selected. DC-LVDS clocks may select any disabled state. For either LVDS coupling, "LOW/LOW" is not descriptive of the output clock behavior; the output clock will instead behave as HIGH/LOW. 0h = P/N: HIGH/LOW 1h = P/N: LOW/HIGH 2h = P/N: LOW/LOW; For LVDS clocks, LOW/LOW is not valid, and if selected, HIGH/LOW will be used instead. 3h = P/N: HI-Z/HI-Z
1-0	OUT2_DIS_STATE	R/W	0h	OUT2 Disabled State. Selects the state of OUT0_P and OUT0_N when OUT0 is disabled. For AC-LVDS clocks, LOW/LOW must be selected. DC-LVDS clocks may select any disabled state. For either LVDS coupling, "LOW/LOW" is not descriptive of the output clock behavior; the output clock will instead behave as HIGH/LOW. 0h = P/N: HIGH/LOW 1h = P/N: LOW/HIGH 2h = P/N: LOW/LOW; For LVDS clocks, LOW/LOW is not valid, and if selected, HIGH/LOW will be used instead. 3h = P/N: HI-Z/HI-Z

3.102 R103 Register (Offset = 67h) [Reset = 40h]

R103 is shown in Table 3-104.

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Table 3-104. R103 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	OUT0_FMT	R/W	1h	OUT0 Clock Format. 0h = 100 Ω LP-HCSL 1h = 85 Ω LP-HCSL 2h = LVDS 3h = LVCMOS
5-4	RESERVED	R	0h	Reserved
3-2	OUT7_DIS_STATE	R/W	0h	OUT7 Disabled State. Selects the state of OUT0_P and OUT0_N when OUT0 is disabled. For AC-LVDS clocks, LOW/LOW must be selected. DC-LVDS clocks may select any disabled state. For either LVDS coupling, "LOW/LOW" is not descriptive of the output clock behavior; the output clock will instead behave as HIGH/LOW. 0h = P/N: HIGH/LOW 1h = P/N: LOW/HIGH 2h = P/N: LOW/LOW; For LVDS clocks, LOW/LOW is not valid, and if selected, HIGH/LOW will be used instead. 3h = P/N: HI-Z/HI-Z
1-0	OUT6_DIS_STATE	R/W	0h	OUT6 Disabled State. Selects the state of OUT0_P and OUT0_N when OUT0 is disabled. For AC-LVDS clocks, LOW/LOW must be selected. DC-LVDS clocks may select any disabled state. For either LVDS coupling, "LOW/LOW" is not descriptive of the output clock behavior; the output clock will instead behave as HIGH/LOW. 0h = P/N: HIGH/LOW 1h = P/N: LOW/HIGH 2h = P/N: LOW/LOW; For LVDS clocks, LOW/LOW is not valid, and if selected, HIGH/LOW will be used instead. 3h = P/N: HI-Z/HI-Z

3.103 R104 Register (Offset = 68h) [Reset = 55h]

R104 is shown in Table 3-105.

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Table 3-105. R104 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	OUT4_FMT	R/W	1h	OUT4 Clock Format. 0h = 100 Ω LP-HCSL 1h = 85 Ω LP-HCSL 2h = LVDS 3h = LVCMOS
5-4	OUT3_FMT	R/W	1h	OUT3 Clock Format. 0h = 100 Ω LP-HCSL 1h = 85 Ω LP-HCSL 2h = LVDS 3h = LVCMOS
3-2	OUT2_FMT	R/W	1h	OUT2 Clock Format. 0h = 100 Ω LP-HCSL 1h = 85 Ω LP-HCSL 2h = LVDS 3h = LVCMOS
1-0	OUT1_FMT	R/W	1h	OUT1 Clock Format. 0h = 100 Ω LP-HCSL 1h = 85 Ω LP-HCSL 2h = LVDS 3h = LVCMOS

3.104 R105 Register (Offset = 69h) [Reset = 01h]

R105 is shown in Table 3-106.

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Table 3-106. R105 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0h	Reserved
0	IN1_LOS	R/W	1h	IN1 Loss-of-Signal. This is set to 1 to indicate that IN1 is currently invalid. 0h = IN1 Valid 1h = IN1 Invalid

3.105 R106 Register (Offset = 6Ah) [Reset = 15h]

R106 is shown in Table 3-107.

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Table 3-107. R106 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	OUT1_CMOS_1P2V_EN	R/W	0h	OUT1 1.2V CMOS Enable. When the clock format of OUT1 is configured for one of the LVCMOS options, this bit determines if the CMOS clock voltage will be 1.2V or if it will match the VDDO_1_2 supply voltage. When the clock format of OUT1 is not configured for one of the LVCMOS options, this bit is ignored.
6	OUT0_CMOS_1P2V_EN	R/W	0h	OUT0 1.2V CMOS Enable. When the clock format of OUT0 is configured for one of the LVCMOS options, this bit determines if the CMOS clock voltage will be 1.2V or if it will match the VDDO_0 supply voltage. When the clock format of OUT0 is not configured for one of the LVCMOS options, this bit is ignored.
5-4	OUT7_FMT	R/W	1h	OUT7 Clock Format. 0h = 100 Ω LP-HCSL 1h = 85 Ω LP-HCSL 2h = LVDS 3h = LVCMOS
3-2	OUT6_FMT	R/W	1h	OUT6 Clock Format. 0h = 100 Ω LP-HCSL 1h = 85 Ω LP-HCSL 2h = LVDS 3h = LVCMOS
1-0	OUT5_FMT	R/W	1h	OUT5 Clock Format. 0h = 100 Ω LP-HCSL 1h = 85 Ω LP-HCSL 2h = LVDS 3h = LVCMOS

3.106 R107 Register (Offset = 6Bh) [Reset = 00h]

R107 is shown in Table 3-108.

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Table 3-108. R107 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	Reserved
5	OUT7_CMOS_1P2V_EN	R/W	0h	OUT7 1.2V CMOS Enable. When the clock format of OUT7 is configured for one of the LVCMOS options, this bit determines if the CMOS clock voltage will be 1.2V or if it will match the VDDO_7 supply voltage. When the clock format of OUT7 is not configured for one of the LVCMOS options, this bit is ignored.
4	OUT6_CMOS_1P2V_EN	R/W	0h	OUT6 1.2V CMOS Enable. When the clock format of OUT6 is configured for one of the LVCMOS options, this bit determines if the CMOS clock voltage will be 1.2V or if it will match the VDDO_6 supply voltage. When the clock format of OUT6 is not configured for one of the LVCMOS options, this bit is ignored.
3	OUT5_CMOS_1P2V_EN	R/W	0h	OUT5 1.2V CMOS Enable. When the clock format of OUT5 is configured for one of the LVCMOS options, this bit determines if the CMOS clock voltage will be 1.2V or if it will match the VDDO_5 supply voltage. When the clock format of OUT5 is not configured for one of the LVCMOS options, this bit is ignored.
2	OUT4_CMOS_1P2V_EN	R/W	0h	OUT4 1.2V CMOS Enable. When the clock format of OUT4 is configured for one of the LVCMOS options, this bit determines if the CMOS clock voltage will be 1.2V or if it will match the VDDO_3_4 supply voltage. When the clock format of OUT4 is not configured for one of the LVCMOS options, this bit is ignored.
1	OUT3_CMOS_1P2V_EN	R/W	0h	OUT3 1.2V CMOS Enable. When the clock format of OUT3 is configured for one of the LVCMOS options, this bit determines if the CMOS clock voltage will be 1.2V or if it will match the VDDO_3_4 supply voltage. When the clock format of OUT3 is not configured for one of the LVCMOS options, this bit is ignored.
0	OUT2_CMOS_1P2V_EN	R/W	0h	OUT2 1.2V CMOS Enable. When the clock format of OUT2 is configured for one of the LVCMOS options, this bit determines if the CMOS clock voltage will be 1.2V or if it will match the VDDO_1_2 supply voltage. When the clock format of OUT2 is not configured for one of the LVCMOS options, this bit is ignored.

3.107 R108 Register (Offset = 6Ch) [Reset = BBh]

R108 is shown in Table 3-109.

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Table 3-109. R108 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	OUT1_OE_GRP	R/W	Bh	OUT1 Output Enable Group. This field determines whether or not OUT1 is assigned to an output enable group. If is assigned to an output enable group, this field also determines the output enable group assignment. If it is not assigned to an output enable group, this field also determines whether or not OUT1 can be affected by a global output enable pin or the global output enable register field. 0h = 0: OE_GROUP_0 1h = 1: OE_GROUP_1 2h = 2: OE_GROUP_2 3h = 3: OE_GROUP_3 4h = 4: OE_GROUP_4 5h = 5: OE_GROUP_5 6h = 6: OE_GROUP_6 7h = 7: OE_GROUP_7 8h = 8: OE_GROUP_8 9h = 9: OE_GROUP_9 Ah = 10: OE_GROUP_10 Bh = 11: Global OE Only; Not assigned. Affected by global output enable controls. Ch = 12: No OE Group; Not assigned. Not affected by global output enable controls.
3-0	OUT0_OE_GRP	R/W	Bh	OUT0 Output Enable Group. This field determines whether or not OUT0 is assigned to an output enable group. If is assigned to a group, this field also determines the group assignment. If not, this field also determines whether or not OUT0 can be affected by a global output enable pin or the global output enable register field. 0h = 0: OE_GROUP_0 1h = 1: OE_GROUP_1 2h = 2: OE_GROUP_2 3h = 3: OE_GROUP_3 4h = 4: OE_GROUP_4 5h = 5: OE_GROUP_5 6h = 6: OE_GROUP_6 7h = 7: OE_GROUP_7 8h = 8: OE_GROUP_8 9h = 9: OE_GROUP_9 Ah = 10: OE_GROUP_10 Bh = 11: Global OE Only; Not assigned. Affected by global output enable controls. Ch = 12: No OE Group; Not assigned. Not affected by global output enable controls.

3.108 R109 Register (Offset = 6Dh) [Reset = BBh]

R109 is shown in Table 3-110.

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Table 3-110. R109 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	OUT3_OE_GRP	R/W	Bh	OUT3 Output Enable Group. This field determines whether or not OUT3 is assigned to an output enable group. If is assigned to an output enable group, this field also determines the output enable group assignment. If it is not assigned to an output enable group, this field also determines whether or not OUT3 can be affected by a global output enable pin or the global output enable register field. 0h = 0: OE_GROUP_0 1h = 1: OE_GROUP_1 2h = 2: OE_GROUP_2 3h = 3: OE_GROUP_3 4h = 4: OE_GROUP_4 5h = 5: OE_GROUP_5 6h = 6: OE_GROUP_6 7h = 7: OE_GROUP_7 8h = 8: OE_GROUP_8 9h = 9: OE_GROUP_9 Ah = 10: OE_GROUP_10 Bh = 11: Global OE Only; Not assigned. Affected by global output enable controls. Ch = 12: No OE Group; Not assigned. Not affected by global output enable controls.
3-0	OUT2_OE_GRP	R/W	Bh	OUT2 Output Enable Group. This field determines whether or not OUT2 is assigned to an output enable group. If is assigned to an output enable group, this field also determines the output enable group assignment. If it is not assigned to an output enable group, this field also determines whether or not OUT2 can be affected by a global output enable pin or the global output enable register field. 0h = 0: OE_GROUP_0 1h = 1: OE_GROUP_1 2h = 2: OE_GROUP_2 3h = 3: OE_GROUP_3 4h = 4: OE_GROUP_4 5h = 5: OE_GROUP_5 6h = 6: OE_GROUP_6 7h = 7: OE_GROUP_7 8h = 8: OE_GROUP_8 9h = 9: OE_GROUP_9 Ah = 10: OE_GROUP_10 Bh = 11: Global OE Only; Not assigned. Affected by global output enable controls. Ch = 12: No OE Group; Not assigned. Not affected by global output enable controls.

3.109 R110 Register (Offset = 6Eh) [Reset = BBh]

R110 is shown in Table 3-111.

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Table 3-111. R110 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	OUT5_OE_GRP	R/W	Bh	OUT5 Output Enable Group. This field determines whether or not OUT5 is assigned to an output enable group. If is assigned to an output enable group, this field also determines the output enable group assignment. If it is not assigned to an output enable group, this field also determines whether or not OUT5 can be affected by a global output enable pin or the global output enable register field. 0h = 0: OE_GROUP_0 1h = 1: OE_GROUP_1 2h = 2: OE_GROUP_2 3h = 3: OE_GROUP_3 4h = 4: OE_GROUP_4 5h = 5: OE_GROUP_5 6h = 6: OE_GROUP_6 7h = 7: OE_GROUP_7 8h = 8: OE_GROUP_8 9h = 9: OE_GROUP_9 Ah = 10: OE_GROUP_10 Bh = 11: Global OE Only; Not assigned. Affected by global output enable controls. Ch = 12: No OE Group; Not assigned. Not affected by global output enable controls.
3-0	OUT4_OE_GRP	R/W	Bh	OUT4 Output Enable Group. This field determines whether or not OUT4 is assigned to an output enable group. If is assigned to an output enable group, this field also determines the output enable group assignment. If it is not assigned to an output enable group, this field also determines whether or not OUT4 can be affected by a global output enable pin or the global output enable register field. 0h = 0: OE_GROUP_0 1h = 1: OE_GROUP_1 2h = 2: OE_GROUP_2 3h = 3: OE_GROUP_3 4h = 4: OE_GROUP_4 5h = 5: OE_GROUP_5 6h = 6: OE_GROUP_6 7h = 7: OE_GROUP_7 8h = 8: OE_GROUP_8 9h = 9: OE_GROUP_9 Ah = 10: OE_GROUP_10 Bh = 11: Global OE Only; Not assigned. Affected by global output enable controls. Ch = 12: No OE Group; Not assigned. Not affected by global output enable controls.

3.110 R111 Register (Offset = 6Fh) [Reset = BBh]

R111 is shown in Table 3-112.

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Table 3-112. R111 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	OUT7_OE_GRP	R/W	Bh	OUT7 Output Enable Group. This field determines whether or not OUT7 is assigned to an output enable group. If is assigned to an output enable group, this field also determines the output enable group assignment. If it is not assigned to an output enable group, this field also determines whether or not OUT7 can be affected by a global output enable pin or the global output enable register field. 0h = 0: OE_GROUP_0 1h = 1: OE_GROUP_1 2h = 2: OE_GROUP_2 3h = 3: OE_GROUP_3 4h = 4: OE_GROUP_4 5h = 5: OE_GROUP_5 6h = 6: OE_GROUP_6 7h = 7: OE_GROUP_7 8h = 8: OE_GROUP_8 9h = 9: OE_GROUP_9 Ah = 10: OE_GROUP_10 Bh = 11: Global OE Only; Not assigned. Affected by global output enable controls. Ch = 12: No OE Group; Not assigned. Not affected by global output enable controls.
3-0	OUT6_OE_GRP	R/W	Bh	OUT6 Output Enable Group. This field determines whether or not OUT6 is assigned to an output enable group. If is assigned to an output enable group, this field also determines the output enable group assignment. If it is not assigned to an output enable group, this field also determines whether or not OUT6 can be affected by a global output enable pin or the global output enable register field. 0h = 0: OE_GROUP_0 1h = 1: OE_GROUP_1 2h = 2: OE_GROUP_2 3h = 3: OE_GROUP_3 4h = 4: OE_GROUP_4 5h = 5: OE_GROUP_5 6h = 6: OE_GROUP_6 7h = 7: OE_GROUP_7 8h = 8: OE_GROUP_8 9h = 9: OE_GROUP_9 Ah = 10: OE_GROUP_10 Bh = 11: Global OE Only; Not assigned. Affected by global output enable controls. Ch = 12: No OE Group; Not assigned. Not affected by global output enable controls.

3.111 R112 Register (Offset = 70h) [Reset = 99h]

R112 is shown in Table 3-113.

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Table 3-113. R112 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	OUT1_LPHCSL_VOD_SEL	R/W	9h	Programmable LP-HCSL swing for channel 1 0h = 686 mV 1h = 714 mV 2h = 741 mV 3h = 768 mV 4h = 793 mV 5h = 817 mV 6h = 794 mV 7h = 820 mV 8h = 823 mV 9h = 847 mV Ah = 872 mV Bh = 896 mV Ch = 921 mV Dh = 945 mV Eh = 969 mV Fh = 993 mV
3-0	OUT0_LPHCSL_VOD_SEL	R/W	9h	Programmable LP-HCSL swing for channel 0 0h = 686 mV 1h = 714 mV 2h = 741 mV 3h = 768 mV 4h = 793 mV 5h = 817 mV 6h = 794 mV 7h = 820 mV 8h = 823 mV 9h = 847 mV Ah = 872 mV Bh = 896 mV Ch = 921 mV Dh = 945 mV Eh = 969 mV Fh = 993 mV

3.112 R113 Register (Offset = 71h) [Reset = 99h]

R113 is shown in Table 3-114.

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Table 3-114. R113 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	OUT3_LPHCSL_VOD_SEL	R/W	9h	Programmable LP-HCSL swing for channel 3 0h = 686 mV 1h = 714 mV 2h = 741 mV 3h = 768 mV 4h = 793 mV 5h = 817 mV 6h = 794 mV 7h = 820 mV 8h = 823 mV 9h = 847 mV Ah = 872 mV Bh = 896 mV Ch = 921 mV Dh = 945 mV Eh = 969 mV Fh = 993 mV
3-0	OUT2_LPHCSL_VOD_SEL	R/W	9h	Programmable LP-HCSL swing for channel 2 0h = 686 mV 1h = 714 mV 2h = 741 mV 3h = 768 mV 4h = 793 mV 5h = 817 mV 6h = 794 mV 7h = 820 mV 8h = 823 mV 9h = 847 mV Ah = 872 mV Bh = 896 mV Ch = 921 mV Dh = 945 mV Eh = 969 mV Fh = 993 mV

3.113 R114 Register (Offset = 72h) [Reset = 99h]

R114 is shown in Table 3-115.

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Table 3-115. R114 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	OUT5_LPHCSL_VOD_SEL	R/W	9h	Programmable LP-HCSL swing for channel 5 0h = 686 mV 1h = 714 mV 2h = 741 mV 3h = 768 mV 4h = 793 mV 5h = 817 mV 6h = 794 mV 7h = 820 mV 8h = 823 mV 9h = 847 mV Ah = 872 mV Bh = 896 mV Ch = 921 mV Dh = 945 mV Eh = 969 mV Fh = 993 mV
3-0	OUT4_LPHCSL_VOD_SEL	R/W	9h	Programmable LP-HCSL swing for channel 4 0h = 686 mV 1h = 714 mV 2h = 741 mV 3h = 768 mV 4h = 793 mV 5h = 817 mV 6h = 794 mV 7h = 820 mV 8h = 823 mV 9h = 847 mV Ah = 872 mV Bh = 896 mV Ch = 921 mV Dh = 945 mV Eh = 969 mV Fh = 993 mV

3.114 R115 Register (Offset = 73h) [Reset = 99h]

R115 is shown in Table 3-116.

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Table 3-116. R115 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	OUT7_LPHCSL_VOD_SEL	R/W	9h	Programmable LP-HCSL swing for channel 7 0h = 686 mV 1h = 714 mV 2h = 741 mV 3h = 768 mV 4h = 793 mV 5h = 817 mV 6h = 794 mV 7h = 820 mV 8h = 823 mV 9h = 847 mV Ah = 872 mV Bh = 896 mV Ch = 921 mV Dh = 945 mV Eh = 969 mV Fh = 993 mV
3-0	OUT6_LPHCSL_VOD_SEL	R/W	9h	Programmable LP-HCSL swing for channel 6 0h = 686 mV 1h = 714 mV 2h = 741 mV 3h = 768 mV 4h = 793 mV 5h = 817 mV 6h = 794 mV 7h = 820 mV 8h = 823 mV 9h = 847 mV Ah = 872 mV Bh = 896 mV Ch = 921 mV Dh = 945 mV Eh = 969 mV Fh = 993 mV

3.115 R116 Register (Offset = 74h) [Reset = 00h]

R116 is shown in Table 3-117.

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Table 3-117. R116 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	OUT3_SYNC_MODE	R/W	0h	OUT3 Synchronization Mode. Selects the output clock synchronization mode for OUT3. To phase synchronize a group of output clocks, set the synchronization mode of each clock in the group to "Full Sync Mode", and either assign each output clock to the same output enable group or use a global output enable control. If phase synchronization is not necessary, to guarantee at least 4 output clock cycles of delay between output enable assertion and the first output clock edge, set this field to "Self Sync Mode". For minimal delay, set this field to "No Sync Mode". 0h = Full Sync; To phase synchronize a group of output clocks, set the synchronization mode of each clock in the group to "Full Sync Mode", and either assign each output clock to the same output enable group or use a global output enable control. 1h = No Sync; For minimal delay, set this field to "No Sync Mode" 2h = Self Sync; If phase synchronization is not necessary, to guarantee at least 4 output clock cycles of delay between output enable assertion and the first output clock edge, set this field to "Self Sync Mode". 3h = Reserved
5-4	OUT2_SYNC_MODE	R/W	0h	OUT2 Synchronization Mode. Selects the output clock synchronization mode for OUT2. To phase synchronize a group of output clocks, set the synchronization mode of each clock in the group to "Full Sync Mode", and either assign each output clock to the same output enable group or use a global output enable control. If phase synchronization is not necessary, to guarantee at least 4 output clock cycles of delay between output enable assertion and the first output clock edge, set this field to "Self Sync Mode". For minimal delay, set this field to "No Sync Mode". 0h = Full Sync; To phase synchronize a group of output clocks, set the synchronization mode of each clock in the group to "Full Sync Mode", and either assign each output clock to the same output enable group or use a global output enable control. 1h = No Sync; For minimal delay, set this field to "No Sync Mode" 2h = Self Sync; If phase synchronization is not necessary, to guarantee at least 4 output clock cycles of delay between output enable assertion and the first output clock edge, set this field to "Self Sync Mode". 3h = Reserved
3-2	OUT1_SYNC_MODE	R/W	0h	OUT1 Synchronization Mode. Selects the output clock synchronization mode for OUT1. To phase synchronize a group of output clocks, set the synchronization mode of each clock in the group to "Full Sync Mode", and either assign each output clock to the same output enable group or use a global output enable control. If phase synchronization is not necessary, to guarantee at least 4 output clock cycles of delay between output enable assertion and the first output clock edge, set this field to "Self Sync Mode". For minimal delay, set this field to "No Sync Mode". 0h = Full Sync; To phase synchronize a group of output clocks, set the synchronization mode of each clock in the group to "Full Sync Mode", and either assign each output clock to the same output enable group or use a global output enable control. 1h = No Sync; For minimal delay, set this field to "No Sync Mode" 2h = Self Sync; If phase synchronization is not necessary, to guarantee at least 4 output clock cycles of delay between output enable assertion and the first output clock edge, set this field to "Self Sync Mode". 3h = Reserved

Table 3-117. R116 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1-0	OUT0_SYNC_MODE	R/W	0h	OUT0 Synchronization Mode. Selects the output clock synchronization mode for OUT0. To phase synchronize a group of output clocks, set the synchronization mode of each clock in the group to "Full Sync Mode", and either assign each output clock to the same output enable group or use a global output enable control. If phase synchronization is not necessary, to guarantee at least 4 output clock cycles of delay between output enable assertion and the first output clock edge, set this field to "Self Sync Mode". For minimal delay, set this field to "No Sync Mode". 0h = Full Sync; To phase synchronize a group of output clocks, set the synchronization mode of each clock in the group to "Full Sync Mode", and either assign each output clock to the same output enable group or use a global output enable control. 1h = No Sync; For minimal delay, set this field to "No Sync Mode" 2h = Self Sync; If phase synchronization is not necessary, to guarantee at least 4 output clock cycles of delay between output enable assertion and the first output clock edge, set this field to "Self Sync Mode". 3h = Reserved

3.116 R117 Register (Offset = 75h) [Reset = 00h]

R117 is shown in Table 3-118.

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Table 3-118. R117 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	OUT7_SYNC_MODE	R/W	0h	OUT7 Synchronization Mode. Selects the output clock synchronization mode for OUT7. To phase synchronize a group of output clocks, set the synchronization mode of each clock in the group to "Full Sync Mode", and either assign each output clock to the same output enable group or use a global output enable control. If phase synchronization is not necessary, to guarantee at least 4 output clock cycles of delay between output enable assertion and the first output clock edge, set this field to "Self Sync Mode". For minimal delay, set this field to "No Sync Mode". 0h = Full Sync; To phase synchronize a group of output clocks, set the synchronization mode of each clock in the group to "Full Sync Mode", and either assign each output clock to the same output enable group or use a global output enable control. 1h = No Sync; For minimal delay, set this field to "No Sync Mode" 2h = Self Sync; If phase synchronization is not necessary, to guarantee at least 4 output clock cycles of delay between output enable assertion and the first output clock edge, set this field to "Self Sync Mode". 3h = Reserved
5-4	OUT6_SYNC_MODE	R/W	0h	OUT6 Synchronization Mode. Selects the output clock synchronization mode for OUT6. To phase synchronize a group of output clocks, set the synchronization mode of each clock in the group to "Full Sync Mode", and either assign each output clock to the same output enable group or use a global output enable control. If phase synchronization is not necessary, to guarantee at least 4 output clock cycles of delay between output enable assertion and the first output clock edge, set this field to "Self Sync Mode". For minimal delay, set this field to "No Sync Mode". 0h = Full Sync; To phase synchronize a group of output clocks, set the synchronization mode of each clock in the group to "Full Sync Mode", and either assign each output clock to the same output enable group or use a global output enable control. 1h = No Sync; For minimal delay, set this field to "No Sync Mode" 2h = Self Sync; If phase synchronization is not necessary, to guarantee at least 4 output clock cycles of delay between output enable assertion and the first output clock edge, set this field to "Self Sync Mode". 3h = Reserved
3-2	OUT5_SYNC_MODE	R/W	0h	OUT5 Synchronization Mode. Selects the output clock synchronization mode for OUT5. To phase synchronize a group of output clocks, set the synchronization mode of each clock in the group to "Full Sync Mode", and either assign each output clock to the same output enable group or use a global output enable control. If phase synchronization is not necessary, to guarantee at least 4 output clock cycles of delay between output enable assertion and the first output clock edge, set this field to "Self Sync Mode". For minimal delay, set this field to "No Sync Mode". 0h = Full Sync; To phase synchronize a group of output clocks, set the synchronization mode of each clock in the group to "Full Sync Mode", and either assign each output clock to the same output enable group or use a global output enable control. 1h = No Sync; For minimal delay, set this field to "No Sync Mode" 2h = Self Sync; If phase synchronization is not necessary, to guarantee at least 4 output clock cycles of delay between output enable assertion and the first output clock edge, set this field to "Self Sync Mode". 3h = Reserved

Table 3-118. R117 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1-0	OUT4_SYNC_MODE	R/W	0h	OUT4 Synchronization Mode. Selects the output clock synchronization mode for OUT4. To phase synchronize a group of output clocks, set the synchronization mode of each clock in the group to "Full Sync Mode", and either assign each output clock to the same output enable group or use a global output enable control. If phase synchronization is not necessary, to guarantee at least 4 output clock cycles of delay between output enable assertion and the first output clock edge, set this field to "Self Sync Mode". For minimal delay, set this field to "No Sync Mode". 0h = Full Sync; To phase synchronize a group of output clocks, set the synchronization mode of each clock in the group to "Full Sync Mode", and either assign each output clock to the same output enable group or use a global output enable control. 1h = No Sync; For minimal delay, set this field to "No Sync Mode" 2h = Self Sync; If phase synchronization is not necessary, to guarantee at least 4 output clock cycles of delay between output enable assertion and the first output clock edge, set this field to "Self Sync Mode". 3h = Reserved

3.117 R118 Register (Offset = 76h) [Reset = FEh]

R118 is shown in Table 3-119.

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Table 3-119. R118 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	OUT3P_OE_CMOS	R/W	1h	OUT3P LVCMOS Output Enable. Controls whether or not OUT3P can produce an LVCMOS clock. For OUT3P to drive an LVCMOS clock, OUT3 must be enabled by all other output enable logic, OUT3 must be configured for an LVCMOS format that uses that pin, and this bit must be set to 0x1.
6	OUT2N_OE_CMOS	R/W	1h	OUT2N LVCMOS Output Enable. Controls whether or not OUT2N can produce an LVCMOS clock. For OUT2N to drive an LVCMOS clock, OUT2 must be enabled by all other output enable logic, OUT2 must be configured for an LVCMOS format that uses that pin, and this bit must be set to 0x1.
5	OUT2P_OE_CMOS	R/W	1h	OUT2P LVCMOS Output Enable. Controls whether or not OUT2P can produce an LVCMOS clock. For OUT2P to drive an LVCMOS clock, OUT2 must be enabled by all other output enable logic, OUT2 must be configured for an LVCMOS format that uses that pin, and this bit must be set to 0x1.
4	OUT1N_OE_CMOS	R/W	1h	OUT1N LVCMOS Output Enable. Controls whether or not OUT1N can produce an LVCMOS clock. For OUT1N to drive an LVCMOS clock, OUT1 must be enabled by all other output enable logic, OUT1 must be configured for an LVCMOS format that uses that pin, and this bit must be set to 0x1.
3	OUT1P_OE_CMOS	R/W	1h	OUT1P LVCMOS Output Enable. Controls whether or not OUT1P can produce an LVCMOS clock. For OUT1P to drive an LVCMOS clock, OUT1 must be enabled by all other output enable logic, OUT1 must be configured for an LVCMOS format that uses that pin, and this bit must be set to 0x1.
2	OUT0N_OE_CMOS	R/W	1h	OUT0N LVCMOS Output Enable. Controls whether or not OUT0N can produce an LVCMOS clock. For OUT0N to drive an LVCMOS clock, OUT0 must be enabled by all other output enable logic, OUT0 must be configured for an LVCMOS format that uses that pin, and this bit must be set to 0x1.
1	OUT0P_OE_CMOS	R/W	1h	OUT0P LVCMOS Output Enable. Controls whether or not OUT0P can produce an LVCMOS clock. For OUT0P to drive an LVCMOS clock, OUT0 must be enabled by all other output enable logic, OUT0 must be configured for an LVCMOS format that uses that pin, and this bit must be set to 0x1.
0	SINGLE_CMOS_EN_SYNC	R/W	0h	Global Single LVCMOS Enable Synchronization. Each differential output clock pair can be used as two LVCMOS clocks. These two clocks can be enabled/disabled using their respective OUTx_OE_CMOS_P or OUTx_OE_CMOS_N. This field, when set to 0x1, ensures that the enable/disable of the individual LVCMOS clocks, is synchronous with the output clock, such that there will be no runt pulses. 0h = Immediate; Immediately enable/disable the LVCMOS clocks, there may be runt pulses. 1h = Glitchless; Ensures that the enable/disable of the individual LVCMOS clocks, is synchronous with the output clock, such that there will be no runt pulses.

3.118 R119 Register (Offset = 77h) [Reset = FFh]

R119 is shown in Table 3-120.

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Table 3-120. R119 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	OUT7P_OE_CMOS	R/W	1h	OUT7P LVCMOS Output Enable. Controls whether or not OUT7P can produce an LVCMOS clock. For OUT7P to drive an LVCMOS clock, OUT7 must be enabled by all other output enable logic, OUT7 must be configured for an LVCMOS format that uses that pin, and this bit must be set to 0x1.
6	OUT6N_OE_CMOS	R/W	1h	OUT6N LVCMOS Output Enable. Controls whether or not OUT6N can produce an LVCMOS clock. For OUT6N to drive an LVCMOS clock, OUT6 must be enabled by all other output enable logic, OUT6 must be configured for an LVCMOS format that uses that pin, and this bit must be set to 0x1.
5	OUT6P_OE_CMOS	R/W	1h	OUT6P LVCMOS Output Enable. Controls whether or not OUT6P can produce an LVCMOS clock. For OUT6P to drive an LVCMOS clock, OUT6 must be enabled by all other output enable logic, OUT6 must be configured for an LVCMOS format that uses that pin, and this bit must be set to 0x1.
4	OUT5N_OE_CMOS	R/W	1h	OUT5N LVCMOS Output Enable. Controls whether or not OUT5N can produce an LVCMOS clock. For OUT5N to drive an LVCMOS clock, OUT5 must be enabled by all other output enable logic, OUT5 must be configured for an LVCMOS format that uses that pin, and this bit must be set to 0x1.
3	OUT5P_OE_CMOS	R/W	1h	OUT5P LVCMOS Output Enable. Controls whether or not OUT5P can produce an LVCMOS clock. For OUT5P to drive an LVCMOS clock, OUT5 must be enabled by all other output enable logic, OUT5 must be configured for an LVCMOS format that uses that pin, and this bit must be set to 0x1.
2	OUT4N_OE_CMOS	R/W	1h	OUT4N LVCMOS Output Enable. Controls whether or not OUT4N can produce an LVCMOS clock. For OUT4N to drive an LVCMOS clock, OUT4 must be enabled by all other output enable logic, OUT4 must be configured for an LVCMOS format that uses that pin, and this bit must be set to 0x1.
1	OUT4P_OE_CMOS	R/W	1h	OUT4P LVCMOS Output Enable. Controls whether or not OUT4P can produce an LVCMOS clock. For OUT4P to drive an LVCMOS clock, OUT4 must be enabled by all other output enable logic, OUT4 must be configured for an LVCMOS format that uses that pin, and this bit must be set to 0x1.
0	OUT3N_OE_CMOS	R/W	1h	OUT3N LVCMOS Output Enable. Controls whether or not OUT3N can produce an LVCMOS clock. For OUT3N to drive an LVCMOS clock, OUT3 must be enabled by all other output enable logic, OUT3 must be configured for an LVCMOS format that uses that pin, and this bit must be set to 0x1.

3.119 R120 Register (Offset = 78h) [Reset = 01h]

R120 is shown in Table 3-121.

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Table 3-121. R120 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	OUT6_FREQ_DET_EN	R/W	0h	OUT6 Frequency Detector Enable. Enables the frequency detectors for OUT6P and OUT6N. These detect when the output clock frequency is below the threshold specified with OUT6_FREQ_DET_THRESH.
6	OUT5_FREQ_DET_EN	R/W	0h	OUT5 Frequency Detector Enable. Enables the frequency detectors for OUT5P and OUT5N. These detect when the output clock frequency is below the threshold specified with OUT5_FREQ_DET_THRESH.
5	OUT4_FREQ_DET_EN	R/W	0h	OUT4 Frequency Detector Enable. Enables the frequency detectors for OUT4P and OUT4N. These detect when the output clock frequency is below the threshold specified with OUT4_FREQ_DET_THRESH.
4	OUT3_FREQ_DET_EN	R/W	0h	OUT3 Frequency Detector Enable. Enables the frequency detectors for OUT3P and OUT3N. These detect when the output clock frequency is below the threshold specified with OUT3_FREQ_DET_THRESH.
3	OUT2_FREQ_DET_EN	R/W	0h	OUT2 Frequency Detector Enable. Enables the frequency detectors for OUT2P and OUT2N. These detect when the output clock frequency is below the threshold specified with OUT2_FREQ_DET_THRESH.
2	OUT1_FREQ_DET_EN	R/W	0h	OUT1 Frequency Detector Enable. Enables the frequency detectors for OUT1P and OUT1N. These detect when the output clock frequency is below the threshold specified with OUT1_FREQ_DET_THRESH.
1	OUT0_FREQ_DET_EN	R/W	0h	OUT0 Frequency Detector Enable. Enables the frequency detectors for OUT0P and OUT0N. These detect when the output clock frequency is below the threshold specified with OUT0_FREQ_DET_THRESH.
0	OUT7N_OE_CMOS	R/W	1h	OUT7N LVCMOS Output Enable. Controls whether or not OUT7N can produce an LVCMOS clock. For OUT7N to drive an LVCMOS clock, OUT7 must be enabled by all other output enable logic, OUT7 must be configured for an LVCMOS format that uses that pin, and this bit must be set to 0x1.

3.120 R121 Register (Offset = 79h) [Reset = 01h]

R121 is shown in Table 3-122.

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Table 3-122. R121 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0h	Reserved
0	IN2_LOS	R/W	1h	IN2 Loss-of-Signal. This is set to 1 to indicate that IN2 is currently invalid. 0h = IN2 Valid 1h = IN2 Invalid

3.121 R122 Register (Offset = 7Ah) [Reset = 00h]

R122 is shown in Table 3-123.

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Table 3-123. R122 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	OUT4_FREQ_DET_THRESH	R/W	0h	OUT4 Frequency Detector Threshold. Sets the frequency threshold that will be used by the OUT4 Frequency Detector to determine if OUT4P and OUT4N are valid or not. 0h = 1 MHz 1h = 25 MHz
6	OUT3_FREQ_DET_THRESH	R/W	0h	OUT3 Frequency Detector Threshold. Sets the frequency threshold that will be used by the OUT3 Frequency Detector to determine if OUT3P and OUT3N are valid or not. 0h = 1 MHz 1h = 25 MHz
5	OUT2_FREQ_DET_THRESH	R/W	0h	OUT2 Frequency Detector Threshold. Sets the frequency threshold that will be used by the OUT2 Frequency Detector to determine if OUT2P and OUT2N are valid or not. 0h = 1 MHz 1h = 25 MHz
4	OUT1_FREQ_DET_THRESH	R/W	0h	OUT1 Frequency Detector Threshold. Sets the frequency threshold that will be used by the OUT1 Frequency Detector to determine if OUT1P and OUT1N are valid or not. 0h = 1 MHz 1h = 25 MHz
3	OUT0_FREQ_DET_THRESH	R/W	0h	OUT0 Frequency Detector Threshold. Sets the frequency threshold that will be used by the OUT0 Frequency Detector to determine if OUT0P and OUT0N are valid or not. 0h = 1 MHz 1h = 25 MHz
2-1	RESERVED	R	0h	Reserved
0	OUT7_FREQ_DET_EN	R/W	0h	OUT7 Frequency Detector Enable. Enables the frequency detectors for OUT7P and OUT7N. These detect when the output clock frequency is below the threshold specified with OUT7_FREQ_DET_THRESH.

3.122 R123 Register (Offset = 7Bh) [Reset = 00h]

R123 is shown in Table 3-124.

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Table 3-124. R123 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	OUT2_AMP_DET_EN	R/W	0h	OUT2 Amplitude Detector Enable. Enables the amplitude detectors for OUT2P and OUT2N. These detect when the output clock amplitude is below the threshold specified with OUT_AMP_DET_THRESH.
6	OUT1_AMP_DET_EN	R/W	0h	OUT1 Amplitude Detector Enable. Enables the amplitude detectors for OUT1P and OUT1N. These detect when the output clock amplitude is below the threshold specified with OUT_AMP_DET_THRESH.
5	OUT0_AMP_DET_EN	R/W	0h	OUT0 Amplitude Detector Enable. Enables the amplitude detectors for OUT0P and OUT0N. These detect when the output clock amplitude is below the threshold specified with OUT_AMP_DET_THRESH.
4-3	RESERVED	R	0h	Reserved
2	OUT7_FREQ_DET_THRESH	R/W	0h	OUT7 Frequency Detector Threshold. Sets the frequency threshold that will be used by the OUT7 Frequency Detector to determine if OUT7P and OUT7N are valid or not. 0h = 1 MHz 1h = 25 MHz
1	OUT6_FREQ_DET_THRESH	R/W	0h	OUT6 Frequency Detector Threshold. Sets the frequency threshold that will be used by the OUT6 Frequency Detector to determine if OUT6P and OUT6N are valid or not. 0h = 1 MHz 1h = 25 MHz
0	OUT5_FREQ_DET_THRESH	R/W	0h	OUT5 Frequency Detector Threshold. Sets the frequency threshold that will be used by the OUT5 Frequency Detector to determine if OUT5P and OUT5N are valid or not. 0h = 1 MHz 1h = 25 MHz

3.123 R124 Register (Offset = 7Ch) [Reset = 00h]

R124 is shown in Table 3-125.

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Table 3-125. R124 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	OUT_AMP_DET_THRESH	R/W	0h	OUTx Amplitude Detector Threshold. Sets the amplitude threshold that will be used by all of the output amplitude detectors. 0h = 100 mV/300 mV 1h = 150 mV / 350 mV
6-5	RESERVED	R	0h	Reserved
4	OUT7_AMP_DET_EN	R/W	0h	OUT7 Amplitude Detector Enable. Enables the amplitude detectors for OUT7P and OUT7N. These detect when the output clock amplitude is below the threshold specified with OUT_AMP_DET_THRESH.
3	OUT6_AMP_DET_EN	R/W	0h	OUT6 Amplitude Detector Enable. Enables the amplitude detectors for OUT6P and OUT6N. These detect when the output clock amplitude is below the threshold specified with OUT_AMP_DET_THRESH.
2	OUT5_AMP_DET_EN	R/W	0h	OUT5 Amplitude Detector Enable. Enables the amplitude detectors for OUT5P and OUT5N. These detect when the output clock amplitude is below the threshold specified with OUT_AMP_DET_THRESH.
1	OUT4_AMP_DET_EN	R/W	0h	OUT4 Amplitude Detector Enable. Enables the amplitude detectors for OUT4P and OUT4N. These detect when the output clock amplitude is below the threshold specified with OUT_AMP_DET_THRESH.
0	OUT3_AMP_DET_EN	R/W	0h	OUT3 Amplitude Detector Enable. Enables the amplitude detectors for OUT3P and OUT3N. These detect when the output clock amplitude is below the threshold specified with OUT_AMP_DET_THRESH.

3.124 R125 Register (Offset = 7Dh) [Reset = 00h]

R125 is shown in Table 3-126.

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Table 3-126. R125 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CRC_ERROR_EVT_INTR_EN	R/W	0h	OTP CRC Event Interrupt Enable. The value of this field determines whether or not the OTP CRC Error contributes to the Device Interrupt
6	IN2_LOS_LMT_EVT_INTR_EN	R/W	0h	IN2 Loss-of-Signal Limit Event Interrupt Enable. The value of this field determines whether or not the IN2 Loss-of-Signal Limit Event contributes to the Device Interrupt
5	IN1_LOS_LMT_EVT_INTR_EN	R/W	0h	IN1 Loss-of-Signal Limit Event Interrupt Enable. The value of this field determines whether or not the IN1 Loss-of-Signal Limit Event contributes to the Device Interrupt
4	IN0_LOS_LMT_EVT_INTR_EN	R/W	0h	IN0 Loss-of-Signal Limit Event Interrupt Enable. The value of this field determines whether or not the IN0 Loss-of-Signal Limit Event contributes to the Device Interrupt
3	IN2_LOS_EVT_INTR_EN	R/W	0h	IN2 Loss-of-Signal Event Interrupt Enable. The value of this field determines whether or not the IN2 Loss-of-Signal Event contributes to the Device Interrupt
2	IN1_LOS_EVT_INTR_EN	R/W	0h	IN1 Loss-of-Signal Event Interrupt Enable. The value of this field determines whether or not the IN1 Loss-of-Signal Event contributes to the Device Interrupt
1	IN0_LOS_EVT_INTR_EN	R/W	0h	IN0 Loss-of-Signal Event Interrupt Enable. The value of this field determines whether or not the IN0 Loss-of-Signal Event contributes to the Device Interrupt
0	DEV_INTR	R	0h	Device Interrupt. Indicates if one or more enabled interrupts have been asserted. Once this field is set, it is cleared only when all contributing interrupt event status fields have been cleared via I2C. The enables for each of the interrupt flags are not stored in OTP, and must be set through I2C after startup for interrupt detection.

3.125 R126 Register (Offset = 7Eh) [Reset = 00h]

R126 is shown in Table 3-127.

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Table 3-127. R126 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	OUT3N_FREQ_ERR_EVT_INTR_EN	R/W	0h	OUT3N Frequency Error Event Interrupt Enable. Determines whether or not assertions of OUT3N_FREQ_ERR_EVT should contribute to the device interrupt signal.
6	OUT3P_FREQ_ERR_EVT_INTR_EN	R/W	0h	OUT3P Frequency Error Event Interrupt Enable. Determines whether or not assertions of OUT3P_FREQ_ERR_EVT should contribute to the device interrupt signal.
5	OUT2N_FREQ_ERR_EVT_INTR_EN	R/W	0h	OUT2N Frequency Error Event Interrupt Enable. Determines whether or not assertions of OUT2N_FREQ_ERR_EVT should contribute to the device interrupt signal.
4	OUT2P_FREQ_ERR_EVT_INTR_EN	R/W	0h	OUT2P Frequency Error Event Interrupt Enable. Determines whether or not assertions of OUT2P_FREQ_ERR_EVT should contribute to the device interrupt signal.
3	OUT1N_FREQ_ERR_EVT_INTR_EN	R/W	0h	OUT1N Frequency Error Event Interrupt Enable. Determines whether or not assertions of OUT1N_FREQ_ERR_EVT should contribute to the device interrupt signal.
2	OUT1P_FREQ_ERR_EVT_INTR_EN	R/W	0h	OUT1P Frequency Error Event Interrupt Enable. Determines whether or not assertions of OUT1P_FREQ_ERR_EVT should contribute to the device interrupt signal.
1	OUT0N_FREQ_ERR_EVT_INTR_EN	R/W	0h	OUT0N Frequency Error Event Interrupt Enable. Determines whether or not assertions of OUT0N_FREQ_ERR_EVT should contribute to the device interrupt signal.
0	OUT0P_FREQ_ERR_EVT_INTR_EN	R/W	0h	OUT0P Frequency Error Event Interrupt Enable. Determines whether or not assertions of OUT0P_FREQ_ERR_EVT should contribute to the device interrupt signal.

3.126 R127 Register (Offset = 7Fh) [Reset = 00h]

R127 is shown in Table 3-128.

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Table 3-128. R127 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	OUT7N_FREQ_ERR_EVT_INTR_EN	R/W	0h	OUT7N Frequency Error Event Interrupt Enable. Determines whether or not assertions of OUT7N_FREQ_ERR_EVT should contribute to the device interrupt signal.
6	OUT7P_FREQ_ERR_EVT_INTR_EN	R/W	0h	OUT7P Frequency Error Event Interrupt Enable. Determines whether or not assertions of OUT7P_FREQ_ERR_EVT should contribute to the device interrupt signal.
5	OUT6N_FREQ_ERR_EVT_INTR_EN	R/W	0h	OUT6N Frequency Error Event Interrupt Enable. Determines whether or not assertions of OUT6N_FREQ_ERR_EVT should contribute to the device interrupt signal.
4	OUT6P_FREQ_ERR_EVT_INTR_EN	R/W	0h	OUT6P Frequency Error Event Interrupt Enable. Determines whether or not assertions of OUT6P_FREQ_ERR_EVT should contribute to the device interrupt signal.
3	OUT5N_FREQ_ERR_EVT_INTR_EN	R/W	0h	OUT5N Frequency Error Event Interrupt Enable. Determines whether or not assertions of OUT5N_FREQ_ERR_EVT should contribute to the device interrupt signal.
2	OUT5P_FREQ_ERR_EVT_INTR_EN	R/W	0h	OUT5P Frequency Error Event Interrupt Enable. Determines whether or not assertions of OUT5P_FREQ_ERR_EVT should contribute to the device interrupt signal.
1	OUT4N_FREQ_ERR_EVT_INTR_EN	R/W	0h	OUT4N Frequency Error Event Interrupt Enable. Determines whether or not assertions of OUT4N_FREQ_ERR_EVT should contribute to the device interrupt signal.
0	OUT4P_FREQ_ERR_EVT_INTR_EN	R/W	0h	OUT4P Frequency Error Event Interrupt Enable. Determines whether or not assertions of OUT4P_FREQ_ERR_EVT should contribute to the device interrupt signal.

3.127 R128 Register (Offset = 80h) [Reset = 00h]

R128 is shown in Table 3-129.

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Table 3-129. R128 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	OUT2N_AMP_ERR_EVT_INTR_EN	R/W	0h	OUT2N Amplitude Error Event Interrupt Enable. Determines whether or not assertions of OUT2N_AMP_ERR_EVT should contribute to the device interrupt signal.
6	OUT2P_AMP_ERR_EVT_INTR_EN	R/W	0h	OUT2P Amplitude Error Event Interrupt Enable. Determines whether or not assertions of OUT2P_AMP_ERR_EVT should contribute to the device interrupt signal.
5	OUT1N_AMP_ERR_EVT_INTR_EN	R/W	0h	OUT1N Amplitude Error Event Interrupt Enable. Determines whether or not assertions of OUT1N_AMP_ERR_EVT should contribute to the device interrupt signal.
4	OUT1P_AMP_ERR_EVT_INTR_EN	R/W	0h	OUT1P Amplitude Error Event Interrupt Enable. Determines whether or not assertions of OUT1P_AMP_ERR_EVT should contribute to the device interrupt signal.
3	OUT0N_AMP_ERR_EVT_INTR_EN	R/W	0h	OUT0N Amplitude Error Event Interrupt Enable. Determines whether or not assertions of OUT0N_AMP_ERR_EVT should contribute to the device interrupt signal.
2	OUT0P_AMP_ERR_EVT_INTR_EN	R/W	0h	OUT0P Amplitude Error Event Interrupt Enable. Determines whether or not assertions of OUT0P_AMP_ERR_EVT should contribute to the device interrupt signal.
1-0	RESERVED	R	0h	Reserved

3.128 R129 Register (Offset = 81h) [Reset = 00h]

R129 is shown in Table 3-130.

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Table 3-130. R129 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	OUT6N_AMP_ERR_EVT_INTR_EN	R/W	0h	OUT6N Amplitude Error Event Interrupt Enable. Determines whether or not assertions of OUT6N_AMP_ERR_EVT should contribute to the device interrupt signal.
6	OUT6P_AMP_ERR_EVT_INTR_EN	R/W	0h	OUT6P Amplitude Error Event Interrupt Enable. Determines whether or not assertions of OUT6P_AMP_ERR_EVT should contribute to the device interrupt signal.
5	OUT5N_AMP_ERR_EVT_INTR_EN	R/W	0h	OUT5N Amplitude Error Event Interrupt Enable. Determines whether or not assertions of OUT5N_AMP_ERR_EVT should contribute to the device interrupt signal.
4	OUT5P_AMP_ERR_EVT_INTR_EN	R/W	0h	OUT5P Amplitude Error Event Interrupt Enable. Determines whether or not assertions of OUT5P_AMP_ERR_EVT should contribute to the device interrupt signal.
3	OUT4N_AMP_ERR_EVT_INTR_EN	R/W	0h	OUT4N Amplitude Error Event Interrupt Enable. Determines whether or not assertions of OUT4N_AMP_ERR_EVT should contribute to the device interrupt signal.
2	OUT4P_AMP_ERR_EVT_INTR_EN	R/W	0h	OUT4P Amplitude Error Event Interrupt Enable. Determines whether or not assertions of OUT4P_AMP_ERR_EVT should contribute to the device interrupt signal.
1	OUT3N_AMP_ERR_EVT_INTR_EN	R/W	0h	OUT3N Amplitude Error Event Interrupt Enable. Determines whether or not assertions of OUT3N_AMP_ERR_EVT should contribute to the device interrupt signal.
0	OUT3P_AMP_ERR_EVT_INTR_EN	R/W	0h	OUT3P Amplitude Error Event Interrupt Enable. Determines whether or not assertions of OUT3P_AMP_ERR_EVT should contribute to the device interrupt signal.

3.129 R130 Register (Offset = 82h) [Reset = 70h]

R130 is shown in Table 3-131.

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Table 3-131. R130 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6	IN2_LOS_EVT	R/W	1h	IN2 Loss-of-Signal Event. Indicates whther or not IN2_LOS has been asserted since this field was last cleared. 0h = No LOS Event 1h = LOS Event Detected
5	IN1_LOS_EVT	R/W	1h	IN1 Loss-of-Signal Event. Indicates whther or not IN1_LOS has been asserted since this field was last cleared. 0h = No LOS Event 1h = LOS Event Detected
4	IN0_LOS_EVT	R/W	1h	IN0 Loss-of-Signal Event. Indicates whther or not IN0_LOS has been asserted since this field was last cleared. 0h = No LOS Event 1h = LOS Event Detected
3	RESERVED	R	0h	Reserved
2	RESERVED	R	0h	Reserved
1	OUT7N_AMP_ERR_EVT_INTR_EN	R/W	0h	OUT7N Amplitude Error Event Interrupt Enable. Determines whether or not assertions of OUT7N_AMP_ERR_EVT should contribute to the device interrupt signal.
0	OUT7P_AMP_ERR_EVT_INTR_EN	R/W	0h	OUT7P Amplitude Error Event Interrupt Enable. Determines whether or not assertions of OUT7P_AMP_ERR_EVT should contribute to the device interrupt signal.

3.130 R131 Register (Offset = 83h) [Reset = 00h]

R131 is shown in Table 3-132.

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Table 3-132. R131 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	IN1_LOS_CNTR	R	0h	IN1 Loss-of-Signal Counter Readback. Reading this field returns the current value of the IN1 Loss-of-Signal Counter, which represents the number of times that IN1_LOS has been asserted since IN1_LOS_LMT_EVT was cleared. After the device power-up sequence finishes (output clocks are ready to be driven out), this counter starts from 0, and is incremented by 1 each time IN1_LOS is asserted. The counter is cleared if the device is reset via the PWRGD_PWRDN# GPIO function, and when the IN1_LOS_LMT_EVT field is written with a 1.
3-0	IN0_LOS_CNTR	R	0h	IN0 Loss-of-Signal Counter Readback. Reading this field returns the current value of the IN0 Loss-of-Signal Counter, which represents the number of times that IN0_LOS has been asserted since IN0_LOS_LMT_EVT was cleared. After the device power-up sequence finishes (output clocks are ready to be driven out), this counter starts from 0, and is incremented by 1 each time IN0_LOS is asserted. The counter is cleared if the device is reset via the PWRGD_PWRDN# GPIO function, and when the IN0_LOS_LMT_EVT field is written with a 1.

3.131 R132 Register (Offset = 84h) [Reset = 20h]

R132 is shown in Table 3-133.

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Table 3-133. R132 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	LOS_LMT	R/W	2h	Loss-of-Signal Limit. The maximum allowable INx Loss-of-Signal events that can occur before the corresponding INx_LOS_LMT_EVT field is set.
3-0	IN2_LOS_CNTR	R	0h	IN2 Loss-of-Signal Counter Readback. Reading this field returns the current value of the IN2 Loss-of-Signal Counter, which represents the number of times that IN2_LOS has been asserted since IN2_LOS_LMT_EVT was cleared. After the device power-up sequence finishes (output clocks are ready to be driven out), this counter starts from 0, and is incremented by 1 each time IN2_LOS is asserted. The counter is cleared if the device is reset via the PWRGD_PWRDN# GPIO function, and when the IN2_LOS_LMT_EVT field is written with a 1.

3.132 R133 Register (Offset = 85h) [Reset = 00h]

R133 is shown in Table 3-134.

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Table 3-134. R133 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	OUT0N_FREQ_GOOD	R	0h	OUT0N Frequency Detector Good. Live status bit that indicates whether or not the output clock frequency is below the threshold specified with OUT0_FREQ_DET_THRESH.
6	OUT0P_FREQ_GOOD	R	0h	OUT0P Frequency Detector Good. Live status bit that indicates whether or not the output clock frequency is below the threshold specified with OUT0_FREQ_DET_THRESH.
5	CRC_ERROR_EVT	R/W	0h	OTP CRC Event. Set to 1 when CRC_ERROR transitions from 0 (CRC OK or CRC Check In Progress) to 1 (CRC Error).
4	CRC_ERROR	R	0h	CRC Check Status 0 ==> Normal ; 1==> CRC Error (data corruption)
3	CRC_DONE	R	0h	CRC status. 1 == > CRC computation is done
2	IN2_LOS_LMT_EVT	R/W	0h	IN2 Loss-of-Signal Limit Event. Indicates whether or not the number of IN2 Loss-of-Signal events has exceeded the value of LOS_LMT, since the last time this field was cleared. Write a '1' to this field to clear the IN2 LOS LMT EVENT counter. 0h = LOS_LMT Not Exceeded 1h = LOS_LMT Exceeded
1	IN1_LOS_LMT_EVT	R/W	0h	IN1 Loss-of-Signal Limit Event. Indicates whether or not the number of IN1 Loss-of-Signal events has exceeded the value of LOS_LMT, since the last time this field was cleared. Write a '1' to this field to clear the IN1 LOS LMT EVENT counter. 0h = LOS_LMT Not Exceeded 1h = LOS_LMT Exceeded
0	IN0_LOS_LMT_EVT	R/W	0h	IN0 Loss-of-Signal Limit Event. Indicates whether or not the number of IN0 Loss-of-Signal events has exceeded the value of LOS_LMT, since the last time this field was cleared. Write a '1' to this field to clear the IN0 LOS LMT EVENT counter. 0h = LOS_LMT Not Exceeded 1h = LOS_LMT Exceeded

3.133 R134 Register (Offset = 86h) [Reset = 00h]

R134 is shown in Table 3-135.

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Table 3-135. R134 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	OUT4N_FREQ_GOOD	R	0h	OUT4N Frequency Detector Good. Live status bit that indicates whether or not the output clock frequency is below the threshold specified with OUT4_FREQ_DET_THRESH.
6	OUT4P_FREQ_GOOD	R	0h	OUT4P Frequency Detector Good. Live status bit that indicates whether or not the output clock frequency is below the threshold specified with OUT4_FREQ_DET_THRESH.
5	OUT3N_FREQ_GOOD	R	0h	OUT3N Frequency Detector Good. Live status bit that indicates whether or not the output clock frequency is below the threshold specified with OUT3_FREQ_DET_THRESH.
4	OUT3P_FREQ_GOOD	R	0h	OUT3P Frequency Detector Good. Live status bit that indicates whether or not the output clock frequency is below the threshold specified with OUT3_FREQ_DET_THRESH.
3	OUT2N_FREQ_GOOD	R	0h	OUT2N Frequency Detector Good. Live status bit that indicates whether or not the output clock frequency is below the threshold specified with OUT2_FREQ_DET_THRESH.
2	OUT2P_FREQ_GOOD	R	0h	OUT2P Frequency Detector Good. Live status bit that indicates whether or not the output clock frequency is below the threshold specified with OUT2_FREQ_DET_THRESH.
1	OUT1N_FREQ_GOOD	R	0h	OUT1N Frequency Detector Good. Live status bit that indicates whether or not the output clock frequency is below the threshold specified with OUT1_FREQ_DET_THRESH.
0	OUT1P_FREQ_GOOD	R	0h	OUT1P Frequency Detector Good. Live status bit that indicates whether or not the output clock frequency is below the threshold specified with OUT1_FREQ_DET_THRESH.

3.134 R135 Register (Offset = 87h) [Reset = 00h]

R135 is shown in Table 3-136.

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Table 3-136. R135 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	Reserved
5	OUT7N_FREQ_GOOD	R	0h	OUT7N Frequency Detector Good. Live status bit that indicates whether or not the output clock frequency is below the threshold specified with OUT7_FREQ_DET_THRESH.
4	OUT7P_FREQ_GOOD	R	0h	OUT7P Frequency Detector Good. Live status bit that indicates whether or not the output clock frequency is below the threshold specified with OUT7_FREQ_DET_THRESH.
3	OUT6N_FREQ_GOOD	R	0h	OUT6N Frequency Detector Good. Live status bit that indicates whether or not the output clock frequency is below the threshold specified with OUT6_FREQ_DET_THRESH.
2	OUT6P_FREQ_GOOD	R	0h	OUT6P Frequency Detector Good. Live status bit that indicates whether or not the output clock frequency is below the threshold specified with OUT6_FREQ_DET_THRESH.
1	OUT5N_FREQ_GOOD	R	0h	OUT5N Frequency Detector Good. Live status bit that indicates whether or not the output clock frequency is below the threshold specified with OUT5_FREQ_DET_THRESH.
0	OUT5P_FREQ_GOOD	R	0h	OUT5P Frequency Detector Good. Live status bit that indicates whether or not the output clock frequency is below the threshold specified with OUT5_FREQ_DET_THRESH.

3.135 R136 Register (Offset = 88h) [Reset = 00h]

R136 is shown in Table 3-137.

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Table 3-137. R136 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	OUT3N_FREQ_ERR_EVT	R/W1C	0h	OUT3N Frequency Error Event Flag. Set to 1 when OUT3N_FREQ_GOOD transitions from 1 (Good) to 0 (Error).
6	OUT3P_FREQ_ERR_EVT	R/W1C	0h	OUT3P Frequency Error Event Flag. Set to 1 when OUT3P_FREQ_GOOD transitions from 1 (Good) to 0 (Error).
5	OUT2N_FREQ_ERR_EVT	R/W1C	0h	OUT2N Frequency Error Event Flag. Set to 1 when OUT2N_FREQ_GOOD transitions from 1 (Good) to 0 (Error).
4	OUT2P_FREQ_ERR_EVT	R/W1C	0h	OUT2P Frequency Error Event Flag. Set to 1 when OUT2P_FREQ_GOOD transitions from 1 (Good) to 0 (Error).
3	OUT1N_FREQ_ERR_EVT	R/W1C	0h	OUT1N Frequency Error Event Flag. Set to 1 when OUT1N_FREQ_GOOD transitions from 1 (Good) to 0 (Error).
2	OUT1P_FREQ_ERR_EVT	R/W1C	0h	OUT1P Frequency Error Event Flag. Set to 1 when OUT1P_FREQ_GOOD transitions from 1 (Good) to 0 (Error).
1	OUT0N_FREQ_ERR_EVT	R/W1C	0h	OUT0N Frequency Error Event Flag. Set to 1 when OUT0N_FREQ_GOOD transitions from 1 (Good) to 0 (Error).
0	OUT0P_FREQ_ERR_EVT	R/W1C	0h	OUT0P Frequency Error Event Flag. Set to 1 when OUT0P_FREQ_GOOD transitions from 1 (Good) to 0 (Error).

3.136 R137 Register (Offset = 89h) [Reset = 00h]

R137 is shown in Table 3-138.

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Table 3-138. R137 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	OUT7N_FREQ_ERR_EVT	R/W1C	0h	OUT7N Frequency Error Event Flag. Set to 1 when OUT7N_FREQ_GOOD transitions from 1 (Good) to 0 (Error).
6	OUT7P_FREQ_ERR_EVT	R/W1C	0h	OUT7P Frequency Error Event Flag. Set to 1 when OUT7P_FREQ_GOOD transitions from 1 (Good) to 0 (Error).
5	OUT6N_FREQ_ERR_EVT	R/W1C	0h	OUT6N Frequency Error Event Flag. Set to 1 when OUT6N_FREQ_GOOD transitions from 1 (Good) to 0 (Error).
4	OUT6P_FREQ_ERR_EVT	R/W1C	0h	OUT6P Frequency Error Event Flag. Set to 1 when OUT6P_FREQ_GOOD transitions from 1 (Good) to 0 (Error).
3	OUT5N_FREQ_ERR_EVT	R/W1C	0h	OUT5N Frequency Error Event Flag. Set to 1 when OUT5N_FREQ_GOOD transitions from 1 (Good) to 0 (Error).
2	OUT5P_FREQ_ERR_EVT	R/W1C	0h	OUT5P Frequency Error Event Flag. Set to 1 when OUT5P_FREQ_GOOD transitions from 1 (Good) to 0 (Error).
1	OUT4N_FREQ_ERR_EVT	R/W1C	0h	OUT4N Frequency Error Event Flag. Set to 1 when OUT4N_FREQ_GOOD transitions from 1 (Good) to 0 (Error).
0	OUT4P_FREQ_ERR_EVT	R/W1C	0h	OUT4P Frequency Error Event Flag. Set to 1 when OUT4P_FREQ_GOOD transitions from 1 (Good) to 0 (Error).

3.137 R138 Register (Offset = 8Ah) [Reset = 00h]

R138 is shown in Table 3-139.

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Table 3-139. R138 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	OUT2N_AMP_GOOD	R	0h	OUT2N Amplitude Detector Good. Live status bit that indicates whether or not the output clock amplitude is below the threshold specified with OUT_AMP_DET_THRESH.
6	OUT2P_AMP_GOOD	R	0h	OUT2P Amplitude Detector Good. Live status bit that indicates whether or not the output clock amplitude is below the threshold specified with OUT_AMP_DET_THRESH.
5	OUT1N_AMP_GOOD	R	0h	OUT1N Amplitude Detector Good. Live status bit that indicates whether or not the output clock amplitude is below the threshold specified with OUT_AMP_DET_THRESH.
4	OUT1P_AMP_GOOD	R	0h	OUT1P Amplitude Detector Good. Live status bit that indicates whether or not the output clock amplitude is below the threshold specified with OUT_AMP_DET_THRESH.
3	OUT0N_AMP_GOOD	R	0h	OUT0N Amplitude Detector Good. Live status bit that indicates whether or not the output clock amplitude is below the threshold specified with OUT_AMP_DET_THRESH.
2	OUT0P_AMP_GOOD	R	0h	OUT0P Amplitude Detector Good. Live status bit that indicates whether or not the output clock amplitude is below the threshold specified with OUT_AMP_DET_THRESH.
1-0	RESERVED	R	0h	Reserved

3.138 R139 Register (Offset = 8Bh) [Reset = 00h]

R139 is shown in Table 3-140.

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Table 3-140. R139 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	OUT6N_AMP_GOOD	R	0h	OUT6N Amplitude Detector Good. Live status bit that indicates whether or not the output clock amplitude is below the threshold specified with OUT_AMP_DET_THRESH.
6	OUT6P_AMP_GOOD	R	0h	OUT6P Amplitude Detector Good. Live status bit that indicates whether or not the output clock amplitude is below the threshold specified with OUT_AMP_DET_THRESH.
5	OUT5N_AMP_GOOD	R	0h	OUT5N Amplitude Detector Good. Live status bit that indicates whether or not the output clock amplitude is below the threshold specified with OUT_AMP_DET_THRESH.
4	OUT5P_AMP_GOOD	R	0h	OUT5P Amplitude Detector Good. Live status bit that indicates whether or not the output clock amplitude is below the threshold specified with OUT_AMP_DET_THRESH.
3	OUT4N_AMP_GOOD	R	0h	OUT4N Amplitude Detector Good. Live status bit that indicates whether or not the output clock amplitude is below the threshold specified with OUT_AMP_DET_THRESH.
2	OUT4P_AMP_GOOD	R	0h	OUT4P Amplitude Detector Good. Live status bit that indicates whether or not the output clock amplitude is below the threshold specified with OUT_AMP_DET_THRESH.
1	OUT3N_AMP_GOOD	R	0h	OUT3N Amplitude Detector Good. Live status bit that indicates whether or not the output clock amplitude is below the threshold specified with OUT_AMP_DET_THRESH.
0	OUT3P_AMP_GOOD	R	0h	OUT3P Amplitude Detector Good. Live status bit that indicates whether or not the output clock amplitude is below the threshold specified with OUT_AMP_DET_THRESH.

3.139 R140 Register (Offset = 8Ch) [Reset = 00h]

R140 is shown in Table 3-141.

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Table 3-141. R140 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	OUT1N_AMP_ERR_EVT	R/W1C	0h	OUT1N Amplitude Error Event Flag. Set to 1 when OUT1N_AMP_GOOD transitions from 1 (Good) to 0 (Error).
6	OUT1P_AMP_ERR_EVT	R/W1C	0h	OUT1P Amplitude Error Event Flag. Set to 1 when OUT1P_AMP_GOOD transitions from 1 (Good) to 0 (Error).
5	OUT0N_AMP_ERR_EVT	R/W1C	0h	OUT0N Amplitude Error Event Flag. Set to 1 when OUT0N_AMP_GOOD transitions from 1 (Good) to 0 (Error).
4	OUT0P_AMP_ERR_EVT	R/W1C	0h	OUT0P Amplitude Error Event Flag. Set to 1 when OUT0P_AMP_GOOD transitions from 1 (Good) to 0 (Error).
3-2	RESERVED	R	0h	Reserved
1	OUT7N_AMP_GOOD	R	0h	OUT7N Amplitude Detector Good. Live status bit that indicates whether or not the output clock amplitude is below the threshold specified with OUT_AMP_DET_THRESH.
0	OUT7P_AMP_GOOD	R	0h	OUT7P Amplitude Detector Good. Live status bit that indicates whether or not the output clock amplitude is below the threshold specified with OUT_AMP_DET_THRESH.

3.140 R141 Register (Offset = 8Dh) [Reset = 00h]

R141 is shown in Table 3-142.

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Table 3-142. R141 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	OUT5N_AMP_ERR_EVT	R/W1C	0h	OUT5N Amplitude Error Event Flag. Set to 1 when OUT5N_AMP_GOOD transitions from 1 (Good) to 0 (Error).
6	OUT5P_AMP_ERR_EVT	R/W1C	0h	OUT5P Amplitude Error Event Flag. Set to 1 when OUT5P_AMP_GOOD transitions from 1 (Good) to 0 (Error).
5	OUT4N_AMP_ERR_EVT	R/W1C	0h	OUT4N Amplitude Error Event Flag. Set to 1 when OUT4N_AMP_GOOD transitions from 1 (Good) to 0 (Error).
4	OUT4P_AMP_ERR_EVT	R/W1C	0h	OUT4P Amplitude Error Event Flag. Set to 1 when OUT4P_AMP_GOOD transitions from 1 (Good) to 0 (Error).
3	OUT3N_AMP_ERR_EVT	R/W1C	0h	OUT3N Amplitude Error Event Flag. Set to 1 when OUT3N_AMP_GOOD transitions from 1 (Good) to 0 (Error).
2	OUT3P_AMP_ERR_EVT	R/W1C	0h	OUT3P Amplitude Error Event Flag. Set to 1 when OUT3P_AMP_GOOD transitions from 1 (Good) to 0 (Error).
1	OUT2N_AMP_ERR_EVT	R/W1C	0h	OUT2N Amplitude Error Event Flag. Set to 1 when OUT2N_AMP_GOOD transitions from 1 (Good) to 0 (Error).
0	OUT2P_AMP_ERR_EVT	R/W1C	0h	OUT2P Amplitude Error Event Flag. Set to 1 when OUT2P_AMP_GOOD transitions from 1 (Good) to 0 (Error).

3.141 R142 Register (Offset = 8Eh) [Reset = 00h]

R142 is shown in Table 3-143.

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Table 3-143. R142 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	Reserved
3	OUT7N_AMP_ERR_EVT	R/W1C	0h	OUT7N Amplitude Error Event Flag. Set to 1 when OUT7N_AMP_GOOD transitions from 1 (Good) to 0 (Error).
2	OUT7P_AMP_ERR_EVT	R/W1C	0h	OUT7P Amplitude Error Event Flag. Set to 1 when OUT7P_AMP_GOOD transitions from 1 (Good) to 0 (Error).
1	OUT6N_AMP_ERR_EVT	R/W1C	0h	OUT6N Amplitude Error Event Flag. Set to 1 when OUT6N_AMP_GOOD transitions from 1 (Good) to 0 (Error).
0	OUT6P_AMP_ERR_EVT	R/W1C	0h	OUT6P Amplitude Error Event Flag. Set to 1 when OUT6P_AMP_GOOD transitions from 1 (Good) to 0 (Error).

3.142 R143 Register (Offset = 8Fh) [Reset = 02h]

R143 is shown in Table 3-144.

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Table 3-144. R143 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	Reserved
3-0	PROD_REV_ID	R	2h	4 product ID/revision ID

3.143 R144 Register (Offset = 90h) [Reset = 18h]

R144 is shown in Table 3-145.

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Table 3-145. R144 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	OTP_ID	R	18h	OTP ID. Loaded from the OTP, this field is used to identify the device's OTP configuration.

3.144 R147 Register (Offset = 93h) [Reset = 5Bh]

R147 is shown in Table 3-146.

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Table 3-146. R147 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	UNLOCK_PROTECTED_REG	R/W	5Bh	Internal register unlock, write "0x5B" to unlock the write operation for protected registers.

3.145 R148 Register (Offset = 94h) [Reset = 00h]

R148 is shown in Table 3-147.

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Table 3-147. R148 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	VDDR_SUP_LVL_DET_RB	R	0h	VDDR Supply Level Detector Readback. Reading this field returns a 2-bit code corresponding to the detected supply level for VDDR. 0h = 3.3 V 1h = 1.8 V 2h = 2.5 V 3h = <1.8 V
5-4	VDDX_SUP_LVL_DET_RB	R	0h	VDDX Supply Level Detector Readback. Reading this field returns a 2-bit code corresponding to the detected supply level for VDDX. 0h = 3.3 V 1h = 1.8 V 2h = 2.5 V 3h = <1.8 V
3-2	VDDD_SUP_LVL_DET_RB	R	0h	VDDD Supply Level Detector Readback. Reading this field returns a 2-bit code corresponding to the detected supply level for VDDD. 0h = 3.3 V 1h = 1.8 V 2h = 2.5 V 3h = <1.8 V
1-0	VDDA_SUP_LVL_DET_RB	R	0h	VDDA Supply Level Detector Readback. Reading this field returns a 2-bit code corresponding to the detected supply level for VDDA. 0h = 3.3 V 1h = 1.8 V 2h = 2.5 V 3h = <1.8 V

3.146 R149 Register (Offset = 95h) [Reset = 00h]

R149 is shown in Table 3-148.

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Table 3-148. R149 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	VDDO_5_SUP_LVL_DET_RB	R	0h	VDDO_5 Supply Level Detector Readback. Reading this field returns a 2-bit code corresponding to the detected supply level for VDDO_5. 0h = 3.3 V 1h = 1.8 V 2h = 2.5 V 3h = <1.8 V
5-4	VDDO_3_4_SUP_LVL_DET_RB	R	0h	VDDO_3_4 Supply Level Detector Readback. Reading this field returns a 2-bit code corresponding to the detected supply level for VDDO_3_4. 0h = 3.3 V 1h = 1.8 V 2h = 2.5 V 3h = <1.8 V
3-2	VDDO_1_2_SUP_LVL_DET_RB	R	0h	VDDO_1_2 Supply Level Detector Readback. Reading this field returns a 2-bit code corresponding to the detected supply level for VDDO_1_2. 0h = 3.3 V 1h = 1.8 V 2h = 2.5 V 3h = <1.8 V
1-0	VDDO_0_SUP_LVL_DET_RB	R	0h	VDDO_0 Supply Level Detector Readback. Reading this field returns a 2-bit code corresponding to the detected supply level for VDDO_0. 0h = 3.3 V 1h = 1.8 V 2h = 2.5 V 3h = <1.8 V

3.147 R150 Register (Offset = 96h) [Reset = 00h]

R150 is shown in Table 3-149.

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Table 3-149. R150 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	Reserved
3-2	VDDO_7_SUP_LVL_DET_RB	R	0h	VDDO_7 Supply Level Detector Readback. Reading this field returns a 2-bit code corresponding to the detected supply level for VDDO_7. 0h = 3.3 V 1h = 1.8 V 2h = 2.5 V 3h = <1.8 V
1-0	VDDO_6_SUP_LVL_DET_RB	R	0h	VDDO_6 Supply Level Detector Readback. Reading this field returns a 2-bit code corresponding to the detected supply level for VDDO_6. 0h = 3.3 V 1h = 1.8 V 2h = 2.5 V 3h = <1.8 V

3.148 R153 Register (Offset = 99h) [Reset = 20h]

R153 is shown in Table 3-150.

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Table 3-150. R153 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	Reserved
5-0	OTP_PAGE0_SEL_CODE	R/W	20h	OTP Page 0 Selection Code. Pages are selected with three 3-level values, PAGE_SEL_2, PAGE_SEL_1, and PAGE_SEL_0. Each of these three values is encoded as a 2-bit value, such that the full OTP page selection code is a 6-bit value. Each 2-bit subset of the OTP page selection code is encoded such that "00" = LOW, "01" = MID, "11" = HIGH, and "10" = DON'T CARE. This field's value should be programmed in the OTP with the 6-bit selection code that will be used to select Page 0 of the OTP.

3.149 R154 Register (Offset = 9Ah) [Reset = 23h]

R154 is shown in Table 3-151.

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Table 3-151. R154 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	Reserved
5-0	OTP_PAGE1_SEL_CODE	R/W	23h	OTP Page 1 Selection Code. Pages are selected with three 3-level values, PAGE_SEL_2, PAGE_SEL_1, and PAGE_SEL_0. Each of these three values is encoded as a 2-bit value, such that the full OTP page selection code is a 6-bit value. Each 2-bit subset of the OTP page selection code is encoded such that "00" = LOW, "01" = MID, "11" = HIGH, and "10" = DON'T CARE. This field's value should be programmed in the OTP with the 6-bit selection code that will be used to select Page 1 of the OTP.

3.150 R155 Register (Offset = 9Bh) [Reset = 2Ch]

R155 is shown in Table 3-152.

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Table 3-152. R155 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	Reserved
5-0	OTP_PAGE2_SEL_CODE	R/W	2Ch	OTP Page 2 Selection Code. Pages are selected with three 3-level values, PAGE_SEL_2, PAGE_SEL_1, and PAGE_SEL_0. Each of these three values is encoded as a 2-bit value, such that the full OTP page selection code is a 6-bit value. Each 2-bit subset of the OTP page selection code is encoded such that "00" = LOW, "01" = MID, "11" = HIGH, and "10" = DON'T CARE. This field's value should be programmed in the OTP with the 6-bit selection code that will be used to select Page 2 of the OTP.

3.151 R156 Register (Offset = 9Ch) [Reset = 2Fh]

R156 is shown in Table 3-153.

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Table 3-153. R156 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	Reserved
5-0	OTP_PAGE3_SEL_CODE	R/W	2Fh	OTP Page 3 Selection Code. Pages are selected with three 3-level values, PAGE_SEL_2, PAGE_SEL_1, and PAGE_SEL_0. Each of these three values is encoded as a 2-bit value, such that the full OTP page selection code is a 6-bit value. Each 2-bit subset of the OTP page selection code is encoded such that "00" = LOW, "01" = MID, "11" = HIGH, and "10" = DON'T CARE. This field's value should be programmed in the OTP with the 6-bit selection code that will be used to select Page 3 of the OTP.

3.152 R157 Register (Offset = 9Dh) [Reset = 00h]

R157 is shown in Table 3-154.

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Table 3-154. R157 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	OTP_PAGE_RB	R	0h	OTP Page Readback. Reading this field returns the current OTP Page, which ranges from 0 to 3. This is the page number that is mapped to the current OTP Page Selection Code.
5-0	OTP_PAGE_SEL_CODE_RB	R	0h	OTP Page Selection Code Readback. Reading this field returns the current OTP Page Selection Code, based on the OTP_PAGE_SEL_PU_x register fields, the sampled values of GPIO[2:0] at power-up, and any dynamic OTP page selection pin events.

3.153 R187 Register (Offset = BBh) [Reset = 00h]

R187 is shown in Table 3-155.

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Table 3-155. R187 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CRC_COMPUTED	R/W	0h	Computed CRC, calculated at startup. The computed CRC includes the stored CRC in the calculation. If the stored CRC is correct, then the computed CRC will be 0 and CRC_ERROR will be 0. Otherwise, the computed CRC will be non-zero and CRC_ERROR will be 1.

3.154 R188 Register (Offset = BCh) [Reset = 02h]

R188 is shown in Table 3-156.

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Table 3-156. R188 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6	RESERVED	R	0h	Reserved
5	RESERVED	R	0h	Reserved
4	RESERVED	R	0h	Reserved
3	RESERVED	R	0h	Reserved
2	RESERVED	R	0h	Reserved
1	BOOTOSC_CLK_DIS	R/W	1h	Forcibly select Boot oscillator clock as system clock
0	RESERVED	R	0h	Reserved

3.155 R253 Register (Offset = FDh) [Reset = 00h]

R253 is shown in Table 3-157.

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Table 3-157. R253 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	0h	Reserved
1-0	PAGE_SEL_0	R/W	0h	Register Page Select. Writing this field changes the register page that is accessble via I2C. Each collection of 256 registers forms a register page. Corresponding PAGE_SEL fields exist in the same location on each register page. In other words, PAGE_SEL_0 in R253[0], PAGE_SEL_1 in R509[0], PAGE_SEL_2 in R765[0], and PAGE_SEL_3 in R1021[0]. All PAGE_SEL_x fields share the same behavior.

3.156 R319 Register (Offset = 13Fh) [Reset = 01h]

R319 is shown in Table 3-158.

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Table 3-158. R319 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0h	Reserved
0	CLK_READY	R/W	1h	FOD Clocks Ready. This is set to 1 to indicate that the FODs are currently ready to be used as a clock source.

3.157 R576 Register (Offset = 240h) [Reset = 00h]

R576 is shown in Table 3-159.

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Table 3-159. R576 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0h	Reserved
0	OUT0_DIS	R/W	0h	OUT0 Disable. When set to 0, all other contributors are considered to determine if OUT0 should be enabled. When set to 1, OUT0 is disabled.

3.158 R580 Register (Offset = 244h) [Reset = 00h]

R580 is shown in Table 3-160.

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Table 3-160. R580 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0h	Reserved
0	OUT1_DIS	R/W	0h	OUT1 Disable. When set to 0, all other contributors are considered to determine if OUT1 should be enabled. When set to 1, OUT1 is disabled.

3.159 R584 Register (Offset = 248h) [Reset = 00h]

R584 is shown in Table 3-161.

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Table 3-161. R584 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0h	Reserved
0	OUT2_DIS	R/W	0h	OUT2 Disable. When set to 0, all other contributors are considered to determine if OUT2 should be enabled. When set to 1, OUT2 is disabled.

3.160 R588 Register (Offset = 24Ch) [Reset = 00h]

R588 is shown in Table 3-162.

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Table 3-162. R588 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0h	Reserved
0	OUT3_DIS	R/W	0h	OUT3 Disable. When set to 0, all other contributors are considered to determine if OUT3 should be enabled. When set to 1, OUT3 is disabled.

3.161 R592 Register (Offset = 250h) [Reset = 00h]

R592 is shown in Table 3-163.

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Table 3-163. R592 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0h	Reserved
0	OUT4_DIS	R/W	0h	MSB's of count for code 0

3.162 R596 Register (Offset = 254h) [Reset = 00h]

R596 is shown in Table 3-164.

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Table 3-164. R596 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0h	Reserved
0	OUT5_DIS	R/W	0h	OUT5 Disable. When set to 0, all other contributors are considered to determine if OUT5 should be enabled. When set to 1, OUT5 is disabled.

3.163 R600 Register (Offset = 258h) [Reset = 00h]

R600 is shown in Table 3-165.

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Table 3-165. R600 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0h	Reserved
0	OUT6_DIS	R/W	0h	OUT6 Disable. When set to 0, all other contributors are considered to determine if OUT6 should be enabled. When set to 1, OUT6 is disabled.

3.164 R604 Register (Offset = 25Ch) [Reset = 00h]

R604 is shown in Table 3-166.

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Table 3-166. R604 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0h	Reserved
0	OUT7_DIS	R/W	0h	OUT7 Disable. When set to 0, all other contributors are considered to determine if OUT7 should be enabled. When set to 1, OUT7 is disabled.

3.165 R624 Register (Offset = 270h) [Reset = 00h]

R624 is shown in Table 3-167.

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Table 3-167. R624 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6	RESERVED	R	0h	Reserved
5	RESERVED	R	0h	Reserved
4	RESERVED	R	0h	Reserved
3	RESERVED	R	0h	Reserved
2	RESERVED	R	0h	Reserved
1	PATH1_FOD_SEL	R/W	0h	FOD PATH1 Post-divider FOD Select. Selects the clock that is used as the input to the FOD PATH1 Post-divider. This field is locked, and requires unlocking UNLOCK_PROTECTED_REG before using. 0h = FOD0 1h = FOD1
0	RESERVED	R	0h	Reserved

3.166 R745 Register (Offset = 2E9h) [Reset = 00h]

R745 is shown in Table 3-168.

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Table 3-168. R745 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	OUT2P_INV_POL	R/W	0h	OUT2P Polarity Inversion.
6	OUT1P_INV_POL	R/W	0h	OUT1P Polarity Inversion.
5	OUT0P_INV_POL	R/W	0h	OUT0P Polarity Inversion.
4-0	RESERVED	R	0h	Reserved

3.167 R746 Register (Offset = 2EAh) [Reset = 00h]

R746 is shown in Table 3-169.

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Table 3-169. R746 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	OUT2N_INV_POL	R/W	0h	OUT2N Polarity Inversion.
6	OUT1N_INV_POL	R/W	0h	OUT1N Polarity Inversion.
5	OUT0N_INV_POL	R/W	0h	OUT0N Polarity Inversion.
4	OUT7P_INV_POL	R/W	0h	OUT7P Polarity Inversion.
3	OUT6P_INV_POL	R/W	0h	OUT6P Polarity Inversion.
2	OUT5P_INV_POL	R/W	0h	OUT5P Polarity Inversion.
1	OUT4P_INV_POL	R/W	0h	OUT4P Polarity Inversion.
0	OUT3P_INV_POL	R/W	0h	OUT3P Polarity Inversion.

3.168 R747 Register (Offset = 2EBh) [Reset = 00h]

R747 is shown in Table 3-170.

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Table 3-170. R747 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0h	Reserved
4	OUT7N_INV_POL	R/W	0h	OUT7N Polarity Inversion.
3	OUT6N_INV_POL	R/W	0h	OUT6N Polarity Inversion.
2	OUT5N_INV_POL	R/W	0h	OUT5N Polarity Inversion.
1	OUT4N_INV_POL	R/W	0h	OUT4N Polarity Inversion.
0	OUT3N_INV_POL	R/W	0h	OUT3N Polarity Inversion.

3.169 R762 Register (Offset = 2FAh) [Reset = 00h]

R762 is shown in Table 3-171.

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Table 3-171. R762 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DIE_ID_1[7:0]	R	0h	X-coor [7:0], LOT ID[23:16]

3.170 R763 Register (Offset = 2FBh) [Reset = 00h]

R763 is shown in Table 3-172.

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Table 3-172. R763 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6-0	DIE_ID_1[14:8]	R	0h	X-coor [7:0], LOT ID[23:16]

3.171 R764 Register (Offset = 2FCh) [Reset = 00h]

R764 is shown in Table 3-173.

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Table 3-173. R764 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DIE_ID_2[7:0]	R	0h	LOT ID[15:0]

3.172 R766 Register (Offset = 2FEh) [Reset = 00h]

R766 is shown in Table 3-174.

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Table 3-174. R766 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DIE_ID_2[15:8]	R	0h	LOT ID[15:0]

3.173 R767 Register (Offset = 2FFh) [Reset = 00h]

R767 is shown in Table 3-175.

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Table 3-175. R767 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DIE_ID_3[7:0]	R	0h	Spare third word for DIE_ID

3.174 R768 Register (Offset = 300h) [Reset = 00h]

R768 is shown in Table 3-176.

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Table 3-176. R768 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DIE_ID_3[15:8]	R	0h	Spare third word for DIE_ID

3.175 R770 Register (Offset = 302h) [Reset = 00h]

R770 is shown in Table 3-177.

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Table 3-177. R770 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	STORED_CRC	R/W	0h	Stored CRC

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
December 2025	*	Initial Release

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