User's Guide
SNVU155A–June 2012–Revised April 2013

AN-2264 LMR70503 Demo Board

1 Introduction

The LMR70503 is an inverting buck-boost converter with adjustable negative output voltage in a tiny 8-bump DSBGA package (0.84 mm × 1.615 mm × 0.6 mm). Its unique control method is designed to provide fast transient response, low output noise, high efficiency, and tight regulation in the smallest possible PCB area. The LMR70503 has built in soft start, peak current limit, minimum switching frequency limit, and Under Voltage Lock Out (UVLO), with no external compensation required. For ease of use, the EN pin is referred to the IC ground instead of the negative output voltage. The LMR70503 is operating in Discontinuous Conduction Mode (DCM) in light load. The minimum switching frequency is limited to 500 kHz to avoid audio frequency interference to other systems. Very small total solution size can be achieved with the tiny footprint of the LMR70503 and the low external component count.

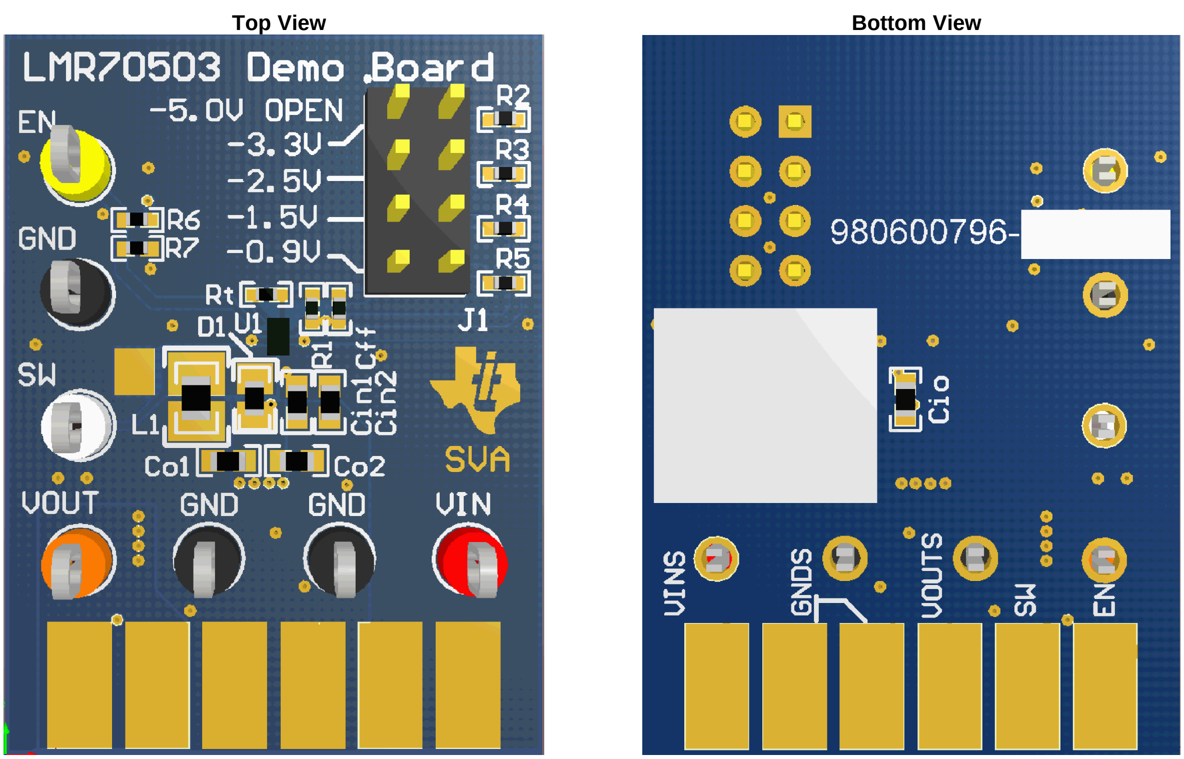

Figure 1. LMR70503 Demo Board

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2 LMR70503 Demo Board Schematic

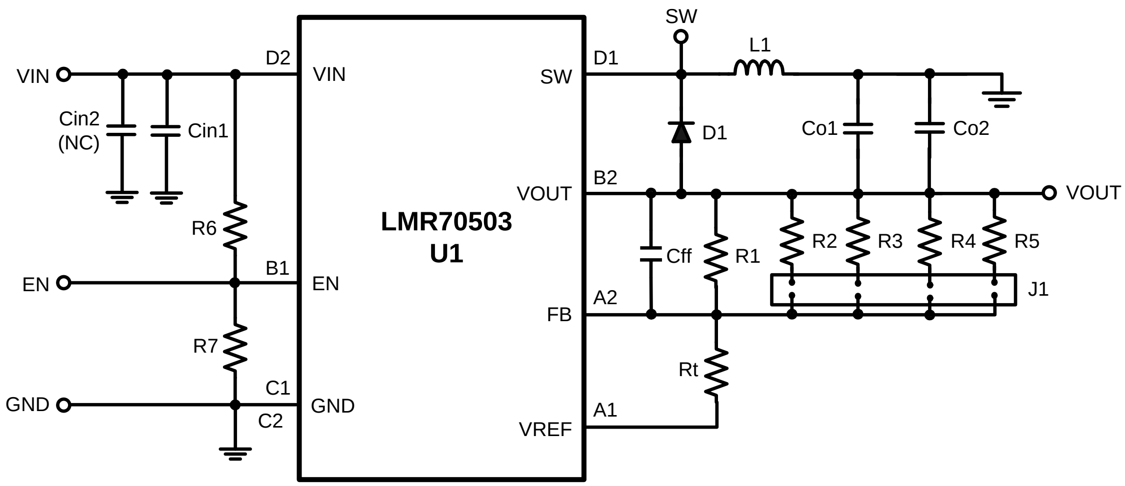


Figure 2. LMR70503 Demo Board Schematic

3 LMR70503 Features

- Tiny 8-Bump DSBGA Package: 0.84 mm × 1.615 mm × 0.6 mm
- 2.8 V to 5.5 V Input Voltage Range
- Adjustable Output Voltage: -0.9 V to -5.5 V
- 320 mA Switch Current Limit
- 500 kHz Minimum Switching Frequency
- Ground Referred Enable Input
- Under Voltage Lock Out (UVLO)
- No External Compensation
- Internal Soft Start
- 1 µA Shutdown Supply Current
- WEBENCH® Enabled

4 Selecting the Output Voltage

One of five output voltages can be selected by J1. The default setting is J1 open and the output voltage is -5.0 V, set by resistor divider R1 and R_t:

$$V_{OUT} = - V_{REF} * R1 / R_t \quad (1)$$

When one of the four positions of J1 is connected, the resistor connected between this position and V_{OUT} is paralleled with R1 to provide a lower magnitude output voltage. Output voltages of -3.3 V, -2.5 V, -1.5 V and -0.9 V can be selected by J1, as shown in Figure 1 and Figure 2.

Output voltage other than these five preset values can be achieved by replacing R1 and keep J1 open:

$$R1 = R_t * |V_{OUT}| / V_{REF} \quad (2)$$

where V_{REF} is typically 1.19 Vand R_t is 100 kΩ. R_t can be selected between 20 kΩ and 100 kΩ.

5 Operation Description

The LMR70503 controller incorporates a unique peak current mode control method with a minimum switching frequency limit. With fixed peak current limit, the switching frequency decreases with decreased load current. At light load, the switching frequency will decrease to the audible frequency range, which is not acceptable in many applications. The LMR70503 is designed to operate with peak current mode control and limit the switching frequency to 500 kHz (typical) minimum, to avoid audible frequency interference. At light load, when the switching frequency drops to the minimum, the inductor current limit is reduced instead of frequency to maintain regulation. The LMR70503 also incorporates an internal dummy load to maintain output regulation in the minimum ON-time (T_{ON-MIN}) condition. The maximum load the LMR70503 can provide is limited by the maximum peak inductor current and the minimum off time (T_{OFF_MIN}) of the high side switch. The maximum load varies with input voltage, output voltage and the inductor value. For more details on the LMR70503 operation, see *LMR70503 SIMPLE SWITCHER Buck-Boost Converter For Negative Output Voltage in DSBGA* (SNVS850).

6 Enable and Disable

The LMR70503 features an enable (EN) pin and associated comparator to allow the user to easily sequence the LMR70503 from an external voltage rail, or to manually set the input UVLO threshold. Enable threshold levels are referred to the LMR70503 ground, instead of the lowest potential: the negative output voltage. It is important to ensure that a valid input voltage (2.8 V ≤ V_{IN}≤ 5.5 V) is present on the VIN pin before the EN input is asserted. Also, the voltage on the EN pin must always be less than V_{IN}. This applies to both static and dynamic operation, and during start up and shut down sequences. The demo board includes a resistor divider (R6 and R7) to pull EN pin up to half of V_{IN}. The LMR70503 will be enabled when V_{IN} is higher than the UVLO level (typically 2.55 V with 0.13 V hysteresis band). Use the EN post to control the EN pin externally.

7 Inductor and Diode

The inductor and diode selected on the demo board are optimized for very small total solution size. Larger size inductor and diode can improve overall efficiency if size constraints allow. Bigger footprints are provided for customer convenience.

8 Soft Start and Soft Off

The soft start action is inherent with the maximum peak current limit and the minimum off time. During start up, the inductor current rises to the maximum peak current limit, then the high-side switch is turned off for $T_{OFF-MIN}$ to let the inductor current charge the output capacitor(s). Then the high-side turns on to repeat the cycle. After the output voltage is charged to the regulation level, the LMR70503 will operate in steady state. The soft start time will be longer with more output capacitance, lower supply voltage V_{IN}, and more loading during start up. When shutdown, the LMR70503 incorporates an output voltage discharge feature to bring the output voltage to zero volts, regardless of the load current.

9 Quick Setup Procedures

Step 1: Connect a power supply to VIN terminals

Step 2: Connect a load to VOUT terminals

Step 3: EN terminal can be left floating for normal operation. It can be connected to external signal for sequencing.

Step 4: Set V_{IN} = 5V, with 0A load applied, check V_{OUT} with a voltmeter. Nominal -5 V

Step 5: Apply a 50mA load and check V_{OUT}. Nominal -5 V

10 Edge Connector

Figure 3 shows net names of the edge connector pins. The top side of the edge connector is connected to the power traces of the LMR70503 demo board. The bottom side are signal pins. The VINS, VOUTS and GNDS pins are sensing pins for V_{IN}, V_{OUT} and ground respectively. The sensing pins are connected to the power nets via net ties close to the IC. They are designed for more accurate efficiency measurement when edge connector is used. Additional voltage drops on the edge connector are bypassed if efficiency is measured by:

$$I_{OUT} \times (VOUTS - GNDS) / (I_{IN} \times (VINS - GNDS)) \quad (3)$$

Figure 3. Edge Connector

11 LMR70503 Bill of Materials

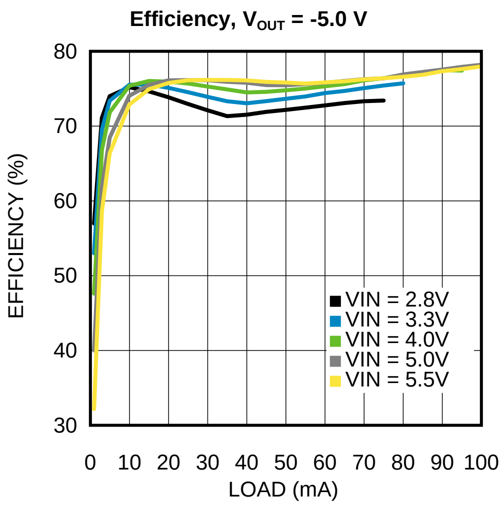
V_{IN} = 2.8 V to 5.5 V, V_{OUT} has options of -0.9 V, -1.5 V, -2.5 V, -3.3 V, and -5.0 V. Optimized for minimum solution size.

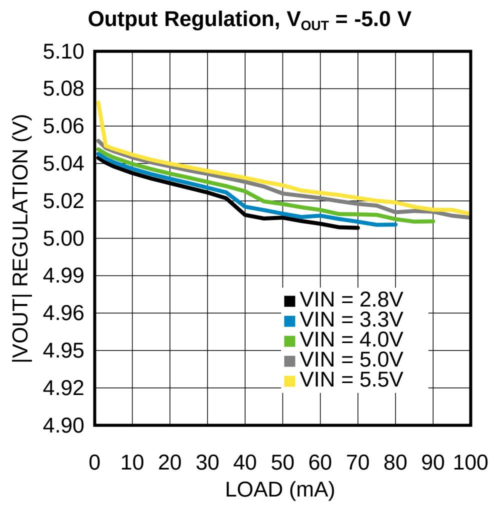
Table 1. Bill of Materials

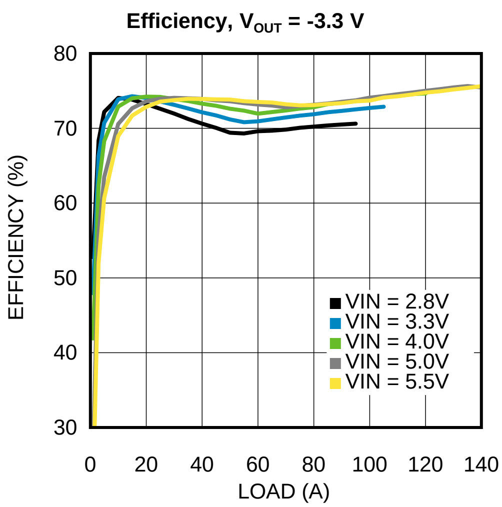
Designator	Value	Case Size	Manufacturer	Manufacturer P/N
U1	Inverting Buck-Boost	8-bump DSBGA	Texas Instruments	LMR70503
C_{IN1}	10 µF 10 V X5R	0603	TDK	C1608X5R1A106M
C_{O1}, C_{O2}	22 µF 6.3 V X5R	0603	TDK	C1608X5R0J226M
C_{ff}	10PF 50V 5% NP0	0402	Murata	GRM1555C1H100JZ01D
D	Schottky 30 V 500 mA	SOD882	NXP Semi	PMEG3005EL
L	6.8 µH, 0.76 A 362 mΩ	2.0*2.0*1.2mm	TDK	VLS2012ET-6R8M
R_t	100 kΩ, 1%, 0.063W	0402	Vishay Dale	CRCW0402100KFKED
R1, R3	422 kΩ, 1%, 0.063W	0402	Vishay Dale	CRCW0402422KFKED
R2	820 kΩ, 5%, 0.063W	0402	Vishay Dale	CRCW0402820KFKED
R4	180 kΩ 1/16W 1%	0402	Vishay Dale	CRCW0402180KFKED
R5	93.1 kΩ, 1%, 0.063W	0402	Vishay Dale	CRCW040293K1FKED
R6, R7	20 kΩ, 5%, 0.063W	0402	Vishay Dale	CRCW040220K0JNED

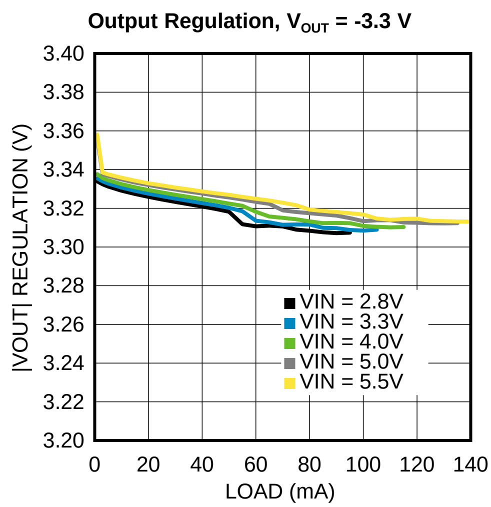
12 Typical Performance Characteristics

Unless otherwise specified, the following conditions apply: V_{IN} = 3.3 V, V_{OUT} = -5.0 V, V_{EN} = 1.8 V, C_{IN} = 10 µF, 6.3 V, X5R ceramic capacitor; C_{OUT} = 2 × 22 µF, 6.3 V, X5R ceramic capacitor; L = 6.8 µH (VLS2012ET-6R8M); $T_{AMBIENT}$ = 25 °C.

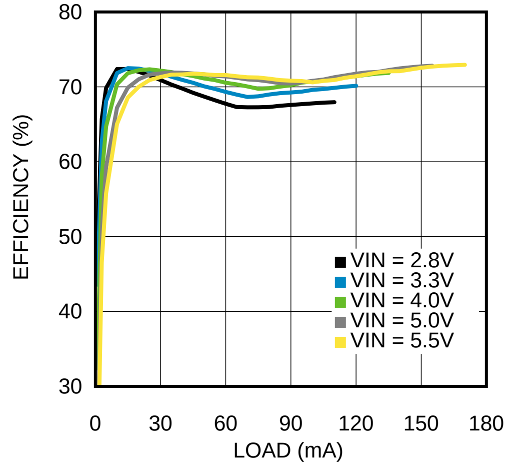




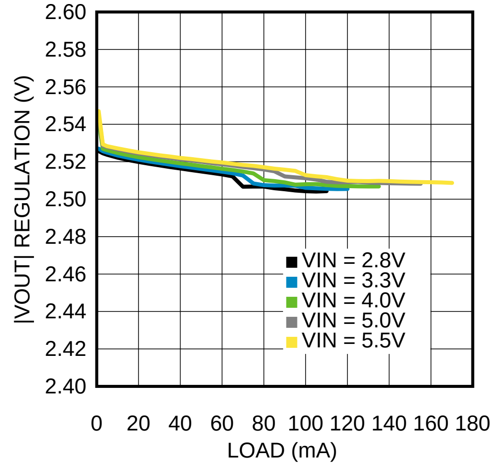




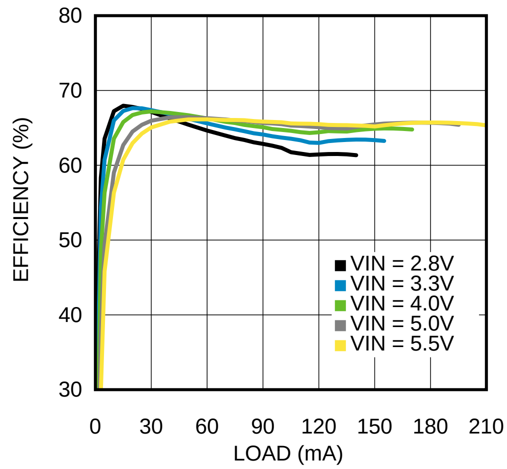
Efficiency, V_{OUT} = -2.5 V



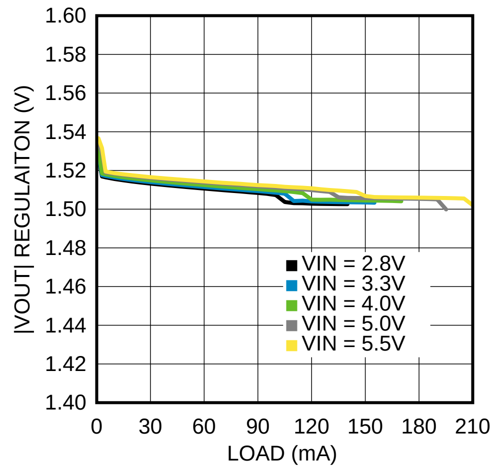
Output Regulation, V_{OUT} = -2.5 V



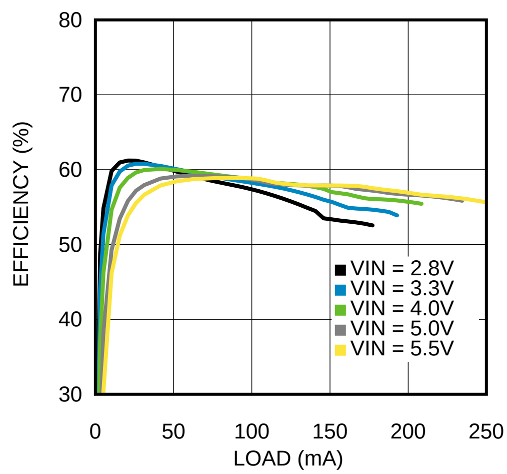
Efficiency, V_{OUT} = -1.5 V



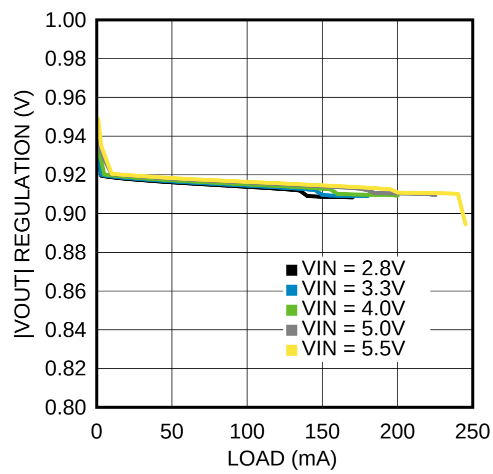
Output Regulation, V_{OUT} = -1.5 V



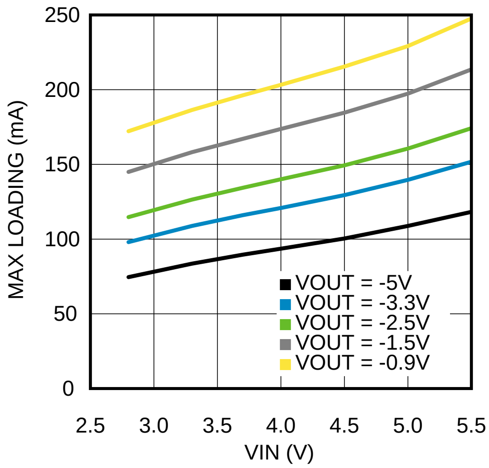
Efficiency, V_{OUT} = -0.9 V



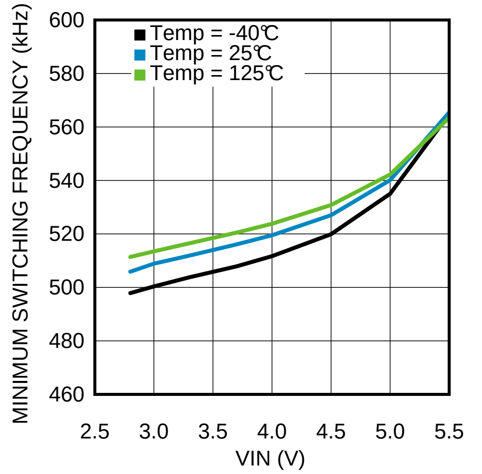
Output Regulation, V_{OUT} = -0.9 V



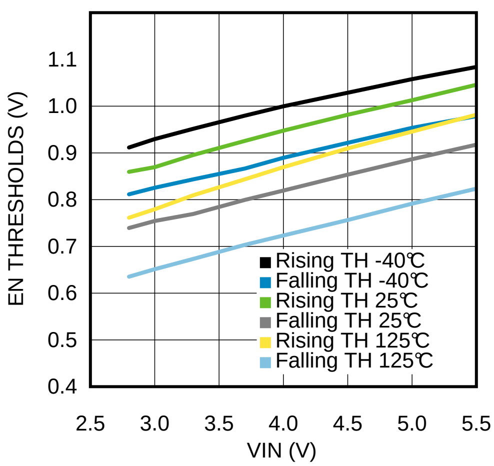
Maximum Load Current



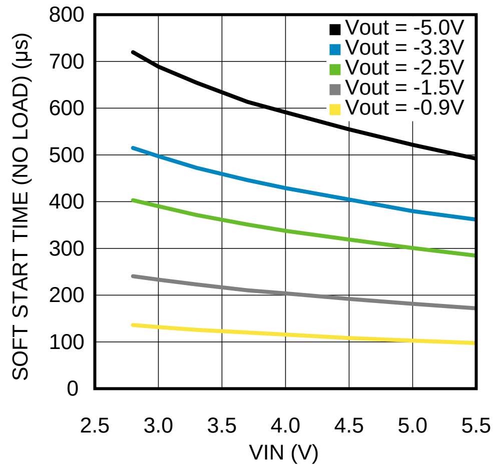
Minimum Switching Frequency



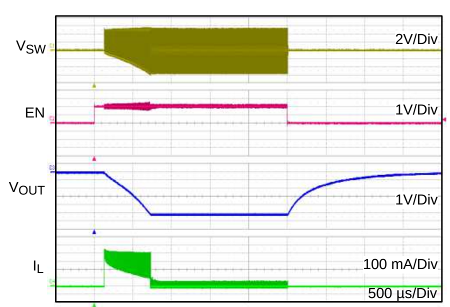
Enable Thresholds



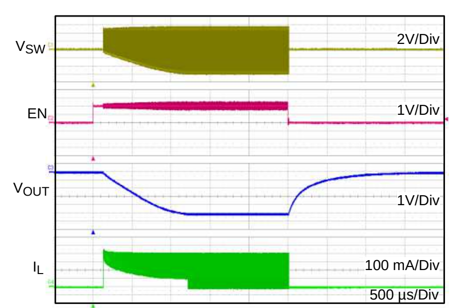
Soft Start Time (No Load)



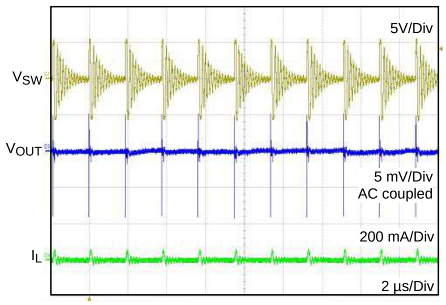
Soft Start And Soft Off Waveform
V_{IN} = 5.0 V, V_{OUT} = -5.0 V, No Load



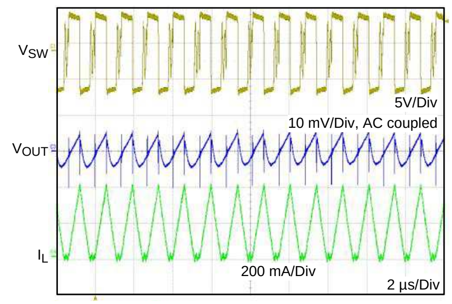
Soft Start And Soft Off Waveform
V_{IN} = 5.0 V, V_{OUT} = -5.0 V, Load = 50 Ω



Typical Switching Waveform
V_{IN} = 5.0 V, V_{OUT} = -5.0 V, No Load



Typical Switching Waveform
V_{IN} = 5.0 V, V_{OUT} = -5.0 V, I_{OUT} = 70 mA



13 Demo Board Layout

The LMR70503 Demo Board is a four layer board with two internal ground planes. The layout of the top and bottom layers is shown in the following figures.

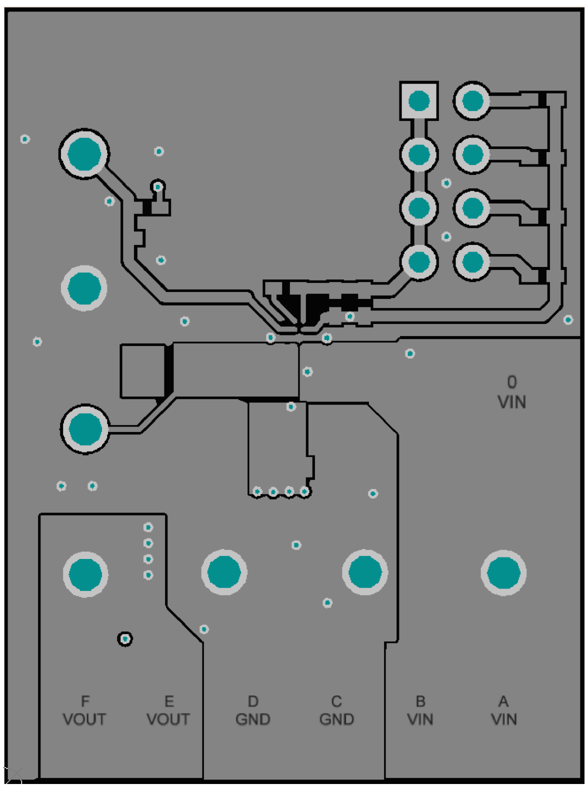


Figure 4. Top Layer

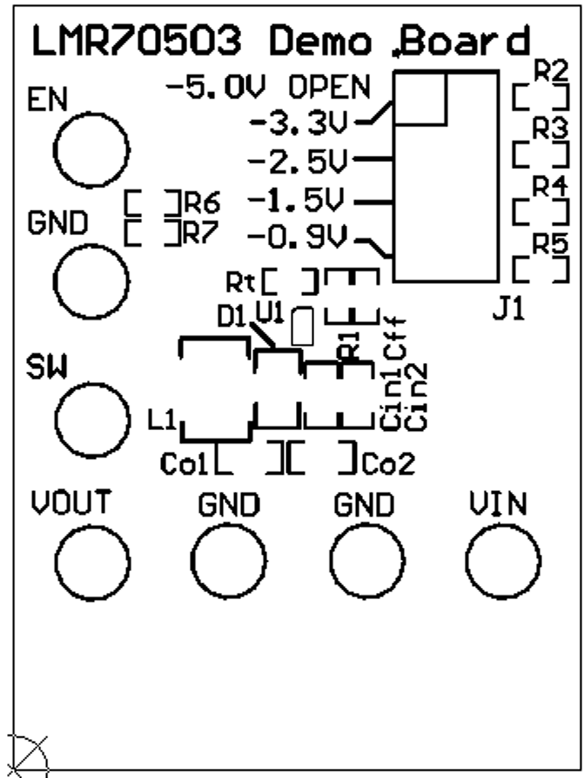


Figure 5. Top Overlay

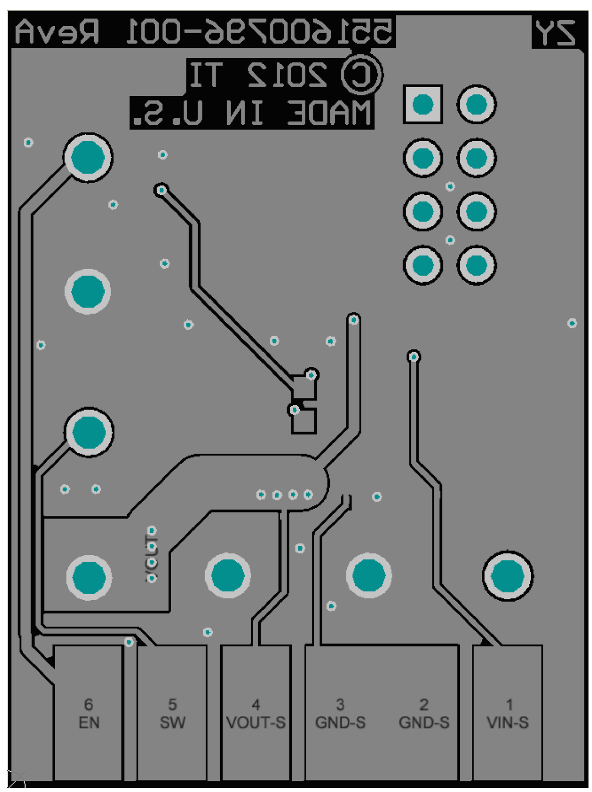


Figure 6. Bottom Layer

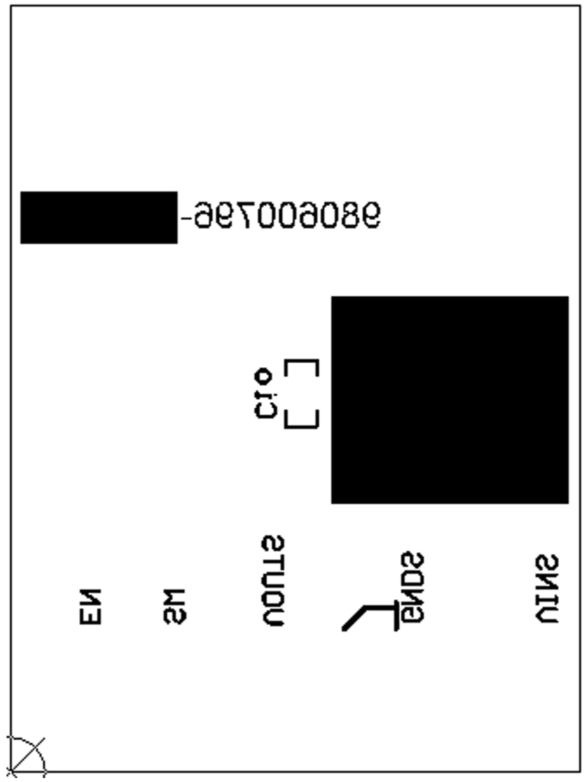


Figure 7. Bottom Overlay

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